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MAX22502E

100Mbps Full-Duplex RS-485/RS-422 Transceiver for Long Cables

General Description

The MAX22502E full-duplex, ESD-protected, RS-485/RS-422 transceiver is optimized for high-speed (up to 100Mbps) communication over long cables. This transceiver features larger receiver hysteresis for high noise rejection and improved signal integrity. Integrated preemphasis circuitry extends the distance, and increases the data rate, of reliable communication by reducing inter-symbol interference (ISI) caused by long cables when supplied with 5V. Integrated hot-swap protection and a fail-safe receiver ensure a logic-high on the receiver output when input signals are shorted or open for longer than 10 μ s (typ).

The MAX22502E is available in a 12-pin TDFN-EP (3mm x 3mm) package and operates over the -40°C to +125°C ambient temperature range.

Applications

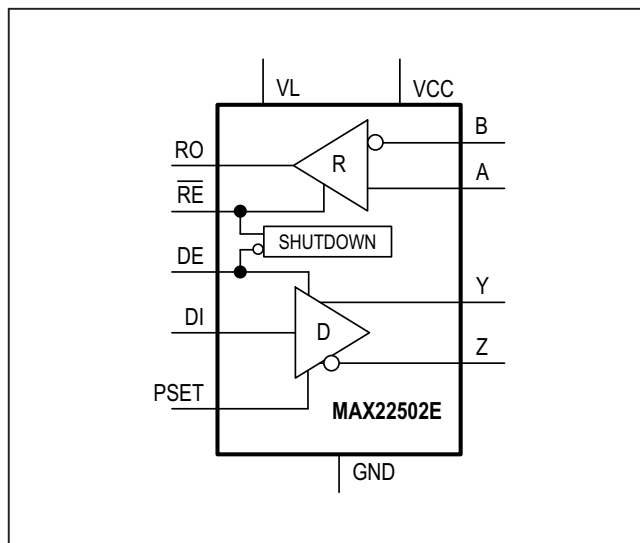
- Motion Control
- Encoder Interfaces
- Field Bus Networks
- Industrial Control Systems
- Backplane Busses

Benefits and Features

- High-Speed Operation Over Long Distances
 - Up to 100Mbps Data Rate
 - Integrated Preemphasis Extends Cable Length
 - High Receiver Sensitivity
 - Wide Receiver Bandwidth
 - Symmetrical Receiver Thresholds
- Integrated Protection Increases Robustness
 - -15V to +15V Common Mode Range
 - ± 15 kV ESD Protection (Human Body Model)
 - ± 7 kV IEC61000-4-2 Air-Gap ESD Protection
 - ± 6 kV IEC61000-4-2 Contact Discharge ESD Protection
 - Driver Outputs are Short-Circuit Protected
- Flexibility for Many Different Applications
 - 3V to 5.5V Supply Range
 - Low Voltage Logic Supply Down to 1.6V
 - Low 5 μ A (max) Shutdown Current
 - Available in 12-pin TDFN (3mm x 3mm) Package
 - -40°C to +125°C Operating Temperature Range

Ordering Information appears at end of data sheet.

Simplified Block Diagram



Absolute Maximum Ratings

V_{CC} -0.3 V to +6 V
 \overline{RE} , DE, DI, VL -0.3 V to +6 V
 RO -0.3 V to ($V_L + 0.3$) V
 $PSET$ -0.3 V to ($V_{CC} + 0.3$) V
A, B, Y, Z -15V to +15V
Short-Circuit Duration (RO , Y, Z) to GND
Continuous Power Dissipation (Single Layer Board
(derate 15.9mW/°C above +70°C)) 1269mW

Continuous Power Dissipation (Multilayer Board (derate
24.4mW/°C above +70°C)) 1951mW
Operating Temperature Range -40°C to +125°C
Junction Temperature +150°C
Storage Temperature Range -65°C to +150°C
Reflow Temperature +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN-EP

PACKAGE CODE	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	63°C/W
Junction to Case (θ_{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, V_L ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Supply Voltage	V _{CC}	Preemphasis disabled		3.0		5.5	V
		Preemphasis enabled		4.5	5	5.5	
Supply Current	I _{CC}	DE = high, $\overline{\text{RE}}$ = low, no load			12.7	16.5	mA
Shutdown Supply Current	I _{SHDN}	DE = low, $\overline{\text{RE}}$ = high				5	μA
Logic Supply Voltage	V _L			1.6		V _{CC}	V
Logic Supply Current	I _L	No load on RO			16.4	23	μA
DRIVER							
Differential Driver Output	V _{OD}	Figure 1, Figure 2	R _L = 54Ω	1.5			V
			R _L = 100Ω	2.0			
Differential Driver Preemphasis Ratio	D _{PRE}	Preemphasis enabled, 4.5V ≤ V _{CC} ≤ 5.5V (Note 3)	R _L = 54Ω	1.33	1.37	1.41	V/V
			R _L = 100Ω	1.33	1.37	1.41	
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	R _L = 54Ω, Figure 1 (Note 4)			0.2		V
Driver Common-Mode Output Voltage	V _{OC}	R _L = 54Ω, Normal mode and preemphasis, Figure 1			V _{CC} /2	3	V
Change In Magnitude of Common-Mode Voltage	ΔV _{OC}	R _L = 100Ω or 54Ω, Figure 1 (Note 4)			0.2		V
Single-Ended Driver Output High	V _{OH}	Y or Z output	I _{OUT} = -20mA	2.2			V
Single-Ended Driver Output Low	V _{OL}	Y or Z output	I _{OUT} = +20mA	0.8			V
Differential Output Capacitance	C _{OD}	DE = $\overline{\text{RE}}$ = high, f = 4MHz			50		pF
Driver Short-Circuit Output Current	I _{OST}	-15V ≤ V _{OUT} ≤ +15V			250		mA
RECEIVER							
Input Current (A and B)	I _{A,B}	DE = GND, V _{CC} = GND, +3.6V or 5.5V	V _{IN} = +12V	+1100			μA
			V _{IN} = -7V	-1000			
Differential Input Capacitance	C _{A,B}	Between A and B, DE = GND, f = 2MHz			50		pF
Common Mode Voltage Range	V _{CM}				-15	+15	V
Receiver Differential Threshold High	V _{TH_H}	-15V ≤ V _{CM} ≤ +15V			+50	+200	mV
Receiver Differential Threshold Low	V _{TH_L}	-15V ≤ V _{CM} ≤ +15V			-200	-50	mV
Receiver Input Hysteresis	ΔV _{TH}	V _{CM} = 0V, time from last transition is < t _{D_FS}			250		mV
Differential Input Fail-Safe Level	V _{TH_FS}	-15V ≤ V _{CM} ≤ +15V			-50	+50	mV

Electrical Characteristics (continued)(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, V_L ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INTERFACE (\overline{RE}, RO, DE, DI)						
Input Voltage High	V _{IH}	DE, DI, \overline{RE}	2/3 x V _L			V
Input Voltage Low	V _{IL}	DE, DI, \overline{RE}			1/3 x V _L	V
Input Current	I _{IN}	DI and DE, \overline{RE} (after first transition)	-2		+2	μA
Input Impedance on First Transition	R _{IN_FT}	DE, \overline{RE}			10	kΩ
RO Output Voltage High	V _{OH}	\overline{RE} = GND, (V _A - V _B) > 200mV, I _{OUT} = -1mA	V _L - 0.4			V
RO Output Low Voltage	V _{OL}	\overline{RE} = GND, (V _A - V _B) < -200mV, I _{OUT} = +1mA			0.4	V
Three-State Output Current at Receiver	I _{OZR}	\overline{RE} = high, 0 ≤ V _{RO} ≤ V _L	-1		+1	μA
PROTECTION						
Thermal Shutdown Threshold	T _{SH}			+160		°C
Thermal Shutdown Hysteresis	T _{SH_HYS}			10		°C
ESD Protection (A and B Pins)		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap Discharge to GND		±7		
		IEC61000-4-2 Contact Discharge to GND		±6		
ESD Protection (All Other Pins)		Human Body Model		±2		kV

Electrical Characteristics - Switching(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, V_L ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Note 1, 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER (Note 5)						
Driver Propagation Delay	t _{DPLH}	R _L = 54Ω, C _L = 50pF, Figures 3, 4			20	ns
	t _{DPHL}	R _L = 54Ω, C _L = 50pF, Figures 3, 4			20	
Differential Driver Output Skew	t _{DSKEW}	t _{DPLH} - t _{DPHL} , R _L = 54Ω, C _L = 50pF, Figure 3 , Figure 4 (Note 6)	V _L = V _{CC} , V _{CC} ≥ 3V		1.2	ns
		t _{DPLH} - t _{DPHL} , R _L = 54Ω, C _L = 50pF, Figure 3 , Figure 4 (Note 6)	V _L does not equal V _{CC}		1.6	
Driver Differential Output Rise and Fall Time	t _{HL} , t _{LH}	R _L = 54Ω, C _L = 50pF, Figure 4 (Note 6)			3	ns
Data Rate	DR				100	Mbps

Electrical Characteristics - Switching (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC}, V_L ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted (Note 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Enable to Output High	t _{DZH}	R _L = 500Ω, C _L = 50pF, Figure 5 , Figure 6				30	ns
Driver Enable to Output Low	t _{DZL}	R _L = 500Ω, C _L = 50pF, Figure 5 , Figure 6				30	ns
Driver Disable Time from Low	t _{DLZ}	R _L = 500Ω, C _L = 50pF, Figure 5 , Figure 6				30	ns
Driver Disable Time from High	t _{DHZ}	R _L = 500Ω, C _L = 50pF, Figure 5 , Figure 6				30	ns
Driver Enable from Shutdown to Output High	t _{DZH} (SHDN)	R _L = 1kΩ, C _L = 15pF, Figure 5 , Figure 6				100	μs
Driver Enable from Shutdown to Output Low	t _{DZL} (SHDN)	R _L = 1kΩ, C _L = 15pF, Figure 5 , Figure 6				100	μs
Time to Shutdown	t _{SHDN}	(Note 7, Note 8)		50		800	ns
Driver Preemphasis Interval	t _{PRE}	4.5V ≤ V _{CC} ≤ 5.5V, Figure 2	R _{PSET} = 4kΩ	10	13	16	ns
			R _{PSET} = 400kΩ	0.8	1	1.2	μs
RECEIVER (Note 5)							
Delay to Fail-Safe Operation	t _{D_FS}			10			μs
Receiver Propagation Delay	t _{RPLH}	C _L = 15pF, Figure 7 , Figure 8				20	ns
	t _{RPHL}	C _L = 15pF, Figure 7 , Figure 8				20	
Receiver Output Skew	t _{RSKEW}	t _{RPHL} - t _{RPLH} , C _L = 15pF, Figure 7 , Figure 8				2.5	ns
Data Rate	DR					100	Mbps
Receiver Enable to Output High	t _{RZH}	R _L = 1kΩ, C _L = 15pF, Figure 9				30	ns
Receiver Enable to Output Low	t _{RZL}	R _L = 1kΩ, C _L = 15pF, Figure 9				30	ns
Receiver Disable Time from Low	t _{RLZ}	R _L = 1kΩ, C _L = 15pF, Figure 9				30	ns
Receiver Disable Time from High	t _{RHZ}	R _L = 1kΩ, C _L = 15pF, Figure 9				30	ns
Receiver Enable from Shutdown to Output High	t _{RZH} (SHDN)	R _L = 1kΩ, C _L = 15pF, Figure 9				100	μs
Receiver Enable from Shutdown to Output Low	t _{RZL} (SHDN)	R _L = 1kΩ, C _L = 15pF, Figure 9				100	μs
Time to Shutdown	t _{SHDN}	(Note 7, Note 8)		50		800	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.**Note 2:** All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.**Note 3:** V_{ODP} is the differential voltage between Y and Z during the preemphasis interval and is the differential voltage when preemphasis is disabled. V_{ODP} = D_{PRE} × V_{OD}.**Note 4:** ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.**Note 5:** Capacitive load includes test probe and fixture capacitance.**Note 6:** Not production tested. Guaranteed by design.**Note 7:** Shutdown is enabled by driving $\overline{\text{RE}}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.**Note 8:** The timing parameter refers to the driver or receiver enable delay, when the device has exited the initial hot-swap protect state and is in normal operating mode.

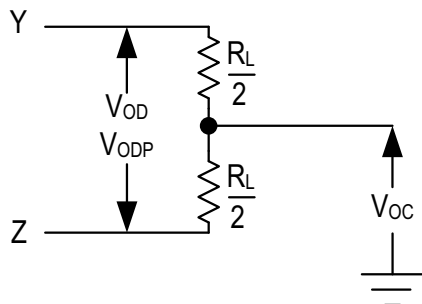


Figure 1. Driver DC Test Load

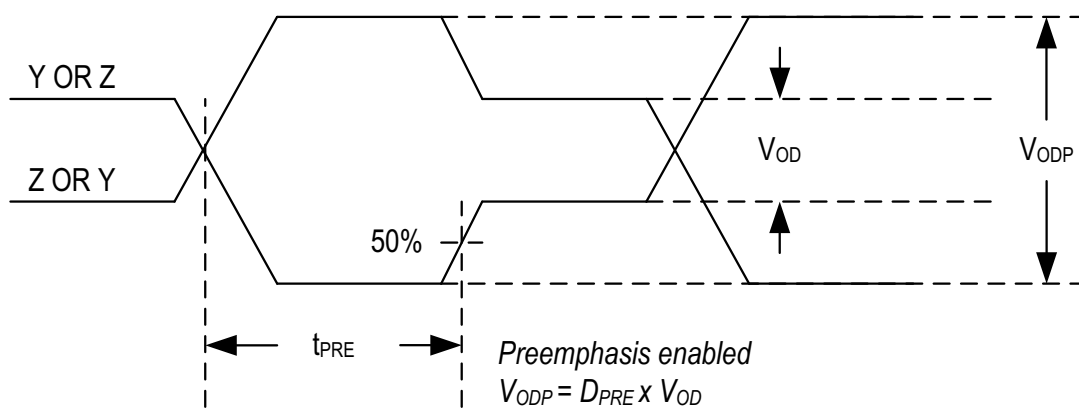


Figure 2. Driver Preemphasis Timing

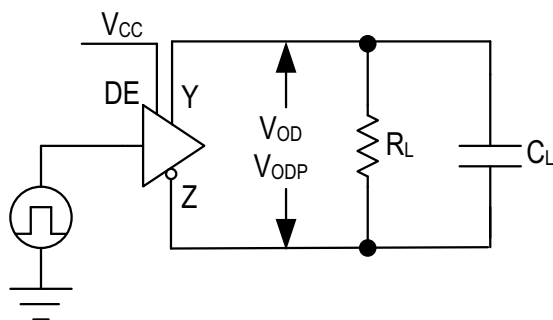


Figure 3. Driver Timing Test Circuit



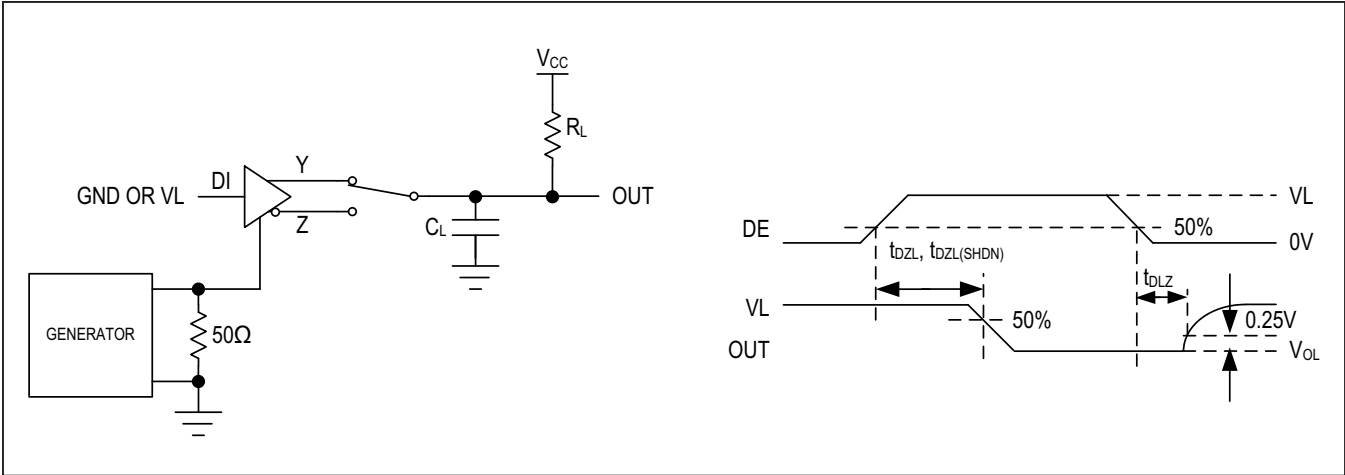


Figure 6. Driver Enable and Disable Times (t_{DZL} , t_{DLZ})

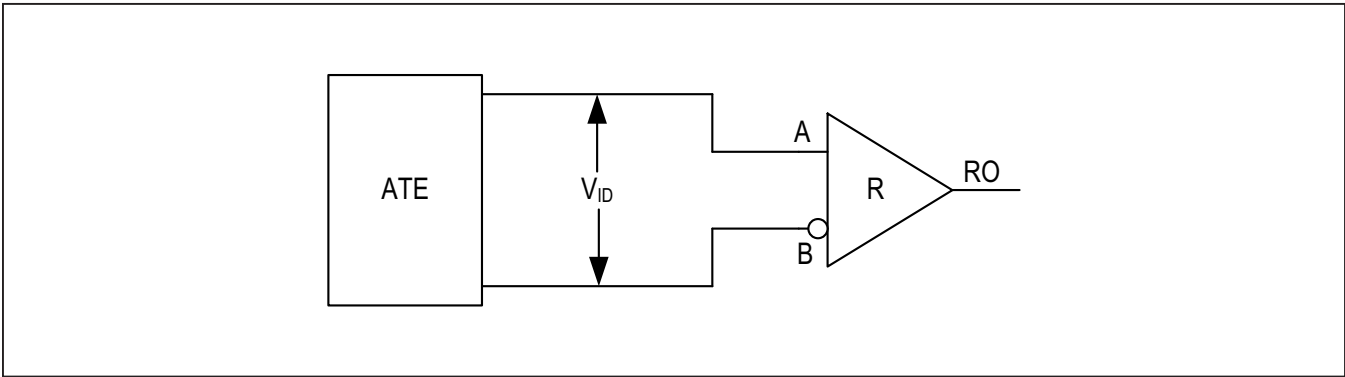


Figure 7. Receiver Propagation Delay Test Circuit

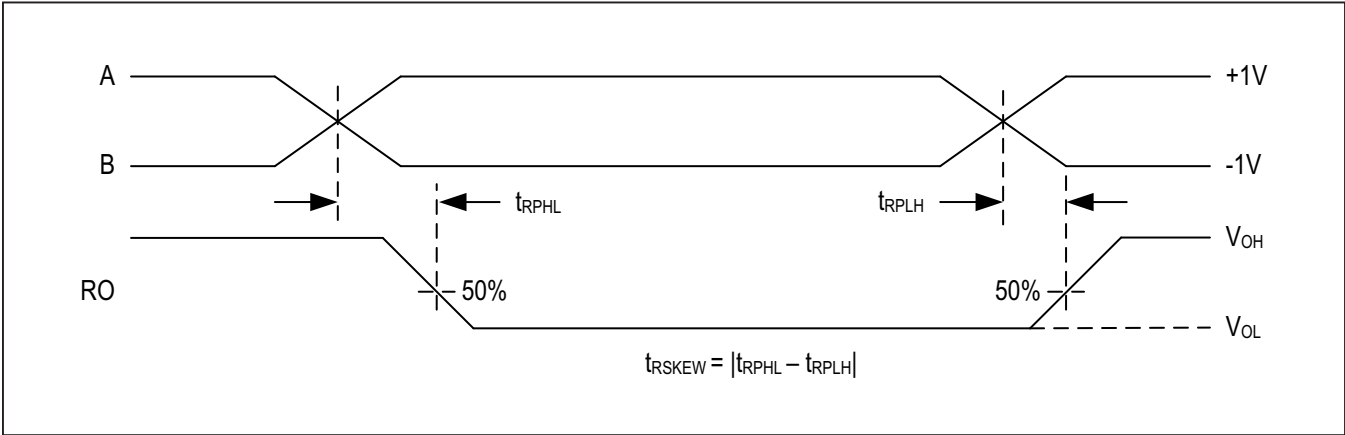


Figure 8. Receiver Propagation Delays

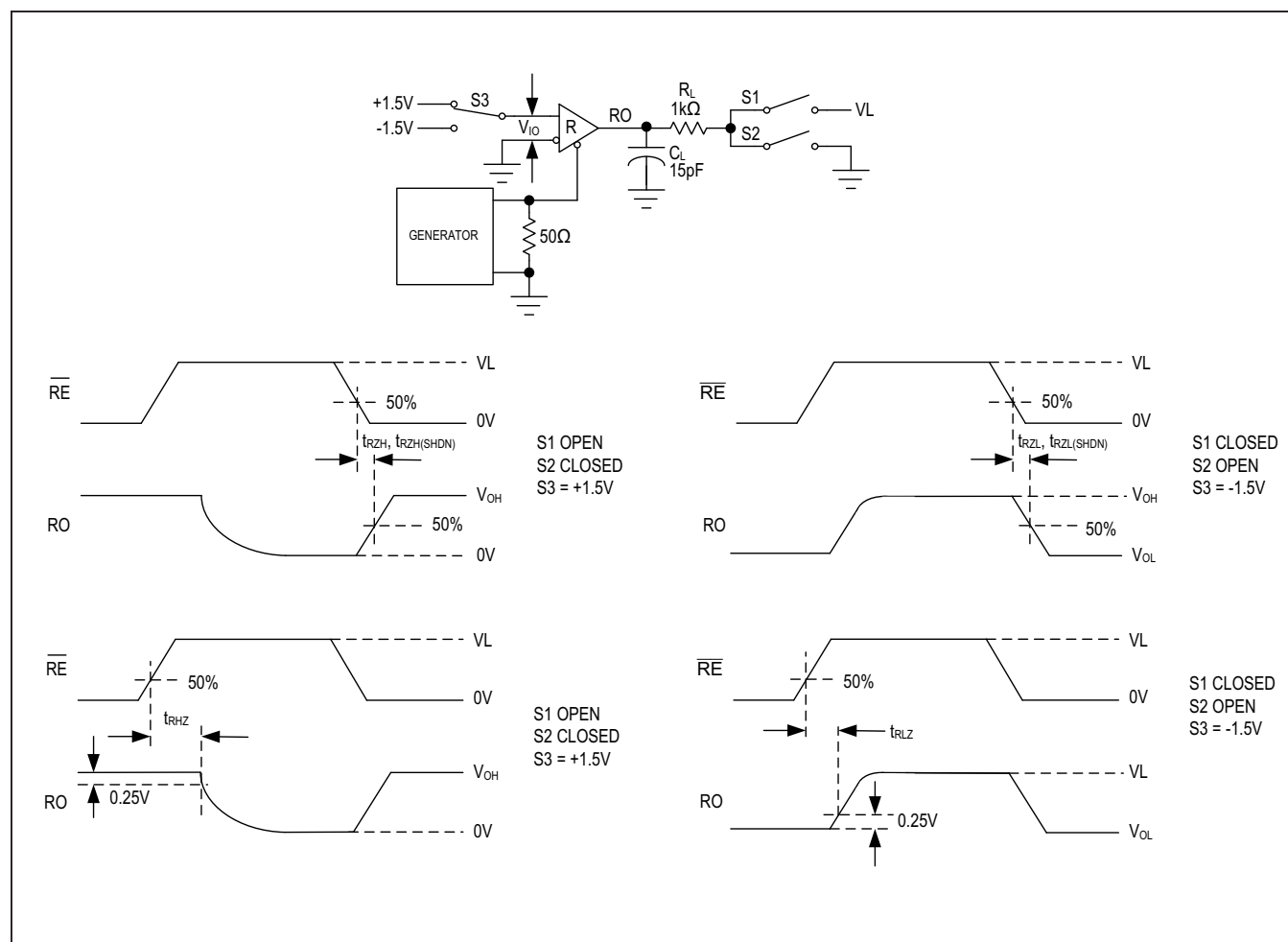
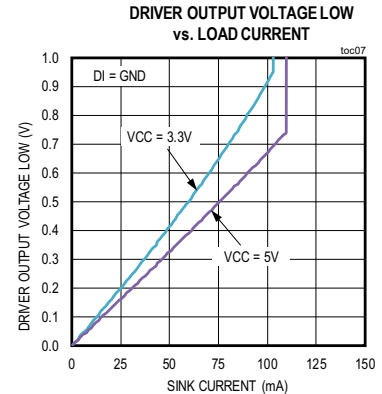
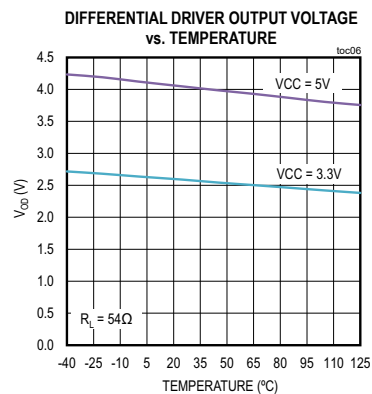
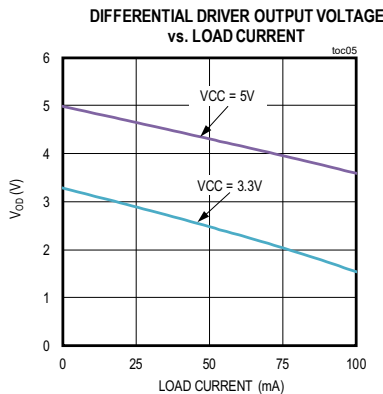
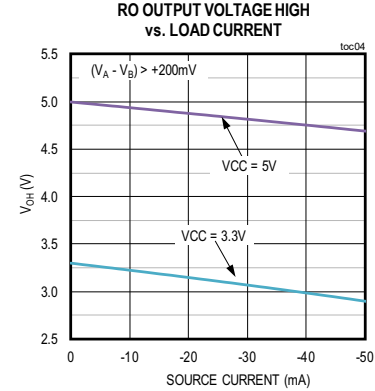
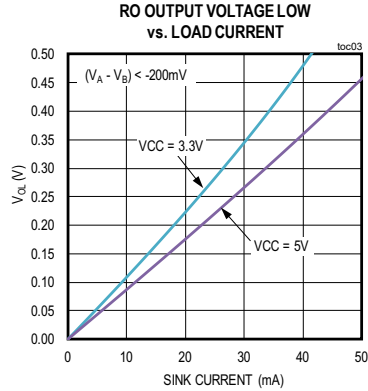
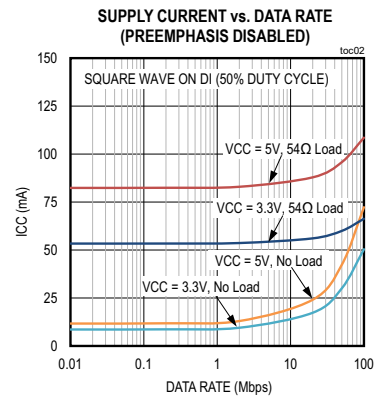
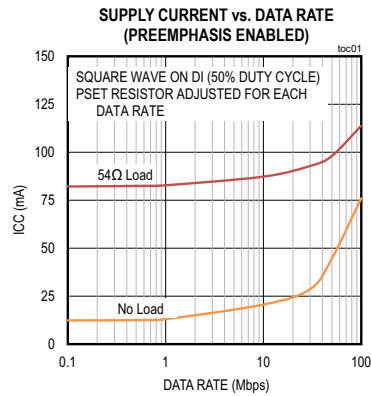


Figure 9. Receiver Enable and Disable Times

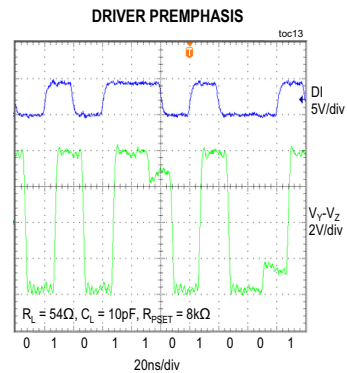
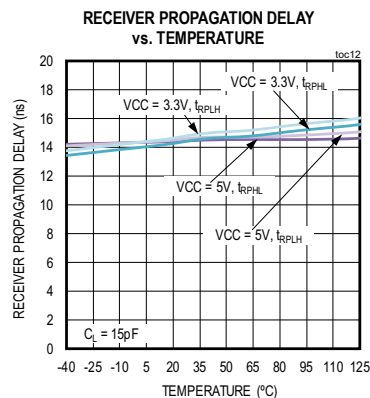
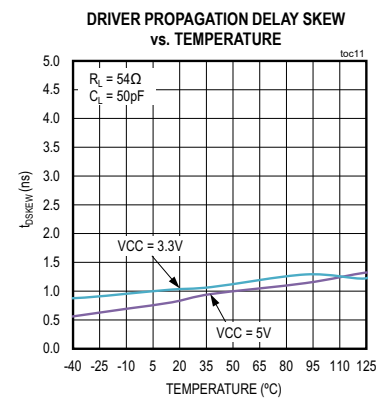
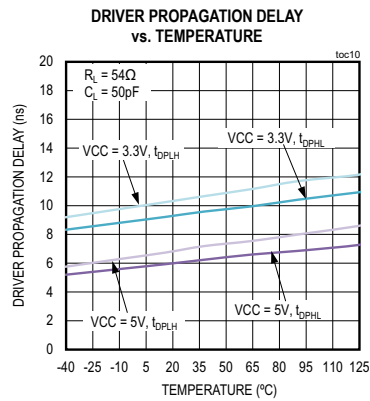
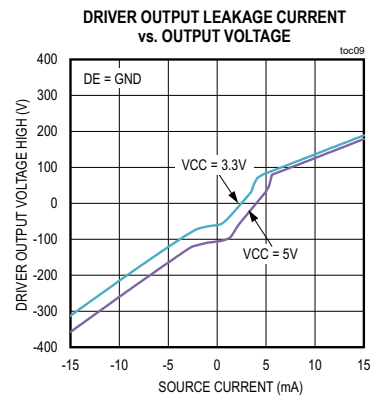
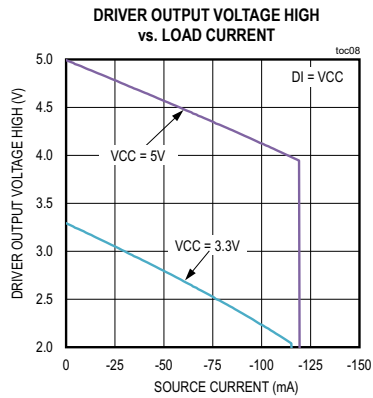
Typical Operating Characteristics

$V_{CC} = 5V$, $V_L = V_{CC}$, 60 Ω termination between Y and Z, $T_A = 25^\circ C$, unless otherwise noted.



Typical Operating Characteristics (continued)

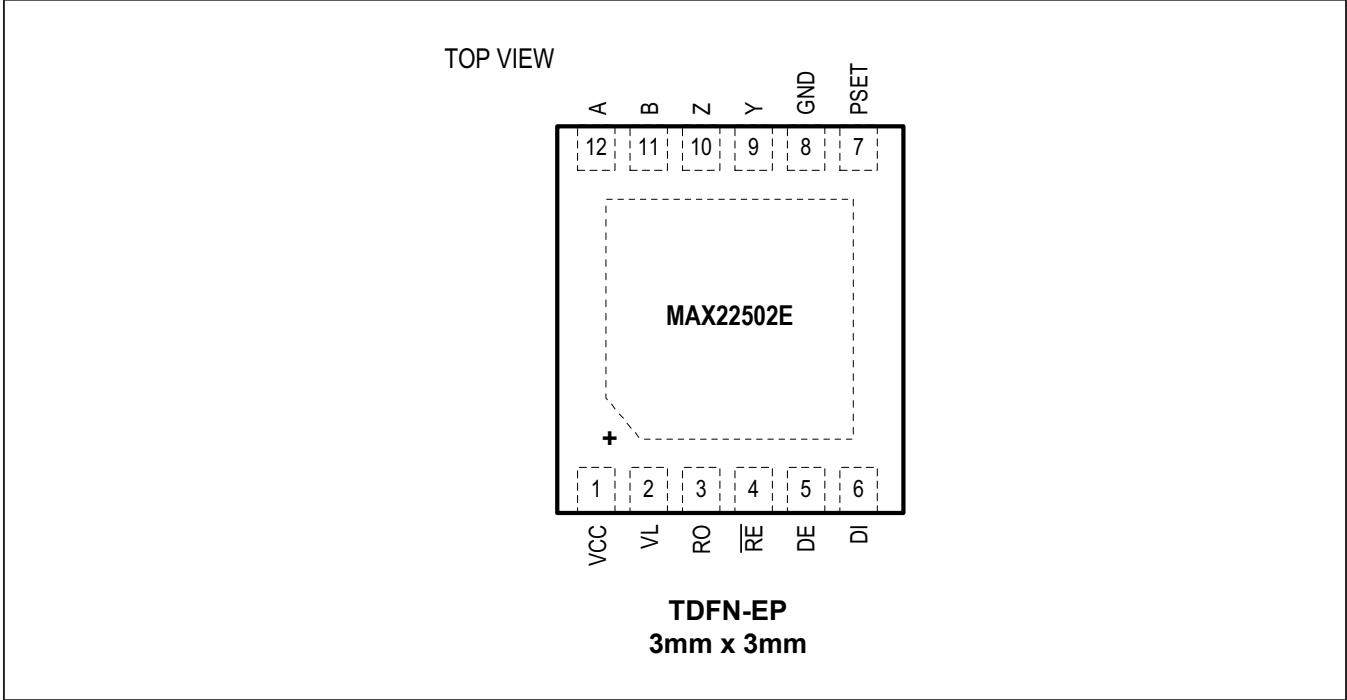
$V_{CC} = 5V$, $V_L = V_{CC}$, 60 Ω termination between Y and Z, $T_A = 25^\circ C$, unless otherwise noted.



MAX22502E

100Mbps Full-Duplex RS-485/RS-422 Transceiver for Long Cables

Pin Configuration



Pin Description

MAX22502E

PIN	NAME	FUNCTION
1	V _{CC}	Supply Input. Bypass V _{CC} to ground with a 0.1μF ceramic capacitor as close to the device as possible.
2	V _L	Logic Supply Input. V _L defines the interface logic levels on DE, DI, and RO. Apply a voltage between 1.6V to 5.5V to V _L . Ensure that V _L ≤ V _{CC} for normal operation. Bypass V _L to ground with a 0.1μF capacitor as close to the device as possible.
3	RO	Receiver Output. See the Receiving Function Table for more information.
4	RE	Receiver Enable. Set RE high to disable the receiver and tri-state RO. The device is in low-power shutdown when RE = high and DE = low.
5	DE	Driver Output Enable. Set DE high to enable driver. Set DE low to three-state the driver output.
6	DI	Driver Input. See the Transmitting Function Table for more information.
7	PSET	Preemphasis Select Control Input. Connect a resistor from PSET to GND to select the preemphasis duration. See the Layout Recommendations in the Applications Information section for more information. To disable preemphasis, connect PSET to GND or V _{CC} .
8	GND	Ground
9	Y	Noninverting Driver Output
10	Z	Inverting Driver Output
11	B	Inverting Receiver Input
12	A	Noninverting Receiver Input

MAX22502E

100Mbps Full-Duplex RS-485/RS-422
Transceiver for Long Cables

Functional Diagrams

Transmitting Function Table

INPUTS			OUTPUTS	
RE	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown. Y and Z are high-impedance	

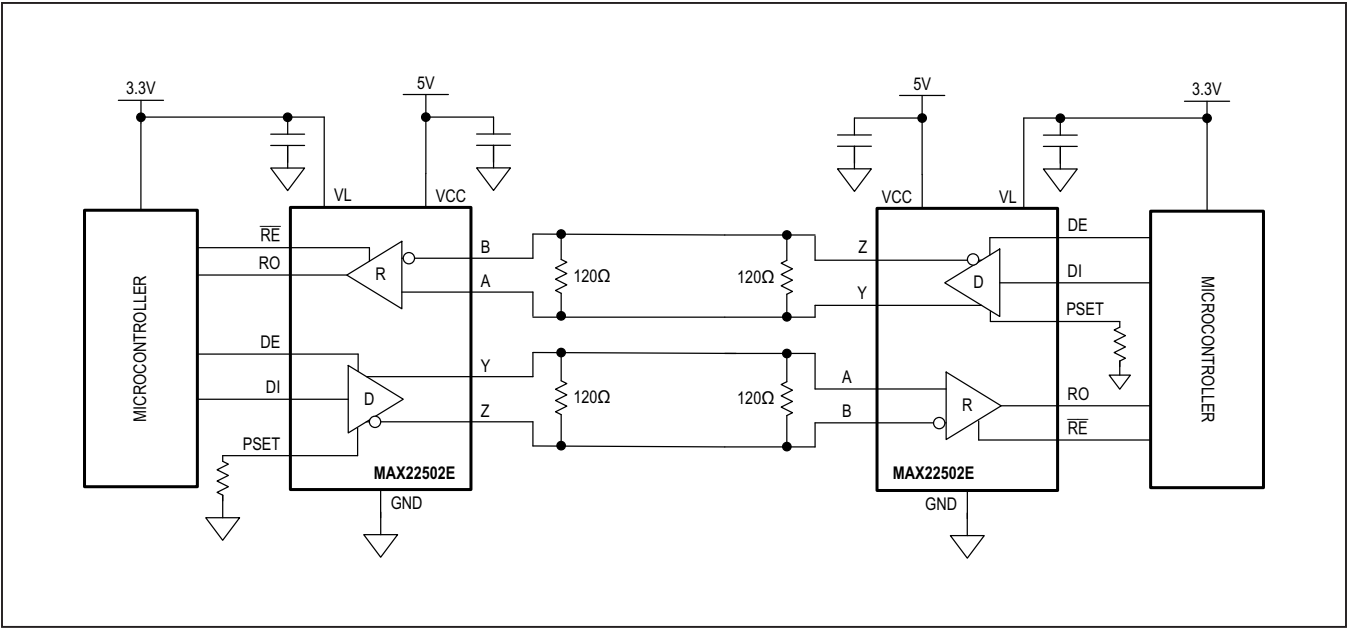
X = Don't care

Receiving Function Table

INPUTS				OUTPUTS
RE	DE	(V _A - V _B)	Time from Last A-B Transition	RO
0	X	≥ V _{TH_H}	Always	1
0	X	V _{TH_L} < (V _A - V _B) < V _{TH_H}	< t _{D_FS}	Indeterminate RO is latched to previous value
0	X	-50mV < (V _A - V _B) < +50mV	> t _{D_FS}	1
0	X	≤ V _{TH_L}	Always	0
0	X	Open/Shorted	> t _{D_FS}	1
1	1	X	X	High Impedance
1	0	X	X	Shutdown. RO is high-impedance

X = Don't care

Full-Duplex Point-to-Point Application Circuit



Detailed Description

The MAX22502E ESD-protected RS-485/RS-422 transceiver is optimized for high-speed, full-duplex communications over long cables. This transceiver features integrated hot-swap functionality to eliminate false transitions on the driver during power-up or during a hot-plug event. Fail-safe receiver inputs guarantee a logic-high on the receiver output when inputs are shorted or open for longer than 10 μ s (typ).

Receiver Threshold Voltages

The MAX22502E receiver features a large threshold hysteresis of 250mV (typ) for increased differential noise rejection.

Additionally, the receiver features symmetrical threshold voltages. Symmetric thresholds have the advantage that recovered data at the RO output does not have duty cycle distortion. Typically, fail-safe receivers, which have unipolar (non-symmetric) thresholds, show some duty cycle distortion at high signal attenuation due to long cable lengths.

Preemphasis

When powered by 5V, the MAX22502E features integrated driver preemphasis circuitry, which strongly improves signal integrity at high data rates over long distances by reducing intersymbol interference (ISI) caused by long cables. Preemphasis is set by connecting a resistor (R_{PSET}) between PSET and ground.

Long cables attenuate the high-frequency content of transmitted signals due to the cable's limited bandwidth. This causes signal/pulse distortion at the receiving end, resulting in ISI. ISI causes jitter in data and clock recovery circuits. ISI can be visualized by considering the following cases: If a series of ones (1s) is transmitted, followed by a zero (0), the transmission-line voltage has risen to a high value by the end of the string of ones. It takes longer for the signal to move toward the '0' state because the starting voltage on the line is so far from the zero crossing. Similarly, if a data pattern has a string of zeros followed by a one and then another zero, the one-to-zero transition starts from a voltage that is much closer to the zero crossing ($V_Y - V_Z = 0$) and it takes much less time for the signal to reach the zero crossing.

Preemphasis reduces ISI by boosting the differential signal amplitude at every transition edge, counteracting the high frequency attenuation of the cable. When the DI input changes from a logic low to a logic high, the differential output ($V_Y - V_Z$) is driven high to V_{ODP} . At the end of the preemphasis interval, the differential voltage returns to a lower level (V_{OD}). The preemphasis differential high voltage (V_{ODP}) is typically 1.37 times the V_{OD} voltage.

If DI switches back to a logic-low state before the preemphasis interval ends, the differential output switches directly from the 'strong' V_{ODP} high to a 'strong' low ($-V_{ODP}$).

Driver behavior is similar when the DI input changes from a logic-high to a logic-low. When this occurs, the differential output is pulled low to $-V_{ODP}$ until the end of the preemphasis interval, at which point $V_Y - V_Z = -V_{ODP}$.

Preemphasis Setting

Connect a resistor (R_{PSET}) between PSET and GND to set the preemphasis time interval on the MAX22502E. An optimum preemphasis interval ranges from 1 to 1.5 unit intervals (bit time). Use the following equation to calculate the resistance needed on PSET to achieve a 1.2 preemphasis interval:

$$R_{PSET} = 400 \times 10^9 / DR$$

where DR is the data rate and $1\text{Mbps} \leq DR \leq 100\text{Mbps}$.

Preemphasis only minimally degrades the jitter on the eye diagram when using short cables, making it reasonable to permanently enable preemphasis on systems where cable lengths may vary or change. [Figure 10](#) and [Figure 11](#) are eye diagrams taken at 100Mbps over a 10m cat5e cable. Note that the eye varies only slightly as preemphasis is enabled or disabled.

[Figure 12](#) and [Figure 13](#) show the driver eye diagrams over a long cable length. The MAX22502E was used as the driver and the eye diagrams were taken at the receiver input after a length of 100m cat5e cable. [Figure 12](#) shows the signal at the receiver when the driver preemphasis is disabled. [Figure 13](#) shows the receiver signal when preemphasis is enabled.

Fail-Safe Functionality

The MAX22502E features fail-safe receiver inputs, guaranteeing a logic-high on the receiver output (RO) when the receiver inputs are shorted or open for longer than 10 μ s (typ). When the differential receiver input voltage is less than 50mV for more than 10 μ s (typ), RO is logic-high. For example, in the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination resistor, so $(V_A - V_B = 0V) > -50\text{mV}$ and RO is guaranteed to be a logic-high after 10 μ s (typ).

Driver Single-Ended Operation

The Y and Z outputs on the MAX22502E can be used in the standard differential operating mode or as single-ended outputs. Because the driver outputs swing rail-to-rail, they can also be used as individual standard TTL logic outputs.

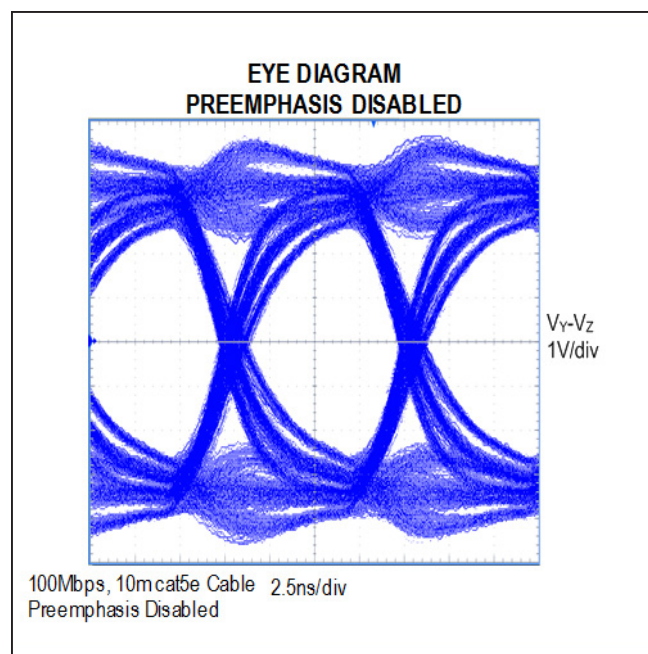


Figure 10. Eye Diagram, 100Mbps Over 10m Cat5e Cable, Preemphasis Disabled, $V_{CC} = V_L = 5V$

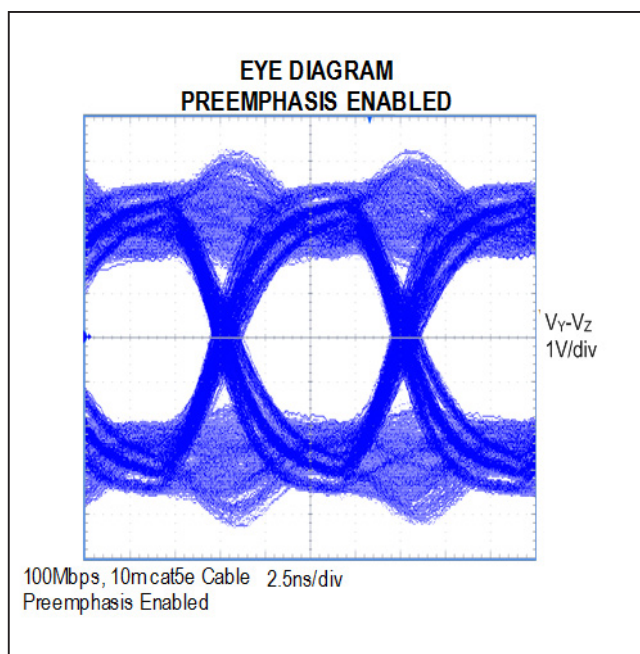


Figure 11. Eye Diagram, 100Mbps Over 10m Cat5e Cable, Preemphasis Enabled, $V_{CC} = V_L = 5V$

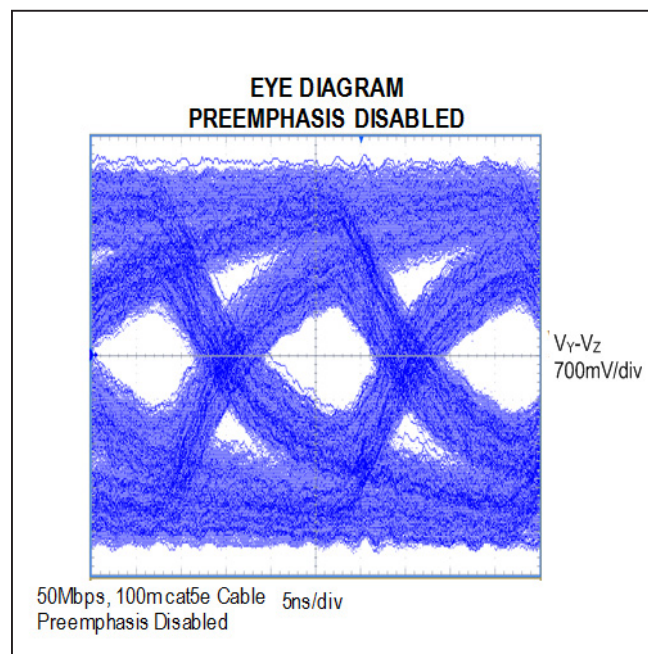


Figure 12. Eye Diagram, 50Mbps Over 100m Cat5e Cable, Preemphasis Disabled, $V_{CC} = V_L = 5V$

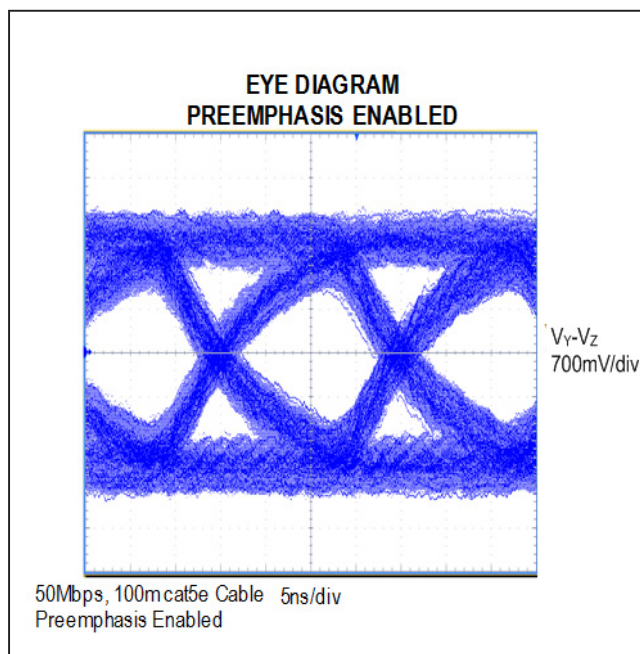


Figure 13. Eye Diagram, 50Mbps Over 100m Cat5e Cable, Preemphasis Enabled, $V_{CC} = V_L = 5V$

Hot-Swap Capability

The DE and $\overline{\text{RE}}$ enable inputs feature hot-swap functionality. At each input there are two NMOS devices, M1 and M2 (Figure 14). When V_{CC} ramps from zero, an internal 10ms timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 500 μA current sink, and M1, a 100 μA current sink, pull DE to GND through a 5k Ω resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10 μs , the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

There is a complimentary circuit for $\overline{\text{RE}}$ that uses two PMOS devices to pull RE to V_{CC} .

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

The MAX22502E features low-power shutdown mode to reduce supply current when the transceiver is not needed. Pull the $\overline{\text{RE}}$ input high and the DE input low to put the device in low-power shutdown mode. If the inputs are in this state for at least 800ns, the part is guaranteed to enter shutdown. The MAX22502E draws 5 μA (max) of supply current when the device is in shutdown.

The $\overline{\text{RE}}$ and DE inputs can be driven simultaneously. The MAX22502E is guaranteed not to enter shutdown if $\overline{\text{RE}}$ is high and DE is low for less than 50ns.

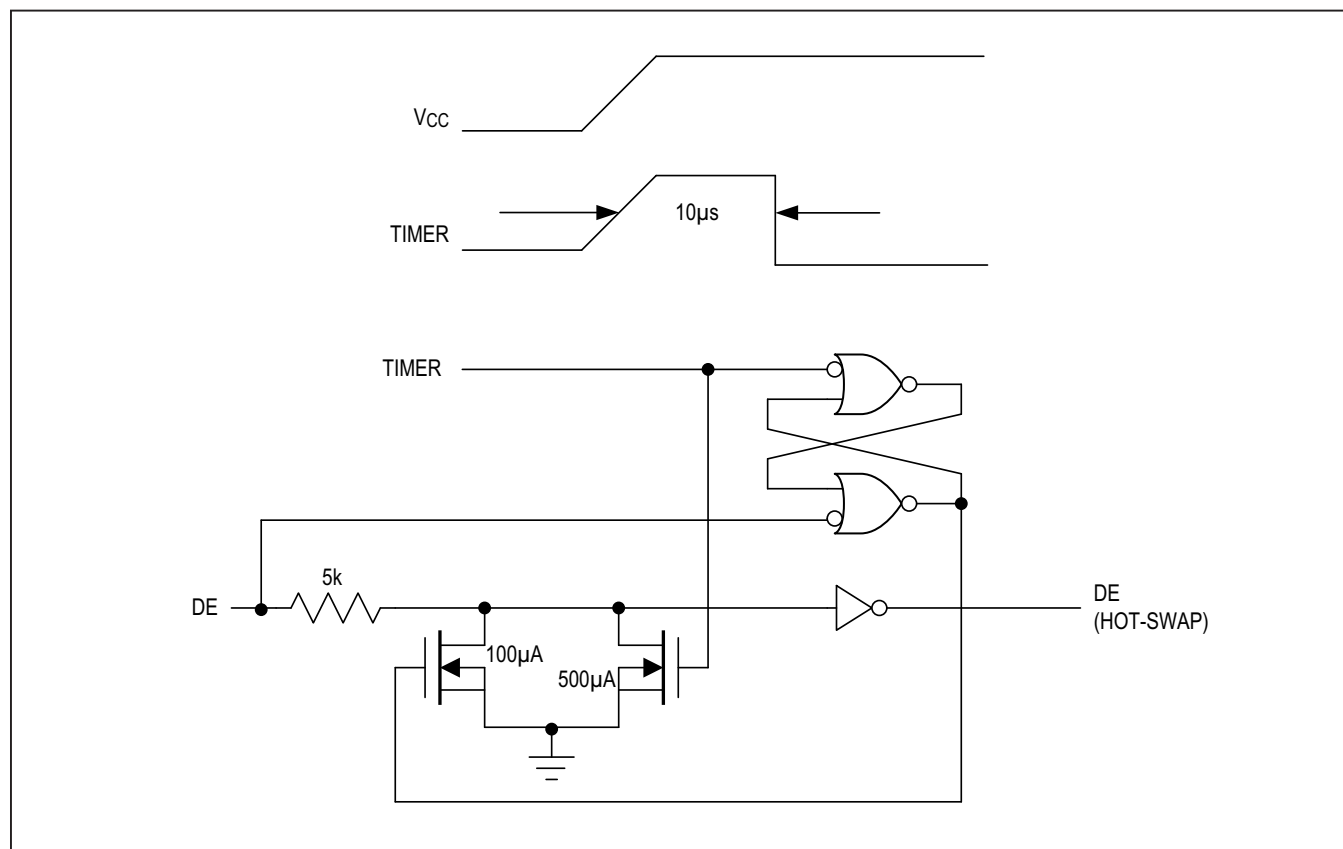


Figure 14. Simplified Structure of the Driver Enable (DE) Pin

Applications Information

Powering the MAX22502E

No particular power supply sequencing is required for the MAX22502 V_{CC} and V_L supplies during power-up. However, ensure that $V_L \leq V_{CC}$ for normal operation.

Layout Recommendations

Ensure that the preemphasis set resistor (R_{PSET}) is located close to the PSET and GND pins in order to minimize interference by other signals. Minimize the trace length to the PSET resistor. Additionally, place a ground plane under R_{PSET} and surround it with ground connections/traces to minimize interference from the A and B switching signals. See [Figure 15](#).

Network Topology

The MAX22502E transceiver is designed for high-speed bidirectional RS-485/RS-422 data communications. Multidrop networks can cause impedance discontinuities which affect signal integrity. Maxim recommends using a point-to-point network topology, instead of a multidrop topology, when communicating with high data rates. Terminate the transmission line at both ends with the cable's characteristic impedance to reduce reflections.

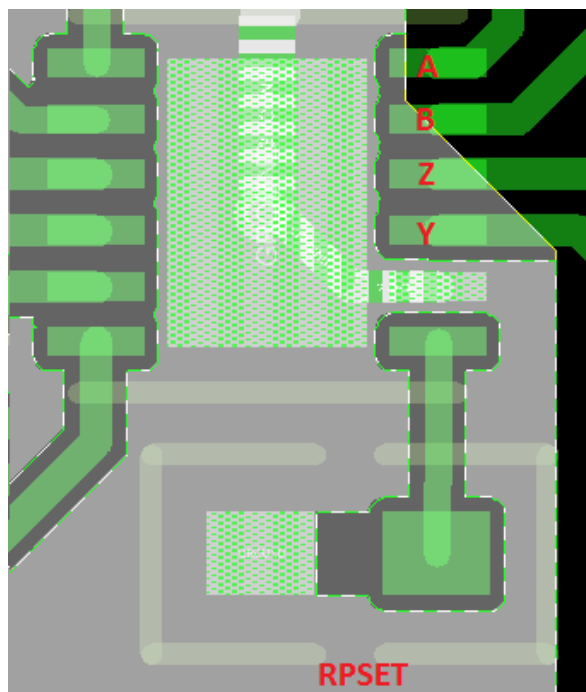


Figure 15. Sample PSET Resistor Placement

MAX22502E

100Mbps Full-Duplex RS-485/RS-422
Transceiver for Long Cables

Ordering Information

PART	PREEMPHASIS	LOGIC SUPPLY	PIN-PACKAGE	PACKAGE CODE
MAX22502EATC+	Y	Y	TDFN12-EP*	TD1233+1C
MAX22502EATC+T	Y	Y	TDFN12-EP*	TD1233+1C

+Denotes a lead (Pb)-free/RoHS-compliant package.

*EP = Exposed Pad

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/17	Initial release	—
1	4/19	Corrected part references in the text	14, 17
.1		Corrected typo in Figure 8	8

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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