CS5166

5-Bit Synchronous CPU Controller with Power Good and Current Limit

The CS5166 is a synchronous dual NFET buck controller. It is designed to power the core logic of the latest high performance CPUs. It uses V^{2}™ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and power system. The CS5166 provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS5166 is specifically designed to power Intel's Pentium®II processor and includes the following features: 5−bit DAC with 1.0% tolerance, Power Good output, adjustable hiccup mode overcurrent protection, V_{CC} monitor, Soft Start, adaptive voltage positioning, overvoltage protection, remote sense and current sharing capability.

The CS5166 will operate over a 4.15 to 14 V range using either single or dual input voltage and is available in a 16 lead wide body surface mount package.

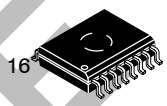
Features

- V^2 Control Topology
- Dual N−Channel Design
- 125 ns Controller Transient Response
- Excess of 1.0 MHz Operation
- 5−Bit DAC with 1.0% Tolerance
- Power Good Output With Internal Delay
- Adjustable Hiccup Mode Overcurrent Protection
- Complete Pentium II System Requires Just 21 Components
- 5.0 V & 12 V Operation
- Adaptive Voltage Positioning
- Remote Sense Capability
- Current Sharing Capability
- V_{CC} Monitor
- Overvoltage Protection (OVP)
- Programmable Soft Start
- 200 ns PWM Blanking
- 65 ns FET Nonoverlap Time
- 40 ns Gate Rise and Fall Times (3.3 nF Load)

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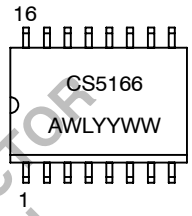
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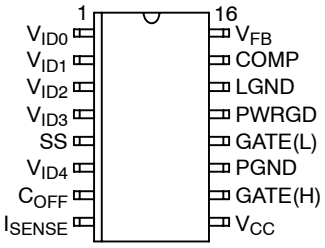
SO−16L
DW SUFFIX
CASE 751G

MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5166GDW16	SO−16L	46 Units/Rail
CS5166GDWR16	SO−16L	1000 Tape & Reel

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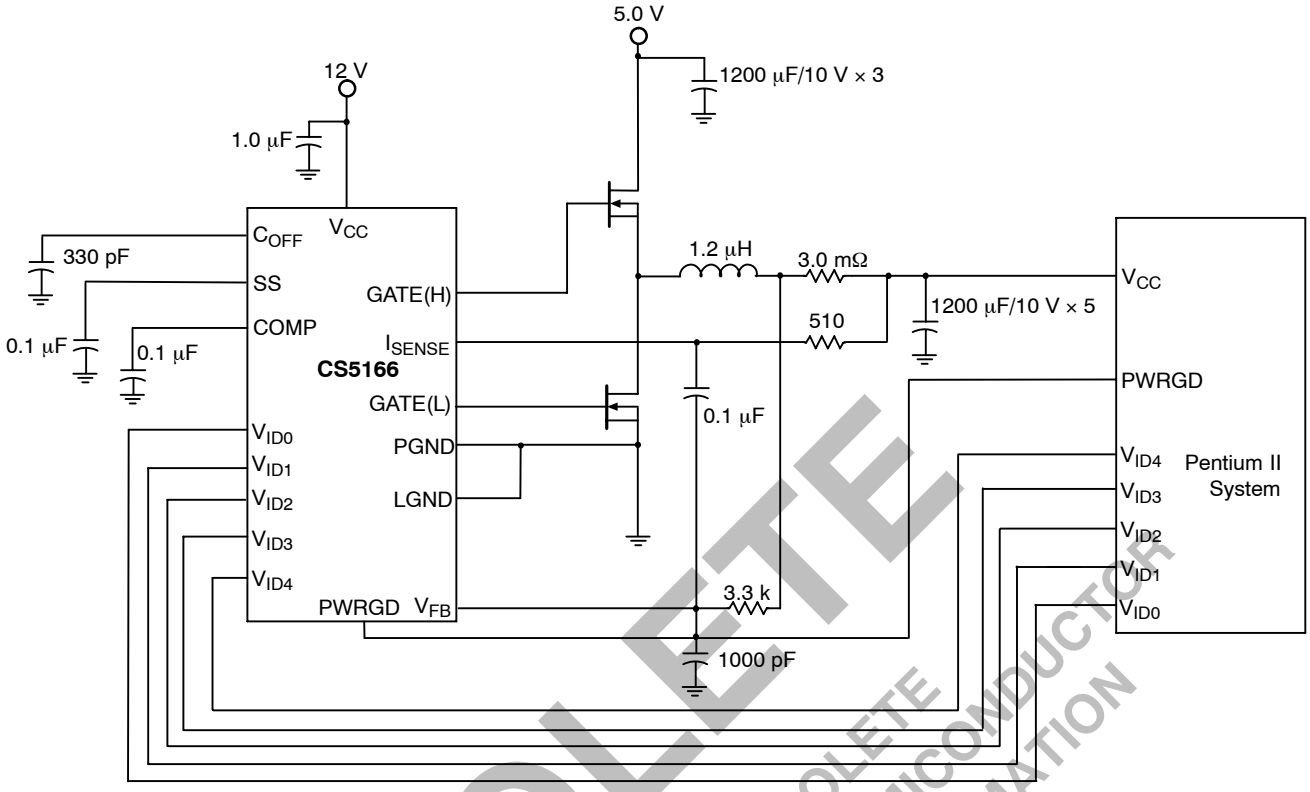


Figure 1. Application Diagram, 5.0 V to 2.8 V @ 14.2 A for 300 MHz Pentium II

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ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	0 to 150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, T_S	−65 to +150	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	16 V	−0.3 V	N/A	1.5 A peak, 200 mA DC
Soft Start Capacitor	SS	6.0 V	−0.3 V	200 μA	10 μA
Compensation Capacitor	COMP	6.0 V	−0.3 V	10 mA	1.0 mA
Voltage Feedback and Current Sense Comparator Input	V_{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Off−Time Capacitor	C_{OFF}	6.0 V	−0.3 V	1.0 mA	50 mA
Voltage ID DAC Inputs	V_{ID0}−V_{ID4}	6.0 V	−0.3 V	1.0 mA	10 μA
High−Side FET Driver	GATE(H)	16 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
Low−Side FET Driver	GATE(L)	16 V	−0.3 V	1.5 A peak, 200 mA DC	1.5 A peak, 200 mA DC
Current Sense Comparator Input	I_{SENSE}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Power Good Output	PWRGD	6.0 V	−0.3 V	10 μA	30 mA
Power Ground	PGND	0 V	0 V	1.5 A peak, 200 mA DC	N/A
Logic Ground	LGND	0 V	0 V	100 mA	N/A

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.0 DAC Code: ($V_{ID4} = V_{ID3} = V_{ID2} = V_{ID1} = 0$); $C_{GATE(H)} = C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1$ μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
V_{CC} Supply Current					
Operating	$1.0\ V < V_{FB} < V_{DAC}$ (max on−time), No Loads on GATE(H) and GATE(L)	–	12	20	mA
V_{CC} Monitor					
Start Threshold	GATE(H) switching	3.75	3.95	4.15	V
Stop Threshold	GATE(H) not switching	3.65	3.87	4.05	V
Hysteresis	Start−Stop	–	80	–	mV
Error Amplifier					
V_{FB} Bias Current	$V_{FB} = 0$ V	–	0.1	1.0	μA
COMP Source Current	COMP = 1.2 V to 3.6 V; $V_{FB} = 1.9$ V	15	30	60	μA
COMP CLAMP Voltage	$V_{FB} = 1.9$ V, Adjust COMP voltage for Comp current = 60 μA	0.85	1.0	1.15	V
COMP Clamp Current	COMP = 0 V	0.4	1.0	1.6	mA
COMP Sink Current	$V_{COMP} = 1.2$ V; $V_{FB} = 2.2$ V; $V_{SS} > 2.5$ V	180	400	800	μA
Open Loop Gain	Note 2	50	60	–	dB
Unity Gain Bandwidth	Note 2	0.5	2.0	–	MHz
PSRR @ 1.0 kHz	Note 2	60	85	–	dB
Overcurrent Detection					
Current Limit Voltage	$V_{FB} = 0$ V to 3.5 V, $8.0\ V < V_{CC} < 12\ V + 10\%$	55	76	130	mV
I_{SENSE} Bias Current	$I_{SENSE} = 2.8$ V	13	30	50	μA

2. Guaranteed by design, not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (continued) (0°C < T_A < 70°C; 0°C < T_J < 125°C; 8.0 V < V_{CC} < 14 V; 2.0 DAC Code: (V_{ID4} = V_{ID3} = V_{ID2} = V_{ID1} = 0); $C_{GATE(H)}$ = $C_{GATE(L)}$ = 3.3 nF; C_{OFF} = 330 pF; C_{SS} = 0.1 μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
GATE(H) and GATE(L)					
High Voltage at 100 mA	Measure V_{CC} − GATE	−	1.2	2.0	V
Low Voltage at 100 mA	Measure GATE	−	1.0	1.5	V
Rise Time	1.6 V < GATE < (V_{CC} − 2.5 V)	−	40	80	ns
Fall Time	(V_{CC} − 2.5 V) > GATE > 1.6 V	−	40	80	ns
GATE(H) to GATE(L) Delay	GATE(H) < 2.0 V; GATE(L) > 2.0 V	30	65	100	ns
GATE(L) to GATE(H) Delay	GATE(L) < 2.0 V; GATE(H) > 2.0 V	30	65	100	ns
GATE pull−down	Resistor to PGND, Note 3	20	50	115	kΩ
Fault Protection					
SS Charge Time	V_{FB} = 3.0 V, V_{ISENSE} = 2.8 V	1.6	3.3	5.0	ms
SS Pulse Period	V_{FB} = 3.0 V, V_{ISENSE} = 2.8 V	25	100	200	ms
SS Duty Cycle	(Charge Time/Period) × 100	1.0	3.3	6.0	%
SS COMP Clamp Voltage	V_{FB} = 2.7 V; V_{SS} = 0 V	0.50	0.95	1.10	V
V_{FB} Low Comparator	Increase V_{FB} till normal off−time	0.9	1.0	1.1	V
PWM Comparator					
Transient Response	V_{FB} = 1.2 to 5.0 V. 500 ns after GATE(H) (after Blanking time) to GATE(H) = (V_{CC} −1.0 V) to 1.0 V	−	115	175	ns
Minimum Pulse Width (Blanking Time)	Drive V_{FB} 1.2 V to 5.0 V upon GATE(H) rising edge (> V_{CC} − 1.0 V), measure GATE(H) pulse width	100	200	300	ns
C_{OFF}					
Normal Off−Time	V_{FB} = 2.7 V	1.0	1.6	2.3	μs
Extended Off−Time	V_{SS} = V_{FB} = 0 V	5.0	8.0	12.0	μs
Time−Out Timer					
Time−Out Time	V_{FB} = 2.7 V, Measure GATE(H) Pulse Width	10	30	50	μs
Fault Duty Cycle	V_{FB} = 0V	30	50	70	%
Power Good Output					
Low to High Delay	V_{FB} = (0.8 × V_{DAC}) to V_{DAC}	30	65	110	μs
High to Low Delay	V_{FB} = $V_{DAC\ to}$ (0.8 × V_{DAC})	30	75	120	μs
Output Low Voltage	V_{FB} = 2.4 V, I_{PWRGD} = 500 μA	−	0.2	0.3	V
Sink Current Limit	V_{FB} = 2.4 V, PWRGD = 1.0 V	0.5	4.0	15.0	mA

3. Guaranteed by design, not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.0 DAC Code: ($V_{ID4} = V_{ID3} = V_{ID2} = V_{ID1} = 0$); $C_{GATE(H)} = C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1\ \mu F$, unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC									
Accuracy (all codes except 11111)					Measure V_{FB} = COMP (C_{OFF} = GND) 25°C ≤ T_J ≤ 125°C; V_{CC} = 12 V	−1.0	–	+1.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
1	0	0	0	0	–	3.489	3.525	3.560	V
1	0	0	0	1	–	3.390	3.425	3.459	V
1	0	0	1	0	–	3.291	3.325	3.358	V
1	0	0	1	1	–	3.192	3.225	3.257	V
1	0	1	0	0	–	3.093	3.125	3.156	V
1	0	1	0	1	–	2.994	3.025	3.055	V
1	0	1	1	0	–	2.895	2.925	2.954	V
1	0	1	1	1	–	2.796	2.825	2.853	V
1	1	0	0	0	–	2.697	2.725	2.752	V
1	1	0	0	1	–	2.598	2.625	2.651	V
1	1	0	1	0	–	2.499	2.525	2.550	V
1	1	0	1	1	–	2.400	2.425	2.449	V
1	1	1	0	0	–	2.301	2.325	2.348	V
1	1	1	0	1	–	2.202	2.225	2.247	V
1	1	1	1	0	–	2.103	2.125	2.146	V
0	0	0	0	0	–	2.054	2.075	2.095	V
0	0	0	0	1	–	2.004	2.025	2.045	V
0	0	0	1	0	–	1.955	1.975	1.994	V
0	0	0	1	1	–	1.905	1.925	1.944	V
0	0	1	0	0	–	1.856	1.875	1.893	V
0	0	1	0	1	–	1.806	1.825	1.843	V
0	0	1	1	0	–	1.757	1.775	1.792	V
0	0	1	1	1	–	1.707	1.725	1.742	V
0	1	0	0	0	–	1.658	1.675	1.691	V
0	1	0	0	1	–	1.608	1.625	1.641	V
0	1	0	1	0	–	1.559	1.575	1.590	V
0	1	0	1	1	–	1.509	1.525	1.540	V
0	1	1	0	0	–	1.460	1.475	1.489	V
0	1	1	0	1	–	1.410	1.425	1.439	V
0	1	1	1	0	–	1.361	1.375	1.388	V
0	1	1	1	1	–	1.311	1.325	1.338	V
1	1	1	1	1	–	1.219	1.247	1.269	V
Input Threshold					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	1.000	1.250	2.400	V
Input Pull−up Resistance					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	25	50	100	kΩ
Input Pull−up Voltage						4.85	5.00	5.15	V

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ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $8.0\ V < V_{CC} < 14\ V$; 2.0 DAC Code: ($V_{ID4} = V_{ID3} = V_{ID21} = V_{ID1} = 0$); $C_{GATE(H)} = C_{GATE(L)} = 3.3$ nF; $C_{OFF} = 330$ pF; $C_{SS} = 0.1$ μF, unless otherwise specified.)

Threshold Accuracy					Lower Threshold			Upper Threshold			Unit
					Min	Typ	Max	Min	Typ	Max	
DAC CODE											
% of Nominal DAC Output					−12	−8.5	−5.0	5.0	8.5	12	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}							
1	0	0	0	0	3.102	3.225	3.348	3.701	3.824	3.948	V
1	0	0	0	1	3.014	3.133	3.253	3.596	3.716	3.836	V
1	0	0	1	0	2.926	3.042	3.158	3.491	3.607	3.724	V
1	0	0	1	1	2.838	2.950	3.063	3.386	3.499	3.612	V
1	0	1	0	0	2.750	2.859	2.968	3.281	3.390	3.500	V
1	0	1	0	1	2.662	2.767	2.873	3.176	3.282	3.388	V
1	0	1	1	0	2.574	2.676	2.778	3.071	3.173	3.276	V
1	0	1	1	1	2.486	2.584	2.683	2.966	3.065	3.164	V
1	1	0	0	0	2.398	2.493	2.588	2.861	2.956	3.052	V
1	1	0	0	1	2.310	2.401	2.493	2.756	2.848	2.940	V
1	1	0	1	0	2.222	2.310	2.398	2.651	2.739	2.828	V
1	1	0	1	1	2.134	2.218	2.303	2.546	2.631	2.716	V
1	1	1	0	0	2.046	2.127	2.208	2.441	2.522	2.604	V
1	1	1	0	1	1.958	2.035	2.113	2.336	2.414	2.492	V
1	1	1	1	0	1.870	1.944	2.018	2.231	2.305	2.380	V
0	0	0	0	0	1.826	1.898	1.971	2.178	2.251	2.324	V
0	0	0	0	1	1.782	1.8520	1.923	2.126	2.197	2.268	V
0	0	0	1	0	1.738	1.807	1.876	2.073	2.142	2.212	V
0	0	0	1	1	1.694	1.761	1.828	2.021	2.088	2.156	V
0	0	1	0	0	1.650	1.715	1.781	1.968	2.034	2.100	V
0	0	1	0	1	1.606	1.669	1.733	1.916	1.980	2.044	V
0	0	1	1	0	1.562	1.624	1.686	1.863	1.925	1.988	V
0	0	1	1	1	1.518	1.578	1.638	1.811	1.871	1.932	V
0	1	0	0	0	1.474	1.532	1.591	1.758	1.817	1.876	V
0	1	0	0	1	1.430	1.486	1.543	1.706	1.763	1.820	V
0	1	0	1	0	1.386	1.441	1.496	1.653	1.708	1.764	V
0	1	0	1	1	1.342	1.395	1.448	1.601	1.654	1.708	V
0	1	1	0	0	1.298	1.349	1.401	1.548	1.600	1.652	V
0	1	1	0	1	1.254	1.303	1.353	1.496	1.546	1.596	V
0	1	1	1	0	1.210	1.258	1.306	1.443	1.491	1.540	V
0	1	1	1	1	1.166	1.212	1.258	1.391	1.437	1.484	V
1	1	1	1	1	1.094	1.138	1.181	1.306	1.349	1.393	V

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PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO–16L	PIN SYMBOL	FUNCTION
1, 2, 3, 4, 6	V_{ID0}–V_{ID4}	Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V if left open. V_{ID4} selects the DAC range. When V_{ID4} is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When V_{ID4} is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments.
5	SS	Soft Start Pin. A capacitor from this pin to LGND sets the Soft Start and fault timing.
7	C_{OFF}	Off−Time Capacitor Pin. A capacitor from this pin to LGND sets both the normal and extended off time.
8	I_{SENSE}	Current Sense Comparator Inverting Input.
9	V_{CC}	Input Power Supply Pin.
10	GATE(H)	High Side Switch FET driver pin.
11	PGND	High current ground for the GATE(H) and GATE(L) pins.
12	GATE(L)	Low Side Synchronous FET driver pin.
13	PWRGD	Power Good Output. Open collector output drives low when V_{FB} is out of regulation.
14	LGND	Reference ground. All control circuits are referenced to this pin.
15	COMP	Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation.
16	V_{FB}	Error Amp, PWM Comparator feedback input, Current Sense Comparator Non−Inverting input, and PWRGD Comparator input.

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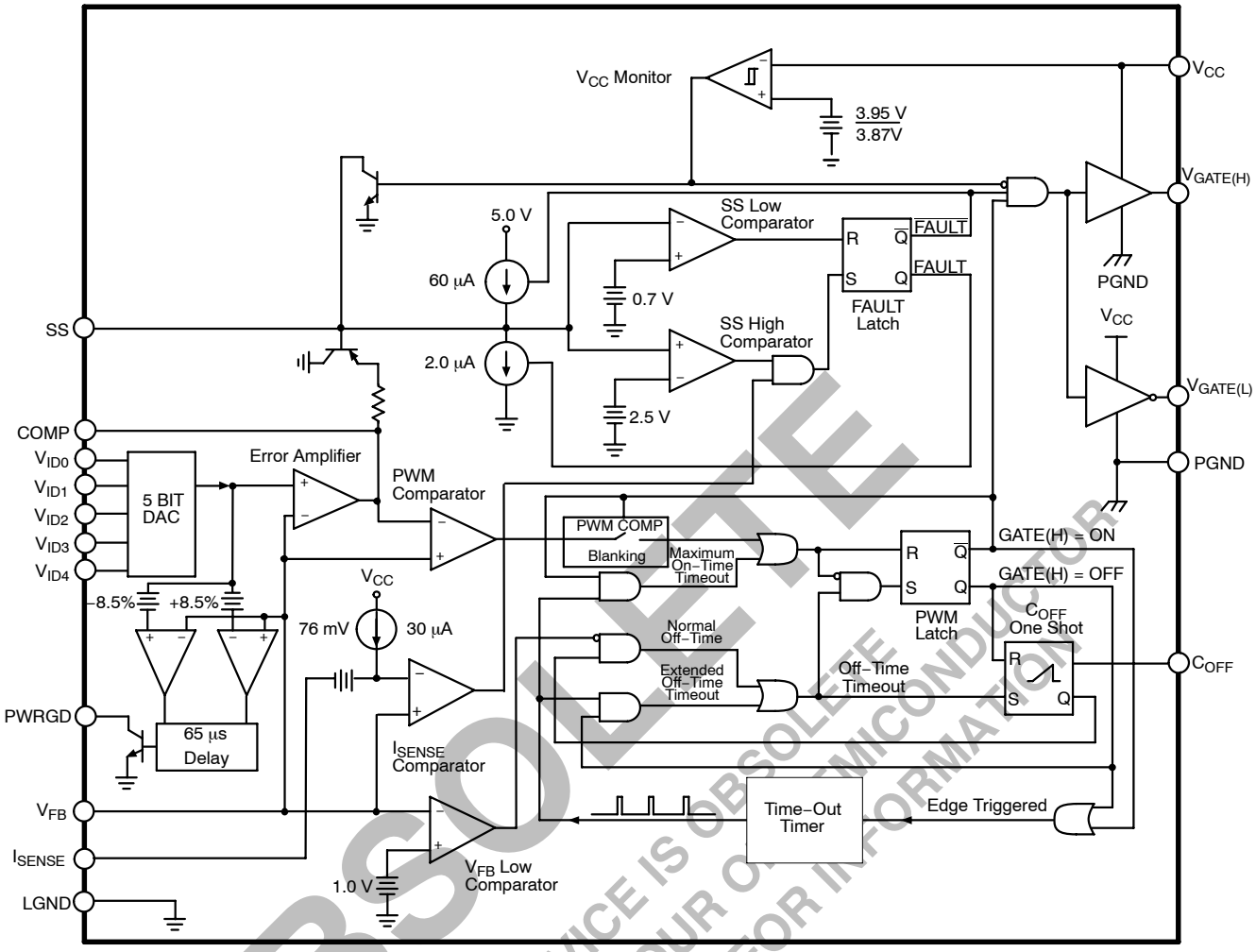


Figure 2. Block Diagram

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TYPICAL PERFORMANCE CHARACTERISTICS

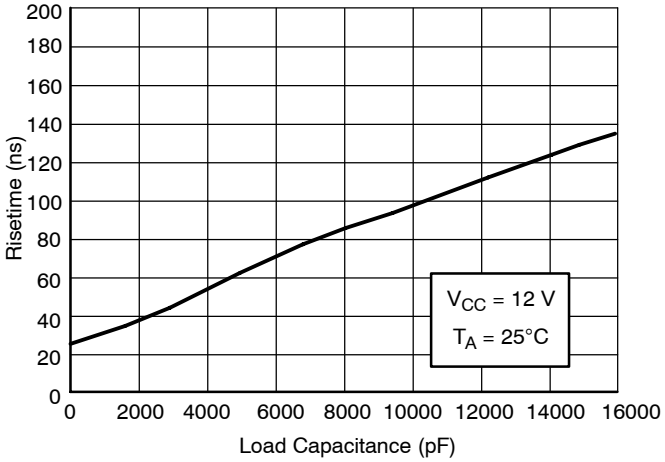


Figure 3. GATE(L) Risetime vs. Load Capacitance

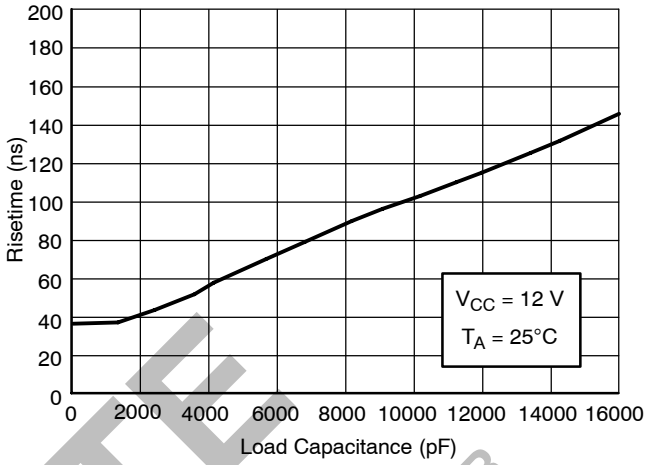


Figure 4. GATE(H) Risetime vs. Load Capacitance

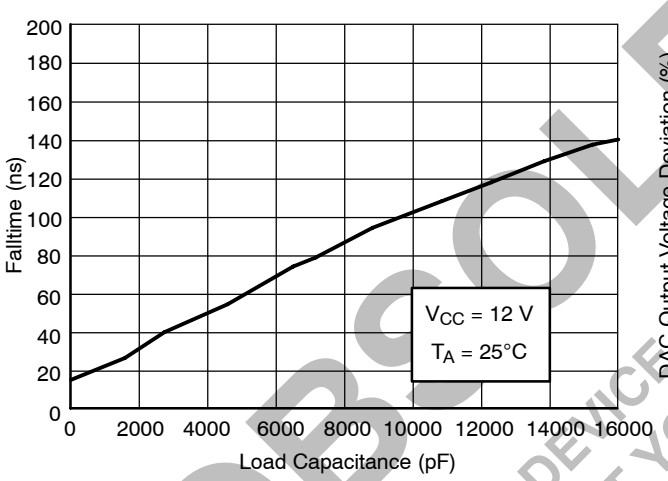


Figure 5. GATE(H) & GATE(L) Falltime vs. Load Capacitance

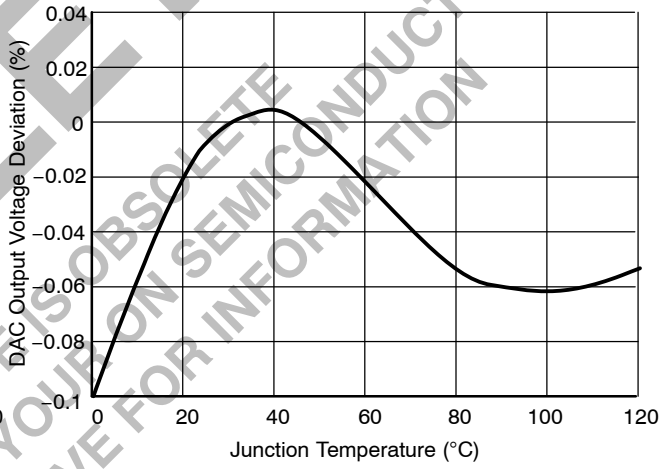


Figure 6. DAC Output Voltage vs. Temperature, DAC Code = 10111, V_{CC} = 12 V

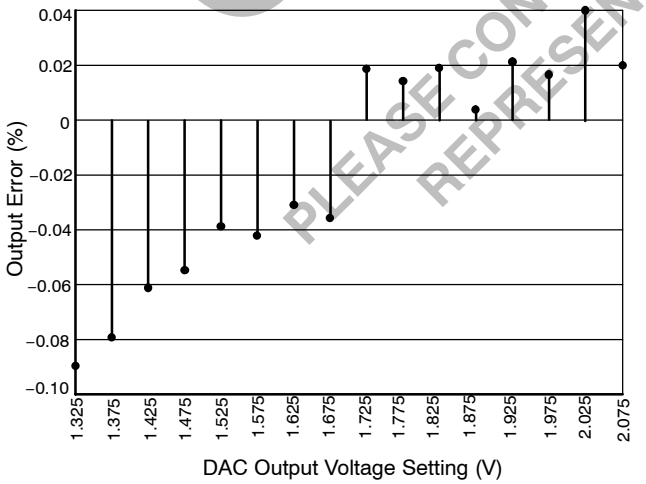


Figure 7. Percent Output Error vs. DAC Voltage Setting, V_{CC} = 12 V, T_A = 25°C, V_{ID4} = 0

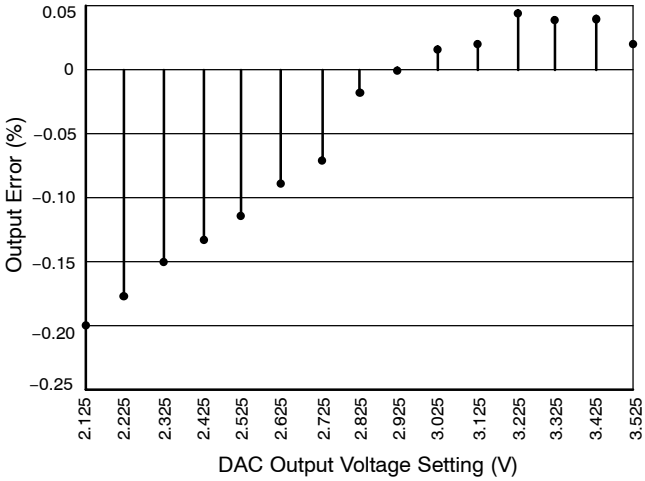


Figure 8. Percent Output Error vs. DAC Output Voltage Setting V_{CC} = 12 V, T_A = 25°C, V_{ID4} = 1

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APPLICATIONS INFORMATION

THEORY OF OPERATION

V² Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

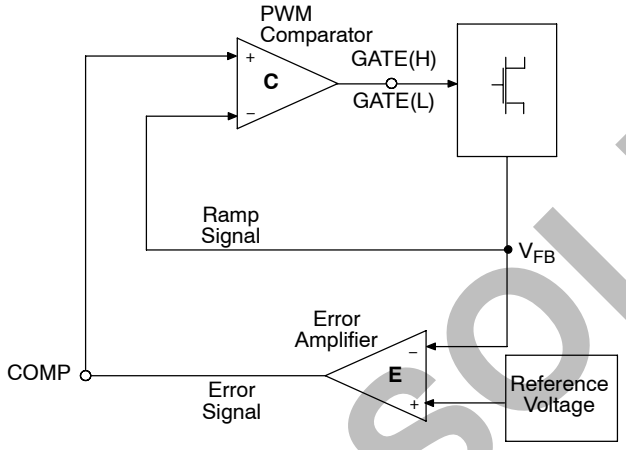


Figure 9. V^2 Control Diagram

The V^2 control method is illustrated in Figure 9. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

The Bode plot in Figure 10 shows the gain and phase margin of the CS5166 single pole feedback loop and demonstrates the overall stability of the CS5166−based regulator.

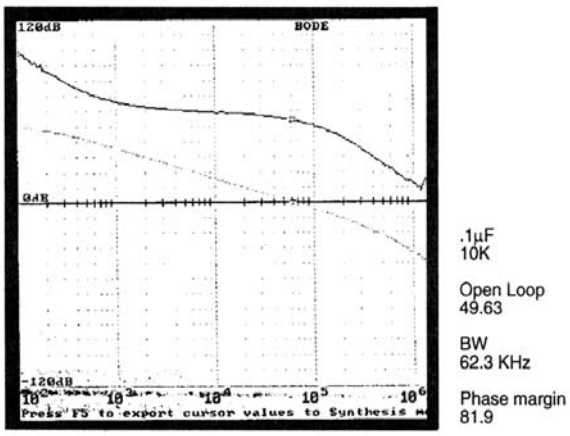


Figure 10. Feedback Loop Bode Plot

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.

A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

Constant Off Time

To maximize transient response, the CS5166 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C_{OFF} capacitor. To maintain regulation, the V^2 control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub−harmonic oscillations at high duty cycles is avoided.

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Switch on time is limited by an internal 30 μs (typical) timer, minimizing stress to the power components.

Programmable Output

The CS5166 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5166 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the V_{FB} pin, as in traditional controllers. The CS5166 is specifically designed to meet or exceed Intel's Pentium II specifications.

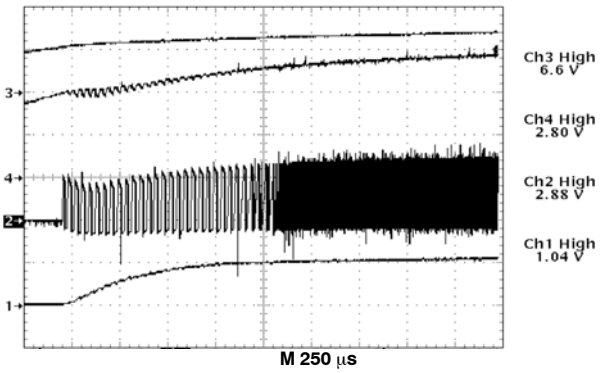
Start Up

Until the voltage on the V_{CC} supply pin exceeds the 3.95 V monitor threshold, the Soft Start and GATE pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the V_{CC} pin exceeds the monitor threshold, the GATE(H) output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a 50% duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

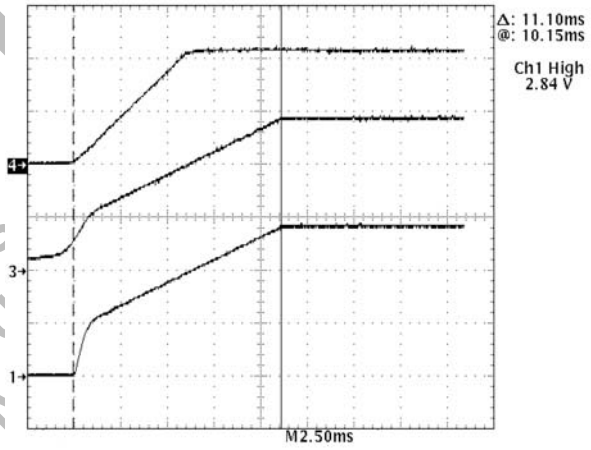
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C_{OFF} capacitor. The V^2 control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin.



Trace 1– Regulator Output Voltage (1.0 V/div.)
Trace 2– Inductor Switching Node (2.0 V/div.)
Trace 3– 12 V Input (V_{CC}) (5.0 V/div.)
Trace 4– 5.0 V Input (1.0 V/div.)

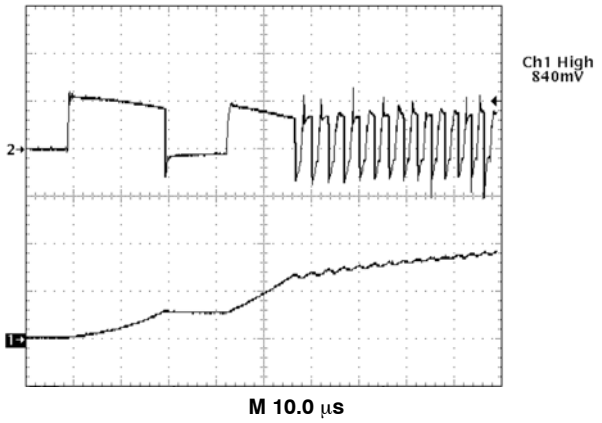
Figure 11. Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.



Trace 1– Regulator Output Voltage (1.0 V/div.)
Trace 3– COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4– Soft Start Pin (2.0 V/div.)

Figure 12. Demonstration Board Startup Waveforms

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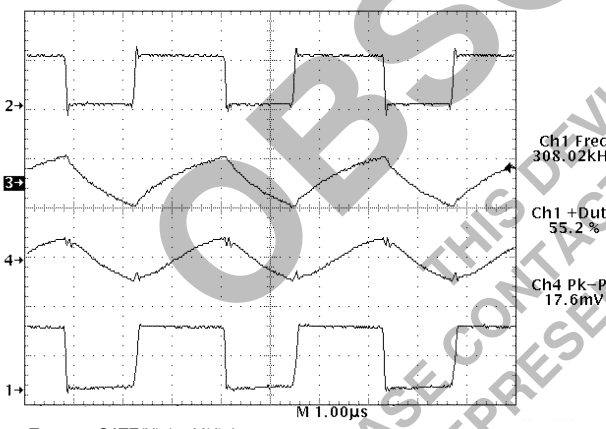


Trace 1– Regulator Output Voltage (5.0 V/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)

Figure 13. Demonstration Board Enable Startup Waveforms

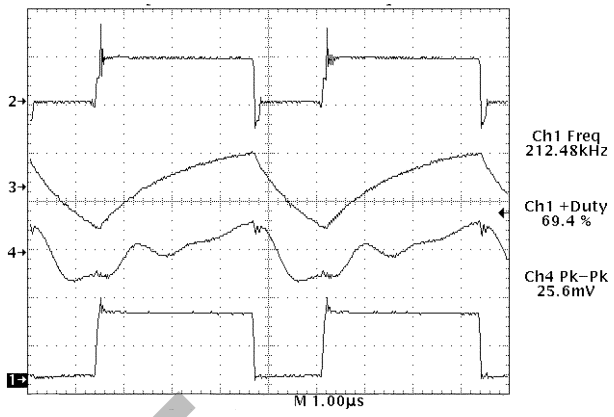
Normal Operation

During normal operation, switch off time is constant and set by the C_{OFF} capacitor. Switch on time is adjusted by the V^2 control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working and the ESR of the output capacitors (see Figures 14 and 15).



Trace 1– GATE(H) (10 V/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)
Trace 3– Output Inductor Ripple Current (2.0 A/div.)
Trace 4– V_{OUT} ripple (20 mV/div.)

Figure 14. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, 0.5 A Load, V_{OUT} = +2.825 V (DAC = 10111)



Trace 1– GATE(H) (10 V/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)
Trace 3– Output Inductor Ripple Current (2.0 A/div.)
Trace 4– V_{OUT} ripple (20 mV/div.)

Figure 15. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, I_{LOAD} = 14 A, V_{OUT} = +2.825 V (DAC = 10111)

Transient Response

The CS5166 V^2 control loop's 150 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre−positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

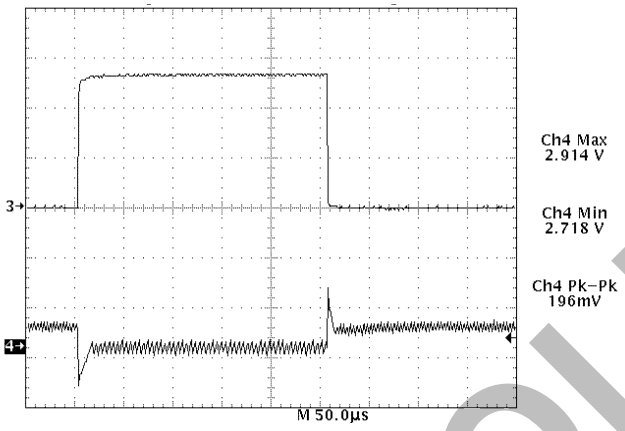
Holding tolerance to 1.0% allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A "Droop Resistor", implemented through a PC board trace, connects the Error Amps feedback pin (V_{FB}) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, an 50 mV drop is developed across this resistor. This results in output voltage being offset −25 mV low.

The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before

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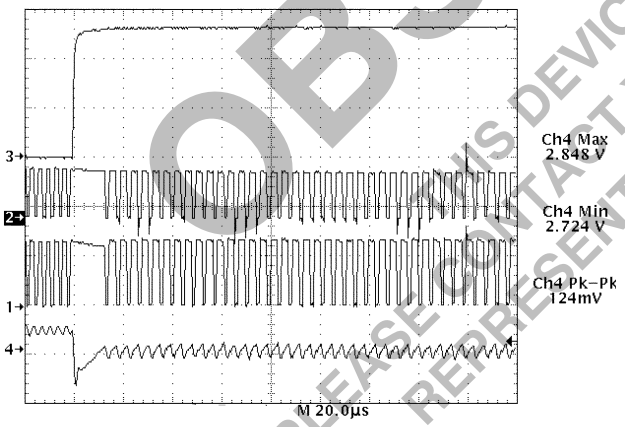
reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre−positioned +25 mV. Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre−positioned −25 mV (see Figures 16, 17, and 18). For best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the Maximum On−Time is exceeded while responding to a sudden increase in Load current, a normal off−time occurs to prevent saturation of the output inductor.



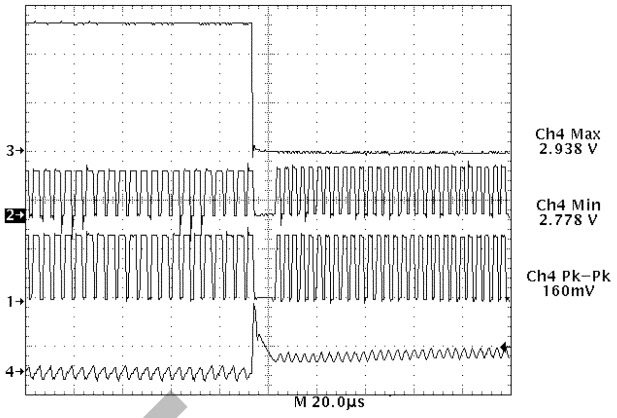
Trace 3− Load Current (5.0 A/10 mV/div.)
Trace 4− V_{OUT} (100 mV/div.)

Figure 16. Output Voltage Transient Response to a 14 A Load Pulse, V_{OUT} = +2.825 V (DAC = 10111)



Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Load Current (5.0 A/div)
Trace 4− V_{OUT} (100 mV/div.)

Figure 17. Output Voltage Transient Response to a 14 A Load Step, V_{OUT} = +2.825 V (DAC = 10111)



Trace 1− GATE(H) (10 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)
Trace 3− Load Current (5.0 A/div)
Trace 4− V_{OUT} (100 mV/div.)

Figure 18. Output Voltage Transient Response to a 14 A Load Turn−Off, V_{OUT} = +2.825 V (DAC = 10111)

Power Supply Sequencing

The CS5166 offers inherent protection from undefined start up conditions, regardless of the 12 V and 5.0 V supply power up sequencing. The turn on slew rates of the 12 V and 5.0 V power supplies can be varied over wide ranges without affecting the output voltage or causing detrimental effects to the buck regulator.

PROTECTION AND MONITORING FEATURES

Overcurrent Protection

A loss−less hiccup mode current limit protection feature is provided, requiring only the Soft Start capacitor to implement. The CS5166 provides overcurrent protection by sensing the current through a “Droop” resistor, using an internal current sense comparator. The comparator compares this voltage drop to an internal reference voltage of 76 mV (typical).

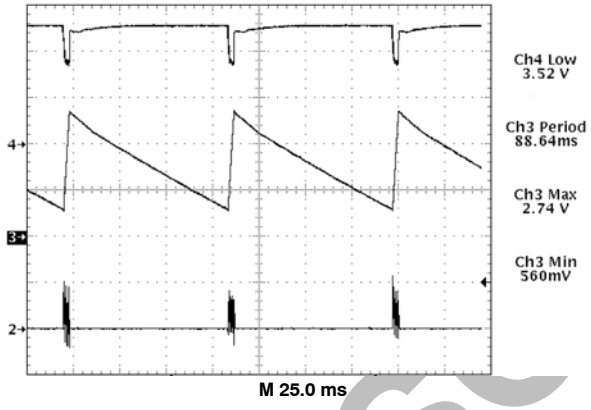
If the voltage drop across the “Droop” resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching. During this overcurrent condition, the CS5166 stays off for the time it takes the Soft Start capacitor to slowly discharge by a 2.0 µA current source until it reaches its lower 0.7 V threshold.

At that time the regulator attempts to restart normally by delivering short gate pulses to both FET’s. The CS5166 will operate initially in its extended off time mode with a 50% duty cycle, while the Soft Start capacitor is charged with a 60 mA charge current. The gates will switch on while the

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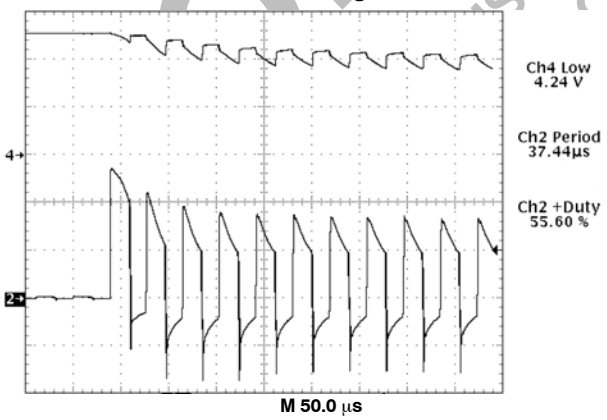
Soft Start capacitor is charged to its upper 2.7 V threshold. During an overload condition the Soft Start charge/discharge current ratio sets the duty cycle for the pulses (2.0 μA/60 μA = 3.3%), while actual duty cycle is half that due to the extended off time mode (1.65%) when V_{FB} is less than 1.0 V. The Soft Start hiccup pulses last for a 3.0 ms period at the end of which the duty cycle repeats if a fault is detected, otherwise normal operation resumes.

The protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the overcurrent condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume. The current limit trip point can be adjusted through an external resistor, providing the user with the current limit set−point flexibility.



Trace 4− 5.0 V Supply Voltage (2.0 V/div.)
Trace 3− Soft Start Timing Capacitor (1.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

Figure 19. Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge



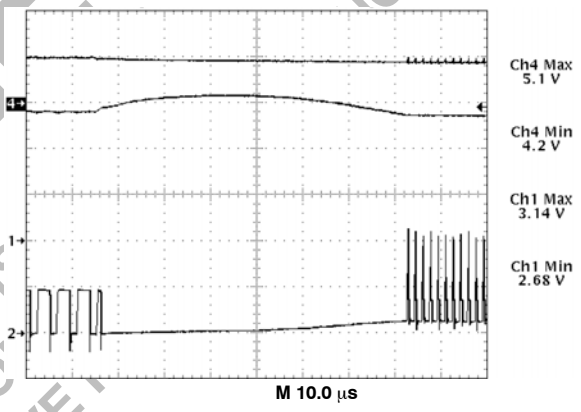
Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

Figure 20. Demonstration Board Startup with Regulator Output Shorted To Ground

Overvoltage Protection

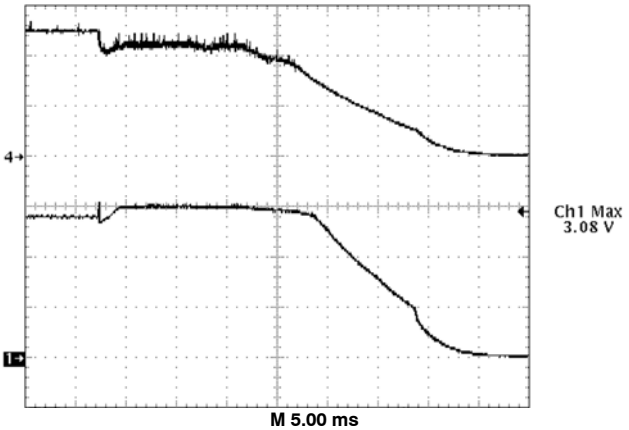
Overvoltage protection (OVP) is provided as result of the normal operation of the V^2 control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns, causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 21 and 22). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function. If a dedicated OVP output is required, it can be implemented using the circuit in Figure 23. In this figure the OVP signal will go high (overvoltage condition), if the output voltage (V_{CORE}) exceeds 20% of the voltage set by the particular DAC code and provided that PWRGD is low. It is also required that the overvoltage condition be present for at least the PWRGD delay time for the OVP signal to be activated. The resistor values shown in Figure 23 are for V_{DAC} = +2.8 V (DAC = 10111). The V_{OVP} (overvoltage trip−point) can be set using the following equation:

$$V_{OVP} = V_{BEQ3}\left(1 + \frac{R2}{R1}\right)$$



Trace 4− 5.0 V from PC Power Supply (5.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node 5.0 V/div.)

Figure 21. OVP Response to an Input−to−Output Short Circuit by Immediately Providing 0% Duty Cycle, Crow−Barring the Input Voltage to Ground



Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)

Figure 22. OVP Response to an Input−to−Output Short Circuit by Pulling the Input Voltage to Ground

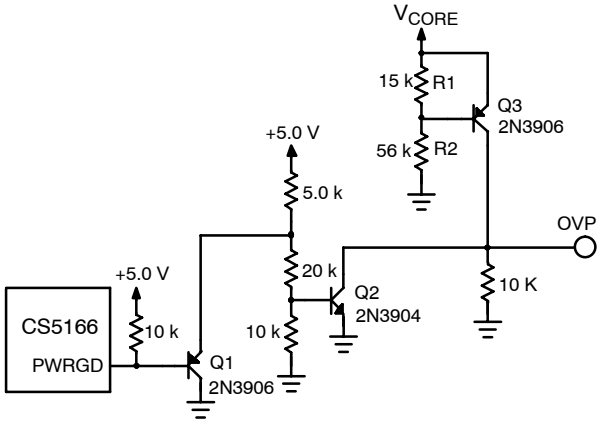
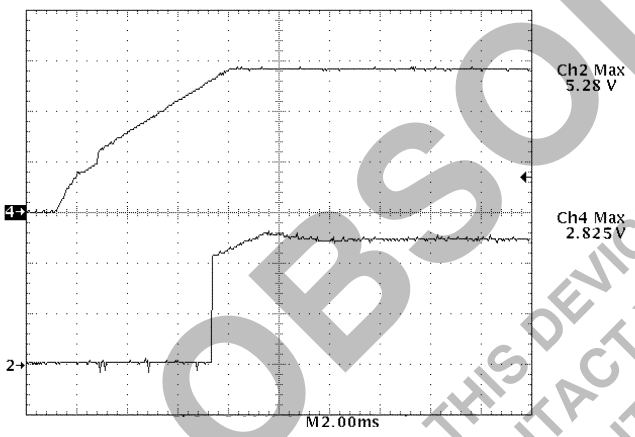


Figure 23. Circuit To Implement A Dedicated OVP Output Using The CS5166

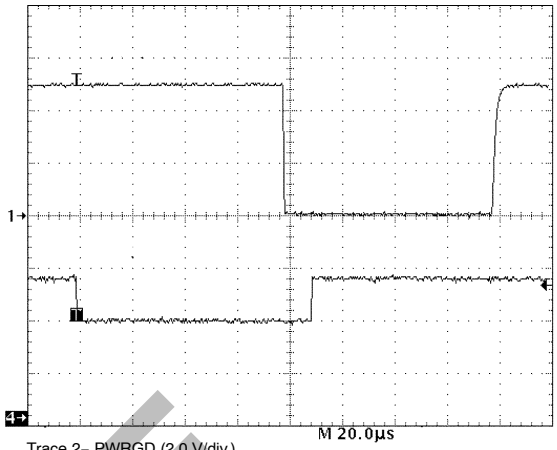
Power Good Circuit

The Power Good pin (pin 13) is an open−collector signal consistent with TTL DC specifications. It is externally pulled−up, and is pulled low (below 0.3 V) when the regulator output voltage typically exceeds ± 8.5% of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is ± 12%.



Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{OUT} (1.0 V/div.)

Figure 24. PWRGD Signal Becomes Logic High as V_{OUT} Enters −8.5% of Lower PWRGD Threshold, V_{OUT} = +2.825 V (DAC = 10111)

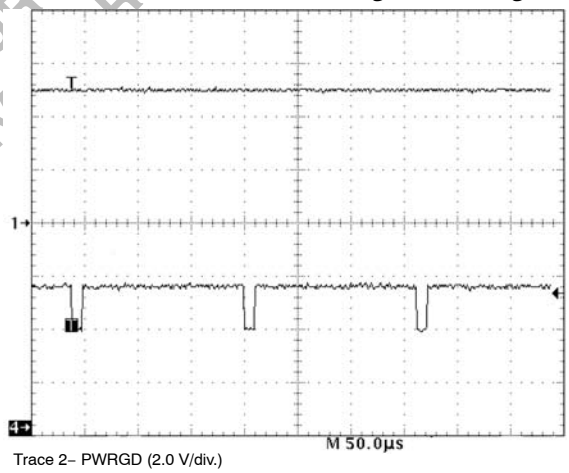


Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{FB} (1.0 V/div.)

Figure 25. Power Good Response to an Out of Regulation Condition

Figure 25 shows the relationship between the regulated output voltage V_{FB} and the Power Good signal. To prevent Power Good from interrupting the CPU unnecessarily, the CS5166 has a built−in delay to prevent noise at the V_{FB} pin from toggling Power Good. The internal time delay is designed to take about 75 µs for Power Good to go low and 65 µs for it to recover. This allows the Power Good signal to be completely insensitive to out of regulation conditions that are present for a duration less than the built in delay (see Figure 26).

It is therefore required that the output voltage attains an out of regulation or in regulation level for at least the built−in delay time duration before the Power Good signal can change state.



Trace 2− PWRGD (2.0 V/div.)
Trace 4− V_{FB} (1.0 V/div.)

Figure 26. Power Good is Insensitive to Out of Regulation Conditions that are Present for a Duration Less Than the Built In Delay

External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure). This circuit operates by pulling the Soft Start pin high, and the I_{SENSE} pin low, emulating a current limit condition.

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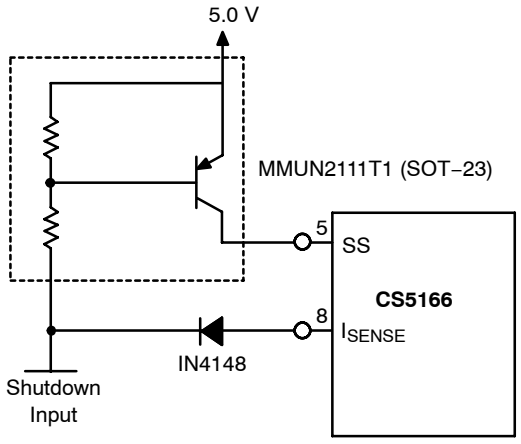


Figure 27. Implementing Shutdown with the CS5166

Selecting External Components

The CS5166 buck regulator can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

NFET Power Transistors

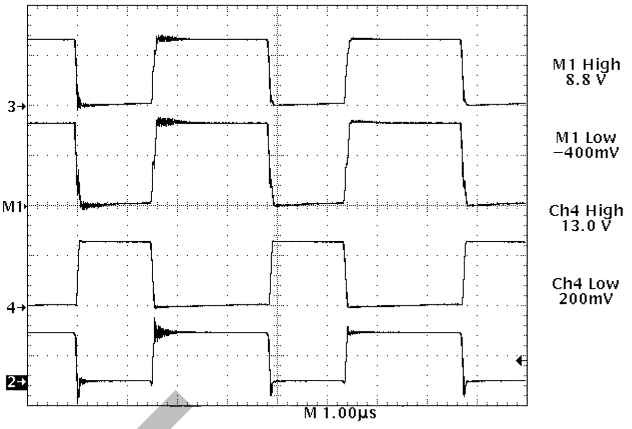
Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level FETs. A charge pump may be easily implemented to support 5.0 V only systems. Multiple FET's may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where V_{CC} = 12 V and 5.0 V is used as the source for the regulator output current, the following gate drive is provided:

$$V_{GS(TOP)} = 12\ V - 5.0\ V = 7.0\ V$$

$$V_{GS(BOTTOM)} = 12\ V$$

(see Figure 28)



Trace 3– GATE(H) (10 V/div.)
Trace 1– GATE(H) – 5.0 V_{IN}
Trace 4– GATE(L) (10 V/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)

Figure 28. Gate Drive Waveforms Depicting Rail to Rail Swing



Trace 1 = GATE(H) (5.0 V/div.)
Trace 2 = GATE(L) (5.0 V/div.)

Figure 29. Normal Operation Showing the Guaranteed Non−Overlap Time Between the High and Low−Side MOSFET Gate Drives, I_{LOAD} = 14 A

The CS5166 provides adaptive control of the external NFET conduction times by guaranteeing a typical 65 ns non−overlap (as seen in Figure 29) between the upper and lower MOSFET gate drive pulses. This feature eliminates the potentially catastrophic effect of "shoot−through current", a condition during which both FETs conduct causing them to overheat, self−destruct, and possibly inflict irreversible damage to the processor.

The most important aspect of FET performance is RDS_{ON}, which effects regulator efficiency and FET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows:

Switching MOSFET:

$$Power = I_{LOAD}^2 \times RDS_{ON} \times duty\ cycle$$

Synchronous MOSFET:

$$Power = I_{LOAD}^2 \times RDS_{ON} \times (1 - duty\ cycle)$$

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Duty Cycle =

$$\frac{V_{OUT} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET})}{\left[V_{IN} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET}) - (I_{LOAD} \times RDS_{ON\ OF\ SWITCH\ FET})\right]}$$

Off Time Capacitor (C_{OFF})

The C_{OFF} timing capacitor sets the regulator off time:

$$T_{OFF} = C_{OFF} \times 4848.5$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the C_{OFF} timing capacitor:

$$C_{OFF} = \frac{\text{Perioid} \times (1 - \text{duty cycle})}{4848.5}$$

where:

$$\text{Period} = \frac{1}{\text{switching frequency}}$$

Schottky Diode for Synchronous FET

For synchronous operation, a Schottky diode may be placed in parallel with the synchronous FET to conduct the inductor current upon turn off of the switching FET to improve efficiency. The CS5166 reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous FET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non−overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense. The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:

$$\text{Power} = V_{BD} \times I_{LOAD} \times \text{conduction time} \times \text{switching frequency}$$

Where V_{BD} = the forward drop of the MOSFET body diode. For the CS5166 demonstration board:

$$\text{Power} = 1.6\ V \times 14.2\ A \times 100\ ns \times 200\ kHz = 0.45\ W$$

This is only 1.1% of the 40 W being delivered to the load.

"Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation causes the thickness of the PCB layer to vary. 2) the mismatch of L/W, and 3) temperature variation.

1. **Sheet Resistivity** for one ounce copper, the thickness variation typically 1.15 mil to 1.35 mil. Therefore the error due to sheet resistivity is:

$$\frac{1.35 - 1.15}{1.25} = 16\%$$

2. **Mismatch due to L/W.** The variation in L/W is governed by variations due to the PCB manufacturing process that affect the geometry and the power dissipation capability of the droop resistor. The error due to L/W mismatch is typically 1.0%.
3. **Thermal Considerations.** Due to $I^2 \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$R = R_{20}[1 + \alpha_{20}(T - 20)]$$

where:
R_{20} = resistance at 20°C

$$\alpha = \frac{0.00393}{^\circ C}$$

T = operating temperature
R = desired droop resistor value
For temperature T = 50°C, the % R change = 12%

Droop Resistor Tolerance

Tolerance due to sheet resistivity variation	16%
Tolerance due to L/W error	1.0%
Tolerance due to temperature variation	12%
Total tolerance for droop resistor	29%

In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage full load is above the minimum DC tolerance spec.

$$V_{DROOP(TYP)} = \frac{[V_{DAC(MIN)} - V_{DC(MIN)}]}{1 + R_{DROOP(TOLERANCE)}}$$

Example: for a 300 MHz Pentium II, the DC accuracy spec is $2.74 < V_{CC(CORE)} < 2.9$ V, and the AC accuracy spec is $2.67\ V < V_{CC(CORE)} < 2.93$ V. The CS5166 DAC output voltage is $+2.796\ V < V_{DAC} < +2.853$ V. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$V_{DROOP(TYP)} = \frac{[V_{DAC(MIN)} - V_{DC\ PENTIUMII(MIN)}]}{1 + R_{DROOP(TOLERANCE)}}$$

$$= \frac{2.796\ V - 2.74\ V}{1.3} = 43\ mV$$

With the CS5166 DAC accuracy being 1.0%, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 25 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of −43 mV is developed across the resistor. Therefore, the regulator output is pre−positioned at 25 mV above the nominal output voltage before a load turn−on. The total voltage drop due to a load step is ΔV−25 mV and the

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deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre−positioned at 18 mV below the nominal voltage before a load turn−off. The total voltage increase due to a load turn−off is ΔV−18 mV and the deviation from the nominal output voltage is 18 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre−charged to value that is either 25 mV above the nominal output voltage before a load turn−on or, 18 mV below the nominal output voltage before a load turn−off (see Figure 16).

Obviously, the larger the voltage drop across the droop resistor (the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.

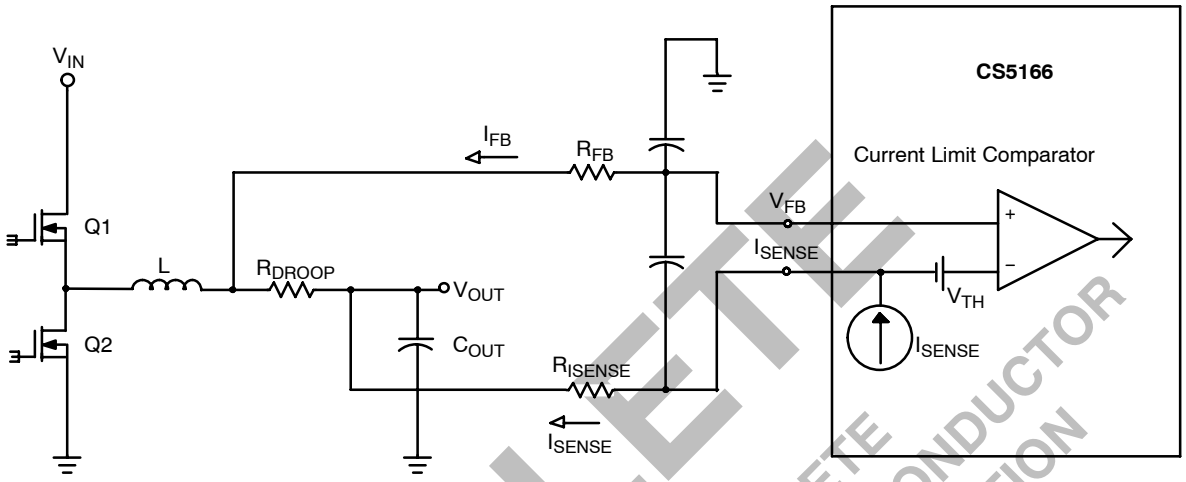


Figure 30. Circuit Used to Determine the Voltage Across the Droop Resistor that will Trip the Internal Current Sense Comparator

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Current Limit Setpoint Calculations

The following is the design equations used to set the current limit trip point by determining the value of the embedded PCB trace used as a current sensing element.

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point. For example the IRL 3103S (D^2 PAK) MOSFET has a continuous drain current rating of 45 A at V_{GS} = 10 V and T_C = 100°C. Temperature curves on MOSFET manufacturers' data sheets allow the designer to determine the MOSFET drain current at a particular V_{GS} and T_J (junction temperature). This, in turn, will assist the designer to set a proper current limit, without causing device breakdown during an overload condition.

For 300 MHz Pentium II CPU the full load is 14.2 A. The internal current sense comparator current limit voltage limits are: 55 mV < V_{TH} < 130 mV. Also, there is a 29% total variation in R_{SENSE} as discussed in the previous section.

We select the value of the current sensing element (embedded PCB trace) for the minimum current limit setpoint:

$$R_{SENSE(MAX)} = \frac{V_{TH(MIN)}}{I_{CL(MIN)}} \Rightarrow R_{SENSE} \times 1.29 = \frac{55\ mV}{14.2\ A} \Rightarrow$$

$$R_{SENSE} \times 1.29 = 3.87\ m\Omega \Rightarrow R_{SENSE} = 3.0\ m\Omega$$

We calculate the range of load currents that will cause the internal current sense comparator to detect and overload condition.

From the overcurrent detection data section on page 3.

Nominal Current Limit Setpoint

$$V_{TH(TYP)} = 76\ mV$$

$$I_{CL(NOM)} = \frac{V_{TH(TYP)}}{R_{SENSE(NOM)}}$$

Maximum Current Limit Setpoint

$$\text{Therefore, } I_{CL(NOM)} = \frac{76\ mV}{3.0\ m\Omega} = 25.3$$

$$V_{TH(MAX)} = 110\ mV$$

Therefore,

$I_{CL(MAX)}$ =

$$\frac{110\ mV}{R_{SENSE(MIN)}} = \frac{110\ mV}{R_{SENSE} \times 0.71} = \frac{110\ mV}{3.0\ m\Omega \times 0.71} = 51.6\ A$$

Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a 3.0 mΩ embedded PCB trace is: 14.2 A < I_{CL} < 51.6 A, with 25.3 A being the nominal overload condition.

There may be applications whose layout will require the use of two extra filter components, a 510 Ω resistor in series with the I_{SENSE} pin, and a 0.1 μF capacitor between the I_{SENSE} and V_{FB} pins. These are needed for proper current limit operation and the resistor value is layout dependent.

This series resistor affects the calculation of the current limit setpoint, and has to be taken into account when determining an effective current limit.

The calculations below show how the current limit setpoint is determined when this 510 Ω is taken into consideration.

$$V_{TRIP} = V_{TH} + (I_{SENSE} \times R_{ISENSE}) - (R_{FB} \times I_{FB})$$

Where:

V_{TRIP} = voltage across the droop resistor that trips the I_{SENSE} comparator.

V_{TH} = internal I_{SENSE} comparator threshold

I_{SENSE} = I_{SENSE} bias current

R_{ISENSE} = I_{SENSE} pin 510 Ω filter resistor

R_{FB} = V_{FB} pin 3.3 k filter resistor

I_{FB} = V_{FB} bias current

Minimum current sense resistor (droop resistor) voltage drop required for current limit when R_{ISENSE} is used

$$V_{TRIP(MIN)} = 55\ mV + (13\ \mu A \times 510) - (3.3\ k \times 1.0\ \mu A)$$

$$= 55\ mV + 6.6\ mV - 3.3\ mV = 58.3\ mV$$

Nominal current sense resistor (droop resistor) voltage drop required for current limit when R_{ISENSE} is used

$$V_{TRIP(NOM)} = 76\ mV + (30\ \mu A \times 510) - (3.3\ k \times 0.1\ \mu A)$$

$$= 76\ mV + 15.3\ mV - 0.33\ mV = 90.97\ mV$$

Maximum current sense resistor (droop resistor) voltage drop required for current limit when R_{ISENSE} is used

$$V_{TRIP(NOM)} = 110\ mV + (50\ \mu A \times 510)$$

$$= 110\ mV + 25.5\ mV = 135.5\ mV$$

The value of R_{SENSE} (current sense PCB trace) is then calculated:

$$R_{SENSE(MAX)} = \frac{58.3\ mV}{14.2\ A} = 4.1\ m\Omega$$

$$R_{SENSE(NOM)} = \frac{R_{SENSE(MAX)}}{1.29} = \frac{4.1\ m\Omega m}{1.29} = 3.18\ m\Omega$$

The range of load currents that will cause the internal current sense comparator to detect an overload condition is as follows:

Nominal Current Limit Setpoint

$$I_{CL(NOM)} = \frac{V_{TRIP(NOM)}}{R_{SENSE(NOM)}}$$

Therefore,

$$I_{CL(NOM)} = \frac{90.97\ mV}{3.18\ m\Omega} = 28.6\ A$$

Maximum Current Limit Setpoint

$$I_{CL(MAX)} = \frac{V_{TRIP(MAX)}}{R_{SENSE(MAX)}}$$

Therefore,

$$I_{CL(MAX)} = \frac{135\ mV}{3.18\ m\Omega \times 0.71} = 60\ A$$

Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a 3.0 mΩ embedded PCB trace is: 14.2 A < ICL 60 A, with 28.6 A being the nominal overload condition.

Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$R_{AR} = \rho \times \frac{L}{A} \text{ or } R = \rho \times \frac{L}{(W \times t)}$$

where:

A = W × t = cross−sectional area

ρ = the copper resistivity (μΩ − mil)

L = length (mils)

W = width (mils)

t = thickness (mils)

For most PCBs the copper thickness, t, is 35 μm (1.37 mils) for one ounce copper. ρ = 717.86 μΩ−mil

For a Pentium II load of 14.2 A the resistance needed to create a 43 mV drop at full load is:

$$\text{Response Droop} = \frac{43\ mV}{I_{OUT}} = \frac{43\ mV}{14.2\ A} = 3.0\ m\Omega$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$\Delta R = 12\%\ @\ T_A = +50^{\circ}C$$

$$\Delta R = 34\%\ @\ T_A = +100^{\circ}C$$

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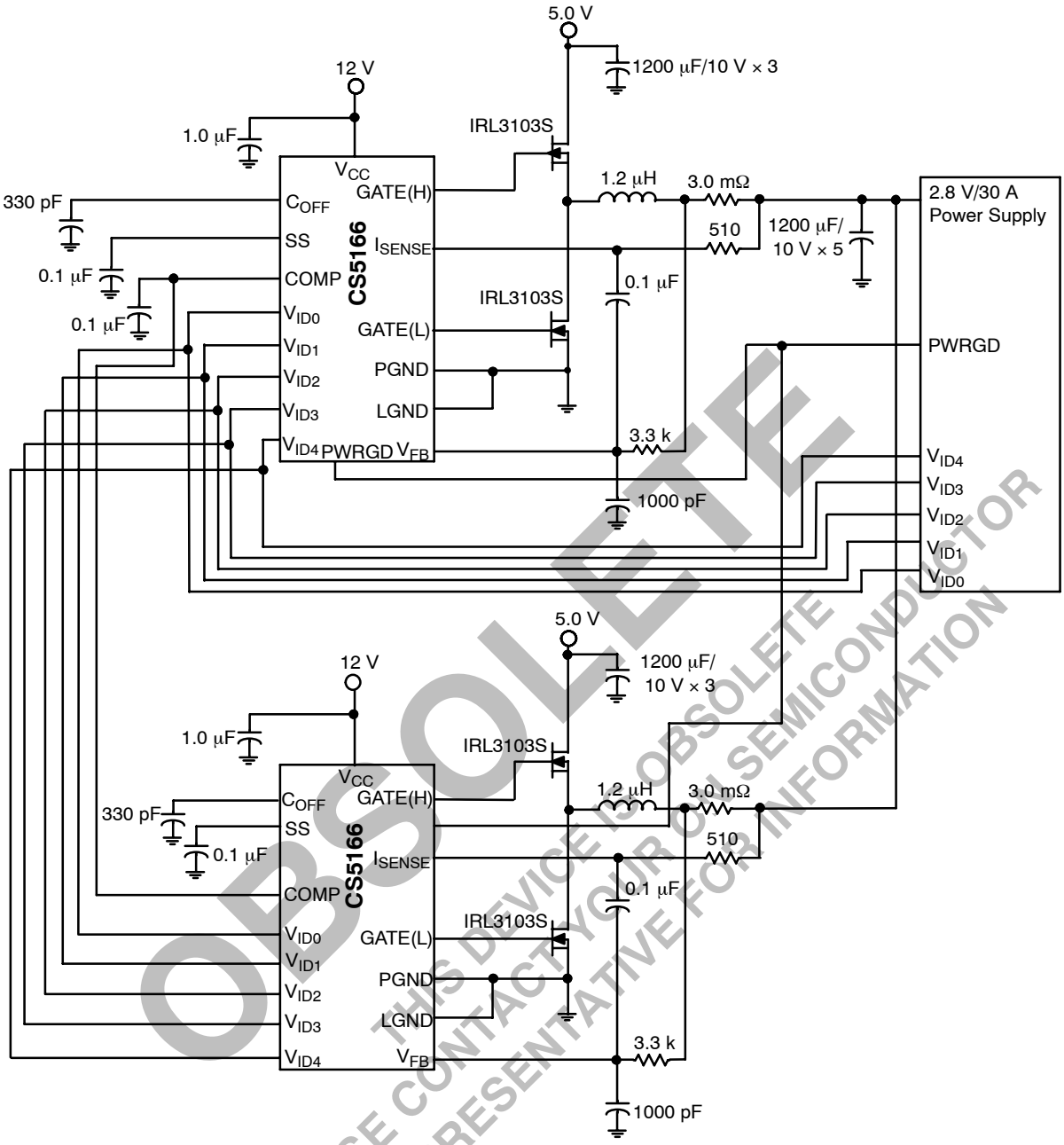


Figure 31. Current Sharing of a 2.8 V/30 A Power Supply Using Two CS5166 Synchronous Buck Regulators

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Droop Resistor Width Calculations

The droop resistor must have the ability to handle the load current and therefore requires a minimum width which is calculated as follows (assume one ounce copper thickness):

$$W = \frac{I_{LOAD}}{0.05}$$

where:

W = minimum width (in mils) required for proper power dissipation, and I_{LOAD} Load Current Amps.

The Pentium□II maximum load current is 14.2 A. Therefore:

$$W = \frac{14.2\ A}{0.05} = 284\ mils = 0.7213\ cm$$

Droop Resistor Length Calculation

$$L = \frac{R_{DROOP} \times W \times t}{\rho}$$

$$= \frac{0.0030 \times 284 \times 1.37}{717.86} = 1626\ mil = 4.13\ cm$$

Implementing Current Sharing Using the "Droop Resistor"

In addition to improving load transient performance, the CS5166 V^2 control method allows the droop resistor to provide the additional capability to easily implement current sharing. Figure 31 shows a simplified schematic of two current sharing synchronous buck regulators. Each buck regulator's droop resistor is terminated at the load. The PWM control signal from each Error Amp is connected together, causing the inner PWM loop to regulate to a common voltage. Since the voltage at each resistor terminal is the same, this configuration results in equal voltage being applied across each matched droop resistor. The result is equal current flowing through each buck regulator. An additional benefit is that synchronization to a common switching frequency tends to be achieved because each regulator shares a common PWM ramp signal.

In practice, each buck regulator will regulate to a slightly different output voltage due to mismatching of the PWM comparators, slope of the PWM ramp (output voltage ripple), and propagation delays. At light loads, the results can be very poor current sharing. With zero output current, some regulators may be sourcing current while others may be sinking current.

This results in additional power dissipation and lower efficiency than would be obtained by a single regulator. This is usually not an issue since efficiency is most important when a supply is fully loaded.

This effect is similar to the difference in efficiency between synchronous and non−synchronous buck regulators. Synchronous buck regulators have lower efficiency at light loads because inductor current is always continuous, flowing from the load to ground during switch off−time through the synchronous rectifier. Under full load conditions, the synchronous design is more efficient due to the lower voltage drop across the synchronous rectifier. Likewise, the efficiency of droop sharing regulators will be lower at light loads due to the continuous current flow in the droop resistors. Efficiency at heavy loads tends to be higher due to reduced I^2R losses.

The output current of each regulator can be calculated from:

$$I_N = \frac{(V_{OUT(N)} - V_{OUT})}{R_{DROOP(N)}}$$

where: $V_{OUT(N)}$ and $R_{DROOP(N)}$ are the output voltage and droop resistance of a particular regulator and V_{OUT} is the system output voltage. Output current is the sum of each regulator's current:

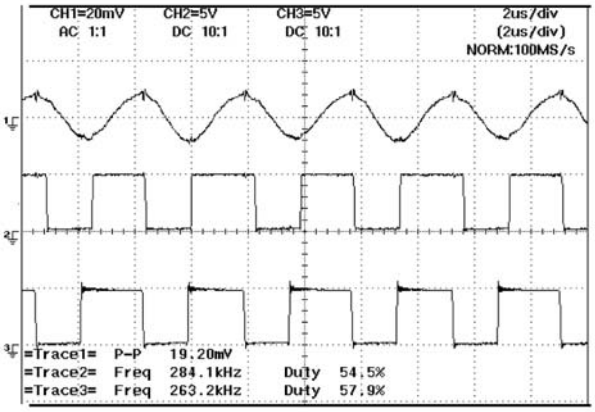
$$I_{OUT} = I1 + I2 + ... + I_N$$

Current sharing improves with increasing load current. The increasing voltage drop across the droop resistor due to increasing load current eventually swamps out the differences in regulator output voltages. If a large enough voltage can be developed across the droop resistors, current sharing accuracy will be determined solely by their matching. To realize the benefits of current sharing, it is not necessary to obtain perfect matching. Keeping output currents within ± 10% is usually acceptable.

For microprocessor applications, the value of the droop resistor must be selected to optimize adaptive voltage positioning, current sharing, current limit and efficiency. Current sharing is realized by simply connecting the COMP pins of the respective buck regulators, as shown in Figure 31.

Figure 32 shows operation with no load. In this case, there is insufficient output voltage ripple across the droop resistor to produce complete synchronization. Duty Cycle is close to the theoretical 56% (V_{OUT}/V_{IN}) resulting in a switching frequency of approximately 275 kHz.

Figure 34 shows operation with a 30 Amp load. Synchronization between the two regulators is now obtained due to increased ripple voltage. Increases losses cause the V^2 control loop to increase on−time to compensate. This results in a larger duty cycle and a corresponding decrease in switching frequency to 233 kHz.



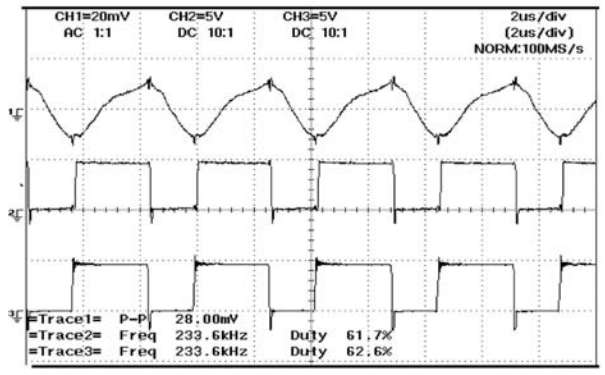
Trace 1 = Output voltage ripple.

Trace 2 = Buck regulator #1 inductor switching node.

Trace 3 = Buck regulator #2 inductor switching node.

Figure 32. No Load Waveforms

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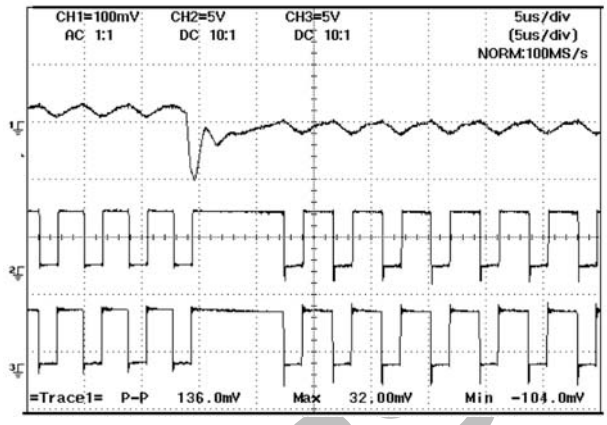


Trace 1 = Output voltage ripple.

Trace 2 = Buck regulator #1 inductor switching node.

Trace 3 = Buck regulator #2 inductor switching node.

Figure 33. 15 A Load Transient Waveforms



Trace 1 = Output voltage ripple.

Trace 2 = Buck regulator #1 inductor switching node.

Trace 3 = Buck regulator #2 inductor switching node.

Figure 34. 30 A Load Waveforms

Figure 33 shows supply response to a 15 A load step with a 30 A/μs slew rate. The V^2 control loop immediately forces the duty cycle to 100%, ramping the current in both inductors up. A voltage spike of 136 mV due to output capacitor impedance occurs. The inductive component of the spike due to ESL recovers within several microseconds. The resistive component due to ESR decreases as inductor current replaces capacitor current.

The benefit of adaptive voltage positioning in reducing the voltage spike can readily be seen. The difference in DC voltage and duty cycle can also be observed. This particular transient occurred near the beginning of regulator off time, resulting in a longer recovery time and increased voltage spike.

Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

Inductor Ripple Current

$$\text{Ripple Current} = \frac{[(V_{IN} - V_{OUT}) \times V_{OUT}]}{(\text{Switching Frequency} \times L \times V_{IN})}$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Freq = 200 kHz

$$\text{Ripple Current} = \frac{[(5.0\text{ V} - 2.8\text{ V}) \times 2.8\text{ V}]}{[200\text{ kHz} \times 1.2\ \mu\text{H} \times 5.0\text{ V}]} = 5.1\text{ A}$$

Output Ripple Voltage

V_{RIPPLE} = Inductor Ripple Current × Output Capacitor ESR

Example:

V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Switching Frequency = 200 kHz

Output Ripple Voltage = 5.1 A × Output Capacitor ESR (from manufacturer's specs)

ESR of Output Capacitors to limit Output Voltage Spikes

$$\text{ESR} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

This applies for current spikes that are faster than regulator response time. Printed Circuit Board resistance will add to the ESR of the output capacitors.

In order to limit spikes to 100 mV for a 14.2 A Load Step, ESR = 0.1/14.2 = 0.007 Ω

Inductor Peak Current

$$\text{Peak Current} = \text{Maximum Load Current} + \left(\frac{\text{Ripple Current}}{2}\right)$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, I_{LOAD} = 14.2 A, L = 1.2 μH, Freq = 200 kHz

$$\text{Peak Current} = 14.2\text{ A} + (5.1/2) = 16.75\text{ A}$$

A key consideration is that the inductor must be able to deliver the Peak Current at the switching frequency without saturating.

Response Time to Load Increase

(limited by Inductor value unless Maximum On−Time is exceeded)

$$\text{Response Time} = \frac{L \times \Delta I_{OUT}}{(V_{IN} - V_{OUT})}$$

Example: V_{IN} = +5.0 V, V_{OUT} = +2.8 V, L = 1.2 μH, 14.2 A change in Load Current

$$\text{Response Time} = \frac{1.2\ \mu\text{H} \times 14.2\text{ A}}{(5.0\text{ V} - 2.8\text{ V})} = 7.7\ \mu\text{s}$$

Response Time to Load Decrease

(limited by Inductor value)

$$\text{Response Time} = \frac{L \times \text{Change in } I_{OUT}}{V_{OUT}}$$

Example: V_{OUT} = +2.8 V, 14.2 A change in Load Current, L = 1.2 μH

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$$\text{Response Time} = \frac{1.2\ \mu\text{H} \times 14.2\ \text{A}}{2.8\ \text{V}} = 6.1\ \mu\text{s}$$

Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

THERMAL MANAGEMENT

Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of 150°C or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$\text{Thermal Impedance} = \frac{T_{J(MAX)} - T_A}{\text{Power}}$$

A heatsink may be added to TO−220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

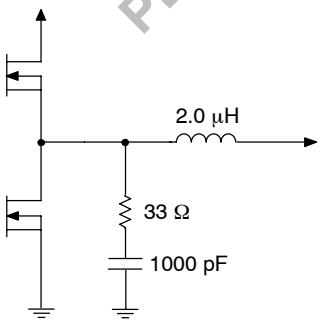


Figure 35. Filter Components

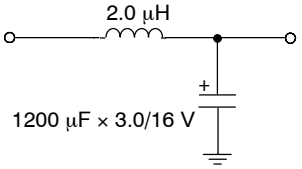


Figure 36. Input Filter

Layout Guidelines

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5166.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections. Avoid connecting the IC GND (LGND) between the source of the lower FET and the input capacitor GND.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double−sided PCBs a single large ground plane (usually the bottom) is recommended.
5. Even though double sided PCBs are usually sufficient for a good layout, four−layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the +5.0 V and GND planes, the top layer for the power connections and component vias, and the bottom layer for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The FET gate traces to the IC must be as short, straight, and wide as possible. Ideally, the IC has to be placed right next to the FETs.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching FET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the V_{FB} filter resistor in series with theV_{FB} pin (pin 16) right at the pin.
12. Place the V_{FB} filter capacitor right at the V_{FB} pin (pin 16).
13. The “Droop” Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
14. Place the V_{CC} bypass capacitor as close as possible to the V_{CC} pin and connect it to the PGND pin of the IC. Connect the PGND pin directly to the GND plane.

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15. Create a subground (local GND) plane preferably on the PCB top layer and under the IC controller. Connect all logic capacitor returns and the LGND pin of the IC to this place. Connect the subground plane to the main GND plane using a minimum of four (4) vias.

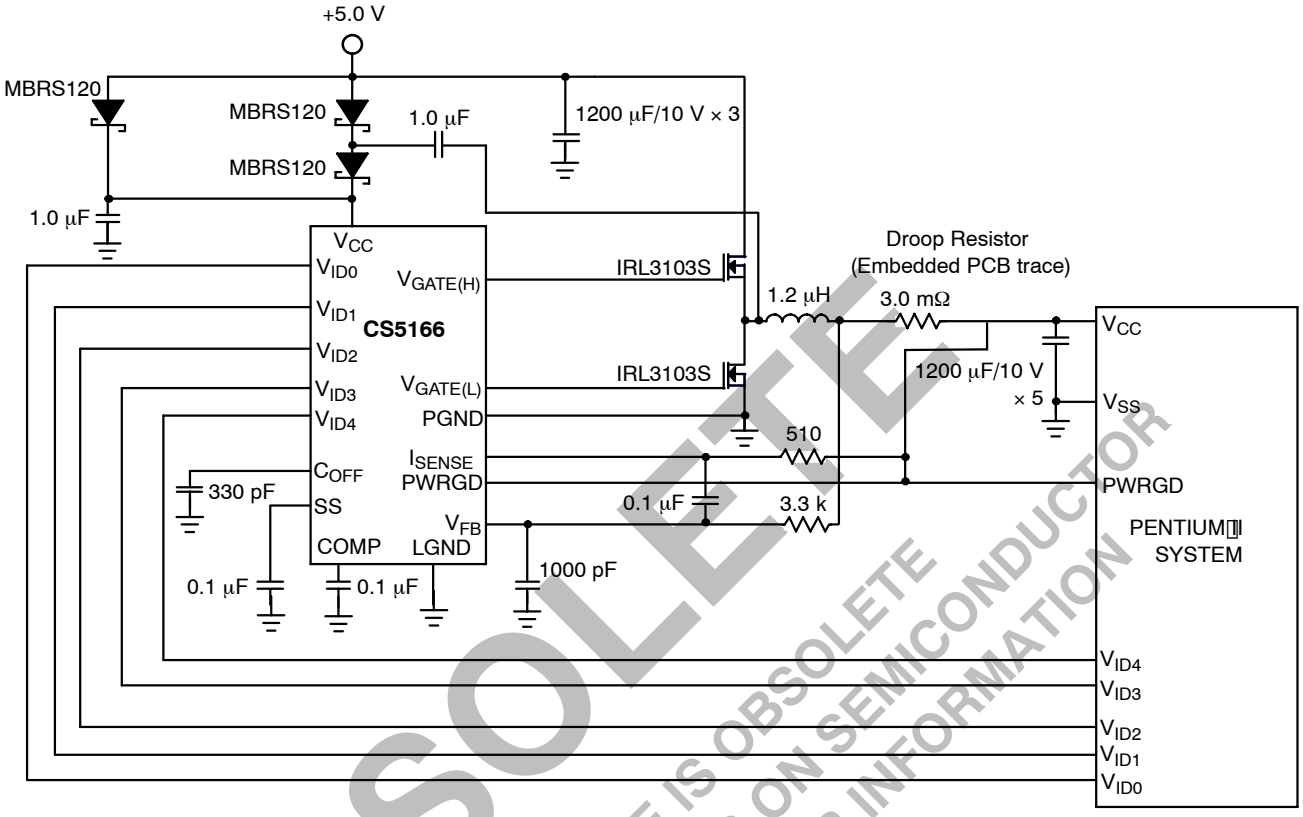
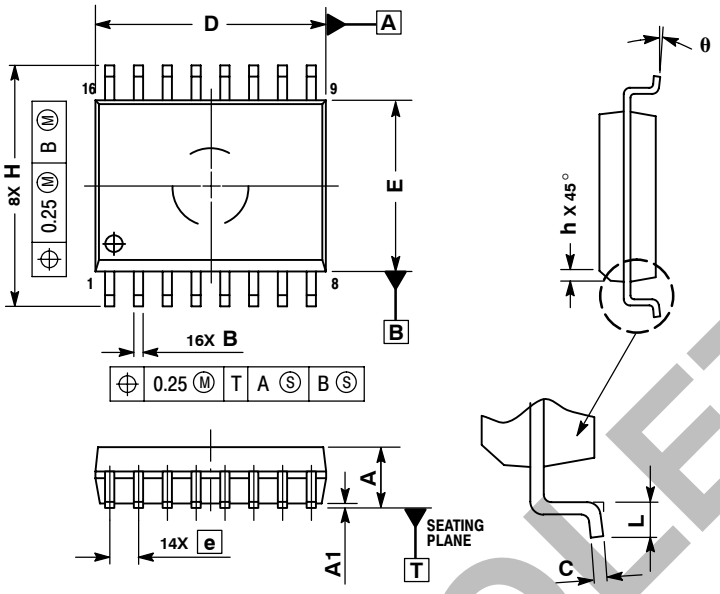


Figure 37. Additional Application Diagram, +5.0 V to +2.8 V @ 14.2 A for 300 MHz Pentium II

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PACKAGE DIMENSIONS

SO−16L
DW SUFFIX
CASE 751G−03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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PACKAGE THERMAL DATA

Parameter		SO−16L	Unit
$R_{\Theta JC}$	Typical	23	°C/W
$R_{\Theta JA}$	Typical	105	°C/W

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