

## Setting Up the Evaluation Board for the ADCLK950

### PACKAGE LIST

**Evaluation board with ADCLK950 component installed**

**Applicable documents (schematic, layout)**

### GENERAL DESCRIPTION

This user guide describes how to set up and use the evaluation board for the [ADCLK950](#). The ADCLK950 data sheet should be used in conjunction with this user guide.

The data sheet contains full technical details about the specifications and operation of this device.

The ADCLK950 is a very high performance clock fanout buffer. The evaluation board is fabricated using a high quality Rogers dielectric material. Transmission line paths are kept as close to 50  $\Omega$  as possible.

### DIGITAL PICTURE OF EVALUATION BOARD

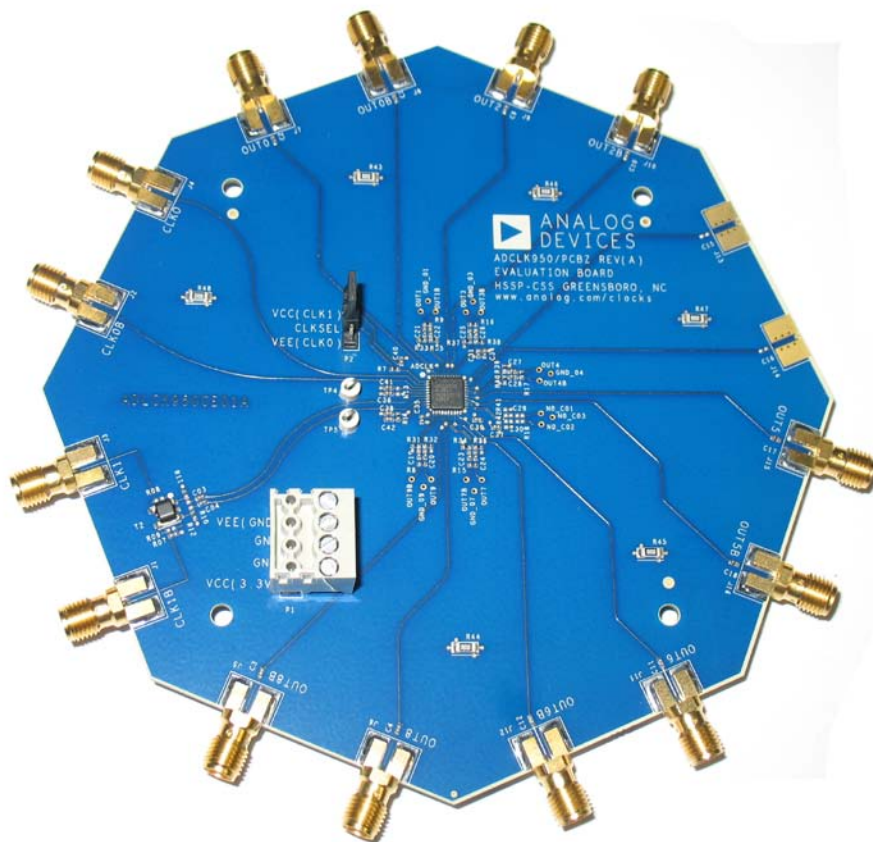


Figure 1. ADCLK950 Evaluation Board

08666-101

**TABLE OF CONTENTS**

Package List .....	1	Recommended Board Setup .....	3
General Description .....	1	Clock Outputs.....	4
Digital Picture of Evaluation Board .....	1	Evaluation Board Schematic and Artwork.....	5
Revision History .....	2	ESD Caution.....	8
Evaluation Board Hardware.....	3		

**REVISION HISTORY**

**11/09—Revision 0: Initial Version**

## EVALUATION BOARD HARDWARE

### RECOMMENDED BOARD SETUP

The recommended setup for the ADCLK950 evaluation board is shown in Figure 2.  $V_{CC}$  is set to 3.3 V and  $V_{EE}$  is set to GND. The CLKSEL jumper (P2) is provided to select the desired input configuration.

On the evaluation board, Input CLK0 and Input  $\overline{\text{CLK0}}$  are set up for dc-coupled operation to the ADCLK950 via J2 and J4. This input configuration requires the user to provide the appropriate ac swing and common-mode voltage to both inputs. Refer to the ADCLK950 data sheet for input specifications.

CLK1 is set up to evaluate with a single-ended source via the balun on the evaluation board. In addition, series capacitors in the path provide ac-coupled inputs to the ADCLK950. The common-mode voltage for both inputs is provided by tying

$V_{REF1}$  and  $V_{T1}$  together. This connection is made with R14 installed at the factory.

The range of the peak-to-peak input voltage swing at CLK1 is 0.2 V p-p to 1.7 V p-p. Note that output jitter performance is degraded by an input slew rate, as shown in the data sheet.

**Table 1. Basic Equipment Required**

Quantity	Description
1	Single power supply
1	Signal source
1	High bandwidth oscilloscope
1	High bandwidth differential probe (optional)
4	Matched high speed cables

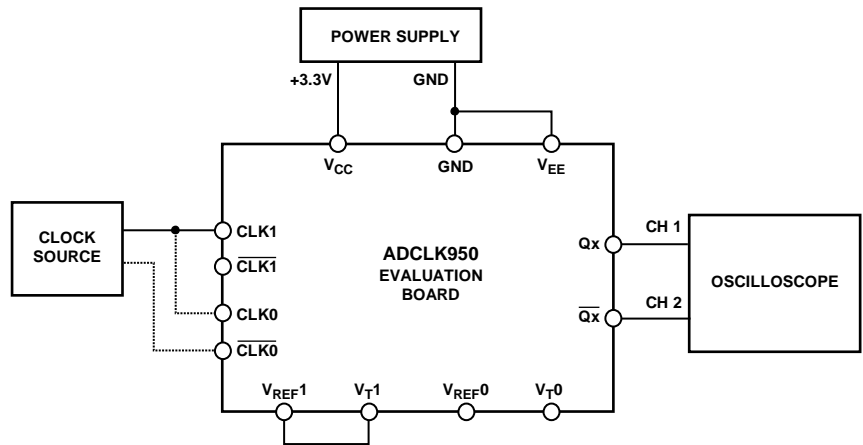


Figure 2. Recommended Setup for Device Evaluation

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**CLOCK OUTPUTS**

The ADCLK950 has 10 differential outputs. The five even-ordered differential clock outputs on the evaluation board are biased to GND via 200 Ω and ac-coupled to the SMAs. From the SMAs, use matched 50 Ω coaxial cables into the oscilloscope for evaluation. The five odd-ordered differential outputs on the evaluation board are not launched. Use a high bandwidth differential probe and oscilloscope close to the ADCLK950 device for evaluation. See the evaluation board schematic in Figure 4 for more details.

**Table 2. Power Connections via P1**

Label	ADCLK950
GND	Connect to GND
VCC	Connect to 3.3 V
VEE	Connect to GND

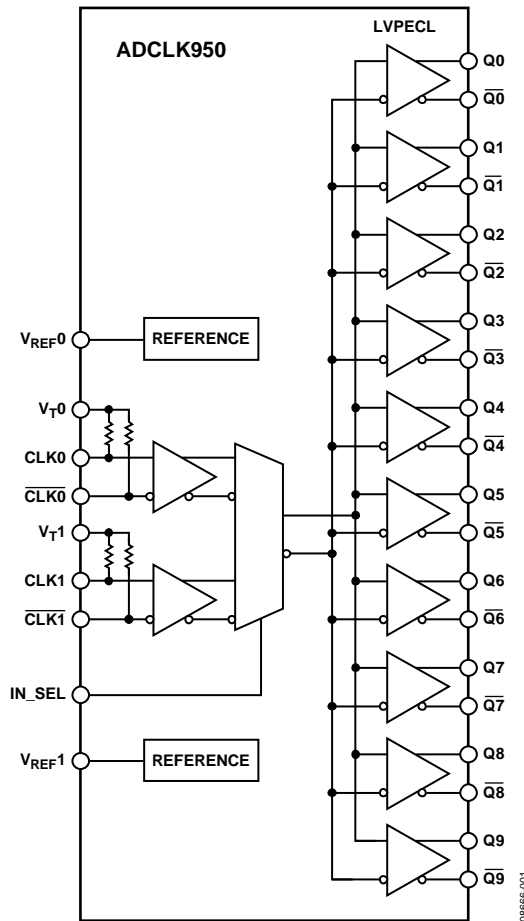


Figure 3. ADCLK950 1:10 Clock/Data Buffer Block Diagram



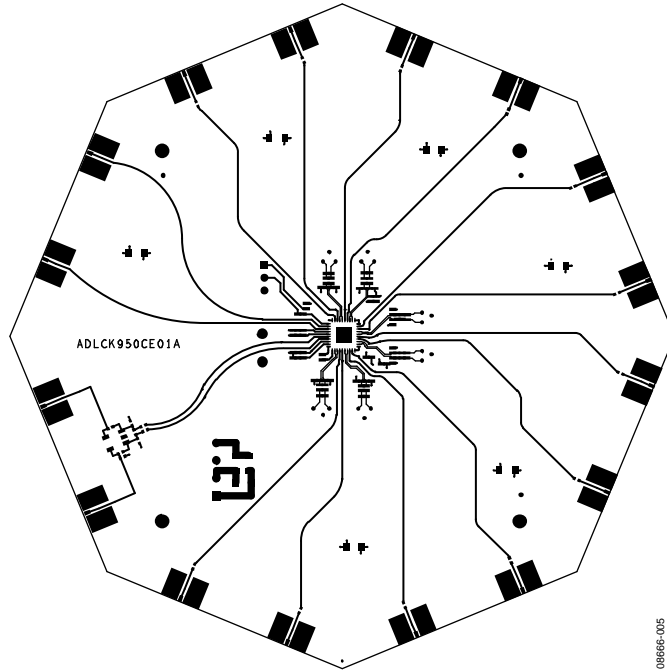


Figure 5. Top Trace Layer

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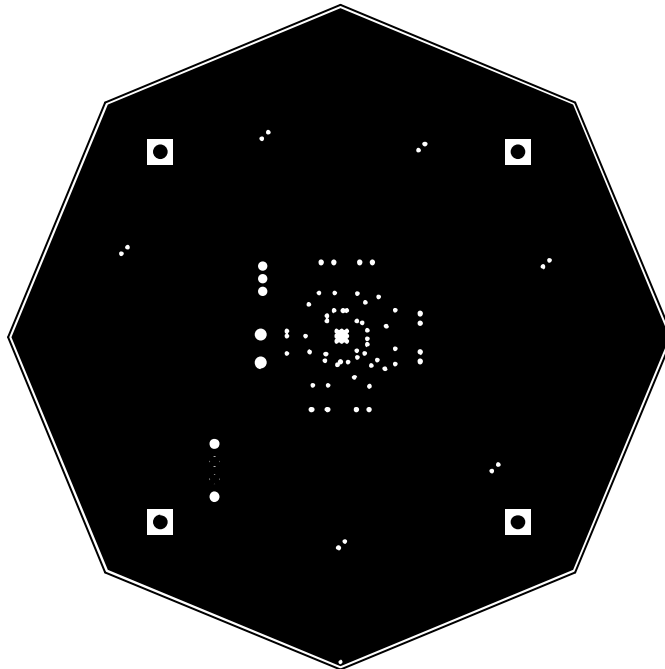


Figure 6. Ground Plane Layer

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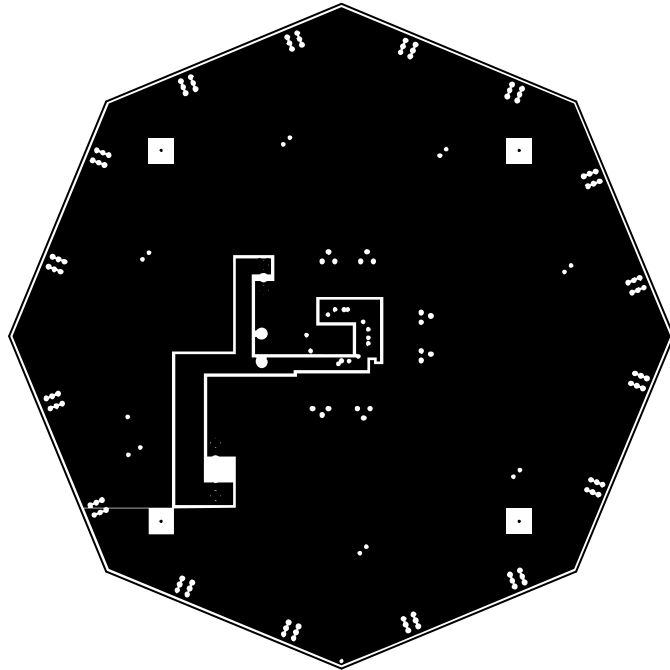


Figure 7.  $V_{CC}$  and  $V_{EE}$  Power Plane Layer

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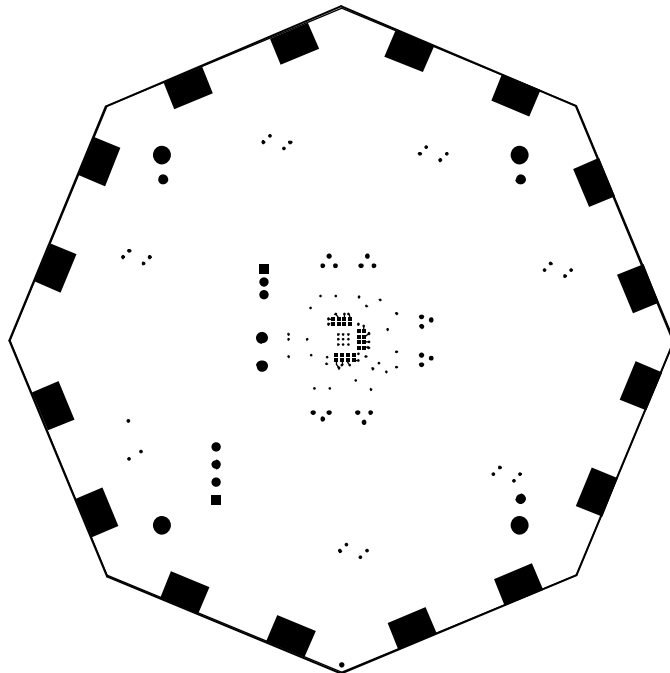


Figure 8. Bottom Trace Layer

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## NOTES

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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