

32-Bit Traveo™ Family Microcontroller Datasheet

This section provides an overview of the S6J3120 series. The S6J3120 series is a set of 32-bit microcontrollers designed for in-vehicle use. It uses the Arm® Cortex®-R5 CPU as a CPU.

Features

This section explains the features of the S6J3120 series.

Cortex-R5 Core

■ This section explains the Cortex-R5 CPU core.

- Arm Cortex-R5
- 32-bit Arm architecture
 - 2-instruction issuance super scalar
 - 8-stage pipeline
- Armv7/Thumb®-2 instruction set
- MPU (memory protection) equipped
 - 16-area support
- ECC support for the TCM ports for RAM
 - 1-bit error correction and 2-bit error detection (SEC-DED)
- TCM ports
 - 2 TCM ports
 - ATCM port
 - BTCM port (B0TCM, B1TCM)
- Caches
 - Instruction cache 16 KB
 - Data cache 16 KB
- VIC port
 - Low latency interrupt
- AXI master interface
 - 64-bit AXI interface (instruction/data access)
 - 32-bit AXI interface (I/O access)
- AXI slave interface
 - 64-bit AXI interface (TCM port access)
- ETM-R5 trace

Peripheral Functions

This section explains peripheral functions.

- Clock generation
 - Main clock oscillation (4 MHz)
 - No sub clock oscillation
 - CR oscillation (100 kHz)
 - CR oscillation (4 MHz)
- Built-in Flash memory size
 - Program: 1024 K + 64 KB (S6J312AHzC*)/768 K + 64 KB (S6J3129HzC*)
 - *z: A/B
 - Work: 112 KB (S6J312AHzC*)/ 112 KB (S6J3129HzC*)
 - *z: A/B

- Built-in RAM size
 - TCRAM 64 KB(S6J312AHzC*)/ 48 KB(S6J3129HzC*)
 - System SRAM 16 KB (S6J312AHzC*)/ 16 KB (S6J3129HzC*)
 - Backup RAM 8 KB (S6J312AHzC*)/ 8 KB (S6J3129HzC*)
 - *z: A/B
- General-purpose ports: 112 channels (S6J312AHzC*)/ 112 channels (S6J3129HzC*)
 - *z: A/B
- External bus interface
 - 24-bit address, 16-bit data
- DMA controller
 - Up to 16 channels can be activated simultaneously.
- A/D converter (successive approximation type)
 - 12-bit resolution, 2 units mounted: Max 50 channels (22 channels + 28 channels)(S6J312AHzC*)/ Max 50 channels (22 channels + 28 channels)(S6J3129HzC*)
 - *z: A/B
- External interrupt input: 16 channels
 - Level ("H"/"L") and edge (rising/falling) can be detected.
- Multi-function serial (transmission and reception FIFOs mounted) :Max 10 channels(S6J312AHzC*)/ Max 10 channels(S6J3129HzC*)
 - *z: A/B
 - <I²C>
 - Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
 - Standard mode (Max. 100 kbps) is supported only.
 - DMA transfer is supported.
 - <UART (asynchronous serial interface) >
 - Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
 - Parity check can be enabled/disabled.
 - Built-in dedicated baud rate generator
 - An external clock can be used as a transfer clock.
 - Parity, frame, overrun error detection functions are available.
 - DMA transfer is supported.
 - <CSIO (synchronous serial interface) >
 - Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
 - Support for SPI. Both master and slave roles are supported. Data length in bits can be set to a value from 5 to 16 or one of the values of 20, 24, and 32.
 - Built-in dedicated baud rate generator (master operation)
 - External clock input is enabled (slave operation).

- Overrun error detection function is available.
- DMA transfer is supported.
- Serial chip select SPI function

<LIN-UART (asynchronous serial interface for LIN) >

- Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
- Support for LIN protocol revision 2.1
- Both master and slave roles are supported.
- Framing error and overrun error detection
- LIN Synch break generation and detection, LIN Synch Delimiter generation
- Built-in dedicated baud rate generator
- The external clock can be adjusted by the reload counter.
- DMA transfer is supported.

■ CAN controller: CAN-FD Max 3 channel

- CAN-FD (V3.2.0)
- CAN transfer speed :5 Mbps
- CAN Clock :Max 40 MHz
- 192 message buffers/channel (reception message buffer size)
- 32 message buffer/channel (transmission message buffer size)

■ Base timer: MAX 30 channels

- 16-bit Timer.
- It is selectable by 4 functions of the PWM/PPG/PWC/Reload Timer.
- 2-channel cascade connection enables operation as a 32-bit timer.(PWC and Reload Timer)

■ Reload timer: Max 10 channels

- 32-bit Timer.

■ Free-run timer: Max 6 channels

- 32-bit Timer.
- Main clock oscillation and CR oscillation are available.
- Free-run timer output can work in combination with an input capture and an output compare.

■ Input capture: Max 12 channels

- 32-bit Timer.

■ Output compare: Max 12 channels

- 32-bit Timer.

■ Sound generator : Max 3 channels

- Frequency and amplitude sequencers provided.

■ Stepping motor controller : Max 4 channels

- 8-/10-bit PWM
- High current output supported (4 lines × 4 channels)
- Can refer back electromotive force using pin-shared A/D converter

■ LCD controller

- Common output : 4 , Segment output : 32
- Duty drive (SEG0 to SEG31) and static drive (ST0 to ST8) can be switched.
- Each of COM0 to COM3, SEG0 to SEG31, V0, V1, V2, and V3 pins for duty drive can be switched to the general-purpose port. (The SEG23 to SEG31 pins can be switched to static driving.)
- V0, V1, V2 and V3 pin can be used as the general-purpose port. But V3 pin cannot be used as an output pin.

- Each of ST0 to ST8 pins for static drive can be switched to the general-purpose port, or it can be switched to the segment output of duty drive.

■ Quad position & revolution counter(QPRC) : Max 2 channels

■ Real time clock (RTC) (day/hour/minute/second)

- Main clock oscillation or CR oscillation (100 kHz) can be selected as an operation clock.

■ Calibration: Real time clock (RTC) driven by the CR clock

- Correction can be done by configuring the prescaler of the real time clock based on the ratio between the main clock and the CR clock.

■ Clock supervisor

- Abnormality (such as damaged crystal) of the main clock oscillation (4 MHz) can be monitored.
- The clock can switch to the CR clock when an abnormality is detected.
- PLL abnormality can be detected.

■ CRC generation

- Fixed-length CRC
 - CCITT CRC16 generator polynomial: 0x1021
 - IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

■ DDR HS-SPI

- E²PROM and the flash device of the Single/Dual/Quad-SPI protocol can be connected.

■ Watchdog timer

- Hardware watchdog
- Software watchdog

■ NMI

■ I/O relocation

- Peripheral function pin locations can be changed.

■ Low-power consumption control

- Standby function
- Power-off function
- Partial wakeup function

■ Power-on reset

■ Low-voltage detection reset

■ Security

- Flash security
- Interface security (JTAG + test port)
- SHE
- Unique device ID

■ Package: LEU144 (S6J312xHzC*)

- *x:A/9, z: A/B

■ CMOS 55 nm technology

■ Power supply

- 5 V single power supply
- The voltage step-down circuit generates internal 1.2 V from 5 V.
- 5 V power supply is used for I/O.

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1. Product Lineup

The following table lists the product lineup of the S6J3120 series.

Table 1-1 Memory Size

		S6J312AHzC*	S6J3129HzC*
Flash	Program	1024 KBytes + Small sector (8 KB x 8)	768 KBytes + Small sector (8 KB x 8)
	Work	112 KBytes	112 KBytes
RAM	TCRAM	64 KBytes	48 KBytes
	System SRAM	16 KBytes	16 KBytes
	Backup RAM	8 KBytes	8 KBytes

*z: A/B

Table 1-2 SHE Option

	S6J312xHAC*	S6J312xHBC*
Security (SHE)	ON	OFF

* x: A/9

Table 1-3: Product Lineup

	S6J312xHzC*1
CPU core	Coretex-R5
CMOS 55 nm technology	55 nm
Package	LEU144
Main clock	4 MHz
Built-in CR oscillator	100 kHz
	4 MHz
Maximum CPU operating frequency	128 MHz
Watchdog timer	1 channel (hardware) 1 channel (software)
Clock supervisor	YES
External power supply, low-voltage detection reset	YES
Internal power supply, low-voltage detection reset	YES
NMI request	YES
External interrupt	16 channels
DMA controller	16 channels
CAN-FD	3 channels (192 msg buffers/ch)
Multi-function serial	10 channels*2
A/D converter	12-bit (2 units) Unit 0 x 22 channels Unit 1 x 28 channels
Free-run timer	6 channels
Input capture	12 channels
Output compare	12 channels

	S6J312xHzC*¹
Base timer (16-bit)	30 channels
Real time clock (RTC)	1 channel
CR clock calibration	YES
CRC generation	YES
Low-power consumption mode	Standby function Power-off function Partial wakeup function
SHE	YES
External BUS I/F	Address : 24-bit Data :16-bit
Reload Timer(32-bit)	10 channels
Quad Position & Revolution Counter	2 channels
DDR HS-SPI	YES
LCD Controller	32 seg x 4 com (Static drive 8 seg x 1 com)
Sound Generator	3 channels
Stepping Motor Controller	4 channels
General-purpose port GPIO	112 channels
Power supply	5 V ± 10 %
Operation assurance temperature (Ta)	-40 °C to +105 °C
On-chip debugger (JTAG)	YES

*¹: x: A/9, z: A/B

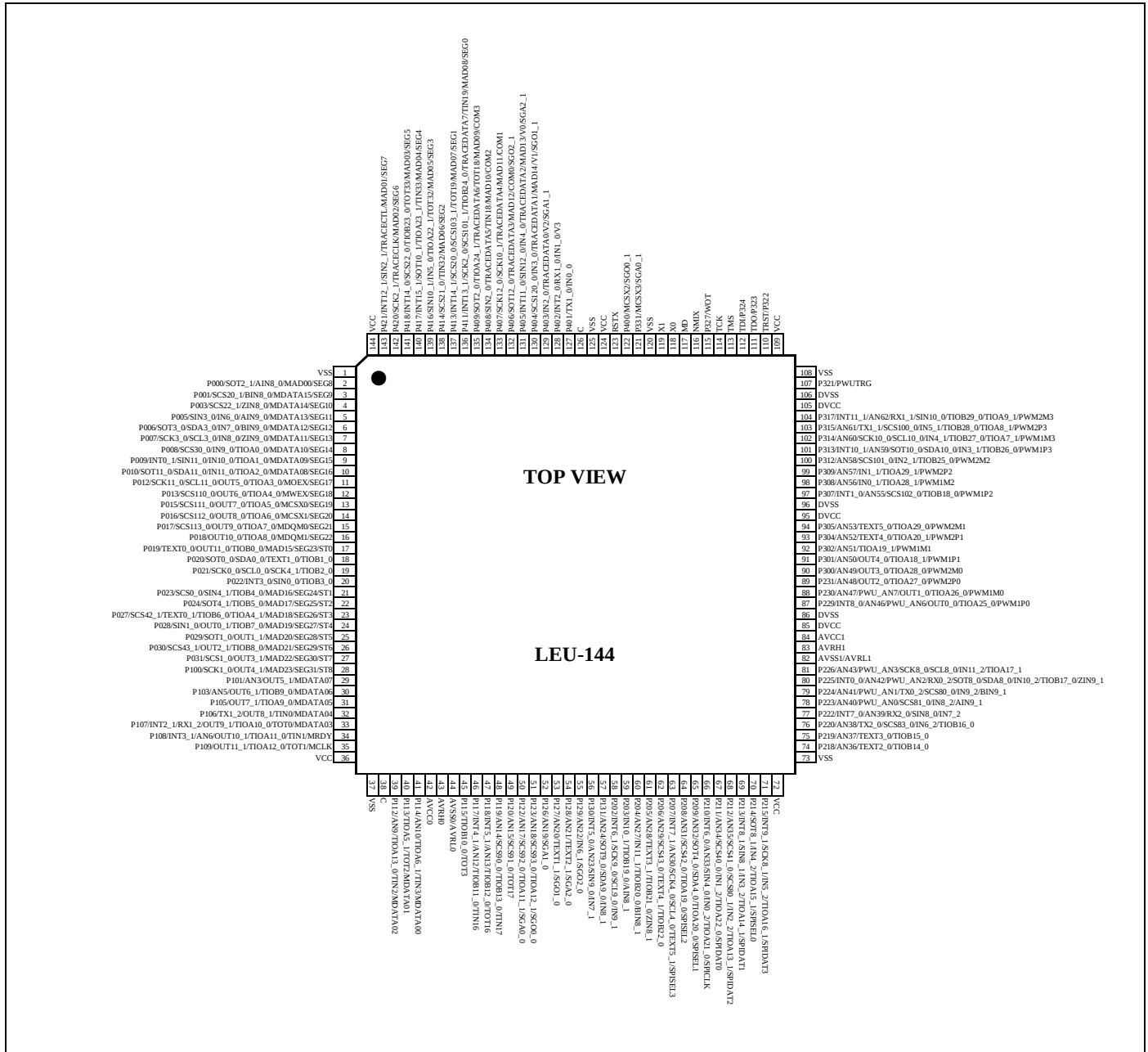
*²: I²C-UART function is not supported at Multi-function serial ch.1, ch.2, and ch.12.

2. Pin Assignment

The following figures show the pin assignment of the S6J3120 series.

Figure 2-1 Pin Assignment for S6J312xHzC*

* x: A/9, z: A/B



3. Pin Description

This section provides a list of the pin functions of the S6J3120 series

Table 3-1 S6J312xHzC* Pin Functions

* x: A/9, z: A/B

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
2	P000 SOT2_1 AIN8_0 MAD00 SEG8	- - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial data output pin (1) QPRC ch.8 AIN input pin (0) External bus interface address bit0 output pin LCDC segment 8 (Duty) output pin
3	P001 SCS20_1 BIN8_0 MDATA15 SEG9	- - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial chip select 0 I/O pin (1) QPRC ch.8 BIN input pin (0) External bus interface data bus bit15 I/O pin LCDC segment 9 (Duty) output pin
4	P003 SCS22_1 ZIN8_0 MDATA14 SEG10	- - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial chip select 2 output pin (1) QPRC ch.8 ZIN input pin (0) External bus interface data bus bit14 I/O pin LCDC segment 10 (Duty) output pin
5	P005 SIN3_0 IN6_0 AIN9_0 MDATA13 SEG11	- - - - - -	K	General-purpose I/O port Multi-function serial ch.3 serial data input pin (0) Input capture ch.6 input pin (0) QPRC ch.9 AIN input pin (0) External bus interface data bus bit13 I/O pin LCDC segment 11 (Duty) output pin
6	P006 SOT3_0 SDA3_0 IN7_0 BIN9_0 MDATA12 SEG12	- - - - - -	K	General-purpose I/O port Multi-function serial ch.3 serial data output pin (0) I ² C bus ch.3 serial data I/O pin Input capture ch.7 input pin (0) QPRC ch.9 BIN input pin (0) External bus interface data bus bit12 I/O pin LCDC segment 12 (Duty) output pin
7	P007 SCK3_0 SCL3_0 IN8_0 ZIN9_0 MDATA11 SEG13	- - - - - -	K	General-purpose I/O port Multi-function serial ch.3 clock I/O pin (0) I ² C bus ch.3 serial clock I/O pin Input capture ch.8 input pin (0) QPRC ch.9 ZIN input pin (0) External bus interface data bus bit11 I/O pin LCDC segment 13 (Duty) output pin
8	P008 SCS30_0 IN9_0 TIOA0_0 MDATA10 SEG14	- - - - - -	K	General-purpose I/O port Multi-function serial ch.3 serial chip select 0 I/O pin (0) Input capture ch.9 input pin (0) Base timer ch.0 TIOA output pin (0) External bus interface data bus bit10 I/O pin LCDC segment 14 (Duty) output pin
9	P009 INT0_1 SIN11_0 IN10_0 TIOA1_0 MDATA09 SEG15	- - - - - -	K	General-purpose I/O port INT0 external interrupt input pin (1) Multi-function serial ch.11 serial data input pin (0) Input capture ch.10 input pin (0) Base timer ch.1 TIOA I/O pin (0) External bus interface data bus bit9 I/O pin LCDC segment 15 (Duty) output pin

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
10	P010 SOT11_0 SDA11_0 IN11_0 TIOA2_0 MDATA08 SEG16	- - - - - - -	K	General-purpose I/O port Multi-function serial ch.11 serial data output pin (0) I ² C bus ch.11 serial data I/O pin Input capture ch.11 input pin (0) Base timer ch.2 TIOA output pin (0) External bus interface data bus bit8 I/O pin LCDC segment 16 (Duty) output pin
11	P012 SCK11_0 SCL11_0 OUT5_0 TIOA3_0 MOEX SEG17	- - - - - - -	K	General-purpose I/O port Multi-function serial ch.11 clock I/O pin (0) I ² C bus ch.11 serial clock I/O pin Output compare ch.5 output pin (0) Base timer ch.3 TIOA I/O pin (0) External bus interface read enable output pin LCDC segment 17 (Duty) output pin
12	P013 SCS110_0 OUT6_0 TIOA4_0 MWEX SEG18	- - - - - -	K	General-purpose I/O port Multi-function serial ch.11 serial chip select 0 I/O pin (0) Output compare ch.6 output pin (0) Base timer ch.4 TIOA output pin (0) External bus interface write enable output pin LCDC segment 18 (Duty) output pin
13	P015 SCS111_0 OUT7_0 TIOA5_0 MCSX0 SEG19	- - - - - -	K	General-purpose I/O port Multi-function serial ch.11 serial chip select 1 output pin (0) Output compare ch.7 output pin (0) Base timer ch.5 TIOA I/O pin (0) External bus interface chip select 0 output pin LCDC segment 19 (Duty) output pin
14	P016 SCS112_0 OUT8_0 TIOA6_0 MCSX1 SEG20	- - - - - -	K	General-purpose I/O port Multi-function serial ch.11 serial chip select 2 output pin (0) Output compare ch.8 output pin (0) Base timer ch.6 TIOA output pin (0) External bus interface chip select 1 output pin LCDC segment 20 (Duty) output pin
15	P017 SCS113_0 OUT9_0 TIOA7_0 MDQM0 SEG21	- - - - - -	K	General-purpose I/O port Multi-function serial ch.11 serial chip select 3 output pin (0) Output compare ch.9 output pin (0) Base timer ch.7 TIOA I/O pin (0) External bus interface byte mask 0 output pin LCDC segment 21 (Duty) output pin
16	P018 OUT10_0 TIOA8_0 MDQM1 SEG22	- - - - -	K	General-purpose I/O port Output compare ch.10 output pin (0) Base timer ch.8 TIOA output pin (0) External bus interface byte mask 1 output pin LCDC segment 22 (Duty) output pin
17	P019 TEXT0_0 OUT11_0 TIOB0_0 MAD15 SEG23/ST0	- - - - - -	K	General-purpose I/O port Free-run timer 0 clock input pin (0) Output compare ch.11 output pin (0) Base timer ch.0 TIOB input pin (0) External bus interface address bit15 output pin LCDC segment 23 (Duty) / segment 0 (Static) output pin
18	P020 SOT0_0 SDA0_0 TEXT1_0 TIOB1_0	- - - - -	Q	General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I ² C bus ch.0 serial data I/O pin Free-run timer 1 clock input pin (0) Base timer ch.1 TIOB input pin (0)

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
19	P021 SCK0_0 SCL0_0 SCK4_1 TIOB2_0	- - - - -	Q	General-purpose I/O port Multi-function serial ch.0 clock I/O pin (0) I ² C bus ch.0 serial clock I/O pin Multi-function serial ch.4 clock I/O pin (1) Base timer ch.2 TIOB input pin (0)
20	P022 INT3_0 SIN0_0 TIOB3_0	- - - -	Q	General-purpose I/O port INT3 external interrupt input pin (0) Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0)
21	P023 SCS0_0 SIN4_1 TIOB4_0 MAD16 SEG24/ST1	- - - - - -	K	General-purpose I/O port Multi-function serial ch.0 serial chip select 0 I/O pin (0) Multi-function serial ch.4 serial data input pin (1) Base timer ch.4 TIOB input pin (0) External bus interface address bit16 output pin LCDC segment 24 (Duty) / segment 1 (Static) output pin
22	P024 SOT4_1 TIOB5_0 MAD17 SEG25/ST2	- - - - -	K	General-purpose I/O port Multi-function serial ch.4 serial data output pin (1) Base timer ch.5 TIOB input pin (0) External bus interface address bit17 output pin LCDC segment 25 (Duty) / segment 2 (Static) output pin
23	P027 SCS42_1 TEXT0_1 TIOB6_0 TIOA4_1 MAD18 SEG26/ST3	- - - - - -	K	General-purpose I/O port Multi-function serial ch.4 serial chip select 2 output pin (1) Free-run timer 0 clock input pin (1) Base timer ch.6 TIOB input pin (0) Base timer ch.4 TIOA output pin (1) External bus interface address bit18 output pin LCDC segment 26 (Duty) / segment 3 (Static) output pin
24	P028 SIN1_0 OUT0_1 TIOB7_0 MAD19 SEG27/ST4	- - - - - -	K	General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Output compare ch.0 output pin (1) Base timer ch.7 TIOB input pin (0) External bus interface address bit19 output pin LCDC segment 27 (Duty) / segment 4 (Static) output pin
25	P029 SOT1_0 OUT1_1 MAD20 SEG28/ST5	- - - - -	K	General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) Output compare ch.1 output pin (1) External bus interface address bit20 output pin LCDC segment 28 (Duty) / segment 5 (Static) output pin
26	P030 SCS43_1 OUT2_1 TIOB8_0 MAD21 SEG29/ST6	- - - - - -	K	General-purpose I/O port Multi-function serial ch.4 serial chip select 3 output pin (1) Output compare ch.2 output pin (1) Base timer ch.8 TIOB input pin (0) External bus interface address bit21 output pin LCDC segment 29 (Duty) / segment 6 (Static) output pin
27	P031 SCS1_0 OUT3_1 MAD22 SEG30/ST7	- - - - -	K	General-purpose I/O port Multi-function serial ch.1 serial chip select 0 I/O pin (0) Output compare ch.3 output pin (1) External bus interface address bit22 output pin LCDC segment 30 (Duty) / segment 7 (Static) output pin
28	P100 SCK1_0 OUT4_1 MAD23 SEG31/ST8	- - - - -	K	General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) Output compare ch.4 output pin (1) External bus interface address bit23 output pin LCDC segment 31 (Duty) / segment 8 (Static) output pin

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
29	P101 AN3 OUT5_1 MDATA07	- - - -	B	General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1) External bus interface data bit7 I/O pin
30	P103 AN5 OUT6_1 TIOB9_0 MDATA06	- - - - -	B	General-purpose I/O port ADC analog 5 input pin Output compare ch.6 output pin (1) Base timer ch.9 TIOB input pin (0) External bus interface data bit6 I/O pin
31	P105 OUT7_1 TIOA9_0 MDATA05	- - - -	Q	General-purpose I/O port Output compare ch.7 output pin (1) Base timer ch.9 TIOA I/O pin (0) External bus interface data bit5 I/O pin
32	P106 TX1_2 OUT8_1 TIN0 MDATA04	- - - - -	Q	General-purpose I/O port CAN transmission data 1 output pin (2) Output compare ch.8 output pin (1) Reload timer ch.0 event input pin (0) External bus interface data bit4 I/O pin
33	P107 INT2_1 RX1_2 OUT9_1 TIOA10_0 TOT0 MDATA03	- - - - - - -	Q	General-purpose I/O port INT2 external interrupt input pin (1) CAN reception data 1 input pin (2) Output compare ch.9 output pin (1) Base timer ch.10 TIOA output pin (0) Reload timer ch.0 output pin (0) External bus interface data bit3 I/O pin
34	P108 INT3_1 AN6 OUT10_1 TIOA11_0 TIN1 MRDY	- - - - - - -	B	General-purpose I/O port INT3 external interrupt input pin (1) ADC analog 6 input pin Output compare ch.10 output pin (1) Base timer ch.11 TIOA I/O pin (0) Reload timer ch.1 event input pin (0) External bus interface ready input pin
35	P109 OUT11_1 TIOA12_0 TOT1 MCLK	- - - - -	Q	General-purpose I/O port Output compare ch.11 output pin (1) Base timer ch.12 TIOA output pin (0) Reload timer ch.1 output pin (0) External bus interface system clock output pin
39	P112 AN9 TIOA13_0 TIN2 MDATA02	- - - - -	B	General-purpose I/O port ADC analog 9 input pin Base timer ch.13 TIOA I/O pin (0) Reload timer ch.2 event input pin (0) External bus interface data bit2 I/O pin
40	P113 TIOA5_1 TOT2 MDATA01	- - - -	Q	General-purpose I/O port Base timer ch.5 TIOA I/O pin (1) Reload timer ch.2 output pin (0) External bus interface data bit1 I/O pin
41	P114 AN10 TIOA6_1 TIN3 MDATA00	- - - - -	B	General-purpose I/O port ADC analog 10 input pin Base timer ch.6 TIOA output pin (1) Reload timer ch.3 event input pin (0) External bus interface data bit0 I/O pin
45	P115 TIOB10_0 TOT3	- - -	Q	General-purpose I/O port Base timer ch.10 TIOB input pin (0) Reload timer ch.3 output pin (0)

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
46	P117 INT4_1 AN12 TIOB11_0 TIN16	- - - - -	B	General-purpose I/O port INT4 external interrupt input pin (1) ADC analog 12 input pin Base timer ch.11 TIOB input pin (0) Reload timer ch.16 event input pin (0)
47	P118 INT5_1 AN13 TIOB12_0 TOT16	- - - - -	B	General-purpose I/O port INT5 external interrupt input pin (1) ADC analog 13 input pin Base timer ch.12 TIOB input pin (0) Reload timer ch.16 output pin (0)
48	P119 AN14 SCS90_0 TIOB13_0 TIN17	- - - - -	B	General-purpose I/O port ADC analog 14 input pin Multi-function serial ch.9 serial chip select 0 I/O pin (0) Base timer ch.13 TIOB input pin (0) Reload timer ch.17 event input pin (0)
49	P120 AN15 SCS91_0 TOT17	- - - -	B	General-purpose I/O port ADC analog 15 input pin Multi-function serial ch.9 serial chip select 1 output pin (0) Reload timer ch.17 output pin (0)
50	P122 AN17 SCS92_0 TIOA11_1 SGA0_0	- - - - -	B	General-purpose I/O port ADC analog 17 input pin Multi-function serial ch.9 serial chip select 2 output pin (0) Base timer ch.11 TIOA I/O pin (1) Sound generator ch.0 SGA output pin (0)
51	P123 AN18 SCS93_0 TIOA12_1 SGO0_0	- - - - -	B	General-purpose I/O port ADC analog 18 input pin Multi-function serial ch.9 serial chip select 3 output pin (0) Base timer ch.12 TIOA output pin (1) Sound generator ch.0 SGO output pin (0)
52	P126 AN19 SGA1_0	- - -	B	General-purpose I/O port ADC analog 19 input pin Sound generator ch.1 SGA output pin (0)
53	P127 AN20 TEXT1_1 SGO1_0	- - - -	B	General-purpose I/O port ADC analog 20 input pin Free-run timer 1 clock input pin (1) Sound generator ch.1 SGO output pin (0)
54	P128 AN21 TEXT2_1 SGA2_0	- - - -	B	General-purpose I/O port ADC analog 21 input pin Free-run timer 2 clock input pin (1) Sound generator ch.2 SGA output pin (0)
55	P129 AN22 IN6_1 SGO2_0	- - - -	B	General-purpose I/O port ADC analog 22 input pin Input capture ch.6 input pin (1) Sound generator ch.2 SGO output pin (0)
56	P130 INT5_0 AN23 SIN9_0 IN7_1	- - - - -	B	General-purpose I/O port INT5 external interrupt input pin (0) ADC analog 23 input pin Multi-function serial ch.9 serial data input pin (0) Input capture ch.7 input pin (1)
57	P131 AN24 SOT9_0 SDA9_0 IN8_1	- - - - -	B	General-purpose I/O port ADC analog 24 input pin Multi-function serial ch.9 serial data output pin (0) I ² C bus ch.9 serial data I/O pin Input capture ch.8 input pin (1)

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
58	P202 INT6_1 SCK9_0 SCL9_0 IN9_1	- - - - -	Q	General-purpose I/O port INT6 external interrupt input pin (1) Multi-function serial ch.9 clock I/O pin (0) I ² C bus ch.9 serial clock I/O pin Input capture ch.9 input pin (1)
59	P203 IN10_1 TIOB19_0 AIN8_1	- - - -	Q	General-purpose I/O port Input capture ch.10 input pin (1) Base timer ch.19 TIOB input pin (0) QPRC ch.8 AIN input pin (1)
60	P204 AN27 IN11_1 TIOB20_0 BIN8_1	- - - - -	B	General-purpose I/O port ADC analog 27 input pin Input capture ch.11 input pin (1) Base timer ch.20 TIOB input pin (0) QPRC ch.8 BIN input pin (1)
61	P205 AN28 TEXT3_1 TIOB21_0 ZIN8_1	- - - - -	B	General-purpose I/O port ADC analog 28 input pin Free-run timer 3 clock input pin (1) Base timer ch.21 TIOB input pin (0) QPRC ch.8 ZIN input pin (1)
62	P206 AN29 SCS43_0 TEXT4_1 TIOB22_0	- - - - -	B	General-purpose I/O port ADC analog 29 input pin Multi-function serial ch.4 serial chip select 3 output pin (0) Free-run timer 4 clock input pin (1) Base timer ch.22 TIOB input pin (0)
63	P207 INT7_1 AN30 SCK4_0 SCL4_0 TEXT5_1 SPISEL3	- - - - - - -	B	General-purpose I/O port INT7 external interrupt input pin (1) ADC analog 30 input pin Multi-function serial ch.4 clock I/O pin (0) I ² C bus ch.4 serial clock I/O pin Free-run timer 5 clock input pin (1) HS-SPI slave select 3 output pin
64	P208 AN31 SCS42_0 TIOA19_0 SPISEL2	- - - - -	B	General-purpose I/O port ADC analog 31 input pin Multi-function serial ch.4 serial chip select 2 output pin (0) Base timer ch.19 TIOA I/O pin (0) HS-SPI slave select 2 output pin
65	P209 AN32 SOT4_0 SDA4_0 TIOA20_0 SPISEL1	- - - - - -	B	General-purpose I/O port ADC analog 32 input pin Multi-function serial ch.4 serial data output pin (0) I ² C bus ch.4 serial data I/O pin Base timer ch.20 TIOA output pin (0) HS-SPI slave select 1 output pin
66	P210 INT6_0 AN33 SIN4_0 IN0_2 TIOA21_0 SPICLK	- - - - - - -	B	General-purpose I/O port INT6 external interrupt input pin (0) ADC analog 33 input pin Multi-function serial ch.4 serial data input pin (0) Input capture ch.0 input pin (2) Base timer ch.21 TIOA I/O pin (0) HS-SPI clock output pin

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
67	P211 AN34 SCS40_0 IN1_2 TIOA22_0 SPIDAT0	- - - - - -	B	General-purpose I/O port ADC analog 34 input pin Multi-function serial ch.4 serial chip select 0 I/O pin (0) Input capture ch.1 input pin (2) Base timer ch.22 TIOA output pin (0) HS-SPI data 0 I/O pin
68	P212 AN35 SCS41_0 SCS80_1 IN2_2 TIOA13_1 SPIDAT2	- - - - - - -	B	General-purpose I/O port ADC analog 35 input pin Multi-function serial ch.4 serial chip select 1 output pin (0) Multi-function serial ch.8 serial chip select 0 I/O pin (1) Input capture ch.2 input pin (2) Base timer ch.13 TIOA I/O pin (1) HS-SPI data 2 I/O pin
69	P213 INT8_1 SIN8_1 IN3_2 TIOA14_1 SPIDAT1	- - - - - -	Q	General-purpose I/O port INT8 external interrupt input pin (1) Multi-function serial ch.8 serial data input pin (1) Input capture ch.3 input pin (2) Base timer ch.14 TIOA output pin (1) HS-SPI data 1 I/O pin
70	P214 SOT8_1 IN4_2 TIOA15_1 SPISEL0	- - - - -	Q	General-purpose I/O port Multi-function serial ch.8 serial data output pin (1) Input capture ch.4 input pin (2) Base timer ch.15 TIOA I/O pin (1) HS-SPI slave select 0 output pin
71	P215 INT9_1 SCK8_1 IN5_2 TIOA16_1 SPIDAT3	- - - - - -	Q	General-purpose I/O port INT9 external interrupt input pin (1) Multi-function serial ch.8 clock I/O pin (1) Input capture ch.5 input pin (2) Base timer ch.16 TIOA output pin (1) HS-SPI data 3 I/O pin
74	P218 AN36 TEXT2_0 TIOB14_0	- - - -	B	General-purpose I/O port ADC analog 36 input pin Free-run timer 2 clock input pin (0) Base timer ch.14 TIOB input pin (0)
75	P219 AN37 TEXT3_0 TIOB15_0	- - - -	B	General-purpose I/O port ADC analog 37 input pin Free-run timer 3 clock input pin (0) Base timer ch.15 TIOB input pin (0)
76	P220 AN38 TX2_0 SCS83_0 IN6_2 TIOB16_0	- - - - - -	B	General-purpose I/O port ADC analog 38 input pin CAN transmission data 2 output pin (0) Multi-function serial ch.8 serial chip select 3 output pin (0) Input capture ch.6 input pin (2) Base timer ch.16 TIOB input pin (0)
77	P222 INT7_0 AN39 RX2_0 SIN8_0 IN7_2	- - - - - -	B	General-purpose I/O port INT7 external interrupt input pin (0) ADC analog 39 input pin CAN reception data 2 input pin (0) Multi-function serial ch.8 serial data input pin (0) Input capture ch.7 input pin (2)

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
78	P223 AN40 PWU_AN0 SCS81_0 IN8_2 AIN9_1	- - - - - -	B	General-purpose I/O port ADC analog 40 input pin Partial wakeup ADC analog 0 input pin Multi-function serial ch.8 serial chip select 1 output pin (0) Input capture ch.8 input pin (2) QPRC ch.9 AIN input pin (1)
79	P224 AN41 PWU_AN1 TX0_2 SCS80_0 IN9_2 BIN9_1	- - - - - -	B	General-purpose I/O port ADC analog 41 input pin Partial wakeup ADC analog 1 input pin CAN transmission data 0 output pin (2) Multi-function serial ch.8 serial chip select 0 I/O pin (0) Input capture ch.9 input pin (2) QPRC ch.9 BIN input pin (1)
80	P225 INT0_0 PWU_AN2 AN42 RX0_2 SOT8_0 SDA8_0 IN10_2 TIOB17_0 ZIN9_1	- - - - - - - - -	B	General-purpose I/O port INT0 external interrupt input pin (0) Partial wakeup ADC analog 2 input pin ADC analog 42 input pin CAN reception data 0 input pin (2) Multi-function serial ch.8 serial data output pin (0) I ² C bus ch.8 serial data I/O pin Input capture ch.10 input pin (2) Base timer ch.17 TIOB input pin (0) QPRC ch.9 ZIN input pin (1)
81	P226 AN43 PWU_AN3 SCK8_0 SCL8_0 IN11_2 TIOA17_1	- - - - - -	B	General-purpose I/O port ADC analog 43 input pin Partial wakeup ADC analog 3 input pin Multi-function serial ch.8 clock I/O pin (0) I ² C bus ch.8 serial clock I/O pin Input capture ch.11 input pin (2) Base timer ch.17 TIOA I/O pin (1)
87	P229 INT8_0 AN46 PWU_AN6 OUT0_0 TIOA25_0 PWM1P0	- - - - - -	M	General-purpose I/O port INT8 external interrupt input pin (0) ADC analog 46 input pin Partial wakeup ADC analog 6 input pin Output compare ch.0 output pin (0) Base timer ch.25 TIOA I/O pin (0) SMC ch.0 (P1) output pin
88	P230 AN47 PWU_AN7 OUT1_0 TIOA26_0 PWM1M0	- - - - - -	M	General-purpose I/O port ADC analog 47 input pin Partial wakeup ADC analog 7 input pin Output compare ch.1 output pin (0) Base timer ch.26 TIOA output pin (0) SMC ch.0 (M1) output pin
89	P231 AN48 OUT2_0 TIOA27_0 PWM2P0	- - - - -	M	General-purpose I/O port ADC analog 48 input pin Output compare ch.2 output pin (0) Base timer ch.27 TIOA I/O pin (0) SMC ch.0 (P2) output pin
90	P300 AN49 OUT3_0 TIOA28_0 PWM2M0	- - - - -	M	General-purpose I/O port ADC analog 49 input pin Output compare ch.3 output pin (0) Base timer ch.28 TIOA output pin (0) SMC ch.0 (M2) output pin

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
91	P301 AN50 OUT4_0 TIOA18_1 PWM1P1	- - - - -	M	General-purpose I/O port ADC analog 50 input pin Output compare ch.4 output pin (0) Base timer ch.18 TIOA output pin (1) SMC ch.1 (P1) output pin
92	P302 AN51 TIOA19_1 PWM1M1	- - - -	M	General-purpose I/O port ADC analog 51 input pin Base timer ch.19 TIOA I/O pin (1) SMC ch.1 (M1) output pin
93	P304 AN52 TEXT4_0 TIOA20_1 PWM2P1	- - - - -	M	General-purpose I/O port ADC analog 52 input pin Free-run timer 4 clock input pin (0) Base timer ch.20 TIOA output pin (1) SMC ch.1 (P2) output pin
94	P305 AN53 TEXT5_0 TIOA29_0 PWM2M1	- - - - -	M	General-purpose I/O port ADC analog 53 input pin Free-run timer 5 clock input pin (0) Base timer ch.29 TIOA I/O pin (0) SMC ch.1 (M2) output pin
97	P307 INT1_0 AN55 SCS102_0 TIOB18_0 PWM1P2	- - - - -	M	General-purpose I/O port INT1 external interrupt input pin (0) ADC analog 55 input pin Multi-function serial ch.10 serial chip select 2 output pin (0) Base timer ch.18 TIOB input pin (0) SMC ch.2 (P1) output pin
98	P308 AN56 IN0_1 TIOA28_1 PWM1M2	- - - - -	M	General-purpose I/O port ADC analog 56 input pin Input capture ch.0 input pin (1) Base timer ch.28 TIOA output pin (1) SMC ch.2 (M1) output pin
99	P309 AN57 IN1_1 TIOA29_1 PWM2P2	- - - - -	M	General-purpose I/O port ADC analog 57 input pin Input capture ch.1 input pin (1) Base timer ch.29 TIOA I/O pin (1) SMC ch.2 (P2) output pin
100	P312 AN58 SCS101_0 IN2_1 TIOB25_0 PWM2M2	- - - - -	M	General-purpose I/O port ADC analog 58 input pin Multi-function serial ch.10 serial chip select 1 output pin (0) Input capture ch.2 input pin (1) Base timer ch.25 TIOB input pin (0) SMC ch.2 (M2) output pin
101	P313 INT10_1 AN59 SOT10_0 SDA10_0 IN3_1 TIOB26_0 PWM1P3	- - - - - - -	M	General-purpose I/O port INT10 external interrupt input pin (1) ADC analog 59 input pin Multi-function serial ch.10 serial data output pin (0) I ² C bus ch.10 serial data I/O pin Input capture ch.3 input pin (1) Base timer ch.26 TIOB input pin (0) SMC ch.3 (P1) output pin

Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
102	P314 AN60 SCK10_0 SCL10_0 IN4_1 TIOB27_0 TIOA7_1 PWM1M3	- - - - - - - -	M	General-purpose I/O port ADC analog 60 input pin Multi-function serial ch.10 clock I/O pin (0) I ² C bus ch.10 serial clock I/O pin Input capture ch.4 input pin (1) Base timer ch.27 TIOB input pin (0) Base timer ch.7 TIOA I/O pin (1) SMC ch.3 (M1) output pin
103	P315 AN61 TX1_1 SCS100_0 IN5_1 TIOB28_0 TIOA8_1 PWM2P3	- - - - - - - -	M	General-purpose I/O port ADC analog 61 input pin CAN transmission data 1 output pin (1) Multi-function serial ch.10 serial chip select 0 I/O pin (0) Input capture ch.5 input pin (1) Base timer ch.28 TIOB input pin (0) Base timer ch.8 TIOA output pin (1) SMC ch.3 (P2) output pin
104	P317 INT11_1 AN62 RX1_1 SIN10_0 TIOB29_0 TIOA9_1 PWM2M3	- - - - - - - -	M	General-purpose I/O port INT11 external interrupt input pin (1) ADC analog 62 input pin CAN reception data 1 input pin (1) Multi-function serial ch.10 serial data input pin (0) Base timer ch.29 TIOB input pin (0) Base timer ch.9 TIOA I/O pin (1) SMC ch.3 (M2) output pin
107	P321 PWUTRG	- -	R	General-purpose output port Partial wakeup trigger output pin
110	TRST P322	N -	J	JTAG test reset input pin General-purpose output port
111	TDO P323	- -	I	JTAG test data output pin General-purpose output port
112	TDI P324	- -	D	JTAG test data input pin General-purpose output port
113	TMS	-	E	JTAG test mode state input pin
114	TCK	-	E	JTAG test clock input pin
115	P327 WOT	- -	Q	General-purpose I/O port RTC output pin
116	NMIX	-	F	Non-maskable interrupt input pin
117	MD	-	C	Mode pin
118	X0	-	G	Main clock oscillation input pin
119	X1	-	G	Main clock oscillation output pin
121	P331 MCSX3 SGA0_1	- - -	Q	General-purpose I/O port External bus interface chip select 3 output pin Sound generator ch.0 SGA output pin (1)
122	P400 MCSX2 SGO0_1	- - -	Q	General-purpose I/O port External bus interface chip select 2 output pin Sound generator ch.0 SGO output pin (1)
123	RSTX	N	F	External reset input pin
127	P401 TX1_0 IN0_0	- - -	Q	General-purpose I/O port CAN transmission data 1 output pin (0) Input capture ch.0 input pin (0)

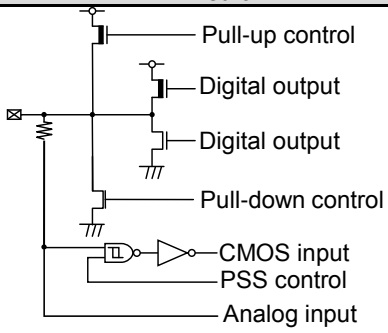
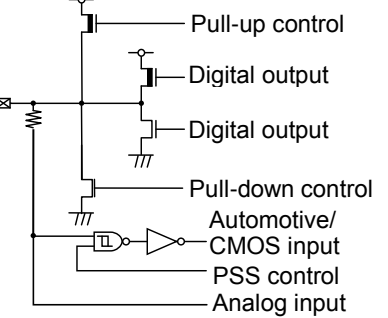
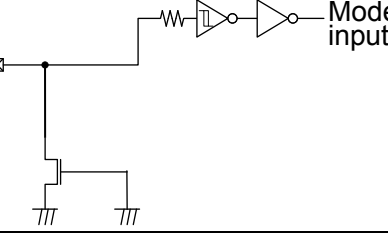
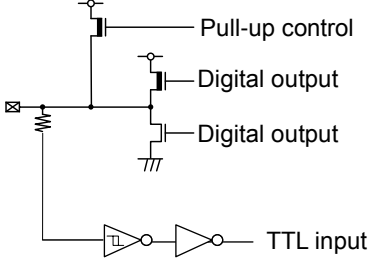
Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
128	P402 INT2_0 RX1_0 IN1_0 V3	- - - - -	L	General-purpose I/O port (Input only. No output.) INT2 external interrupt input pin (0) CAN reception data 1 input pin (0) Input capture ch.1 input pin (0) LCD reference voltage V3 input pin
129	P403 IN2_0 TRACEDATA0 V2 SGA1_1	- - - - -	B	General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin LCD reference voltage V2 input pin Sound generator ch.1 SGA output pin (1)
130	P404 SCS120_0 IN3_0 TRACEDATA1 MAD14 V1 SGO1_1	- - - - - - -	B	General-purpose I/O port Multi-function serial ch.12 serial chip select 0 I/O pin (0) Input capture ch.3 input pin (0) Trace data 1 output pin External bus interface address bit14 output pin LCD reference voltage V1 input pin Sound generator ch.1 SGO output pin (1)
131	P405 INT11_0 SIN12_0 IN4_0 TRACEDATA2 MAD13 V0 SGA2_1	- - - - - - -	B	General-purpose I/O port INT11 external interrupt input pin (0) Multi-function serial ch.12 serial data input pin (0) Input capture ch.4 input pin (0) Trace data 2 output pin External bus interface address bit13 output pin LCD reference voltage V0 input pin Sound generator ch.2 SGA output pin (1)
132	P406 SOT12_0 TRACEDATA3 MAD12 COM0 SGO2_1	- - - - - -	K	General-purpose I/O port Multi-function serial ch.12 serial data output pin (0) Trace data 3 output pin External bus interface address bit12 output pin LCD segment(duty) common 0 output pin Sound generator ch.2 SGO output pin (1)
133	P407 SCK12_0 SCK10_1 TRACEDATA4 MAD11 COM1	- - - - - -	K	General-purpose I/O port Multi-function serial ch.12 clock I/O pin (0) Multi-function serial ch.10 clock I/O pin (1) Trace data 4 output pin External bus interface address bit11 output pin LCD segment(duty) common 1 output pin
134	P408 SIN2_0 TRACEDATA5 TIN18 MAD10 COM2	- - - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial data input pin (0) Trace data 5 output pin Reload timer ch.18 event input pin (0) External bus interface address bit10 output pin LCD segment(duty) common 2 output pin
135	P409 SOT2_0 TIOA24_1 TRACEDATA6 TOT18 MAD09 COM3	- - - - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial data output pin (0) Base timer ch.24 TIOA output pin (1) Trace data 6 output pin Reload timer ch.18 output pin (0) External bus interface address bit9 output pin LCD segment(duty) common 3 output pin

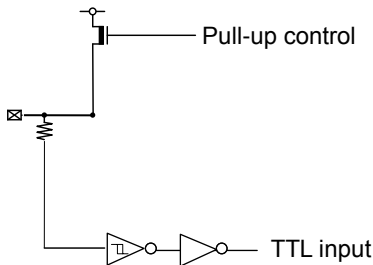
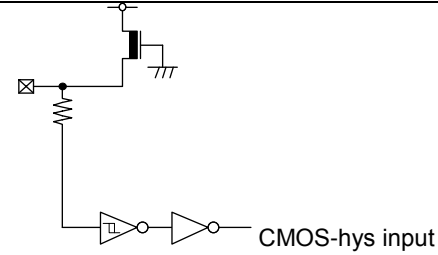
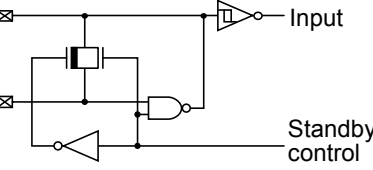
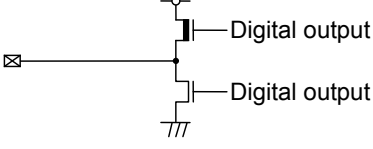
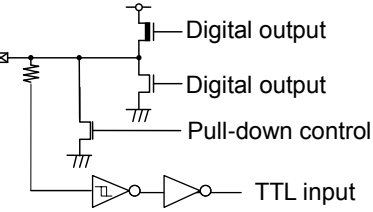
Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
136	P411 INT13_1 SCK2_0 SCS101_1 TIOB24_0 TRACEDATA7 TIN19 MAD08 SEG0	- - - - - - - - -	K	General-purpose I/O port INT13 external interrupt input pin (1) Multi-function serial ch.2 clock I/O pin (0) Multi-function serial ch.10 serial chip select 1 output pin (1) Base timer ch.24 TIOB input pin (0) Trace data 7 output pin Reload timer ch.19 event input pin (0) External bus interface address bit8 output pin LCDC segment 0 (Duty) output pin
137	P413 INT14_1 SCS20_0 SCS103_1 TOT19 MAD07 SEG1	- - - - - - -	K	General-purpose I/O port INT14 external interrupt input pin (1) Multi-function serial ch.2 serial chip select 0 I/O pin (0) Multi-function serial ch.10 serial chip select 3 output pin (1) Reload timer ch.19 output pin (0) External bus interface address bit7 output pin LCDC segment 1 (Duty) output pin
138	P414 SCS21_0 TIN32 MAD06 SEG2	- - - - -	K	General-purpose I/O port Multi-function serial ch.2 serial chip select 1 output pin (0) Reload timer ch.32 event input pin (0) External bus interface address bit6 output pin LCDC segment 2 (Duty) output pin
139	P416 SIN10_1 IN5_0 TIOA22_1 TOT32 MAD05 SEG3	- - - - - - -	K	General-purpose I/O port Multi-function serial ch.10 serial data input pin (1) Input capture ch.5 input pin (0) Base timer ch.22 TIOA output pin (1) Reload timer ch.32 output pin (0) External bus interface address bit5 output pin LCDC segment 3 (Duty) output pin
140	P417 INT15_1 SOT10_1 TIOA23_1 TIN33 MAD04 SEG4	- - - - - - -	K	General-purpose I/O port INT15 external interrupt input pin (1) Multi-function serial ch.10 serial data output pin (1) Base timer ch.23 TIOA I/O pin (1) Reload timer ch.33 event input pin (0) External bus interface address bit4 output pin LCDC segment 4 (Duty) output pin
141	P418 INT14_0 SCS22_0 TIOB23_0 TOT33 MAD03 SEG5	- - - - - - -	K	General-purpose I/O port INT14 external interrupt input pin (0) Multi-function serial ch.2 serial chip select 2 output pin (0) Base timer ch.23 TIOB input pin (0) Reload timer ch.33 output pin (0) External bus interface address bit3 output pin LCDC segment 5 (Duty) output pin
142	P420 SCK2_1 TRACECLK MAD02 SEG6	- - - - -	K	General-purpose I/O port Multi-function serial ch.2 clock I/O pin (1) Trace clock External bus interface address bit2 output pin LCDC segment 6 (Duty) output pin
143	P421 INT12_1 SIN2_1 TRACECTL MAD01 SEG7	- - - - - -	K	General-purpose I/O port INT12 external interrupt input pin (1) Multi-function serial ch.2 serial data input pin (1) Trace control External bus interface address bit1 output pin LCDC segment 7 (Duty) output pin
42	AVCC0	-	-	Analog power supply pin for AD converter unit 0

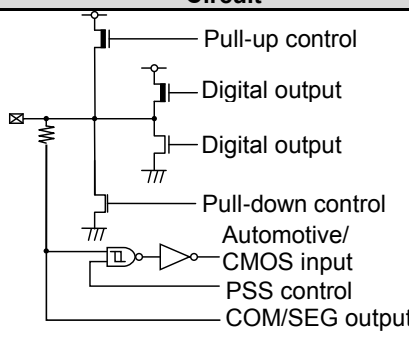
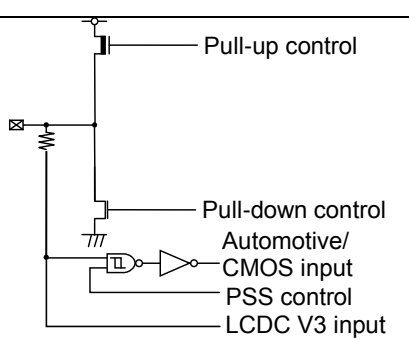
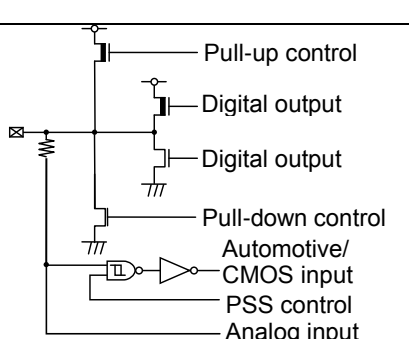
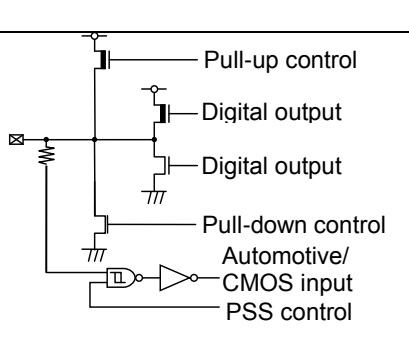
Pin No.	Pin Name	Polarity	I/O Circuit Type	Function
84	AVCC1	-	-	Analog power supply pin for AD converter unit 1
43	AVRH0	-	-	Upper-limit reference voltage pin for AD converter unit 0
83	AVRH1	-	-	Upper-limit reference voltage pin for AD converter unit 1
44	AVSS0 AVRL0	- -	- -	GND pin for AD converter unit 0 Lower-limit reference voltage pin for AD converter unit 0
82	AVSS1 AVRL1	- -	- -	GND pin for AD converter unit 1 Lower-limit reference voltage pin for AD converter unit 1
38 126	C	-	-	External capacity connection output pin
36 72 109 124 144	VCC	-	-	Power supply pin
1 37 73 108 120 125	VSS	-	-	GND
85 95 105	DVCC	-	-	Power Supply pin for SMC high current
86 96 106	DVSS	-	-	GND pin for SMC high current

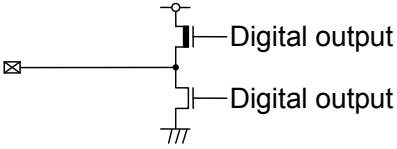
4. I/O Circuit Types

This section explains I/O circuit types.

Type	Circuit	Overview
A	 Pull-up control Digital output Digital output Pull-down control CMOS input PSS control Analog input	- General-purpose I/O port with analog input - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis input
B	 Pull-up control Digital output Digital output Pull-down control Automotive/ CMOS input PSS control Analog input	- General-purpose I/O port with analog input - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable
C	 Mode input	- Mode input - CMOS hysteresis input
D	 Pull-up control Digital output Digital output TTL input	- JTAG - General-purpose output port - Output of 2 mA - 50 kΩ with pull-up resistor control - TTL input

Type	Circuit	Overview
E		- JTAG - 50 kΩ with pull-up resistor control - TTL input
F		- CMOS hysteresis input - 50 kΩ with pull-up resistor
G		- Main oscillation I/O
I		- JTAG - Output of 2 mA
J		- JTAG - General-purpose output port - Output of 2 mA - 50 kΩ with pull-down resistor control - TTL input

Type	Circuit	Overview
K	 Pull-up control Digital output Digital output Pull-down control Automotive/ CMOS input PSS control COM/SEG output	- General-purpose I/O port with COM/SEG output - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable
L	 Pull-up control Pull-down control Automotive/ CMOS input PSS control LCDC V3 input	- General-purpose I/O port with LCDC V3 input - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable
M	 Pull-up control Digital output Digital output Pull-down control Automotive/ CMOS input PSS control Analog input	- General-purpose I/O port with analog input - Output of 1 mA or 2 mA or 30 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable
Q	 Pull-up control Digital output Digital output Pull-down control Automotive/ CMOS input PSS control	- General-purpose I/O port - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable

Type	Circuit	Overview
R		- Output of 2 mA

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40 % to 70 % relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40 % and 70 %.
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

- (1) Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
- (2) Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
- (3) Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
- (4) Radiation, Including Cosmic Radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
- (5) Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than V_{CC} or lower than V_{SS} ; or the voltage applied between a V_{CC} pin and a V_{SS} pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies ($AVCC0$, $AVCC1$, $AVRH0$, and $AVRH1$) and analog inputs do not exceed the digital power supply (V_{CC}) at the analog system power-on and power-off times. V_{CC} and DV_{CC} must be set to the same voltage. The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (V_{CC}) and analog supply voltages ($AVCC0$, $AVCC1$, $AVRH0$, and $AVRH1$), and the power supply voltage of high-current output buffer pins (DV_{CC}), or turn on the digital supply voltage (V_{CC}) and then the analog supply voltages ($AVCC0$, $AVCC1$, $AVRH0$, and $AVRH1$), and the power supply voltage of high-current output buffer pins (DV_{CC}).

About Handling Unused Pins

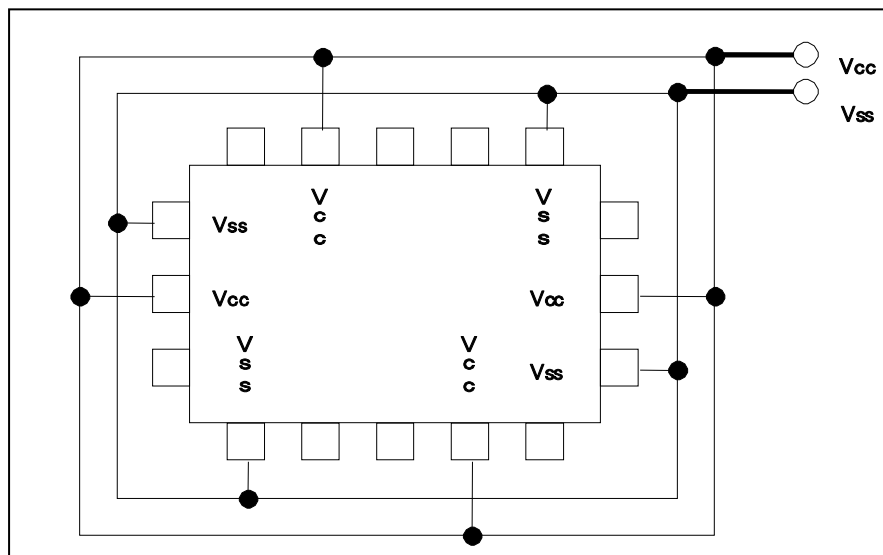
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kilohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple V_{CC} and V_{SS} pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the V_{CC} and V_{SS} pins to the power source and ground externally. Also handle all the V_{SS} power supply pins in this way as shown in the following diagram. If there are multiple V_{CC} or V_{SS} systems, the device does not operate normally even within the guaranteed operating range.

Figure 6-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the V_{CC} and V_{SS} of this device.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the V_{CC} pin and the V_{SS} pin.

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

About the Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

About the Power-on Time

To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on

Point to Note during PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that $AVCC = AVRH = VCC$ and $AVSS = AVRL = VSS$.

Points to Note About Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AVCC, AVRH, and AVRL) and analog inputs (AN3, AN5 to AN6, AN9 to AN10, AN12 to AN15, AN17 to AN24, AN27 to AN43, AN46 to AN53, and AN55 to AN62) of an A/D converter.

At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AVCC. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

Treatment of Power supplies for High Current Output Buffer Pins (DVCC, DVSS)

Be sure to turn on the digital power supply voltage (VCC) first, and then turn on the power supply voltage for high current output buffer pins (DVCC, DVSS). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply voltage (VCC).

Even if the high current output buffer pins are used as general-purpose ports, the power supply voltage of high current output buffer pins (DVCC, DVSS) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

Connect the pins to have $DVCC = VCC$ and $DVSS = VSS$.

About C Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 126 in S6J312xHzC* specifications) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet.

*x: A/9, z: A/B

Precautions on Designing a Mounting Substrate

Measures against heat generation from the package must be taken for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad. For detailed information about mount conditions, contact your sales representative.

Notes on Writing to a Register Containing a Status Flag

In writing to a register containing a status flag (particularly an interrupt request flag, etc.) to control a function, it is important to take care not to accidentally clear the status flag.

Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.

Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

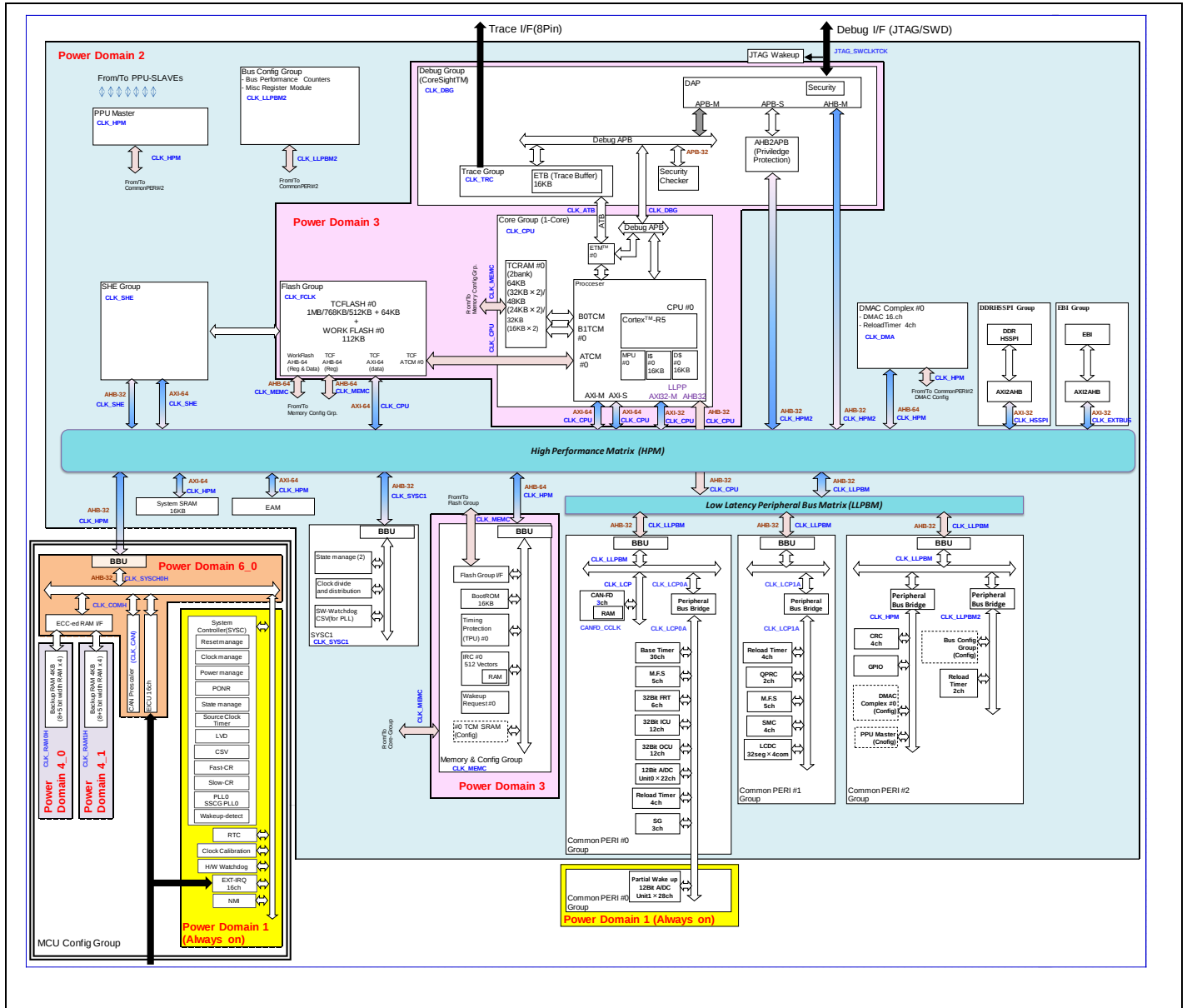
Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

7. Block Diagram

This section provides block diagrams of the S6J3120 series.

Figure 7-1 S6J312xHzC* Block Diagram

*x: A/9, z: A/B



8. Memory Map

This section explains the memory map.

Figure 8-1 Memory Map(S6J312AHzC/9HzC*)

*z: A/B

ADDRESS		group	S6J312AHzC*	S6J3129HzC*
START	END		part	part
0x0000_0000	0x0000_7FFF	Internal area for CR5 Complex	TCRAM (Main 64KByte)	TCRAM (Main 48KByte)
0x0000_8000	0x0000_BFFF		Reserved	Reserved
0x0000_C000	0x0000_FFFF		Reserved	Reserved
0x0001_0000	0x007F_FFFF		Reserved	Reserved
0x0080_0000	0x00BF_FFFF		TCM_FLASH (Small Sector 8KByte×8)	TCM_FLASH (Small Sector 8KByte×8)
0x009F_0000	0x009F_FFFF		TCM_FLASH (Code 1MByte)	TCM_FLASH (Code 768KByte)
0x00A0_0000	0x00A7_FFFF		Reserved	Reserved
0x00A8_0000	0x00AB_FFFF		Reserved	Reserved
0x00AC_0000	0x00AF_FFFF		Reserved	Reserved
0x00B0_0000	0x00DF_FFFF		Reserved	Reserved
0x00E0_0000	0x00FF_FFFF		Reserved	Reserved
0x0100_0000	0x019E_FFFF		AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)	AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)
0x019F_0000	0x019F_FFFF		AXI_FLASH_MEMORY (Code 1MByte *Mirror)	AXI_FLASH_MEMORY (Code 768KByte *Mirror)
0x01A0_0000	0x01A7_FFFF		Reserved	Reserved
0x01A8_0000	0x01AB_FFFF		Reserved	Reserved
0x01AC_0000	0x01AF_FFFF		Reserved	Reserved
0x01B0_0000	0x01DF_FFFF		Reserved	Reserved
0x01E0_0000	0x01FF_FFFF		Reserved	Reserved
0x0200_0000	0x0200_3FFF	Shared Flash and memory area	SYSTEM SRAM (16KByte)	SYSTEM SRAM (16KByte)
0x0200_4000	0x0203_FFFF		Reserved	Reserved
0x0204_0000	0x027F_FFFF		Reserved	Reserved
0x0280_0000	0x0280_002F		Exclusive Access Memory	Exclusive Access Memory
0x0280_0030	0x033F_FFFF		Reserved	Reserved
0x0400_0000	0x05FF_FFFF		AXI_SLAVE_CORE0	AXI_SLAVE_CORE0
0x0600_0000	0x06FF_FFFF		Reserved	Reserved
0x0E00_0000	0x0E01_BFFF		WORK_FLASH (112KByte mirror area 1)	WORK_FLASH (112KByte mirror area 1)
0x0E01_C000	0x0E0F_FFFF		Reserved	Reserved
0x0E10_0000	0x0E1F_FFFF		Reserved	Reserved
0x0E20_0000	0x0E21_BFFF	External bus area	WORK_FLASH (112KByte mirror area 3)	WORK_FLASH (112KByte mirror area 3)
0x0E21_C000	0x0E2F_FFFF		Reserved	Reserved
0x0E30_0000	0x0E31_BFFF		WORK_FLASH (112KByte mirror area 4)	WORK_FLASH (112KByte mirror area 4)
0x0E31_C000	0x0E3F_FFFF		Reserved	Reserved
0x0E40_0000	0x0E7F_FFFF		Reserved	Reserved
0x0E80_0000	0x0E80_1FFF		Backup RAM 8KByte	Backup RAM 8KByte
0x0E80_2000	0x0E80_FFFF		Reserved	Reserved
0x0E81_0000	0x0E87_FFFF		Reserved	Reserved
0x0E88_0000	0x0FFF_FFFF		Reserved	Reserved
0x1000_0000	0x1FFF_FFFF		EBI_MEMORY(SRAM/FLASH)	EBI_MEMORY(SRAM/FLASH)
0x2000_0000	0x7FFF_FFFF	Reserved	Reserved	Reserved
0x8000_0000	0x8FFF_FFFF	HSPID memory area	HSPID0_MEMORY	HSPID0_MEMORY
0x9000_0000	0xAFFF_FFFF	Reserved	Reserved	Reserved
0xB000_0000	0xB483_FFFF	Peri area	Peri_area	Peri_area
0xB484_0000	0xB484_FFFF		APPS#5	APPS#5
0xB485_0000	0xB48B_FFFF		Peri_area	Peri_area
0xB48C_0000	0xB48C_FFFF		APPS#7	APPS#7
0xB48D_0000	0xB7FF_FFFF		Peri_area	Peri_area
0xB800_0000	0xBFFF_FFFF		Reserved	Reserved
0xC000_0000	0xFFFF_DFFF	Reserved	Reserved	Reserved
0xFFFF_E000	0xFFFF_FFFF	Error Config	ERRCFG	ERRCFG
0xFFFF_0000	0xFFFF_3FFF	BootROM	BootRom	BootRom
0xFFFF_4000	0xFFFF_FFFF	Reserved	Reserved	Reserved

- Only the CPU core can access 0000_0000 ~ 01FF_FFFF. Bus masters other than the CPU core cannot access the region.
- Internal area of CR5 complex (0000_0000 ~ 01FF_FFFF) is mapped to AXI_SLAVE_CORE0. All bus masters can access to internal area of CR5 complex via AXI_SLAVE_CORE0.
- In each of the following memory area combinations, the areas are physically the same memory area.
 1. TCM FLASH (0x00A0_0000 -) and AXI FLASH MEMORY (0x01A0_0000 -)
 2. TCM FLASH Small Sector (0x009F_0000 -) and AXI FLASH MEMORY Small Sector (0x019F_0000 -)
 3. WORKFLASH (0x0E00_0000 -), WORKFLASH (0x0E20_0000 -), and WORKFLASH (0x0E30_0000 -)

The ECC movement in TCM port is based on ECC setting inside the CPU.

- The differences between the TCM FLASH and AXI FLASH include the following.

Function	TCM FLASH	AXI FLASH
High-speed Access Using Dedicated Bus	Applicable	Not applicable
Write and Erase	Not applicable (Read-only)	Applicable
Read	Applicable	Applicable

- The differences between WORKFLASH areas include the following.

Area	Function
WORKFLASH Area 1	Used in write operation (with ECC)
WORKFLASH Area 3	Used in write operation (without ECC)
WORKFLASH Area 4	Used in read operation

- Terms are as follows.

Term	Description
TCM RAM	Main RAM
TCM FLASH	Program FLASH (TCM area)
AXI FLASH	Program FLASH (AXI area) This is physically the same as the TCM FLASH.
SYSTEM RAM	System RAM
AXI SLAVE CORE	AXI CPU control area
WORKFLASH	FLASH for work
BACKUP RAM	Backup RAM
EBI MEMORY	Memory for External bus interface
HSSPI0 MEMORY	Memory for DDR HS-SPI
Peri area	Entire area for peripheral functions
APPS#5	Part of area for peripheral functions
APPS#7	Part of area for peripheral functions
ERRCFG	Error configuration area
BootROM	ROM for reset boot

S6J312xHzC* Peripheral Map

* x: A/9, z:A/B

START Address	END Address	Group	Function	PPU No
B000_0000	B010_7FFF		Reserved	-
B010_0000	B010_03FF		EBI registers	0
B010_0400	B010_0FFF		Reserved	-
B010_1000	B010_13FF		DDR_HSSPI	1
B010_0400	B010_7FFF		Reserved	-
B010_8000	B010_80FF	SystemSRAM	SystemSRAM registers	-
B010_8100	B02F_FFFF		Reserved	-
B030_0000	B030_7FFF	SYSC1	System Controller #1	-
B030_8000	B03F_FFFF	SYSC1	SWDT	-
B040_0000	B040_7FFF	MEMORY_CONFIG_GROUP	IRC0	21
B040_8000	B040_FFFF	MEMORY_CONFIG_GROUP	TPU0	19
B041_0000	B041_0FFF	MEMORY_CONFIG_GROUP	TCRAM Control Status Register	16
B041_1000	B041_1FFF	MEMORY_CONFIG_GROUP	TCFlash Control Status Register	17
B041_2000	B041_20FF	MEMORY_CONFIG_GROUP	WFlash Control Status Register	18
B041_2100	B04F_FFFF		Reserved	-
B050_0000	B05F_FFFF		Reserved	-
B060_0000	B060_007F	MCU_CONFIG_GROUP	Protection register area	-
B060_0080	B060_00FF	MCU_CONFIG_GROUP	RUN profile register area	-
B060_0100	B060_017F	MCU_CONFIG_GROUP	PSS profile register area	-
B060_0180	B060_01FF	MCU_CONFIG_GROUP	APP profile register area	-
B060_0200	B060_027F	MCU_CONFIG_GROUP	STS profile register area	-
B060_0280	B060_02FF	MCU_CONFIG_GROUP	System register area	-
B060_0300	B060_037F	MCU_CONFIG_GROUP	CSV	-
B060_0380	B060_03FF	MCU_CONFIG_GROUP	RESET	-
B060_0400	B060_047F	MCU_CONFIG_GROUP	SCT(Fast CR)	34
B060_0480	B060_04FF	MCU_CONFIG_GROUP	SCT(Slow CR)	33
B060_0500	B060_05FF	MCU_CONFIG_GROUP	SCT(Main clock)	35
B060_0600	B060_067F	MCU_CONFIG_GROUP	Clock System	-
B060_0680	B060_06FF	MCU_CONFIG_GROUP	Special register area	-
B060_0700	B060_07FF	MCU_CONFIG_GROUP	Debug register area	-
B060_0800	B060_BFFF	MCU_CONFIG_GROUP	Mode	-
B060_C000	B060_FFFF	MCU_CONFIG_GROUP	HWDT	-
B061_0000	B061_7FFF		Reserved	-
B061_8000	B061_FFFF	MCU_CONFIG_GROUP	RTC	32
B062_0000	B063_FFFF	MCU_CONFIG_GROUP	EIC	-
B064_0000	B065_FFFF		Reserved	-
B066_0000	B067_FFFF		Reserved	-
B068_0000	B068_7FFF	MCU_CONFIG_GROUP	BURAMIF	-
B068_8000	B068_83FF	MCU_CONFIG_GROUP	EICU	37
B068_8400	B068_87FF	MCU_CONFIG_GROUP	CR_Calibration	38
B068_8800	B068_8BFF	MCU_CONFIG_GROUP	IRQ ALL	42
B068_8C00	B068_FFFF	MCU_CONFIG_GROUP	CAN Prescaler	43
B069_0000	B06F_FFFF		Reserved	-
B070_0000	B07F_FFFF		Reserved	-
B080_0000	B0FF_FFFF	Bit RMW alias	BBU for MCU Config (Covers B060_0000 -- B06F_FFFF)	-
B100_0000	B10F_FFFF	Bit RMW alias	BBU for SYSC1 (Covers B030_0000 -- B031_FFFF)	-
B110_0000	B11F_FFFF	Bit RMW alias	BBU for MEMC (Covers B040_0000 -- B041_FFFF)	-
B120_0000	B1FF_FFFF		Reserved	-
B200_0000	B20F_FFFF	SHE	SHE configuration registers	63
B210_0000	B46F_FFFF		Reserved	-

START Address	END Address	Group	Function	PPU No
B470_0000	B470_3FFF	CommonPERI #2	DMAC #0 registers	64
B470_4000	B470_FFFF		Reserved	-
B471_0000	B471_0FFF	CommonPERI #2	MPU for DMAC#0	66
B471_1000	B471_3FFF		Reserved	-
B471_4000	B471_4FFF	CommonPERI #2	DMA Complex #0 registers (Additional registers, RLTs)	68
B471_5000	B471_7FFF		Reserved	-
B471_8000	B471_83FF	CommonPERI #2	CRC#0	70
B471_8400	B471_87FF	CommonPERI #2	CRC#1	71
B471_8800	B471_8BFF	CommonPERI #2	CRC#2	72
B471_8C00	B471_8FFF	CommonPERI #2	CRC#3	73
B471_9000	B473_7FFF		Reserved	-
B473_8000	B473_FFFF	CommonPERI #2	GPIO	74
B474_0000	B474_7FFF	CommonPERI #2	PPC	75
B474_8000	B474_FFFF	CommonPERI #2	RIC	76
B475_0000	B475_7FFF	CommonPERI #2	PPU	-
B475_8000	B478_7FFF		Reserved	-
B478_8000	B478_83FF	CommonPERI #2	Reload Timer ch.32	160
B478_8400	B478_87FF	CommonPERI #2	Reload Timer ch.33	161
B478_8800	B478_FBFF		Reserved	-
B478_FC00	B478_FFFF	CommonPERI #2	Misc registers	82
B479_0000	B47F_FFFF		Reserved	-
B480_0000	B480_03FF	CommonPERI #0	M.F.Serial ch.0	176
B480_0400	B480_07FF	CommonPERI #0	M.F.Serial ch.1	177
B480_0800	B480_0BFF	CommonPERI #0	M.F.Serial ch.2	178
B480_0C00	B480_0FFF	CommonPERI #0	M.F.Serial ch.3	179
B480_1000	B480_13FF	CommonPERI #0	M.F.Serial ch.4	180
B480_1400	B480_7FFF		Reserved	-
B480_8000	B480_83FF	CommonPERI #0	BaseTimer ch.0	88
B480_8400	B480_87FF	CommonPERI #0	BaseTimer ch.1	89
B480_8800	B480_8BFF	CommonPERI #0	BaseTimer ch.2	90
B480_8C00	B480_8FFF	CommonPERI #0	BaseTimer ch.3	91
B480_9000	B480_93FF	CommonPERI #0	BaseTimer ch.4	92
B480_9400	B480_97FF	CommonPERI #0	BaseTimer ch.5	93
B480_9800	B480_9BFF	CommonPERI #0	BaseTimer ch.6	94
B480_9C00	B480_9FFF	CommonPERI #0	BaseTimer ch.7	95
B480_A000	B480_A3FF	CommonPERI #0	BaseTimer ch.8	96
B480_A400	B480_A7FF	CommonPERI #0	BaseTimer ch.9	97
B480_A800	B480_ABFF	CommonPERI #0	BaseTimer ch.10	98
B480_AC00	B480_AFFF	CommonPERI #0	BaseTimer ch.11	99
B480_B000	B480_FFFF		Reserved	-
B481_0000	B481_03FF	CommonPERI #0	Reload Timer ch.0	128
B481_0400	B481_07FF	CommonPERI #0	Reload Timer ch.1	129
B481_0800	B481_0BFF	CommonPERI #0	Reload Timer ch.2	130
B481_0C00	B481_0FFF	CommonPERI #0	Reload Timer ch.3	131
B481_1000	B481_FFFF		Reserved	-
B482_0000	B482_03FF	CommonPERI #0	FRT ch.0	208
B482_0400	B482_07FF	CommonPERI #0	FRT ch.1	209
B482_0800	B482_0BFF	CommonPERI #0	FRT ch.2	210
B482_0C00	B482_0FFF	CommonPERI #0	FRT ch.3	211
B482_1000	B482_13FF	CommonPERI #0	FRT ch.4	212
B482_1400	B482_17FF	CommonPERI #0	FRT ch.5	213
B482_1800	B482_7FFF		Reserved	-
B482_8000	B482_83FF	CommonPERI #0	ICU ch.0 / ch.1	224
B482_8400	B482_87FF	CommonPERI #0	ICU ch.2 / ch.3	225
B482_8800	B482_8BFF	CommonPERI #0	ICU ch.4 / ch.5	226
B482_8C00	B482_8FFF	CommonPERI #0	ICU ch.6 / ch.7	227
B482_9000	B482_93FF	CommonPERI #0	ICU ch.8 / ch.9	228
B482_9400	B482_97FF	CommonPERI #0	ICU ch.10 / ch.11	229
B482_9800	B482_FFFF		Reserved	-

START Address	END Address	Group	Function	PPU No
B483_0000	B483_03FF	CommonPERI #0	OCU ch.0 / ch.1	240
B483_0400	B483_07FF	CommonPERI #0	OCU ch.2 / ch.3	241
B483_0800	B483_0BFF	CommonPERI #0	OCU ch.4 / ch.5	242
B483_0C00	B483_0FFF	CommonPERI #0	OCU ch.6 / ch.7	243
B483_1000	B483_13FF	CommonPERI #0	OCU ch.8 / ch.9	244
B483_1400	B483_17FF	CommonPERI #0	OCU ch.10 / ch.11	245
B483_1800	B483_FBFF		Reserved	-
B483_FC00	B483_FFFF	Common PERI #0	Misc registers	80
B484_0000	B484_FFFF	APPS #5	APPS#5 area	-
B485_0000	B487_FFFF		Reserved	-
B488_0000	B488_03FF	CommonPERI #1	M.F.Serial ch.8	184
B488_0400	B488_07FF	CommonPERI #1	M.F.Serial ch.9	185
B488_0800	B488_0BFF	CommonPERI #1	M.F.Serial ch.10	186
B488_0C00	B488_0FFF	CommonPERI #1	M.F.Serial ch.11	187
B488_1000	B488_13FF	CommonPERI #1	M.F.Serial ch.12	188
B488_1400	B488_FFFF		Reserved	-
B489_0000	B489_03FF	CommonPERI #1	Reload Timer ch.16	144
B489_0400	B489_07FF	CommonPERI #1	Reload Timer ch.17	145
B489_0800	B489_0BFF	CommonPERI #1	Reload Timer ch.18	146
B489_0C00	B489_0FFF	CommonPERI #1	Reload Timer ch.19	147
B489_1000	B489_7FFF		Reserved	-
B489_8000	B489_83FF	CommonPERI #1	QPRC ch.8	200
B489_8400	B489_87FF	CommonPERI #1	QPRC ch.9	201
B489_8800	B48B_0FFF		Reserved	-
B48B_1000	B48B_FBFF		Reserved	-
B48B_FC00	B48B_FFFF	CommonPERI #1	Misc registers	81
B48C_0000	B48C_FFFF	APPS #7	APPS#7 area	-
B48D_0000	B48F_FFFF		Reserved	-
B490_0000	B490_FFFF	CommonPERI #0	CAN_FD ch.0	256
B491_0000	B491_FFFF	CommonPERI #0	CAN_FD ch.1	257
B492_0000	B492_FFFF	CommonPERI #0	CAN_FD ch.2	258
B493_0000	B4BF_FFFF		Reserved	-
B4C0_0000	B4FF_FFFF	Bit RMW alias	BBU for CommonPERI#0 (Covers B490_0000 -- B497_FFFF)	-
B500_0000	B5FF_FFFF		Reserved	-
B600_0000	B6FF_FFFF		Reserved	-
B700_0000	B77F_FFFF	Bit RMW alias	BBU alias for CommonPERI#2 (Covers B470_0000 -- B47F_FFFF)	-
B780_0000	B7BF_FFFF	Bit RMW alias	BBU alias for CommonPERI#0 (Covers B480_0000 -- B487_FFFF)	-
B7C0_0000	B7FF_FFFF	Bit RMW alias	BBU alias for CommonPERI#1 (Covers B488_0000 -- B48F_FFFF)	-
B800_0000	FFFE_DFFF		Reserved	-
FFFE_E000	FFFE_FBFC	Error Config	IRC	-
FFFE_FC00	FFFE_FFFF	Error Config	BootROM I/F	20

■ - APPS#5 area

START Address	END Address		Function	PPU No
B484_0000	B484_03FF	APPS #5	Sound Generator ch.0	264
B484_0400	B484_07FF	APPS #5	Sound Generator ch.1	265
B484_0800	B484_0BFF	APPS #5	Sound Generator ch.2	266
B484_0C00	B484_37FF		Reserved	-
B484_3800	B484_3BFF	APPS #5	BaseTimer ch.12	278
B484_3C00	B484_3FFF	APPS #5	BaseTimer ch.13	279
B484_4000	B484_43FF	APPS #5	BaseTimer ch.14	280
B484_4400	B484_47FF	APPS #5	BaseTimer ch.15	281
B484_4800	B484_4BFF	APPS #5	BaseTimer ch.16	282
B484_4C00	B484_4FFF	APPS #5	BaseTimer ch.17	283
B484_5000	B484_53FF	APPS #5	BaseTimer ch.18	284
B484_5400	B484_57FF	APPS #5	BaseTimer ch.19	285
B484_5800	B484_5BFF	APPS #5	BaseTimer ch.20	286
B484_5C00	B484_5FFF	APPS #5	BaseTimer ch.21	287
B484_6000	B484_63FF	APPS #5	BaseTimer ch.22	288
B484_6400	B484_67FF	APPS #5	BaseTimer ch.23	289
B484_6800	B484_6BFF	APPS #5	BaseTimer ch.24	290
B484_6C00	B484_6FFF	APPS #5	BaseTimer ch.25	291
B484_7000	B484_73FF	APPS #5	BaseTimer ch.26	292
B484_7400	B484_77FF	APPS #5	BaseTimer ch.27	293
B484_7800	B484_7BFF	APPS #5	BaseTimer ch.28	294
B484_7C00	B484_7FFF	APPS #5	BaseTimer ch.29	295
B484_8000	B484_83FF	APPS #5	A/D unit0	296
B484_8400	B484_87FF	APPS #5	A/D unit1 , Partial Wake Up	297
B484_8800	B484_8BFF	APPS #5	A/D analog input control	298
B484_8C00	B484_8FFF		Reserved	-
B484_9000	B484_93FF	APPS #5	Global Timer	300
B484_9400	B484_FFFF		Reserved	-

■ - APPS#7 area

START Address	END Address		Function	PPU No
B48C_0000	B48C_3FFF		Reserved	-
B48C_4000	B48C_43FF	APPS #7	Stepper Motor Control ch.0	317
B48C_4400	B48C_47FF	APPS #7	Stepper Motor Control ch.1	318
B48C_4800	B48C_4BFF	APPS #7	Stepper Motor Control ch.2	319
B48C_4C00	B48C_4FFF	APPS #7	Stepper Motor Control ch.3	320
B48C_5000	B48C_57FF		Reserved	-
B48C_5800	B48C_5BFF	APPS #7	SMC Trigger Generator	323
B48C_5C00	B48C_5FFF	APPS #7	Liquid Crystal Display Controller	324
B48C_6000	B48C_63FF	APPS #7	Liquid Crystal Display input/output control	325
B48C_6400	B48C_FFFF		Reserved	-

When MPU attribute of Cortex®-R5 is configured as "Normal", store buffer inside Cortex®-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.

MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.

- Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF]
- Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF]
- Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]

MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.

- FLASH Memory (when writing commands)

SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)

9. Pin Statuses In CPU Status

Table 9-1 Pin State Table (1/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2			External Reset Factor 3		Internal Reset Factor #2	Sleep mode	Stop mode #4	Timer mode #4														
			External factor generation in progress		After external factor releasing	External factor generation in progress		After external factor releasing		External Reset Factor 3				CPU Sleep mode	High impedance disabled (SYSIO.SPECIFGR, PSSP.ACTRL=0)	When High impedance Enabled (SYSIO.SPECIFGR, PSSP.ACTRL=1)	High impedance disabled (SYSIO.SPECIFGR, PSSP.ACTRL=0)	When High impedance Enabled (SYSIO.SPECIFGR, PSSP.ACTRL=1)										
			Internal reset issuance in progress	Internal reset issuance in progress		Internal reset issuance in progress	Internal reset issuance in progress	Internal reset issuance in progress	Internal reset issuance in progress	Internal reset issuance in progress									Internal reset issuance in progress									
2	P000/SOT2_1/AIN8_0/MAD00/SEG8	With control	Hi-Z/ Input blocked		Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3 #6	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #1	Last state retained #3 #6	Hi-Z/ Input blocked #6													
3	P001/SCS20_1/BIN8_0/MDATA15/SEG9																											
4	P003/SCS22_1/ZIN8_0/MDATA14/SEG10																											
5	P005/SIN3_0/IN6_0/AIN9_0/MDATA13/SEG11																											
6	P006/SOT3_0/SDA3_0/INT_0/BIN9_0/MDATA12/SEG12																											
7	P007/SCK3_0/SCL3_0/IN8_0/ZIN9_0/MDATA11/SEG13																											
8	P008/SCS30_0/IN9_0/TIOA0_0/MDATA10/SEG14																											
9	P009/INT0_1/SIN11_0/IN10_0/TIOA1_0/MDATA09/SEG15																											
10	P010/SOT11_0/SDA11_0/IN11_0/TIOA2_0/MDATA08/SEG16		Output "L"/ Input blocked	Output "L"/ Last status retained	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3 #6	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #6	Last state retained #3 #6	Hi-Z/ Input blocked #6													
11	P012/SCK11_0/SCL11_0/OUT5_0/TIOA3_0/ MDEX/SEG17																											
12	P013/SCS110_0/OUT6_0/TIOA4_0/ MDEX/SEG18																											
13	P015/SCS111_0/OUT7_0/TIOA5_0/ MGSX0/SEG19																											
14	P016/SCS112_0/OUT8_0/TIOA6_0/ MGSX1/SEG20																											
15	P017/SCS113_0/OUT9_0/TIOA7_0/ MDQMO/SEG21																											
16	P018/OUT10_0/TIOA8_0/ MDQM1/SEG22																											
17	P019/TEXT0_0/OUT11_0/TIOB0_0/MAD15/SEG23/ST0 #9															With control	Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3 #6	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #1	Last state retained #3 #6	Hi-Z/ Input blocked #6
18	P020/SOT0_0/SDA0_0/TEXT1_0/TIOB1_0																											
19	P021/SCK0_0/SCL0_0/SCK4_1/TIOB2_0																											
20	P022/INT3_0/SIN0_0/TIOB3_0																											
21	P023/SCS0_0/SIN4_1/TIOB4_0/MAD16/SEG24/ST1 #9																											
22	P024/SOT4_1/TIOB5_0/MAD17/SEG25/ST2 #9																											
23	P027/SCS42_1/TEXT0_1/TIOB6_0/TIOA4_1/MAD18/SEG26/ST3 #9																											
24	P028/SIN1_0/OUT0_1/TIOB7_0/MAD19/SEG27/ST4 #9																											
25	P029/SOT1_0/OUT1_1/MAD20/SEG28/ST5 #9	Output "L"/ Input blocked	Output "L"/ Last status retained	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Output "L"/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3 #6	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #6	Last state retained #3 #6	Hi-Z/ Input blocked #6														
26	P030/SCS43_1/OUT2_1/TIOB8_0/MAD21/SEG29/ST6 #9																											
27	P031/SCS1_0/OUT3_1/MAD22/SEG30/ST7 #9																											
28	P100/SCK1_0/OUT4_1/MAD23/SEG31/ST8 #9																											
29	P101/AN3/OUT5_1/MDATA07														With control		Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #1	Last state retained #3	Hi-Z/ Input blocked #6
30	P103/AN5/OUT6_1/TIOB9_0/MDATA06																											
31	P105/OUT7_1/TIOA9_0/MDATA05																											
32	P106/TX1_2/OUT8_1/TINO/MDATA04																											
33	P107/INT2_1/RX1_2/OUT9_1/TIOA10_0/TOTO/MDATA03																											
34	P108/INT3_1/AN6/OUT10_1/TIOA11_0/TINI/MRDY																											
35	P109/OUT11_1/TIOA12_0/TOT1/MCLK																											
39	P112/AN9/TIOA13_0/TIN2/MDATA02																											
40	P113/TIOA5_1/TOT2/MDATA01																											
41	P114/AN10/TIOA6_1/TIN3/MDATA00																											
45	P115/TIOB10_0/TOT3																											
46	P117/INT4_1/AN12/TIOB11_0/TIN16																											
47	P118/INT5_1/AN13/TIOB12_0/TOT16																											
48	P119/AN14/SCS90_0/TIOB13_0/TIN17																											
49	P120/AN15/SCS91_0/TOT17																											
50	P122/AN17/SCS92_0/TIOA11_1/SGA0_0																											
51	P123/AN18/SCS93_0/TIOA12_1/SGA0_0																											
52	P126/AN19/SGA1_0	With control	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #1	Last state retained #3	Hi-Z/ Input blocked #6														
53	P127/AN20/TEXT1_1/SGA1_0																											
54	P128/AN21/TEXT2_1/SGA2_0																											
55	P129/AN22/IN6_1/SGA2_0																											
56	P130/INT5_0/AN23/SIN9_0/INT_1																											
57	P131/AN24/SOT9_0/SDA9_0/IN8_1																											
58	P202/INT6_1/SCK9_0/SCL9_0/IN9_1																											
59	P203/IN10_1/TIOB19_0/AIN8_1																											
60	P204/AN27/IN11_1/TIOB20_0/BIN8_1																											
61	P205/AN28/TEXT3_1/TIOB21_0/ZIN8_1																											
62	P206/AN29/SCS43_0/TEXT4_1/TIOB22_0																											
63	P207/INT7_1/AN30/SCK4_0/SCL4_0/TEXT5_1/SPISEL3																											
64	P208/AN31/SCS42_0/TIOA19_0/SPISEL2																											
65	P209/AN32/SOT4_0/SDA4_0/TIOA20_0/SPISEL1																											
66	P210/INT6_0/AN33/SIN4_0/INO_2/TIOA21_0/SPICK																											
67	P211/AN34/SCS40_0/IN1_2/TIOA22_0/SPIDAT0																											
68	P212/AN35/SCS41_0/SCS80_1/IN2_2/TIOA13_1/SPIDAT2																											
69	P213/INT8_1/SIN8_1/IN3_2/TIOA14_1/SPIDAT1	With control	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retains #6	Last state retained #3	Hi-Z/ Input blocked #6	Hi-Z/ Input blocked #1	Last state retained #3	Hi-Z/ Input blocked #6														
70	P214/SOT8_1/IN4_2/TIOA15_1/SPISEL0																											
71	P215/INT9_1/SCK8_1/IN5_2/TIOA16_1/SPIDAT3																											

Table 9-2 Pin State Table (2/2)

Pin No.	Pin Name	GPORTEN Control	External Reset Factor 1			External Reset Factor 2			External Reset Factor 3	Internal Reset Factor #2	Sleep mode	Stop mode #4		Timer mode #4	
			External factor generation in progress	After external factor releasing		External factor generation in progress	After external factor releasing					High Impedance disabled (SYS0_SPEFGR, PSSPACTRL=0)	When High Impedance Enabled (SYS0_SPEFGR, PSSPACTRL=1)	High Impedance disabled (SYS0_SPEFGR, PSSPACTRL=0)	When High Impedance Enabled (SYS0_SPEFGR, PSSPACTRL=1)
			Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORTEN setting)	Internal reset issuance in progress	Internal reset issuance in progress	After internal reset issuance (Before GPORTEN setting)	Internal reset issuance in progress			After internal reset issuance (Before GPORTEN setting)	CPU Sleep mode		
74	P218/AN36/TEXT2_0/T10B14_0	With control	Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retain	Last state retained	Last state retained #3	Hi-Z/ Input blocked	Last state retained #3	Hi-Z/ Input blocked	
75	P219/AN37/TEXT3_0/T10B15_0														
76	P220/AN38/TX2_0/SCS83_0/IN6_2/T10B16_0														
77	P222/INT7_0/AN39/RX2_0/SIN8_0/IN7_2														
78	P223/AN40/PMU_AN0/SCS81_0/IN8_2/AIN9_1														
79	P224/AN41/PMU_AN1/TX0_2/SCS80_0/IN9_2/BIN9_1														
80	P225/INT0_0/AN42/PMU_AN2/RX0_2/SOT8_0/SDA8_0/IN10_2/T10B17_0/ZIN9_1														
81	P226/AN43/PMU_AN3/SCK8_0/SCL8_0/IN11_2/T10A17_1														
87	P229/INT8_0/AN46/PMU_AN6/OUT0_0/T10A25_0/PMW1P0														
88	P230/AN47/PMU_AN7/OUT1_0/T10A26_0/PMW1M0														
89	P231/AN48/OUT2_0/T10A27_0/PMW2P0														
90	P300/AN49/OUT3_0/T10A28_0/PMW2M0														
91	P301/AN50/OUT4_0/T10A18_1/PMW1P1														
92	P302/AN51/T10A19_1/PMW1M1														
93	P304/AN52/TEXT4_0/T10A20_1/PMW2P1														
94	P305/AN53/TEXT5_0/T10A29_0/PMW2M1														
97	P307/INT1_0/AN55/SCS102_0/T10B18_0/PMW1P2														
98	P308/AN56/IN0_1/T10A28_1/PMW1M2														
99	P309/AN57/IN1_1/T10A29_1/PMW2P2														
100	P312/AN58/SCS101_0/IN2_1/T10B25_0/PMW2M2														
101	P313/INT10_1/AN59/SOT10_0/SDA10_0/IN3_1/T10B26_0/PMW1P3														
102	P314/AN60/SCK10_0/SCL10_0/IN4_1/T10B27_0/T10A7_1/PMW1M3														
103	P315/AN61/TX1_1/SCS100_0/IN5_1/T10B28_0/T10A8_1/PMW2P3														
104	P317/INT11_1/AN62/RX1_1/SIN10_0/T10B29_0/T10A9_1/PMW2M3														
107	P321/PMUTRG	-	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked #8 (Status immediately before the shutdown retain) #6 (PMUTRG output/ Input blocked #7)	Hi-Z/ Input blocked #8 (Last state retained) #6 (PMUTRG output/ Input blocked #7)	Hi-Z/ Input blocked #8 (Last state retained) #3 #6 (#7)	Hi-Z/ Input blocked #8 (Last state retained) #3	Hi-Z/ Input blocked				
110	TRST/P322		Input enabled	Input enabled	Input enabled	Input enabled	Input enabled (Status immediately before the shutdown retain #7)	Input enabled (Last state retained #7)	Input enabled (Last state retained #3 #7)	Input enabled (Hi-Z/ Input blocked #7)	Input enabled (Hi-Z/ Input blocked #7)				
111	TDO/P323		-	-	-	-									
112	TDI/P324		Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled				
113	TMS														
114	TCK														
115	P327/WOT	With control	Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retain	Last state retained	Last state retained #3	Hi-Z/ Input blocked	Last state retained #3	Hi-Z/ Input blocked		
116	NMI_X	-	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled				
117	ND														
118	X0														
119	X1														
121	P331/MCSX3/SGAO_1	With control	Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retain	Last state retained	Last state retained #3	Hi-Z/ Input blocked	Last state retained #3	Hi-Z/ Input blocked		
122	P400/MCSX2/SGO0_1														
123	RSTX	-	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled				
127	P401/TX1_0/IN0_0	With control	Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retain	Last state retained #3	Last state retained #3	Hi-Z/ Input blocked #1	Hi-Z/ Input blocked #1	Hi-Z/ Input blocked #1		
128	P402/INT2_0/RX1_0/IN1_0/V3														
129	P403/IN2_0/TRACEDATA0/V2/SGA1_1														
130	P404/SCS120_0/IN3_0/TRACEDATA1/MAD14/V1/SGO1_1														
131	P405/INT11_0/SIN12_0/IN4_0/TRACEDATA2/MAD13/V0/SGA2_1														
132	P406/SOT12_0/TRACEDATA3/MAD12/COM0/SGO2_1 #9														
133	P407/SCK12_0/SCK10_1/TRACEDATA4/MAD11/COM1 #9														
134	P408/SIN2_0/TRACEDATA5/TIN18/MAD10/COM2 #9														
135	P409/SOT2_0/T10A24_1/TRACEDATA6/TOT18/MAD09/COM3 #9														
136	P411/INT13_1/SCK2_0/SCS101_1/T10B24_0/TRACEDATA7/TIN19/MAD08/SEGO														
137	P413/INT14_1/SCS20_0/SCS103_1/TOT19/MAD07/SEG1														
138	P414/SCS21_0/TIN32/MAD06/SEG2														
139	P416/SIN10_1/IN5_0/T10A22_1/TOT32/MAD05/SEG3														
140	P417/INT15_1/SOT10_1/T10A23_1/TIN33/MAD04/SEG4														
141	P418/INT14_0/SCS22_0/T10B23_0/TOT33/MAD03/SEG5														
142	P420/SCK2_1/TRACECLK/MAD02/SEG6														
143	P421/INT12_1/SIN2_1/TRACECTL/MAD01/SEG7														
			Hi-Z/ Input blocked	Hi-Z/ Last status retained	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Hi-Z/ Input blocked	Status immediately before the shutdown retain #6	Last state retained #3	Last state retained #3	Hi-Z/ Input blocked #1	Hi-Z/ Input blocked #1	Hi-Z/ Input blocked #1		

- *1: Input disable is not valid when external interrupts are enabled.
- *2: Recovery from standby (power off) becomes a factor.
- *3: The pin state from the time that HOLDIO_PD2 was set (SYSC0_SPECIFGR.HOLDIO_PD2 = 1) is retained. If power-off has not occurred and HOLDIO_PD2 has not been set (SYSC0_SPECIFGR.HOLDIO_PD2 = 0), the last state is retained.
- *4: To power off power domains 2 and 3, be sure to set HOLDIO_PD2 (SYSC0_SPECIFGR.HOLDIO_PD2 = 1).
- *5: The pin state when the PORT function is enabled is shown.
- *6: When Port is used as LCD setting, PIN state becomes the following.

Power Domain 2 Control	Power-Off	Power-on		
mode	-	Except PSS Main oscillation Timer mode	PSS Main oscillation Timer mode	
Main oscillation enable setting	-	-	enable (LCR0:LCEN = 1)	disable (LCR0:LCEN = 0)
PIN state	Output "L" / Input blocked	Output "L" / Input blocked	Retention of LCD display	Output "L" / Input blocked

- *7: When the PWU function is enabled, a change to output occurs.
- *8: When PPC_PCFGRIj:POF[2:0] is set to initial value.
- *9: When reset is issued, the following ports become "L" output as the initial state.
- P019, P023, P024, P027, P028, P029, P030, P031, P100, P406, P407, P408, P409
- Therefore, don't add the Pull-up registers outside of this product to the above ports.
- In case that the above ports are used as Pull-up, use the Pull-up function implemented in this product.
- External Reset Factor 1
 - Power-on reset (PONR)
 - RAM retention low-voltage detection reset (RVD)
 - Internal power supply low-voltage detection reset (LVDL1R)
 - RSTX pin + MD pin simultaneous assert reset (INITX)
 - External Reset Factor 2
 - RSTX pin input reset (RSTX)
 - External Reset Factor 3
 - Hardware watchdog reset (HWDR)
 - Software watchdog reset (SWDR)
 - PLL clock supervisor reset (CSVPRn)
 - SSCG clock supervisor reset (CSVSRn)
 - Profile error reset (PRFERR)
 - Software trigger hard reset (SHRST)
 - Software reset (SRST)
 - Internal Reset Factor
 - Standby transition reset/ Power domain reset

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1, *2}	V _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	
	DV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	DV _{CC} = V _{CC}
Analog supply voltage ^{*1, *2}	AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{CC} = V _{CC}
Analog reference voltage ^{*1}	AVRH	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC}
Input voltage ^{*1}	V _{I1}	V _{SS} -0.3	V _{CC} +0.3	V	
	V _{I2}	DV _{SS} -0.3	DV _{CC} +0.3	V	SMC shared pin
Analog pin input voltage ^{*1}	V _{IA1}	V _{SS} -0.3	V _{CC} +0.3	V	
	V _{IA2}	DV _{SS} -0.3	DV _{CC} +0.3	V	SMC shared pin
Output voltage ^{*1}	V _{O1}	V _{SS} -0.3	V _{CC} +0.3	V	
	V _{O2}	DV _{SS} -0.3	DV _{CC} +0.3	V	SMC shared pin
Maximum clamp current	I _{CLAMP}	-	4	mA	*8
Total maximum clamp current	Σ I _{CLAMP}	-	20	mA	*8
"L"-level maximum output current ^{*3}	I _{OL1}	-	3.5	mA	When setting is 1 mA ^{*6}
	I _{OL2}	-	7	mA	When setting is 2 mA
	I _{OL3}	-	40	mA	When setting is 30 mA ^{*7}
"L"-level average output current ^{*4}	I _{OLAV1}	-	1	mA	When setting is 1 mA ^{*6}
	I _{OLAV2}	-	2	mA	When setting is 2 mA
	I _{OLAV3}	-	30	mA	When setting is 30 mA ^{*7}
"L"-level total output current ^{*5}	ΣI _{OL1}	-	40	mA	*6
	ΣI _{OL2}	-	150	mA	*7
"H"-level maximum output current ^{*3}	I _{OH1}	-	-3.5	mA	When setting is 1 mA ^{*6}
	I _{OH2}	-	-7	mA	When setting is 2 mA
	I _{OH3}	-	-40	mA	When setting is 30 mA ^{*7}
"H"-level average output current ^{*4}	I _{OHAV1}	-	-1	mA	When setting is 1 mA ^{*6}
	I _{OHAV2}	-	-2	mA	When setting is 2 mA
	I _{OHAV3}	-	-30	mA	When setting is 30 mA ^{*7}
"H"-level total output current ^{*5}	ΣI _{OH1}	-	-40	mA	*6
	ΣI _{OH2}	-	-150	mA	*7
Power consumption	P _D	-	2000	mW	S6J312xHzC ^{*9}
Operating temperature	T _A	-40	+105	°C	
Storage temperature	T _{stg}	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS} = DV_{SS} = AV_{SS} = 0.0 V.

*2: AV_{CC}, DV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} and DV_{CC} do not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current X the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: general-purpose ports

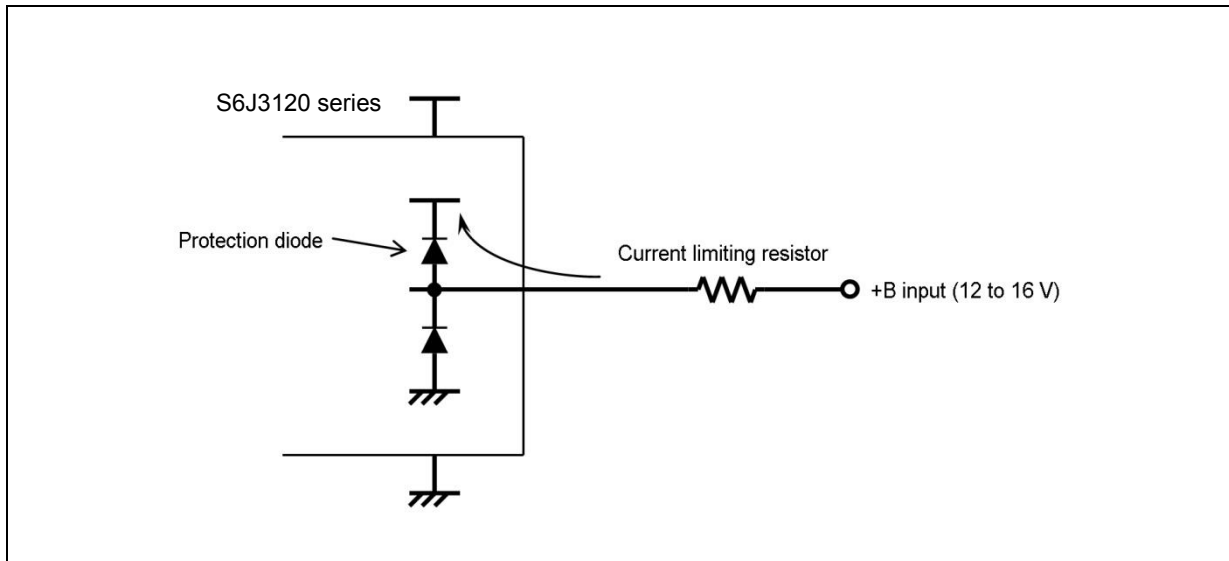
*7: Corresponding pins: P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317

*8: Corresponding pins: All general-purpose ports and analog input pins.

- Use the device within the recommended operating conditions.
- Use the device with direct voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*9: It is standard when four-layer substrate is used.

Example of a recommended circuit



WARNING:

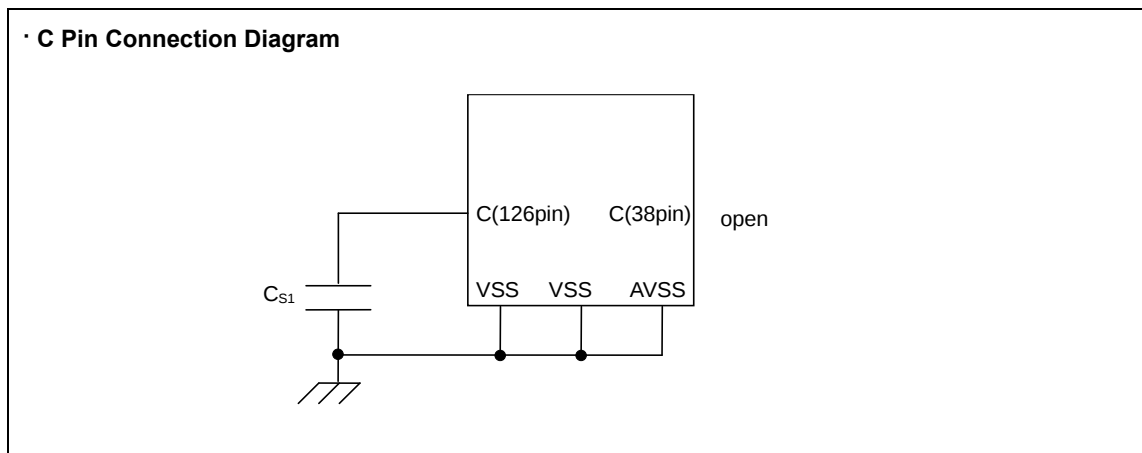
- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

10.2 Recommended Operating Conditions

 $(V_{SS} = DV_{SS} = AV_{SS} = 0.0 \text{ V})$

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	4.5	5.5	V	Recommended operation assurance range
	DV_{CC}	4.5	5.5	V	
	AV_{CC}	4.5	5.5	V	
	V_{CC}	3.5	5.5	V	Operation assurance range
	DV_{CC}	3.5	5.5	V	
	AV_{CC}	3.5	5.5	V	
Smoothing capacitor*	C_{S1}	4.7		μF	Tolerance of up to $\pm 40\%$, 126 pin Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	$^{\circ}\text{C}$	S6J312xHzC* * x:A/9, z:A/B

*: For the connections of smoothing capacitor C_{S1} , see the following diagram.



WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

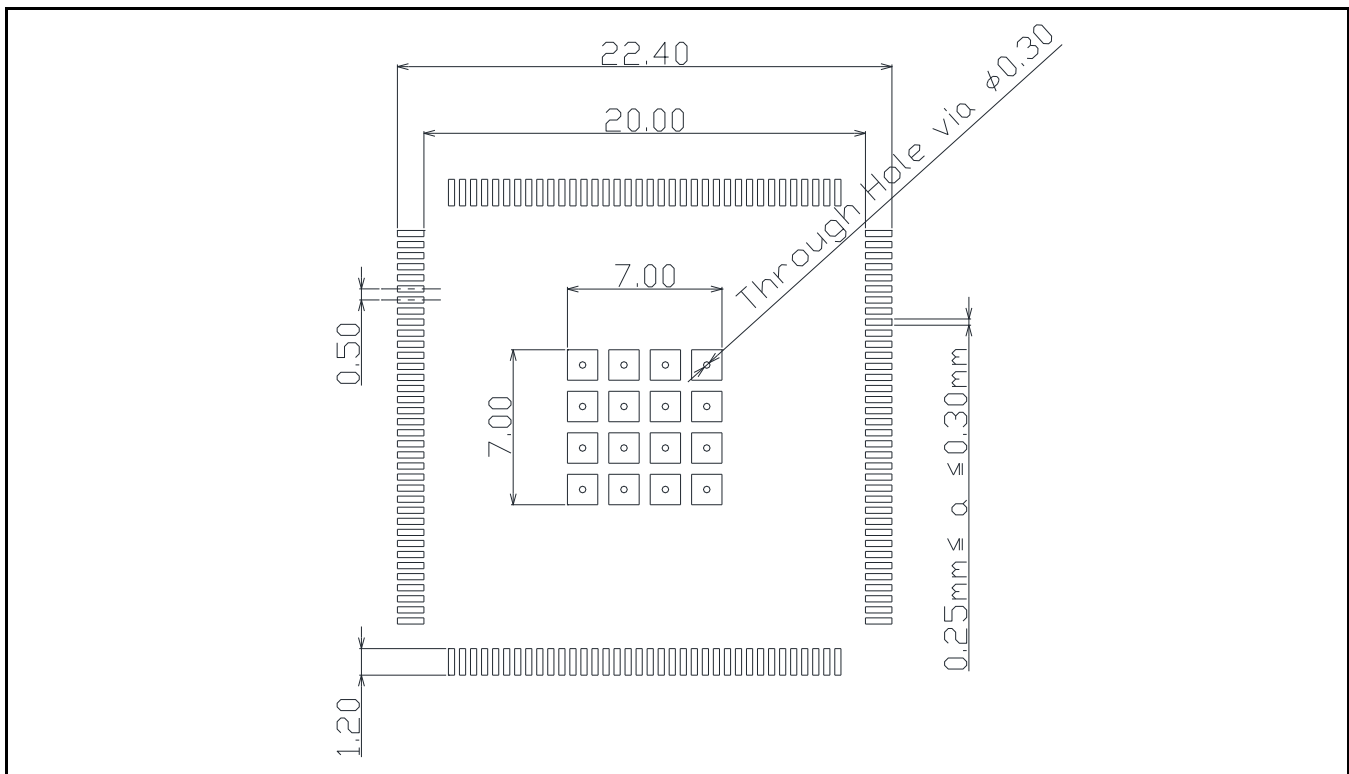
Notes:

- The following condition should be satisfied in order to facilitate heat dissipation.
 1. 4 or more layers PCB should be used.
 2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)
 3. 1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90 % or more. The layer can be used for system ground.
 4. 35~50 % of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.
 5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.

Figure10.2-1: Example thermal via holes on PCB.

Notes:

- Figure 10.2-1 is a schematic diagram showing PCB in section.
- Figure 10.2-2 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.
- If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Figure 10.2-2: Land Pattern and Thermal Via LEU144


10.3 DC Characteristics

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V _{IH1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P327, P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	CMOS Schmitt input level selected	0.7×V _{CC}	-	V _{CC} +0.3	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317		0.7×DV _{CC}	-	DV _{CC} +0.3	V	
"H" level input voltage	V _{IH2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P327 to P331 P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Automotive input level selected	0.8×V _{CC}	-	V _{CC} +0.3	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317		0.8×DV _{CC}	-	DV _{CC} +0.3	V	
	V _{IH4}	RSTX, NMIX	-	0.7×V _{CC}	-	V _{CC} +0.3	V	
	V _{IH5}	MD	-	0.7×V _{CC}	-	V _{CC} +0.3	V	
	V _{IH6}	TRST, TCK, TDI, TMS	TTL input level	2.3	-	V _{CC} +0.3	V	
"L" level input voltage	V _{IL1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P327 to P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	CMOS Schmitt input level selected	V _{SS} -0.3	-	0.3×V _{CC}	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317		DV _{SS} -0.3	-	0.3×DV _{CC}	V	

(TA: Recommended operating conditions, Vcc = DVcc = 5.0 V ±10 %, Vss = DVss = AVss = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V _{IL2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P327, P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Automotive input level selected	Vss-0.3	-	0.5×V _{CC}	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317		DVss-0.3	-	0.5×DV _{CC}	V	
	V _{IL4}	RSTX, NMIX	-	Vss-0.3	-	0.3×V _{CC}	V	
	V _{IL5}	MD	-	Vss-0.3	-	0.3×V _{CC}	V	
	V _{IL6}	TRST, TCK, TDI, TMS	TTL input level	Vss-0.3	-	0.8	V	
"H" level output voltage	V _{OH1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P321 to P324, P327, P331, P400 to P401, P403 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V _{CC} = 4.5 V I _{OH} = -2.0 mA	V _{CC} -0.5	-	V _{CC}	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OH} = -2.0 mA	DV _{CC} -0.5	-	DV _{CC}	V	
"H" level output voltage	V _{OH2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P321 to P324, P327, P331, P400 to P401, P403 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V _{CC} = 4.5 V I _{OH} = -1.0 mA	V _{CC} -0.5	-	V _{CC}	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OH} = -1.0 mA	DV _{CC} -0.5	-	DV _{CC}	V	
"H" level output voltage	V _{OH3}	P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OH} = -30.0 mA	DV _{CC} -0.5	-	DV _{CC}	V	

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V _{OL1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P321 to P324, P327, P331, P400 to P401, P403 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V _{CC} = 4.5 V I _{OL} = 2.0 mA	0	-	0.4	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OL} = 2.0 mA	0	-	0.4	V	
"L" level output voltage	V _{OL2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P321 to P324, P327, P331, P400 to P401, P403 to P409, P411, P413 to P414, P416 to P418, P420 to P421	V _{CC} = 4.5 V I _{OL} = 1.0 mA	0	-	0.4	V	
		P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OL} = 1.0 mA	0	-	0.4	V	
"L" level output voltage	V _{OL3}	P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	DV _{CC} = 4.5 V I _{OL} = 30.0 mA	0	-	0.55	V	

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I _{IL}	All input pins	V _{CC} = DV _{CC} = AV _{CC} = 5.5 V V _{SS} < V _I < V _{CC}	-5	-	+5	μA	
Pull-up resistor	R _{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R _{UP2}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317, P327, P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Pull-up resistor selected	25	-	100	kΩ	
	R _{UP3}	TDI(P324), TMS, TCK	-	25	-	100	kΩ	
Pull-down resistor	R _{DOWN1}	P000 to P001, P003, P005 to P010, P012 to P013, P015 to P024, P027 to P031, P100 to P101, P103, P105 to P109, P112 to P115, P117 to P120, P122 to P123, P126 to P131, P202 to P215, P218 to P220, P222 to P226, P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317, P327, P331, P400 to P409, P411, P413 to P414, P416 to P418, P420 to P421	Pull-down resistor selected	25	-	100	kΩ	
	R _{DOWN2}	TRST(P322)	-	25	-	100	kΩ	
Input capacitance	C _{IN}	Pins other than VCC, VSS, AVCC0, AVCC1, AVSS0, AVSS1	-	-	5	15	pF	

(T_A: Recommended operating conditions, V_{cc} = DV_{cc} = 5.0 V ±10 %, V_{ss} = DV_{ss} = AV_{ss} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current S6J312xHzC * *x:A/9 z: A/B	I _{CC5}	VCC	Normal operation	-	90	195	mA	Operating at 128 MHz
			Flash write/erase	-	125	255	mA	Operating at 128 MHz
	I _{CCS5}		CPU Sleep	-	60	160	mA	Operating at 128 MHz
	I _{CCT5}		Timer mode	-	480	1450	μA	T _A = 25 °C Slow-CR source Oscillation
	I _{CCT5M}		Timer mode (Main OSC)	-	1340	2525	μA	T _A = 25 °C Main source Oscillation*
	I _{CCH5}		Stop mode	-	480	1450	μA	T _A = 25 °C
	I _{CCP}		PWU mode (Shutdown)	-	52.5	129.7	μA	T _A = 25 °C (PWU operation cycle 16 ms)
				-	46.2	115.5	μA	T _A = 25 °C (PWU operation cycle 32 ms)
	I _{CCT52}		Timer mode (Shutdown)	-	40	100	μA	T _A = 25 °C Slow-CR source Oscillation
	I _{CCT52M}		Timer mode (Main OSC) (Shut down)	-	350	520	μA	T _A = 25 °C Main source Oscillation*
	I _{CCH52}		Stop mode (Shutdown)	-	40	100	μA	T _A = 25 °C

Refer to Hardware manual "APPENDIX State transition" for Internal clock frequency setting / Setting of the power domain / Regulator setting.

*: The external load capacitance connected to X0/X1 is considered as 10 pF.

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current Output drive Capacity Phase to phase deviation1	ΔV_{OH3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn (n = 0 to 3)	DV _{CC} = 4.5 V I _{OH} = -30.0 mA Maximum deviation of V _{OH3}	-	-	90	mV	*
High current Output drive Capacity Phase to phase Deviation2	ΔV_{OL3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn (n = 0 to 3)	DV _{CC} = 4.5 V I _{OH} = -30.0 mA Maximum deviation of V _{OL3}	-	-	90	mV	*
LCD divider resistor	R _{LCD}	V0 to V1, V1 to V2, V2 to V3	-	6.25	12.5	25	kΩ	
COM0 to COM3 output impedance	R _{VCOM}	COMm (m = 0 to 3)	-	-	-	4.5	kΩ	
SEG00 to SEG31 output impedance	R _{VSEG}	SEGN (n = 00 to 31)	-	-	-	17	kΩ	
LCDC leak current	I _{LCDC}	V0 to V3, COMm (m = 0 to 3) SEGN (n = 00 to 31)	T _A = 25 °C	-0.5	-	+0.5	μA	

*: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of VOH3/VOL3 for each pin is defined. Same for other channels.

10.4 AC Characteristics

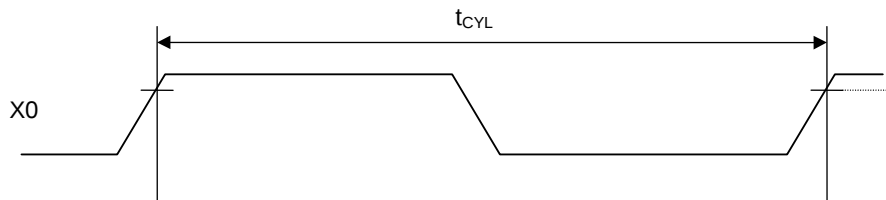
10.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _C	X0, X1	-	-	4	-	MHz	
Source oscillation clock cycle time	t _{CYL}	X0, X1	-	-	250	-	ns	
CAN PLL jitter (during lock)	t _{PJ}	-	-	-10	-	+10	ns	*
Built-in slow-CR oscillation frequency	F _{CRS}	-	-	50	100	150	kHz	
Built-in fast-CR oscillation frequency	F _{CRF}	-	-	2.4	4	6.0	MHz	
PLL input clock frequency	F _{PLLI}	-	-	-	4	-	MHz	
PLL macro oscillation clock frequency	F _{PLLO}	-	-	400	-	512	MHz	
SSCG-PLL input clock frequency	F _{SSCGPLLI}	-	-	-	4	-	MHz	
SSCG-PLL macro oscillation clock frequency	F _{SSCGPLLO}	-	-	400	-	512	MHz	

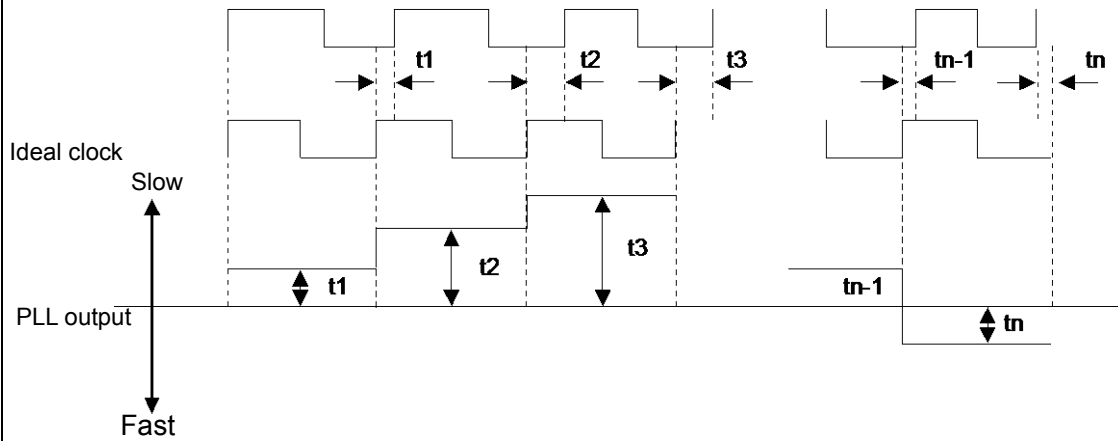
*: The maximum/minimum values have been standardized with the main clock and PLL clock in use.

- X0 and X1 clock timing



- CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.



10.4.2 Internal Clock Timing

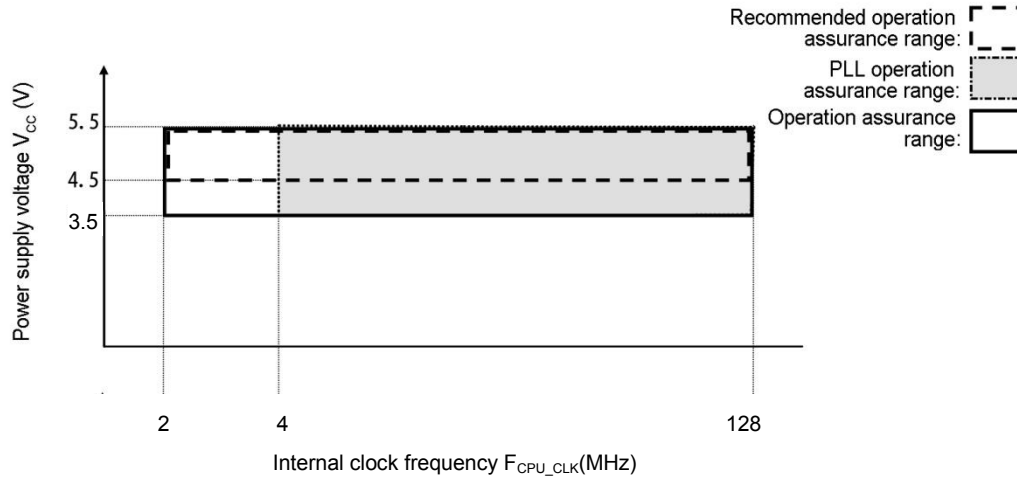
(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	S6J312xHzC* Value * x:A/9, z:A/B			Unit	Remarks
				Min	Typ	Max		
Internal Clock Frequency	F _{CLK_CPU}	-	-	-	-	128	MHz	CLK_CPU
	F _{CLK_FCLK}	-	-	-	-	64	MHz	CLK_FCLK
	F _{CLK_ATB}	-	-	-	-	64	MHz	CLK_ATB
	F _{CLK_DBG}	-	-	-	-	64	MHz	CLK_DBG
	F _{CLK_HPM}	-	-	-	-	32	MHz	CLK_HPM
	F _{CLK_HPM2}	-	-	-	-	16	MHz	CLK_HPM2
	F _{CLK_DMA}	-	-	-	-	32	MHz	CLK_DMA
	F _{CLK_MEMC}	-	-	-	-	32	MHz	CLK_MEMC
	F _{CLK_EXTBUS}	-	-	-	-	25	MHz	CLK_EXTBUS
	F _{CLK_SYSC1}	-	-	-	-	32	MHz	CLK_SYSC1
	F _{CLK_HAPP0A0}	-	-	-	-	32	MHz	CLK_HAPP0A0
	F _{CLK_HAPP0A1}	-	-	-	-	32	MHz	CLK_HAPP0A1
	F _{CLK_HAPP1B0}	-	-	-	-	32	MHz	CLK_HAPP1B0
	F _{CLK_HAPP1B1}	-	-	-	-	32	MHz	CLK_HAPP1B1
	F _{CLK_LLBBM}	-	-	-	-	128	MHz	CLK_LLBBM
	F _{CLK_LLBBM2}	-	-	-	-	64	MHz	CLK_LLBBM2
	F _{CLK_LCP}	-	-	-	-	64	MHz	CLK_LCP
	F _{CLK_LCP0}	-	-	-	-	32	MHz	CLK_LCP0
	F _{CLK_LCP0A}	-	-	-	-	32	MHz	CLK_LCP0A
	F _{CLK_LCP1}	-	-	-	-	32	MHz	CLK_LCP1
	F _{CLK_LCP1A}	-	-	-	-	32	MHz	CLK_LCP1A
	F _{CLK_LAPP0}	-	-	-	-	32	MHz	CLK_LAPP0
	F _{CLK_LAPP0A}	-	-	-	-	32	MHz	CLK_LAPP0A
	F _{CLK_LAPP1}	-	-	-	-	32	MHz	CLK_LAPP1
	F _{CLK_LAPP1A}	-	-	-	-	32	MHz	CLK_LAPP1A
	F _{CLK_TRC}	-	-	-	-	64	MHz	CLK_TRC
	F _{CLK_HSSPI}	-	-	-	-	32	MHz	CLK_HSSPI
	F _{CLK_SYSC0H}	-	-	-	-	32	MHz	CLK_SYSC0H
	F _{CLK_COMH}	-	-	-	-	32	MHz	CLK_COMH
	F _{CLK_RAM0H}	-	-	-	-	32	MHz	CLK_RAM0H
	F _{CLK_RAM1H}	-	-	-	-	32	MHz	CLK_RAM1H
	F _{CLK_SYSC0P}	-	-	-	-	32	MHz	CLK_SYSC0P
	F _{CLK_COMP}	-	-	-	-	32	MHz	CLK_COMP
	F _{CANFD_CCLK}	-	-	-	-	40	MHz	CANFD_CCLK

Parameter	Symbol	Pin Name	Conditions	S6J312xHzC* Value * x:A/9, z:A/B			Unit	Remarks
				Min	Typ	Max		
Internal clock cycle time	tCLK_CPU	-	-	7.82	-	-	ns	CLK_CPU
	tCLK_FLASH	-	-	15.64	-	-	ns	CLK_FCLK
	tCLK_ATB	-	-	15.64	-	-	ns	CLK_ATB
	tCLK_DBG	-	-	15.64	-	-	ns	CLK_DBG
	tCLK_HPM	-	-	31.28	-	-	ns	CLK_HPM
	tCLK_HPM2	-	-	62.54	-	-	ns	CLK_HPM2
	tCLK_DMA	-	-	31.28	-	-	ns	CLK_DMA
	tCLK_MEMC	-	-	31.28	-	-	ns	CLK_MEMC
	tCLK_EXTBUS	-	-	40.00	-	-	ns	CLK_EXTBUS
	tCLK_SYSC1	-	-	31.28	-	-	ns	CLK_SYSC1
	tCLK_HAPP0A0	-	-	31.28	-	-	ns	CLK_HAPP0A0
	tCLK_HAPP0A1	-	-	31.28	-	-	ns	CLK_HAPP0A1
	tCLK_HAPP1B0	-	-	31.28	-	-	ns	CLK_HAPP1B0
	tCLK_HAPP1B1	-	-	31.28	-	-	ns	CLK_HAPP1B1
	tCLK_LLPBM	-	-	7.82	-	-	ns	CLK_LLPBM
	tCLK_LLPBM2	-	-	15.64	-	-	ns	CLK_LLPBM2
	tCLK_LCP	-	-	15.64	-	-	ns	CLK_LCP
	tCLK_LCP0	-	-	31.28	-	-	ns	CLK_LCP0
	tCLK_LCP0A	-	-	31.28	-	-	ns	CLK_LCP0A
	tCLK_LCP1	-	-	31.28	-	-	ns	CLK_LCP1
	tCLK_LCP1A	-	-	31.28	-	-	ns	CLK_LCP1A
	tCLK_LAPP0	-	-	31.28	-	-	ns	CLK_LAPP0
	tCLK_LAPP0A	-	-	31.28	-	-	ns	CLK_LAPP0A
	tCLK_LAPP1	-	-	31.28	-	-	ns	CLK_LAPP1
	tCLK_LAPP1A	-	-	31.28	-	-	ns	CLK_LAPP1A
	tCLK_TRC	-	-	15.64	-	-	ns	CLK_TRC
	tCLK_HSSPI	-	-	31.28	-	-	ns	CLK_HSSPI
	tCLK_SYSC0H	-	-	31.28	-	-	ns	CLK_SYSC0H
	tCLK_COMH	-	-	31.28	-	-	ns	CLK_COMH
	tCLK_RAM0H	-	-	31.28	-	-	ns	CLK_RAM0H
	tCLK_RAM1H	-	-	31.28	-	-	ns	CLK_RAM1H
	tCLK_SYSC0P	-	-	31.28	-	-	ns	CLK_SYSC0P
	tCLK_COMP	-	-	31.28	-	-	ns	CLK_COMP
	tCANFD_CCLK	-	-	25.00	-	-	ns	CANFD_CCLK

– Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

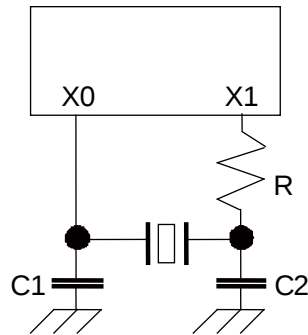


Note: A supply voltage that is equal to or less than the set voltage for low-voltage detection causes a reset.

Relationship between the oscillation clock frequency and internal clock frequency

Oscillation Clock Frequency	Main Clock	PLL Multiplier Setting	PLL Output Division Setting	PLL Clock
4 MHz	4 MHz	128	4	128 MHz
4 MHz	4 MHz	120	6	80 MHz

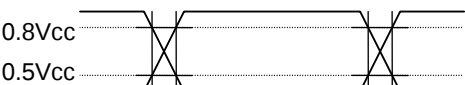
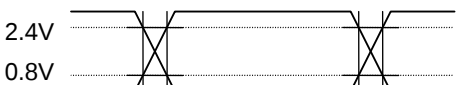
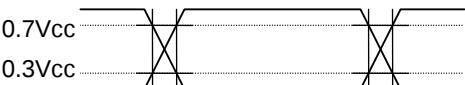
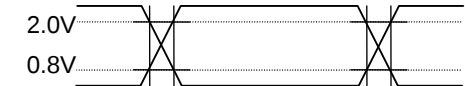
- Oscillation circuit example



Notes:

- When configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.
- The maximum PLL clock frequency must be 128MHz.
Output division configuration can be set by the following.
 - PLLDIVM bit in SYSC0_RUNPLL0CNTR register
 - PLLDIVM bit in SYSC0_PSSPLL0CNTR register
 - SSCGDIVM bit in SYSC0_RUNSSCG0CNTR0 register
 - SSCGDIVM bit in SYSC0_PSSSSCG0CNTR0 register
 (e.g. If PLLout is 448 MHz, these settings must be configured as "multiply by 4" and over multiplication setting)

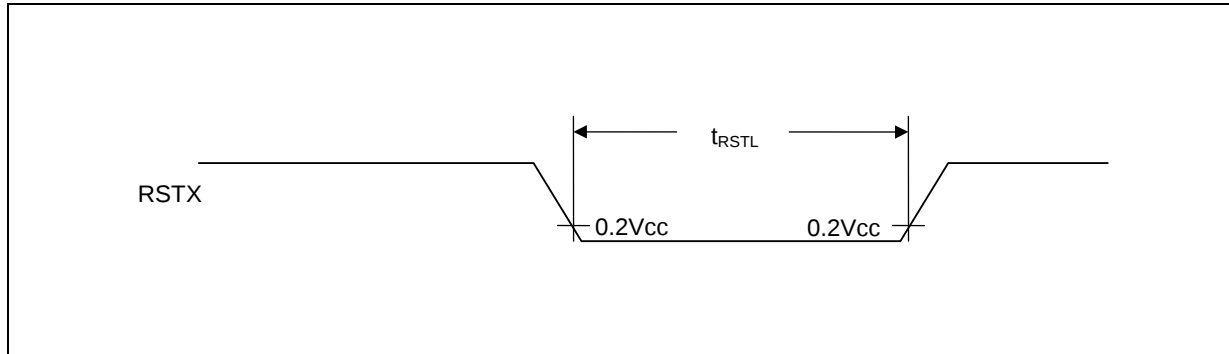
AC characteristics are specified by the following measurement reference voltage values.

Input signal waveform	Output signal waveform
Hysteresis input pin (Automotive) 	Output pin 
Hysteresis input pin (CMOS Schmitt) 	
Hysteresis input pin (TTL) 	

10.4.3 Reset Input

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{RSTL}	RSTX	-	10	-	μs	
Width for reset input removal				1	-	μs	



10.4.4 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC	-	2.15	2.35	2.55	V	
Level detection hysteresis width	-	VCC	-	-	100	-	mV	
Level detection time	-	-	-	-	-	540	μs	*1
Level release voltage	-	VCC	-	2.25	2.45	2.65	V	
Power off time	-	VCC	-	1	-	-	ms	*2
Power ramp rate	dV/dt	VCC	VCC: 0.2 V to 2.55 V	-	-	6	mV/μs	*3
Maximum ramp rate guaranteed to not generate power-on reset	dV/dt	VCC	VCC: Between 2.6 V and 4.5 V	-	-	50	mV/μs	*4

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: If VCC is held below 0.2 V for a minimum period of t_{OFF}, power-on reset will occur. If t_{OFF} is not satisfied, power-on reset will still occur if the power ramp rate is kept below 6 mV/μs.

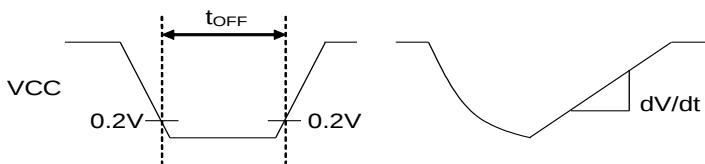
*3: This is the power ramp rate with which power-on reset will always occur regardless of power-off time, as mentioned in *2.

*4: When VCC is within 2.6 V - 4.5 V, and VCC fluctuation is below 50 mV/μs, the power-on reset is suppressed. Between 4.5 V - 5.5 V, the power-on reset does not occur with any VCC fluctuation.

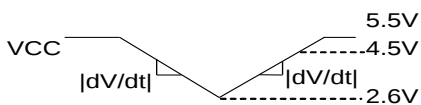
Note:

When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate at Power-on



• Maximum ramp rate guaranteed to not generate power-on reset



10.4.5 Clock Output Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)
 (External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t _{CYC}	MCLK	2 mA is selected in ODR bit in PPC_PCFGR register.	40	-	ns	
Clock high width *1	t _{CHCL}	MCLK		d _H t _{CYC} - 7	d _H t _{CYC} + 7	ns	
Clock low width *2	t _{CLCH}	MCLK		d _L t _{CYC} - 7	d _L t _{CYC} + 7	ns	

*1: If division-ratio is even value, d_H is equivalent to 0.5.

Otherwise, d_H is calculated as the following.

d_H = The number rounding "division-ratio x 0.5" down to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit and EXTBUSDIV bit setting.

ex). Setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, d_H is calculated as 0.429.

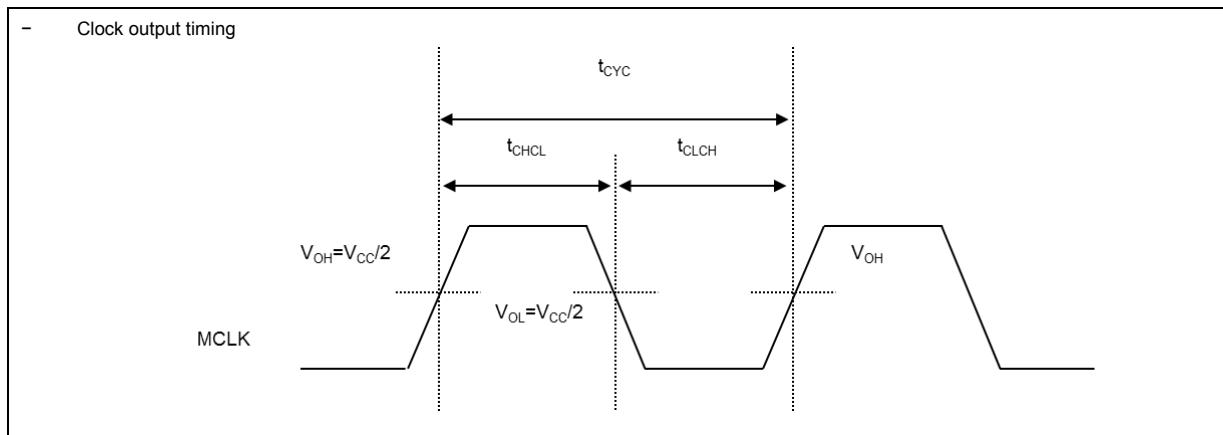
*2: If division-ratio is even value, d_L is equivalent to 0.5.

Otherwise, d_L is calculated as the following.

d_L = The number rounding "division-ratio x 0.5" up to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit and EXTBUSDIV bit setting.

ex). Setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, d_L is calculated as 0.571.



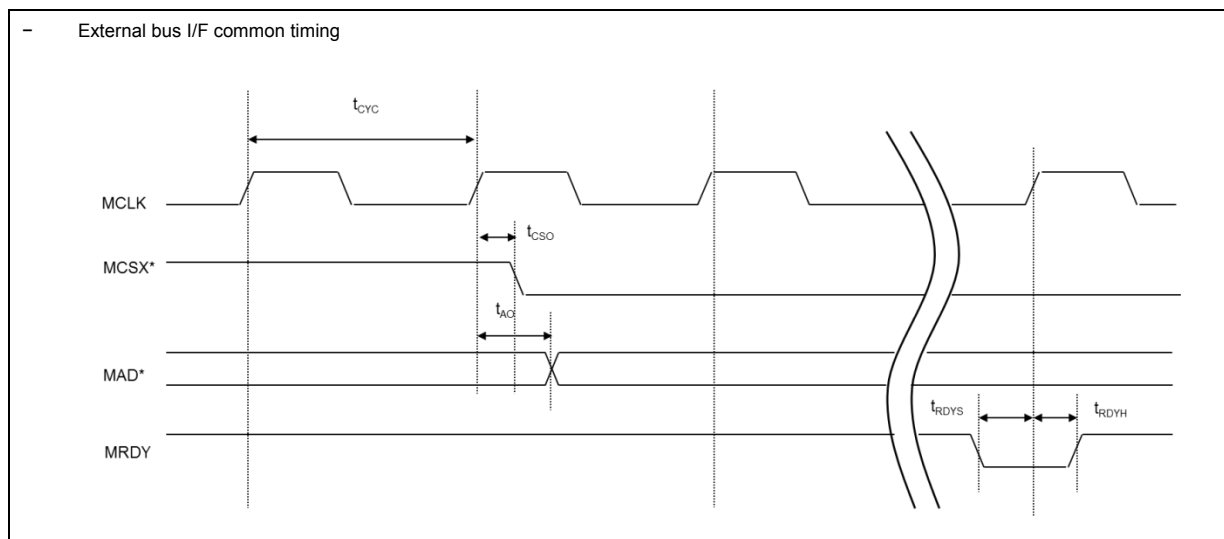
10.4.6 External Bus Interface Timing

10.4.6.1 Common Timing Between Read and Write

(TA: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

(External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time (without MRDY)	t _{CYC}	MCLK	2 mA is selected in ODR bit in PPC_PCFGR register.	40	-	ns	
Cycle time (with MRDY)	t _{CYC}	MCLK		50	-	ns	If using MRDY, set MCLK to 20 MHz or less.
CS delay time	t _{CSO}	MCLK, MCSX0 to MCSX3		0.5	18	ns	
Address delay time	t _{AO}	MCLK, MAD00 to MAD23		0.5	18	ns	
RDY setup time	t _{RDYS}	MCLK, MRDY	"CMOS Schmitt input" and "Disable noise filter" are selected in PPC_PCFGR register.	21	-	ns	
RDY hold time	t _{RDYH}	MCLK, MRDY		0	-	ns	

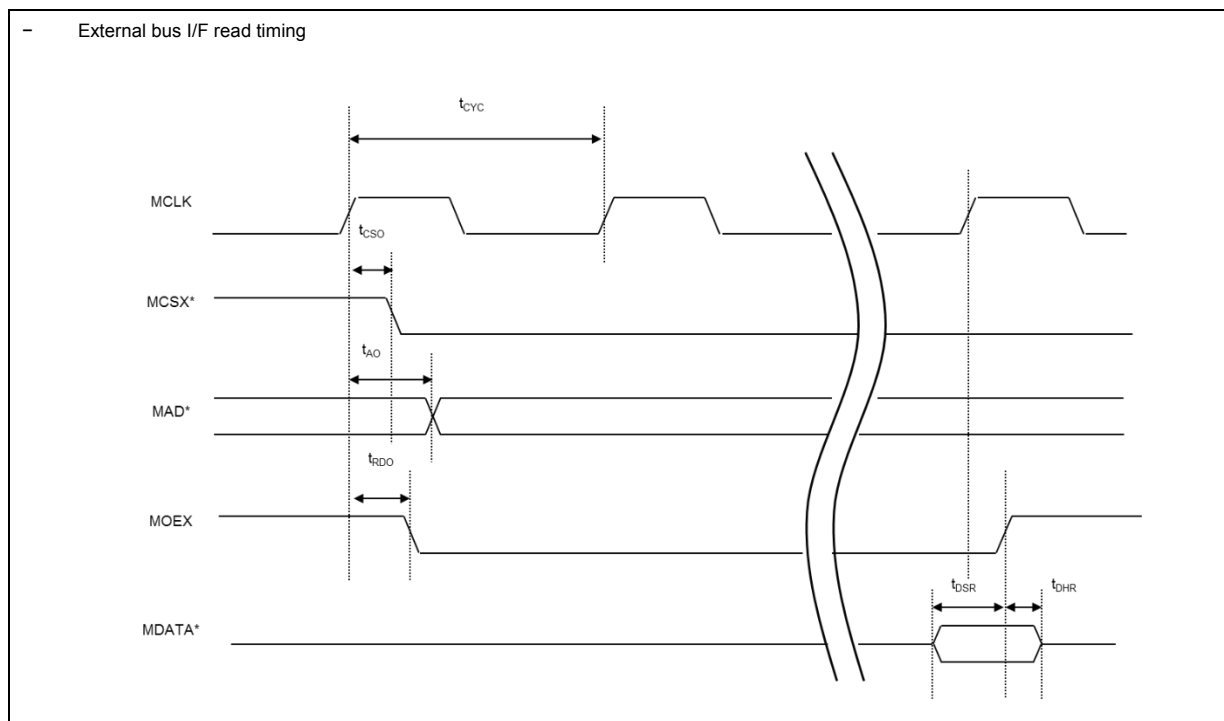


10.4.6.2 Read Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

(External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data setup time	t _{DSR}	MOEX, MDATA00 to MDATA15	"CMOS Schmitt input" and "Disable noise filter" are selected in PPC_PCFGR register.	21+t _{cyc}	-	ns	
Data hold time	t _{DHR}	MOEX, MDATA00 to MDATA15		0	-	ns	
MOEX delay time	t _{RDO}	MCLK, MOEX	2 mA is selected in ODR bit in PPC_PCFGR register.	0.5	18	ns	

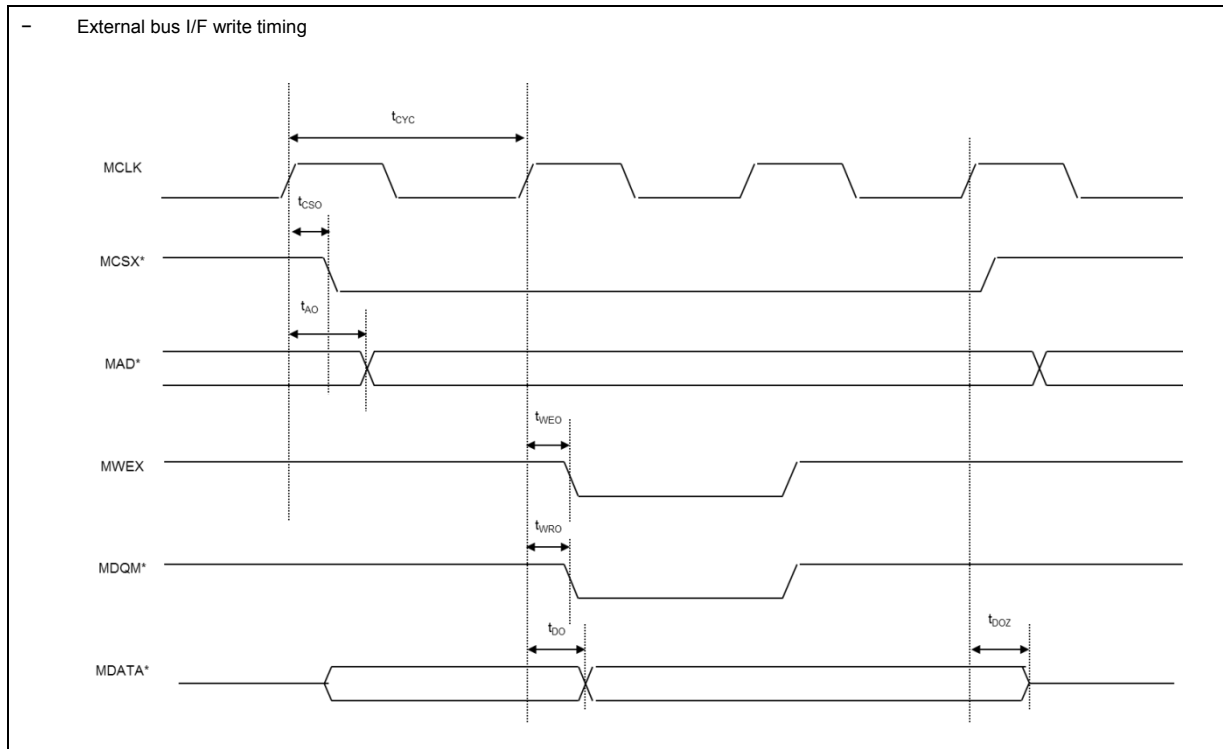


10.4.6.3 Write Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

(External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MWEX delay time	t _{WEO}	MCLK, MWEX	2 mA is selected in ODR bit in PPC_PCFGR register.	0.5	18	ns	
Byte mask delay time	t _{WRO}	MCLK, MDQM0 to MDQM1		0.5	18	ns	
Data delay time	t _{DO}	MCLK, MDATA00 to MDATA15		0.5	18	ns	
Data delay time (Hi-Z output)	t _{DOZ}	MCLK, MDATA00 to MDATA15		-	18	ns	



10.4.7 Multi-Function Serial

10.4.7.1 CSIO Timing (SMR:MD[2:0] = 010_B)

(5-1-1) Normal Synchronous Transfer (SCR:SPI = 0) and Serial Clock Output Signal Detect Level "H" (SMR:SCINV = 0)

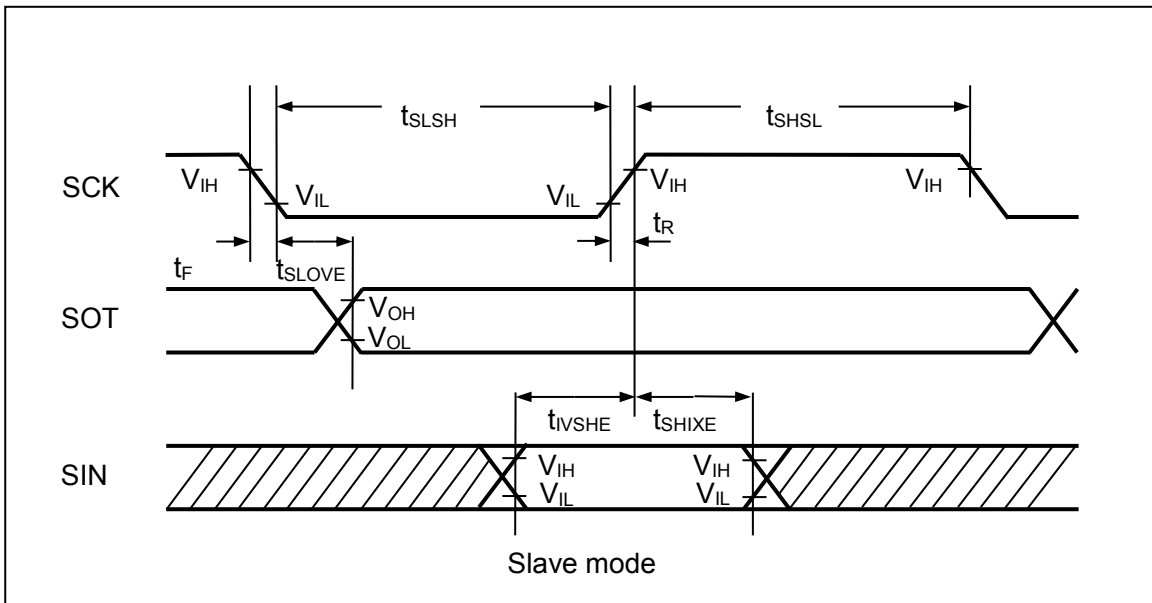
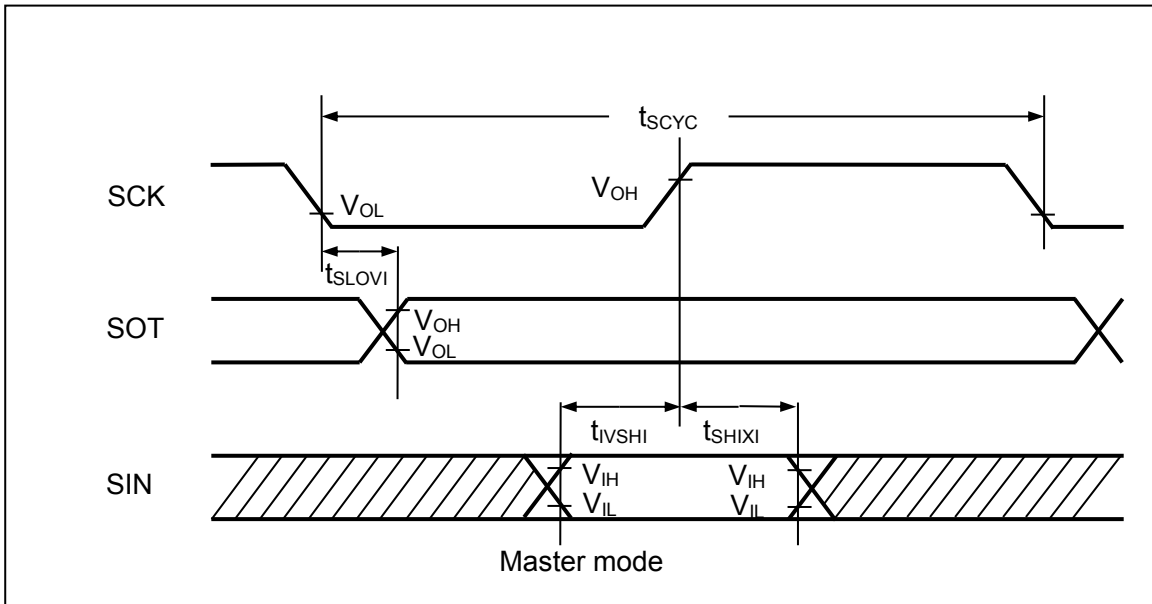
(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	4t _{CLK_LCPnA} *	-	ns	
SCK ↓ → SOT delay time	t _{SLOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		30	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CLK_LCPnA} * +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}			2t _{CLK_LCPnA} * -10	-	ns	
SCK ↓ → SOT delay time	t _{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-	30	ns	
Valid SIN → SCK ↑ setup time	t _{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		10	-	ns	
SCK ↑ → Valid SIN hold time	t _{SHIXE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		20	-	ns	
SCK fall time	t _F	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	
SCK rise time	t _R	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5-1-2) Normal Synchronous Transfer (SCR:SPI = 0) and Serial Clock Output Signal Detect Level "L"
(SMR:SCINV = 1)

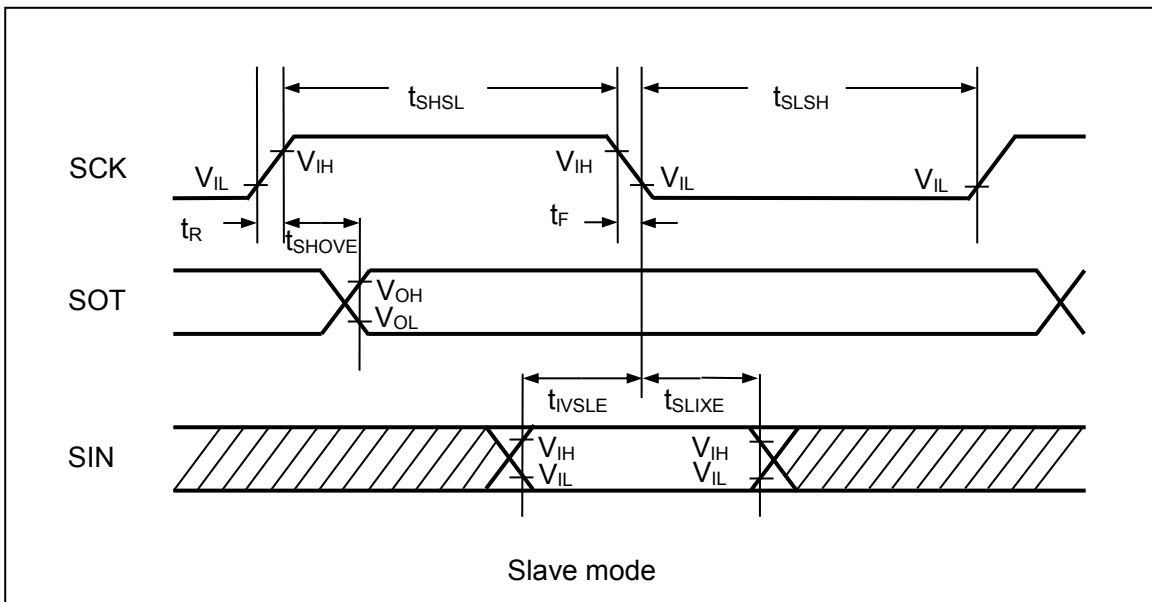
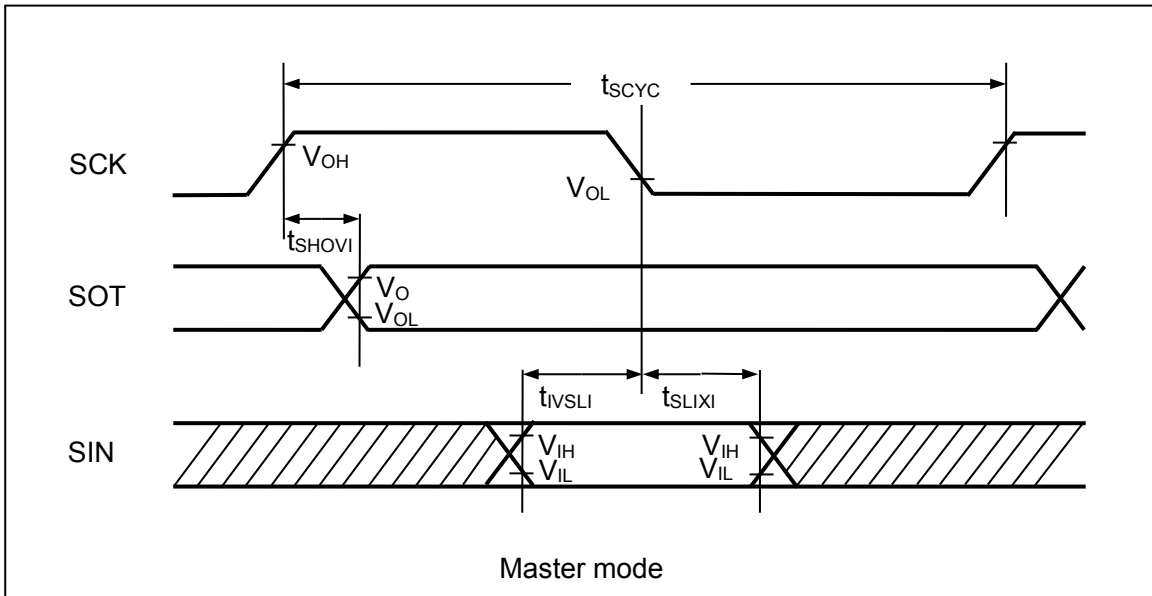
 (T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	4t _{CLK_LCPnA} *	-	ns	
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		30	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CLK_LCPnA} * +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}			2t _{CLK_LCPnA} * -10	-	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-	30	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		10	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		20	-	ns	
SCK fall time	t _F	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	
SCK rise time	t _R	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.



(5-1-3) SPI Supported (SCR:SPI = 1), and Serial Clock Output Signal Detect Level "H" (SMR:SCINV = 0)

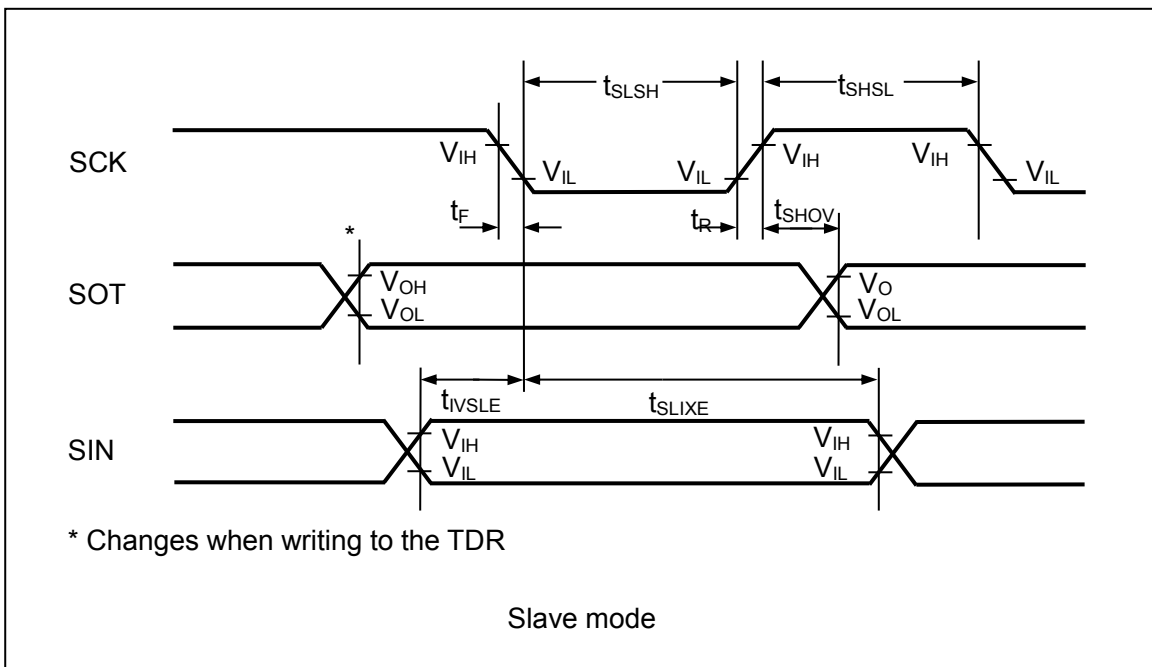
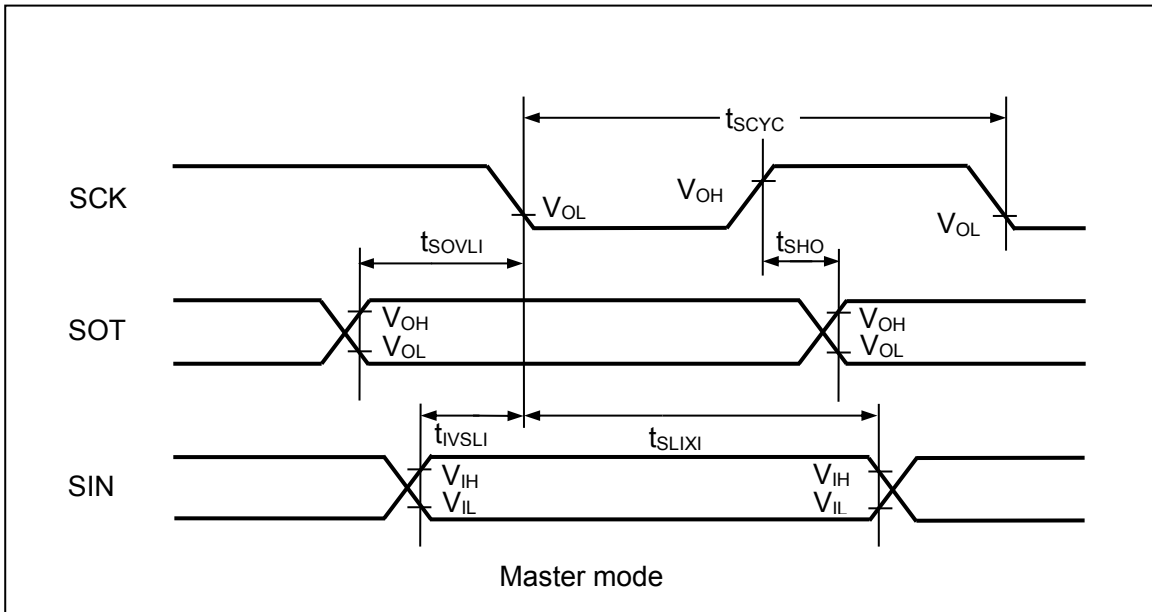
(TA: Recommended operating conditions, Vcc = DVcc = 5.0 V ±10 %, Vss = DVss = AVss = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	4t _{CLK_LCPnA} *	-	ns	
SCK ↑ → SOT delay time	t _{SHOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		30	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		0	-	ns	
SOT → SCK ↓ delay time	t _{SOVLI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		2t _{CLK_LCPnA} * -30	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CLK_LCPnA} * +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}			2t _{CLK_LCPnA} * -10	-	ns	
SCK ↑ → SOT delay time	t _{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-	30	ns	
Valid SIN → SCK ↓ setup time	t _{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		10	-	ns	
SCK ↓ → Valid SIN hold time	t _{SLIXE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		20	-	ns	
SCK fall time	t _F	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	
SCK rise time	t _R	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5-1-4) SPI Supported (SCR:SPI = 1), and Serial Clock Output Signal Detect Level "L" (SMR:SCINV = 1)

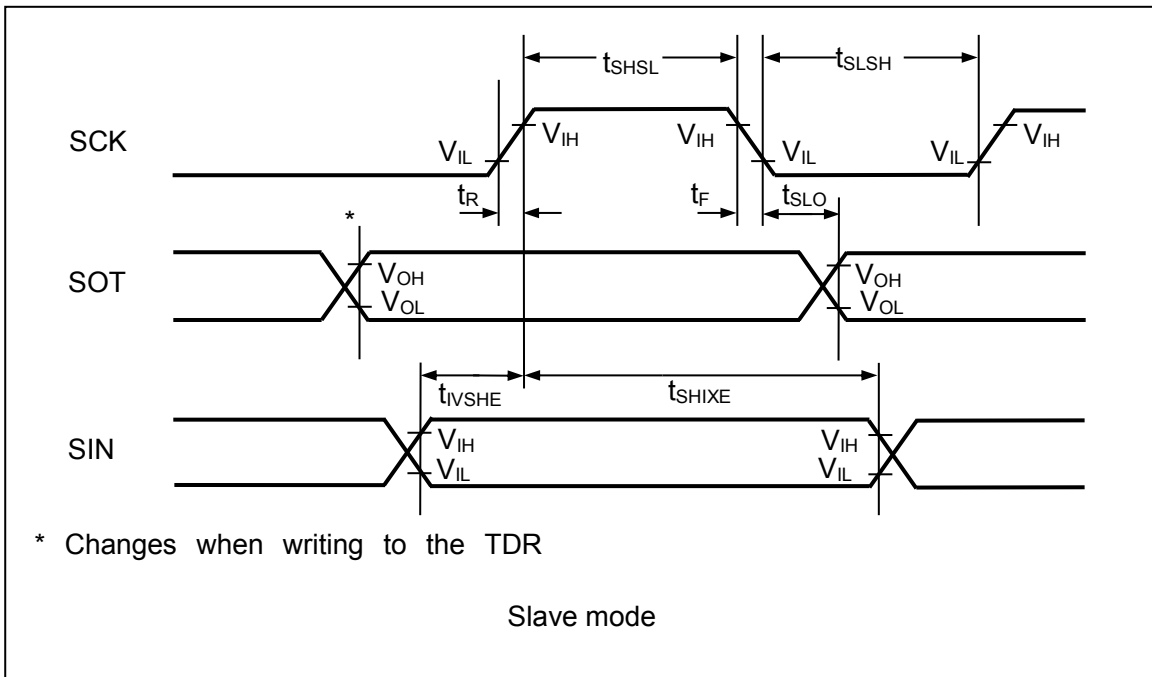
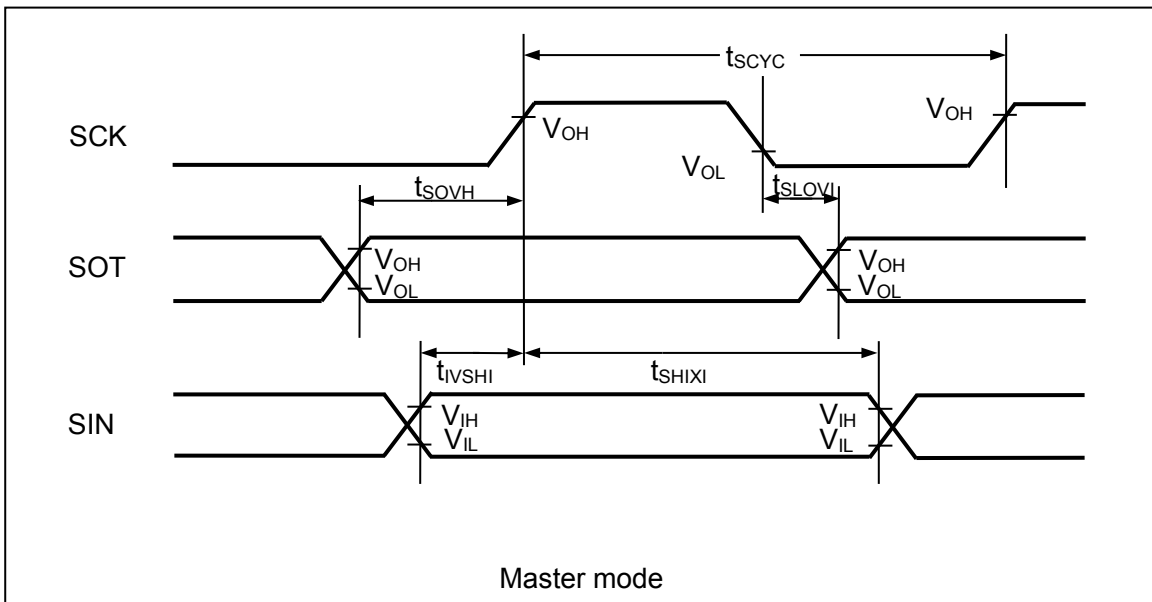
(TA: Recommended operating conditions, Vcc = DVcc = 5.0 V ±10 %, Vss = DVss = AVss = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master mode ($C_L = 50$ pF, $I_{OL} = -2$ mA, $I_{OH} = 2$ mA), ($C_L = 20$ pF, $I_{OL} = -1$ mA, $I_{OH} = 1$ mA)	$4t_{CLK_LCPnA}^*$	-	ns	
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		30	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		0	-	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		$2t_{CLK_LCPnA}^* - 30$	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave mode ($C_L = 50$ pF, $I_{OL} = -2$ mA, $I_{OH} = 2$ mA), ($C_L = 20$ pF, $I_{OL} = -1$ mA, $I_{OH} = 1$ mA)	$t_{CLK_LCPnA}^* + 10$	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK_LCPnA}^* - 10$	-	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		-	30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		10	-	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4, SCK8 to SCK12		-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5-1-5) Serial Chip Select Used (SCSCR:CSEN = 1)

■ Mark level "H" of serial clock output (SMR, SCSFR:SCINV = 0)

■ Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL = 1)

(TA: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ → SCK ↓ setup time	t _{CSSI}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CSSU} *1-50	-	ns	
SCK ↑ → SCS ↑ hold time	t _{CSHI}			t _{CSHD} *2+0	-	ns	
SCS deselect time	t _{CSDI}			SCS0x to SCS4x, SCS8x to SCS12x	t _{CSDS} *3-50 +5t _{CLK_LCPnA} *4	-	
SCS ↓ → SCK ↓ setup time	t _{CSSE}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +30	-	ns	
SCK ↑ → SCS ↑ hold time	t _{CSHE}			0	-	ns	
SCS deselect time	t _{CSDE}			3t _{CLK_LCPnA} *4 +30	-	ns	
SCS ↓ → SOT delay time	t _{DSE}	SCS0x to SCS4x, SCS8x to SCS12x, SOT0 to SOT4, SOT8 to SOT12		-	40	ns	
SCS ↑ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↓ → SCS ↓ clock switching time	t _{SCC}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x		Master mode round operation (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +0	3t _{CLK_LCPnA} *4 +50	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

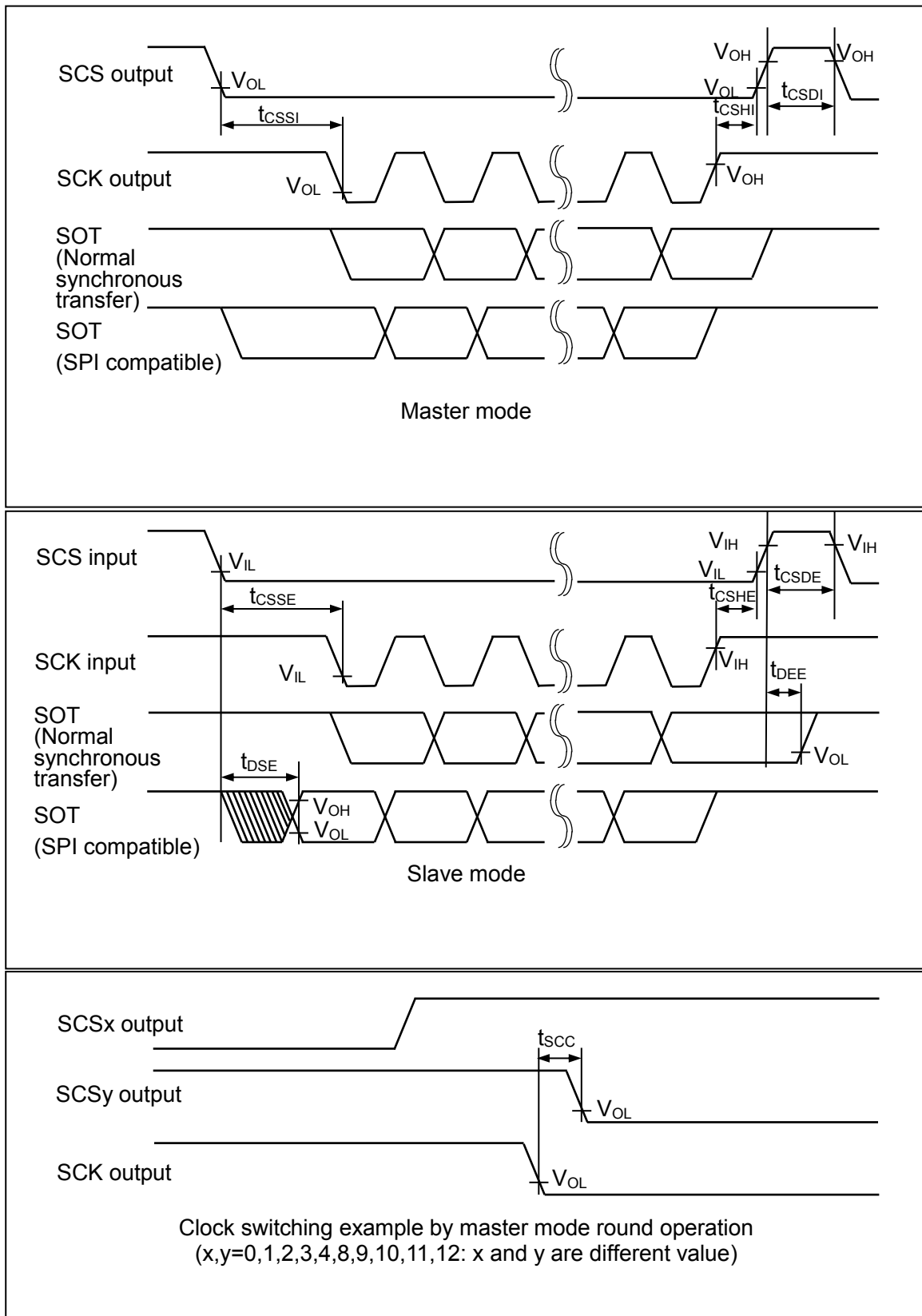
*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

*4 t_{CLK_LCPnA} n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.



(5-1-6) Serial Chip Select Used (SCSCR:CSSEN = 1)

■ Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■ Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL = 1)

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ → SCK ↑ setup time	t _{CSSU}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CSSU} *1-50	-	ns	
SCK ↓ → SCS ↑ hold time	t _{CSHI}			t _{CSHD} *2+0	-	ns	
SCS deselect time	t _{CSDI}			t _{CSDS} *3-50 + 5t _{CLK_LCPnA} *4	-	ns	
SCS ↓ → SCK ↑ setup time	t _{CSSE}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +30	-	ns	
SCK ↓ → SCS ↑ hold time	t _{CSHE}			0	-	ns	
SCS deselect time	t _{CSDE}			3t _{CLK_LCPnA} *4 +30	-	ns	
SCS ↓ → SOT delay time	t _{DSE}			-	40	ns	
SCS ↑ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↑ → SCS ↓ clock switching time	t _{SCC}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode round operation (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +0	3t _{CLK_LCPnA} *4 +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

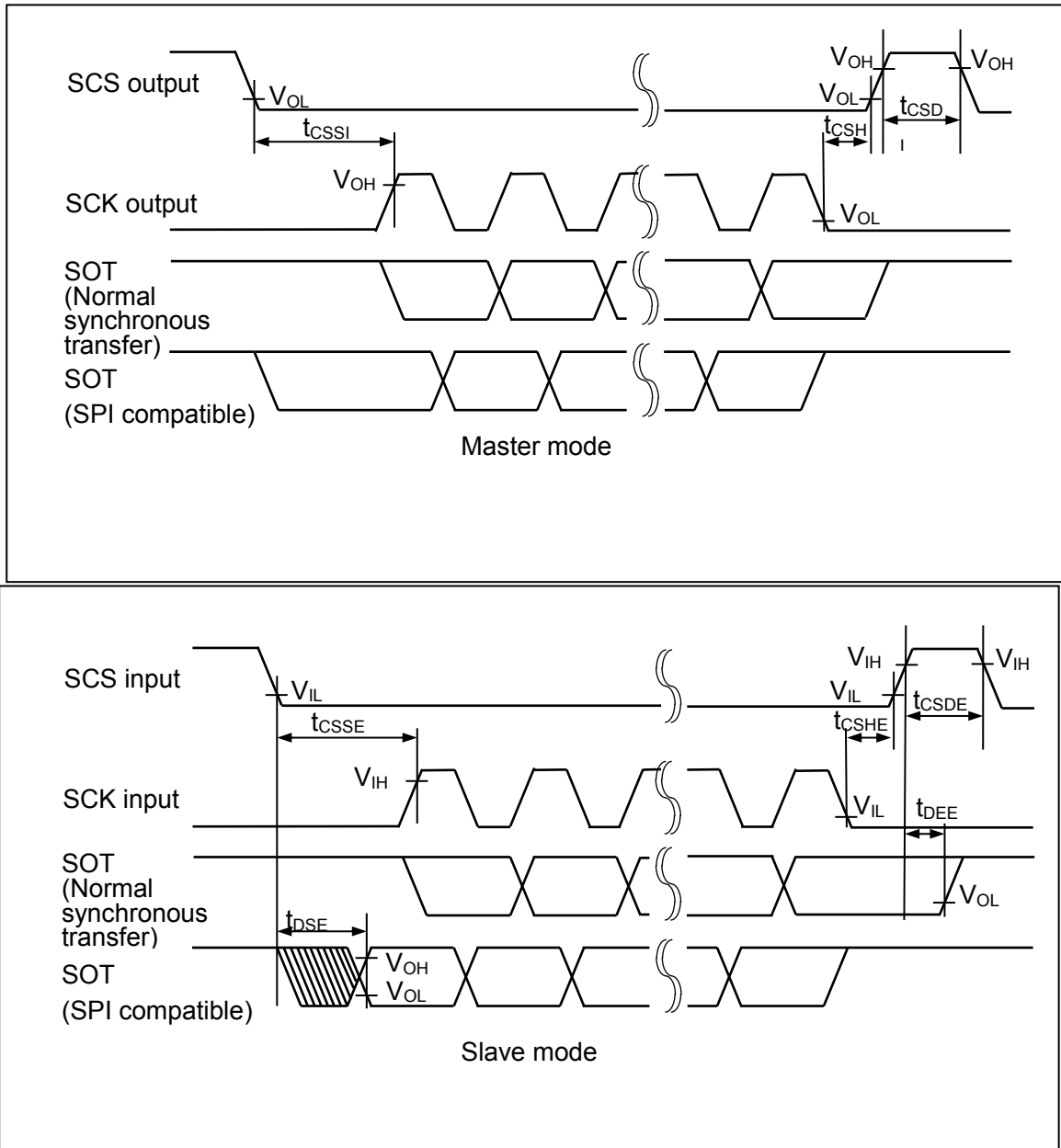
*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

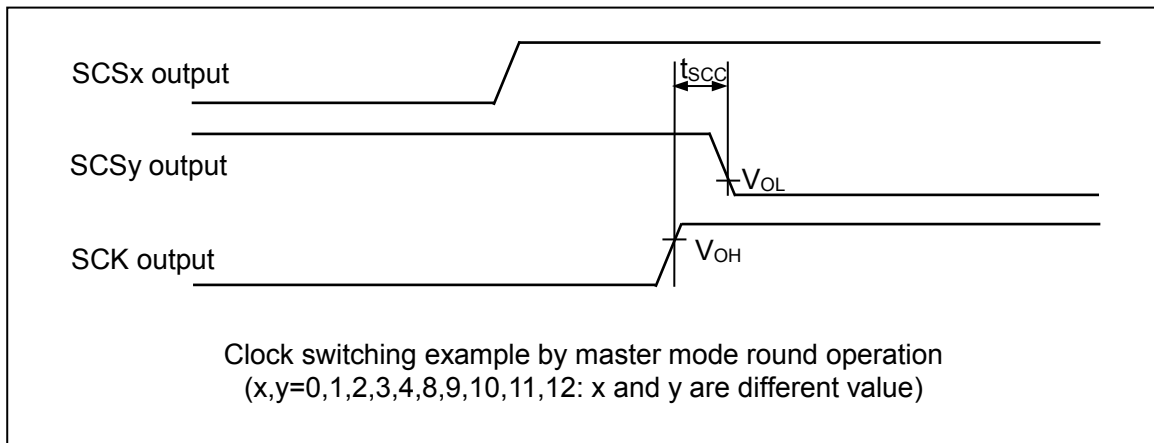
For details on *1, *2, and *3 above, see the hardware manual.

*4 t_{CLK_LCPnA} n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.





(5-1-7) Serial Chip Select Used (SCSCR:CSSEN = 1)

■ Serial clock output signal detect level "H" (SMR, SCSFR:SCINV = 0)

■ Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0

(TA: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↓ setup time	t _{CSSI}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CSSU} *1-50	-	ns	
SCK ↑ → SCS ↓ hold time	t _{CSHI}			t _{CSHD} *2+0	-	ns	
SCS deselect time	t _{CSDI}			t _{CSDS} *3-50 + 5t _{CLK_LCPnA} *4	-	ns	
SCS ↑ → SCK ↓ setup time	t _{CSSE}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +30	-	ns	
SCK ↑ → SCS ↓ hold time	t _{CSHE}			0	-	ns	
SCS deselect time	t _{CSDI}			3t _{CLK_LCPnA} *4 +30	-	ns	
SCS ↑ → SOT delay time	t _{DSE}			-	40	ns	
SCS ↓ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↓ → SCS ↑ clock switching time	t _{SCC}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode round operation (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4 +0	3t _{CLK_LCPnA} *4 +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

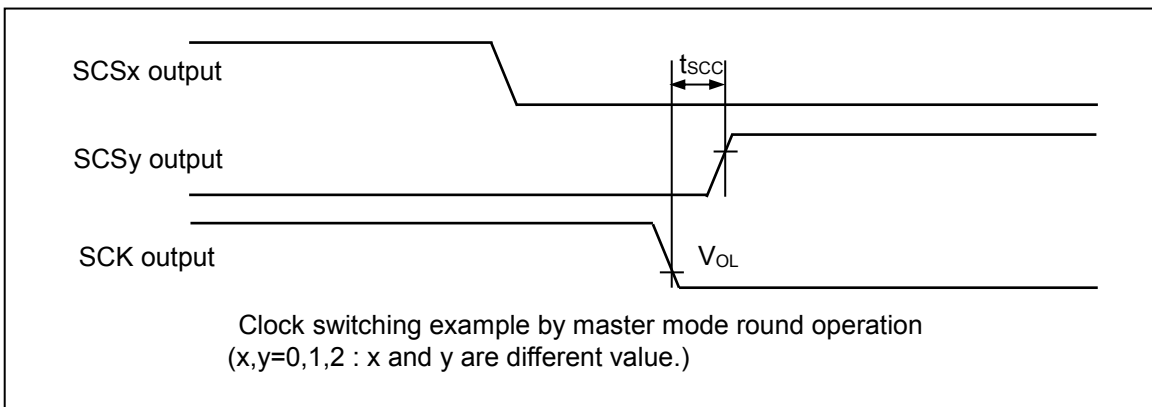
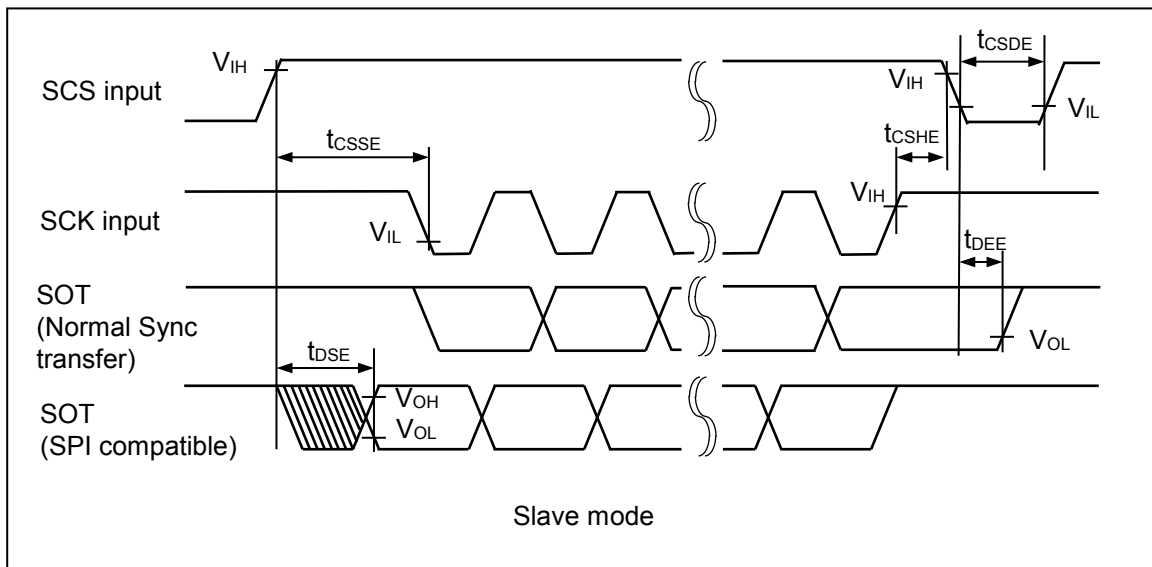
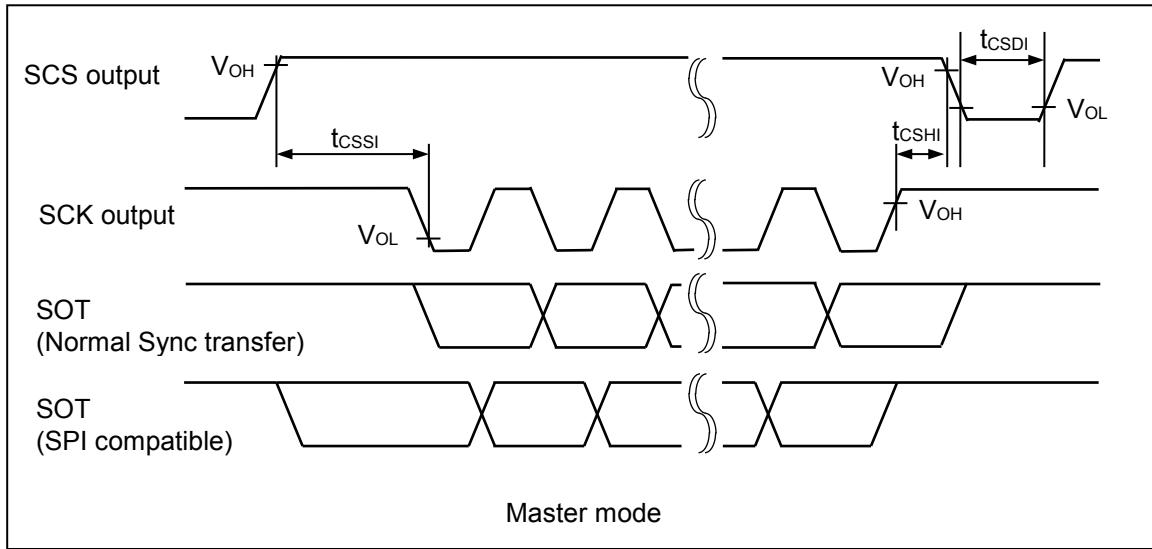
*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

*4 t_{CLK_LCPnA} n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual



(5-1-8) Serial Chip Select Used (SCSCR:CSSEN = 1)

■ Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)

■ Serial Chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0)

(TA: Recommended operating conditions, Vcc = DVcc = 5.0 V ±10 %, Vss = DVss = AVss = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ → SCK ↑ setup time	t _{CSSU}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CSSU} *1-50	-	ns	
SCK ↓ → SCS ↓ hold time	t _{CSHI}			t _{CSHD} *2+0	-	ns	
SCS deselect time	t _{CSDI}			t _{CSDS} *3-50 + 5t _{CLK_LCPnA} *4	-	ns	
SCS ↑ → SCK ↑ setup time	t _{CSSE}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Slave mode (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4+30	-	ns	
SCK ↓ → SCS ↓ hold time	t _{CSHE}			0	-	ns	
SCS deselect time	t _{CSDI}			3t _{CLK_LCPnA} *4+30	-	ns	
SCS ↑ → SOT delay time	t _{DSE}			-	40	ns	
SCS ↓ → SOT delay time	t _{DEE}			0	-	ns	
SCK ↑ → SCS ↑ clock switching time	t _{SCC}	SCK0 to SCK4, SCK8 to SCK12, SCS0x to SCS4x, SCS8x to SCS12x	Master mode round operation (C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	3t _{CLK_LCPnA} *4+0	3t _{CLK_LCPnA} *4 +50	ns	

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSHD} = SCSTR:CSHD[7:0] x serial chip select timing operating clock

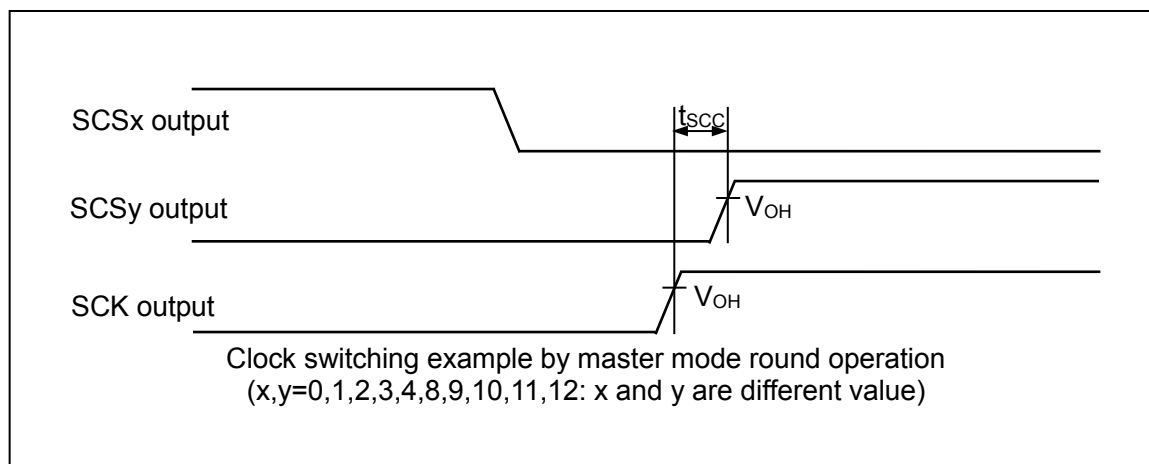
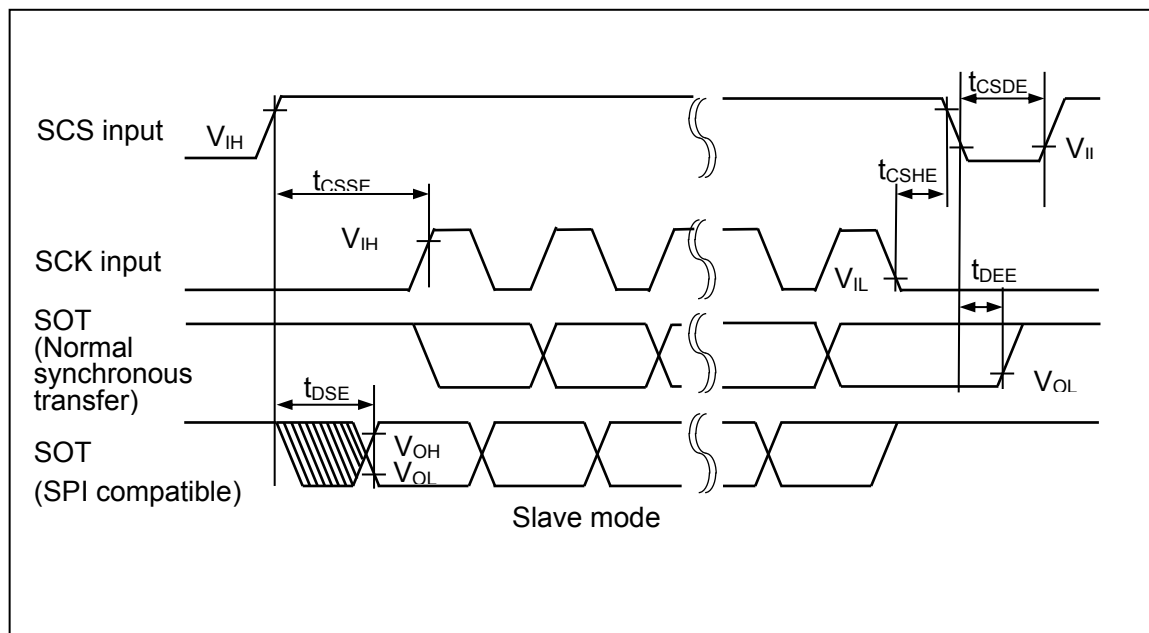
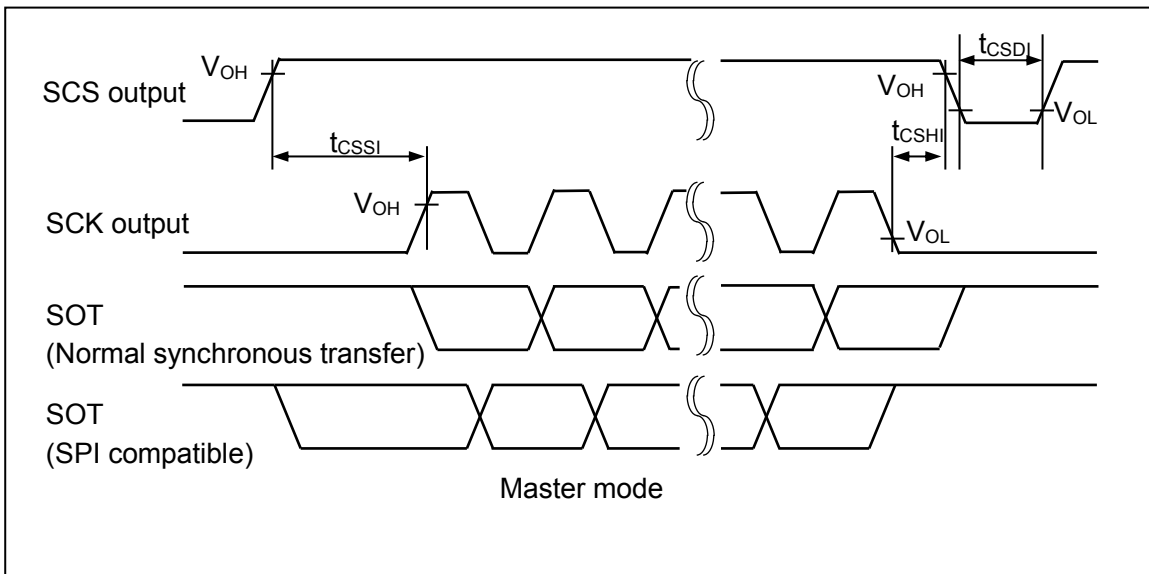
*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

For details on *1, *2, and *3 above, see the hardware manual.

*4 t_{CLK_LCPnA} n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12

Notes:

- This is the AC characteristic in CLK synchronized mode.
- CL is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



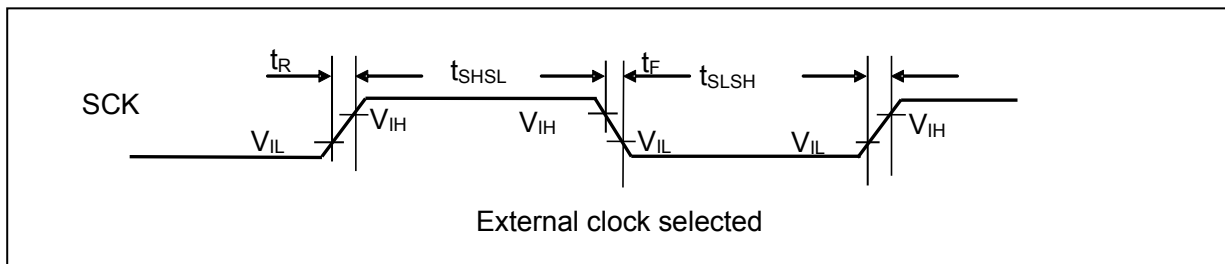
10.4.7.2 UART (Async Serial Interface) Timing (SMR:MD[2:0] = 000_B, 001_B)

(5-2-1) External Clock Selected (BGR:EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CLK_LCPnA} * + 10	-	ns	
Serial clock "H" pulse width	t _{SHSL}			t _{CLK_LCPnA} * + 10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12



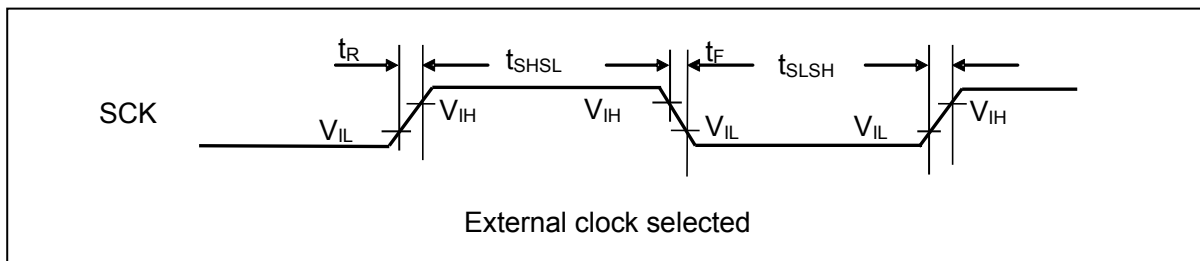
10.4.7.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR:MD[2:0] = 011_B)

(5-3-1) External Clock Selected (BGR:EXT = 1)

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(C _L = 50 pF, I _{OL} = -2 mA, I _{OH} = 2 mA), (C _L = 20 pF, I _{OL} = -1 mA, I _{OH} = 1 mA)	t _{CLK_LCPnA} * + 10	-	ns	
Serial clock "H" pulse width	t _{SHSL}			t _{CLK_LCPnA} * + 10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

*: n = 0:ch.0 to ch.4, n = 1:ch.8 to ch.12



10.4.7.4 I²C Timing (SMR:MD[2:0] = 100B)

(T_A: Recommended operating conditions, V_{CC} = 5.0 V +5%/-10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Unit	Remarks
				Min	Max		
SCL clock frequency	f _{SCL}	SCL0, SCL3, SCL4, SCL8 to SCL11	C _L = 50 pF, R = (V _p /I _{OL}) ^{*1}	0	100	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t _{HDSTA}	SDA0, SDA3, SDA4, SDA8 to SDA11 SCL0, SCL3, SCL4, SCL8 to SCL11		4.0	-	μs	
Period of "L" for SCL clock	t _{LOW}	SCL0, SCL3, SCL4, SCL8 to SCL11		4.7	-	μs	
Period of "H" for SCL clock	t _{HIGH}			4.0	-	μs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t _{SUSTA}	SDA0, SDA3, SDA4, SDA8 to SDA11 SCL0, SCL3, SCL4, SCL8 to SCL11		4.7	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}			0	3.45 ^{*2}	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}			250	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t _{SUSTO}			4.0	-	μs	
Bus-free time between "stop" condition and "start" condition	t _{BUF}	-		4.7	-	μs	
Noise filter	t _{SP}	-		t _{NFT} ^{*3}	-	ns	

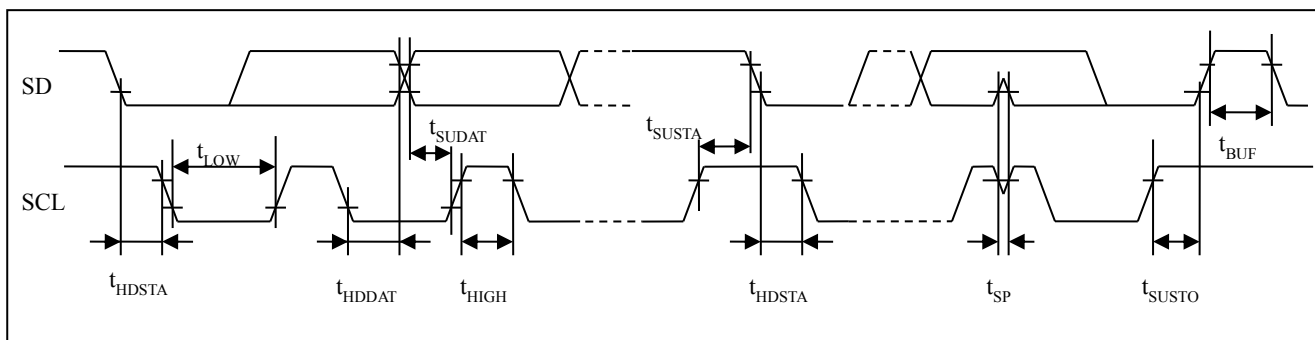
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively V_p shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: t_{NFT} = (NFCR:NFT[4:0]+1) x 2 x tCLK_LCP0A

Notes:

- In this device, Standard mode (Max. 100 kbps) is supported only.
- This model does not support high-speed mode. (Max. 400 kbps).
- This model does not support Min. I_{OL} = 3 mA with V_{OL} = 0.4 V.



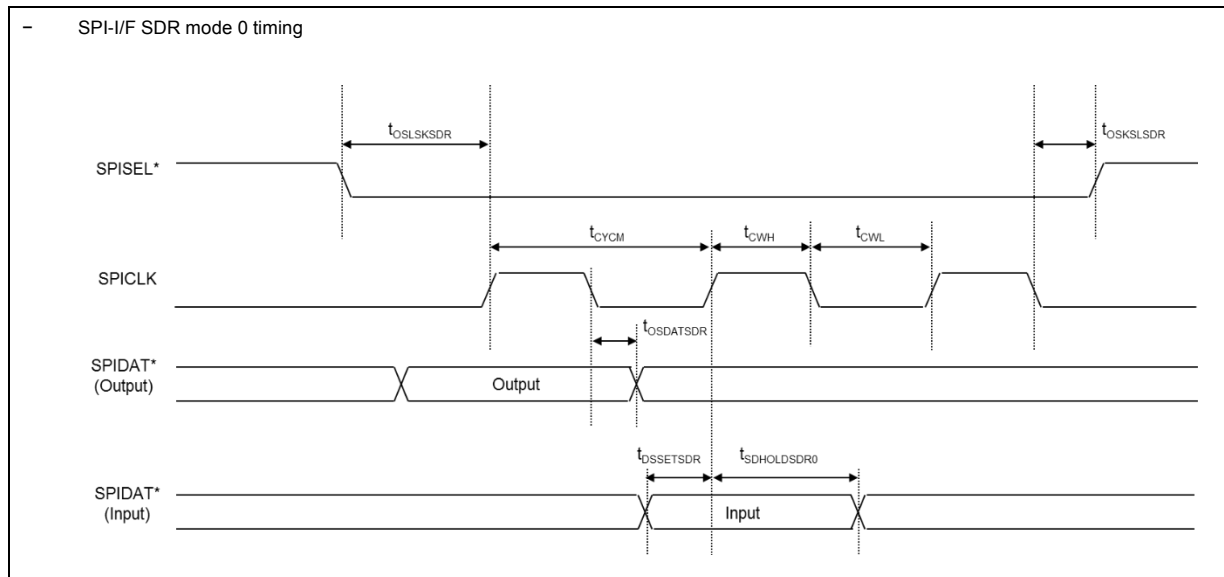
10.4.8 HS-SPI Timing

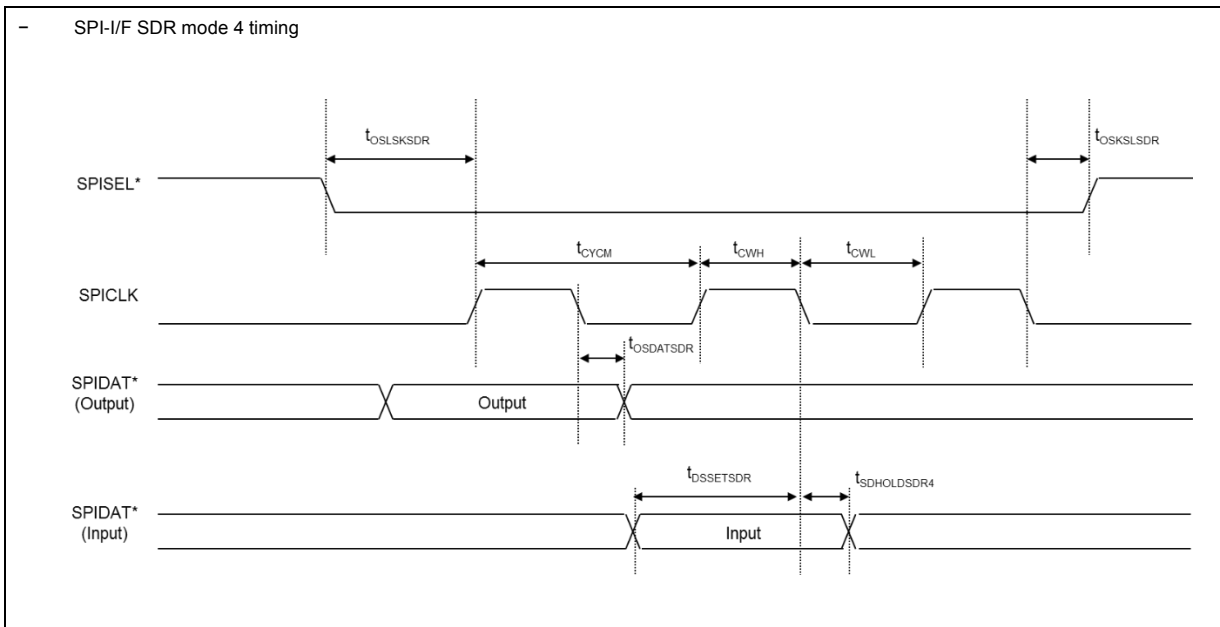
10.4.8.1 SDR Mode Timing

(TA: Recommended operating conditions, Vcc = DVcc = 5.0 V ±10 %, Vss = DVss = AVss = 0.0 V)

(External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t _{CYCM}	SPICLK	2 mA is selected in ODR bit in PPC_PCFGR register.	62.5	-	ns	Slave mode is not supported.
Clock high width	t _{CWH}	SPICLK		0.5t _{CYCM} − 4	-	ns	
Clock low width	t _{CWL}	SPICLK		0.5t _{CYCM} − 4	-	ns	
Valid SPISEL → SPICLK start time (mode0 / mode4)	t _{OSLSKSDR}	SPICLK, SPISEL0 to SPISEL3		1.5t _{CYCM} − 15	-	ns	Minimum setting value of SS2CD bit is 01 _B
SPICLK end → Invalid SPISEL time (mode0 / mode4)	t _{OSKSLSDR}			t _{CYCM} − 10	-	ns	
SPIDAT output time	t _{OSDATSDR}	SPICLK, SPIDAT0 to SPIDAT3		-10	10	ns	
SPIDAT setup	t _{DSSETSDR}	SPICLK, SPIDAT0 to SPIDAT3	14	-	ns		
SPIDAT hold (mode0)	t _{SDHOLDSDR0}		0.5t _{CYCM}	-	ns		
SPIDAT hold (mode4)	t _{SDHOLDSDR4}		0	-	ns		



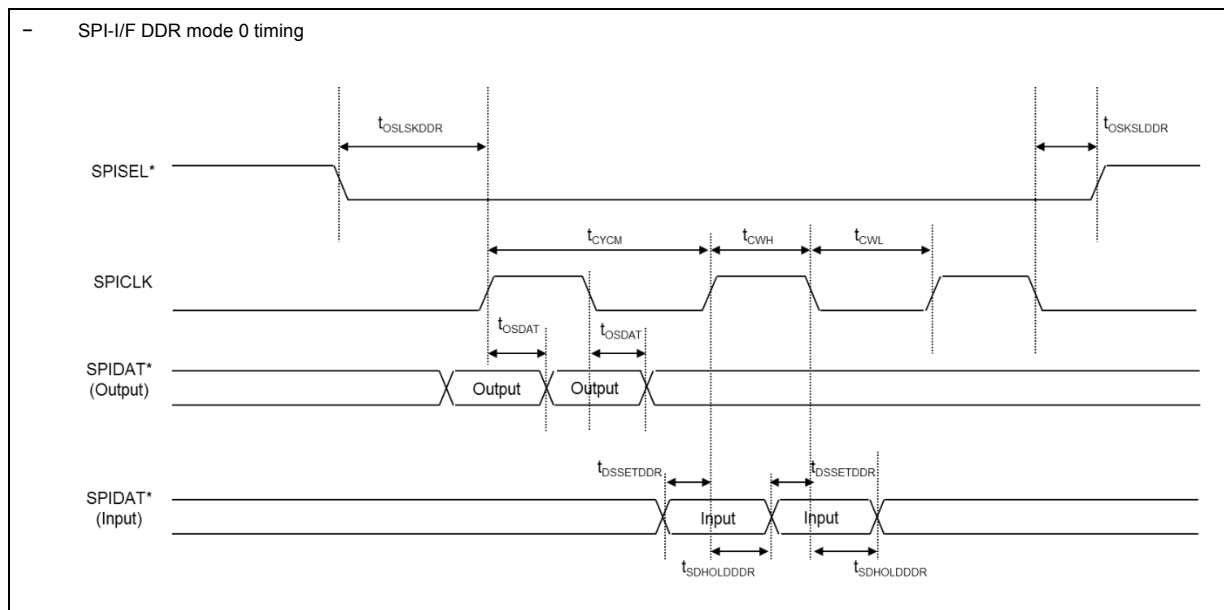


10.4.8.2 DDR Mode Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

(External load capacitance 16 pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t _{CYCM}	SPICLK	2 mA is selected in ODR bit in PPC_PCFGR register.	62.5	-	ns	Slave mode is not supported.
Clock high width	t _{CWH}	SPICLK		0.5t _{CYCM} − 4	-	ns	
Clock low width	t _{CWL}	SPICLK		0.5t _{CYCM} − 4	-	ns	
Valid SPISEL → SPICLK start time (mode0)	t _{OSLSKDDR}	SPICLK, SPISEL0 to SPISEL3		1.75t _{CYCM} − 15	-	ns	Minimum setting value of SS2CD bit is 01 _B
SPICLK end → Invalid SPISEL time (mode0)	t _{OSKSLDDR}			0.75t _{CYCM} − 10	-	ns	
SPIDAT output time	t _{OSDATDDR}	SPICLK, SPIDAT0 to SPIDAT3		0.25t _{CYCM} − 10	0.25t _{CYCM} + 10	ns	
SPIDAT setup	t _{DSSETDDR}	SPICLK, SPIDAT0 to SPIDAT3	14	-	ns		
SPIDAT hold (mode0)	t _{SDHOLDDDR}		"CMOS Schmitt input" and "Disable noise filter" are selected in PPC_PCFGR register.	0	-	ns	

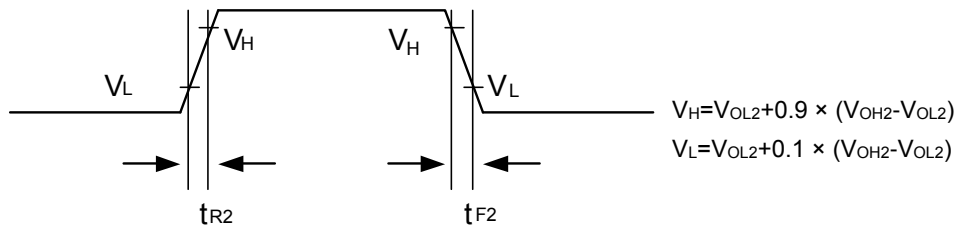


10.4.9 High Current Output Slew Rate

 (T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise / fall time	t _{R2} , t _{F2}	P229 to P231, P300 to P302, P304 to P305, P307 to P309, P312 to P315, P317	-	15	-	100	ns	load capacitance 85 pF

- Slew rate output timing

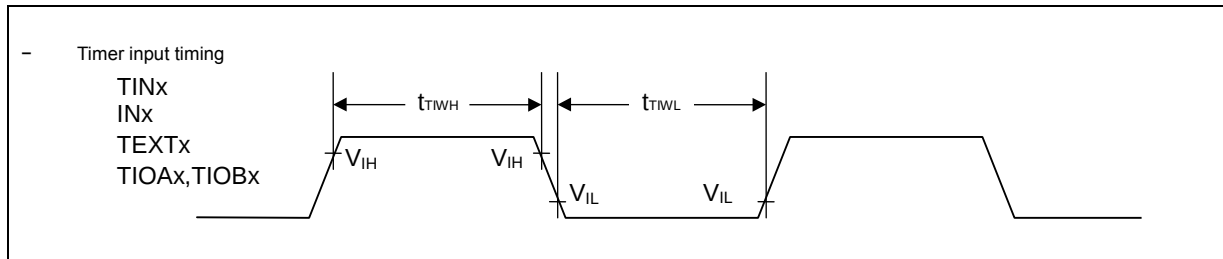


10.5 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TW_H} , t _{TW_L}	TIN0 to TIN3, TIN16 to TIN19	-	4t _{CLK_LCPnA} *	-	ns	4t _{CLK_LCPnA} * ≥100 ns
				100			4t _{CLK_LCPnA} * <100 ns
		TIN32 to TIN33	-	4t _{CLK_LLPM2}	-	ns	4t _{CLK_LLPM2} ≥100 ns
				100			4t _{CLK_LLPM2} <100 ns
		IN0 to IN11	-	4t _{CLK_LCP0A}	-	ns	4t _{CLK_LCP0A} ≥100 ns
				100			4t _{CLK_LCP0A} <100 ns
		TEXT0 to 5	-	4t _{CLK_LCP0A}	-	ns	4t _{CLK_LCP0A} ≥100 ns
				100			4t _{CLK_LCP0A} <100 ns
		TIOA0 to TIOA29 TIOB0 to TIOB29	-	4t _{CLK_LCP0A}	-	ns	4t _{CLK_LCP0A} ≥100 ns
				100			4t _{CLK_LCP0A} <100 ns

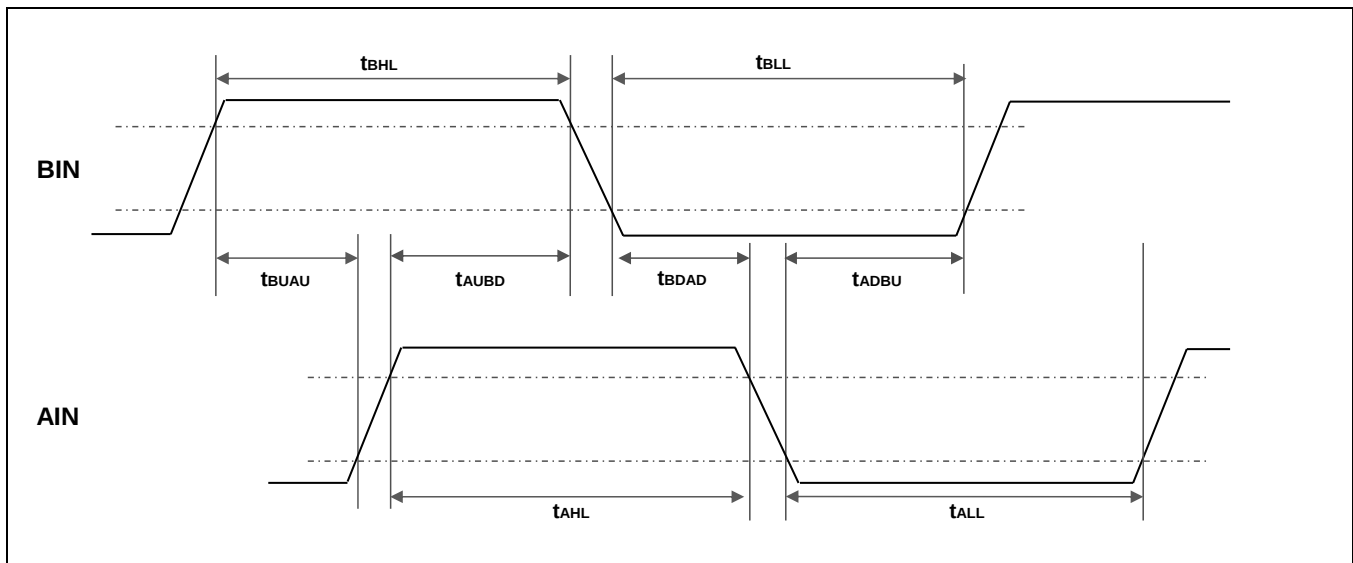
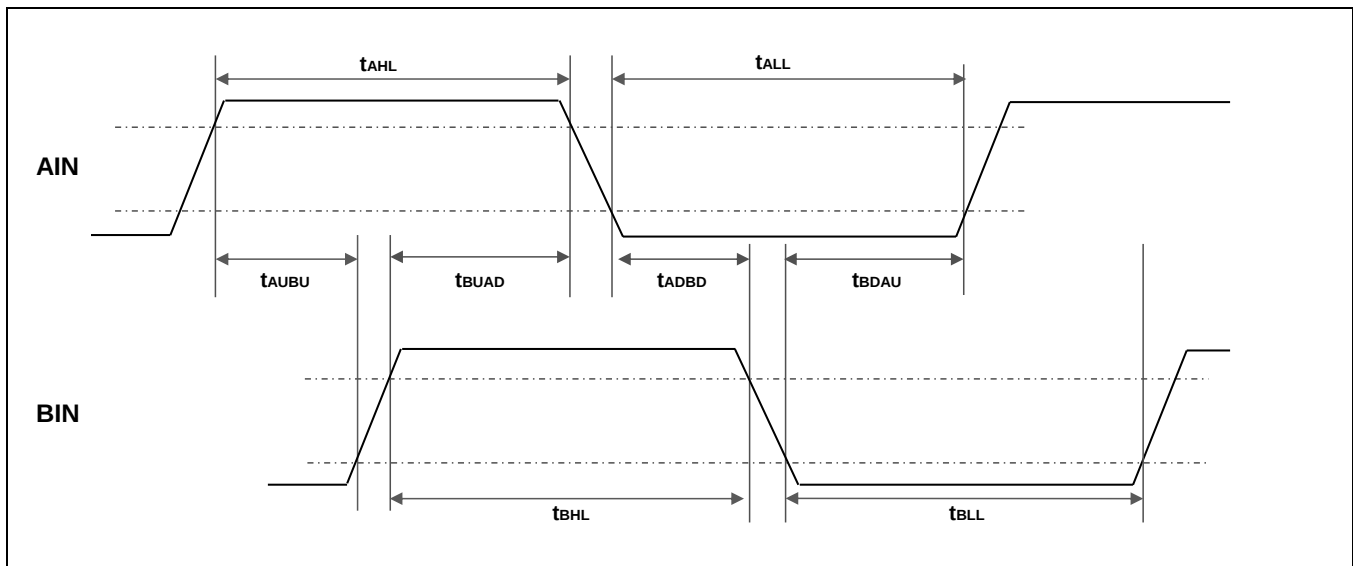
*: n = 0:ch.0 to ch.3, n = 1:ch.16 to ch.19

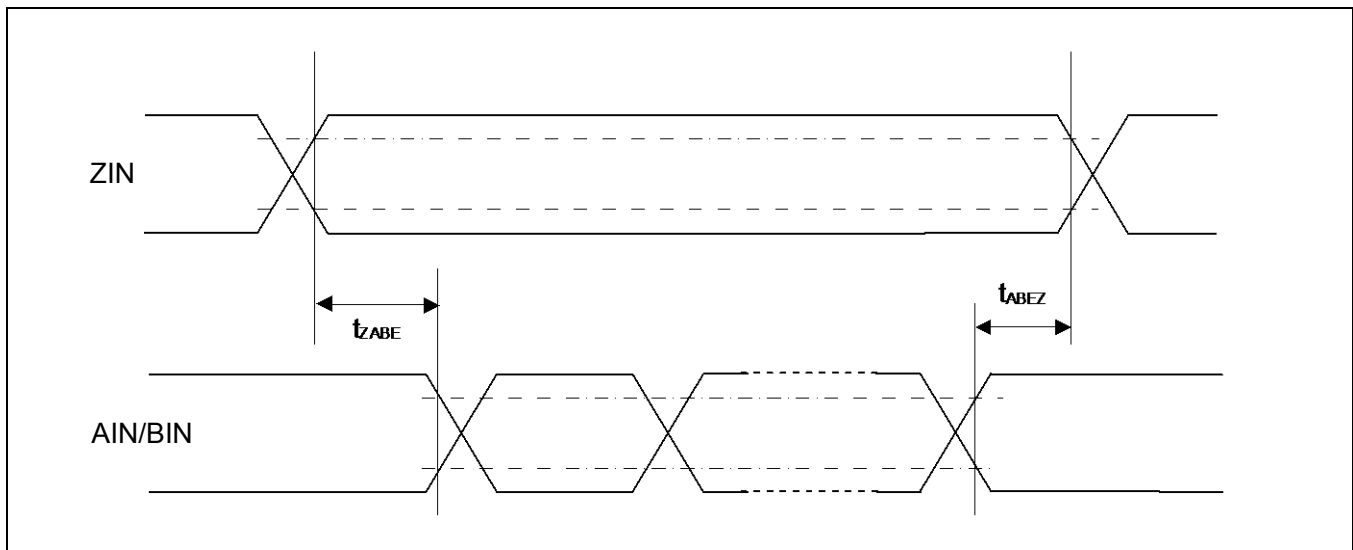
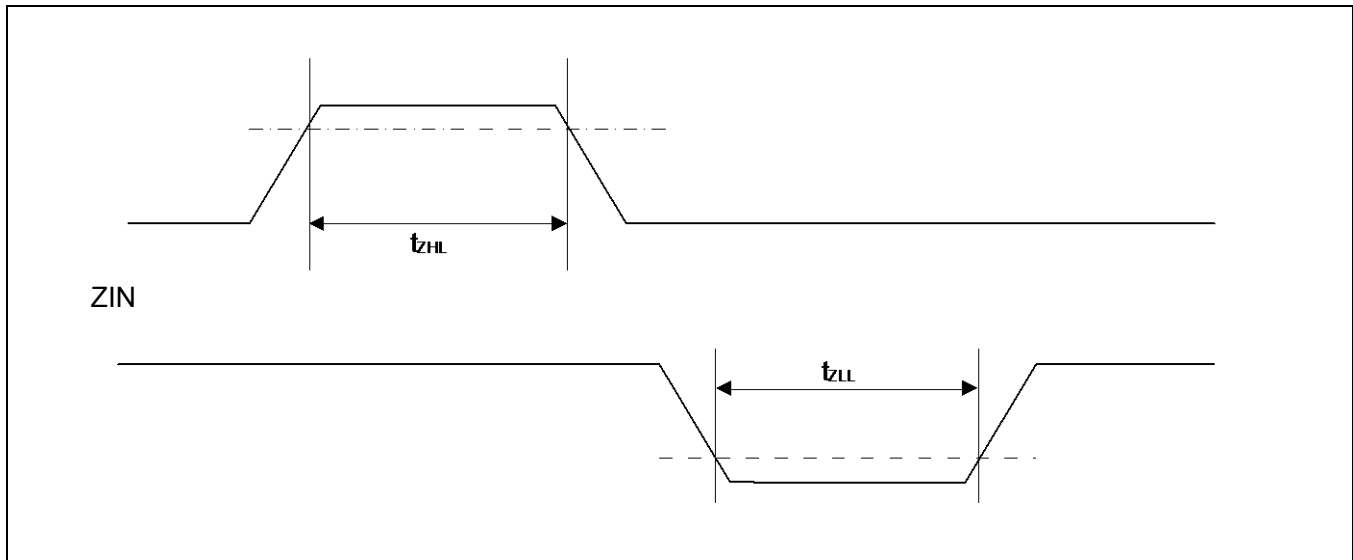


10.6 QPRC Timing

(T_A: Recommended operating conditions, V_{cc} = DV_{cc} = 5.0 V ±10 %, V_{ss} = DV_{ss} = AV_{ss} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
AIN pin "H" width	t _{AHL}	AIN8 to AIN9	-	4t _{CLK_LCP1A}	-	ns	4t _{CLK_LCP1A} ≥ 100 ns
AIN pin "L" width	t _{ALL}	AIN8 to AIN9	-				
BIN pin "H" width	t _{BHL}	BIN8 to BIN9	-				
BIN pin "L" width	t _{BLL}	BIN8 to BIN9	-				
Time from AIN pin "H" level to BIN rise	t _{AUBU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "H" level to AIN fall	t _{BUAD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "L" level to BIN fall	t _{ADBD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "L" level to AIN rise	t _{BDAU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "H" level to AIN rise	t _{BUAU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "H" level to BIN fall	t _{AUBD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from BIN pin "L" level to AIN fall	t _{BDAD}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
Time from AIN pin "L" level to BIN rise	t _{ADBU}	AIN8 to AIN9, BIN8 to BIN9	PC_Mode2 or PC_Mode3				
ZIN pin "H" width	t _{ZHL}	ZIN8 to ZIN9	QCR:CGSC = "0"				
ZIN pin "L" width	t _{ZLL}	ZIN8 to ZIN9	QCR:CGSC = "0"				
Time from determined ZIN level to AIN/BIN rise and fall	t _{ZABE}	AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9	QCR:CGSC = "1"				
Time from AIN/BIN rise and fall time to determined ZIN level	t _{ABEZ}	AIN8 to AIN9, BIN8 to BIN9, ZIN8 to ZIN9	QCR:CGSC = "1"				

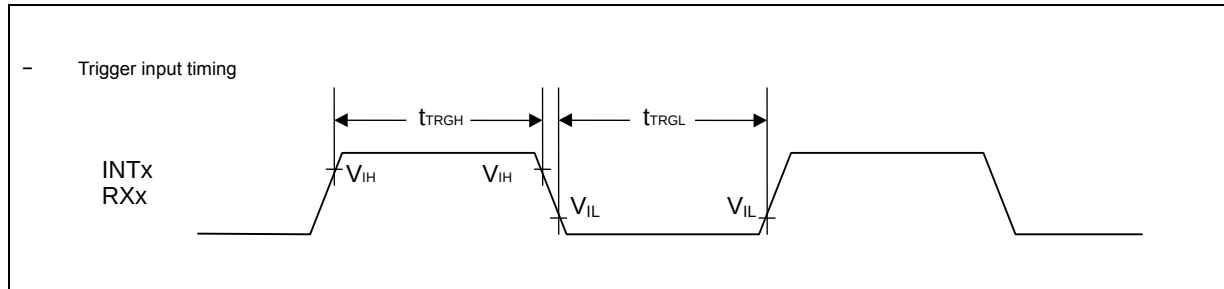




10.7 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

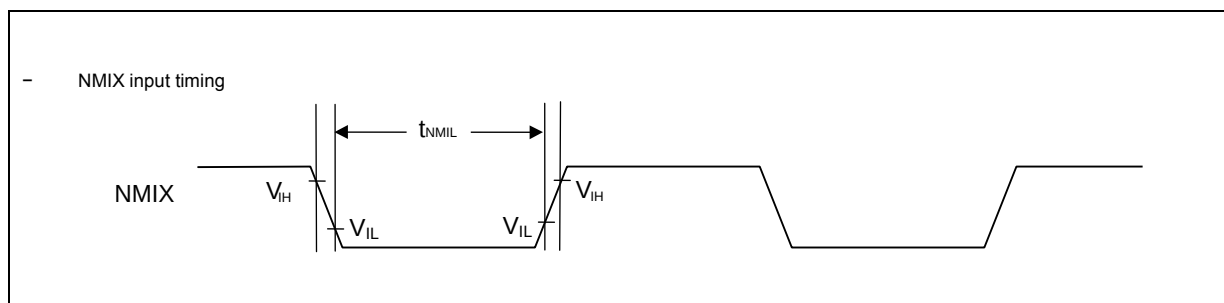
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH}	INT0 to INT15	-	100	-	ns	
	t _{TRGL}	INT0 to INT15	-	1	-	µs	Stop mode



10.8 NMI Input Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{NMIL}	NMIX	-	300	-	ns	



10.9 Low-Voltage Detection (External Low-Voltage Detection)

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{DP5}	VCC	-	3.5	-	5.5	V	
Detection voltage	V _{DL0}	VCC	*1 *3	3.6	3.8	4.0	V	When power-supply voltage falls and detection level is set initially
	V _{DL1}	VCC	*1 *4	3.8	4.0	4.2	V	
	V _{DL2}	VCC	*1 *5	4	4.2	4.4	V	
Hysteresis width	V _{HYS}	VCC	-	-	100	-	mV	When power-supply voltage rises
Low-voltage detection time	T _d	-	-	-	-	30	μs	
Power supply voltage regulation	-	VCC	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_d), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage (V_{DL})

*3: SYSC0_RUNLVDCFGR.LVDH1V = 0100_B or SYSC0_PSSLVDCFGR.LVDH1V = 0100_B

*4: SYSC0_RUNLVDCFGR.LVDH1V = 0101_B or SYSC0_PSSLVDCFGR.LVDH1V = 0101_B

*5: SYSC0_RUNLVDCFGR.LVDH1V = 0110_B or SYSC0_PSSLVDCFGR.LVDH1V = 0110_B

10.10 Low-Voltage Detection (RAM Retention Low-Voltage Detection)

(T_A: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{RDP5}	-	-	0.6	-	1.4	V	
Detection voltage*	V _{RDL}	-	*1	0.9	0.95	1.0	V	When power-supply voltage falls
Hysteresis width	V _{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises
Low-voltage detection time	T _{Rd}	-	-	-	-	30	μs	

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

10.11 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection)

 (TA: Recommended operating conditions, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks	Guaranteed MCU operation range
				Min	Typ	Max			
Power supply voltage range	V _{RDP5}	-	-	0.6	-	1.4	V		No
Detection voltage*	V _{RDL0}	-	*1 *2 *4	0.92	0.97	1.02	V	When power-supply voltage falls	
	V _{RDL1}	-	*1 *3 *4	1.02	1.07	1.12	V		
Hysteresis width	V _{RHYS}	-	-	-	75	-	mV	When power-supply voltage rises	
Low-voltage detection time	T _{Rd}	-	-	-	-	30	μs		

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: SYSC0_RUNLVDCFGR.LVDL1V = 10_B or SYSC0_PSSLVDCFGR.LVDL1V = 10_B

*3: SYSC0_RUNLVDCFGR.LVDL1V = 11_B or SYSC0_PSSLVDCFGR.LVDL1V = 11_B

*4: These detection voltage level settings are below the minimum operation voltage.

Between these detection voltages and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.

Note that although the detection level is below the minimum operation voltage, the LVD reset factor flag is set as the voltage drops below the detection level.

10.12 A/D Converter

10.12.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = DV_{CC} = 5.0 V ±10 %, V_{SS} = DV_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total Error	-	-	-	-	±12	LSB	*3
Integral Nonlinearity	-	-	-	-	±4.0	LSB	*4
Differential Nonlinearity	-	-	-	-	±1.9	LSB	*4
Zero transition voltage	V _{ZT}	*6	AVRL -11.5LSB	-	AVRL +12.5LSB	V	*5
Full-scale transition voltage	V _{FST}	*6	AVRH -13.5LSB	-	AVRH +10.5LSB	V	
Sampling time	t _{SMP}	-	0.3	-	12	μs	*1
Compare time	t _{COMP}	-	0.7	-	28	μs	*1
A/D conversion time	t _{CONV}	-	1.0	-	40	μs	*1
Analog port input current	I _{AIN}	*7	-1.0	-	1.0	μA	V _{AVSS} ≤ V _{AIN} ≤ V _{AVCC}
		*8	-2.0	-	2.0		
		*9	-3.0	-	3.0		
Analog input voltage	V _{AIN}	*6	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH0,AVRH1	4.5	-	5.5	V	AV _{CC} ≥ AVRH
	AVRL	AVRL0/AVSS0, AVRL1/AVSS1	-	0.0	-	V	
Power supply current	I _A	AVCC	-	500	900	μA	per one unit
	I _{AH}		-	1.0	100	μA	*2
	I _R	AVRH	-	1	2	mA	per one unit
	I _{RH}		-	-	5.0	μA	*2
Variation between channels	-	*10	-	-	4	LSB	
		AN32 to AN43, AN46 to AN53, AN55 to AN62	-	-	4	LSB	

*1: Time for each channel

*2: The power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if the A/D converter is not operating and CPU is stopped.

*3: Total Error is a comprehensive static error that includes the linearity. 1LSB = (AVRH-AVRL)/4096

*4: 1LSB = (V_{FST}-V_{ZT})/4094

*5: 1LSB = (AVRH-AVRL)/4096

*6: AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, AN27 to AN43, AN46 to AN53, and AN55 to AN62

*7: AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN42

*8: AN0 to AN2, and AN43

*9: AN44 to AN62

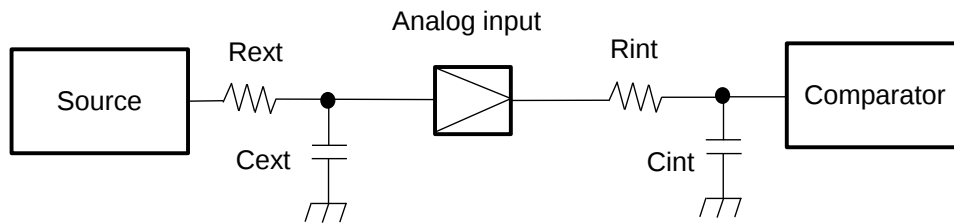
*10: AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN31

10.12.2 Notes on Using A/D converters

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 μF) to an analog input pin.

Analog input circuit model



- R_{int} : Analog input impedance
3.9 kilohms (max) ($4.5\text{ V} \leq AV_{cc} \leq 5.5\text{ V}$)
- C_{int} : Capacitance of MCU input pin
11.0pF (max) ($4.5\text{ V} \leq AV_{cc} \leq 5.5\text{ V}$)
- R_{ext} : External driving impedance
- C_{ext} : Capacitance of PCB at A/D converter input

The following approximation formula for the replacement model above can be used:
sampling time (minimum) = $9 \times (R_{in} + R_{ext}) \times C_{in} + R_{ext} \times C_{ext}$

Note: Listed values must be considered as reference values.

10.12.3 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter

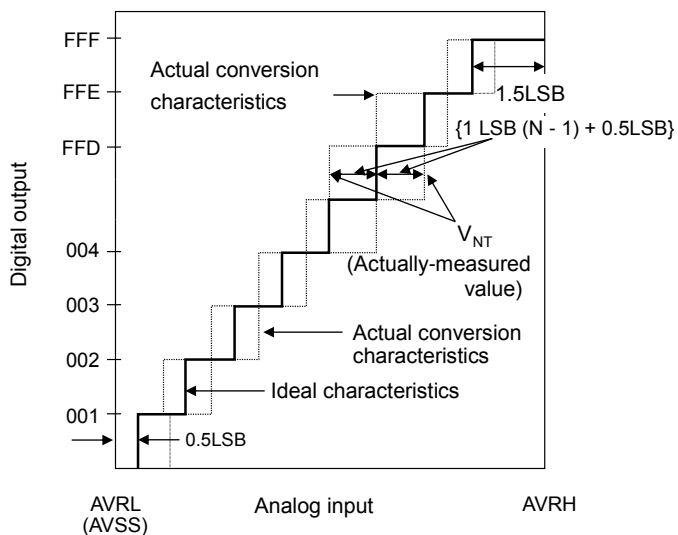
Integral Nonlinearity error *: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non-linearity error.

Differential Nonlinearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB

Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.

*: Represented as "Linearity error" in the former product series.

Total error



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N-1) + 0.5\text{LSB}\}}{1\text{LSB}} \quad [\text{LSB}]$$

$$1\text{LSB}(\text{Ideal value}) = \frac{\text{AVRH} - \text{AVRL}}{4096} \quad [\text{V}]$$

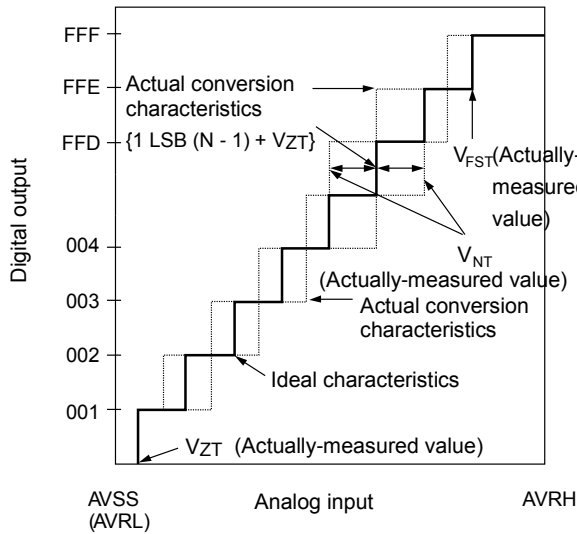
N: A/D converter digital output value.

$V_{ZT}(\text{Ideal value}) = \text{AVRL} + 0.5\text{LSB}[\text{V}]$

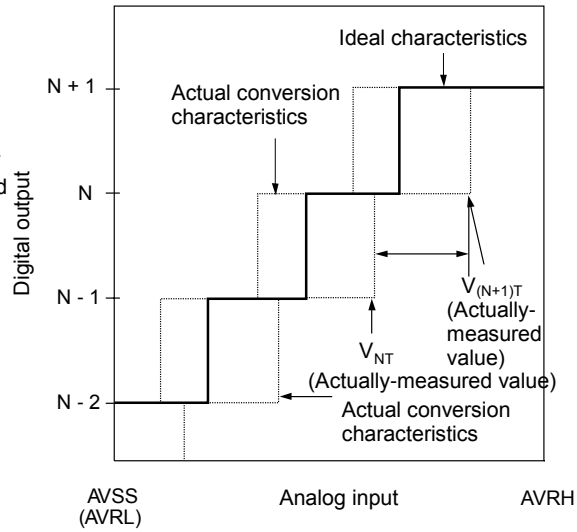
$V_{FST}(\text{Ideal value}) = \text{AVRH} - 1.5\text{LSB}[\text{V}]$

V_{NT} : Voltage at which the digital output changes from "(N - 1)" to "N".

Integral Nonlinearity



Differential Nonlinearity



$$\text{Integral Nonlinearity of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N-1) + V_{ZT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential Nonlinearity of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} \quad -1 \text{ LSB } [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{ZT}}{4094} \quad [\text{V}]$$

V_{ZT} : Voltage for which digital output changes from "0x000" to "0x001"

V_{FST} : Voltage for which digital output changes from "0xFFE" to "0xFFF".

10.13 Flash Memory

Parameter	Rating			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	300	1100	ms	8-KB sector* ¹ Internal preprogramming time included
	-	800	3700	ms	64-KB sector* ¹ Internal preprogramming time included
8-bit write time	-	15	288	μs	System-level overhead time excluded* ¹
16-bit write time	-	19	384	μs	System-level overhead time excluded* ¹
32-bit write time	-	27	567	μs	System-level overhead time excluded* ¹
64-bit write time	-	45	945	μs	System-level overhead time excluded* ¹
8-bit (with ECC) write time	-	19	384	μs	System-level overhead time excluded* ¹
16-bit (with ECC) write time	-	23	483	μs	System-level overhead time excluded* ¹
32-bit (with ECC) write time	-	31	651	μs	System-level overhead time excluded* ¹
64-bit (with ECC) write time	-	49	1029	μs	System-level overhead time excluded* ¹
Erase count* ² / Data retention time	1,000/20 years, 10,000/10 years, 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T _A = +85 degrees Celsius

*1: Guaranteed value for up to 100,000 erases

*2: Number of erases for each sector

Notes:

- While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.
- In the application system where V_{CC} might be shut down while writing or erasing, be sure to turn the power off by using an external low-voltage detection function.
- To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC} at 2.7 V or more within the duration calculated by the following expression:

$$T_d^{*1} [\mu s] + (1 / F_{CRF}^{*2} [MHz]) \times 1029 + 25 [\mu s]$$

*1 : See "12.8 Low-voltage detection (external low-voltage detection)"

*2 : See "12.4.1 Source clock timing"

11. Ordering Information

Part Number	Package
S6J3129HACSE20000	144-pin Plastic, TEQFP(LEU144)
S6J3129HBCSE2000A	
S6J312AHACSE2000A	

Note:

– S6J312xHzCSEy0000*

"x"/"y" is an part number option. For the part number option, see the following table.
 For details on each package, see "PACKAGE DIMENSIONS."

* z: A/B

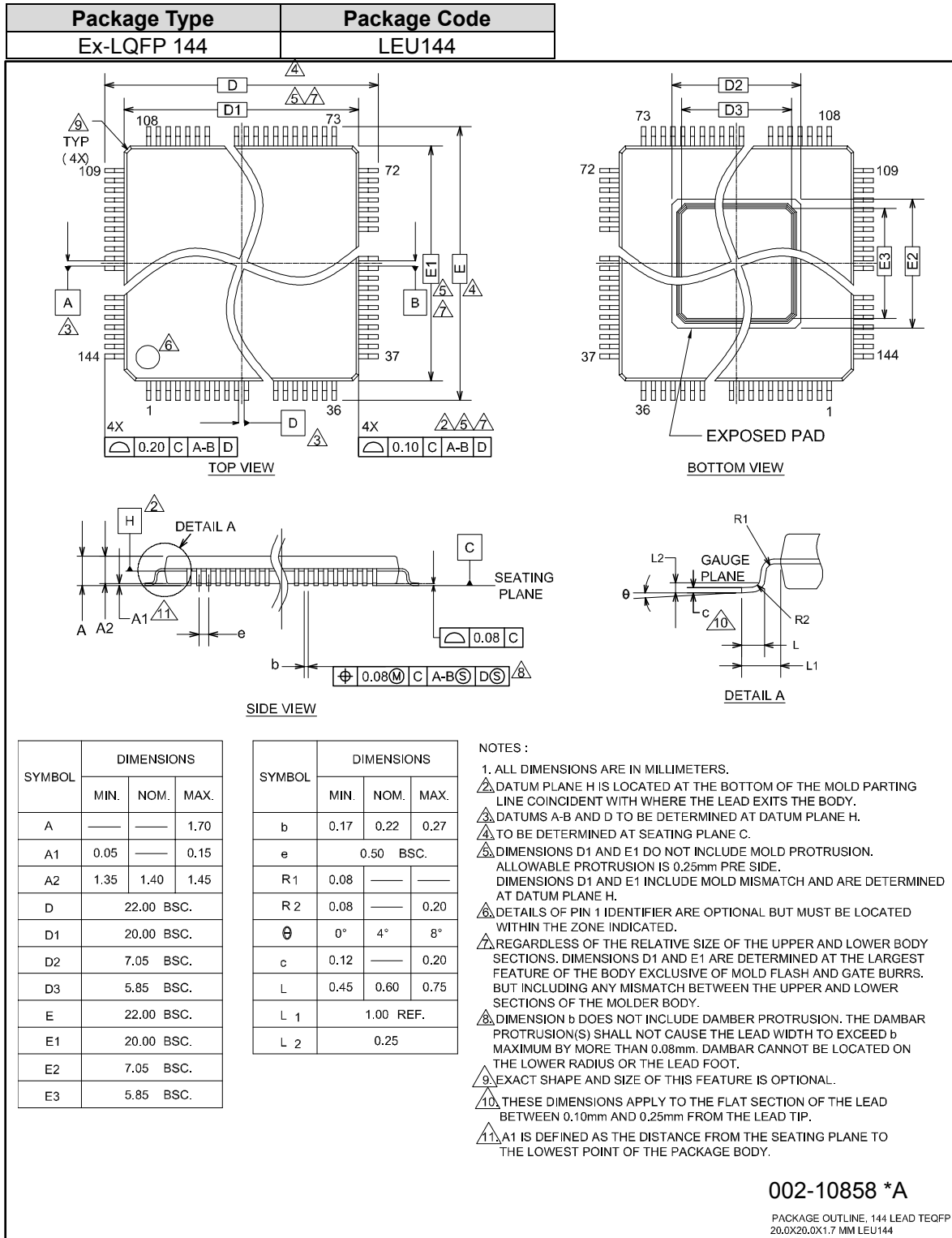
12. Part Number Option

Part Number Option "x"	FLASH Memory
A	1 MByte
9	768 KByte

Part Number Option "y"	
2	PureSn & Halogen Free

Part Number Option "z"	SHE
A	SHE ON
B	SHE OFF

13. Package Dimensions



14. Errata

This section describes the errata for the S6J3120 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
S6J3129HACSE20000
S6J3129HBCSE2000A
S6J312AHACSE2000A

S6J3120 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3120 Series devices.

Items	Part Number	Fix Status
MCAN wrong message transmission	S6J3129HACSE20000	Not be planned.
	S6J3129HBCSE2000A	
	S6J312AHACSE2000A	

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control field information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

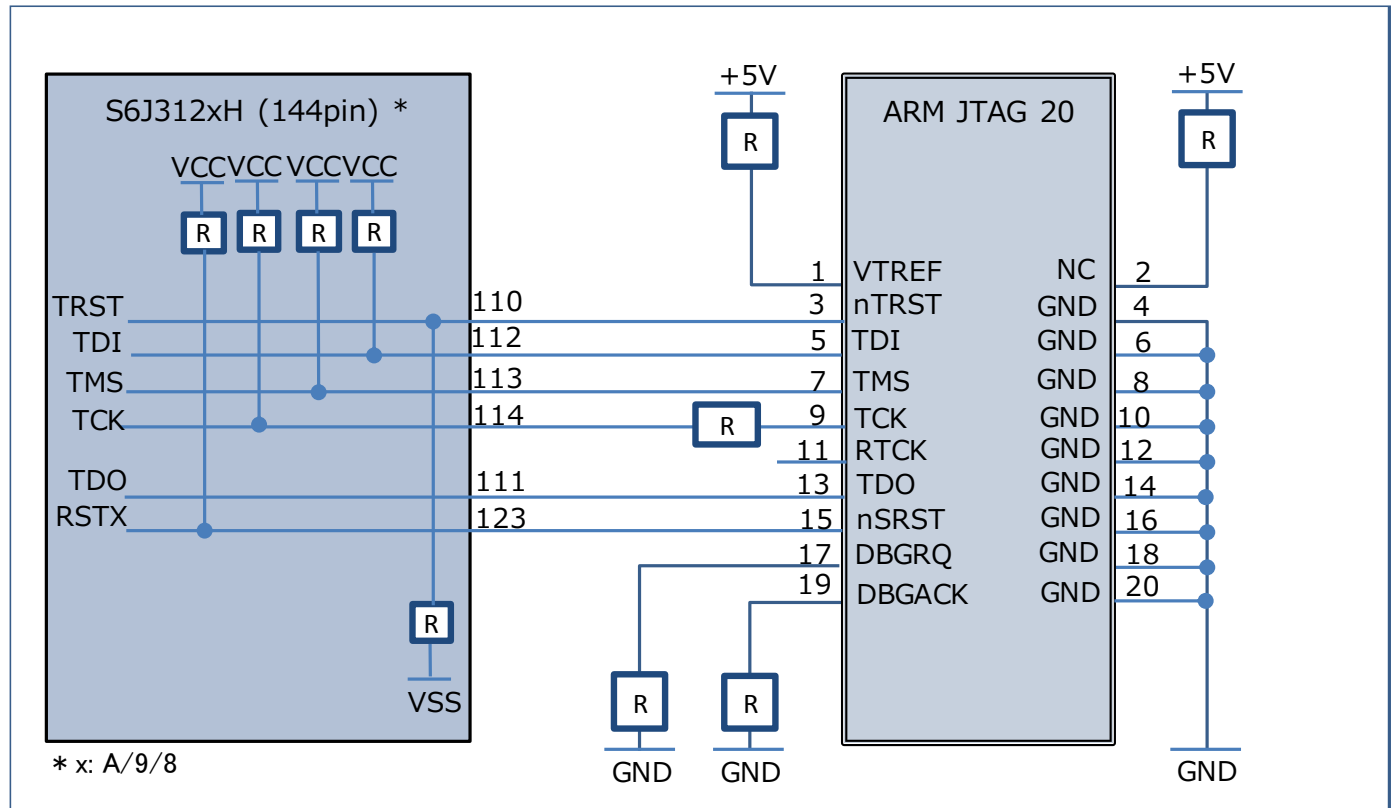
■ Fix Status

Not be planned

15. Appendix

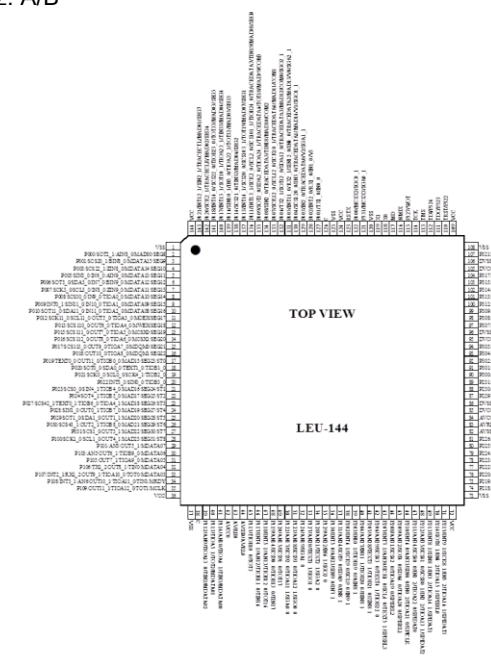
15.1 Application 1: JTAG tool connection

This is an application example of JTAG tool connection.



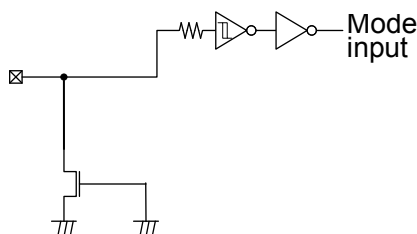
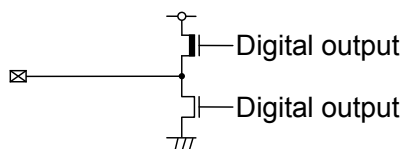
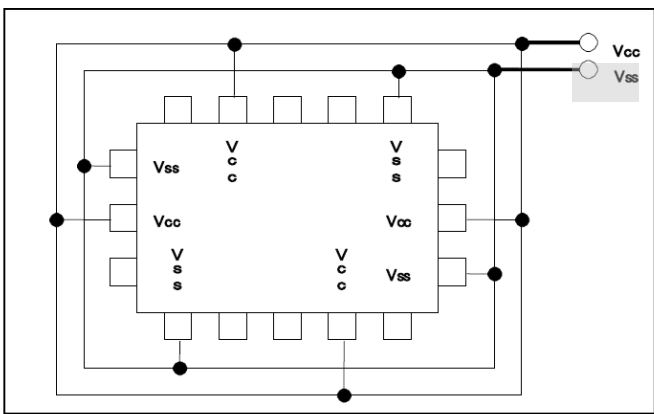
16. Major Changes

Page	Section	Change Results
Revision *A		
1	Features Cortex-R5 Core	Revised the following note. (Error) □ ECC support for the TCM ports (Correct) □ ECC support for the TCM ports for RAM
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows. (Correct) ■ Built-in Flash memory size □ Program: 1024 K + 64 KB (S6J312AHzB*)/768 K + 64 KB (S6J3129HzB*)/512 K + 64 KB (S6J3128HzB*) □ *z: A/B □ Work: 112 KB (S6J312AHzB*)/ 112 KB (S6J3129HzB*)/112 KB (S6J3128HzB*) □ *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows. (Correct) ■ Built-in RAM size □ TCRAM 64 KB(S6J312AHzB*)/ 48 KB(S6J3129HzB*)/32 KB(S6J3128HzB*) □ System SRAM 16 KB (S6J312AHzB*)/ 16 KB (S6J3129HzB*)/ 16 KB (S6J3128HzB*) □ Backup RAM 8 KB (S6J312AHzB*)/ 8 KB (S6J3129HzB*)/8 KB (S6J3128HzB*) □ *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows. (Correct) ■ General-purpose ports: 112 channels (S6J312AHzB*)/ 112 channels (S6J3129HzB*)/ 112 channels (S6J3128HzB*) □ *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows. (Correct) ■ A/D converter (successive approximation type) □ 12-bit resolution, 2 units mounted: Max 50 channels (22 channels + 28 channels)(S6J312AHzB*)/ Max 50 channels (22 channels + 28 channels)(S6J3129HzB*)/ Max 50 channels (22 channels + 28 channels)(S6J3128HzB*) □ *z: A/B
1	Features Peripheral Functions	Revised the full production and SHE-OFF series as follows. (Correct) ■ Multi-function serial (transmission and reception FIFOs mounted) :Max 10 channels(S6J312AHzB*)/ Max 10 channels(S6J3129HzB*)/ Max 10 channels(S6J3128HzB*) □ *z: A/B
1	Features Peripheral Functions	Added the following function lists. <I ² C> □ Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO □ Standard mode (Max. 100kbps) is supported only. □ DMA transfer is supported.
2	Features Peripheral Functions	Revised the following function list. (Error) □ CAN transfer speed :1Mbps (Correct) □ CAN transfer speed :5Mbps

Page	Section	Change Results
2	Features Peripheral Functions	Added the following function list under CAN controller. □ 32 message buffer/channel (transmission message buffer size)
2	Features Peripheral Functions	Added the following function list under Low-power consumption. □ Partial wakeup function
2	Features Peripheral Functions	Revised the follows as full production. (Correct) ■ Package: LEU144 (S6J312xHzB*) □ *x: A/9/8, z: A/B
6	1. Product Lineup	Added "Table 3-1 Memory Size" as full production.
6	1. Product Lineup	Added "Table 3-2 SHE Option" as full production.
6	1. Product Lineup	Added full production and notes as follows. *1: x: A/9/8, z: A/B *2: I ² C-UART function is not supported at Multi-function serial ch.1, ch.2, and ch.12.
6	1. Product Lineup	Revised the following frequency. (Correct) Maximum CPU operating frequency : 128 MHz
7	1. Product Lineup	Added the following function list under Low-power consumption. – Partial wakeup function
8	2. Pin Assignment	Revised "Figure 4-1 Pin Assignment for S6J312xHzB*" as follows. (Correct) * x: A/9/8, z: A/B 
9	3. Pin Description	Revised the tables as follows for full production. (Correct) Table 5-1 S6J312xHzB* Pin Functions * x: A/9/8, z: A/B

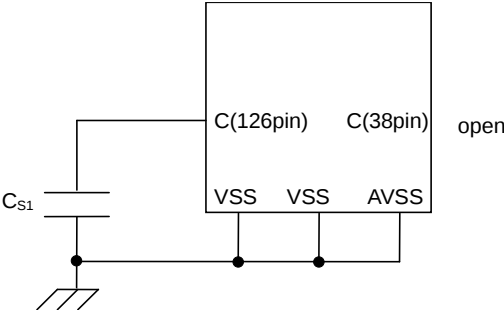
Page	Section	Change Results																																																	
10,11,12,15, 16,17,18, 20,21,24	3. Pin Description	Revised the “I/O pin” to ”output pin” as follows (Correct) Pin 13 Multi-function serial ch.11 serial chip select 1 output pin (0) Pin14 Multi-function serial ch.11 serial chip select 2 output pin (0) Pin 15 Multi-function serial ch.11 serial chip select 3 output pin (0) Pin 23 Multi-function serial ch.4 serial chip select 2 output pin (1) Pin 26 Multi-function serial ch.4 serial chip select 3 output pin (1) Pin 49 Multi-function serial ch.9 serial chip select 1 output pin (0) Pin 50 Multi-function serial ch.9 serial chip select 2 output pin (0) Pin 51 Multi-function serial ch.9 serial chip select 3 output pin (0) Pin 62 Multi-function serial ch.4 serial chip select 3 output pin (0) Pin 64 Multi-function serial ch.4 serial chip select 2 output pin (0) Pin 68 Multi-function serial ch.4 serial chip select 1 output pin (0) Pin 76 Multi-function serial ch.8 serial chip select 3 output pin (0) Pin 78 Multi-function serial ch.8 serial chip select 1 output pin (0) Pin 97 Multi-function serial ch.10 serial chip select 2 output pin (0) Pin 100 Multi-function serial ch.10 serial chip select 1 output pin (0) Pin 136 Multi-function serial ch.10 serial chip select 1 output pin (1) Pin 137 Multi-function serial ch.10 serial chip select 3 output pin (1)																																																	
19	3. Pin Description	Deleted Pin87 RX0_1 from “Table 5-1 S6J312xHzB* Pin Functions” (Error) <table><tr><td rowspan="8">87</td><td>P229</td><td>-</td><td rowspan="8">M</td><td>General-purpose I/O port</td></tr><tr><td>INT8_0</td><td>-</td><td>INT8 external interrupt input pin (0)</td></tr><tr><td>AN46</td><td>-</td><td>ADC analog 46 input pin</td></tr><tr><td>PWU_AN6</td><td>-</td><td>Partial wakeup ADC analog 6 input pin</td></tr><tr><td>RX0_1</td><td>-</td><td>CAN reception data 0 input pin (1)</td></tr><tr><td>OUT0_0</td><td>-</td><td>Output compare ch.0 output pin (0)</td></tr><tr><td>TIOA25_0</td><td>-</td><td>Base timer ch.25 TIOA I/O pin (0)</td></tr><tr><td>PWM1P0</td><td>-</td><td>SMC ch.0 (P1) output pin</td></tr></table> (Correct) <table><tr><td rowspan="8">87</td><td>P229</td><td>-</td><td rowspan="8">M</td><td>General-purpose I/O port</td></tr><tr><td>INT8_0</td><td>-</td><td>INT8 external interrupt input pin (0)</td></tr><tr><td>AN46</td><td>-</td><td>ADC analog 46 input pin</td></tr><tr><td>PWU_AN6</td><td>-</td><td>Partial wakeup ADC analog 6 input pin</td></tr><tr><td>OUT0_0</td><td>-</td><td>Output compare ch.0 output pin (0)</td></tr><tr><td>TIOA25_0</td><td>-</td><td>Base timer ch.25 TIOA I/O pin (0)</td></tr><tr><td>PWM1P0</td><td>-</td><td>SMC ch.0 (P1) output pin</td></tr></table>	87	P229	-	M	General-purpose I/O port	INT8_0	-	INT8 external interrupt input pin (0)	AN46	-	ADC analog 46 input pin	PWU_AN6	-	Partial wakeup ADC analog 6 input pin	RX0_1	-	CAN reception data 0 input pin (1)	OUT0_0	-	Output compare ch.0 output pin (0)	TIOA25_0	-	Base timer ch.25 TIOA I/O pin (0)	PWM1P0	-	SMC ch.0 (P1) output pin	87	P229	-	M	General-purpose I/O port	INT8_0	-	INT8 external interrupt input pin (0)	AN46	-	ADC analog 46 input pin	PWU_AN6	-	Partial wakeup ADC analog 6 input pin	OUT0_0	-	Output compare ch.0 output pin (0)	TIOA25_0	-	Base timer ch.25 TIOA I/O pin (0)	PWM1P0	-	SMC ch.0 (P1) output pin
87	P229	-		M	General-purpose I/O port																																														
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	RX0_1	-			CAN reception data 0 input pin (1)																																														
	OUT0_0	-			Output compare ch.0 output pin (0)																																														
	TIOA25_0	-			Base timer ch.25 TIOA I/O pin (0)																																														
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87	P229	-	M	General-purpose I/O port																																															
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	TIOA25_0	-		Base timer ch.25 TIOA I/O pin (0)																																															
	PWM1P0	-		SMC ch.0 (P1) output pin																																															

Page	Section	Change Results																																										
20	3. Pin Description	Deleted Pin97 RX0_0 from “Table 5-1 S6J312xHzB* Pin Functions” (Error) <table><tr><td rowspan="7">97</td><td>P307</td><td>-</td><td rowspan="7">M</td><td>General-purpose I/O port</td></tr><tr><td>INT1_0</td><td>-</td><td>INT1 external interrupt input pin (0)</td></tr><tr><td>AN55</td><td>-</td><td>ADC analog 55 input pin</td></tr><tr><td>RX0_0</td><td>-</td><td>CAN reception data 0 input pin (0)</td></tr><tr><td>SCS102_0</td><td>-</td><td>Multi-function serial ch.10 serial chip select</td></tr><tr><td>TIOB18_0</td><td>-</td><td>2 I/O pin (0)</td></tr><tr><td>PWM1P2</td><td>-</td><td>Base timer ch.18 TIOB input pin (0)</td></tr><tr><td colspan="5">SMC ch.2 (P1) output pin</td></tr></table>	97	P307	-	M	General-purpose I/O port	INT1_0	-	INT1 external interrupt input pin (0)	AN55	-	ADC analog 55 input pin	RX0_0	-	CAN reception data 0 input pin (0)	SCS102_0	-	Multi-function serial ch.10 serial chip select	TIOB18_0	-	2 I/O pin (0)	PWM1P2	-	Base timer ch.18 TIOB input pin (0)	SMC ch.2 (P1) output pin																		
		97		P307	-		M	General-purpose I/O port																																				
INT1_0	-			INT1 external interrupt input pin (0)																																								
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RX0_0	-			CAN reception data 0 input pin (0)																																								
SCS102_0	-			Multi-function serial ch.10 serial chip select																																								
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(Correct) <table><tr><td rowspan="7">97</td><td>P307</td><td>-</td><td rowspan="7">M</td><td>General-purpose I/O port</td></tr><tr><td>INT1_0</td><td>-</td><td>INT1 external interrupt input pin (0)</td></tr><tr><td>AN55</td><td>-</td><td>ADC analog 55 input pin</td></tr><tr><td>SCS102_0</td><td>-</td><td>Multi-function serial ch.10 serial chip select</td></tr><tr><td>TIOB18_0</td><td>-</td><td>2 output pin (0)</td></tr><tr><td>PWM1P2</td><td>-</td><td>Base timer ch.18 TIOB input pin (0)</td></tr><tr><td colspan="5">SMC ch.2 (P1) output pin</td></tr></table>	97	P307	-	M	General-purpose I/O port	INT1_0	-	INT1 external interrupt input pin (0)	AN55	-	ADC analog 55 input pin	SCS102_0	-	Multi-function serial ch.10 serial chip select	TIOB18_0	-	2 output pin (0)	PWM1P2	-	Base timer ch.18 TIOB input pin (0)	SMC ch.2 (P1) output pin																							
97		P307	-		M	General-purpose I/O port																																						
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		PWM1P2	-			Base timer ch.18 TIOB input pin (0)																																						
	SMC ch.2 (P1) output pin																																											
9,10,11,15,16,17,19,21	3. Pin Description	Added the I2C function to Pin 6,7,10,11,18,19,57,58,63,65,80,81,101,102 <table><tr><td>Pin 6</td><td>SDA3_0</td><td>I²C bus ch.3 serial data I/O pin</td></tr><tr><td>Pin 7</td><td>SCL3_0</td><td>I²C bus ch.3 serial clock I/O pin</td></tr><tr><td>Pin 10</td><td>SDA11_0</td><td>I²C bus ch.11 serial data I/O pin</td></tr><tr><td>Pin 11</td><td>SCL11_0</td><td>I²C bus ch.11 serial clock I/O pin</td></tr><tr><td>Pin 18</td><td>SDA0_0</td><td>I²C bus ch.0 serial data I/O pin</td></tr><tr><td>Pin 19</td><td>SCL0_0</td><td>I²C bus ch.0 serial clock I/O pin</td></tr><tr><td>Pin 57</td><td>SDA9_0</td><td>I²C bus ch.9 serial data I/O pin</td></tr><tr><td>Pin 58</td><td>SCL9_0</td><td>I²C bus ch.9 serial clock I/O pin</td></tr><tr><td>Pin 63</td><td>SDA4_0</td><td>I²C bus ch.4 serial data I/O pin</td></tr><tr><td>Pin 65</td><td>SCL4_0</td><td>I²C bus ch.4 serial clock I/O pin</td></tr><tr><td>Pin 80</td><td>SDA8_0</td><td>I²C bus ch.8 serial data I/O pin</td></tr><tr><td>Pin 81</td><td>SCL8_0</td><td>I²C bus ch.8 serial clock I/O pin</td></tr><tr><td>Pin 101</td><td>SDA10_0</td><td>I²C bus ch.10 serial data I/O pin</td></tr><tr><td>Pin 102</td><td>SCL10_0</td><td>I²C bus ch.10 serial clock I/O pin</td></tr></table>	Pin 6	SDA3_0	I ² C bus ch.3 serial data I/O pin	Pin 7	SCL3_0	I ² C bus ch.3 serial clock I/O pin	Pin 10	SDA11_0	I ² C bus ch.11 serial data I/O pin	Pin 11	SCL11_0	I ² C bus ch.11 serial clock I/O pin	Pin 18	SDA0_0	I ² C bus ch.0 serial data I/O pin	Pin 19	SCL0_0	I ² C bus ch.0 serial clock I/O pin	Pin 57	SDA9_0	I ² C bus ch.9 serial data I/O pin	Pin 58	SCL9_0	I ² C bus ch.9 serial clock I/O pin	Pin 63	SDA4_0	I ² C bus ch.4 serial data I/O pin	Pin 65	SCL4_0	I ² C bus ch.4 serial clock I/O pin	Pin 80	SDA8_0	I ² C bus ch.8 serial data I/O pin	Pin 81	SCL8_0	I ² C bus ch.8 serial clock I/O pin	Pin 101	SDA10_0	I ² C bus ch.10 serial data I/O pin	Pin 102	SCL10_0	I ² C bus ch.10 serial clock I/O pin
Pin 6	SDA3_0	I ² C bus ch.3 serial data I/O pin																																										
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Pin 19	SCL0_0	I ² C bus ch.0 serial clock I/O pin																																										
Pin 57	SDA9_0	I ² C bus ch.9 serial data I/O pin																																										
Pin 58	SCL9_0	I ² C bus ch.9 serial clock I/O pin																																										
Pin 63	SDA4_0	I ² C bus ch.4 serial data I/O pin																																										
Pin 65	SCL4_0	I ² C bus ch.4 serial clock I/O pin																																										
Pin 80	SDA8_0	I ² C bus ch.8 serial data I/O pin																																										
Pin 81	SCL8_0	I ² C bus ch.8 serial clock I/O pin																																										
Pin 101	SDA10_0	I ² C bus ch.10 serial data I/O pin																																										
Pin 102	SCL10_0	I ² C bus ch.10 serial clock I/O pin																																										
18,19	3. Pin Description	Added the Partial wakeup ADC analog input to Pin 78,79,80,81,87,88. <table><tr><td>Pin78</td><td>PWU_AN0</td><td>Partial wakeup ADC analog 0 input pin</td></tr><tr><td>Pin79</td><td>PWU_AN1</td><td>Partial wakeup ADC analog 1 input pin</td></tr><tr><td>Pin80</td><td>PWU_AN2</td><td>Partial wakeup ADC analog 2 input pin</td></tr><tr><td>Pin81</td><td>PWU_AN3</td><td>Partial wakeup ADC analog 3 input pin</td></tr><tr><td>Pin87</td><td>PWU_AN6</td><td>Partial wakeup ADC analog 6 input pin</td></tr><tr><td>Pin88</td><td>PWU_AN7</td><td>Partial wakeup ADC analog 7 input pin</td></tr></table>	Pin78	PWU_AN0	Partial wakeup ADC analog 0 input pin	Pin79	PWU_AN1	Partial wakeup ADC analog 1 input pin	Pin80	PWU_AN2	Partial wakeup ADC analog 2 input pin	Pin81	PWU_AN3	Partial wakeup ADC analog 3 input pin	Pin87	PWU_AN6	Partial wakeup ADC analog 6 input pin	Pin88	PWU_AN7	Partial wakeup ADC analog 7 input pin																								
Pin78	PWU_AN0	Partial wakeup ADC analog 0 input pin																																										
Pin79	PWU_AN1	Partial wakeup ADC analog 1 input pin																																										
Pin80	PWU_AN2	Partial wakeup ADC analog 2 input pin																																										
Pin81	PWU_AN3	Partial wakeup ADC analog 3 input pin																																										
Pin87	PWU_AN6	Partial wakeup ADC analog 6 input pin																																										
Pin88	PWU_AN7	Partial wakeup ADC analog 7 input pin																																										
21	3. Pin Description	Added the Partial wakeup trigger output to Pin 107. <table><tr><td>Pin107</td><td>PWUTRG</td><td>Partial wakeup trigger output pin</td></tr></table>	Pin107	PWUTRG	Partial wakeup trigger output pin																																							
Pin107	PWUTRG	Partial wakeup trigger output pin																																										
19, 20, 23	3. Pin Description	Deleted the following function on each pins. <table><tr><td>Pin 87</td><td>RX0_1</td><td>CAN reception data 0 input pin (1)</td></tr><tr><td>Pin 97</td><td>RX0_0</td><td>CAN reception data 0 input pin (0)</td></tr><tr><td>Pin131</td><td>RX2_1</td><td>CAN reception data 2 output pin (1)</td></tr><tr><td>Pin132</td><td>TX2_1</td><td>CAN transmission data 2 output pin (1)</td></tr></table>	Pin 87	RX0_1	CAN reception data 0 input pin (1)	Pin 97	RX0_0	CAN reception data 0 input pin (0)	Pin131	RX2_1	CAN reception data 2 output pin (1)	Pin132	TX2_1	CAN transmission data 2 output pin (1)																														
Pin 87	RX0_1	CAN reception data 0 input pin (1)																																										
Pin 97	RX0_0	CAN reception data 0 input pin (0)																																										
Pin131	RX2_1	CAN reception data 2 output pin (1)																																										
Pin132	TX2_1	CAN transmission data 2 output pin (1)																																										

Page	Section	Change Results
27	4. I/O Circuit Types	Revised Type C of “I/O Circuit Type” as follows: (Correct) 
30	4. I/O Circuit Types	Added Type R to “11. I/O Circuit Type” R  Output of 2 mA
37	6. Handling Devices	Revised the Vss Pin in Figure 8-1 Pin Assignment. (Correct) Figure 8-1 Pin Assignment 
38	6. Handling Devices	Revised the items as follows. (Correct) This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 126 in S6J312xHzB* specifications) for internal stabilization of the device. For the standard values, see “Recommended operating conditions” in the latest data sheet. *x: A/9/8, z: A/B
39	7. Block Diagram	Revised the title as follows. (Correct) Figure 9-1 S6J312xHzB* Block Diagram *x: A/9/8, z: A/B
39	7. Block Diagram	Added “Partial Wake up” to “Block Diagram”

Page	Section	Change Results																																																																																																																																																																																																																																																																													
40	8. Memory Map	Revised “Figure 10-1 Memory Map” as full production. (Correct)																																																																																																																																																																																																																																																																													
		Figure 10-1 Memory Map(S6J312AHzB/9HzB/8HzB*) *z: A/B <table><thead><tr><th colspan="2">ADDRESS</th><th rowspan="2">group</th><th>S6J312AHzB*</th><th>S6J3129HzB*</th><th>S6J3128HzB*</th></tr><tr><th>START</th><th>END</th><th>part</th><th>part</th><th>part</th></tr></thead><tbody><tr><td>0x0000_0000</td><td>0x0000_7FFF</td><td rowspan="20">Internal area for CRS Complex</td><td>TCRAM (Main 64KByte)</td><td>TCRAM (Main 48KByte)</td><td>TCRAM (Main 32KByte)</td></tr><tr><td>0x0000_8000</td><td>0x0000_BFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0000_C000</td><td>0x0000_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0001_0000</td><td>0x007F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0080_0000</td><td>0x009E_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x009F_0000</td><td>0x009F_FFFF</td><td>TCM_FLASH (Small Sector 8KByte×8)</td><td>TCM_FLASH (Small Sector 8KByte×8)</td><td>TCM_FLASH (Small Sector 8KByte×8)</td></tr><tr><td>0x00A0_0000</td><td>0x00A7_FFFF</td><td>TCM_FLASH (Code 1MByte)</td><td>TCM_FLASH (Code 768KByte)</td><td>TCM_FLASH (Code 512KByte)</td></tr><tr><td>0x00A8_0000</td><td>0x00AB_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x00AC_0000</td><td>0x00AF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x00B0_0000</td><td>0x00DF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x00B0_0000</td><td>0x00FF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0100_0000</td><td>0x019E_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x019F_0000</td><td>0x019F_FFFF</td><td>AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)</td><td>AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)</td><td>AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)</td></tr><tr><td>0x01A0_0000</td><td>0x01A7_FFFF</td><td>AXI_FLASH_MEMORY (Code 1MByte *Mirror)</td><td>AXI_FLASH_MEMORY (Code 768KByte *Mirror)</td><td>AXI_FLASH_MEMORY (Code 512KByte *Mirror)</td></tr><tr><td>0x01A8_0000</td><td>0x01AB_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x01AC_0000</td><td>0x01AF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x01B0_0000</td><td>0x01DF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x01E0_0000</td><td>0x01FF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0200_0000</td><td>0x0200_3FFF</td><td>SYSTEM SRAM (16KByte)</td><td>SYSTEM SRAM (16KByte)</td><td>SYSTEM SRAM (16KByte)</td></tr><tr><td>0x0200_4000</td><td>0x0203_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0204_0000</td><td>0x027F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0280_0000</td><td>0x0280_0FFF</td><td>Exclusive Access Memory</td><td>Exclusive Access Memory</td><td>Exclusive Access Memory</td></tr><tr><td>0x0280_1000</td><td>0x029F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0400_0000</td><td>0x05FF_FFFF</td><td>AXI_SLAVE_CORE0</td><td>AXI_SLAVE_CORE0</td><td>AXI_SLAVE_CORE0</td></tr><tr><td>0x0600_0000</td><td>0x06FF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E00_0000</td><td>0x0E01_BFFF</td><td rowspan="10">Shared Flash and memory area</td><td>WORK_FLASH (112KByte mirror area 1)</td><td>WORK_FLASH (112KByte mirror area 1)</td><td>WORK_FLASH (112KByte mirror area 1)</td></tr><tr><td>0x0E01_C000</td><td>0x0E0F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E10_0000</td><td>0x0E1F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E20_0000</td><td>0x0E21_BFFF</td><td>WORK_FLASH (112KByte mirror area 3)</td><td>WORK_FLASH (112KByte mirror area 3)</td><td>WORK_FLASH (112KByte mirror area 3)</td></tr><tr><td>0x0E21_C000</td><td>0x0E2F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E30_0000</td><td>0x0E31_BFFF</td><td>WORK_FLASH (112KByte mirror area 4)</td><td>WORK_FLASH (112KByte mirror area 4)</td><td>WORK_FLASH (112KByte mirror area 4)</td></tr><tr><td>0x0E31_C000</td><td>0x0E3F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E40_0000</td><td>0x0E7F_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E80_0000</td><td>0x0E80_1FFF</td><td>Backup RAM 8KByte</td><td>Backup RAM 8KByte</td><td>Backup RAM 8KByte</td></tr><tr><td>0x0E80_2000</td><td>0x0E80_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E81_0000</td><td>0x0E87_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x0E88_0000</td><td>0x0FFF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x1000_0000</td><td>0x1FFF_FFFF</td><td rowspan="2">External bus area</td><td>EBI_MEMORY(SRAM/FLASH)</td><td>EBI_MEMORY(SRAM/FLASH)</td><td>EBI_MEMORY(SRAM/FLASH)</td></tr><tr><td>0x2000_0000</td><td>0x7FFF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0x8000_0000</td><td>0x8FFF_FFFF</td><td rowspan="2">HSSPI0 memory area</td><td>HSSPI0_MEMORY</td><td>HSSPI0_MEMORY</td><td>HSSPI0_MEMORY</td></tr><tr><td>0x9000_0000</td><td>0xAFFF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0xB800_0000</td><td>0xB853_FFFF</td><td rowspan="10">Peri area</td><td>Peri_area</td><td>Peri_area</td><td>Peri_area</td></tr><tr><td>0xB854_0000</td><td>0xB864_FFFF</td><td>APPS#5</td><td>APPS#5</td><td>APPS#5</td></tr><tr><td>0xB865_0000</td><td>0xB86B_FFFF</td><td>Peri_area</td><td>Peri_area</td><td>Peri_area</td></tr><tr><td>0xB86C_0000</td><td>0xB86C_FFFF</td><td>APPS#7</td><td>APPS#7</td><td>APPS#7</td></tr><tr><td>0xB86D_0000</td><td>0xB87F_FFFF</td><td>Peri_area</td><td>Peri_area</td><td>Peri_area</td></tr><tr><td>0xB880_0000</td><td>0xB8FF_FFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0xC000_0000</td><td>0xFFFE_DFFF</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr><tr><td>0xFFFE_E000</td><td>0xFFFE_FFFF</td><td>ERRCFG</td><td>ERRCFG</td><td>ERRCFG</td></tr><tr><td>0xFFFF_0000</td><td>0xFFFF_3FFF</td><td>BootRom</td><td>BootRom</td><td>BootRom</td></tr><tr><td>0xFFFF_4000</td><td>0xFFFF_FFFF</td><td>BootROM</td><td>Reserved</td><td>Reserved</td></tr></tbody></table>	ADDRESS		group	S6J312AHzB*	S6J3129HzB*	S6J3128HzB*	START	END	part	part	part	0x0000_0000	0x0000_7FFF	Internal area for CRS Complex	TCRAM (Main 64KByte)	TCRAM (Main 48KByte)	TCRAM (Main 32KByte)	0x0000_8000	0x0000_BFFF	Reserved	Reserved	Reserved	0x0000_C000	0x0000_FFFF	Reserved	Reserved	Reserved	0x0001_0000	0x007F_FFFF	Reserved	Reserved	Reserved	0x0080_0000	0x009E_FFFF	Reserved	Reserved	Reserved	0x009F_0000	0x009F_FFFF	TCM_FLASH (Small Sector 8KByte×8)	TCM_FLASH (Small Sector 8KByte×8)	TCM_FLASH (Small Sector 8KByte×8)	0x00A0_0000	0x00A7_FFFF	TCM_FLASH (Code 1MByte)	TCM_FLASH (Code 768KByte)	TCM_FLASH (Code 512KByte)	0x00A8_0000	0x00AB_FFFF	Reserved	Reserved	Reserved	0x00AC_0000	0x00AF_FFFF	Reserved	Reserved	Reserved	0x00B0_0000	0x00DF_FFFF	Reserved	Reserved	Reserved	0x00B0_0000	0x00FF_FFFF	Reserved	Reserved	Reserved	0x0100_0000	0x019E_FFFF	Reserved	Reserved	Reserved	0x019F_0000	0x019F_FFFF	AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)	AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)	AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror)	0x01A0_0000	0x01A7_FFFF	AXI_FLASH_MEMORY (Code 1MByte *Mirror)	AXI_FLASH_MEMORY (Code 768KByte *Mirror)	AXI_FLASH_MEMORY (Code 512KByte *Mirror)	0x01A8_0000	0x01AB_FFFF	Reserved	Reserved	Reserved	0x01AC_0000	0x01AF_FFFF	Reserved	Reserved	Reserved	0x01B0_0000	0x01DF_FFFF	Reserved	Reserved	Reserved	0x01E0_0000	0x01FF_FFFF	Reserved	Reserved	Reserved	0x0200_0000	0x0200_3FFF	SYSTEM SRAM (16KByte)	SYSTEM SRAM (16KByte)	SYSTEM SRAM (16KByte)	0x0200_4000	0x0203_FFFF	Reserved	Reserved	Reserved	0x0204_0000	0x027F_FFFF	Reserved	Reserved	Reserved	0x0280_0000	0x0280_0FFF	Exclusive Access Memory	Exclusive Access Memory	Exclusive Access Memory	0x0280_1000	0x029F_FFFF	Reserved	Reserved	Reserved	0x0400_0000	0x05FF_FFFF	AXI_SLAVE_CORE0	AXI_SLAVE_CORE0	AXI_SLAVE_CORE0	0x0600_0000	0x06FF_FFFF	Reserved	Reserved	Reserved	0x0E00_0000	0x0E01_BFFF	Shared Flash and memory area	WORK_FLASH (112KByte mirror area 1)	WORK_FLASH (112KByte mirror area 1)	WORK_FLASH (112KByte mirror area 1)	0x0E01_C000	0x0E0F_FFFF	Reserved	Reserved	Reserved	0x0E10_0000	0x0E1F_FFFF	Reserved	Reserved	Reserved	0x0E20_0000	0x0E21_BFFF	WORK_FLASH (112KByte mirror area 3)	WORK_FLASH (112KByte mirror area 3)	WORK_FLASH (112KByte mirror area 3)	0x0E21_C000	0x0E2F_FFFF	Reserved	Reserved	Reserved	0x0E30_0000	0x0E31_BFFF	WORK_FLASH (112KByte mirror area 4)	WORK_FLASH (112KByte mirror area 4)	WORK_FLASH (112KByte mirror area 4)	0x0E31_C000	0x0E3F_FFFF	Reserved	Reserved	Reserved	0x0E40_0000	0x0E7F_FFFF	Reserved	Reserved	Reserved	0x0E80_0000	0x0E80_1FFF	Backup RAM 8KByte	Backup RAM 8KByte	Backup RAM 8KByte	0x0E80_2000	0x0E80_FFFF	Reserved	Reserved	Reserved	0x0E81_0000	0x0E87_FFFF	Reserved	Reserved	Reserved	0x0E88_0000	0x0FFF_FFFF	Reserved	Reserved	Reserved	0x1000_0000	0x1FFF_FFFF	External bus area	EBI_MEMORY(SRAM/FLASH)	EBI_MEMORY(SRAM/FLASH)	EBI_MEMORY(SRAM/FLASH)	0x2000_0000	0x7FFF_FFFF	Reserved	Reserved	Reserved	0x8000_0000	0x8FFF_FFFF	HSSPI0 memory area	HSSPI0_MEMORY	HSSPI0_MEMORY	HSSPI0_MEMORY	0x9000_0000	0xAFFF_FFFF	Reserved	Reserved	Reserved	0xB800_0000	0xB853_FFFF	Peri area	Peri_area	Peri_area	Peri_area	0xB854_0000	0xB864_FFFF	APPS#5	APPS#5	APPS#5	0xB865_0000	0xB86B_FFFF	Peri_area	Peri_area	Peri_area	0xB86C_0000	0xB86C_FFFF	APPS#7	APPS#7	APPS#7	0xB86D_0000	0xB87F_FFFF	Peri_area	Peri_area	Peri_area	0xB880_0000	0xB8FF_FFFF	Reserved	Reserved	Reserved	0xC000_0000	0xFFFE_DFFF	Reserved	Reserved	Reserved	0xFFFE_E000	0xFFFE_FFFF	ERRCFG	ERRCFG	ERRCFG	0xFFFF_0000	0xFFFF_3FFF	BootRom	BootRom	BootRom	0xFFFF_4000	0xFFFF_FFFF	BootROM
ADDRESS		group	S6J312AHzB*	S6J3129HzB*		S6J3128HzB*																																																																																																																																																																																																																																																																									
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0xB800_0000	0xB853_FFFF	Peri area	Peri_area	Peri_area	Peri_area																																																																																																																																																																																																																																																																										
0xB854_0000	0xB864_FFFF		APPS#5	APPS#5	APPS#5																																																																																																																																																																																																																																																																										
0xB865_0000	0xB86B_FFFF		Peri_area	Peri_area	Peri_area																																																																																																																																																																																																																																																																										
0xB86C_0000	0xB86C_FFFF		APPS#7	APPS#7	APPS#7																																																																																																																																																																																																																																																																										
0xB86D_0000	0xB87F_FFFF		Peri_area	Peri_area	Peri_area																																																																																																																																																																																																																																																																										
0xB880_0000	0xB8FF_FFFF		Reserved	Reserved	Reserved																																																																																																																																																																																																																																																																										
0xC000_0000	0xFFFE_DFFF		Reserved	Reserved	Reserved																																																																																																																																																																																																																																																																										
0xFFFE_E000	0xFFFE_FFFF		ERRCFG	ERRCFG	ERRCFG																																																																																																																																																																																																																																																																										
0xFFFF_0000	0xFFFF_3FFF		BootRom	BootRom	BootRom																																																																																																																																																																																																																																																																										
0xFFFF_4000	0xFFFF_FFFF		BootROM	Reserved	Reserved																																																																																																																																																																																																																																																																										
41	8. Memory Map	Added item as follows. “The ECC movement in TCM port is based on ECC setting inside the CPU.”																																																																																																																																																																																																																																																																													
41	8. Memory Map	Revised " S6J312xHAA Peripheral Map" as follows (Correct) S6J312xHzB* Peripheral Map * x:A/9/8, z:A/B																																																																																																																																																																																																																																																																													

Page	Section	Change Results																																																												
45	8. Memory Map	Added “Partial Wake Up” to address of “B484_8400 to B484_87FF”. <table><tr><td>B484_8400</td><td>B484_87FF</td><td>APPS #5</td><td>A/D unit1 , Partial Wake Up</td><td>297</td></tr></table>	B484_8400	B484_87FF	APPS #5	A/D unit1 , Partial Wake Up	297																																																							
B484_8400	B484_87FF	APPS #5	A/D unit1 , Partial Wake Up	297																																																										
45	8. Memory Map	Revised the memory map of APPS#5 as follows. (Correct) <table><tr><td>B484_8C00</td><td>B484_8FFF</td><td></td><td>Reserved</td><td></td></tr><tr><td>B484_9000</td><td>B484_93FF</td><td>APPS #5</td><td>Global Timer</td><td>300</td></tr><tr><td>B484_9400</td><td>B484_FFFF</td><td></td><td>Reserved</td><td></td></tr></table>	B484_8C00	B484_8FFF		Reserved		B484_9000	B484_93FF	APPS #5	Global Timer	300	B484_9400	B484_FFFF		Reserved																																														
B484_8C00	B484_8FFF		Reserved																																																											
B484_9000	B484_93FF	APPS #5	Global Timer	300																																																										
B484_9400	B484_FFFF		Reserved																																																											
45	8. Memory Map	Revised the memory map of APPS#7 as follows. (Correct) <table><tr><td>START</td><td>END</td><td></td><td></td><td>PPU</td></tr><tr><td>Address</td><td>Address</td><td></td><td>Function</td><td>No</td></tr><tr><td>B48C_0000</td><td>B48C_3FFF</td><td></td><td>Reserved</td><td>-</td></tr><tr><td>B48C_4000</td><td>B48C_43FF</td><td>APPS #7</td><td>Stepper Motor Control ch.0</td><td>317</td></tr><tr><td>B48C_4400</td><td>B48C_47FF</td><td>APPS #7</td><td>Stepper Motor Control ch.1</td><td>318</td></tr><tr><td>B48C_4800</td><td>B48C_4BFF</td><td>APPS #7</td><td>Stepper Motor Control ch.2</td><td>319</td></tr><tr><td>B48C_4C00</td><td>B48C_4FFF</td><td>APPS #7</td><td>Stepper Motor Control ch.3</td><td>320</td></tr><tr><td>B48C_5000</td><td>B48C_57FF</td><td></td><td>Reserved</td><td>-</td></tr><tr><td>B48C_5800</td><td>B48C_5BFF</td><td>APPS #7</td><td>SMC Trigger Generator</td><td>323</td></tr><tr><td>B48C_5C00</td><td>B48C_5FFF</td><td>APPS #7</td><td>Liquid Crystal Display Controller</td><td>324</td></tr><tr><td>B48C_6000</td><td>B48C_63FF</td><td>APPS #7</td><td>Liquid Crystal Display input/output control</td><td>325</td></tr><tr><td>B48C_6400</td><td>B48C_FFFF</td><td></td><td>Reserved</td><td>-</td></tr></table>	START	END			PPU	Address	Address		Function	No	B48C_0000	B48C_3FFF		Reserved	-	B48C_4000	B48C_43FF	APPS #7	Stepper Motor Control ch.0	317	B48C_4400	B48C_47FF	APPS #7	Stepper Motor Control ch.1	318	B48C_4800	B48C_4BFF	APPS #7	Stepper Motor Control ch.2	319	B48C_4C00	B48C_4FFF	APPS #7	Stepper Motor Control ch.3	320	B48C_5000	B48C_57FF		Reserved	-	B48C_5800	B48C_5BFF	APPS #7	SMC Trigger Generator	323	B48C_5C00	B48C_5FFF	APPS #7	Liquid Crystal Display Controller	324	B48C_6000	B48C_63FF	APPS #7	Liquid Crystal Display input/output control	325	B48C_6400	B48C_FFFF		Reserved	-
START	END			PPU																																																										
Address	Address		Function	No																																																										
B48C_0000	B48C_3FFF		Reserved	-																																																										
B48C_4000	B48C_43FF	APPS #7	Stepper Motor Control ch.0	317																																																										
B48C_4400	B48C_47FF	APPS #7	Stepper Motor Control ch.1	318																																																										
B48C_4800	B48C_4BFF	APPS #7	Stepper Motor Control ch.2	319																																																										
B48C_4C00	B48C_4FFF	APPS #7	Stepper Motor Control ch.3	320																																																										
B48C_5000	B48C_57FF		Reserved	-																																																										
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B48C_5C00	B48C_5FFF	APPS #7	Liquid Crystal Display Controller	324																																																										
B48C_6000	B48C_63FF	APPS #7	Liquid Crystal Display input/output control	325																																																										
B48C_6400	B48C_FFFF		Reserved	-																																																										
45	8. Memory Map	Added the following note. When MPU attribute of Cortex®-R5 is configured as "Normal", store buffer inside Cortex®-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used. MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence. -Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF] -Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF] -Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF] MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation. -FLASH Memory (when writing commands)																																																												
45	8. Memory Map	Added the following note. SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)																																																												
46,47	9. Pin Status in CPU Status	Added Pin name about I ² C and PWU to Table 11-1 Pin State Table (1/2) and Table 11-2 Pin State Table (2/2).																																																												
47	9. Pin Status in CPU Status	Deleted the following pin name about CANFD ch2 from Table 11-2 Pin State Table (2/2) Pin132 : TX2_1 Pin131 : RX2_1 Pin87 : RX0_1 Pin97 : RX0_0																																																												
48	9. Pin Status in CPU Status	Added the item as follows *7: When the PWU function is enabled, a change to output occurs. *8: When PPC_PCFGRIj:POF[2:0] is set to initial value. *9: When reset is issued, the following ports become "L" output as the initial state.																																																												

Page	Section	Change Results					
50	10. Electrical Characteristics 10.1 Absolute Maximum Ratings	Revised the remarks of Analog supply voltage (Error) $AV_{CC} \leq V_{CC}$ (Correct) $AV_{CC} = V_{CC}$					
50	10. Electrical Characteristics 10.1 Absolute Maximum Ratings	Revised the Symbol of Maximum clamp current. (Error) I_{CLAMP} (Correct) $ I_{CLAMP} $					
50	10. Electrical Characteristics 10.1 Absolute Maximum Ratings	Revised the following note. (Error) *2: VCC and DVCC must be set to the same voltage. Caution must be taken that AVCC and DVCC does not exceed VCC upon power-on and under other circumstances. (Correct) *2: AVCC, DVCC and VCC must be set to the same voltage. It is required that AVCC and DVCC do not exceed VCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on.					
52	10. Electrical Characteristics 10.2 Recommended operating conditions	Revised the following title. (Error) Rating (Correct) Value					
52	10. Electrical Characteristics 10.2 Recommended operating conditions	Revised the parameter of Smoothing capacitor as follows. (Correct) <table><tr><td>Smoothing capacitor*</td><td>C_{S1}</td><td>4.7</td><td>μF</td><td>Tolerance of up to ±40%, 126pin Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.</td></tr></table>	Smoothing capacitor*	C _{S1}	4.7	μF	Tolerance of up to ±40%, 126pin Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.
Smoothing capacitor*	C _{S1}	4.7	μF	Tolerance of up to ±40%, 126pin Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than CS as the smoothing capacitor on the VCC pin.			
52	10. Electrical Characteristics 10.2 Recommended operating conditions	Revised the remarks of Operating temperature as follows. (Error) S6J312HAA (Correct) S6J312xHzB* * x:A/9/8, z:A/B					
52	10. Electrical Characteristics 10.2 Recommended operating conditions	Revised the following Diagram (Correct) · C Pin Connection Diagram 					

Page	Section	Change Results
53	10. Electrical Characteristics 10.2 Recommended operating conditions	Added the following notes. Notes: –The following condition should be satisfied in order to facilitate heat dissipation. 1. 4 or more layers PCB should be used. 2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard) 3. 1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground. 4. 35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer. 5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.
53,54	10. Electrical Characteristics 10.2 Recommended operating conditions	Added the following notes and figures. Figure12.2-1: Example thermal via holes on PCB. Notes: – Figure 12.2-1 is a schematic diagram showing PCB in section. – Figure 12.2-2 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands. – If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand. Figure 12.2-2: Land Pattern and Thermal Via LEU144
63	10. Electrical Characteristics 10.3 DC Characteristics	Revised the following pins of Rup3 (Error) P321, TDI(P324), TMS,TCK (Correct) TDI(P324), TMS,TCK
65	10. Electrical Characteristics 10.3 DC Characteristics	Revised the following values and remarks. ICC5,ICC55:Remarks (Error) Operating at 112 MHz (Correct) Operating at 128MHz ICC5 : Value (Error) Normal Operation typ 100mA max 225mA (Correct) Normal Operation typ 90mA max 195mA ICCT52:Value (Error) max 115µA (Correct) max 100µA ICCT52M:Value (Error) typ 700µA max 885µA (Correct) typ 350µA max 520µA ICCH52:Value (Error) max 110µA (Correct) max 100µA
65	10. Electrical Characteristics 10.3 DC Characteristics	Added the following characteristic ICC_P PWU mode(Shutdown)

Page	Section	Change Results																																																																																																																																																																																																																																																																																													
65	10. Electrical Characteristics 10.3 DC Characteristics	Revised the followings in parameter cell. (Error) S6J312HAA (Correct) S6J312xHzB* *x:A/9/8 z: A/B																																																																																																																																																																																																																																																																																													
69	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised the value of frequency excepts F _{CLK_EXTBUS} and F _{CANFD_CCLK} (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">S6J312xHzB* Value * x:A/9/8, z:A/B</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="34">Internal Clock Frequency</td><td>F_{CLK_CPU}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>128</td><td>MHz</td><td>CLK_CPU</td></tr><tr><td>F_{CLK_FCLK}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_FCLK</td></tr><tr><td>F_{CLK_ATB}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_ATB</td></tr><tr><td>F_{CLK_DBG}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_DBG</td></tr><tr><td>F_{CLK_HPM}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HPM</td></tr><tr><td>F_{CLK_HPM2}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>16</td><td>MHz</td><td>CLK_HPM2</td></tr><tr><td>F_{CLK_DMA}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_DMA</td></tr><tr><td>F_{CLK_MEMC}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_MEMC</td></tr><tr><td>F_{CLK_EXTBUS}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>25</td><td>MHz</td><td>CLK_EXTBUS</td></tr><tr><td>F_{CLK_SYSC1}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_SYSC1</td></tr><tr><td>F_{CLK_HAPP0A0}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HAPP0A0</td></tr><tr><td>F_{CLK_HAPP0A1}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HAPP0A1</td></tr><tr><td>F_{CLK_HAPP1B0}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HAPP1B0</td></tr><tr><td>F_{CLK_HAPP1B1}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HAPP1B1</td></tr><tr><td>F_{CLK_LLPBM}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>128</td><td>MHz</td><td>CLK_LLPBM</td></tr><tr><td>F_{CLK_LLPBM2}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_LLPBM2</td></tr><tr><td>F_{CLK_LCP}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_LCP</td></tr><tr><td>F_{CLK_LCP0}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LCP0</td></tr><tr><td>F_{CLK_LCP0A}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LCP0A</td></tr><tr><td>F_{CLK_LCP1}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LCP1</td></tr><tr><td>F_{CLK_LCP1A}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LCP1A</td></tr><tr><td>F_{CLK_LAPP0}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LAPP0</td></tr><tr><td>F_{CLK_LAPP0A}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LAPP0A</td></tr><tr><td>F_{CLK_LAPP1}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LAPP1</td></tr><tr><td>F_{CLK_LAPP1A}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_LAPP1A</td></tr><tr><td>F_{CLK_TRC}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>64</td><td>MHz</td><td>CLK_TRC</td></tr><tr><td>F_{CLK_HSSPI}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_HSSPI</td></tr><tr><td>F_{CLK_SYSC0H}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_SYSC0H</td></tr><tr><td>F_{CLK_COMH}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_COMH</td></tr><tr><td>F_{CLK_RAM0H}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_RAM0H</td></tr><tr><td>F_{CLK_RAM1H}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_RAM1H</td></tr><tr><td>F_{CLK_SYSC0P}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_SYSC0P</td></tr><tr><td>F_{CLK_COMP}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>32</td><td>MHz</td><td>CLK_COMP</td></tr><tr><td>F_{CANFD_CCLK}</td><td>-</td><td>-</td><td>-</td><td>-</td><td>40</td><td>MHz</td><td>CANFD_CCLK</td></tr></table>	Parameter	Symbol	Pin Name	Conditions	S6J312xHzB* Value * x:A/9/8, z:A/B			Unit	Remarks	Min	Typ	Max	Internal Clock Frequency	F _{CLK_CPU}	-	-	-	-	128	MHz	CLK_CPU	F _{CLK_FCLK}	-	-	-	-	64	MHz	CLK_FCLK	F _{CLK_ATB}	-	-	-	-	64	MHz	CLK_ATB	F _{CLK_DBG}	-	-	-	-	64	MHz	CLK_DBG	F _{CLK_HPM}	-	-	-	-	32	MHz	CLK_HPM	F _{CLK_HPM2}	-	-	-	-	16	MHz	CLK_HPM2	F _{CLK_DMA}	-	-	-	-	32	MHz	CLK_DMA	F _{CLK_MEMC}	-	-	-	-	32	MHz	CLK_MEMC	F _{CLK_EXTBUS}	-	-	-	-	25	MHz	CLK_EXTBUS	F _{CLK_SYSC1}	-	-	-	-	32	MHz	CLK_SYSC1	F _{CLK_HAPP0A0}	-	-	-	-	32	MHz	CLK_HAPP0A0	F _{CLK_HAPP0A1}	-	-	-	-	32	MHz	CLK_HAPP0A1	F _{CLK_HAPP1B0}	-	-	-	-	32	MHz	CLK_HAPP1B0	F _{CLK_HAPP1B1}	-	-	-	-	32	MHz	CLK_HAPP1B1	F _{CLK_LLPBM}	-	-	-	-	128	MHz	CLK_LLPBM	F _{CLK_LLPBM2}	-	-	-	-	64	MHz	CLK_LLPBM2	F _{CLK_LCP}	-	-	-	-	64	MHz	CLK_LCP	F _{CLK_LCP0}	-	-	-	-	32	MHz	CLK_LCP0	F _{CLK_LCP0A}	-	-	-	-	32	MHz	CLK_LCP0A	F _{CLK_LCP1}	-	-	-	-	32	MHz	CLK_LCP1	F _{CLK_LCP1A}	-	-	-	-	32	MHz	CLK_LCP1A	F _{CLK_LAPP0}	-	-	-	-	32	MHz	CLK_LAPP0	F _{CLK_LAPP0A}	-	-	-	-	32	MHz	CLK_LAPP0A	F _{CLK_LAPP1}	-	-	-	-	32	MHz	CLK_LAPP1	F _{CLK_LAPP1A}	-	-	-	-	32	MHz	CLK_LAPP1A	F _{CLK_TRC}	-	-	-	-	64	MHz	CLK_TRC	F _{CLK_HSSPI}	-	-	-	-	32	MHz	CLK_HSSPI	F _{CLK_SYSC0H}	-	-	-	-	32	MHz	CLK_SYSC0H	F _{CLK_COMH}	-	-	-	-	32	MHz	CLK_COMH	F _{CLK_RAM0H}	-	-	-	-	32	MHz	CLK_RAM0H	F _{CLK_RAM1H}	-	-	-	-	32	MHz	CLK_RAM1H	F _{CLK_SYSC0P}	-	-	-	-	32	MHz	CLK_SYSC0P	F _{CLK_COMP}	-	-	-	-	32	MHz	CLK_COMP	F _{CANFD_CCLK}	-	-	-	-	40	MHz	CANFD_CCLK
Parameter	Symbol	Pin Name					Conditions	S6J312xHzB* Value * x:A/9/8, z:A/B				Unit	Remarks																																																																																																																																																																																																																																																																																		
			Min	Typ	Max																																																																																																																																																																																																																																																																																										
Internal Clock Frequency	F _{CLK_CPU}	-	-	-	-	128	MHz	CLK_CPU																																																																																																																																																																																																																																																																																							
	F _{CLK_FCLK}	-	-	-	-	64	MHz	CLK_FCLK																																																																																																																																																																																																																																																																																							
	F _{CLK_ATB}	-	-	-	-	64	MHz	CLK_ATB																																																																																																																																																																																																																																																																																							
	F _{CLK_DBG}	-	-	-	-	64	MHz	CLK_DBG																																																																																																																																																																																																																																																																																							
	F _{CLK_HPM}	-	-	-	-	32	MHz	CLK_HPM																																																																																																																																																																																																																																																																																							
	F _{CLK_HPM2}	-	-	-	-	16	MHz	CLK_HPM2																																																																																																																																																																																																																																																																																							
	F _{CLK_DMA}	-	-	-	-	32	MHz	CLK_DMA																																																																																																																																																																																																																																																																																							
	F _{CLK_MEMC}	-	-	-	-	32	MHz	CLK_MEMC																																																																																																																																																																																																																																																																																							
	F _{CLK_EXTBUS}	-	-	-	-	25	MHz	CLK_EXTBUS																																																																																																																																																																																																																																																																																							
	F _{CLK_SYSC1}	-	-	-	-	32	MHz	CLK_SYSC1																																																																																																																																																																																																																																																																																							
	F _{CLK_HAPP0A0}	-	-	-	-	32	MHz	CLK_HAPP0A0																																																																																																																																																																																																																																																																																							
	F _{CLK_HAPP0A1}	-	-	-	-	32	MHz	CLK_HAPP0A1																																																																																																																																																																																																																																																																																							
	F _{CLK_HAPP1B0}	-	-	-	-	32	MHz	CLK_HAPP1B0																																																																																																																																																																																																																																																																																							
	F _{CLK_HAPP1B1}	-	-	-	-	32	MHz	CLK_HAPP1B1																																																																																																																																																																																																																																																																																							
	F _{CLK_LLPBM}	-	-	-	-	128	MHz	CLK_LLPBM																																																																																																																																																																																																																																																																																							
	F _{CLK_LLPBM2}	-	-	-	-	64	MHz	CLK_LLPBM2																																																																																																																																																																																																																																																																																							
	F _{CLK_LCP}	-	-	-	-	64	MHz	CLK_LCP																																																																																																																																																																																																																																																																																							
	F _{CLK_LCP0}	-	-	-	-	32	MHz	CLK_LCP0																																																																																																																																																																																																																																																																																							
	F _{CLK_LCP0A}	-	-	-	-	32	MHz	CLK_LCP0A																																																																																																																																																																																																																																																																																							
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	F _{CLK_LCP1A}	-	-	-	-	32	MHz	CLK_LCP1A																																																																																																																																																																																																																																																																																							
	F _{CLK_LAPP0}	-	-	-	-	32	MHz	CLK_LAPP0																																																																																																																																																																																																																																																																																							
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	F _{CLK_LAPP1}	-	-	-	-	32	MHz	CLK_LAPP1																																																																																																																																																																																																																																																																																							
	F _{CLK_LAPP1A}	-	-	-	-	32	MHz	CLK_LAPP1A																																																																																																																																																																																																																																																																																							
	F _{CLK_TRC}	-	-	-	-	64	MHz	CLK_TRC																																																																																																																																																																																																																																																																																							
	F _{CLK_HSSPI}	-	-	-	-	32	MHz	CLK_HSSPI																																																																																																																																																																																																																																																																																							
	F _{CLK_SYSC0H}	-	-	-	-	32	MHz	CLK_SYSC0H																																																																																																																																																																																																																																																																																							
	F _{CLK_COMH}	-	-	-	-	32	MHz	CLK_COMH																																																																																																																																																																																																																																																																																							
	F _{CLK_RAM0H}	-	-	-	-	32	MHz	CLK_RAM0H																																																																																																																																																																																																																																																																																							
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	F _{CLK_SYSC0P}	-	-	-	-	32	MHz	CLK_SYSC0P																																																																																																																																																																																																																																																																																							
	F _{CLK_COMP}	-	-	-	-	32	MHz	CLK_COMP																																																																																																																																																																																																																																																																																							
	F _{CANFD_CCLK}	-	-	-	-	40	MHz	CANFD_CCLK																																																																																																																																																																																																																																																																																							

Page	Section	Change Results																																																																																																																																																																																																																																																																																													
70	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised the value of pulse width excepts t_{CLK_EXTBUS} and t_{CANFD_CCLK} (Correct) <table><tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pin Name</th><th rowspan="2">Conditions</th><th colspan="3">S6J312xHAzB* Value * x: A/9/8, z: A/B</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td rowspan="34">Internal clock cycle time</td><td>t_{CLK_CPU}</td><td>-</td><td>-</td><td>7.82</td><td>-</td><td>-</td><td>ns</td><td>CLK_CPU</td></tr><tr><td>t_{CLK_FLASH}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_FLASH</td></tr><tr><td>t_{CLK_ATB}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_ATB</td></tr><tr><td>t_{CLK_DBG}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_DBG</td></tr><tr><td>t_{CLK_HPM}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HPM</td></tr><tr><td>t_{CLK_HPM2}</td><td>-</td><td>-</td><td>62.54</td><td>-</td><td>-</td><td>ns</td><td>CLK_HPM2</td></tr><tr><td>t_{CLK_DMA}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_DMA</td></tr><tr><td>t_{CLK_MEMC}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_MEMC</td></tr><tr><td>t_{CLK_EXTBUS}</td><td>-</td><td>-</td><td>40.00</td><td>-</td><td>-</td><td>ns</td><td>CLK_EXTBUS</td></tr><tr><td>t_{CLK_SYSC1}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_SYSC1</td></tr><tr><td>t_{CLK_HAPP0A0}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HAPP0A0</td></tr><tr><td>t_{CLK_HAPP0A1}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HAPP0A1</td></tr><tr><td>t_{CLK_HAPP1B0}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HAPP1B0</td></tr><tr><td>t_{CLK_HAPP1B1}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HAPP1B1</td></tr><tr><td>t_{CLK_LLPM}</td><td>-</td><td>-</td><td>7.82</td><td>-</td><td>-</td><td>ns</td><td>CLK_LLPM</td></tr><tr><td>t_{CLK_LLPM2}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_LLPM2</td></tr><tr><td>t_{CLK_LCP}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_LCP</td></tr><tr><td>t_{CLK_LCP0}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LCP0</td></tr><tr><td>t_{CLK_LCP0A}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LCP0A</td></tr><tr><td>t_{CLK_LCP1}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LCP1</td></tr><tr><td>t_{CLK_LCP1A}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LCP1A</td></tr><tr><td>t_{CLK_LAPP0}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LAPP0</td></tr><tr><td>t_{CLK_LAPP0A}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LAPP0A</td></tr><tr><td>t_{CLK_LAPP1}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LAPP1</td></tr><tr><td>t_{CLK_LAPP1A}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_LAPP1A</td></tr><tr><td>t_{CLK_TRC}</td><td>-</td><td>-</td><td>15.64</td><td>-</td><td>-</td><td>ns</td><td>CLK_TRC</td></tr><tr><td>t_{CLK_HSSPI}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_HSSPI</td></tr><tr><td>t_{CLK_SYSC0H}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_SYSC0H</td></tr><tr><td>t_{CLK_COMH}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_COMH</td></tr><tr><td>t_{CLK_RAM0H}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_RAM0H</td></tr><tr><td>t_{CLK_RAM1H}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_RAM1H</td></tr><tr><td>t_{CLK_SYSC0P}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_SYSC0P</td></tr><tr><td>t_{CLK_COMP}</td><td>-</td><td>-</td><td>31.28</td><td>-</td><td>-</td><td>ns</td><td>CLK_COMP</td></tr><tr><td>t_{CANFD_CCLK}</td><td>-</td><td>-</td><td>25.00</td><td>-</td><td>-</td><td>ns</td><td>CANFD_CCLK</td></tr></table>	Parameter	Symbol	Pin Name	Conditions	S6J312xHAzB* Value * x: A/9/8, z: A/B			Unit	Remarks	Min	Typ	Max	Internal clock cycle time	t _{CLK_CPU}	-	-	7.82	-	-	ns	CLK_CPU	t _{CLK_FLASH}	-	-	15.64	-	-	ns	CLK_FLASH	t _{CLK_ATB}	-	-	15.64	-	-	ns	CLK_ATB	t _{CLK_DBG}	-	-	15.64	-	-	ns	CLK_DBG	t _{CLK_HPM}	-	-	31.28	-	-	ns	CLK_HPM	t _{CLK_HPM2}	-	-	62.54	-	-	ns	CLK_HPM2	t _{CLK_DMA}	-	-	31.28	-	-	ns	CLK_DMA	t _{CLK_MEMC}	-	-	31.28	-	-	ns	CLK_MEMC	t _{CLK_EXTBUS}	-	-	40.00	-	-	ns	CLK_EXTBUS	t _{CLK_SYSC1}	-	-	31.28	-	-	ns	CLK_SYSC1	t _{CLK_HAPP0A0}	-	-	31.28	-	-	ns	CLK_HAPP0A0	t _{CLK_HAPP0A1}	-	-	31.28	-	-	ns	CLK_HAPP0A1	t _{CLK_HAPP1B0}	-	-	31.28	-	-	ns	CLK_HAPP1B0	t _{CLK_HAPP1B1}	-	-	31.28	-	-	ns	CLK_HAPP1B1	t _{CLK_LLPM}	-	-	7.82	-	-	ns	CLK_LLPM	t _{CLK_LLPM2}	-	-	15.64	-	-	ns	CLK_LLPM2	t _{CLK_LCP}	-	-	15.64	-	-	ns	CLK_LCP	t _{CLK_LCP0}	-	-	31.28	-	-	ns	CLK_LCP0	t _{CLK_LCP0A}	-	-	31.28	-	-	ns	CLK_LCP0A	t _{CLK_LCP1}	-	-	31.28	-	-	ns	CLK_LCP1	t _{CLK_LCP1A}	-	-	31.28	-	-	ns	CLK_LCP1A	t _{CLK_LAPP0}	-	-	31.28	-	-	ns	CLK_LAPP0	t _{CLK_LAPP0A}	-	-	31.28	-	-	ns	CLK_LAPP0A	t _{CLK_LAPP1}	-	-	31.28	-	-	ns	CLK_LAPP1	t _{CLK_LAPP1A}	-	-	31.28	-	-	ns	CLK_LAPP1A	t _{CLK_TRC}	-	-	15.64	-	-	ns	CLK_TRC	t _{CLK_HSSPI}	-	-	31.28	-	-	ns	CLK_HSSPI	t _{CLK_SYSC0H}	-	-	31.28	-	-	ns	CLK_SYSC0H	t _{CLK_COMH}	-	-	31.28	-	-	ns	CLK_COMH	t _{CLK_RAM0H}	-	-	31.28	-	-	ns	CLK_RAM0H	t _{CLK_RAM1H}	-	-	31.28	-	-	ns	CLK_RAM1H	t _{CLK_SYSC0P}	-	-	31.28	-	-	ns	CLK_SYSC0P	t _{CLK_COMP}	-	-	31.28	-	-	ns	CLK_COMP	t _{CANFD_CCLK}	-	-	25.00	-	-	ns	CANFD_CCLK
Parameter	Symbol	Pin Name					Conditions	S6J312xHAzB* Value * x: A/9/8, z: A/B				Unit	Remarks																																																																																																																																																																																																																																																																																		
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	t _{CLK_HPM2}	-	-	62.54	-	-	ns	CLK_HPM2																																																																																																																																																																																																																																																																																							
	t _{CLK_DMA}	-	-	31.28	-	-	ns	CLK_DMA																																																																																																																																																																																																																																																																																							
	t _{CLK_MEMC}	-	-	31.28	-	-	ns	CLK_MEMC																																																																																																																																																																																																																																																																																							
	t _{CLK_EXTBUS}	-	-	40.00	-	-	ns	CLK_EXTBUS																																																																																																																																																																																																																																																																																							
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	t _{CLK_HAPP0A0}	-	-	31.28	-	-	ns	CLK_HAPP0A0																																																																																																																																																																																																																																																																																							
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	t _{CLK_LLPM}	-	-	7.82	-	-	ns	CLK_LLPM																																																																																																																																																																																																																																																																																							
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	t _{CANFD_CCLK}	-	-	25.00	-	-	ns	CANFD_CCLK																																																																																																																																																																																																																																																																																							
71	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised the value of max internal frequency F_{CPU_CLK} in “Guaranteed operation range” (Error) 112MHz (Correct) 128MHz																																																																																																																																																																																																																																																																																													
72	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised the followings “Relationship between the oscillation clock frequency and internal clock frequency” PLL Multiplier Setting (Error) 112 (Correct) 128 PLL Clock (Error) 112MHz (Correct) 128MHz Notes (Error) The maximum PLL clock frequency must be 112MHz. (Correct) The maximum PLL clock frequency must be 128MHz.																																																																																																																																																																																																																																																																																													
74	10. Electrical Characteristics 10.4.4 Power-on Conditions	Added the parameter of “Level release voltage”																																																																																																																																																																																																																																																																																													

Page	Section	Change Results								
74	10. Electrical Characteristics 10.4.4 Power-on Conditions	Revised the value of “Level detection voltage” (Error) min 2.25V typ 2.45V max 2.65V (Correct) min 2.15V typ 2.35V max 2.55V								
101,102	10. Electrical Characteristics 10.4.7.4 I ² C Timing (SMR:MD[2:0]=100B)	Added the characteristic of “I ² C Timing (SMR:MD[2:0]=100B)”								
116,117	10. Electrical Characteristics 10.12 A/D Converter 10.12.1 Electrical Characteristics	Revised the value of “Analog port input current” in the table, and revised the pin name note *7 to *9 (Correct) *7: AN3, AN5, AN6, AN9, AN10, AN12 to AN15, AN17 to AN24, and AN27 to AN42 *8: AN0 to AN2, and AN43 *9: AN44 to AN62								
119	10. Electrical Characteristics 10.12 A/D Converter 10.12.3 Definition of Terms	Revised the followings. (Error) Total error: Difference between the actual value and the theoretical value. The total error (Correct) Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.								
121	10. Electrical Characteristics 10.13 Flash Memory	Deleted the followings. *3: Target value								
122	11. Ordering Information	Added SHE option to the part number <table><tr><th>Part Number Option “z”</th><th>SHE</th></tr><tr><td>A</td><td>SHE ON</td></tr><tr><td>B</td><td>SHE OFF</td></tr></table>	Part Number Option “z”	SHE	A	SHE ON	B	SHE OFF		
Part Number Option “z”	SHE									
A	SHE ON									
B	SHE OFF									
122	12.Part Number Option	Added Flash memory size option to the part number. <table><tr><th>Part Number Option “x”</th><th>FLASH Memory</th></tr><tr><td>A</td><td>1MByte</td></tr><tr><td>9</td><td>768KByte</td></tr><tr><td>8</td><td>512KByte</td></tr></table>	Part Number Option “x”	FLASH Memory	A	1MByte	9	768KByte	8	512KByte
Part Number Option “x”	FLASH Memory									
A	1MByte									
9	768KByte									
8	512KByte									
Revision *B										
1	Cover	Revised the title as follow (error) S6J3120 Series 32-bit Microcontroller Spansion® Traveo™ Family (correct) S6J3120 Series 32-Bit Traveo™ Family Microcontroller Datasheet								
2	Features	Added “CAN-FD (V3.2.0)” under “CAN controller: CAN-FD Max 3 channel”.								
37	6.Handling Devices	Revised the following notice. (Error) About the Power-on Time To prevent the internal built-in voltage step-down circuit from malfunctioning, secure a voltage rising time of 50 μs (between 0.2 V and 2.7 V) or longer at the power-on time. (Correct) About the Power-on Time To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.								

Page	Section	Change Results
70	10. Electrical Characteristics 10.4.2 Internal Clock Timing	Revised the following symbol. (Error) tCLK_FMA (Correct) tCLK_DMA
74	10. Electrical Characteristics 10.4.4 Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and Maximum ramp rate guaranteed to not generate power-on reset. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, Maximum ramp rate guaranteed to not generate power-on reset.
101	10. Electrical Characteristics 10.4.7.4 I2C Timing (SMR:MD[2:0]=100B)	Revised the following pin names. (Error) SCL0 to SCL4 / SDA0 to SDA4 (Correct) SCL0, SCL3, SCL4 / SDA0, SDA3, SDA4
115	10. Electrical Characteristics 10.10 Low-Voltage Detection (RAM Retention Low-Voltage Detection)	Revised the title in 10.10 “Internal Low-Voltage Detection” to “RAM Retention Low-Voltage Detection”.
115	10. Electrical Characteristics 10.11 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection)	Added the notice *4
123	11. Ordering Information	Revised the following part number. (Error) S6J312xHzBASEy0000* (Correct) S6J312xHzCSEy0000*
1,2,6 to 9, 38 to 40, 42,50,52, 65,69,70, 74,123	-	Revised part number from S6J312xxxB to S6J312xxxC.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: S6J3120 Series 32-Bit Traveo™ Family Microcontroller Datasheet

Document Number: 002-04863

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	HIHA	8/7/2014	Initial release New Spec.
*A	4993737	WECU	10/29/2015	Added full product names. Added 144pin PWUTRG function. Added simultaneous function for start timing of PWM does not overlap. Added I2C function. Added SHE-OFF Option. Updated CANFD macro (updated to v3.2.0). Revised min value of VIH6 (TRST, TCK, TDI, TMS) from 2.0V to 2.3V. Revised operating frequency to 128MHz, and revised clock frequency based 128MHz. Revised current consumption standard (ICC5, ICCT52, ICCT52M, ICCH52). Added partial wakeup macro. For detail, see "Major Changes".
*B	5309249	WECU	06/16/2016	Revised part number from S6J311xxxB to S6J311xxxC. For detail, see "Major Changes".
*C	5375465	WECU	07/27/2016	Page 74, 10.4.4 Power-on Conditions Revised Level detection time from 30 to 540, Revised *1 to *4 and Note. Page 115, 10.10 Low-Voltage Detection (RAM Retention Low-Voltage Detection) Added * and Note to Detection voltage. Page 115, 10.11 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection) Added * and Note to Detection voltage.
*D	5554888	WECU	12/15/2016	Page 124, Replaced 13. Package Dimensions Page 125, Added 14. Appendix
*E	5782640	YOST	06/22/2017	Updated Cypress logo. Updated Copyright.
*F	6251474	MXNI	07/18/2018	Part Number Option is updated.
*G	6295507	MXNI	08/30/2018	Page 99 Added 14. Errata

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Тел: +7 (812) 336 43 04 (многоканальный)

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