

# FDM3622

## N-Channel PowerTrench® MOSFET

100V, 4.4A, 60mΩ

### Features

- Max  $r_{DS(on)}$  = 60mΩ at  $V_{GS} = 10V$ ,  $I_D = 4.4A$
- Max  $r_{DS(on)}$  = 80mΩ at  $V_{GS} = 6.0V$ ,  $I_D = 3.8A$
- Low Miller Charge
- Low QRR Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

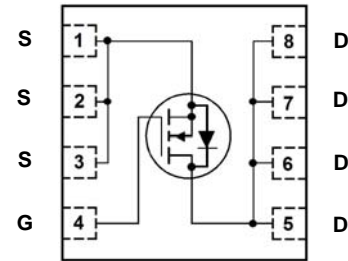
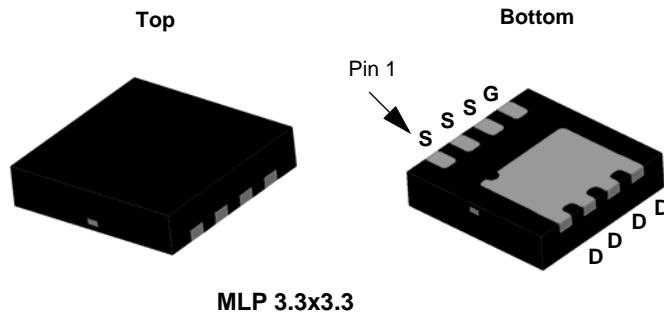


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

### Applications

- Distributed Power Architectures and VRMs.
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Formerly developmental type 82744



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	4.4	A
	-Pulsed	20	
$P_D$	Power Dissipation	2.1	W
	Power Dissipation	0.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDM3622	FDM3622	MLP 3.3x3.3	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$ $T_J = 100^\circ\text{C}$			1	$\mu\text{A}$
					250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2		4	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.4\text{A}$		44	60	m $\Omega$
		$V_{GS} = 6.0\text{V}, I_D = 3.8\text{A}$		56	80	
		$V_{GS} = 10\text{V}, I_D = 4.4\text{A}, T_J = 150^\circ\text{C}$		92	120	

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		820	1090	pF
$C_{oss}$	Output Capacitance			125	170	
$C_{rss}$	Reverse Transfer Capacitance			35	55	
$R_g$	Gate Resistance	$V_{DS} = 15\text{mV}, f = 1\text{MHz}$		3.1		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 4.4\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 24\Omega$		11	20	ns
$t_r$	Rise Time			25	40	
$t_{d(off)}$	Turn-Off Delay Time			35	56	
$t_f$	Fall Time			26	42	
$Q_g$	Total Gate Charge	$V_{GS} = 10\text{V}$		13	17	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 50\text{V}$		3.6		
$Q_{gd}$	Gate to Drain "Miller" Charge	$I_D = 4.4\text{A}$		3.4		

### Drain-Source Diode Characteristics

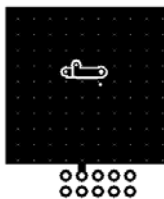
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 4.4\text{A}$			1.25	V
		$V_{GS} = 0\text{V}, I_S = 2.2\text{A}$			1.0	V
$t_{rr}$	Reverse Recovery Time	$I_F = 4.4\text{A}, di/dt = 100\text{A}/\mu\text{s}$			56	ns
$Q_{rr}$	Reverse Recovery Charge				108	

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

(a)  $R_{\theta JA} = 60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB.

(b)  $R_{\theta JA} = 135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.



a.  $60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

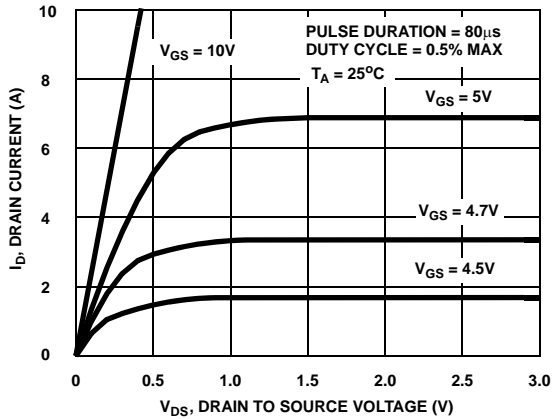


Figure 1. On-Region Characteristics

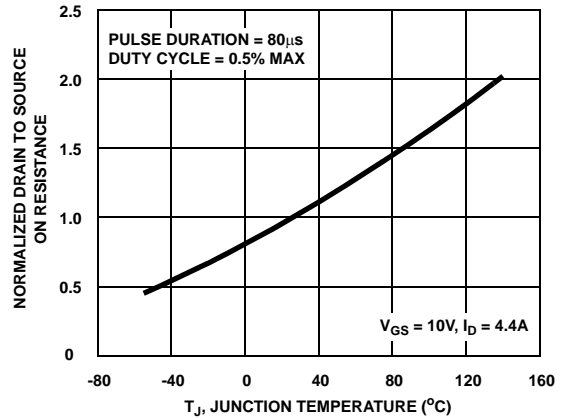


Figure 2. Normalized On-Resistance vs Junction Temperature

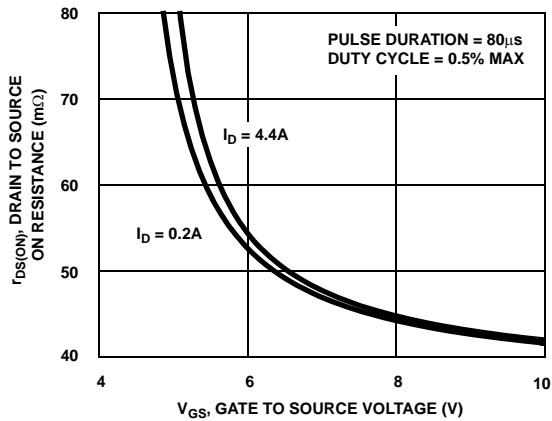


Figure 3. On-Resistance vs Gate to Source Voltage

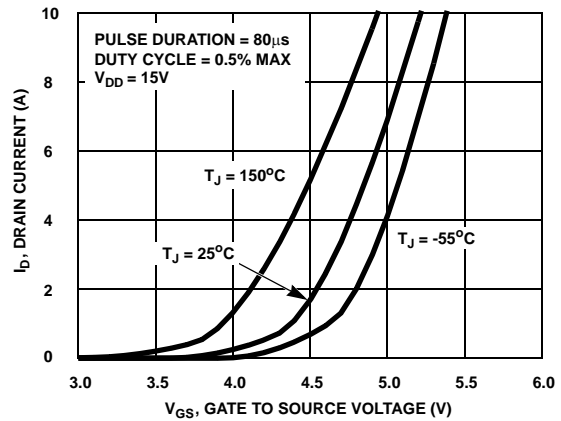


Figure 4. Transfer Characteristics

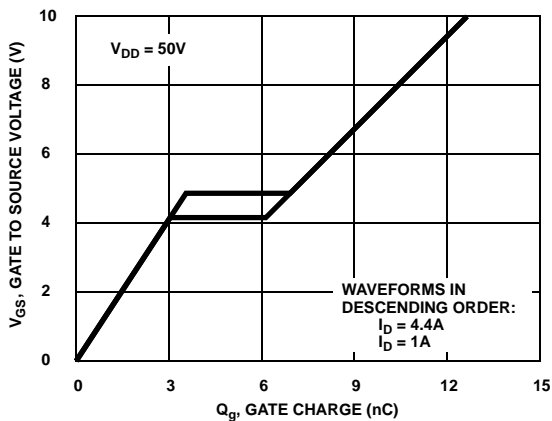


Figure 5. Gate Charge Characteristics

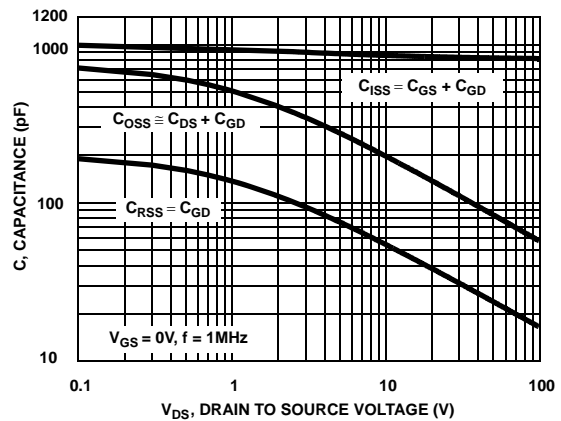
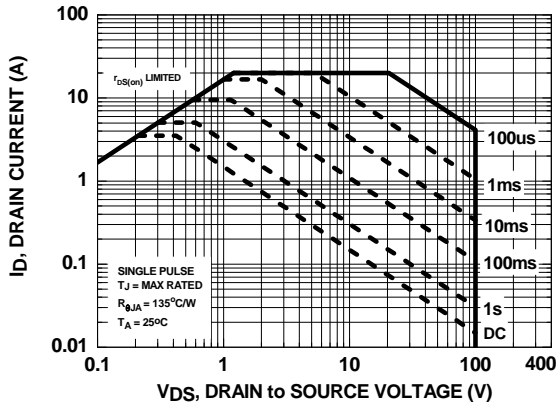
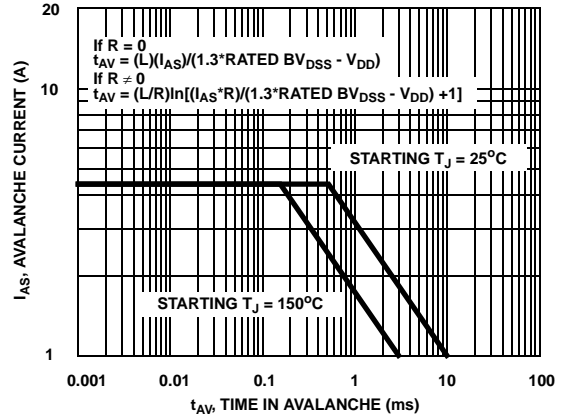


Figure 6. Capacitance vs Drain to Source Voltage

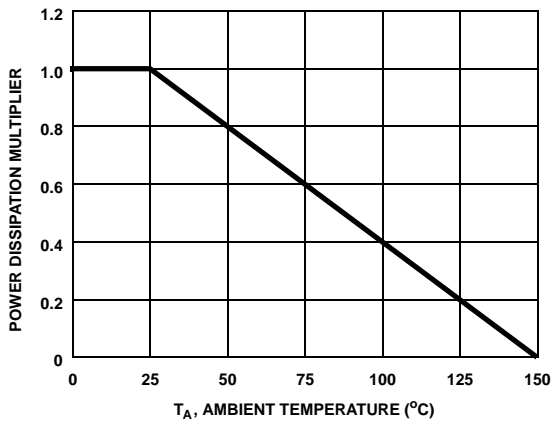
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



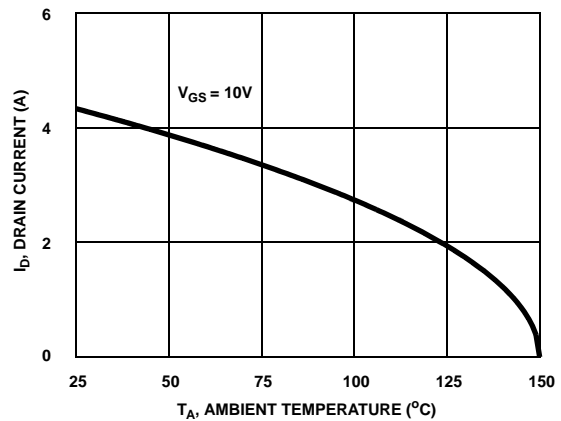
**Figure 7. Forward Bias Safe Operating Area**



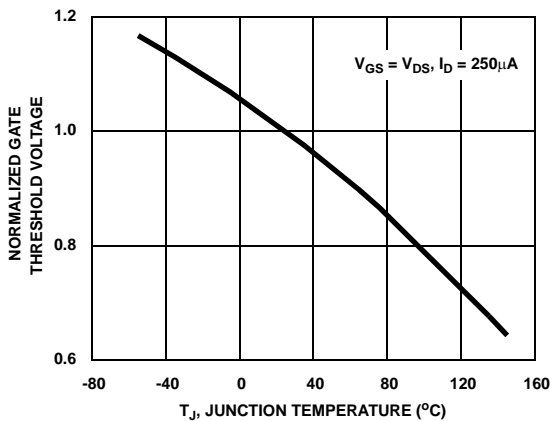
**Figure 8. Uncalamped Inductive Switching Capability**



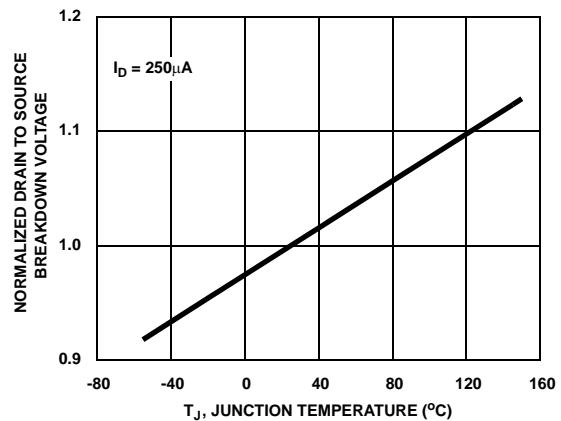
**Figure 9. Normalized Power dissipation vs Ambient Temperature**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**



**Figure 11. Normalized Gate Threshold voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

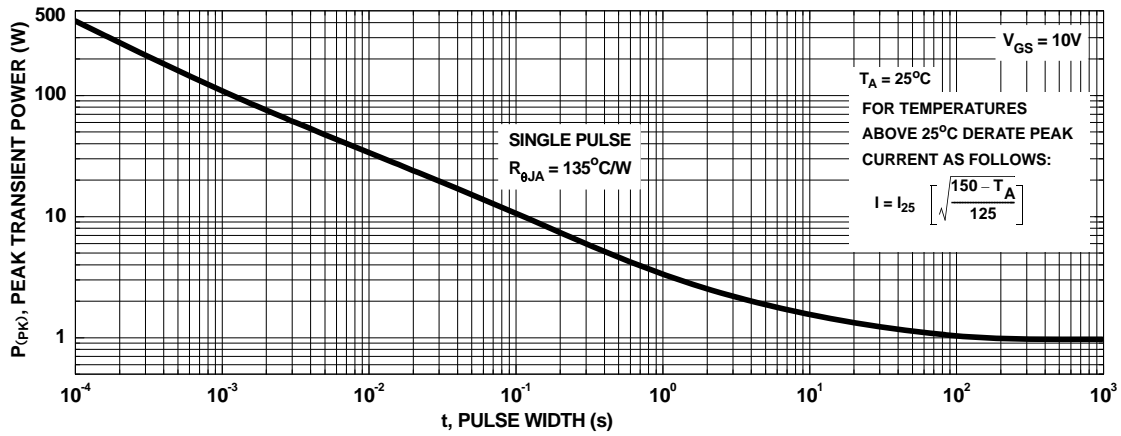


Figure 13. Peak Current Capability

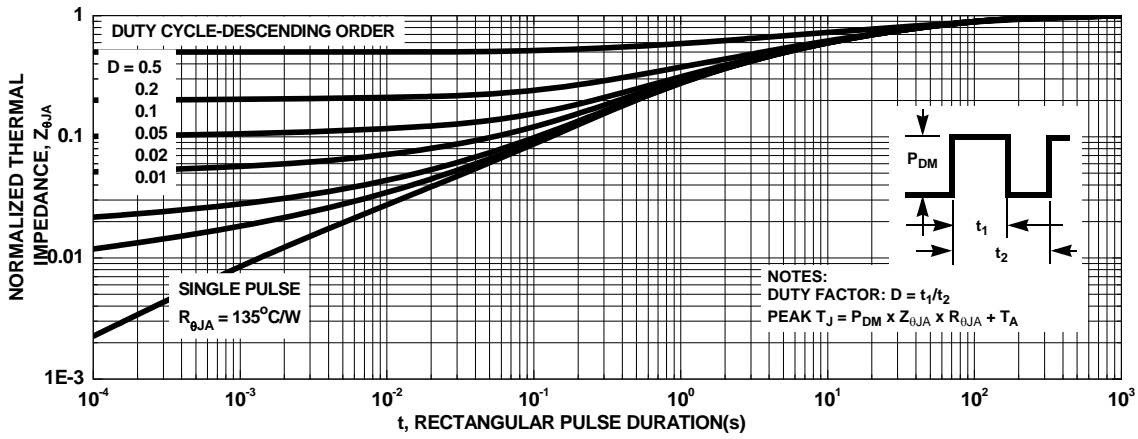
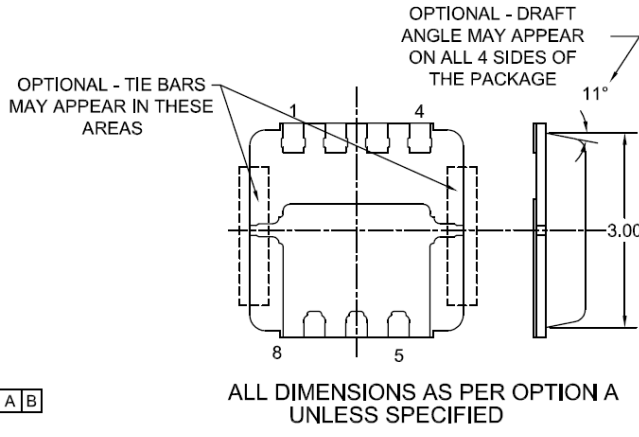
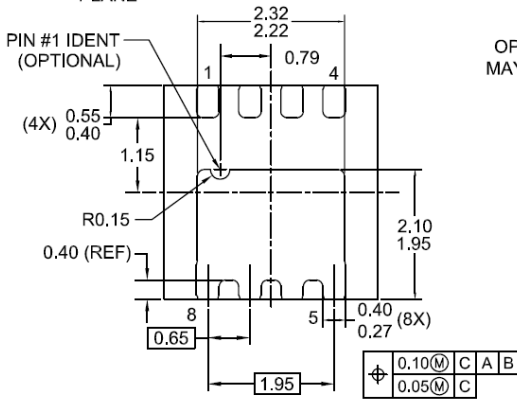
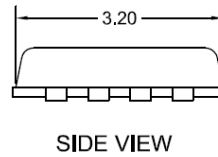
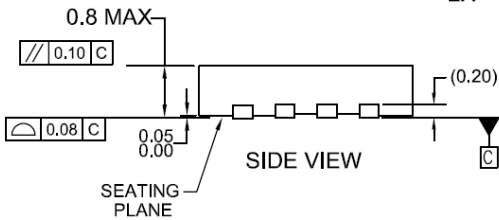
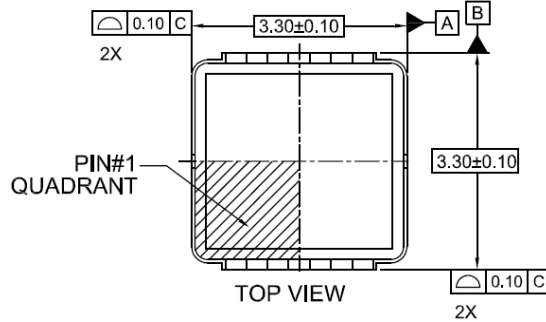
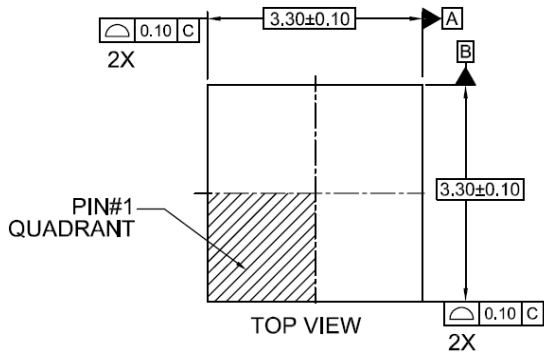
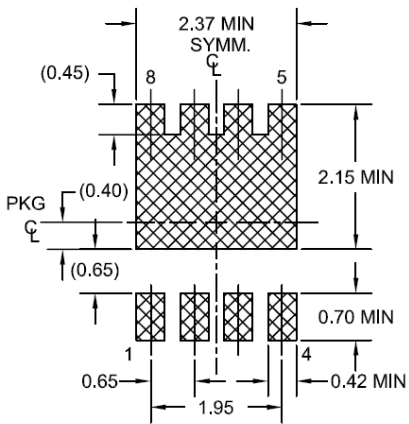


Figure 14. Transient Thermal Response Curve

### Dimensional Outline and Pad Layout



ALL DIMENSIONS AS PER OPTION A UNLESS SPECIFIED







**NOTES:**

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. DIMENSIONS DOES NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
- E. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- F. DRAWING FILENAME:



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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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