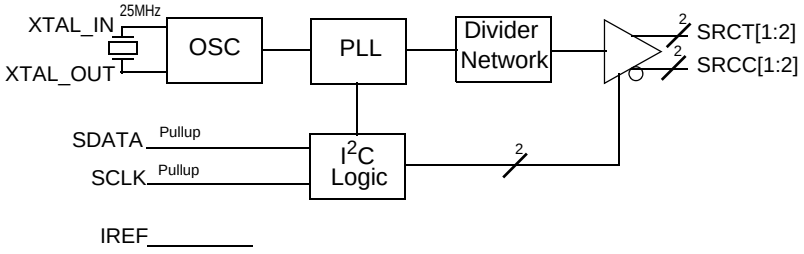
## General Description

The 841S102 is a PLL-based clock synthesizer specifically designed for PCI_Express™ Clock applications. This device generates a 100MHz differential HCSL clock from an input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. An external reference is applied to the XTAL_IN pin with the XTAL_OUT pin left floating.The device offers spread spectrum clock output for reduced EMI applications. An $I^2C$ bus interface is used to enable or disable spread spectrum operation as well as select either a down spread value of -0.35% or -0.5%.The 841S102 is available in a lead-free package.

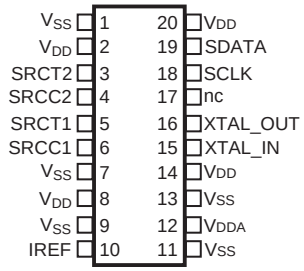
## Features

- Two 0.7V current mode differential HCSL output pairs
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz
- RMS phase jitter @ 100MHz (12kHz – 20MHz): 1.23ps (typical)
- Cycle-to-cycle jitter: 20ps (maximum)
- $I^2C$ support with readback capabilities up to 400kHz
- Spread Spectrum for electromagnetic interference (EMI) reduction
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) package
- PCI Express Gen 1, 2 and 3 jitter compliant

## Block Diagram




## Pin Assignment




**841S102**
**20-Lead TSSOP**
**4.4mm x 6.5mm x 0.925mm package body**
**G Package**
**Top View**

# Pin Description and Pin Characteristics Tables

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 7, 9, 11, 13 | $V_{SS}$ | Power | | Power supply ground. |
| 2, 8, 14, 20 | $V_{DD}$ | Power | | Power supply pins. |
| 3, 4 | SRCT2, SRCC2 | Output | | Differential output pair. HCSL interface levels. |
| 5, 6 | SRCT1, SRCC1 | Output | | Differential output pair. HCSL interface levels. |
| 10 | IREF | Input | | An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode SRCCx, SRCTx clock outputs. |
| 12 | $V_{DDA}$ | Power | | Analog supply for PLL. |
| 15, 16 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 17 | nc | Unused | | No connect. |
| 18 | SCLK | Input | Pullup | $I^2C$ compatible SCLK. This pin has an internal pullup resistor. Open drain. LVCMOS/LVTTL interface levels. |
| 19 | SDATA | I/O | Pullup | $I^2C$ compatible SDATA. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal $I^2C$ serial interface is provided. Through the Serial Data Interface, various device functions, such as clock output buffers, can be individually enabled or disabled. The registers associated with the serial interface initialize to their default setting upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 3A.

The block write and block read protocol is outlined in Table 3B, while Table 3C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 3A.Command Code Definition**

| Bit | Description |
|---|---|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation. |
| 6:5 | Chip select address, set to “00” to access device. |
| 4:0 | Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be “00000”. |

**Table 3B. Block Read and Block Write Protocol**

| Bit | Description = Block Write | Bit | Description = Block Read |
|---|---|---|---|
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits | 11:18 | Command Code - 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29:36 | Data byte 1 - 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 2 - 8 bits | 30:37 | Byte Count from slave - 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte/Slave Acknowledges | 39:46 | Data Byte 1 from slave - 8 bits |
| | Data Byte N - 8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 48:55 | Data Byte 2 from slave - 8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data Bytes from Slave/Acknowledge |
| | | | Data Byte N from slave - 8 bits |
| | | | Not Acknowledge |

**Table 3C. Byte Read and Byte Write Protocol**

| Bit | Description = Byte Write | Bit | Description = Byte Read |
|---|---|---|---|
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits | 11:18 | Command Code - 8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data Byte - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data from slave - 8 bits |
| | | 38 | Not Acknowledge |
| | | 39 | Stop |

## Control Registers

**Table 3D. Byte 0: Control Register 0**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 1 | Reserved | Reserved |
| 5 | 1 | Reserved | Reserved |
| 4 | 1 | SRC[T/C]2 | SRC[T/C]2 Output Enable<br>0 = Disable (Hi-Z)<br>1 = Enable |
| 3 | 1 | SRC[T/C]1 | SRC[T/C]1 Output Enable<br>0 = Disable (Hi-Z)<br>1 = Enable |
| 2 | 1 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

NOTE: Pup denotes Power-up.

**Table 3E. Byte 1: Control Register 1**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3F. Byte 2: Control Register 2**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | SRCT/C | Spread Spectrum Selection<br>0 = -0.35%, 1 = - 0.5% |
| 6 | 1 | Reserved | Reserved |
| 5 | 1 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 0 | SRC | SRC Spread Spectrum Enable<br>0 = Spread Off,<br>1 = Spread On |
| 1 | 1 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3G. Byte 3:Control Register 3**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 1 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 1 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 1 | Reserved | Reserved |
| 2 | 1 | Reserved | Reserved |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Table 3H. Byte 4: Control Register 4**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

**Table 3I. Byte 5: Control Register 5**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | Reserved | Reserved |
| 6 | 0 | Reserved | Reserved |
| 5 | 0 | Reserved | Reserved |
| 4 | 0 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 0 | Reserved | Reserved |
| 0 | 0 | Reserved | Reserved |

**Table 3J. Byte 6: Control Register 6**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | TEST_SEL | REF/N or Hi-Z Select<br>0 = Hi-Z, 1 = REF/N |
| 6 | 0 | TEST_MODE | TEST Clock<br>Mode Entry Control<br>0 = Normal Operation,<br>1 = REF/N or Hi-Z Mode |
| 5 | 0 | Reserved | Reserved |
| 4 | 1 | Reserved | Reserved |
| 3 | 0 | Reserved | Reserved |
| 2 | 0 | Reserved | Reserved |
| 1 | 1 | Reserved | Reserved |
| 0 | 1 | Reserved | Reserved |

NOTE: Pup denotes Power-up.

**Table 3K. Byte 7: Control Register 7**

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | 0 | | Revision Code Bit 3 |
| 6 | 0 | | Revision Code Bit 2 |
| 5 | 0 | | Revision Code Bit 1 |
| 4 | 0 | | Revision Code Bit 0 |
| 3 | 0 | | Vendor ID Bit 3 |
| 2 | 0 | | Vendor ID Bit 2 |
| 1 | 0 | | Vendor ID Bit 1 |
| 0 | 1 | | Vendor ID Bit 0 |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 81.3°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.22 | 3.3 | $V_{DD}$ | V |
| $I_{DD}$ | Power Supply Current | | | | 80 | mA |
| $I_{DDA}$ | Analog Supply Current | | | | 22 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | SDATA, SCLK | | 2.2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | SDATA, SCLK | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | SDATA, SCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 10 | µA |
| $I_{IL}$ | Input Low Current | SDATA, SCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 6A. PCI Express Jitter Specifications, $V_{DD}$ = 3.3V±5%, $T_A$ = -40°C to 85°C**

| Parameter | Symbol | Test Conditions | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---|---|---|---|---|---|---|---|
| $t_j$ (PCIe Gen 1) | Phase Jitter Peak-to-Peak; NOTE 1, 4 | $f$ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 13.3 | 19.3 | 86 | ps |
| $t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f$ = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 1.07 | 1.53 | 3.1 | ps |
| $t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f$ = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 0.19 | 0.32 | 3.0 | ps |
| $t_{REFCLK\_RMS}$ (PCIe Gen 3) | Phase Jitter RMS; NOTE 3, 4 | $f$ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.18 | 0.3 | 0.8 | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the PCI Express Application Note section in the datasheet.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 106 clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

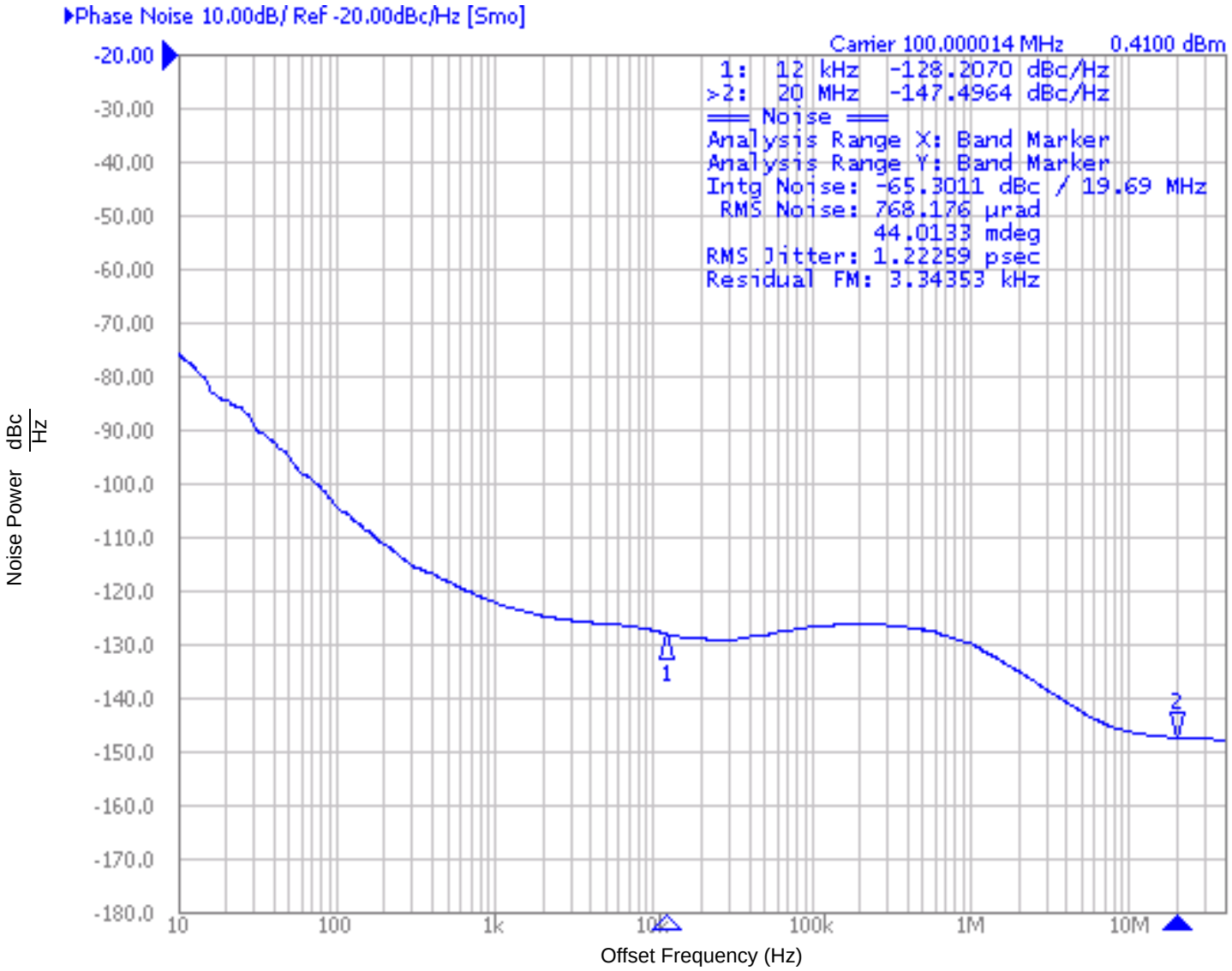
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

**Table 6B. AC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C**

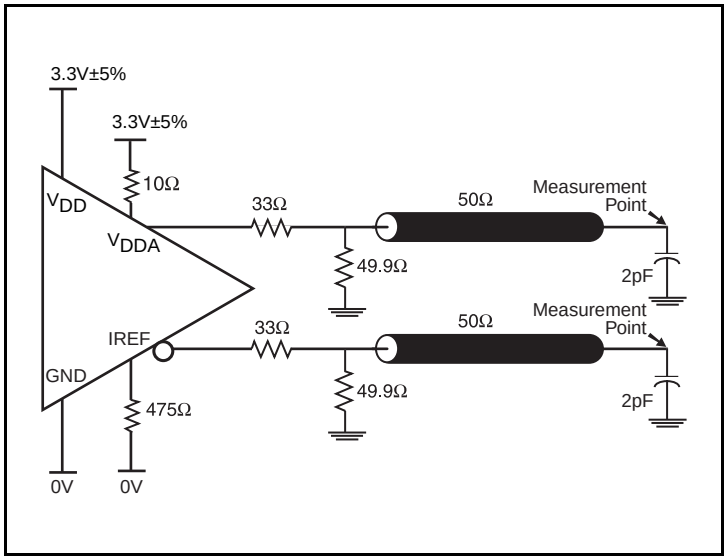
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | 100 | | MHz |
| $f_{REF}$ | Reference frequency | | | 25 | | MHz |
| *t*jit(Ø) | Phase Jitter, RMS (Random); NOTE 1 | 25MHz crystal, *ƒ* = 100MHz, Integration Range: 12kHz – 20MHz | | 1.23 | | ps |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | | 35 | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 2 | PLL Mode | | | 20 | ps |
| $t_L$ | PLL Lock Time | | | | 55 | ms |
| $F_M$ | SSC Modulation Frequency; NOTE 4 | 25MHz Crystal | 30 | 32 | 33.33 | kHz |
| $SSC_{RED}$ | Spectral Reduction; NOTE 4 | | -7 | -10 | | dB |
| $V_{RB}$ | Ring-back Voltage Margin; NOTE 5, 6 | | -100 | | 100 | mV |
| $V_{MAX}$ | Absolute Max. Output Voltage; NOTE 7, 8 | | | | 1150 | mV |
| $V_{MIN}$ | Absolute Min. Output Voltage; NOTE 7, 9 | | -300 | | | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage; NOTE 7, 10, 11 | | 250 | | 550 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all edges; NOTE 7, 10, 12 | | | | 140 | mV |
| | Rise/Fall Edge Rate; NOTE 7, 13 | Measured between 150mV to +150mV | 0.6 | | 4.0 | V/ns |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz quartz crystal.
NOTE 1: Refer to phase jitter plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 4: Spread Spectrum clocking enabled.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: $T_{STABLE}$ is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the VRB ±100mV differential range.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of SRCT equals the falling edge of SRCC.
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising SRCT and falling SRCC, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (SRCT minus SRCC). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

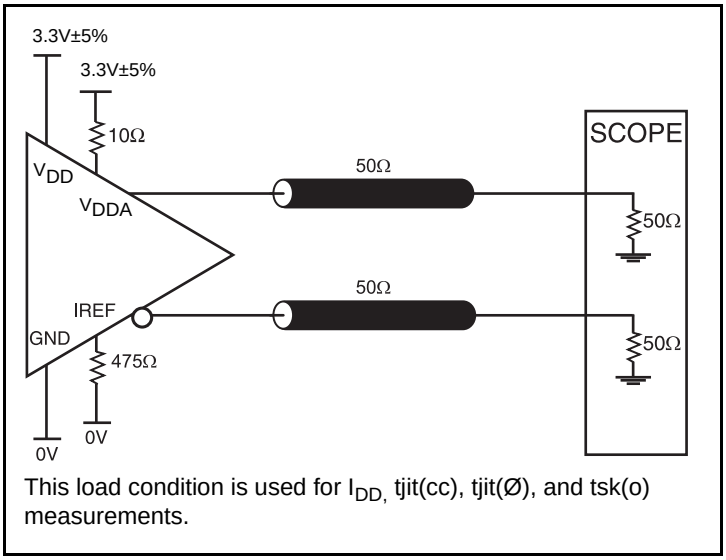
## Typical Phase Noise at 100MHz



## Parameter Measurement Information

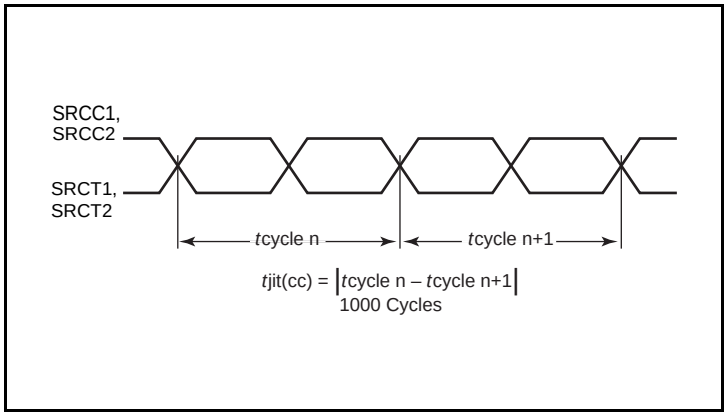



**3.3V HCSL Output Load Test Circuit**

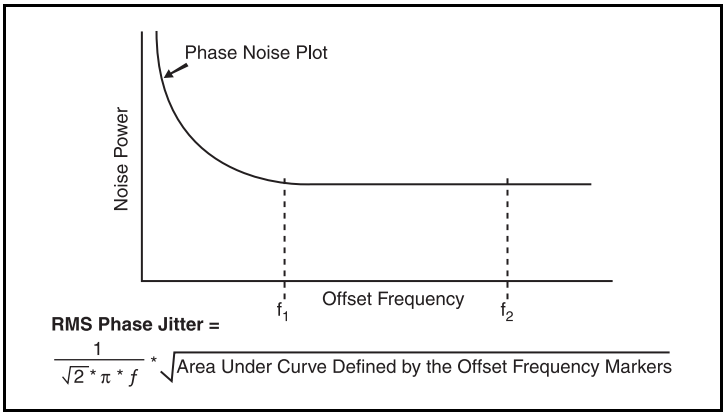



This load condition is used for $I_{DD,}$ tjit(cc), tjit(Ø), and tsk(o) measurements.

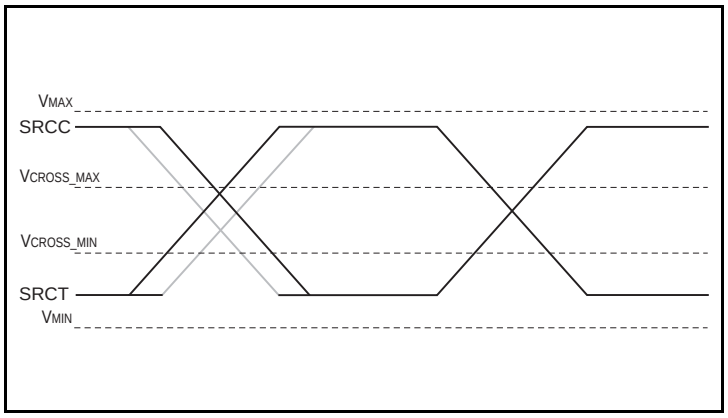
**3.3V HCSL Output Load Test Circuit**



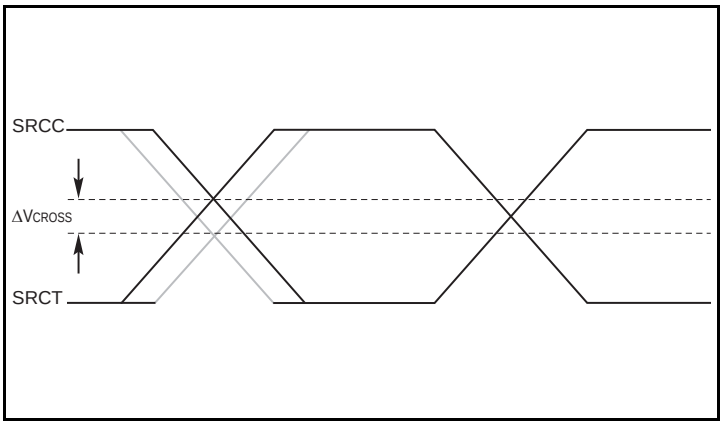

**Cycle-to-Cycle Jitter**




**RMS Phase Jitter**

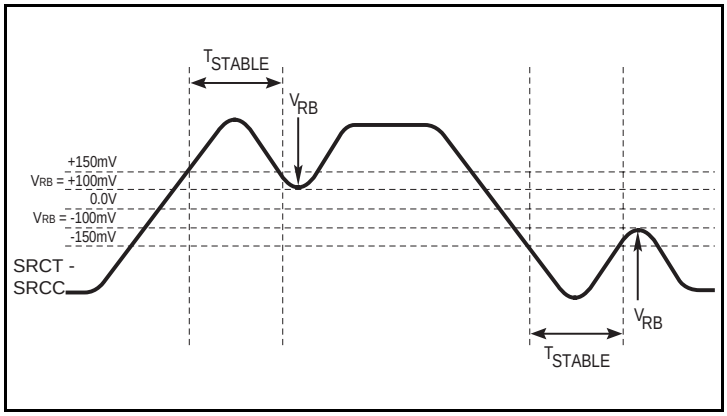



**Single-ended Measurement Points for Absolute Cross Point and Swing**

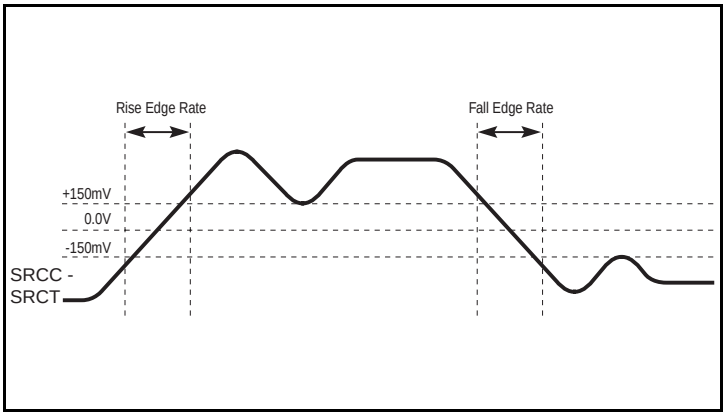



**Single-ended Measurement Points for Delta Cross Point**

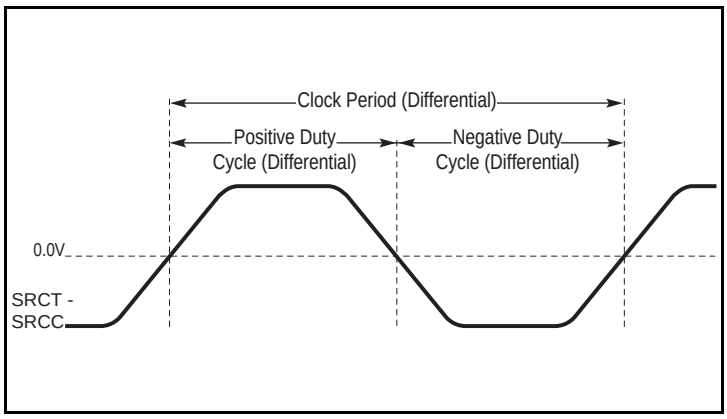
## Parameter Measurement Information, continued




**Differential Measurement Points for Ringback**




**Differential Measurement Points for Rise/Fall Edge Rate**




**Differential Measurement Points for Duty Cycle/Period**

# Applications Information

## Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841S102 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$ and $V_{DDA}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{DD}$ pin and also shows that $V_{DDA}$ requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{DDA}$ pin.

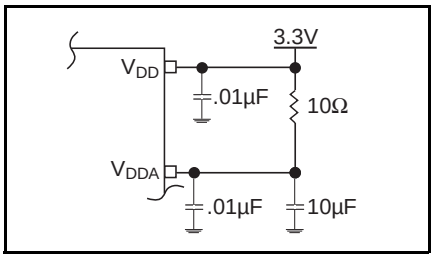



**Figure 1. Power Supply Filtering**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The 841S102 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

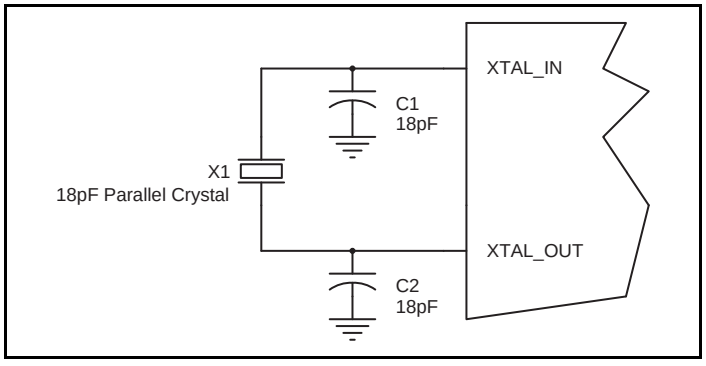



**Figure 2. Crystal Input Interface**

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

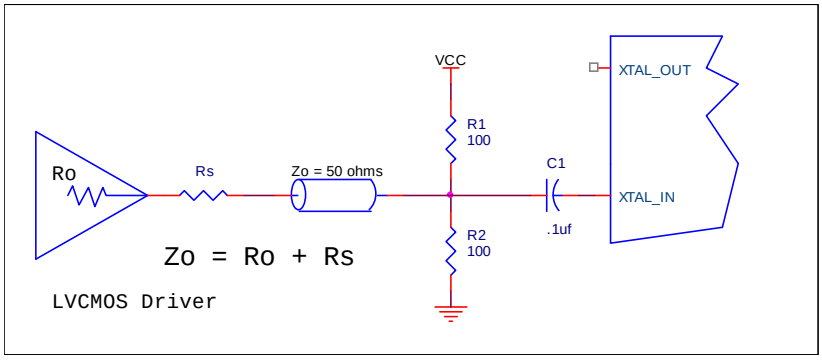



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

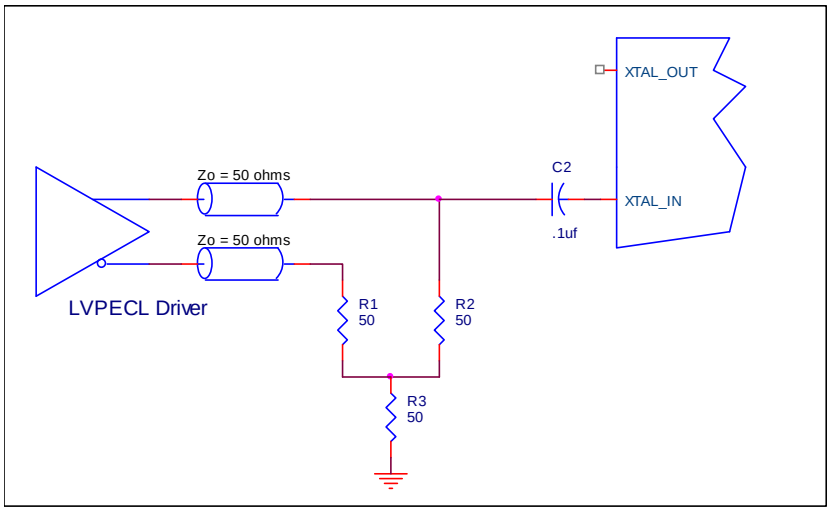



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Recommended Termination

*Figure 4A* is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

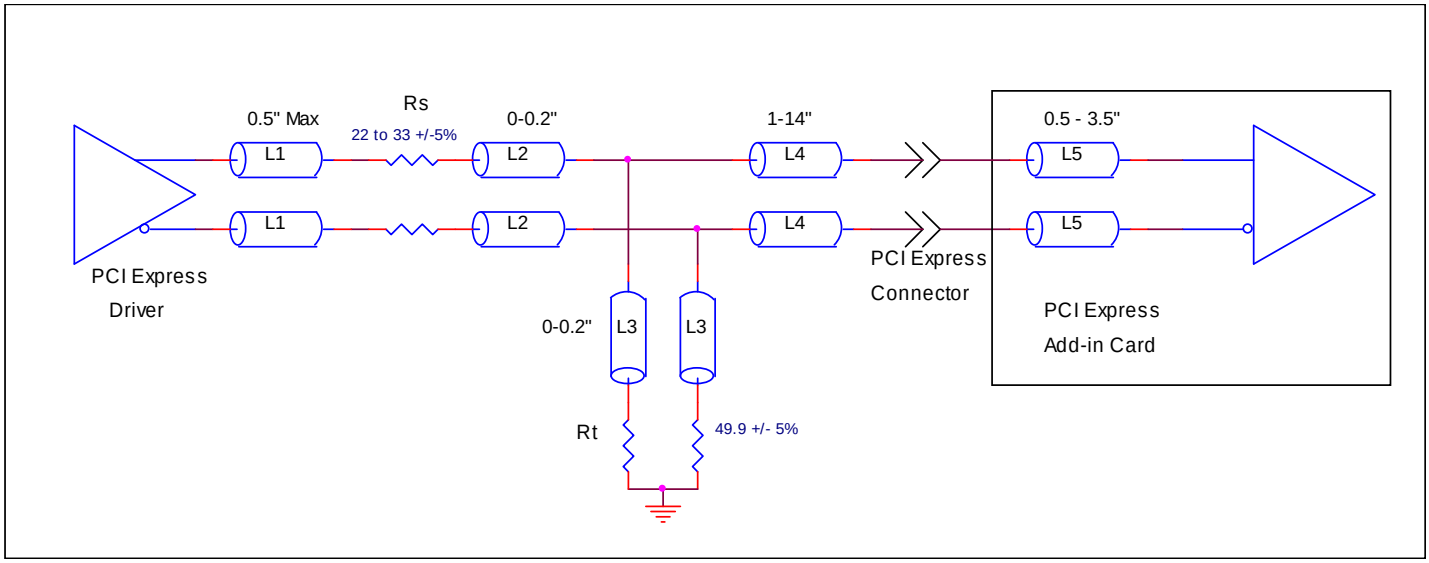



**Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

*Figure 4B* is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

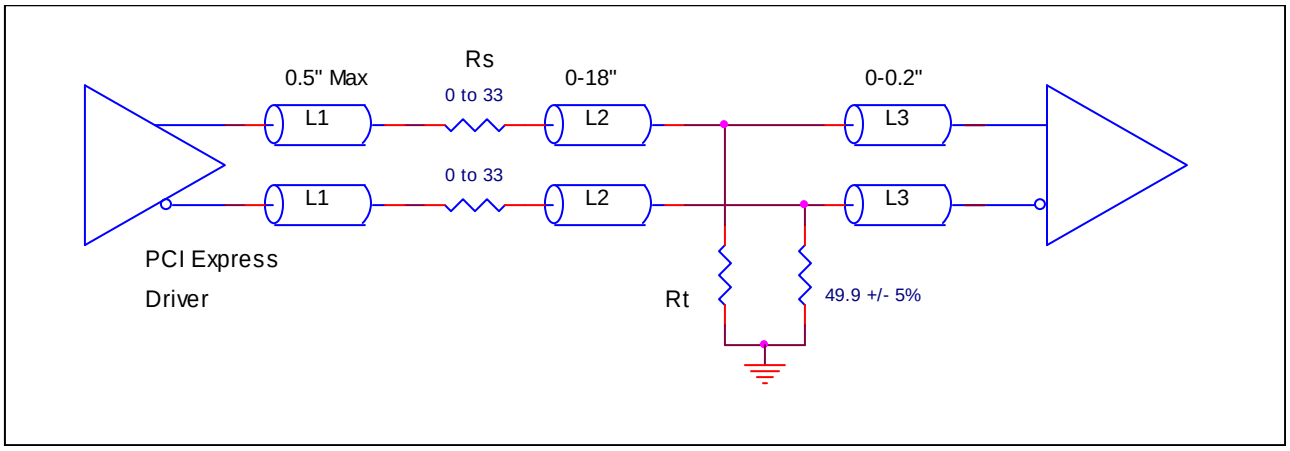



**Figure 4B. Recommended Termination (where a point-to-point connection can be used)**

## PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

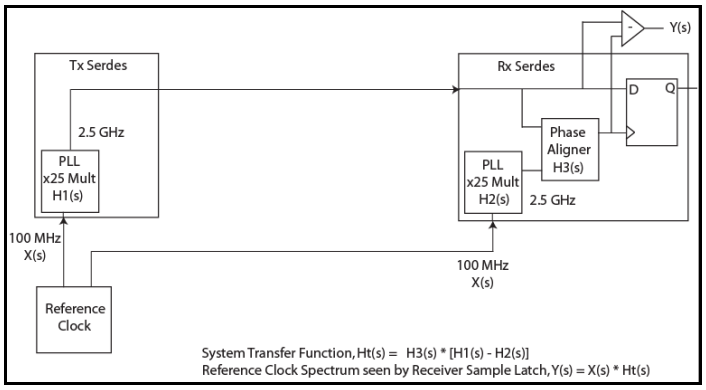
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

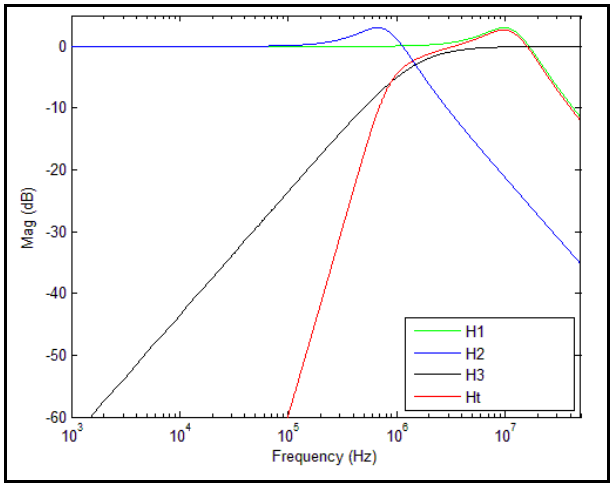
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



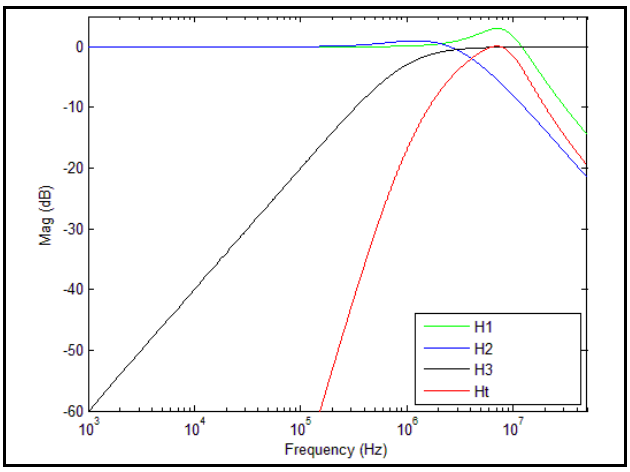

**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

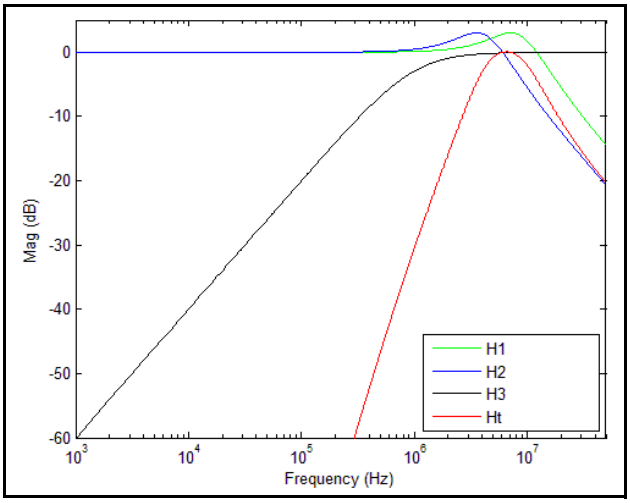



**PCIe Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

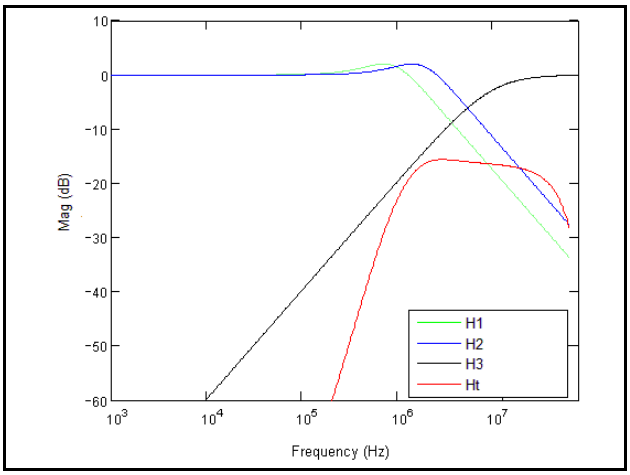



**PCIe Gen 2A Magnitude of Transfer Function**




**PCIe Gen 2B Magnitude of Transfer Function**

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.




**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

## Schematic Layout

Figure 5 shows an example of the 841S102 application schematic where the device is operated at $V_{DD}$ = 3.3V with an 18pF parallel resonant 25MHz crystal. The schematic focuses on functional connections and is intended as an example only and may not represent the exact user configuration. For example the $I^2C$ bus connections are shown as optionally provided via a two pin header whereas they could just as easily be driven from an FPGA. Two types of HCSL termination are shown in this schematic; one for PCIe add-in cards and one for point to point connections, which are connections on the same PCB as the 841S102.

Tuning caps C1 and C2 are required for frequency accuracy. C1 = C2 = 18pF are used in this example as typical values, but their value may be adjusted slightly up or down to optimize the oscillator frequency accuracy. When routing the load caps be sure to keep all routing on the top layer. Route the ground connection of C1 and C2 together and then to a ground at the 841S102. Do not share the tuning capacitor ground with any other ground, that is ensure that only crystal current circulates in the tuning capacitors.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the $V_{DD}$ pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor on the $V_{DD}$ pin must be placed on the device side with direct return to the ground plane though vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter component recommendations are a general guideline to be used for reducing external noise from coupling into the devices.The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

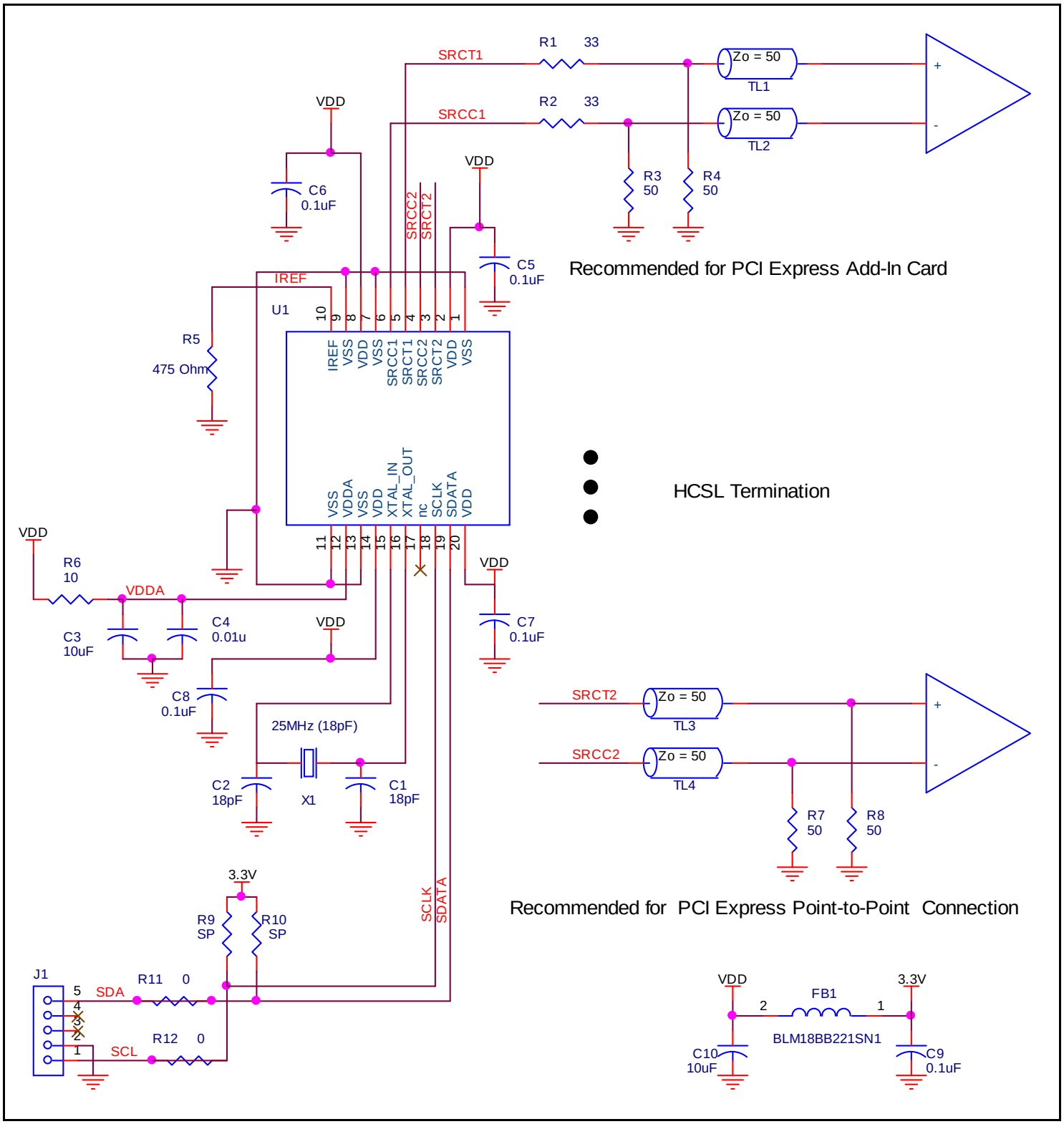



**Figure 5. 841S102 Application Schematic.**

## Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.35% or 0.5% down-spread from the nominal 100MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 6A* below.

The 841S102 triangle modulation frequency deviation is either 0.35% or 0.5% down-spread from the nominal clock frequency.

An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 6B.* The ratio of this difference to the fundamental frequency is typically 0.35% or 0.5%. The resulting spectral reduction will be greater than 7dB, as shown in *Figure 6B*. It is important to note the 841S102 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

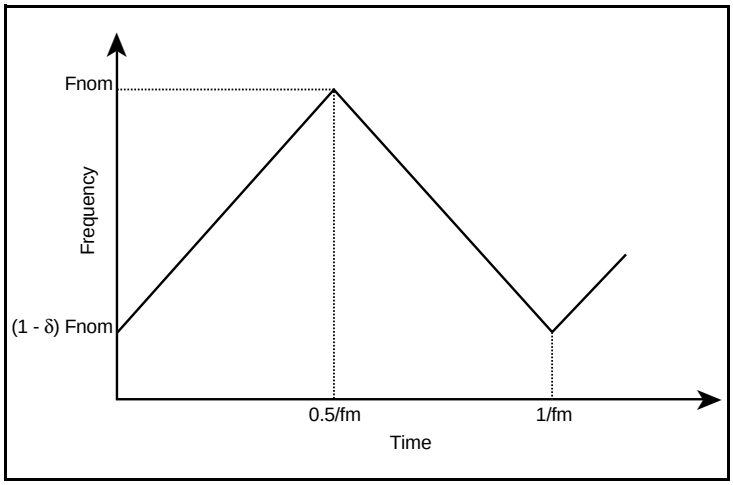



**Figure 6A. Triangle Frequency Modulation**

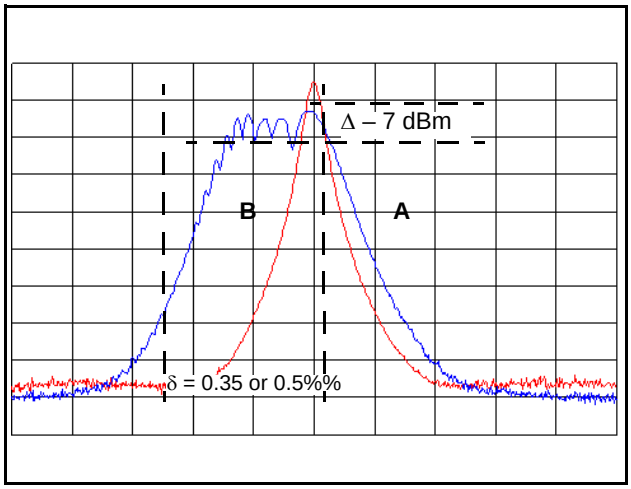



**Figure 6B. 100MHz Typical Clock Output In Frequency Domain**
**(A) Spread-Spectrum OFF**
**(B) Spread-Spectrum ON**

# Power Considerations

This section provides information on power dissipation and junction temperature for the 841S102.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 841S102 is the sum of the core power plus the analog, plus the power dissipated due to loading.
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.
The maximum current at 85°C is as follows:
$I_{DD\_MAX}$ = 75mA
$I_{DDA\_MAX}$ = 20mA

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * ($I_{DD\_MAX}$ + $I_{DDA\_MAX}$) = 3.465V *(75mA + 20mA) = **329.175mW**
- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 44.5mW = **89mW**

**Total Power**$_{\_MAX}$ = 329.175mW + 89mW = **418.175mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.418W * 81.3°C/W = 119°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 81.3°C/W | 76.9°C/W | 74.8°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 7.*

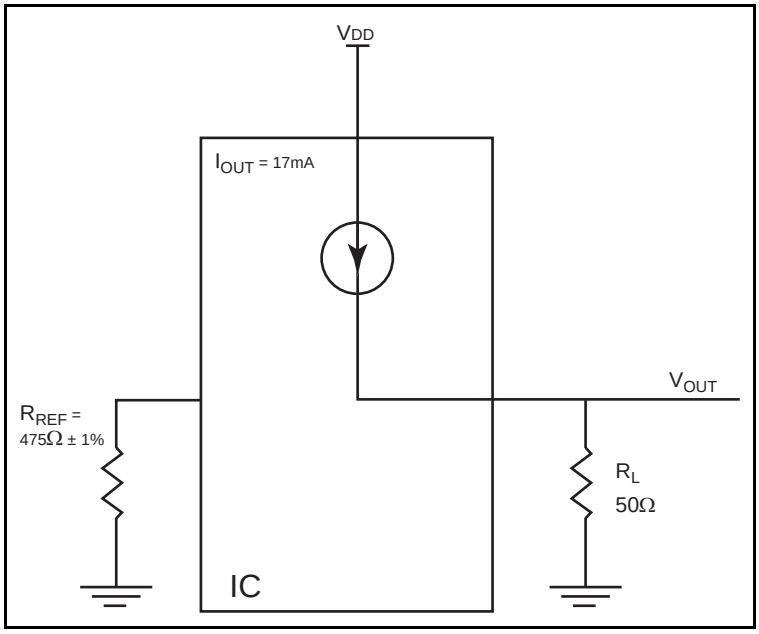



**Figure 7. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DD\_MAX}$.

Power = $(V_{DD\_MAX} – V_{OUT}) * I_{OUT}$,
since $V_{OUT} – I_{OUT} * R_L$

= $(V_{DD\_MA} – I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 81.3°C/W | 76.9°C/W | 74.8°C/W |

## Transistor Count

The transistor count for 841S102 is: 11,775

# Package Outline and Package Dimensions

**Package Outline - G Suffix for 20 Lead TSSOP**

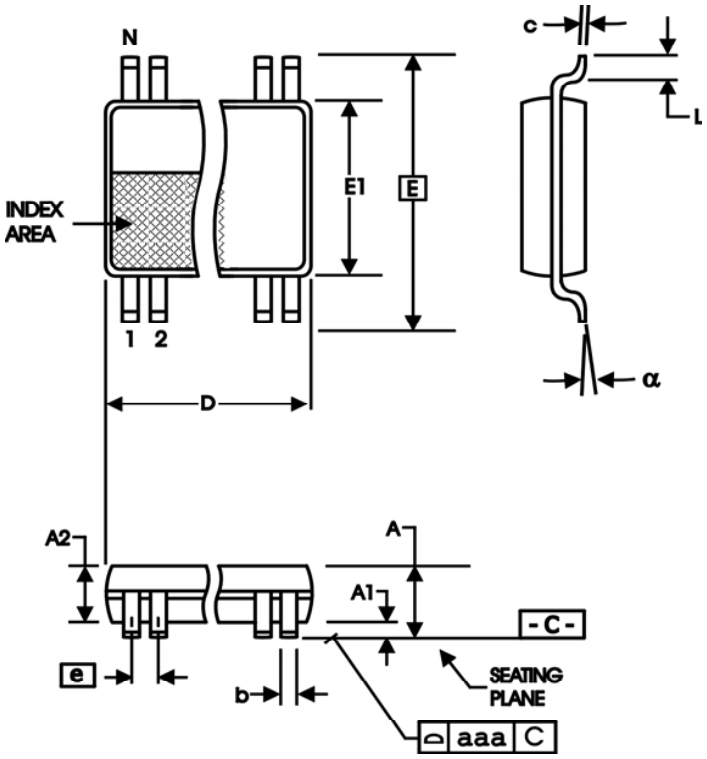



**Table 9. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| α | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 841S102EGILF | ICS41S102EIL | “Lead-Free” 20 Lead TSSOP | Tube | -40°C to 85°C |
| 841S102EGILFT | ICS41S102EIL | “Lead-Free” 20Lead TSSOP | Tape & Reel | -40°C to 85°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | | 13<br>14<br>16, 17<br>18 | Updated the “Overdriving the XTAL Interface” note.<br>Updated the termination note.<br>Updated schematic and text.<br>Spread Spectrum note, second paragraph: The 841S102 triangle modulation frequency deviation is Either 0.35% Or 0.5% down-spread from the nominal clock frequency | 2/8/13 |
| B | | | Updated datasheet header/footer.<br>Deleted “ICS” prefix and “I” suffix in the part number. | 7/7/16 |
| | | | | |

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

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