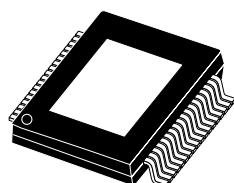
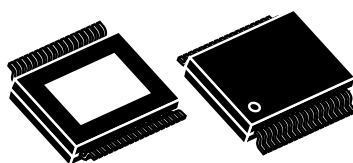


### 20 W + 20 W dual BTL class-D audio amplifier



PowerSSO-36  
exposed pad up



PowerSSO-36 with  
exposed pad down

### Features

- 20 W + 20 W continuous output power:
  - $R_L = 8 \Omega$ , THD = 10% at  $V_{CC} = 18 \text{ V}$
- Wide-range single-supply operation (5 - 18 V)
- High efficiency ( $\eta = 90\%$ )
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential input minimize common-mode noise
- No 'pop' at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- External synchronisation

### Description

The **TDA7491HV** is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-up (EPU) and down (EPD) packages, no separate heatsink is required.

The **TDA7491HV** is pin-to-pin compatible with the TDA7491P and TDA7491LP.

#### Product status link

[TDA7491HV](#)

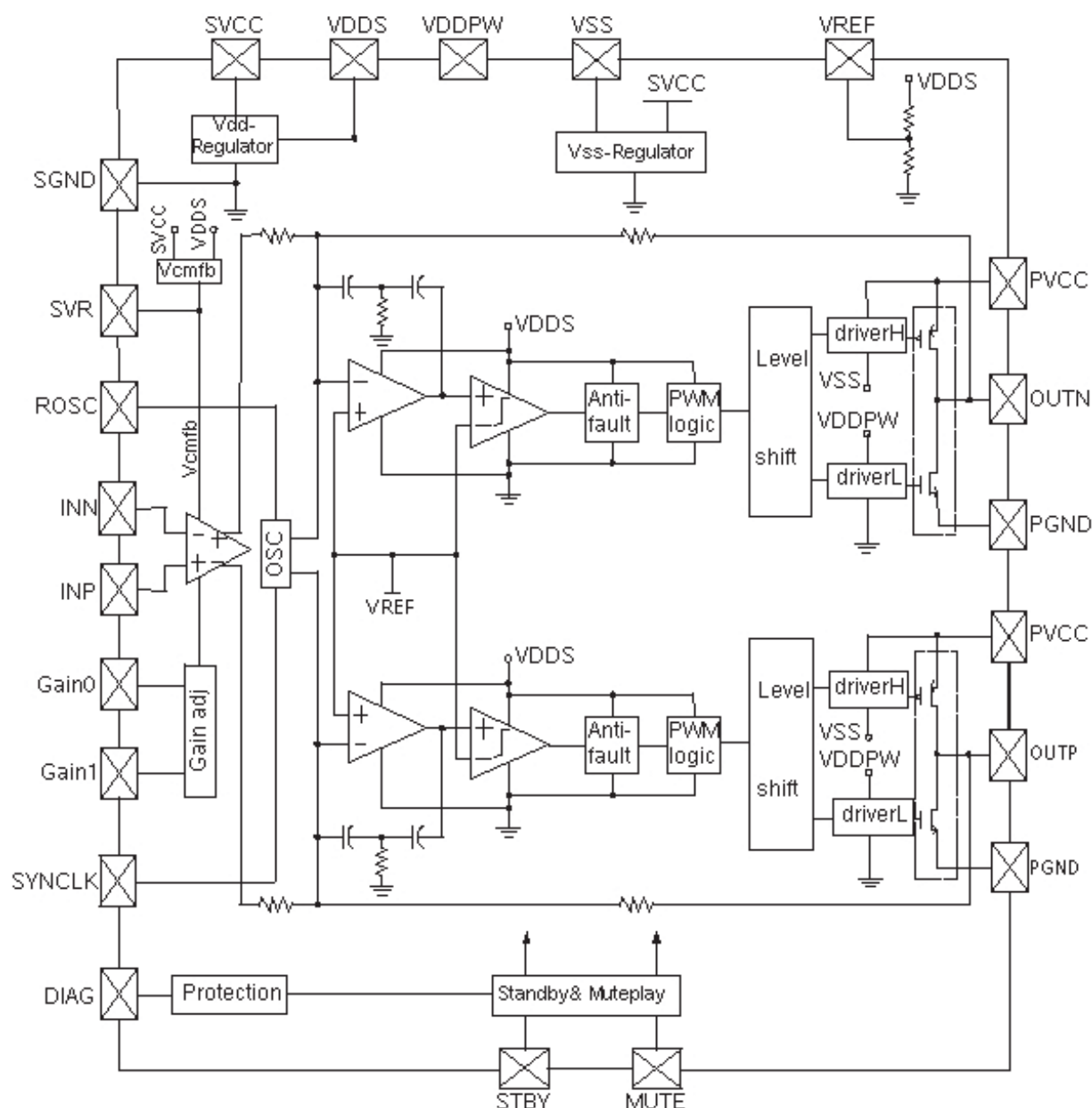
#### Product summary

|                   |                 |
|-------------------|-----------------|
| Order code        | TDA7491HV13TR   |
| Package           | PowerSSO-36 EPD |
| Order code        | TDA7491HVU13TR  |
| Package           | PowerSSO-36 EPU |
| Packing           | Tape and reel   |
| Temperature range | -40 to 85 °C    |

# 1 Device block diagram

Figure 1. Internal block diagram (showing one channel only) shows the block diagram of one of the two identical channels of the TDA7491HV.

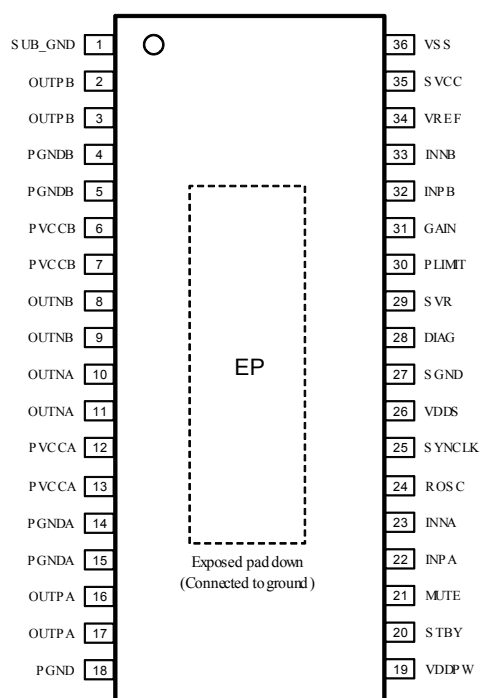
Figure 1. Internal block diagram (showing one channel only)



## 2 Pin description

### 2.1 Pinout (EPD)

**Figure 2. Pin connections (top view, PCB view)**



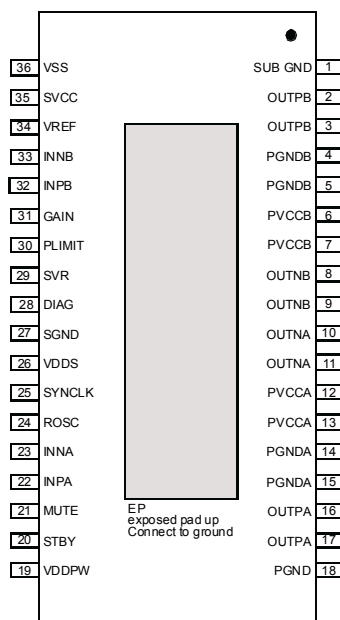
## 2.2 Pin list (EPD)

**Table 1. Pin description list**

| Number | Name    | Type | Description                                                           |
|--------|---------|------|-----------------------------------------------------------------------|
| 1      | SUB_GND | PWR  | Connect to the frame                                                  |
| 2,3    | OUTPB   | O    | Positive PWM for right channel                                        |
| 4,5    | PGNDB   | PWR  | Power stage ground for right channel                                  |
| 6,7    | PVCCB   | PWR  | Power supply for right channel                                        |
| 8,9    | OUTNB   | O    | Negative PWM output for right channel                                 |
| 10,11  | OUTNA   | O    | Negative PWM output for left channel                                  |
| 12,13  | PVCCA   | PWR  | Power supply for left channel                                         |
| 14,15  | PGNDA   | PWR  | Power stage ground for left channel                                   |
| 16,17  | OUTPA   | O    | Positive PWM output for left channel                                  |
| 18     | PGND    | PWR  | Power stage ground                                                    |
| 19     | VDDPW   | O    | 3.3-V (nominal) regulator output referred to ground for power stage   |
| 20     | STBY    | I    | Standby mode control                                                  |
| 21     | MUTE    | I    | Mute mode control                                                     |
| 22     | INPA    | I    | Positive differential input of left channel                           |
| 23     | INNA    | I    | Negative differential input of left channel                           |
| 24     | ROSC    | O    | Master oscillator frequency-setting pin                               |
| 25     | SYNCLK  | I/O  | Clock in/out for external oscillator                                  |
| 26     | VDDS    | O    | 3.3-V (nominal) regulator output referred to ground for signal blocks |
| 27     | SGND    | PWR  | Signal ground                                                         |
| 28     | DIAG    | O    | Open-drain diagnostic output                                          |
| 29     | SVR     | O    | Supply voltage rejection                                              |
| 30     | GAIN0   | I    | Gain setting input 1                                                  |
| 31     | GAIN1   | I    | Gain setting input 2                                                  |
| 32     | INPB    | I    | Positive differential input of right channel                          |
| 33     | INNBB   | I    | Negative differential input of right channel                          |
| 34     | VREF    | O    | Half VDDS (nominal) referred to ground                                |
| 35     | SVCC    | PWR  | Signal power supply                                                   |
| 36     | VSS     | O    | 3.3-V (nominal) regulator output referred to power supply             |
| -      | EP      | -    | Exposed pad for heatsink, to be connected to GND                      |

## 2.3 Pinout (EPU)

**Figure 3. Pin connections (top view, PCB view)**



## 2.4 Pin list (EPU)

**Table 2. Pin description list**

| Number | Name    | Type | Description                                                           |
|--------|---------|------|-----------------------------------------------------------------------|
| 1      | SUB_GND | PWR  | Connect to the frame                                                  |
| 2, 3   | OUTPB   | O    | Positive PWM for right channel                                        |
| 4, 5   | PGNDB   | PWR  | Power stage ground for right channel                                  |
| 6, 7   | PVCCB   | PWR  | Power supply for right channel                                        |
| 8, 9   | OUTNB   | O    | Negative PWM output for right channel                                 |
| 10, 11 | OUTNA   | O    | Negative PWM output for left channel                                  |
| 12, 13 | PVCCA   | PWR  | Power supply for left channel                                         |
| 14, 15 | PGNDA   | PWR  | Power stage ground for left channel                                   |
| 16, 17 | OUTPA   | O    | Positive PWM output for left channel                                  |
| 18     | PGND    | PWR  | Power stage ground                                                    |
| 19     | VDDPW   | O    | 3.3 V (nominal) regulator output referred to ground for power stage   |
| 20     | STBY    | I    | Standby mode control                                                  |
| 21     | MUTE    | I    | Mute mode control                                                     |
| 22     | INPA    | I    | Positive differential input of left channel                           |
| 23     | INNA    | I    | Negative differential input of left channel                           |
| 24     | ROSC    | O    | Master oscillator frequency-setting pin                               |
| 25     | SYNCLK  | I/O  | Clock in/out for external oscillator                                  |
| 26     | VDDS    | O    | 3.3 V (nominal) regulator output referred to ground for signal blocks |
| 27     | SGND    | PWR  | Signal ground                                                         |
| 28     | DIAG    | O    | Open-drain diagnostic output                                          |
| 29     | SVR     | O    | Supply voltage rejection                                              |
| 30     | PLIMIT  | I    | Output voltage level setting                                          |
| 31     | GAIN    | I    | Gain setting input                                                    |
| 32     | INPB    | I    | Positive differential input of right channel                          |
| 33     | INNB    | I    | Negative differential input of right channel                          |
| 34     | VREF    | O    | Half VDDS (nominal) referred to ground                                |
| 35     | SVCC    | PWR  | Signal power supply                                                   |
| 36     | VSS     | O    | 3.3 V (nominal) regulator output referred to power supply             |
| -      | EP      | -    | Exposed pad for heatsink, to be connected to GND                      |

### 3 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol           | Parameter                                                                      | Value      | Unit |
|------------------|--------------------------------------------------------------------------------|------------|------|
| V <sub>CC</sub>  | DC supply voltage for pins PVCCA, PVCCB                                        | 23         | V    |
| V <sub>I</sub>   | Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1 | -0.3 - 3.6 | V    |
| T <sub>op</sub>  | Operating temperature                                                          | -40 to 85  | °C   |
| T <sub>j</sub>   | Junction temperature                                                           | -40 to 150 | °C   |
| T <sub>stg</sub> | Storage temperature                                                            | -40 to 150 | °C   |

**Table 4. Thermal data**

| Symbol                 | Parameter                                                                               | Min. | Typ. | Max. | Unit |
|------------------------|-----------------------------------------------------------------------------------------|------|------|------|------|
| R <sub>th j-case</sub> | Thermal resistance, junction-to-case                                                    |      | 2    | 3    | °C/W |
| R <sub>th j-amb</sub>  | Thermal resistance, junction-to-ambient (mounted on a recommended PCB) <sup>(1)</sup> . |      | 24   |      |      |

1. FR4 with vias to copper area of 9 cm<sup>2</sup>

## 4 Electrical specifications

Unless otherwise stated, the results in Table 1 below are given for the conditions:  $V_{CC} = 18\text{ V}$ ,  $R_L$  (load) =  $8\ \Omega$ ,  $R_{OSC} = R_3 = 39\text{ k}\Omega$ ,  $C_8 = 100\text{ nF}$ ,  $f = 1\text{ kHz}$ ,  $G_V = 20\text{ dB}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

**Table 5. Electrical specifications**

| Symbol        | Parameter                                | Test conditions                                                            | Min. | Typ. | Max. | Unit             |
|---------------|------------------------------------------|----------------------------------------------------------------------------|------|------|------|------------------|
| $V_{CC}$      | Supply voltage                           |                                                                            | 5    | -    | 18   | V                |
| $I_q$         | Total quiescent current                  |                                                                            | -    | 26   | 35   | mA               |
| $I_{qSTBY}$   | Quiescent current in standby             |                                                                            |      | 2.5  | 5.0  | $\mu\text{A}$    |
| $V_{OS}$      | Output offset voltage                    | Play mode                                                                  | -100 |      | +100 | mV               |
|               |                                          | Mute mode                                                                  | -60  |      | +60  |                  |
| $I_{OCP}$     | Overcurrent protection threshold         | $R_L = 0\ \Omega$                                                          | 3    | 5    | -    | A                |
| $T_j$         | Junction temperature at thermal shutdown |                                                                            |      | 150  |      | $^\circ\text{C}$ |
| $R_i$         | Input resistance                         | Differential input                                                         | 54   | 60   |      | k $\Omega$       |
| $V_{UVP}$     | Undervoltage protection threshold        | -                                                                          |      |      | 4.5  | V                |
| $R_{DS(on)}$  | Power transistor on resistance           | High-side                                                                  |      | 0.2  |      | $\Omega$         |
|               |                                          | Low-side                                                                   |      | 0.2  |      |                  |
| $P_o$         | Output power                             | THD = 10%                                                                  |      | 20   |      | W                |
|               |                                          | THD = 1%                                                                   |      | 16   |      |                  |
| $P_o$         | Output power                             | $R_L = 8\ \Omega$ , THD = 10%, $V_{CC} = 12\text{ V}$                      |      | 7.2  |      | W                |
|               |                                          | $R_L = 6\ \Omega$ , THD = 1% $V_{CC} = 25\text{ V}$                        |      | 4.0  |      |                  |
| $P_D$         | Dissipated power                         | $P_o = 20\text{ W} + 20\text{ W}$ ,<br>THD = 10%                           |      | 4.0  |      | W                |
| $\eta$        | Efficiency                               | $P_o = 20\text{ W} + 20\text{ W}$                                          | 80   | 90   |      | %                |
| THD           | Total harmonic distortion                | $P_o = 1\text{ W}$                                                         |      | 0.1  |      | %                |
| $G_V$         | Closed-loop gain                         | GAIN0 = L, GAIN1 = L                                                       | 18   | 20   | 22   | dB               |
|               |                                          | GAIN0 = L, GAIN1 = H                                                       | 24   | 26   | 28   |                  |
|               |                                          | GAIN0 = H, GAIN1 = L                                                       | 28   | 30   | 32   |                  |
|               |                                          | GAIN0 = H, GAIN1 = H                                                       | 30   | 32   | 34   |                  |
| $\Delta G_V$  | Gain matching                            |                                                                            | -1   |      | +1   | dB               |
| CT            | Cross-talk                               | $f = 1\text{ kHz}$ , $P_o = 1\text{ W}$                                    |      | 70   |      | dB               |
| eN            | Total input noise                        | A curve, $G_V = 20\text{ dB}$                                              |      | 20   |      | $\mu\text{V}$    |
|               |                                          | $f = 22\text{ Hz to } 22\text{ kHz}$                                       | -    | 25   | 35   |                  |
| SVRR          | Supply voltage rejection ratio           | $f_r = 100\text{ Hz}$ , $V_r = 1\text{ Vpp}$ , $C_{SVR} = 10\ \mu\text{F}$ |      | 50   |      | dB               |
| $T_r$ , $T_f$ | Rise and fall times                      |                                                                            |      | 40   |      | ns               |
| $f_{SW}$      | Switching frequency                      | Internal oscillator, master mode                                           | 290  | 320  | 350  | kHz              |



| Symbol            | Parameter                 | Test conditions                                                        | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------|------------------------------------------------------------------------|------|------|------|------|
| $f_{\text{SWR}}$  | Switching frequency range | (1)                                                                    | 250  | -    | 400  | kHz  |
| $V_{\text{inH}}$  | Digital input high (H)    | -                                                                      | 2.3  |      |      | V    |
| $V_{\text{inL}}$  | Digital input low (L)     |                                                                        |      |      | 0.8  |      |
| $A_{\text{MUTE}}$ | Mute attenuation          | $V_{\text{MUTE}} = \text{low}$ , $V_{\text{STBY}} = \text{high}$       |      | 80   |      | dB   |
| Function mode     | Standby mode              | $V_{\text{STBY}} < 0.5 \text{ V}$<br>$V_{\text{MUTE}} = \text{X}$      |      |      |      |      |
|                   | Mute mode                 | $V_{\text{STBY}} > 2.9 \text{ V}$<br>$V_{\text{MUTE}} < 0.8 \text{ V}$ |      |      |      |      |
|                   | Play mode                 | $V_{\text{STBY}} > 2.9 \text{ V}$<br>$V_{\text{MUTE}} > 2.9 \text{ V}$ |      |      |      |      |

1. Refer to [Section 8.4 Internal and external clocks](#).

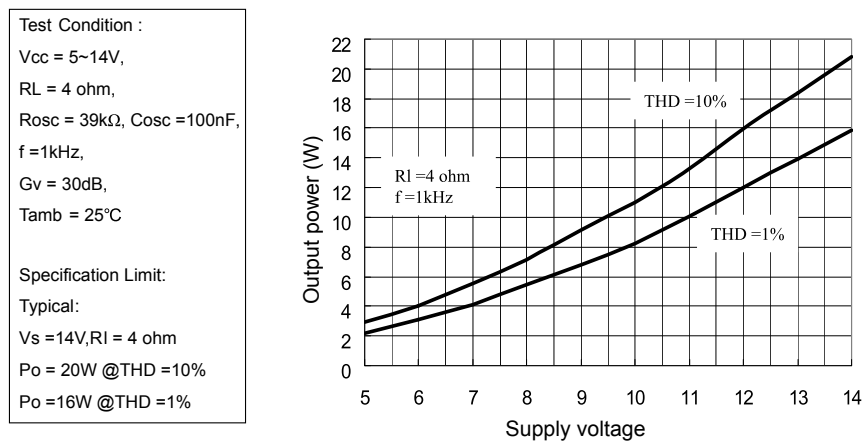
## 5 Characterization curves

The following characterization curves have been produced by using the TDA7491HV evaluation board.

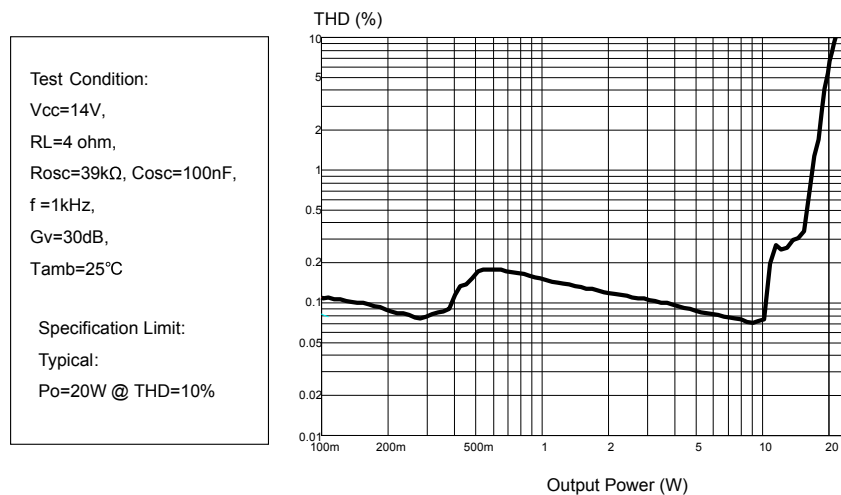
The LC filter for 4  $\Omega$  load uses components of 15  $\mu\text{H}$  and 470 nF, whilst that for 6  $\Omega$  load uses 22  $\mu\text{H}$  and 220 nF and that for 8  $\Omega$  load uses 33  $\mu\text{H}$  and 220 nF.

### 5.1 4 $\Omega$ loads at $V_{CC} = 14\text{ V}$

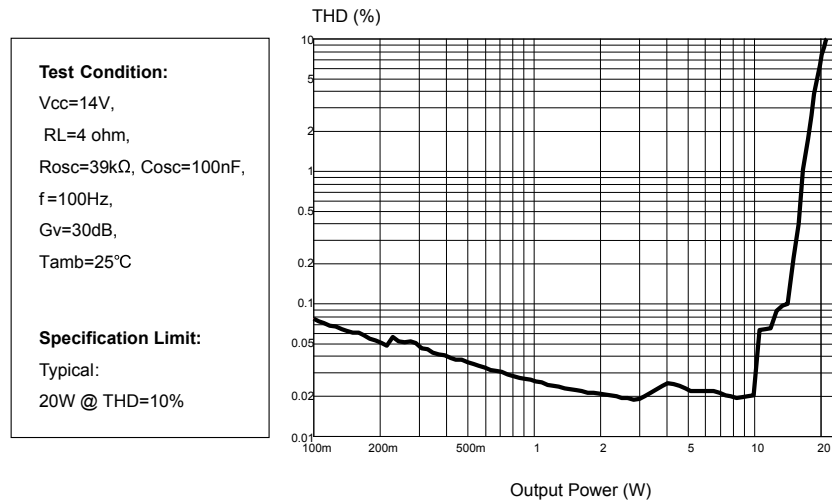
**Figure 4. Output power vs. supply voltage**



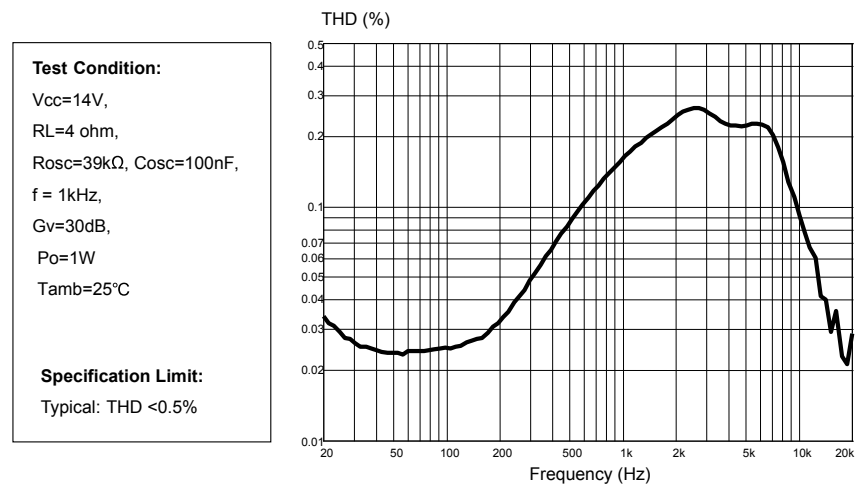
**Figure 5. THD vs. output power (1 kHz)**

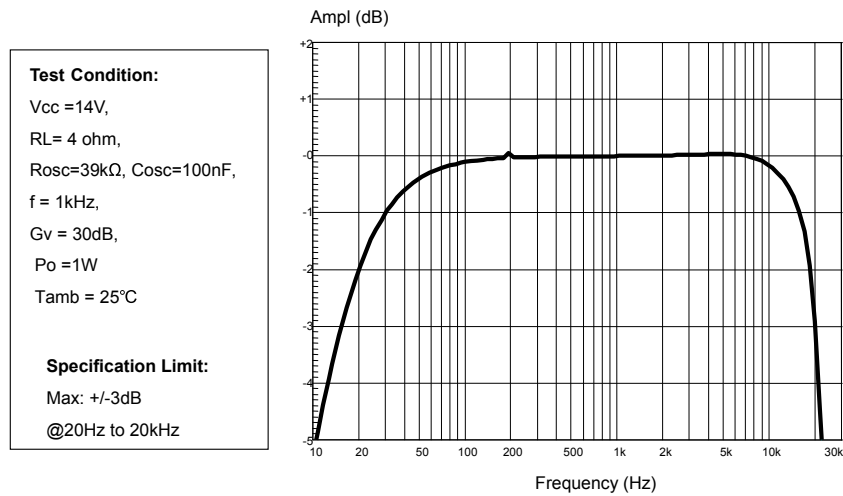
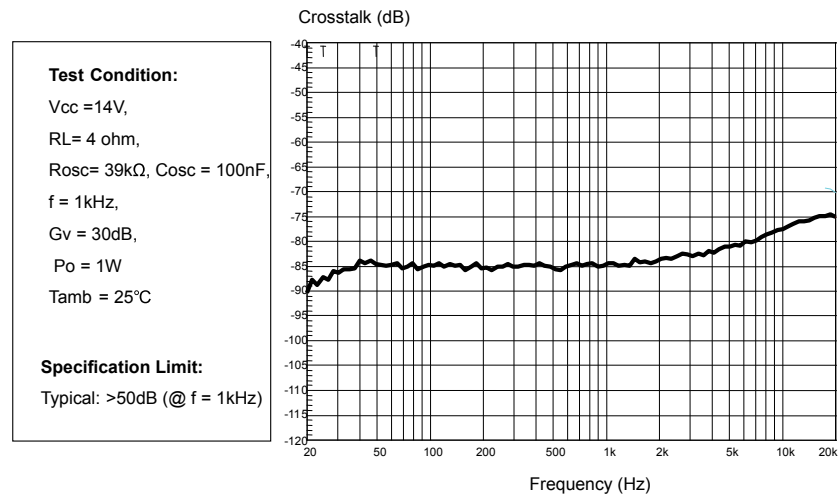
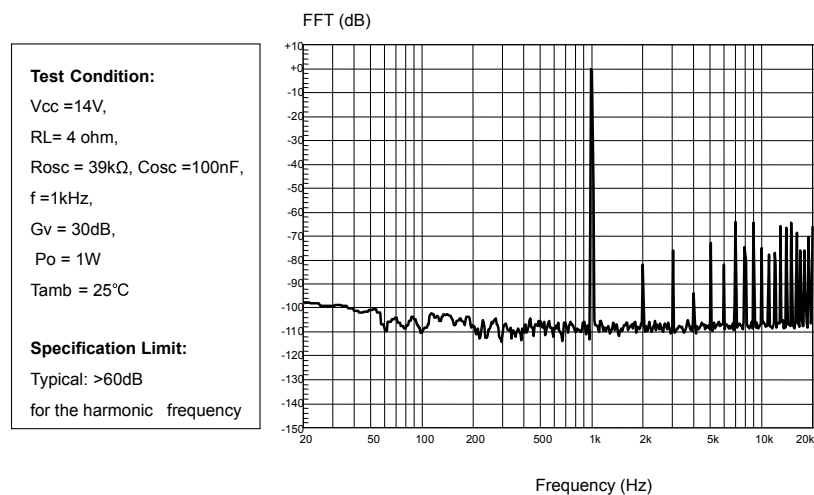


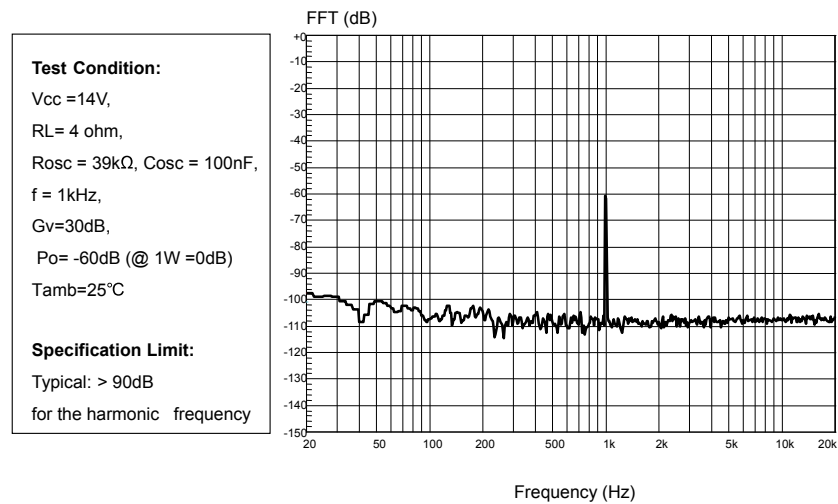
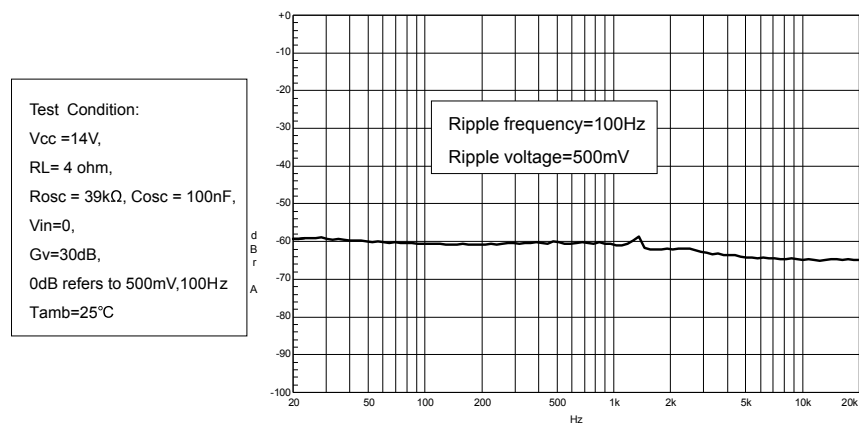
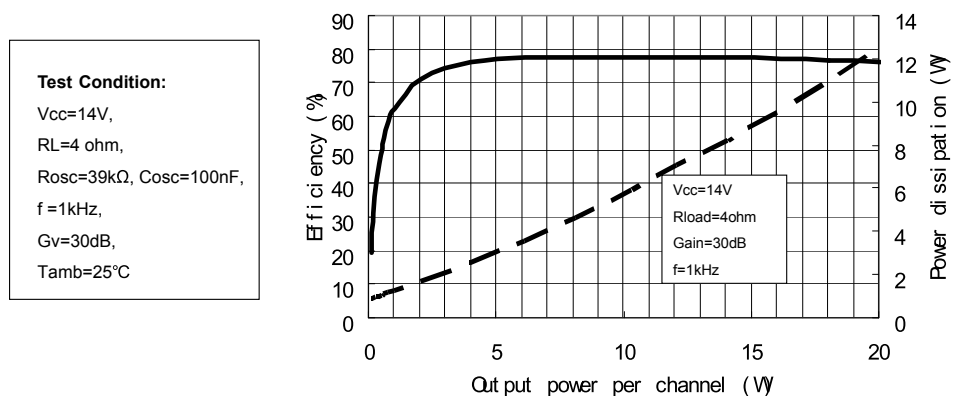
**Figure 6. THD vs. output power (100 Hz)**

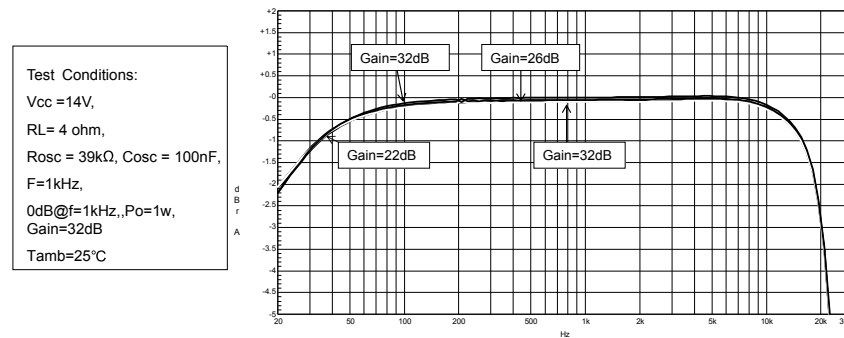
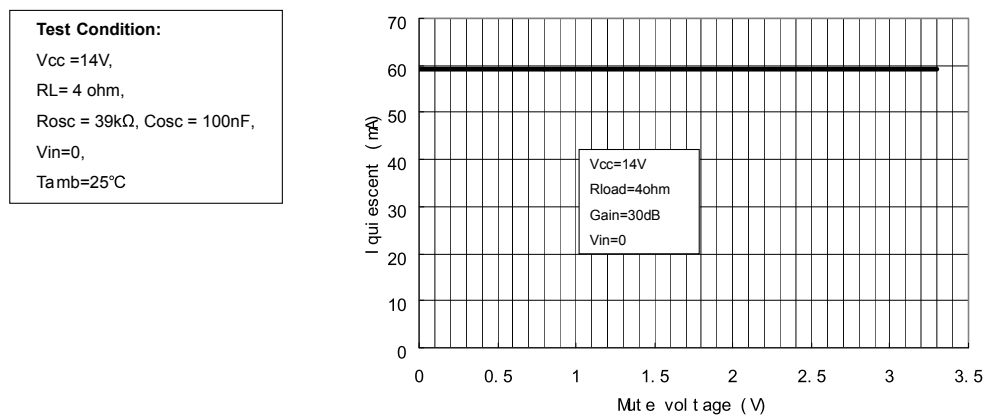
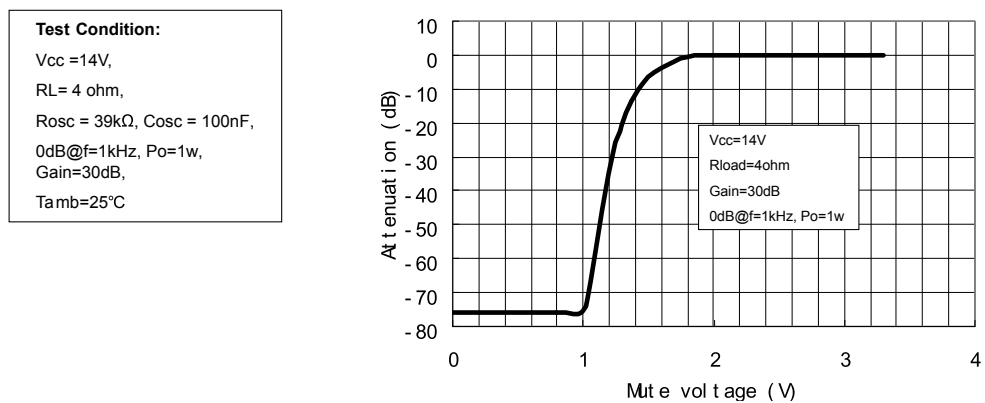


**Figure 7. THD vs. frequency**

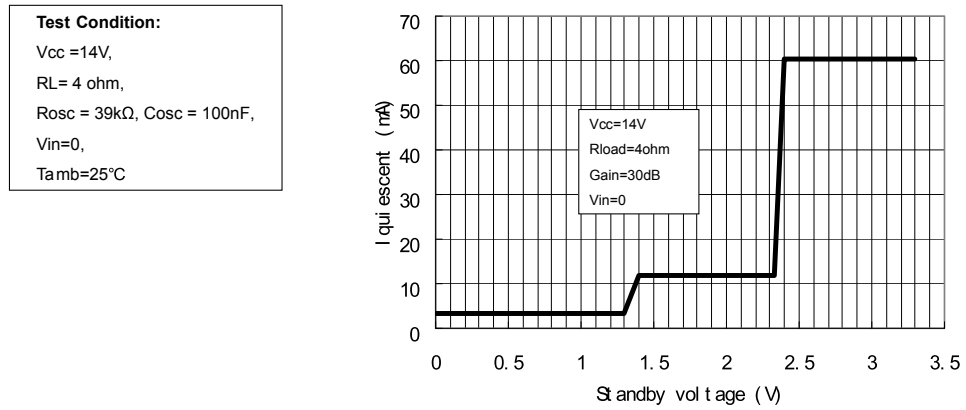


**Figure 8. Frequency response**

**Figure 9. Crosstalk vs. frequency**

**Figure 10. FFT performance (0 dB)**


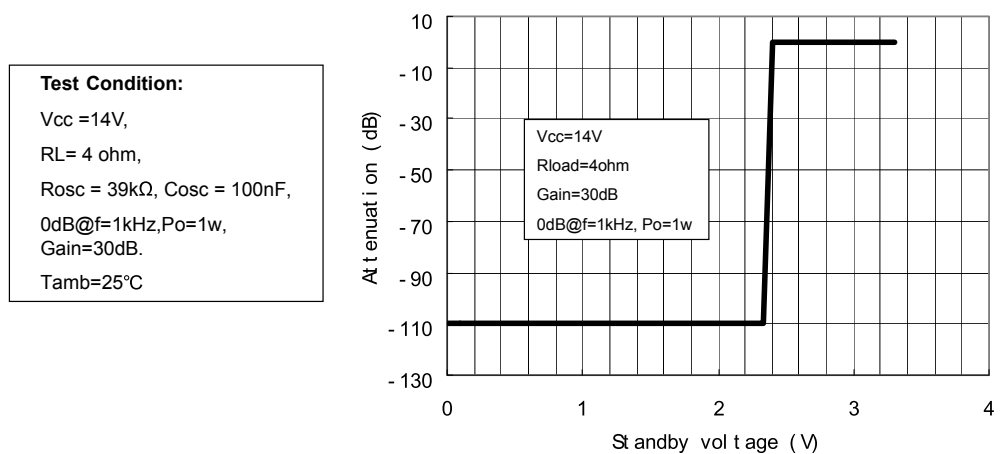
**Figure 11. FFT performance (-60 dB)**

**Figure 12. Power supply rejection ratio vs. frequency**

**Figure 13. Power dissipation and efficiency vs. output power**


**Figure 14. Closed-loop gain vs. frequency**

**Figure 15. Current consumption vs. voltage on pin MUTE**

**Figure 16. Attenuation vs. voltage on pin MUTE**


**Figure 17. Current consumption vs. voltage on pin STBY**

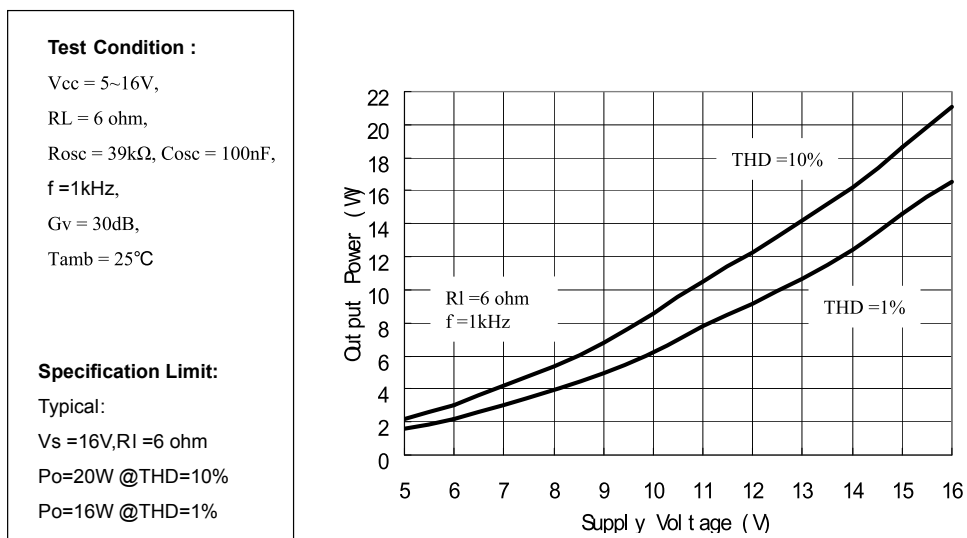


**Figure 18. Attenuation vs. voltage on pin STBY**

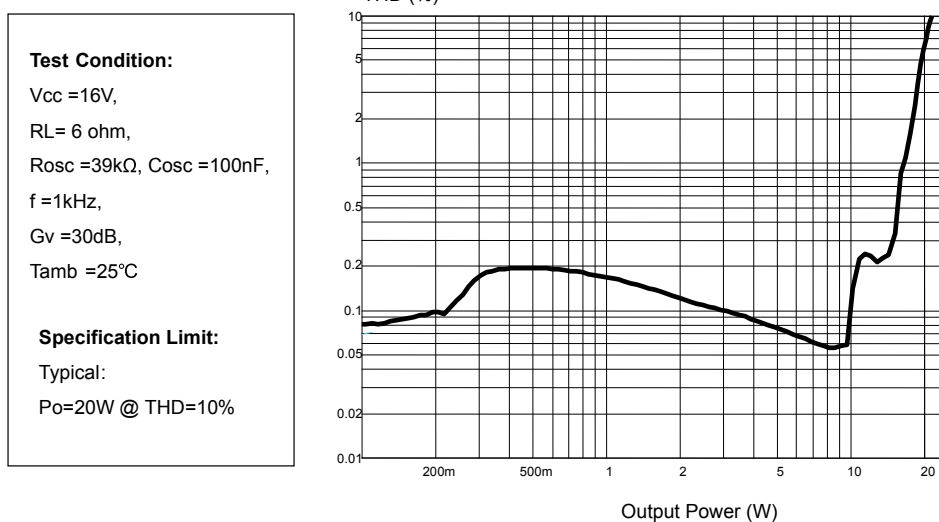


## 5.2 6 $\Omega$ loads at VCC = 16 V

**Figure 19. Output power vs. supply voltage**

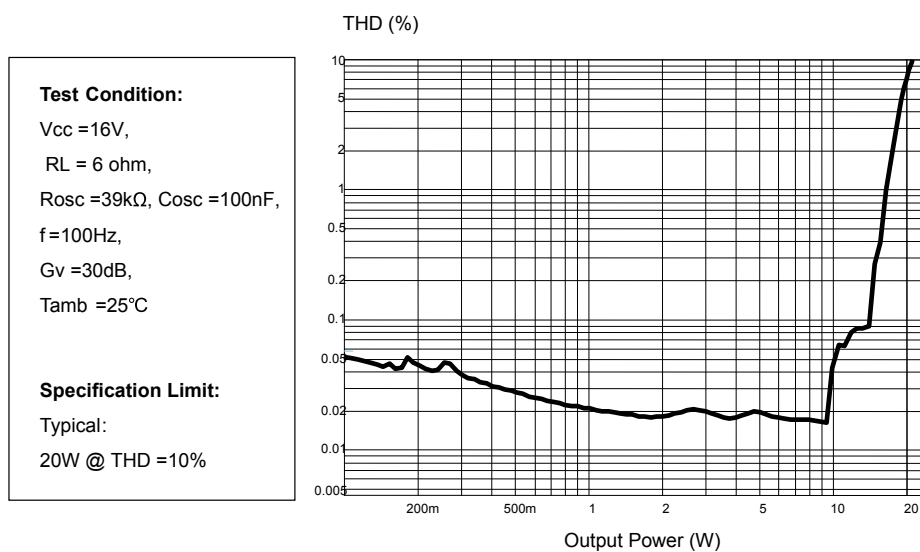


**Figure 20. THD vs. output power (1 kHz)**

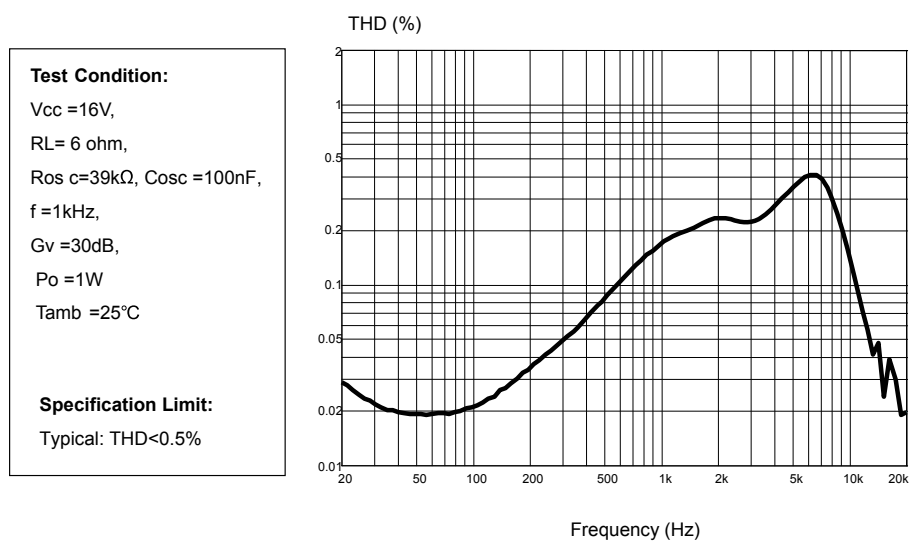




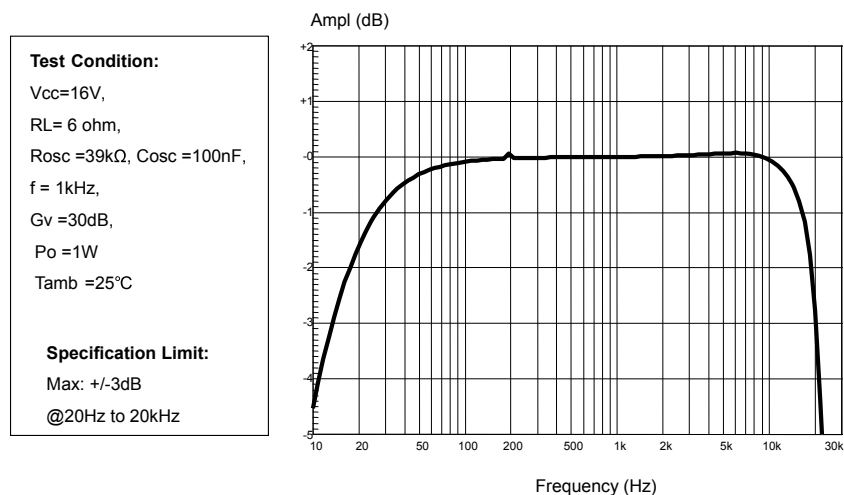
**Figure 21. THD vs. output power (100 Hz)**



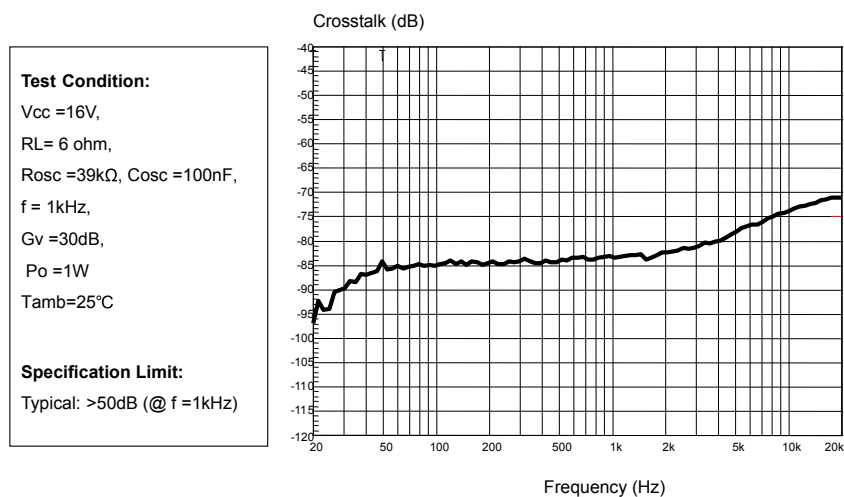
**Figure 22. THD vs. frequency**



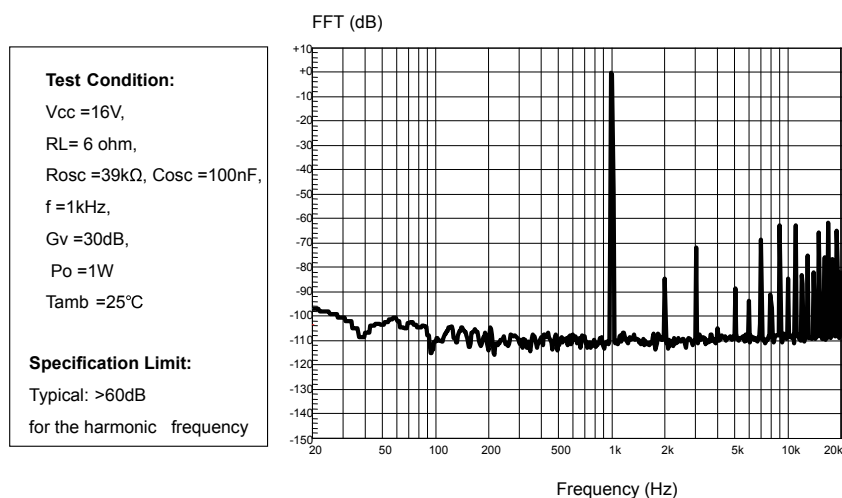
**Figure 23. Frequency response**



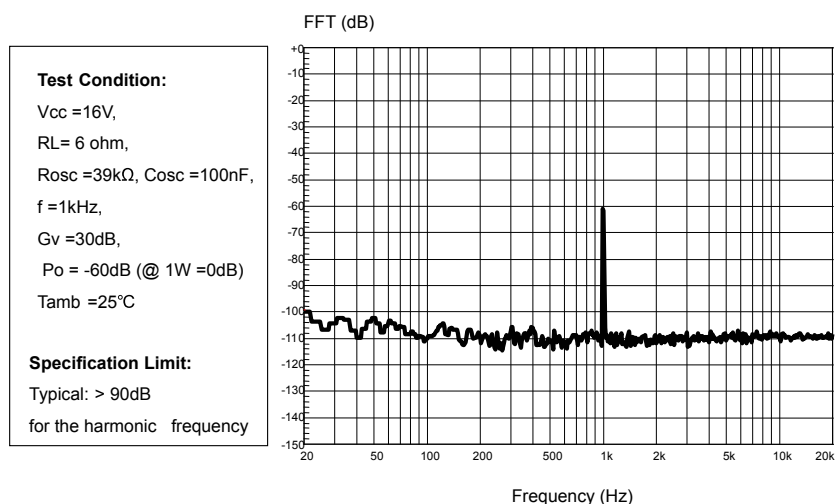
**Figure 24. Crosstalk vs. frequency**



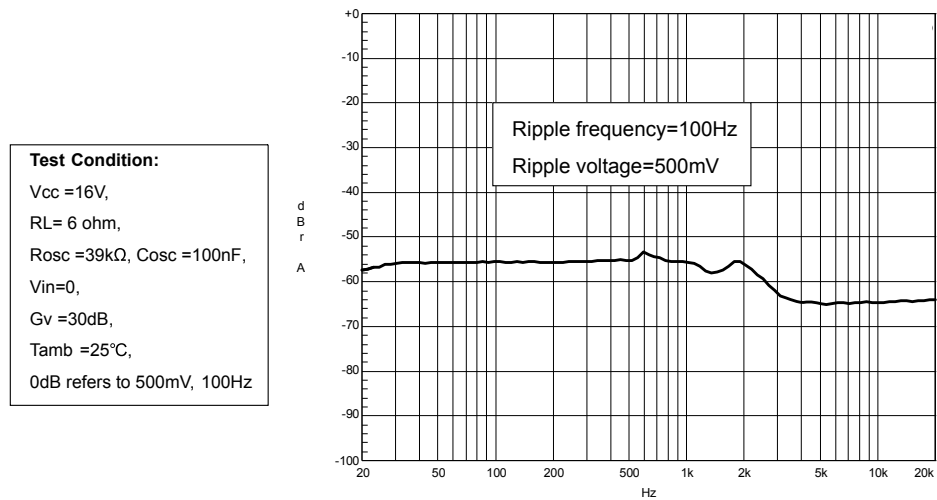
**Figure 25. FFT performance (0 dB)**



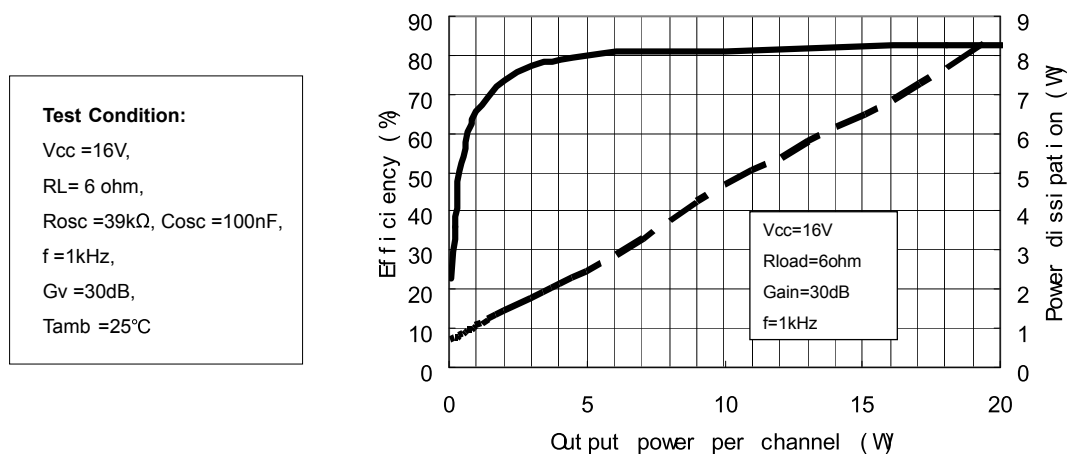
**Figure 26. FFT performance (-60 dB)**



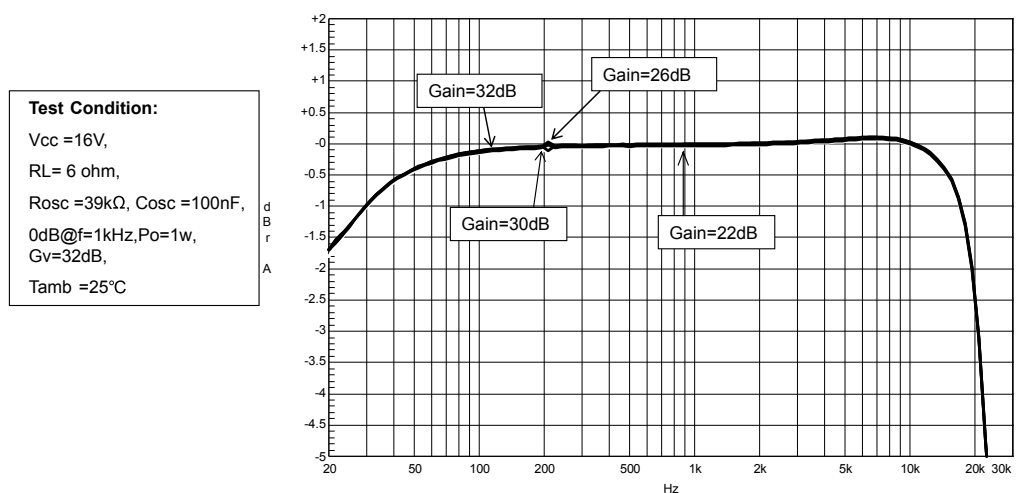
**Figure 27. Power supply rejection ratio vs. frequency**



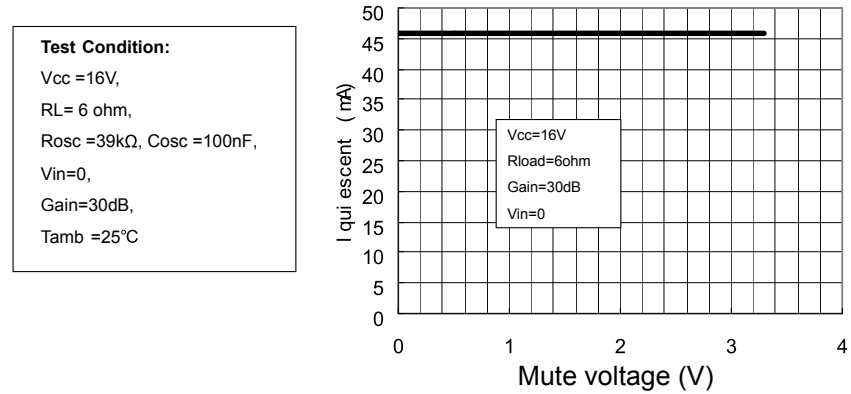
**Figure 28. Power dissipation and efficiency vs. output power**



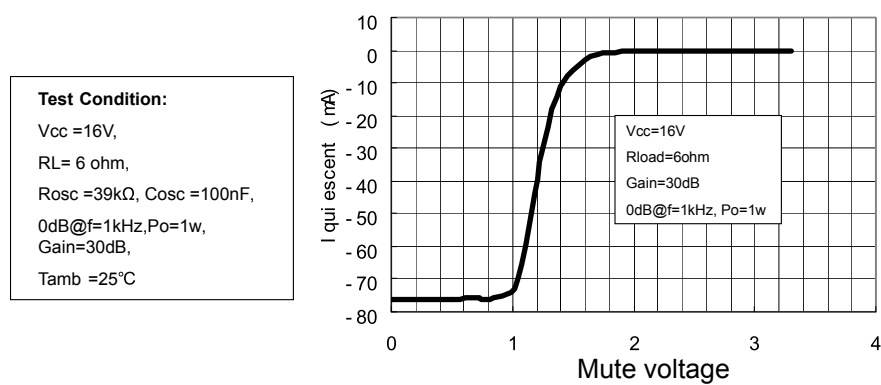
**Figure 29. Closed-loop gain vs. frequency**



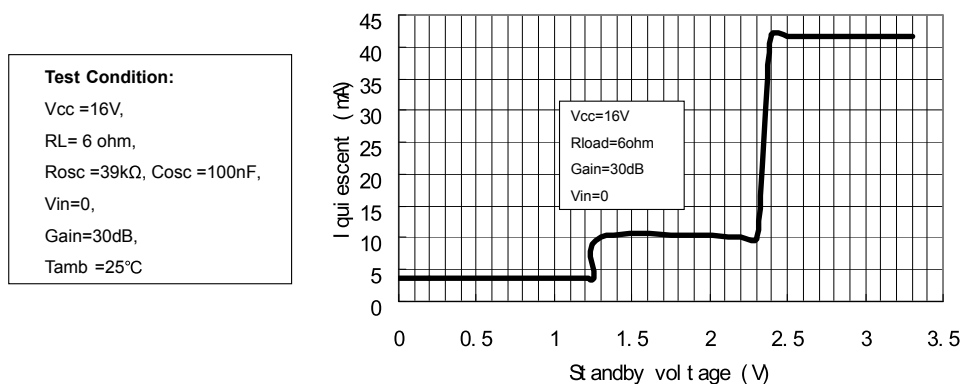
**Figure 30. Current consumption vs. voltage on pin MUTE**



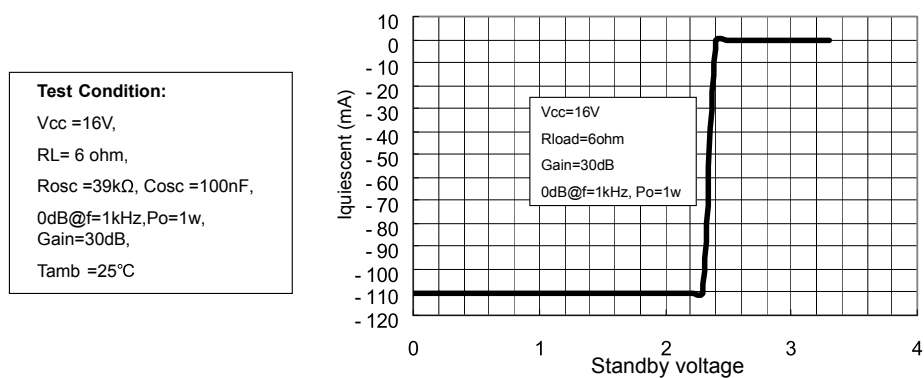
**Figure 31. Attenuation vs. voltage on pin MUTE**



**Figure 32. Current consumption vs. voltage on pin STBY**



**Figure 33. Attenuation vs. voltage on pin STBY**



### 5.3 8 $\Omega$ loads at VCC = 18 V

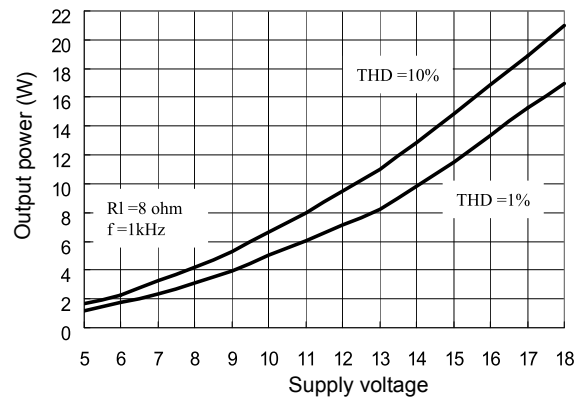
**Figure 34. Output power vs. supply voltage**

**Test conditions :**

VCC = 5~18V,  
 RL = 8 ohm,  
 Rsc = 39k $\Omega$ , Csc = 100nF  
 f = 1kHz,  
 Gv = 30dB,  
 Tamb = 25°C

**Specification limit:**

Typical:  
 Vs = 18V, RL = 8 ohm  
 Po = 20W @THD = 10%  
 Po = 16W @THD = 1%



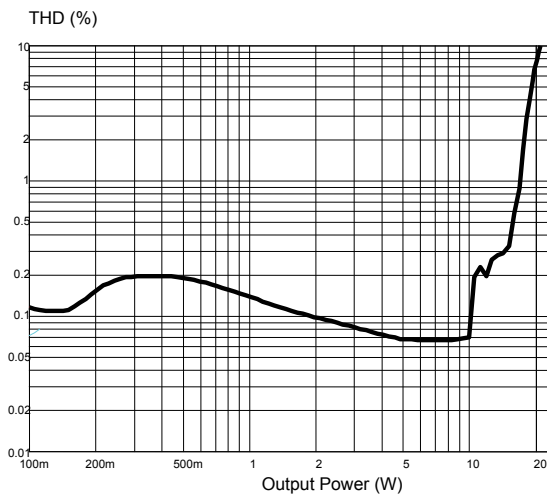
**Figure 35. THD vs. output power (1 kHz)**

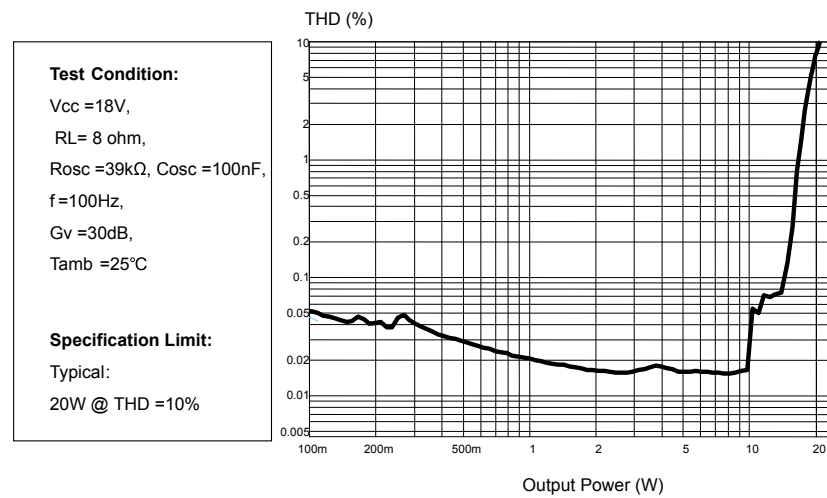
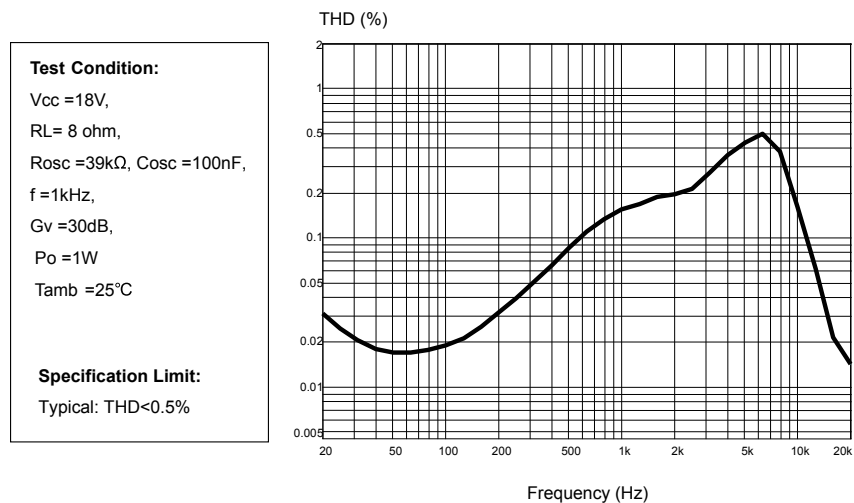
**Test Condition:**

VCC = 18V,  
 RL = 8 ohm,  
 Rsc = 39k $\Omega$ , Csc = 100nF,  
 f = 1kHz,  
 Gv = 30dB,  
 Tamb = 25°C

**Specification Limit:**

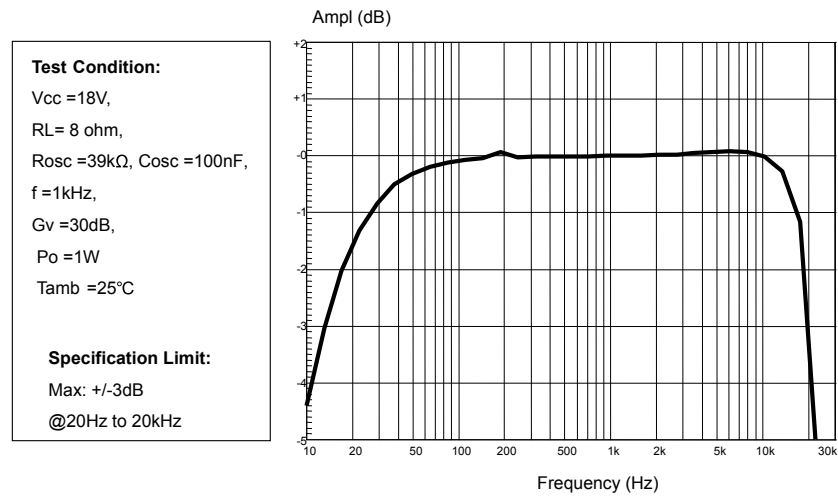
Typical:  
 Po = 20W @ THD = 10%



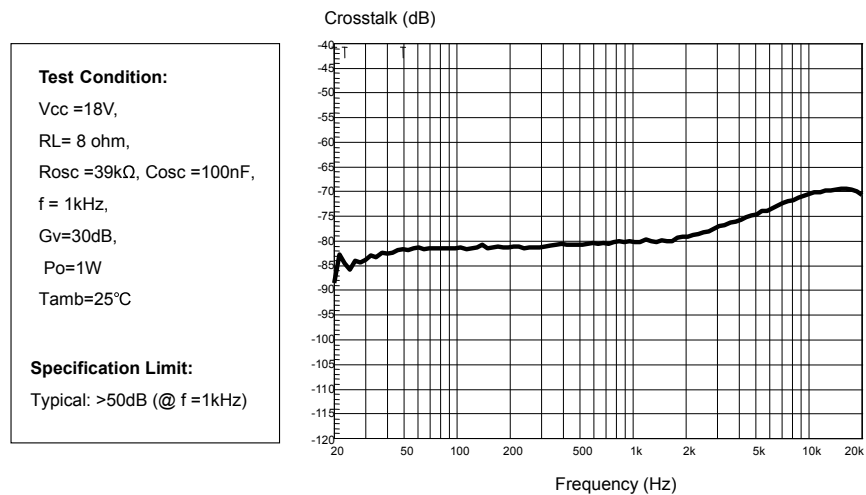
**Figure 36. THD vs. output power (100 Hz)**

**Figure 37. THD vs. frequency**




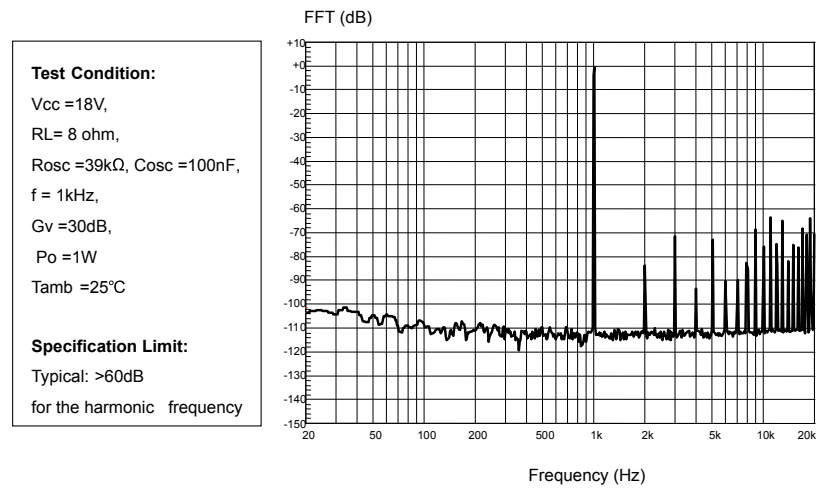
**Figure 38. Frequency response**



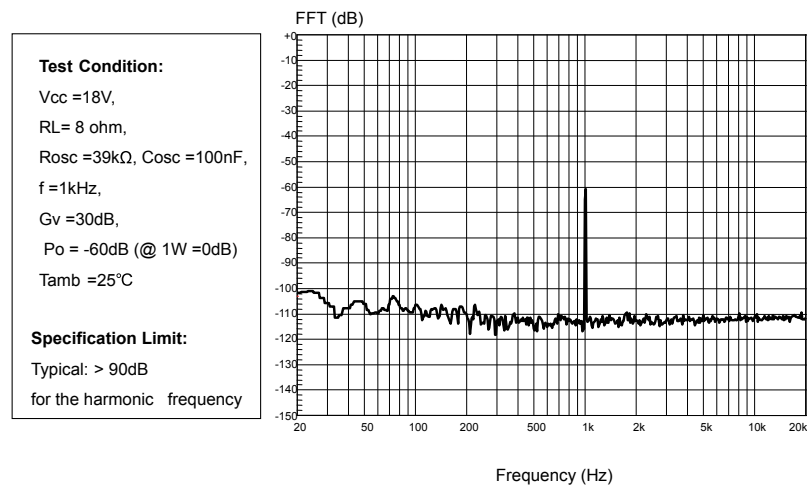
**Figure 39. Crosstalk vs. frequency**

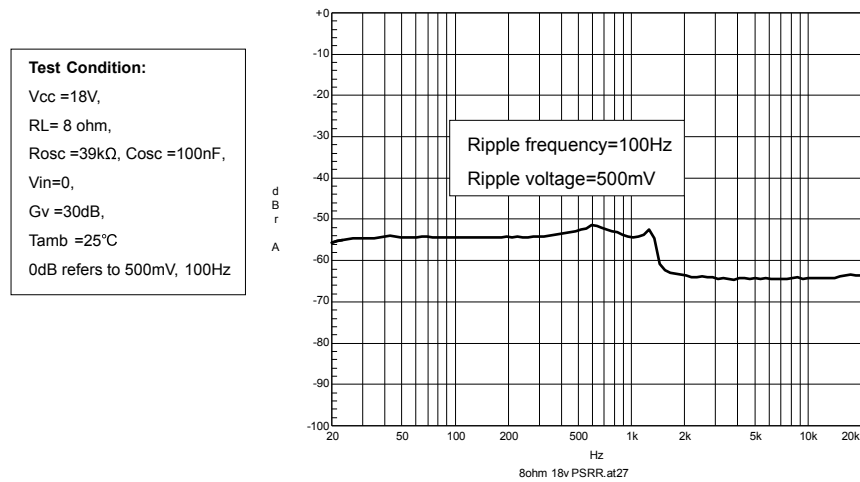
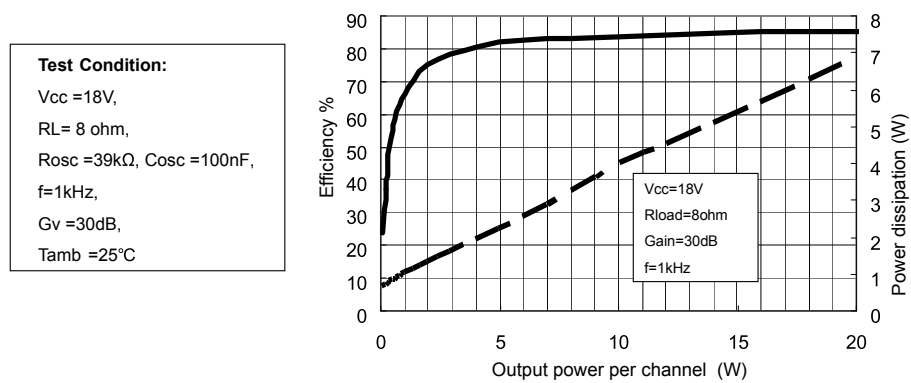


**Figure 40. FFT performance (0 dB)**

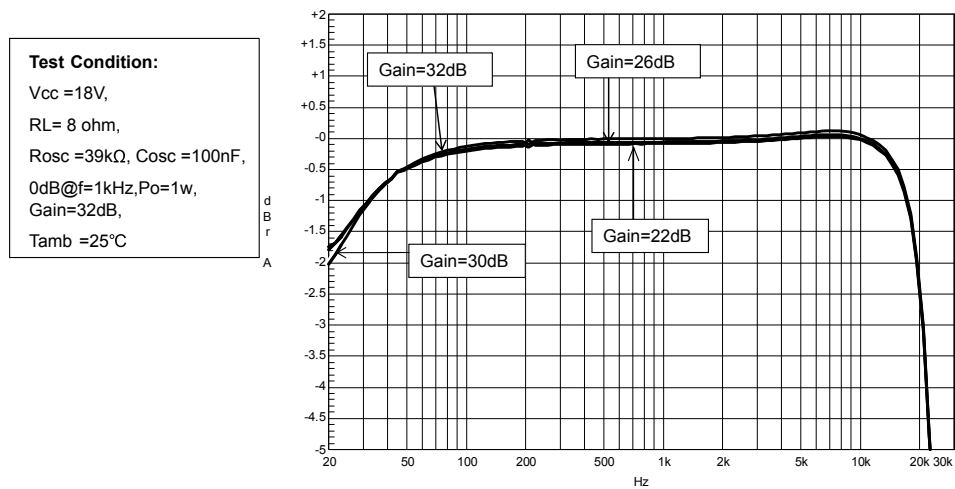


**Figure 41. FFT performance (-60 dB)**

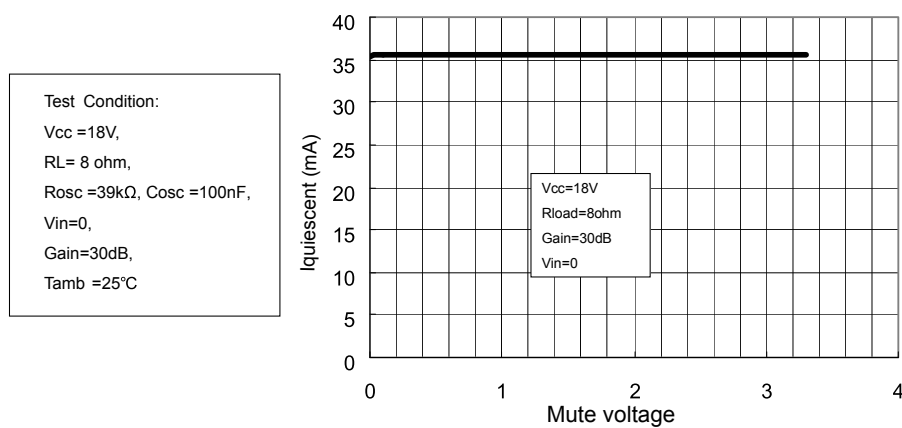


**Figure 42. Power supply rejection ratio vs. frequency**

**Figure 43. Power dissipation and efficiency vs. output power**


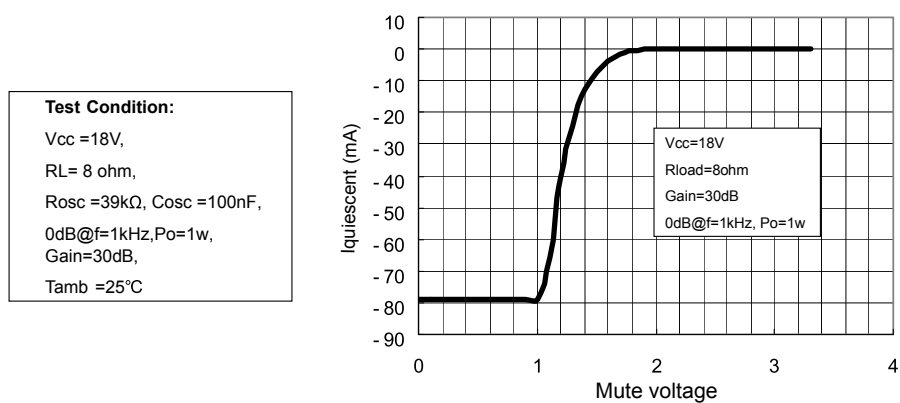
**Figure 44. Closed-loop gain vs. frequency**



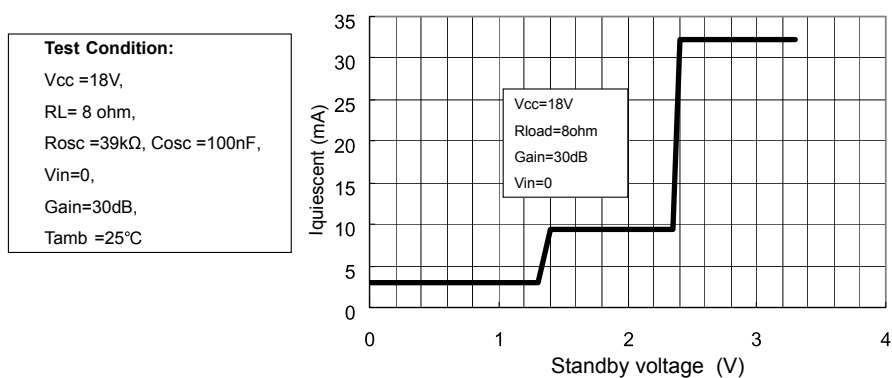
**Figure 45. Current consumption vs. voltage on pin MUTE**



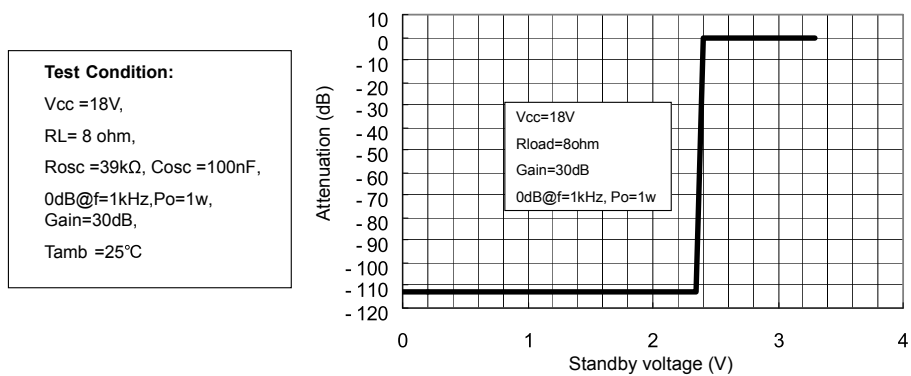
**Figure 46. Attenuation vs. voltage on pin MUTE**



**Figure 47. Current consumption vs. voltage on pin STBY**

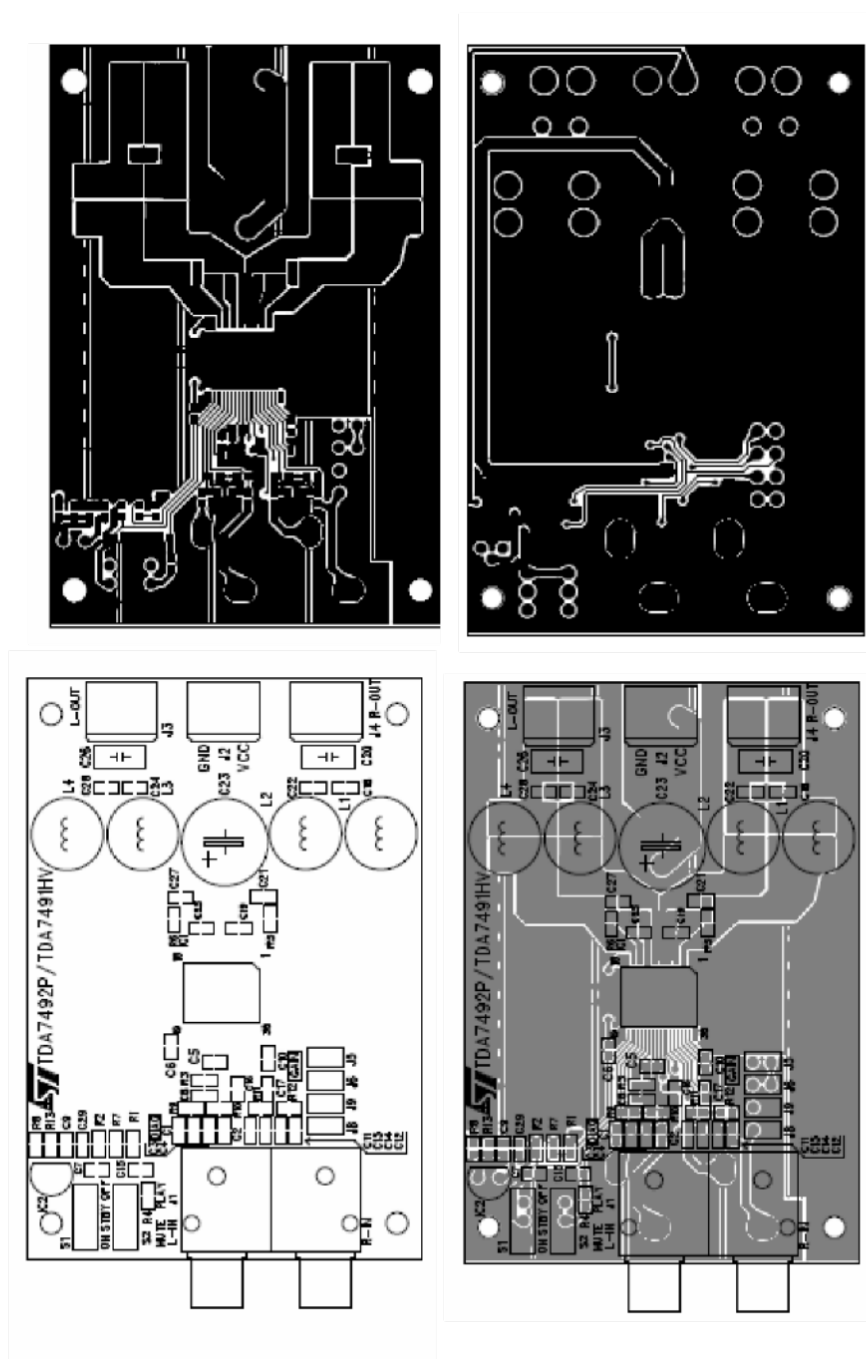


**Figure 48. Attenuation vs. voltage on pin STBY**



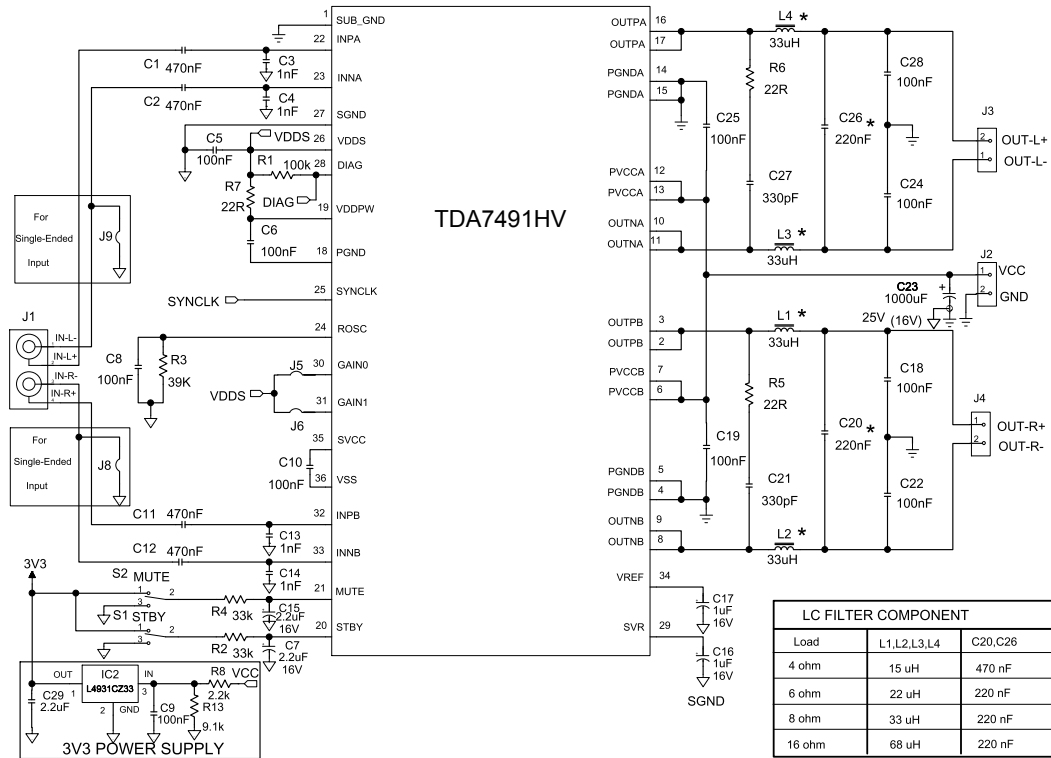
## 6 Test board

Figure 49. Test board (TDA7491HV) layout



## 7 Application circuit

**Figure 50. Application circuit for class-D amplifier**





## 8 Application information

### 8.1 Mode selection

The three operating modes of the TDA7491HV are set by the two inputs, STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

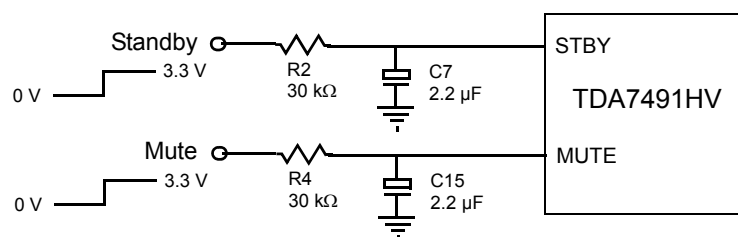
The protection functions of the TDA7491HV are enabled by pulling down the voltages of the STBY and MUTE inputs shown in figure below. The input current of the corresponding pins must be limited to 200  $\mu$ A.

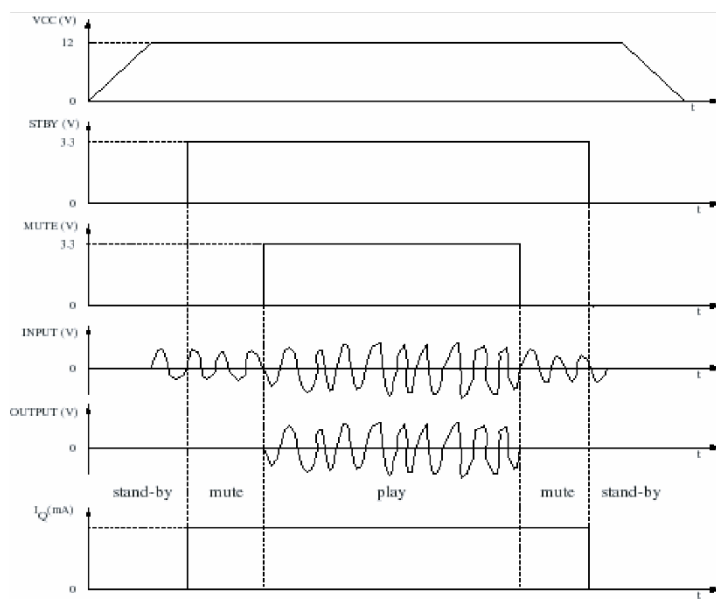
**Table 6. Mode settings**

| Mode    | STBY             | MUTE            |
|---------|------------------|-----------------|
| Standby | L <sup>(1)</sup> | X (do not care) |
| Mute    | H <sup>(1)</sup> | L               |
| Play    | H                | H               |

1. Refer to  $V_{STBY}$  and  $V_{MUTE}$  in [Section 4 Electrical specifications](#)

**Figure 51. Standby and mute circuits**



**Figure 52. Turn-on/off sequence for minimizing speaker “pop”**


## 8.2 Gain setting

The gain of the TDA7491HV is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin31). Internally, the gain is set by changing the feedback resistors of the amplifier.

**Table 7. Gain settings**

| GAIN0            | GAIN1            | Nominal gain, $G_v$ (dB) |
|------------------|------------------|--------------------------|
| L <sup>(1)</sup> | H <sup>(1)</sup> | 20                       |
| L                | H                | 26                       |
| H                | L                | 30                       |
| H                | H                | 32                       |

1. Refer to [Section 4 Electrical specifications](#) for L and H drive levels.

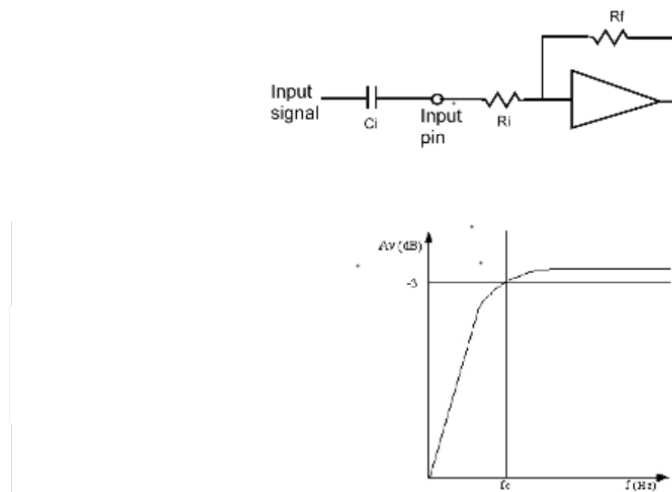
### 8.3 Input resistance and capacitance

The input impedance is set by an internal resistor  $R_i = 68 \text{ k}\Omega$  (typical). An input capacitor ( $C_i$ ) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in figure below. For  $C_i = 220 \text{ nF}$ , the high-pass filter cut-off frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

**Figure 53. Device input circuit and frequency response**



### 8.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all the devices operate at the same clock frequency. This can be implemented by using one TDA7491HV as master clock, while the other devices are in slave mode, that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an output in master mode and an input in slave mode.

#### 8.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency,  $f_{SW}$ , is controlled by the resistor,  $R_{OSC}$ , connected to pin ROSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where  $R_{OSC}$  is in  $\text{k}\Omega$ .

In master mode, pin SYNCLK is used as a clock output pin whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly, then resistor  $R_{OSC}$  must be less than 60  $\text{k}\Omega$  as given below in [Table 8. How to set up SYNCLK.](#)

### 8.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in table below.

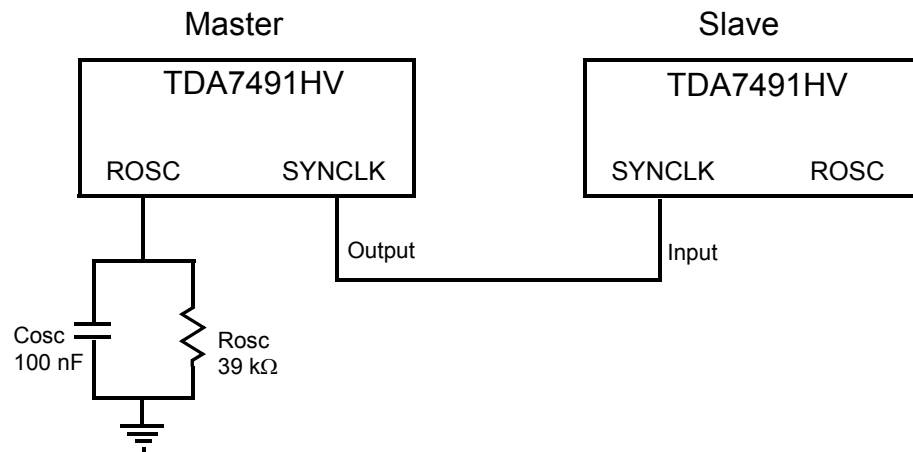
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

**Table 8. How to set up SYNCLK**

| Mode   | ROSC                           | SYNCLK |
|--------|--------------------------------|--------|
| Master | $R_{OSC} < 60 \text{ k}\Omega$ | Output |
| Slave  | Floating (not connected)       | Input  |

**Figure 54. Master and slave connection**



## 8.5 Modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM).

The differential output voltages change between 0 V and  $+V_{CC}$  and between 0 V and  $-V_{CC}$ .

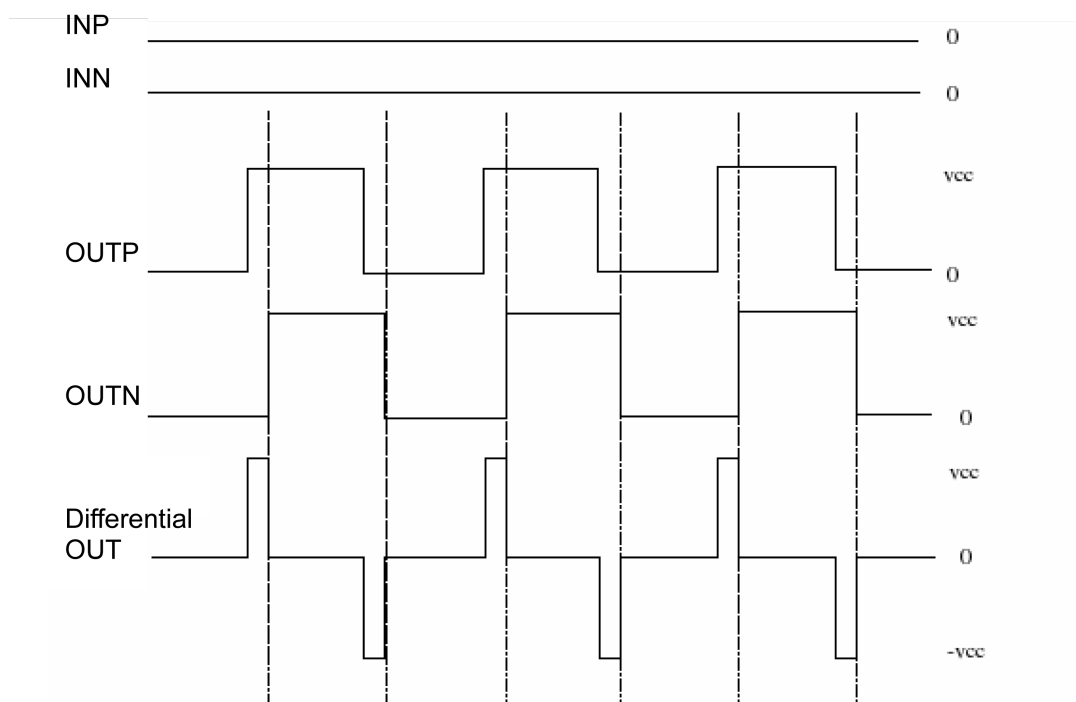
This is in contrast to the traditional bipolar PWM outputs which change between  $+V_{CC}$

and  $-V_{CC}$ . An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform on the load then reducing the current ripple accordingly. The OUTP and OUTN are in the same phase almost overlapped when the input is zero under this condition, then the switching current is low and the related losses in the load are low.

In practice, a short delay is introduced between these two outputs in order to avoid the BTL output switching simultaneously when the input is zero.

Figure below shows the resulting differential output voltage and current when a positive, zero and negative input signal is applied. The resulting differential voltage on the load has a double frequency with respect to outputs OUTP and OUTN, resulting in reduced current ripple.

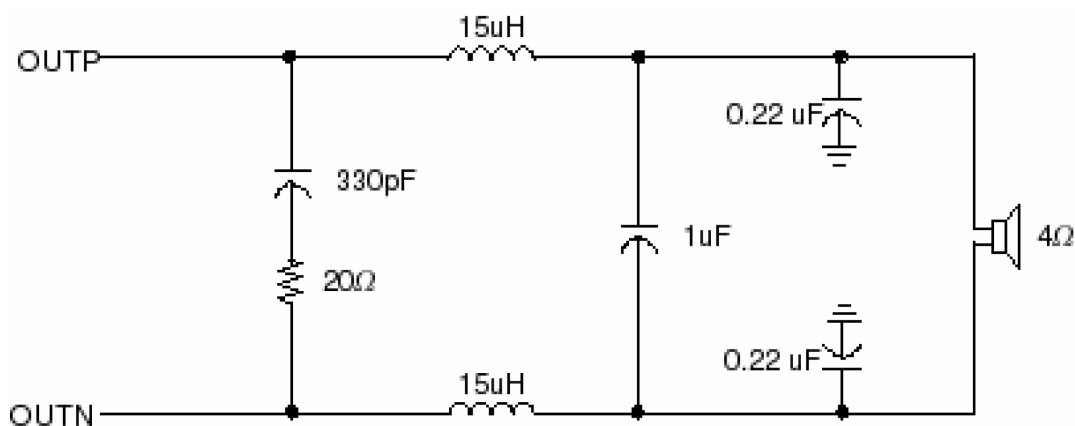
**Figure 55. Unipolar PWM output**



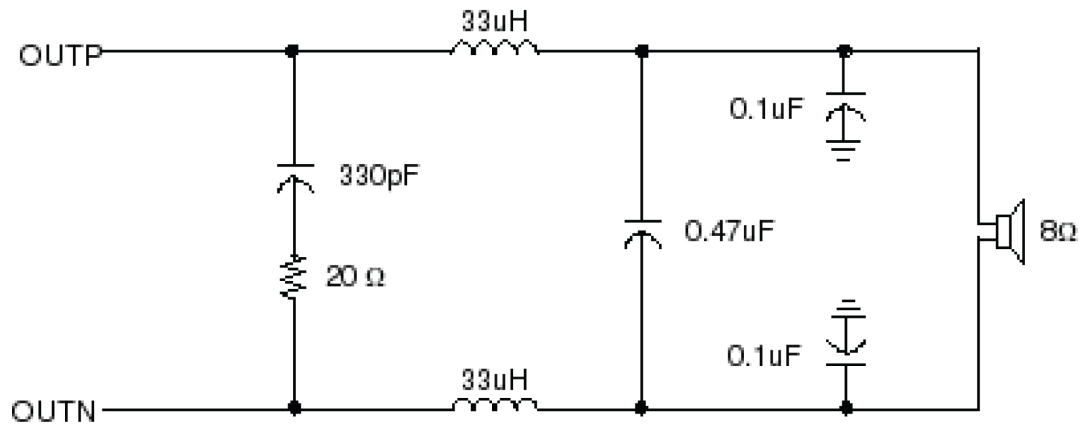
## 8.6 Reconstruction low-pass filter

Standard applications use a low-pass filter before the speaker. The cut-off frequency should be higher than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in figures below.

**Figure 56. Typical LC filter for an 8 Ω speaker**



**Figure 57. Typical LC filter for an 4 Ω speaker**



## 8.7 Protection functions

The TDA7491HV is fully protected against undervoltage, overcurrent and thermal overloads as explained here.

### Undervoltage protection (UVP)

If the supply voltage drops below the value of  $V_{UVP}$  given in [Section 4 Electrical specifications](#) the undervoltage protection is active and forces the outputs to the high-impedance state. When the supply voltage recovers, the device restarts.

### Overcurrent protection (OCP)

If the output current exceeds the value for  $I_{OCP}$  given in [Section 4 Electrical specifications](#), the overcurrent protection is active and forces the outputs to the high-impedance state. Periodically, the device tries to restart. If the overcurrent condition is still present then the OCP remains active. The restart time,  $T_{OC}$ , is determined by the R-C components connected to pin STBY.

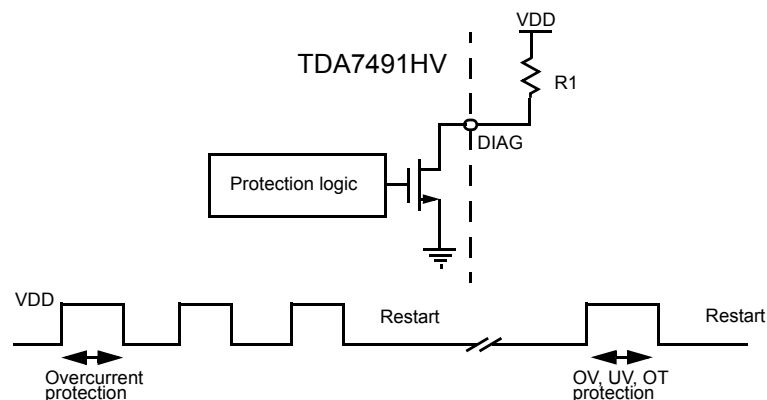
### Thermal protection (OTP)

If the junction temperature,  $T_j$ , reaches 145 °C (nominal), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for  $T_j$ , given in [Section 4 Electrical specifications](#), the device shuts down and the output is forced to the high-impedance state. When the device cools sufficiently the device restarts.

## 8.8 Diagnostic output

The output pin DIAG is an open-drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<18 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 μA) of the pin.

**Figure 58. Behavior of pin DIAG for various protection conditions**



## 8.9 Heatsink requirements

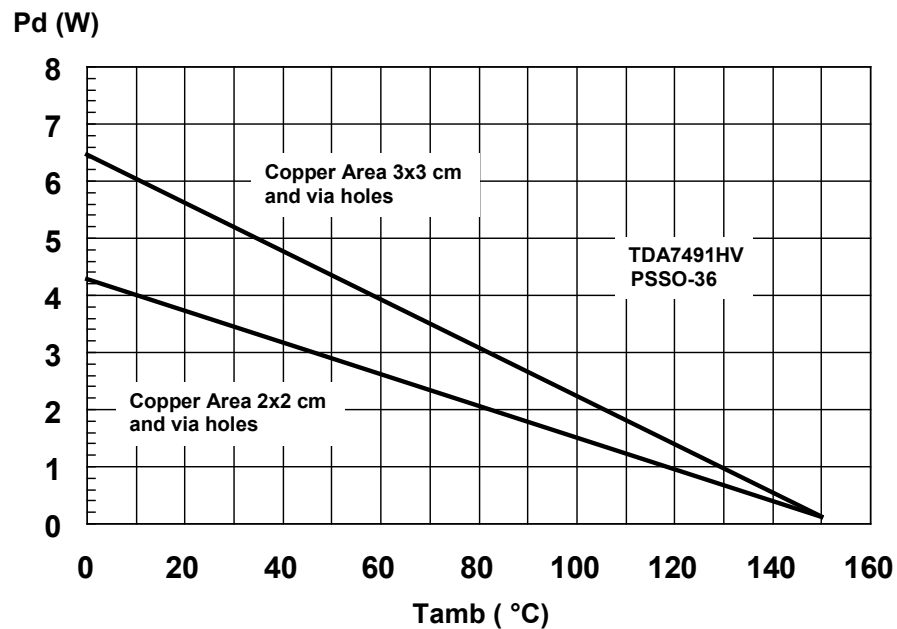
Due to the high efficiency of the class-D amplifier a 2-layer PCB can easily provide the heatsinking capability for low to medium power outputs. Using such a PCB with a copper ground layer of  $3 \times 3 \text{ cm}^2$  and 16 vias connecting it to the contact area for the exposed pad, a thermal resistance, junction-to-ambient (in natural air convection), of  $24^\circ\text{C/W}$  can be achieved.

The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level. With the TDA7491HV driving  $2 \times 8 \Omega$  with a supply of 18 V then the device dissipation is approximately 4 W that gives with the above mentioned PCB a junction temperature rise of about  $90^\circ\text{C}$ .

With a musical program, the dissipated power is about 40% less than the above maximum value. This leads to a junction temperature increase of around  $60^\circ\text{C}$ . So even at the maximum recommended ambient temperature there is a margin of safety before the maximum junction temperature is reached.

Figure below shows the derating curves for copper areas of  $4 \text{ cm}^2$  and  $9 \text{ cm}^2$ .

**Figure 59. Power derating curves for PCB used as heatsink**

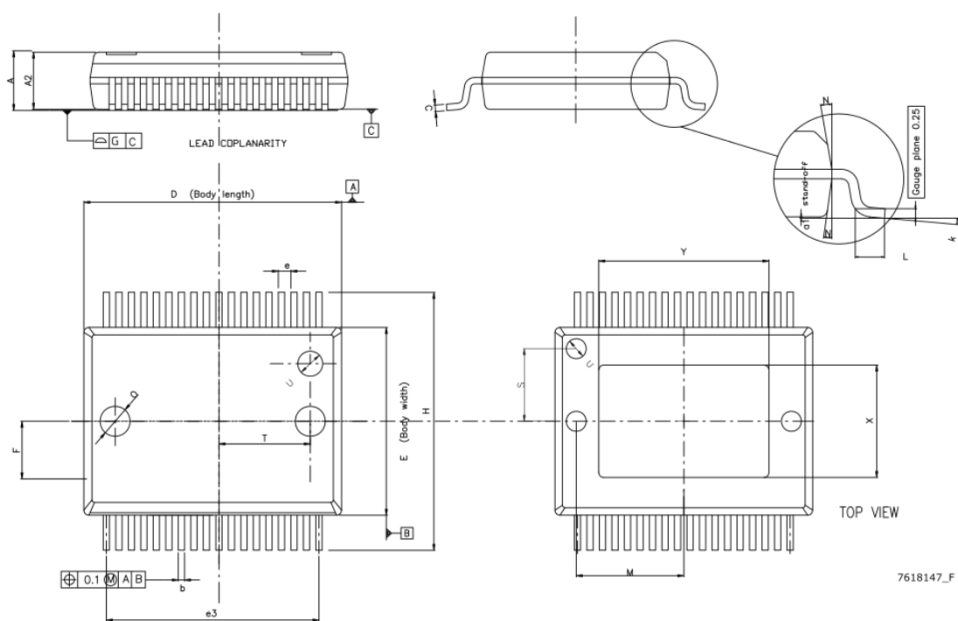


## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 9.1 PowerSSO-36 EPD

**Figure 60. PowerSSO-36 EPD package outline**



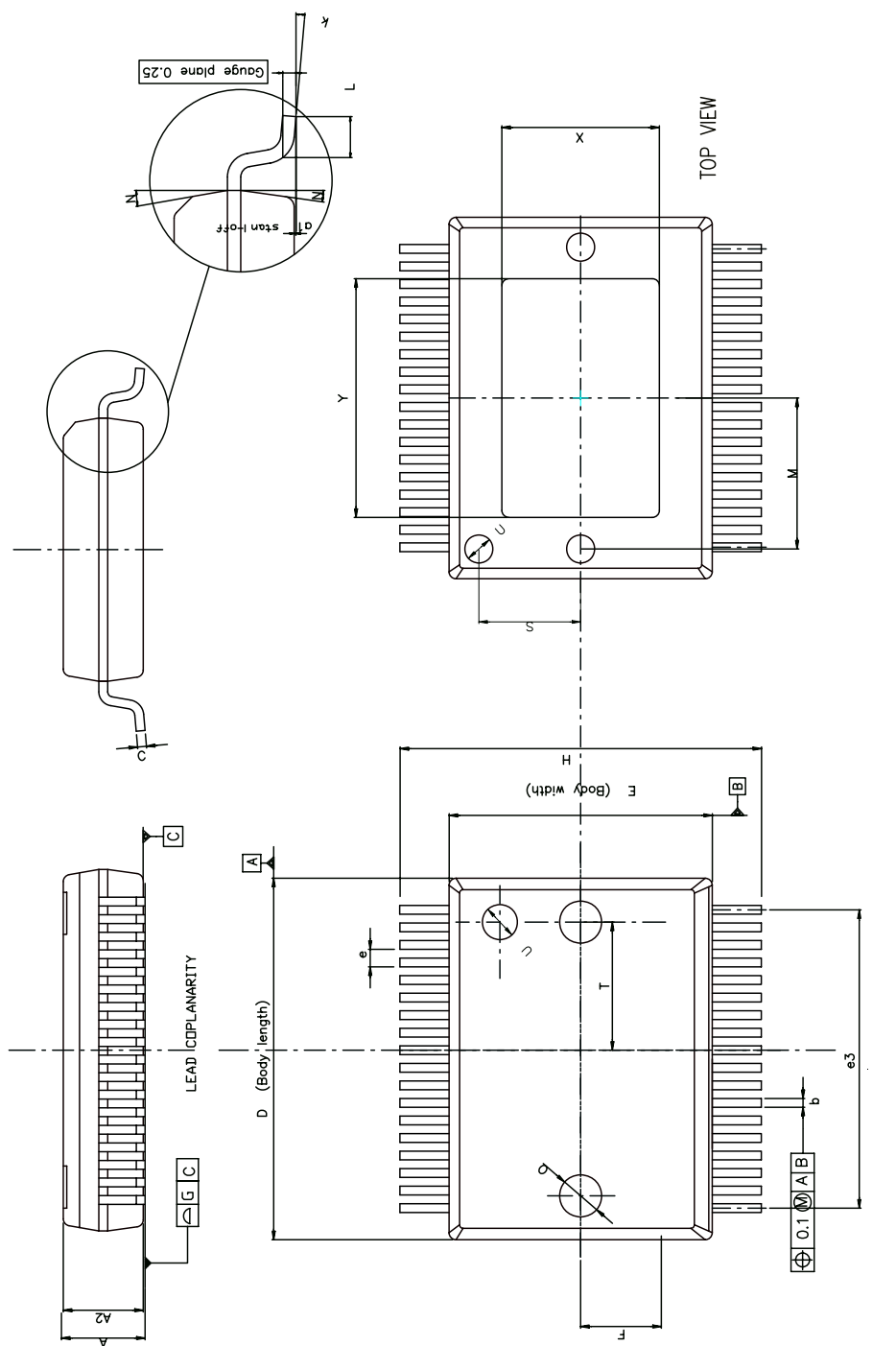


**Table 9. PowerSSO-36 EPD package dimensions**

| Symbol | mm    |      |            | Inches |       |            |
|--------|-------|------|------------|--------|-------|------------|
|        | Min.  | Typ. | Max.       | Min.   | Typ.  |            |
| A      | 2.15  |      | 2.47       | 0.085  |       | 0.097      |
| A2     | 2.15  |      | 2.40       | 0.085  |       | 0.094      |
| a1     | 0.00  |      | 0.10       | 0.000  |       | 0.004      |
| b      | 0.18  |      | 0.36       | 0.007  |       | 0.014      |
| c      | 0.23  |      | 0.32       | 0.009  |       | 0.013      |
| D      | 10.10 |      | 10.50      | 0.398  |       | 0.413      |
| E      | 7.40  |      | 7.60       | 0.291  |       | 0.299      |
| e      |       | 0.5  |            |        | 0.020 |            |
| e3     |       | 8.5  |            |        | 0.335 |            |
| F      |       | 2.3  |            |        | 0.091 |            |
| G      |       |      | 0.10       |        |       | 0.004      |
| H      | 10.10 |      | 10.50      | 0.398  |       | 0.413      |
| h      |       |      | 0.40       |        |       | 0.016      |
| k      | 0     |      | 8 degrees  | 0      |       | 8 degrees  |
| L      | 0.60  |      | 1.00       | 0.024  |       | 0.039      |
| M      |       | 4.30 |            |        | 0.169 |            |
| N      |       |      | 10 degrees |        |       | 10 degrees |
| O      |       | 1.20 |            |        | 0.047 |            |
| Q      |       | 0.80 |            |        | 0.031 |            |
| S      |       | 2.90 |            |        | 0.114 |            |
| T      |       | 3.65 |            |        | 0.144 |            |
| U      |       | 1.00 |            |        | 0.039 |            |
| X      | 4.10  |      | 4.70       | 0.161  |       | 0.185      |
| Y      | 4.90  |      | 7.10       | 0.193  |       | 0.280      |

## 9.2 PowerSSO-36 with exposed pad up

Figure 61. PowerSSO-36 EPU package outline



7618147\_6

**Table 10. PowerSSO-36 EPU package mechanical data**

| Symbol | mm    |      |            | Inches |       |            |
|--------|-------|------|------------|--------|-------|------------|
|        | Min.  | Typ. | Max.       | Min.   | Typ.  | Max.       |
| A      | 2.15  | -    | 2.45       | 0.085  | -     | 0.096      |
| A2     | 2.15  | -    | 2.35       | 0.085  | -     | 0.093      |
| a1     | 0     | -    | 0.10       | 0      | -     | 0.004      |
| b      | 0.18  | -    | 0.36       | 0.007  | -     | 0.014      |
| c      | 0.23  | -    | 0.32       | 0.009  | -     | 0.013      |
| D      | 10.10 | -    | 10.50      | 0.398  | -     | 0.413      |
| E      | 7.40  | -    | 7.60       | 0.291  | -     | 0.299      |
| e      | -     | 0.5  | -          | -      | 0.020 | -          |
| e3     | -     | 8.5  | -          | -      | 0.335 | -          |
| F      | -     | 2.3  | -          | -      | 0.091 | -          |
| G      | -     | -    | 0.10       | -      | -     | 0.004      |
| H      | 10.10 | -    | 10.50      | 0.398  | -     | 0.413      |
| h      | -     | -    | 0.40       | -      | -     | 0.016      |
| k      | 0     | -    | 8 degrees  | -      | -     | 8 degrees  |
| L      | 0.60  | -    | 1.00       | 0.024  | -     | 0.039      |
| M      | -     | 4.30 | -          | -      | 0.169 | -          |
| N      | -     | -    | 10 degrees | -      | -     | 10 degrees |
| O      | -     | 1.20 | -          | -      | 0.047 | -          |
| Q      | -     | 0.80 | -          | -      | 0.031 | -          |
| S      | -     | 2.90 | -          | -      | 0.114 | -          |
| T      | -     | 3.65 | -          | -      | 0.144 | -          |
| U      | -     | 1.00 | -          | -      | 0.039 | -          |
| X      | 4.10  | -    | 4.70       | 0.161  | -     | 0.185      |
| Y      | 6.50  | -    | 7.10       | 0.256  | -     | 0.280      |

## Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                             |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 02-Jul-2008 | 1        | Initial release.                                                                                                                                                                                                                                                                                                                                                    |
| 03-Oct-2008 | 2        | Updated AMR table<br>Updated Chapter 4: Characterization curves on page 12<br>Added Figure 48: Test board (TDA7491HV) layout on page 29<br>Updated Figure 49: PowerSSO-36 EPD outline drawing on page 30 and Table 6: PowerSSO-36 EPD dimensions on page 31<br>Updated Figure 50: Applications circuit for class-D amplifier on page 32                             |
| 29-Jun-2009 | 3        | Updated text concerning oscillator R and C in Section 3.3: Electrical specifications on page 10<br>Updated VOVP minimum value, added VUVP maximum value, updated STBY and MUTE voltages in Table 5: Electrical specifications on page 10<br>Updated equation for fSW Table 5 on page 10<br>Updated Figure 50: Applications circuit for class-D amplifier on page 32 |
| 03-Sep-2009 | 4        | Added text for exposed pad in Figure 2 on page 8<br>Added text for exposed pad in Table 2 on page 9<br>Updated exposed pad Y (Min) dimension in Table 6 on page 31<br>Updated supply voltage for pin DIAG pull-up resistor in Section 7.8 on page 40.                                                                                                               |
| 24-Mar-2011 | 5        | Updated Features<br>Updated Section 3: Electrical specifications<br>Removed filter less operation<br>Extended the temperature range to -40 to +85°C.                                                                                                                                                                                                                |
| 12Sep-2011  | 6        | Updated OUTNA in Table 2: Pin description list                                                                                                                                                                                                                                                                                                                      |
| 20-Feb-2014 | 7        | Updated order code Table 1 on page 1                                                                                                                                                                                                                                                                                                                                |
| 04-Jul-2018 | 8        | Added PowerSSO-36 EPU silhouette in cover page, Section 2.3 Pinout (EPU), Section 2.4 Pin list (EPU) and Section 9.2 PowerSSO-36 with exposed pad up.                                                                                                                                                                                                               |
| 05-Oct-2018 | 9        | Updated product summary table in cover page.                                                                                                                                                                                                                                                                                                                        |

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