# S-5725 Series

## HIGH-SPEED BIPOLAR HALL EFFECT LATCH

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Rev.2.5_02

The S-5725 Series, developed by CMOS technology, is a high-accuracy Hall IC that operates with a high-sensitivity, a high-speed detection and low current consumption.
The output voltage changes when the S-5725 Series detects the intensity level of magnetic flux density and a polarity change. Using the S-5725 Series with a magnet makes it possible to detect the rotation status in various devices.
High-density mounting is possible by using the small SOT-23-3 or the super-small SNT-4A packages.
Due to its high-accuracy magnetic characteristics, the S-5725 Series can make operation's dispersion in the system combined with magnet smaller.

**Caution** **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

## ■ Features

- Pole detection: Bipolar latch
- Detection logic for magnetism*1: $V_{OUT}$ = "L" at S pole detection
  $V_{OUT}$ = "H" at S pole detection
- Output form*1: Nch open-drain output, CMOS output
- Magnetic sensitivity*1: $B_{OP}$ = 0.8 mT typ.
  $B_{OP}$ = 1.8 mT typ.
  $B_{OP}$ = 3.0 mT typ.
  $B_{OP}$ = 7.0 mT typ.
- Operating cycle (current consumption)*1: $t_{CYCLE}$ = 50 μs ($I_{DD}$ = 1400.0 μA) typ.
  $t_{CYCLE}$ = 1.25 ms ($I_{DD}$ = 60.0 μA) typ.
  $t_{CYCLE}$ = 6.05 ms ($I_{DD}$ = 13.0 μA) typ.
- Power supply voltage range: $V_{DD}$ = 2.7 V to 5.5 V
- Operation temperature range: Ta = −40°C to +85°C
- Built-in power-down circuit: Extends battery life (only SNT-4A)
- Lead-free (Sn 100%), halogen-free

***1.** The option can be selected.

## ■ Applications

- Plaything, portable game
- Home appliance
- Housing equipment
- Industrial equipment

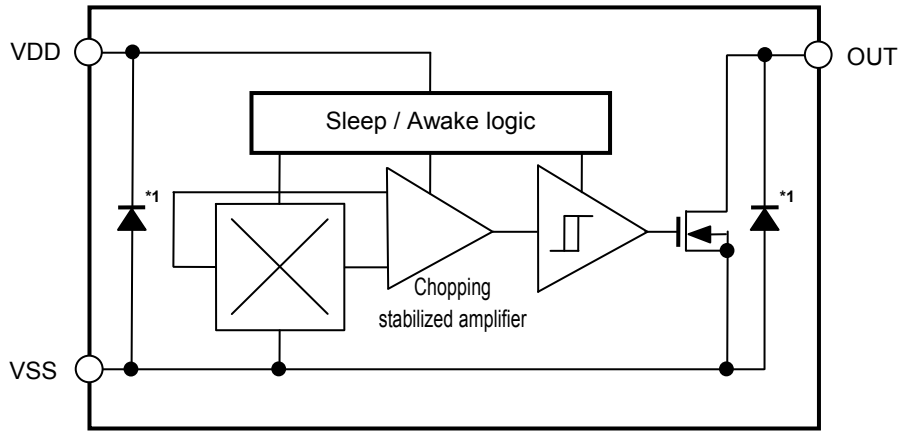
## ■ Packages

- SOT-23-3
- SNT-4A

## ■ Block Diagrams

### 1. Nch open-drain output product

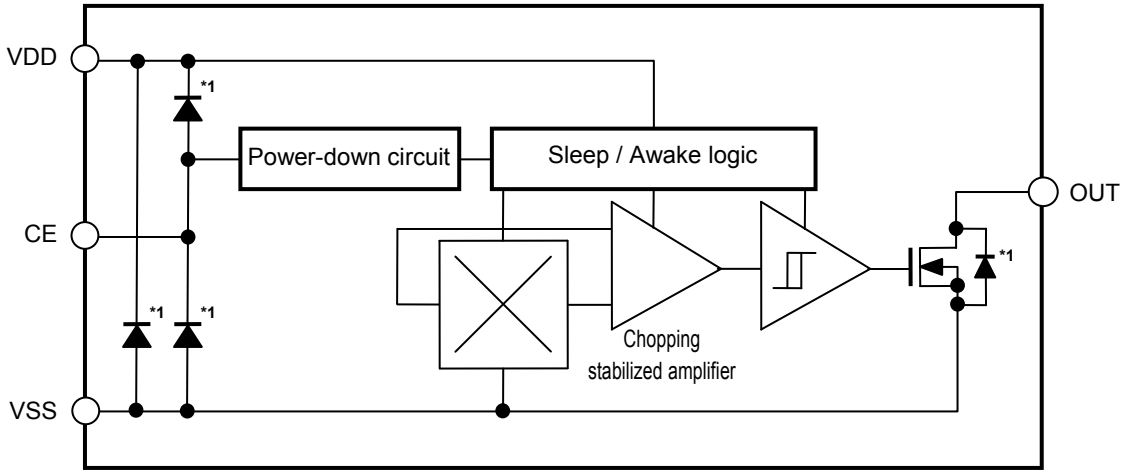
#### 1. 1 Product without power-down function




***1.** Parasitic diode

**Figure 1**

#### 1. 2 Product with power-down function (SNT-4A)

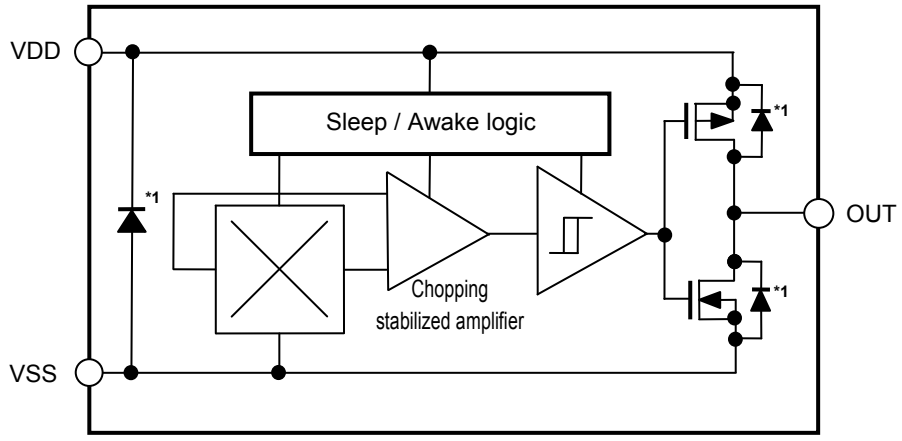



***1.** Parasitic diode

**Figure 2**

## 2. CMOS output product

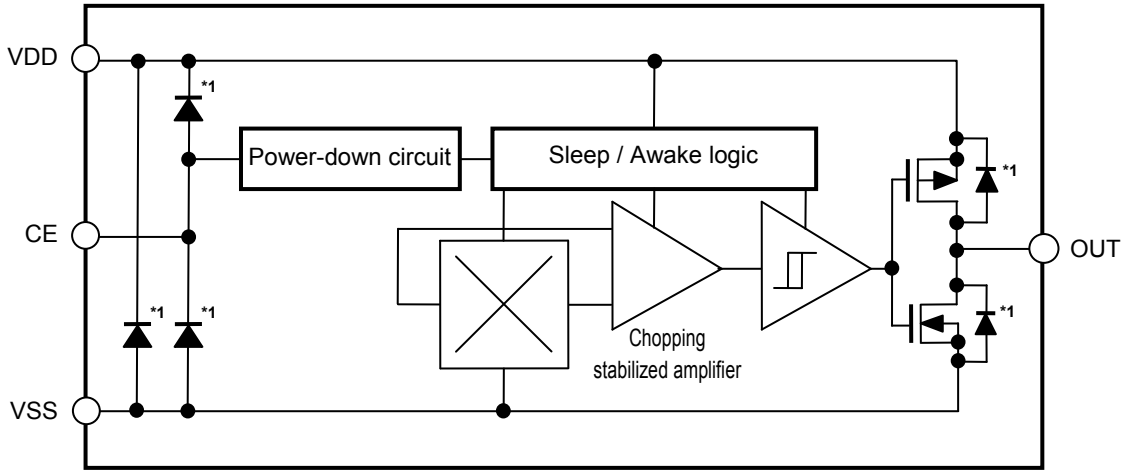
### 2. 1 Product without power-down function




***1.** Parasitic diode

**Figure 3**

### 2. 2 Product with power-down function (SNT-4A)

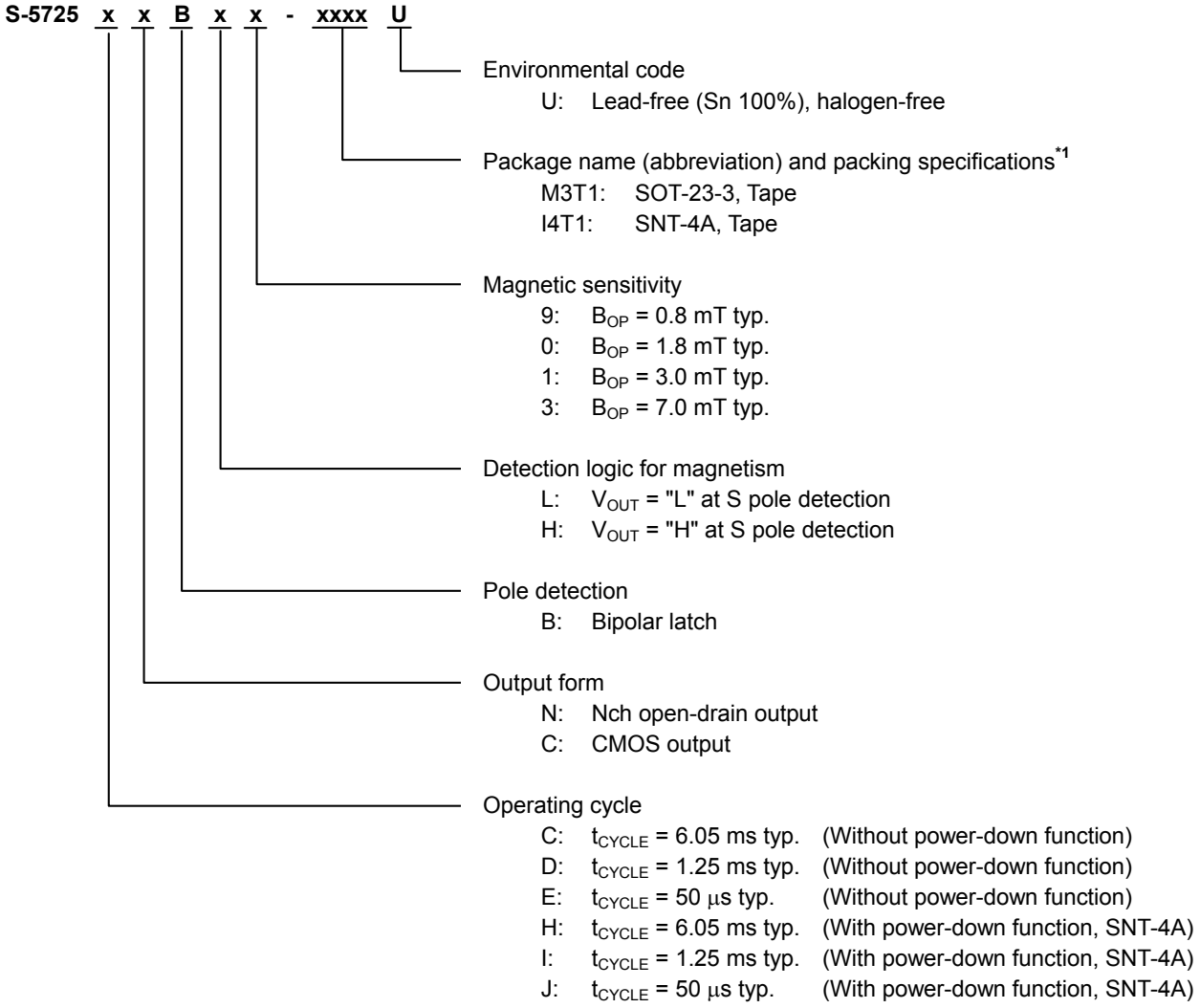



***1.** Parasitic diode

**Figure 4**

## ■ Product Name Structure

### 1. Product name




***1.** Refer to the tape drawing.

### 2. Packages

**Table 1 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| SOT-23-3 | MP003-C-P-SD | MP003-C-C-SD | MP003-Z-R-SD | – |
| SNT-4A | PF004-A-P-SD | PF004-A-C-SD | PF004-A-R-SD | PF004-A-L-SD |

## 3. Product name list

### 3. 1 SOT-23-3

#### 3. 1. 1 Nch open-drain output product

**Table 2**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Power-down Function | Output Form | Pole Detection | Detection Logic for Magnetism | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|---|
| S-5725CNBL9-M3T1U | 6.05 ms typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 0.8 mT typ. |
| S-5725CNBL0-M3T1U | 6.05 ms typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 1.8 mT typ. |
| S-5725CNBL1-M3T1U | 6.05 ms typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725DNBL1-M3T1U | 1.25 ms typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725ENBL9-M3T1U | 50 μs typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 0.8 mT typ. |
| S-5725ENBL0-M3T1U | 50 μs typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 1.8 mT typ. |
| S-5725ENBL1-M3T1U | 50 μs typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725ENBH1-M3T1U | 50 μs typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |

**Remark** Please contact our sales office for products other than the above.

#### 3. 1. 2 CMOS output product

**Table 3**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Power-down Function | Output Form | Pole Detection | Detection Logic for Magnetism | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|---|
| S-5725CCBL9-M3T1U | 6.05 ms typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 0.8 mT typ. |
| S-5725CCBL0-M3T1U | 6.05 ms typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 1.8 mT typ. |
| S-5725CCBL1-M3T1U | 6.05 ms typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725DCBL1-M3T1U | 1.25 ms typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725ECBL9-M3T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 0.8 mT typ. |
| S-5725ECBL0-M3T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 1.8 mT typ. |
| S-5725ECBL1-M3T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 3.0 mT typ. |
| S-5725ECBH0-M3T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725ECBH1-M3T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |

**Remark** Please contact our sales office for products other than the above.

### 3. 2 SNT-4A

#### 3. 2. 1 Nch open-drain output product

**Table 4**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Power-down Function | Output Form | Pole Detection | Detection Logic for Magnetism | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|---|
| S-5725ENBH3-I4T1U | 50 μs typ. | Unavailable | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 7.0 mT typ. |
| S-5725HNBH0-I4T1U | 6.05 ms typ. | Available | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725INBH0-I4T1U | 1.25 ms typ. | Available | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725JNBH0-I4T1U | 50 μs typ. | Available | Nch open-drain output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |

**Remark** Please contact our sales office for products other than the above.

#### 3. 2. 2 CMOS output product

**Table 5**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Power-down Function | Output Form | Pole Detection | Detection Logic for Magnetism | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|---|
| S-5725ECBL9-I4T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 0.8 mT typ. |
| S-5725ECBL0-I4T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "L" at S pole detection | 1.8 mT typ. |
| S-5725ECBH0-I4T1U | 50 μs typ. | Unavailable | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725HCBH0-I4T1U | 6.05 ms typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725HCBH1-I4T1U | 6.05 ms typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |
| S-5725ICBH0-I4T1U | 1.25 ms typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725ICBH1-I4T1U | 1.25 ms typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |
| S-5725JCBH0-I4T1U | 50 μs typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 1.8 mT typ. |
| S-5725JCBH1-I4T1U | 50 μs typ. | Available | CMOS output | Bipolar latch | $V_{OUT}$ = "H" at S pole detection | 3.0 mT typ. |

**Remark** Please contact our sales office for products other than the above.

## ■ Pin Configurations

### 1. SOT-23-3

Top view

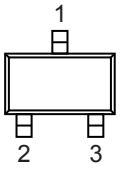



**Figure 5**

**Table 6**

| Pin No. | Symbol | Pin Description |
|---|---|---|
| 1 | VSS | GND pin |
| 2 | VDD | Power supply pin |
| 3 | OUT | Output pin |

### 2. SNT-4A

Top view

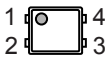



**Figure 6**

**Table 7**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Power supply pin |
| 2 | VSS | GND pin |
| 3 | CE | Enabling pin<br>"H": Enables operation<br>"L": Power-down |
| 4 | OUT | Output pin |

## ■ Absolute Maximum Ratings

**Table 8**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{DD}$ | $V_{SS}$ − 0.3 to $V_{SS}$ + 7.0 | V |
| Input voltage | | $V_{CE}$ | $V_{SS}$ − 0.3 to $V_{DD}$ + 0.3 | V |
| Output current | | $I_{OUT}$ | ±2.0 | mA |
| Output voltage | Nch open-drain output product | $V_{OUT}$ | $V_{SS}$ − 0.3 to $V_{SS}$ + 7.0 | V |
| | CMOS output product | | $V_{SS}$ − 0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | SOT-23-3 | $P_D$ | 430[*1] | mW |
| | SNT-4A | | 300[*1] | mW |
| Operation ambient temperature | | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | −40 to +125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

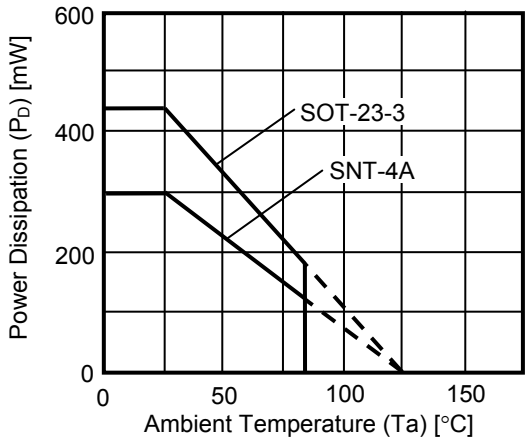



**Figure 7 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

### 1. Product without power-down function

#### 1. 1 S-5725CxBxx

**Table 9**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 13.0 | 20.0 | μA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = −2 mA | $V_{DD}$ − 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.05 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 6.00 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 6.05 | 12.00 | ms | – |

#### 1. 2 S-5725DxBxx

**Table 10**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 60.0 | 90.0 | μA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = −2 mA | $V_{DD}$ − 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.05 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 1.20 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 1.25 | 2.50 | ms | – |

### 1. 3 S-5725ExBxx

**Table 11**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 1400.0 | 2000.0 | μA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = –2 mA | $V_{DD}$ – 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product<br>Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 50 | – | μs | – |
| Sleep mode time | $t_{SL}$ | – | | – | 0 | – | μs | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 50 | 100 | μs | – |

## 2. Product with power-down function (SNT-4A)

### 2. 1 S-5725HxBxx

**Table 12**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 13.0 | 20.0 | μA | 1 |
| Current consumption during power-down | $I_{DD2}$ | $V_{CE}$ = $V_{SS}$ | | – | – | 1 | μA | 6 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = –2 mA | $V_{DD}$ – 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product<br>Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.05 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 6.00 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 6.05 | 12.00 | ms | – |
| Enabling pin input voltage "L" | $V_{CEL}$ | – | | – | – | $V_{DD}$ × 0.3 | V | – |
| Enabling pin input voltage "H" | $V_{CEH}$ | – | | $V_{DD}$ × 0.7 | – | – | V | – |
| Enabling pin input current "L" | $I_{CEL}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 0 V | | –1 | – | 1 | μA | 7 |
| Enabling pin input current "H" | $I_{CEH}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 5.0 V | | –1 | – | 1 | μA | 8 |
| Power-down transition time | $t_{OFF}$ | – | | – | – | 100 | μs | – |
| Enable transition time | $t_{ON}$ | – | | – | – | 100 | μs | – |
| Output logic update time after inputting "H" to enabling pin | $t_{OE}$ | – | | – | – | 200 | μs | – |

### 2. 2 S-5725IxBxx

**Table 13**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 60.0 | 90.0 | μA | 1 |
| Current consumption during power-down | $I_{DD2}$ | $V_{CE}$ = $V_{SS}$ | | – | – | 1 | μA | 6 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = −2 mA | $V_{DD}$ − 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product<br>Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.05 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 1.20 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 1.25 | 2.50 | ms | – |
| Enabling pin input voltage "L" | $V_{CEL}$ | – | | – | – | $V_{DD}$ × 0.3 | V | – |
| Enabling pin input voltage "H" | $V_{CEH}$ | – | | $V_{DD}$ × 0.7 | – | – | V | – |
| Enabling pin input current "L" | $I_{CEL}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 0 V | | −1 | – | 1 | μA | 7 |
| Enabling pin input current "H" | $I_{CEH}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 5.0 V | | −1 | – | 1 | μA | 8 |
| Power-down transition time | $t_{OFF}$ | – | | – | – | 100 | μs | – |
| Enable transition time | $t_{ON}$ | – | | – | – | 100 | μs | – |
| Output logic update time after inputting "H" to enabling pin | $t_{OE}$ | – | | – | – | 200 | μs | – |

### 2. 3 S-5725JxBxx

**Table 14**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 1400.0 | 2000.0 | μA | 1 |
| Current consumption during power-down | $I_{DD2}$ | $V_{CE}$ = $V_{SS}$ | | – | – | 1 | μA | 6 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT}$ = 2 mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT}$ = −2 mA | $V_{DD}$ − 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product<br>Output transistor Nch, $V_{OUT}$ = 5.5 V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 50 | – | μs | – |
| Sleep mode time | $t_{SL}$ | – | | – | 0 | – | μs | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW}$ + $t_{SL}$ | | – | 50 | 100 | μs | – |
| Enabling pin input voltage "L" | $V_{CEL}$ | – | | – | – | $V_{DD}$ × 0.3 | V | – |
| Enabling pin input voltage "H" | $V_{CEH}$ | – | | $V_{DD}$ × 0.7 | – | – | V | – |
| Enabling pin input current "L" | $I_{CEL}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 0 V | | −1 | – | 1 | μA | 7 |
| Enabling pin input current "H" | $I_{CEH}$ | $V_{DD}$ = 5.0 V, $V_{CE}$ = 5.0 V | | −1 | – | 1 | μA | 8 |
| Power-down transition time | $t_{OFF}$ | – | | – | – | 100 | μs | – |
| Enable transition time | $t_{ON}$ | – | | – | – | 100 | μs | – |
| Output logic update time after inputting "H" to enabling pin | $t_{OE}$ | – | | – | – | 200 | μs | – |

## ■ Magnetic Characteristics

### 1. Product with $B_{OP}$ = 0.8 mT typ.

**Table 15**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OP}$ | – | 0.1 | 0.8 | 1.5 | mT | 5 |
| Release point*2 | N pole | $B_{RP}$ | – | −1.5 | −0.8 | −0.1 | mT | 5 |
| Hysteresis width*3 | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 1.6 | – | mT | 5 |

### 2. Product with $B_{OP}$ = 1.8 mT typ.

**Table 16**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OP}$ | – | 0.9 | 1.8 | 2.7 | mT | 5 |
| Release point*2 | N pole | $B_{RP}$ | – | −2.7 | −1.8 | −0.9 | mT | 5 |
| Hysteresis width*3 | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 3.6 | – | mT | 5 |

### 3. Product with $B_{OP}$ = 3.0 mT typ.

**Table 17**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OP}$ | – | 1.4 | 3.0 | 4.0 | mT | 5 |
| Release point*2 | N pole | $B_{RP}$ | – | −4.0 | −3.0 | −1.4 | mT | 5 |
| Hysteresis width*3 | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 6.0 | – | mT | 5 |

### 4. Product with $B_{OP}$ = 7.0 mT typ.

**Table 18**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OP}$ | – | 5.0 | 7.0 | 8.5 | mT | 5 |
| Release point*2 | N pole | $B_{RP}$ | – | −8.5 | −7.0 | −5.0 | mT | 5 |
| Hysteresis width*3 | | $B_{HYS}$ | $B_{HYS} = B_{OP} - B_{RP}$ | – | 14.0 | – | mT | 5 |

***1.** $B_{OP}$: Operation point
$B_{OP}$ is the value of magnetic flux density when the output voltage ($V_{OUT}$) changes after the magnetic flux density applied to the S-5725 Series by the magnet (S pole) is increased (by moving the magnet closer).
$V_{OUT}$ retains the status until a magnetic flux density of the N pole higher than $B_{RP}$ is applied.

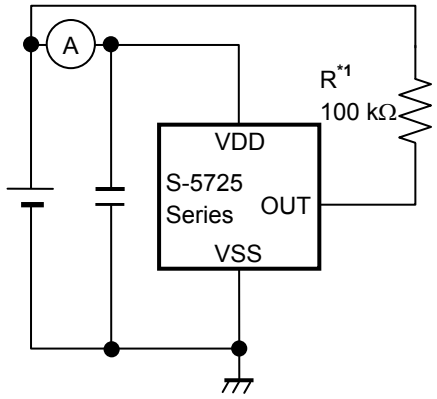
***2.** $B_{RP}$: Release point
$B_{RP}$ is the value of magnetic flux density when the output voltage ($V_{OUT}$) changes after the magnetic flux density applied to the S-5725 Series by the magnet (N pole) is increased (by moving the magnet closer).
$V_{OUT}$ retains the status until a magnetic flux density of the S pole higher than $B_{OP}$ is applied.

***3.** $B_{HYS}$: Hysteresis width
$B_{HYS}$ is the difference between $B_{OP}$ and $B_{RP}$.

**Remark** The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

## ■ Test Circuits

### 1. Product without power-down function




*1. Resistor (R) is unnecessary for the CMOS output product.

**Figure 8 Test Circuit 1**

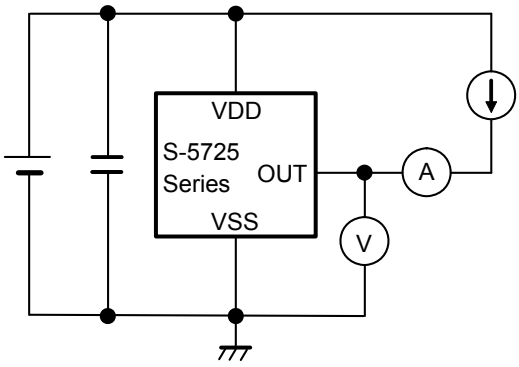



**Figure 9 Test Circuit 2**

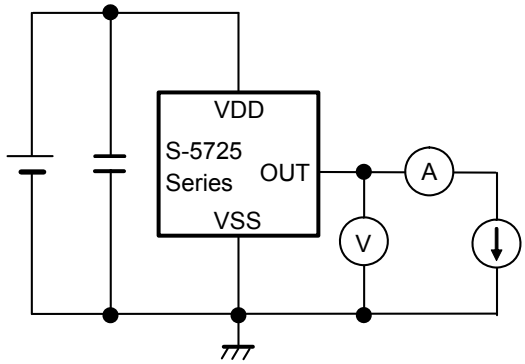



**Figure 10 Test Circuit 3**

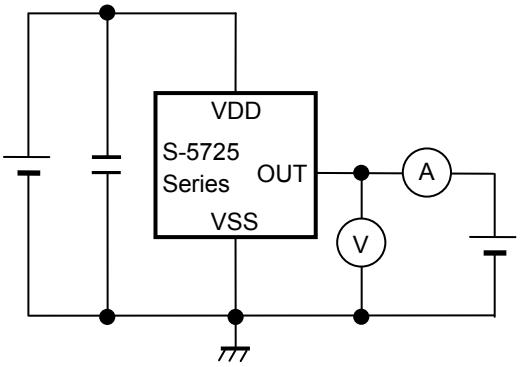
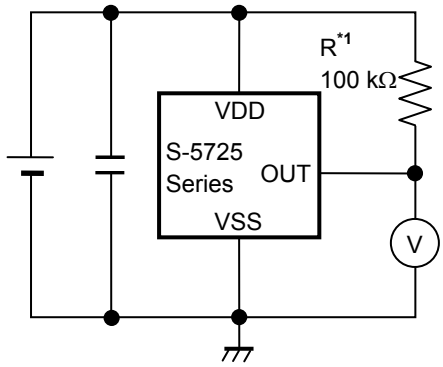


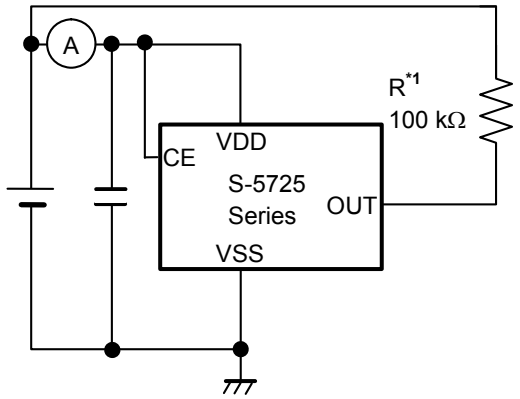

**Figure 11 Test Circuit 4**




*1. Resistor (R) is unnecessary for the CMOS output product.

**Figure 12 Test Circuit 5**

**2. Product with power-down function (SNT-4A)**




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 13 Test Circuit 1**

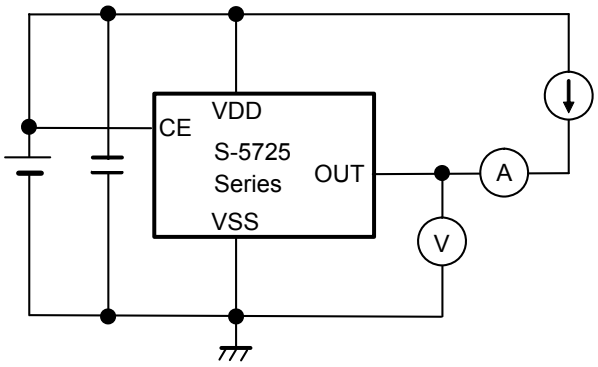



**Figure 14 Test Circuit 2**

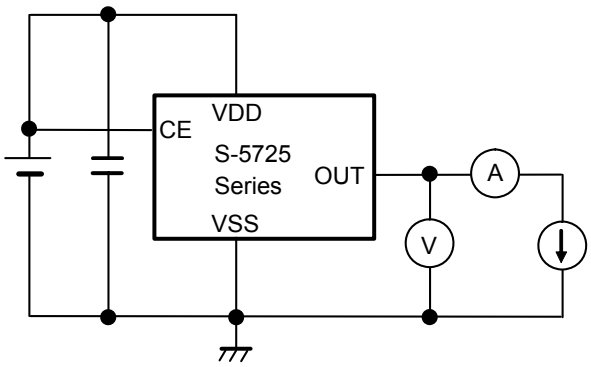



**Figure 15 Test Circuit 3**

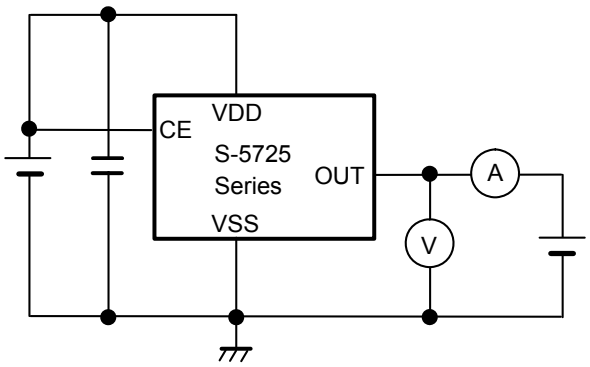
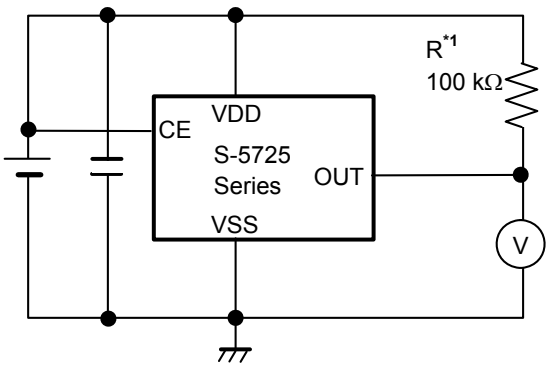
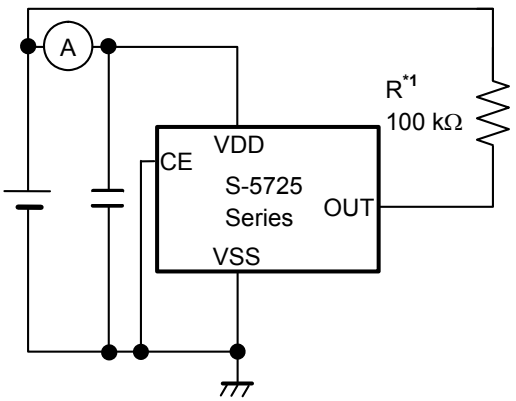



**Figure 16 Test Circuit 4**




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 17 Test Circuit 5**




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 18 Test Circuit 6**

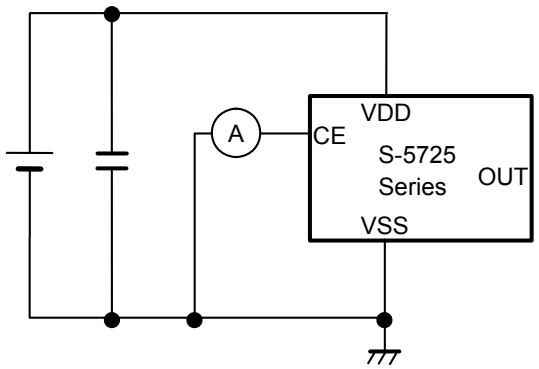



Figure 19 Test Circuit 7

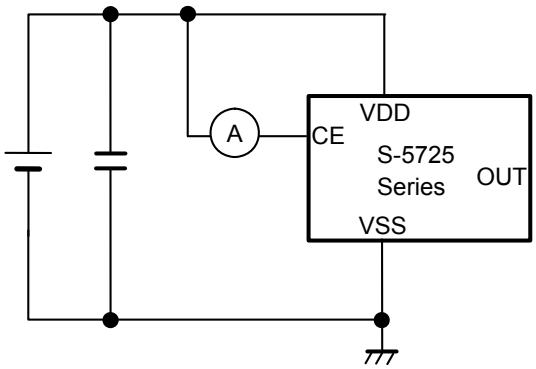
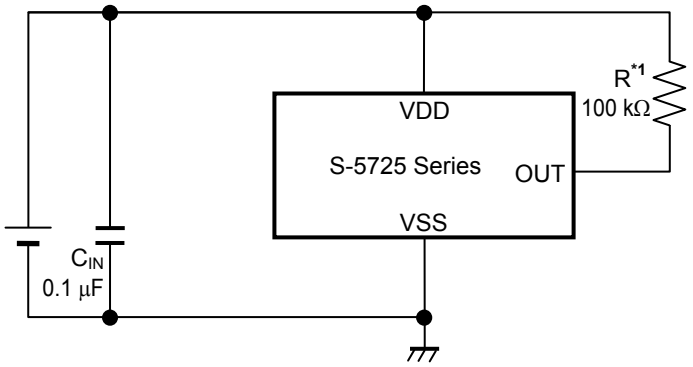



Figure 20 Test Circuit 8

## ■ Standard Circuits

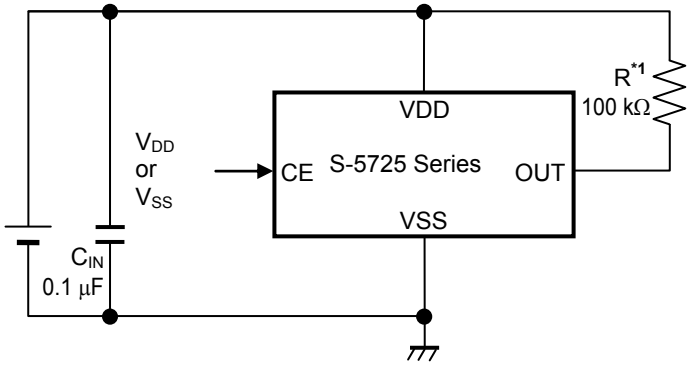
### 1. Product without power-down function




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 21**

### 2. Product with power-down function (SNT-4A)




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 22**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Operation

### 1. Direction of applied magnetic flux

The S-5725 Series detects the magnetic flux density which is vertical to the marking surface.
**Figure 23** and **Figure 24** show the direction in which magnetic flux is being applied.

**1. 1 SOT-23-3**

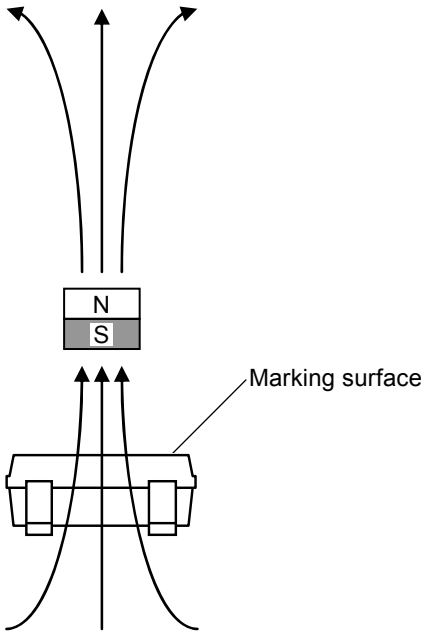



**Figure 23**

**1. 2 SNT-4A**

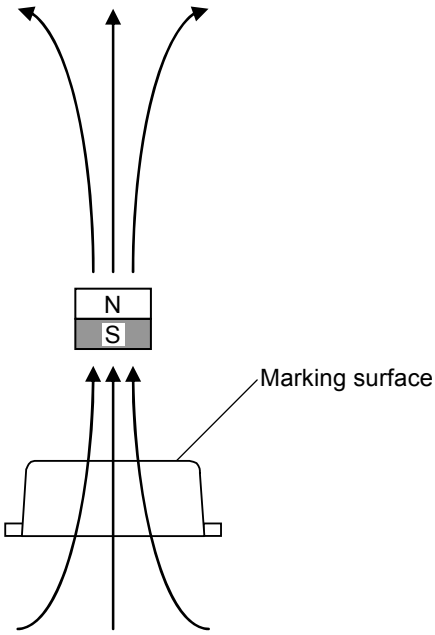



**Figure 24**

### 2. Position of Hall sensor

**Figure 25** and **Figure 26** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

**2. 1 SOT-23-3**

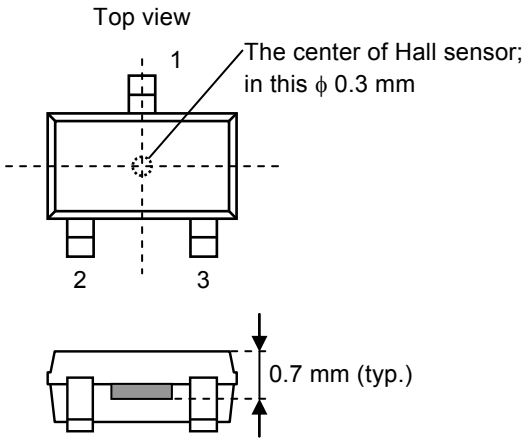



**Figure 25**

**2. 2 SNT-4A**

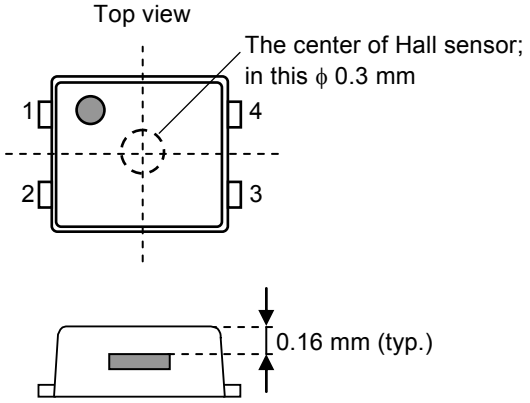



**Figure 26**

## 3. Basic operation

The S-5725 Series changes the output voltage ($V_{OUT}$) according to the level of the magnetic flux density and a polarity change (N pole or S pole) applied by a magnet.
Definition of the magnetic field is performed every operating cycle indicated in "■ **Electrical Characteristics**".

### 3. 1 Product with $V_{OUT}$ = "L" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds the operation point ($B_{OP}$) after the S pole of a magnet is moved closer to the marking surface of the S-5725 Series, $V_{OUT}$ changes from "H" to "L". When the N pole of a magnet is moved closer to the marking surface of the S-5725 Series and the magnetic flux density of the N pole is higher than the release point ($B_{RP}$), $V_{OUT}$ changes from "L" to "H". In case of $B_{RP} < B < B_{OP}$, $V_{OUT}$ retains the status.
**Figure 27** shows the relationship between the magnetic flux density and $V_{OUT}$.

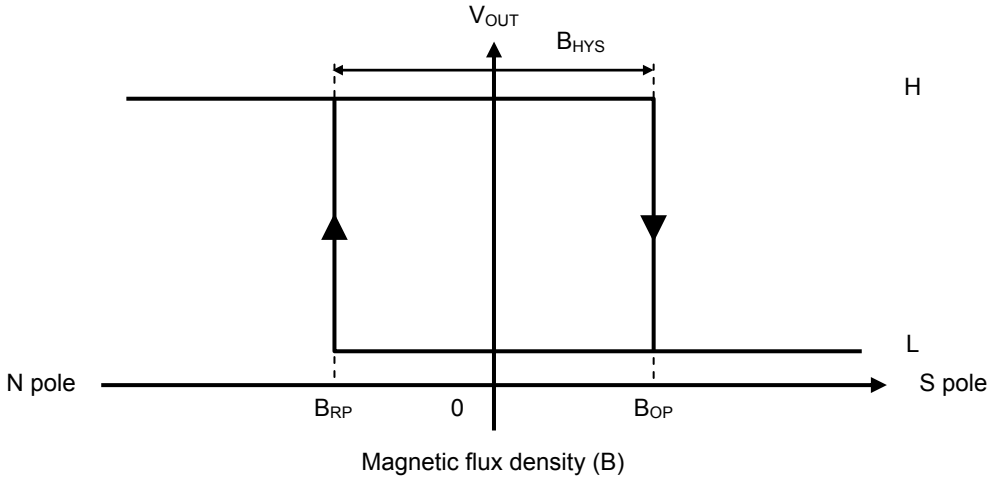



**Figure 27**

### 3. 2 Product with $V_{OUT}$ = "H" at S pole detection

When the magnetic flux density of the S pole perpendicular to the marking surface exceeds $B_{OP}$ after the S pole of a magnet is moved closer to the marking surface of the S-5725 Series, $V_{OUT}$ changes from "L" to "H". When the N pole of a magnet is moved closer to the marking surface of the S-5725 Series and the magnetic flux density of the N pole is higher than $B_{RP}$, $V_{OUT}$ changes from "H" to "L". In case of $B_{RP} < B < B_{OP}$, $V_{OUT}$ retains the status.
**Figure 28** shows the relationship between the magnetic flux density and $V_{OUT}$.

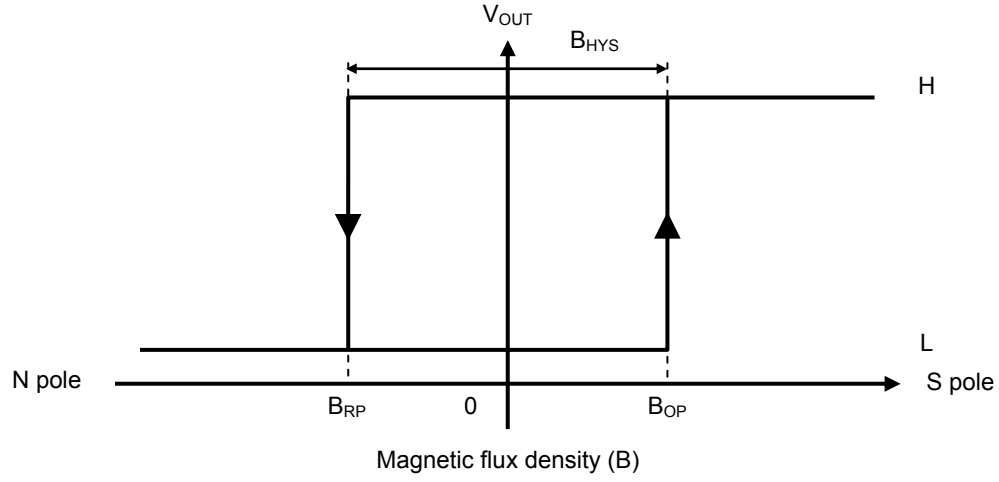



**Figure 28**

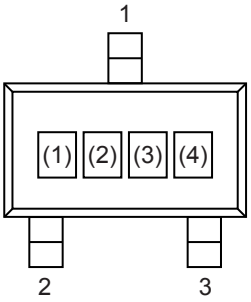
## ■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect on the magnetic characteristics. Avoid large stress which is caused by bend and distortion during mounting the IC on a board or handle after mounting.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Marking Specifications

### 1. SOT-23-3

Top view




(1) to (3): Product code (Refer to **Product name vs. Product code**.)
(4): Lot number

**Product name vs. Product code**

**1. 1 Nch open-drain output product**

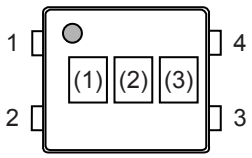
| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-5725CNBL9-M3T1U | X | 9 | R |
| S-5725CNBL0-M3T1U | X | 9 | S |
| S-5725CNBL1-M3T1U | X | 9 | J |
| S-5725DNBL1-M3T1U | X | 9 | K |
| S-5725ENBL9-M3T1U | X | 9 | V |
| S-5725ENBL0-M3T1U | X | 9 | A |
| S-5725ENBL1-M3T1U | X | 9 | B |
| S-5725ENBH1-M3T1U | X | 9 | L |

**1. 2 CMOS output product**

| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-5725CCBL9-M3T1U | X | 9 | P |
| S-5725CCBL0-M3T1U | X | 9 | Q |
| S-5725CCBL1-M3T1U | X | 9 | T |
| S-5725DCBL1-M3T1U | X | 9 | U |
| S-5725ECBL9-M3T1U | X | 9 | W |
| S-5725ECBL0-M3T1U | X | 9 | X |
| S-5725ECBL1-M3T1U | X | 9 | C |
| S-5725ECBH0-M3T1U | X | 9 | Z |
| S-5725ECBH1-M3T1U | X | 9 | Y |

## 2. SNT-4A

Top view




(1) to (3): Product code (Refer to **Product name vs. Product code**.)

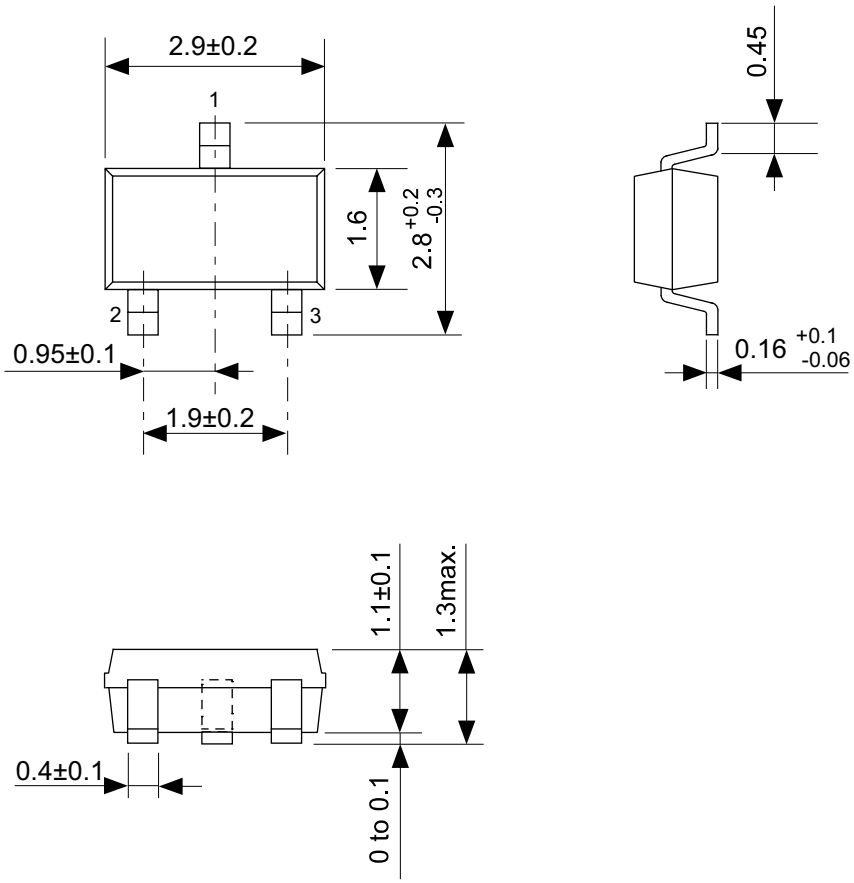
**Product name vs. Product code**

### 2. 1 Nch open-drain output product

| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-5725ENBH3-I4T1U | X | 8 | A |
| S-5725HNBH0-I4T1U | X | 9 | D |
| S-5725INBH0-I4T1U | X | 9 | F |
| S-5725JNBH0-I4T1U | X | 9 | H |

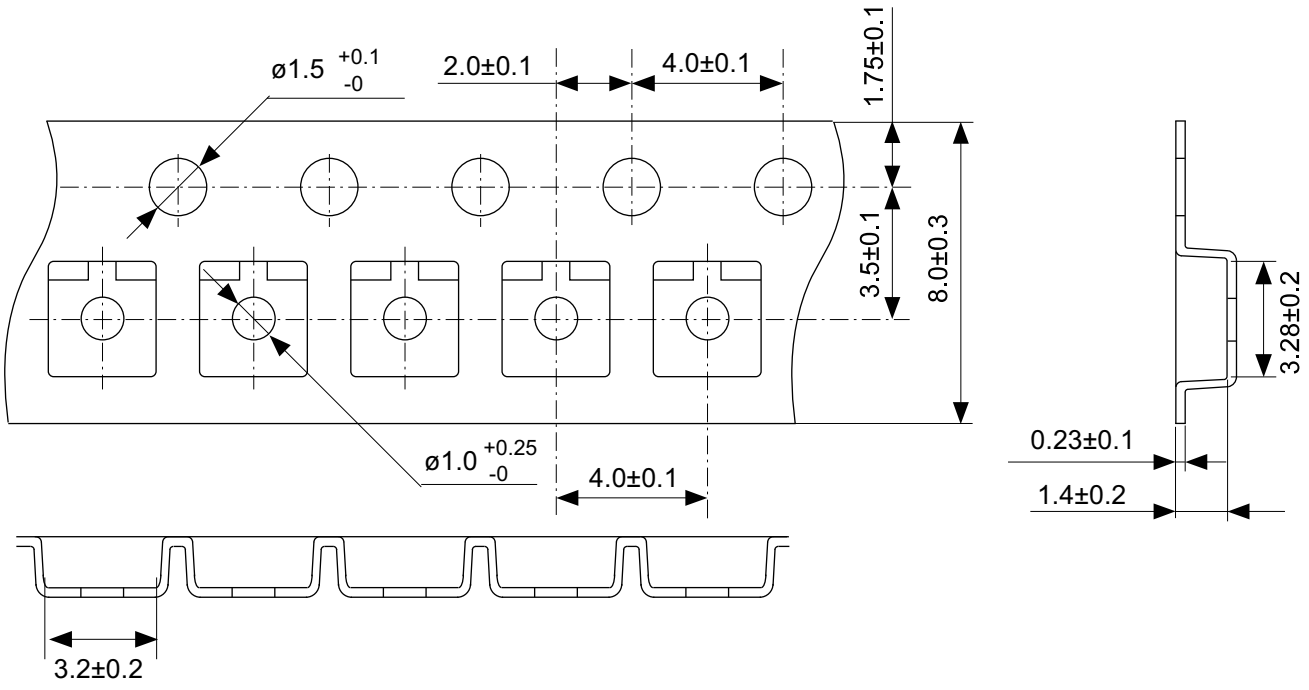
### 2. 2 CMOS output product

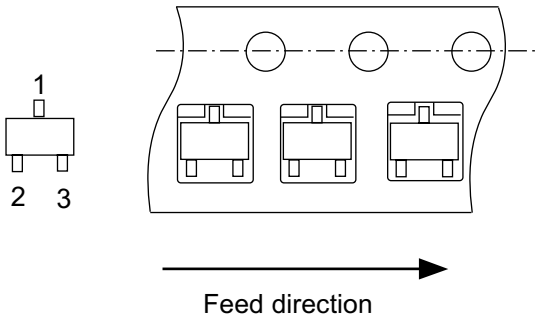
| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-5725ECBL9-I4T1U | X | 9 | W |
| S-5725ECBL0-I4T1U | X | 9 | X |
| S-5725ECBH0-I4T1U | X | 9 | Z |
| S-5725HCBH0-I4T1U | X | 9 | E |
| S-5725HCBH1-I4T1U | X | 9 | M |
| S-5725ICBH0-I4T1U | X | 9 | G |
| S-5725ICBH1-I4T1U | X | 9 | N |
| S-5725JCBH0-I4T1U | X | 9 | I |
| S-5725JCBH1-I4T1U | X | 9 | O |




No. MP003-C-P-SD-1.1

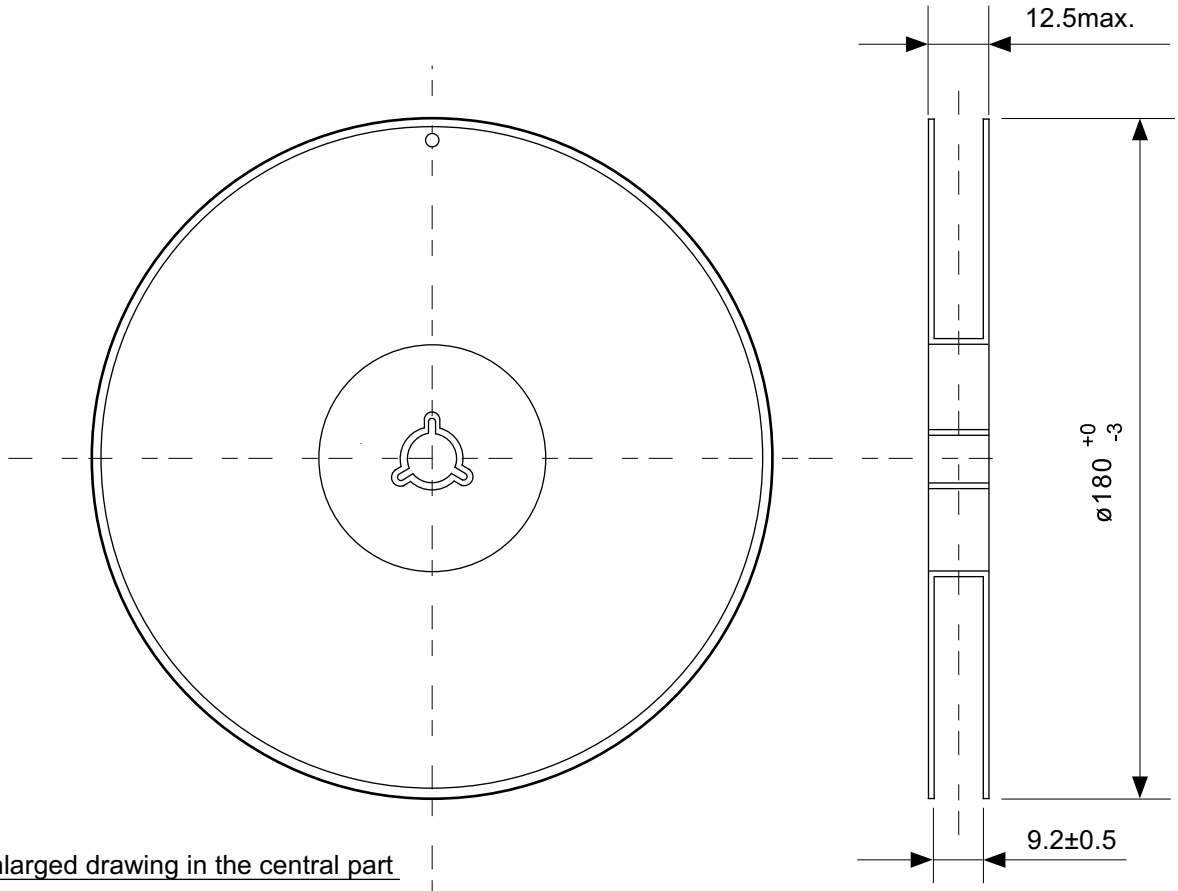
| | |
|---|---|
| TITLE | SOT233-C-PKG Dimensions |
| No. | MP003-C-P-SD-1.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |



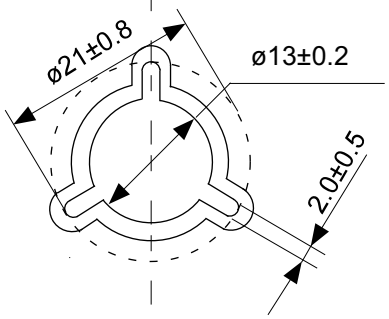




No. MP003-C-C-SD-2.0

| | |
|---|---|
| TITLE | SOT233-C-Carrier Tape |
| No. | MP003-C-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

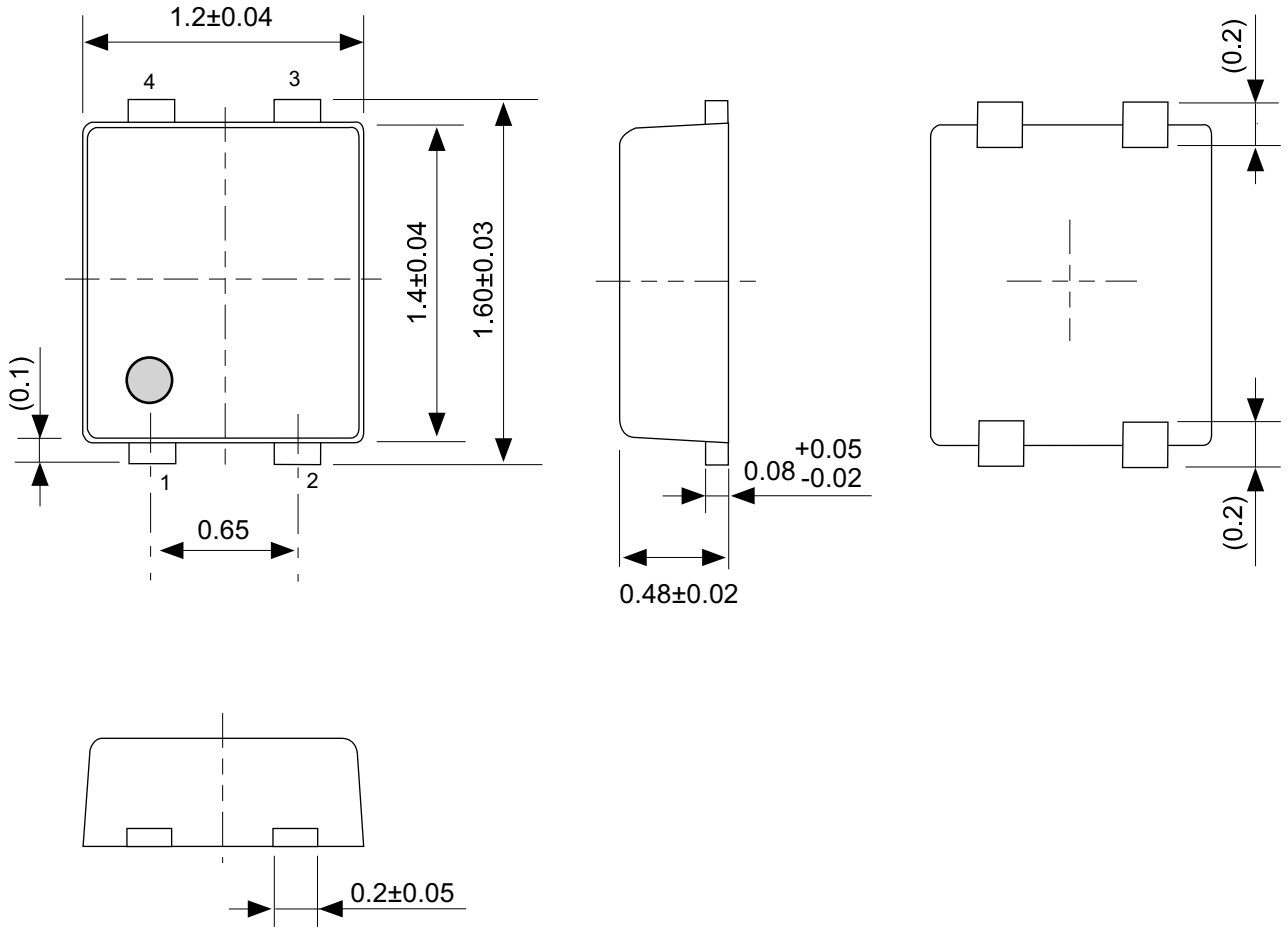



Enlargement drawing in the central part



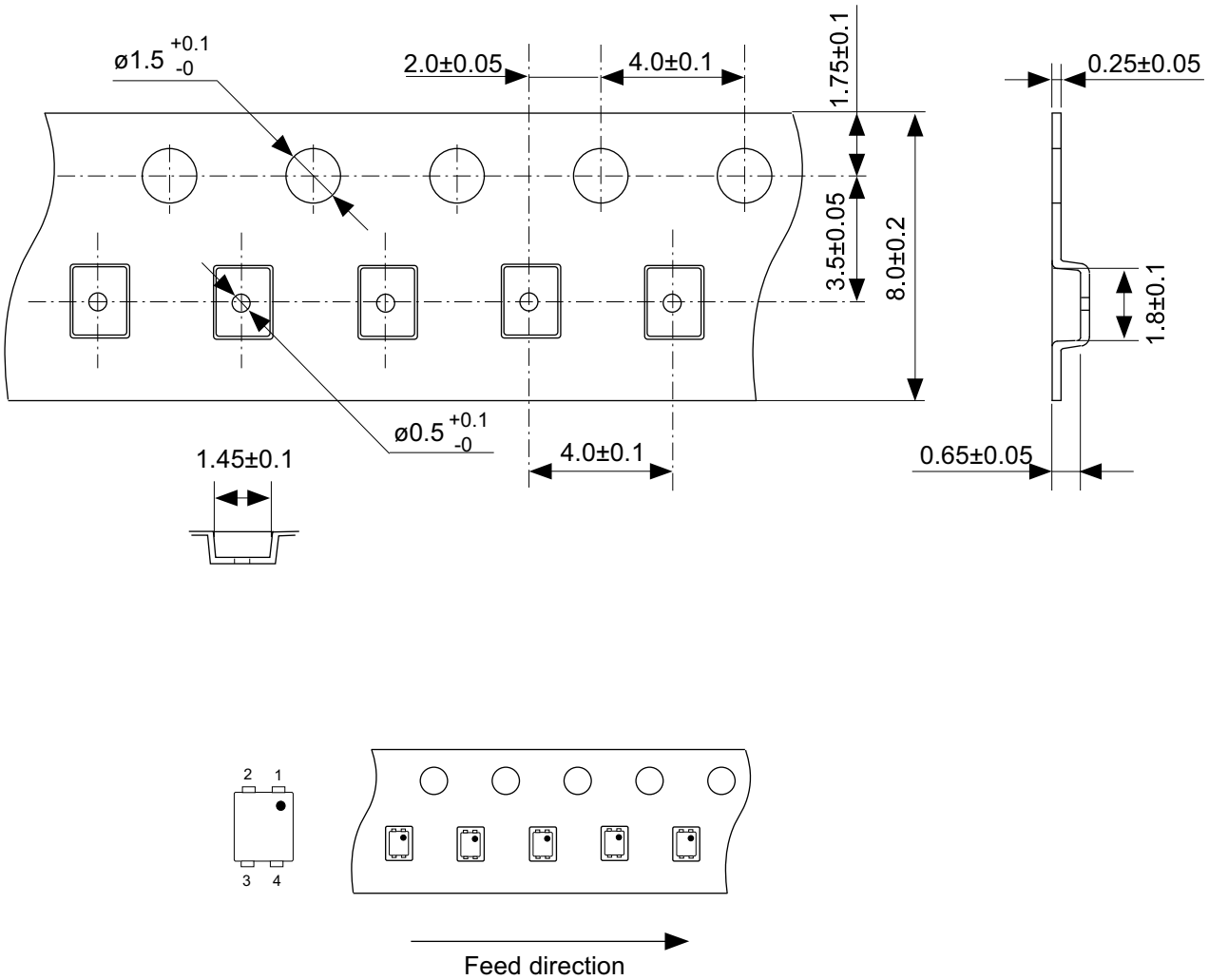

No. MP003-Z-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SOT233-C-Reel | | |
| No. | MP003-Z-R-SD-1.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |




No. PF004-A-P-SD-6.0

| | |
|---|---|
| TITLE | SNT-4A-A-PKG Dimensions |
| No. | PF004-A-P-SD-6.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |




No. PF004-A-C-SD-2.0

| | |
|---|---|
| TITLE | SNT-4A-A-Carrier Tape |
| No. | PF004-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |

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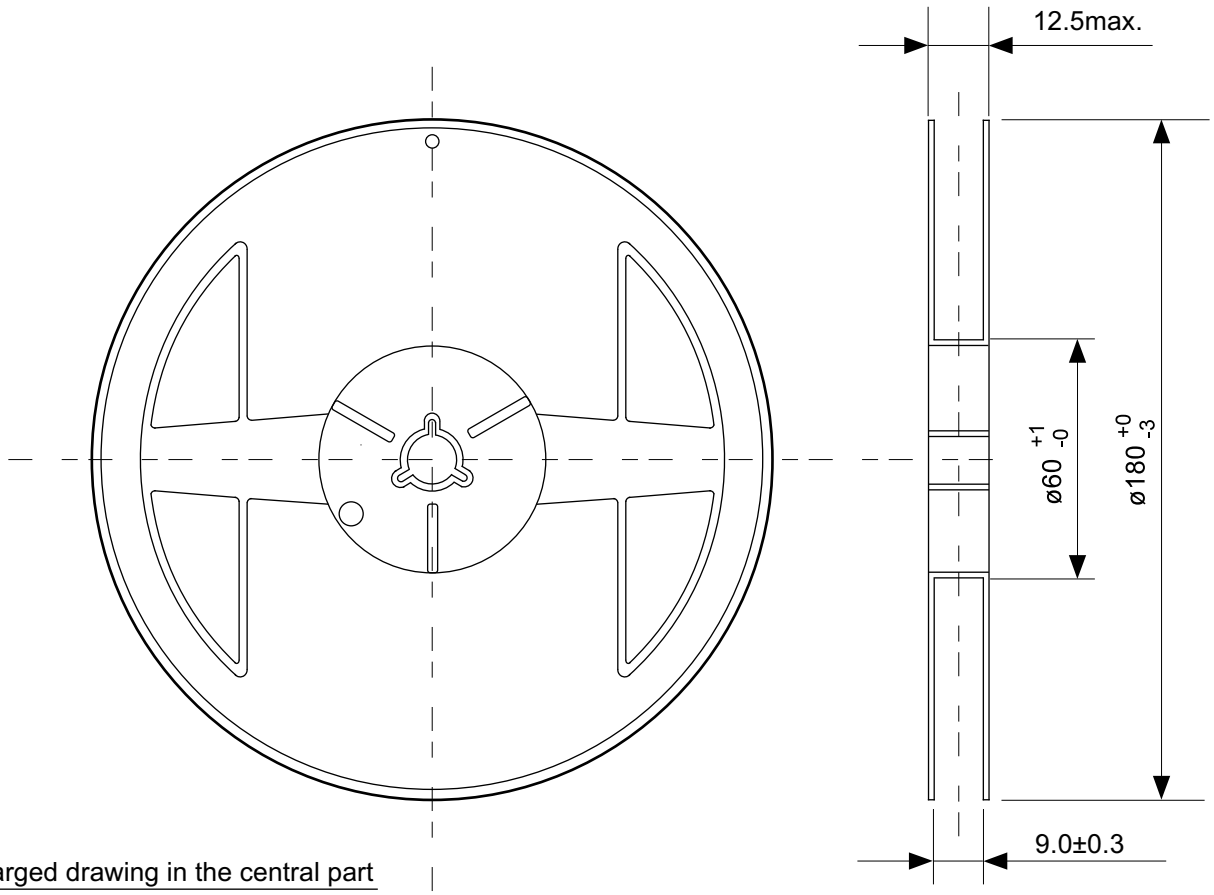
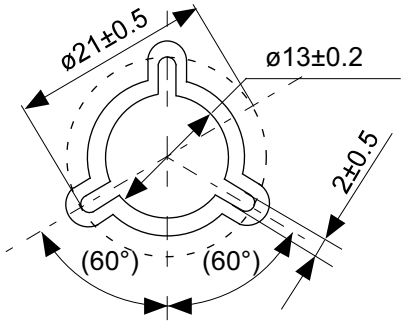



Enlarged drawing in the central part




No. PF004-A-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SNT-4A-A-Reel | | |
| No. | PF004-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
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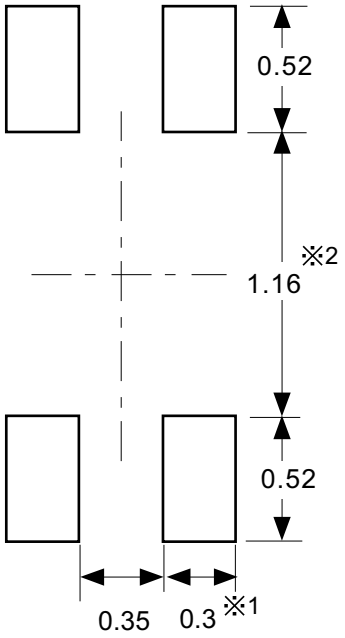


※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

**注意**
1. **パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。**
2. **パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。**
3. **マスク開口サイズと開口位置はランドパターンと合わせてください。**
4. **詳細は ″SNTパッケージ活用の手引き″ を参照してください。**

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

**Caution**
1. **Do not do silkscreen printing and solder printing under the mold resin of the package.**
2. **The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
3. **Match the mask aperture size and aperture position with the land pattern.**
4. **Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

**注意**
1. **请勿在树脂型封装的下面印刷丝网、焊锡。**
2. **在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
3. **钢网的开口尺寸和开口位置请与焊盘模式对齐。**
4. **详细内容请参阅 "SNT 封装的应用指南"。**

No. PF004-A-L-SD-4.1

| | |
|---|---|
| TITLE | SNT-4A-A<br>-Land Recommendation |
| No. | PF004-A-L-SD-4.1 |
| ANGLE | |
| UNIT | mm |
| | |

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2.4-2019.07

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