SL3S10x4

UCODE 7xm-1k, UCODE 7xm-2k and UCODE 7xm+

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1 General description

The UCODE 7xm series is the latest generation of NXP's memory UHF tag ICs. With the high performance read range UCODE 7xm is well suited for applications which require high read range and also demanding an extended user memory to store data specific to customer or products. UCODE 7xm offers a user memory of 1-kbit or 2-kbit, whereas UCODE 7xm+ supports 2-kbit user memory and a 384-bit digital signature.

All products incorporate features known from UCODE 7 like pre-serialization, tag power indicator as well as the product status flag.

There are numbers of applications where the combination of high read range and user memory is needed, such as:

- Inventory and supply chain management
- Process optimization (e.g in the automotive industry)
- Brand protection/authentication (e.g. expensive wines or branded luxury fashion items)
- Automatic vehicle ID where no cryptography is required
- Asset tracking (e.g. for high value assets)
- Aviation spare part tracking

2 Features and benefits

2.1 Key features

- Read sensitivity -19 dBm
- Write sensitivity -12 dBm
- Encoding speed: 32 bits per 1.5 milliseconds
- Up to 2-kbit user memory
- Digital signature
- Standard functionality
  - Untraceable feature
  - Tag Power Indicator
  - Pre-serialization for 96-bit EPC
  - Integrated Product Status Flag (PSF)
  - Parallel encoding mode
- According to EPCglobal v1.2.0
- ATA Spec 2000 low memory tag compliant
- Compatible with single-slit antenna

2.1.1 Memory

- Up to 448-bit of EPC memory
- Supports Pre-serialization for 96-bit EPC
- 96-bit Tag IDentifier (TID) factory locked
- 48-bit unique serial number factory-encoded into TID
- 1-kbit user memory for UCODE 7xm
- 2-kbit user memory for UCODE 7xm
- 2-kbit user memory for UCODE 7xm+
- 384-bit digital signature in UCODE 7xm+
- 32-bit kill password to permanently disable the tag
- 32-bit access password
- Wide operating temperature range: -40 ° C up to +85 ° C
- Minimum 100.000 write cycle endurance
- Data retention 20 years

2.2 Key benefits

2.2.1 End-user benefit

- Extended user memory of up to 2-kbit
- Brand protection feature using digital signature
- Long read/write ranges due to high chip sensitivity
- Reliable operation in dense reader and noisy environments through high interference rejection

2.2.2 Antenna design benefits

- High sensitivity enables smaller and cost efficient antenna designs

2.2.3 Label/module manufacturer benefit

- Large RF pad-to-pad distance to ease antenna design
- Symmetric RF inputs are less sensitive to process variation
- Single-slit antenna for a more mechanically stable antenna connection
- Pre-serialization of the 96-bit EPC
- Extremely fast encoding of the EPC content

2.3 Supported features

- All mandatory commands of EPCglobal v1.2.0 specification are implemented
- The following optional commands are implemented:
  - Access
  - BlockPermalock (block size of 256-bit)
  - 32-bit BlockWrite
- Implemented custom commands and features:
  - Untraceable
  - ReadSignature
  - Product Status Flag bit: enables the UHF RFID tag to be used as EAS (Electronic Article Surveillance) tag without the need for a back-end database.
  - Tag Power Indicator: enables the reader to select only ICs/tags that have enough power to be written to.
  - Parallel encoding: allows for the ability to bring (multiple) tag(s) quickly to the OPEN state and therefore allowing single tags to be identified simply, without timing restrictions, or multiple tags to be e.g. written to at the same time, considerably reducing the encoding process

UCODE 7xm can be used in combination with readers compliant with EPCglobal v1.2.0 standard. For access to full UCODE 7xm family functionality, firmware upgrade of the reader may be necessary.

3 Applications

3.1 Markets

- Logistics
- Smart Manufacturing
- Process automation
- Airline Industry

3.2 Applications

- Inventory and supply chain management
- Asset tracking
- Process optimization(e.g. in the automotive industry)
- Loss prevention
- Aviation spare part tagging
- Airline baggage tagging

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Name	IC type	Description	Version
SL3S1004FUD/BG1	Wafer	UCODE 7xm	1 kB User memory, Gold bumped die on sawn 8" 120 µm wafer with 7 µm Polyimide spacer	not applicable
SL3S1024FUD/BG1	Wafer	UCODE 7xm	2 kB User memory, Gold bumped die on sawn 8" 120 µm wafer with 7 µm Polyimide spacer	not applicable
SL3S1014FUD/BG1	Wafer	UCODE 7xm+	2 kB User memory, Gold bumped die on sawn 8" 120 µm wafer with 7 µm Polyimide spacer	not applicable

5 Block diagram

The UCODE 7xm/7xm+ consists of three major blocks:

- Analog Interface

- Digital Control

- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader which is then processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital control includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.

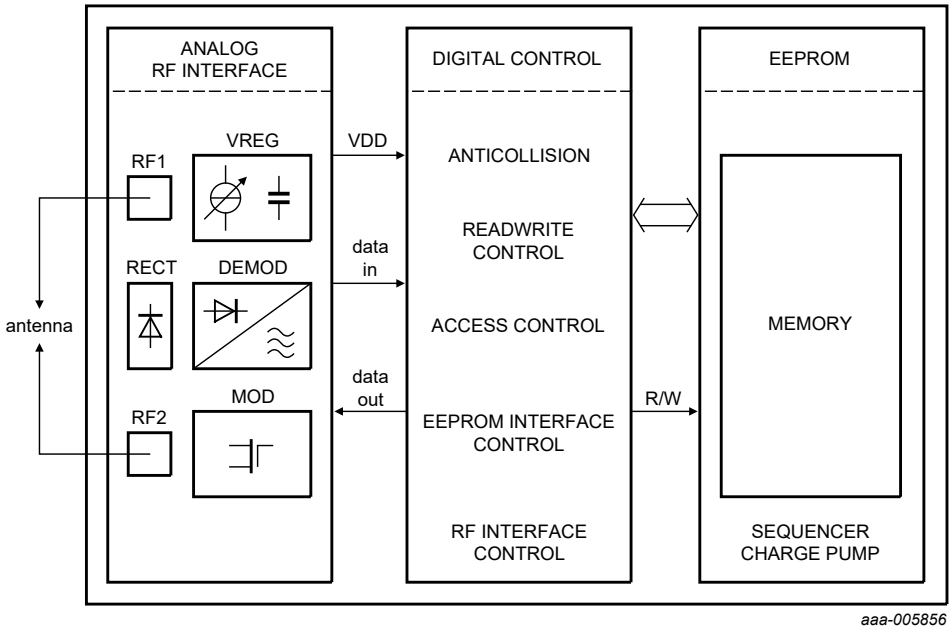


Figure 1. Block diagram of UCODE 7xm/7xm+ ICs

6 Pinning information

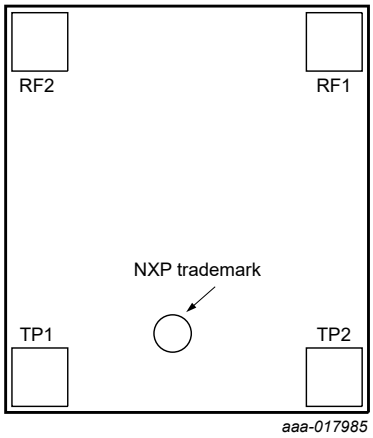


Figure 2. Pinning bare die

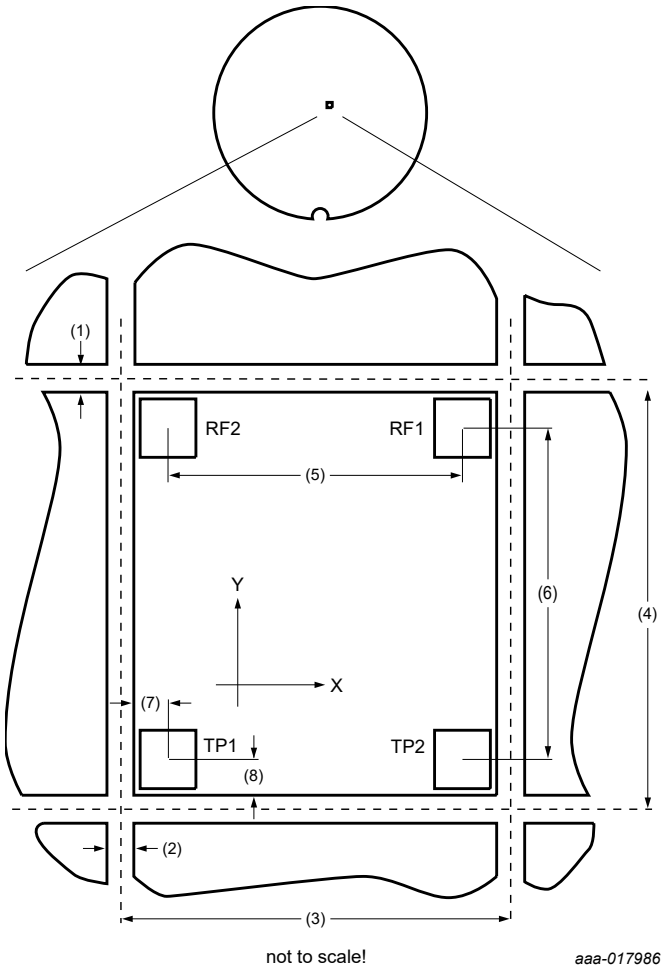
6.1 Pin description

Table 2. Pin description bare die

Symbol	Description
TP1	test pad 1
RF1	antenna connector 1
TP2	test pad 2
RF2	antenna connector 2

7 Wafer layout

7.1 Wafer layout



1. Die to Die distance (metal sealring - metal sealring) 21.4 µm, (X-scribe line width: 15 µm)
2. Die to Die distance (metal sealring - metal sealring) 21.4 µm, (Y-scribe line width: 15 µm)
3. Chip step, x-length: 585µm
4. Chip step, y-length: 645 µm
5. Bump to bump distance X (RF1 - RF2): 480 µm
6. Bump to bump distance Y (TP1 - RF2): 540 µm
7. Distance bump to metal sealring X: 41.8 µm (outer edge - top metal)
8. Distance bump to metal sealring Y: 41.8 µm

Bump size X x Y: 60 µm x 60 µm

Remark: TP1 and TP2 are electrically disconnected after dicing

Figure 3. UCODE 7xm/7xm+ wafer layout

8 Mechanical specification

The UCODE 7xm/7xm+ wafers are available in 120 µm thickness with 7µm Polyimide spacer, resulting in less coupling between the antenna and the active circuit.

8.1 Wafer specification

See Ref: [4].

8.1.1 Wafer

Table 3. Specifications

Wafer	
Designation	each wafer is scribed with batch number and wafer number
Diameter	200 mm (8") unsawn - 205 mm typical sawn on foil
Thickness	120 µm ± 15 µm
Number of pads	4
Pad location	non-diagonal / placed in chip corners
Distance pad to pad RF1-RF2	480.0 µm
Distance pad to pad TP1-RF2	540.0 µm
Process	CMOS 0.14 µm
Batch size	25 wafers
Net dies per wafer	74.535
Wafer backside	
Material	Si
Treatment	ground and stress release
Roughness	R_a max. 0.5 µm, R_t max. 5 µm
Chip dimensions	
Die size excluding scribe	0.570 mm × 0.630 mm = 0.359 mm^2
Scribe line width:	x-dimension = 15 µm
	y-dimension = 15 µm
Passivation on front	
Type	Sandwich structure
Material	PE-Nitride (on top)
Thickness	1.75 µm total thickness of passivation
Polyimide spacer	7 µm ± 1 µm
Au bump	
Bump material	> 99.9 % pure Au
Bump hardness	35 – 80 HV 0.005
Bump shear strength	> 70 MPa

Bump height	25 µm [1]
Bump height uniformity	
within a die	± 2 µm
– within a wafer	± 3 µm
– wafer to wafer	± 4 µm
Bump flatness	± 1.5 µm
Bump size	
– RF1, RF2	60 × 60 µm
– TP1, TP2	60 × 60 µm
Bump size variation	± 5 µm

[1] Because of the 7 µm spacer, the bump will measure 18 µm relative height protruding the spacer.

8.1.2 Fail die identification

No ink dots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See Ref: [4]

8.1.3 Map file distribution

See Ref: [4]

9 Functional description

9.1 Air interface standards

The UCODE 7xm/7xm+ fully supports all mandatory parts of the EPCglobal v1.2.0 specification.

9.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE 7xm/7xm+ IC. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the UCODE 7xm/7xm+ on the tag.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a rectified DC voltage to the analog and digital modules of the IC.

The antenna attached to the chip may use a DC connection between the two antenna pads. Therefore the UCODE 7xm/7xm+ also enables loop antenna design.

9.3 Data transfer

9.3.1 Interrogator to tag Link

An interrogator transmits information to the UCODE 7xm/7xm+ by modulating a UHF RF signal. The UCODE 7xm/7xm+ receives both information and operating energy from this RF signal. Tags are passive, meaning that they have no battery and receive all of their operating energy from the interrogator's RF waveform.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the UCODE 7xm/7xm+ by modulating an RF carrier.

For further details, see Ref: [1].

9.3.2 Tag to interrogator Link

Upon transmitting a valid command, an interrogator receives information from a UCODE 7xm/7xm+ tag by transmitting an unmodulated RF carrier and listening for a backscattered reply. The UCODE 7xm/7xm+ backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details, see Ref: [1].

9.4 UCODE 7xm and UCODE 7xm+ Overview

This table should provide a quick overview on the features implemented in UCODE 7xm and UCODE 7xm+. Details on the features are described in the following paragraphs.

Table 4. Overview of UCODE 7xm and UCODE 7xm+

Features	UCODE 7xm-1k	UCODE 7xm-2k	UCODE 7xm+
User Memory	1024 bit	2048 bit	2048 bit
EPC Memory	max 448 bit	max 448 bit	max 448 bit

Features	UCODE 7xm-1k	UCODE 7xm-2k	UCODE 7xm+
TID Memory	96 bit	96 bit	96 bit
Access Password	32 bit	32 bit	32 bit
Kill Password	32 bit	32 bit	32 bit
PSF (Product Status Flag)	yes	yes	yes
BlockWrite (32 bit)	yes	yes	yes
BlockPermalock (256-bit block size)	yes	yes	yes
Pre-Serialization of 96-bit EPC	yes	yes	yes
Parallel Encoding	yes	yes	yes
Backscatter strength reduction	yes	yes	yes
Tag Power Indicator	yes	yes	yes
Untraceable feature	yes	yes	yes
Digital Signature (384-bit)	-	-	yes

9.5 Supported commands

The UCODE 7xm/7xm+ support all **mandatory** EPCglobal v1.2.0 commands.

In addition the following **optional** commands are supported:

- Access
- BlockPermalock (256-bit block size)
- BlockWrite (max 32 bit on even addresses only)

UCODE 7xm/7xm+ also offers the following **custom** commands:

- Untraceable
- ReadSignature (UCODE 7xm+ only)

9.5.1 Custom commands

9.5.1.1 Untraceable

The Untraceable function allows the UCODE 7xm/7xm+ to hide the complete or parts of the EPC, TID and/or user memory. In addition, the read range can be completely or temporarily reduced.

This command can only be executed from the secured state.

Memory parts which are set untraceable are acting as non-existing.

EPC-field:

Specifies the number of words of the EPC memory which the UCODE 7xm/xm+ back scatters. A change of this field therefore also changes the L bit in the Protocol Control (PC) word.

TID-field:

Hide some ("01") will hide the TID memory from address 20h (included) onwards.

Range-field:

In case of activated range toggling, the read range reduction toggles from the actual value to the second. (e.g. when actual state is normal it toggles to reduced). In case of power loss, the chip reverts to its prior state. At activation of this feature the chip checks if sufficient power would be available, in case range reduction would be active, to communicate with the tag. Only in case this condition is ensured the feature will be activated.

UCODE 7xm/7xm+ does not support the U bit and therefore ignores this value.

Table 5. Untraceable command

	Command	RFU	U	EPC	TID	User	Range	RN	CRC
No. of bits	16	2	1	6	2	1	2	16	16
Description	1110 0010 0000 0000	00	do not care	MSB: "0": show memory above EPC "1": hide memory above EPC 5 LSBs: New EPC length	"00": hide none "01": hide some "10": hide all "11": RFU	"0": view "1": hide	"00": normal "01": toggle "10": reduced "11": RFU	handle	CRC-16

Table 6. Untraceable command-response table

Starting State	Condition	Response	Next State
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	all	-	open
secured	executable	backscatter header when done	secured
killed	all	-	killed

In case of access to the tag, the error condition "memory overrun" will be returned.

9.5.1.2 ReadSignature (UCODE 7xm+ only)

The ReadSignature command allows the read out of the pre-programmed Digital Signature and includes a CRC-16 calculated over the whole command, the handle and the frame-sync.

Table 7. ReadSignature command

	Command	WordPtr	WordCount	RN	CRC
No. of bits	16	EVB	8	16	16
Description	1110 0000 0000 1000	Starting Address Pointer	Number of words to read	Handle	CRC-16

Table 8. Tag reply to a successful ReadSignature command

	Header	Signature Words	RN	CRC
No. of bits	1	Variable	16	16
Description	0	Digital Signature	Handle	CRC-16

The error Response "memory overrun" is returned in case WordCount=0 or in case WordPtr or the combination of WordPtr and WordCount exceeds the range of the Digital Signature.

Table 9. ReadSignature command-response table

Starting State	Condition	Response	Next State
ready	all	-	ready
arbitrate, reply, acknowledged	all	-	arbitrate
open	all	backscatter data	open
secured	all	backscatter data	secured
killed	all	-	killed

Digital Signature

The UCODE 7xm+ is delivered with a factory pre-programmed 384-bit Digital Signature based on the Elliptic Curve Digital Signature Algorithm (ECDSA) using a 192-bit cryptographic key. The parameters of the curve are according to NIST P-192 (secp 192r1). The data digital signed is the 96-bit TID of the UCODE 7xm+.

Verification of the digital signature:

After issuing the ReadSignature command, the tag will return the 384-bit digital signature.

With the knowledge of the Public Key and the algorithm a verification that the silicon is an origin NXP Semiconductor can be made.

UCODE 7xm+ Public Key:

04A72DB4B83233DD9A9711DB071281F14451747F815EEB111F1D4CD3DCAD602
50C830CD287DCEC0B39C76262BA998B7E01

MS VC++ Code Example

```
/**
* Check Originality Signature on curve NID_X9_62_prime192v1
**/
unsigned char CheckOriginalitySignature192UCode7xmBinary(unsigned char * aUid,
unsigned char * aSignature)
{
/* secp192v1 => ECC_Length=24; */
unsigned int ECC_Length = 24;
unsigned int bLength = 12;
char* publickey_str =
"04A72DB4B83233DD9A9711DB071281F14451747F815EEB111F1D4
```

```
CD 3DCAD60250 C830CD287DCEC0B39C76262BA998B7E01"; /* UCODE7xm */
BIGNUM *pk_bignum = BN_new();
EC_POINT *public_key = NULL;
/* Create a EC_KEY for specified curve */
EC_KEY *pubKey = EC_KEY_new_by_curve_name(NID_X9_62_prime192v1); const
EC_GROUP *ecgroup = EC_KEY_get0_group(pubKey);
ECDSA_SIG *signature = ECDSA_SIG_new();
unsigned char r[24]; /* ECC_Length */
unsigned char s[24]; /* ECC_Length */
char r_dest[24*2+1]; /* ECC_Length *2 +1 */
char s_dest[24*2+1]; /* ECC_Length *2 +1 */
unsigned int loop = 0;
if (signature == NULL )
{
return 1;
}
if (pubKey == NULL)
{
printf("Creation of PubKey failed \\n");
return 1;
}
/* Convert the hex public key x,y coordinates to BIGNUM */
BN_hex2bn(&pk_bignum, publickey_str);
public_key = EC_POINT_bn2point(ecgroup, pk_bignum, NULL, NULL);
/* Set the public key point to EC_KEY */
EC_KEY_set_public_key(pubKey, public_key);
/* Extract the r and s part of the signature*/
memcpy(r, aSignature, ECC_Length);
memcpy(s, aSignature+ECC_Length, ECC_Length);
/* BIGNUM conversion function expects r in ASCII value */
for(loop = 0;loop < ECC_Length; loop++)
{
sprintf_s((r_dest+(loop*2)), 3, "%02X", r[loop]);
sprintf_s((s_dest+(loop*2)), 3, "%02X", s[loop]);
}
BN_hex2bn(&signature->r, r_dest);
```

```
BN_hex2bn(&signature->s, s_dest);
/*Signature verification for the UID sent*/
if (ECDSA_do_verify(aUid, bLength, signature, pubKey) == 1)
{
printf("\\nSignature verified successfully\\n\\n");
return 0;
}
else
{
printf("\\nSignature verification failed\\n\\n");
return 1;
}
}
```

9.6 UCODE 7xm/7xm+ memory

The UCODE 7xm/7xm+ memory is implemented according to EPCglobal v1.2.0 and organized in four banks:

Table 10. UCODE 7xm-1k memory sections

Name	Size	Bank
Reserved memory (32-bit ACCESS and 32-bit KILL password)	64 bit	00b
EPC (excluding CRC, PC)	448 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b
User Memory	1024bit	11b

Table 11. UCODE 7xm-2k memory sections

Name	Size	Bank
Reserved memory (32-bit ACCESS and 32-bit KILL password)	64 bit	00b
EPC (excluding CRC, PC)	448 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b
User Memory	2048bit	11b

Table 12. UCODE 7xm+ memory sections

Name	Size	Bank
Reserved memory (32-bit ACCESS and 32-bit KILL password)	64 bit	00b
EPC (excluding CRC, PC)	448 bit	01b
TID (including permalocked unique 48-bit serial number)	96 bit	10b
User Memory	2048bit	11b

The logical address of all memory banks begins at zero (00h).

In addition to the four memory banks a **configuration word** to handle the UCODE 7xm/7xm+ specific features is available at address 200h in the EPC memory. The configuration word is described in detail in Section 9.7.1.

The TID complies to the extended tag Identification scheme according to GS1 EPC Tag Data Standard 1.9. (Ref: [2])

9.6.1 UCODE 7xm/7xm+ overall memory map

Table 13. UCODE 7xm/7xm+ overall memory map

Bank address	Memory address	Type	Content	Initial	Remark
Bank 00	00h to 1Fh	reserved	kill password	all 00h	unlocked memory
	20h to 3Fh	reserved	access password	all 00h	unlocked memory
Bank 01 EPC	00h to 0Fh	EPC	CRC-16		memory mapped calculated CRC
	10h to 14h	EPC	EPC length	00110b	unlocked memory
	15h	EPC	UMI	0b	unlocked memory
	16h	EPC	XPC indicator	0b	hardwired to 0
	17h to 1Fh	EPC	numbering system indicator	00h	unlocked memory
	20h to 1DFh	EPC	EPC	[1]	unlocked memory
Bank 01 ConfigWord	200h	EPC	RFU	0b	locked memory
	201h	EPC	RFU	0b	locked memory
	202h	EPC	Parallel encoding	0b	Action bit [2]
	203h	EPC	RFU	0b	locked memory
	204h	EPC	Tag Power Indicator	0b	Action bit [2]
	205h	EPC	RFU	0b	locked memory
	206h	EPC	RFU	0b	locked memory
	207h	EPC	RFU	0b	locked memory
	208h	EPC	RFU	0b	locked memory
	209h	EPC	max. backscatter strength	1b	permanent bit [3]
	20Ah	EPC	RFU	0b	locked memory
	20Bh	EPC	RFU	0b	locked memory
	20Ch	EPC	RFU	0b	locked memory
	20Dh	EPC	RFU	0b	locked memory
	20Eh	EPC	RFU	0b	locked memory
	20Fh	EPC	PSF alarm flag	0b	Permanent bit [3]
Bank 10 TID	00h to 07h	TID	allocation class identifier	1110 0010b	locked memory
	08h to 13h	TID	tag mask designer identifier	806h	locked memory
	14h	TID	config word indicator	1b [4]	locked memory
	14h to 1Fh	TID	tag model number	TMNR [5]	locked memory
	20h to 2Fh	TID	XTID header	2000h	locked memory
	30h to 5Fh	TID	serial number	SNR	locked memory
Bank 11 USER	000h to 3FFh	USER	User Memory	undefined	unlocked memory UCODE 7xm and 7xm+
	400h to 7FFh	USER	User Memory	undefined	unlocked memory UCODE 7xm+ only

[1] HEX E280 6mmm 0000 nnnn nnnn nnnn
where mmm represents the according to tag model number and n the nibbles of the 48-bit SNR of the TID
[2] Action bits: meant to trigger a feature upon a SELECT command on the related bit ref feature control mechanism, seeSection 9.7.1
[3] Permanent bit: permanently stored bits in the memory; Read/Writeable according to EPC bank lock status, see Section 9.7.1
[4] Indicates the existence of a Configuration Word at the end of the EPC number
[5] See Figure 4

9.6.2 UCODE 7xm/7xm+ TID memory details

	First 48 bit of TID memory	Class ID	Mask Designer ID	Model Number			XTID Header
				Config Word Indicator	Sub Version Nr.	Version (Silicon) Nr.	
UCODE 7xm-1k	E2806D12	E2h	806h	1b	1010b	0010010b	2000h
UCODE 7xm-2k	E2806F12	E2h	806h	1b	1110b	0010010b	2000h
UCODE 7xm+	E2806D92	E2h	806h	1b	1011b	0010010b	2000h

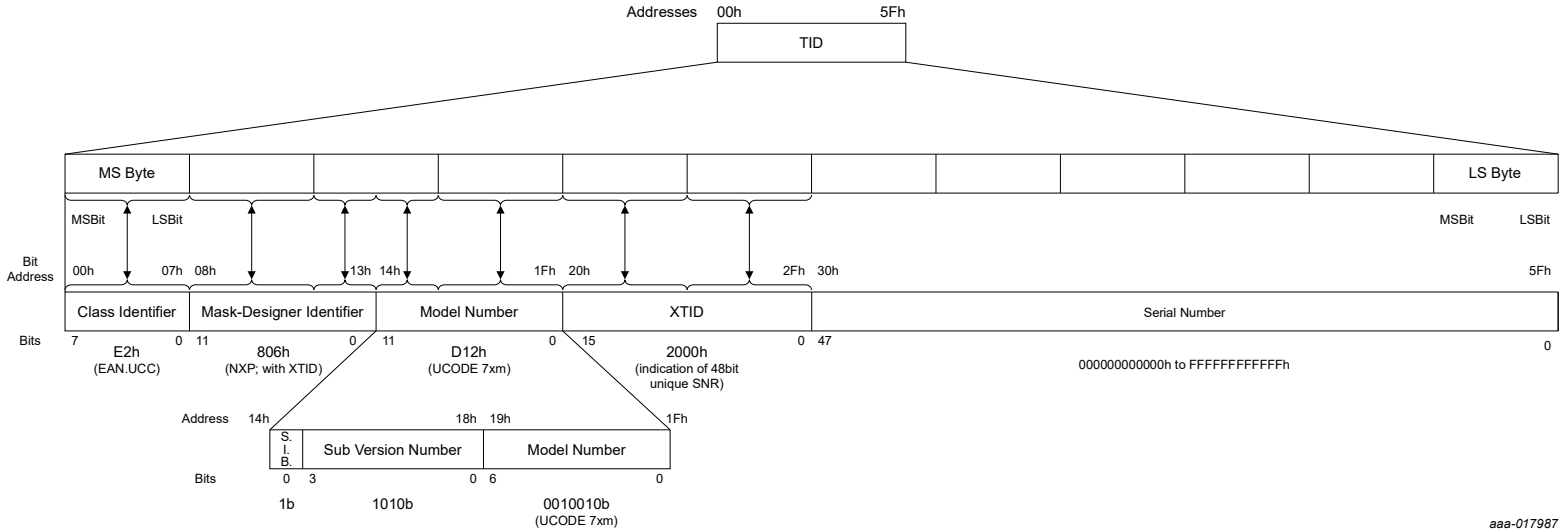


Figure 4. UCODE 7xm/7xm+ TID memory structure

9.7 Supported features

The UCODE 7xm/7xm+ is equipped with features of previous UCODE generation. These features include:

- Pre-serialization of the 96-bit EPC
- Parallel encoding
- Tag Power Indicator
- Backscatter strength reduction
- Product Status Flag (PSF)
- Single-slit antenna solution

These features are implemented in such a way that standard EPCglobal v1.2.0 READ / WRITE / ACCESS / SELECT commands can be used to operate these features.

The Configuration Word, as mentioned in the memory map, describes the additional features located at address 200h of the EPC memory.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag enables the selection of configuration word enhanced transponders in mixed tag populations.

9.7.1 UCODE 7xm/7xm+ features control mechanism

The different features of the UCODE 7xm/7xm+ can be activated / de-activated by addressing or changing the content of the corresponding bit in the configuration word located at address 200h in the EPC memory bank (see Table 14). The de-activation of the action bit features will only happen after chip reset.

Table 14. Configuration word UCODE 7xm/7xm+

Locked memory		Action bit	Locked memory	Action bit	Locked memory		
RFU	RFU	Parallel encoding	RFU	Tag Power Indicator	RFU	RFU	RFU
0	1	2	3	4	5	6	7

Table 15. Configuration word UCODE 7xm/7xm+

Locked memory	Permanent bit	Locked memory					Permanent bit
RFU	max. backscatter strength	RFU	RFU	RFU	RFU	RFU	PSF Alarm bit
8	9	10	11	12	13	14	15

The configuration word contains 2 different type of bits:

- **Action bits**: meant to trigger a feature upon a SELECT command on the related bit:
  Parallel encoding
  Tag Power indicator
- **Permanent bits**: permanently stored bits in the memory
  Max. Backscatter Strength
  PSF Alarm bit

The activation or the de-activation of the feature behind the permanent bits happens only when attempting to write a "1" value to the related bit (value toggling) - writing "0" value will have no effect.

If the feature is activated, the related bit will be read with a "1" value and, if de-activated, with a "0" value.

The permanent bits can only be toggled by using standard EPC WRITE (not a BlockWrite) if the EPC bank is unlocked or within the SECURED state if the EPC is locked. If the EPC is permalocked, they cannot be changed.

Action bits will trigger a certain action only if the pointer of the SELECT command exactly matches the action-bit address (i.e. 202h or 204h), if the length=1 and if mask=1b

(no multiple trigger of actions possible within one single SELECT command).

After issuing a SELECT to any action bits, an interrogator shall transmit CW for RTCal see Ref: [3] + 80 µs before sending the next command.

If the truncate bit in the SELECT command is set to "1" the SELECT will be ignored.

A SELECT on action bits will not change the digital state of the chip.

The action bits can be triggered regardless if the EPC memory is unlocked, locked or permalocked.

9.7.2 Backscatter strength reduction

The UCODE 7xm/7xm+ features two levels of backscatter strengths. Per default, maximum backscatter is enabled in order to enable maximum read rates. When clearing the flag, the strength can be reduced if needed.

9.7.3 Pre-serialization of the 96-bit EPC

Description

The 96-bit EPC, which is the initial EPC length settings of UCODE 7xm/7xm+, will be delivered pre-serialized with the 48-bit serial number from the TID.

The EPC content is identically to the 96-bit TID content except of the 16-bit XTID which is set to "0".

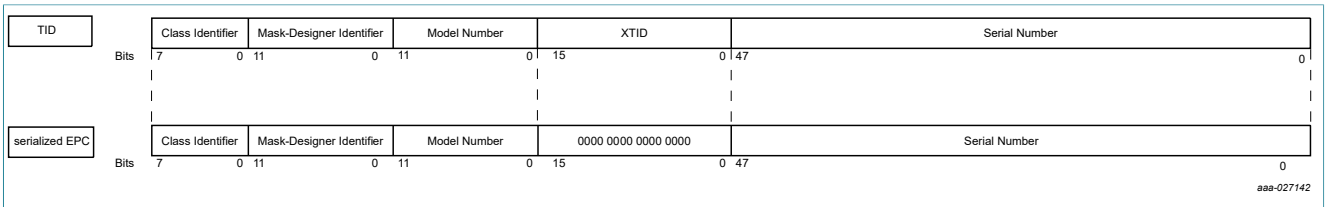


Figure 5. 96-bit Pre serialization

9.7.4 Parallel encoding

Description

This feature of the UCODE 7xm/7xm+ can be activated by the "Parallel encoding bit" in the Configuration-Word located at (202h).

Upon issuing an EPC SELECT command on the "Parallel encoding bit", in a population of UCODE 7xm/7xm+ tags, a subsequent QUERY brings all tags go the OPEN state with a specific handle ("AAAAh").

Once in the OPEN state, for example a WRITE command applies to all tags in the OPEN state (see Figure 7). This parallel encoding is considerably lowering the encoding time compared to a standard implementation (see Figure 6).

The number of tags that can be encoded at the same time depends on the strength of the reader signal. Since all tags backscatter their ACKNOWLEDGE (ACK) response at the same time, the reader observes collision in the signal from the tags.

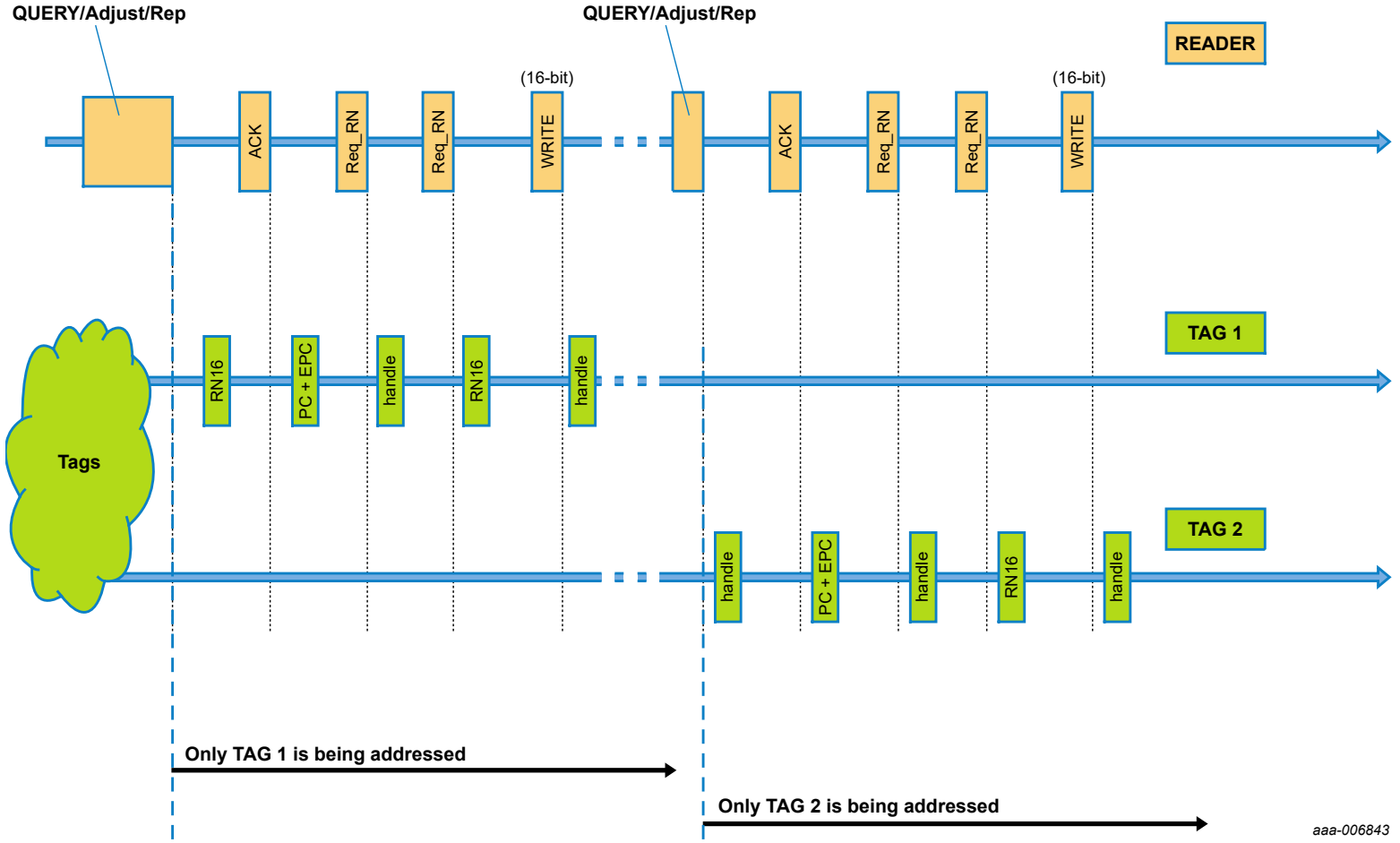


Figure 6. Example of 16-bit Write command with standard EPC Gen 2 commands

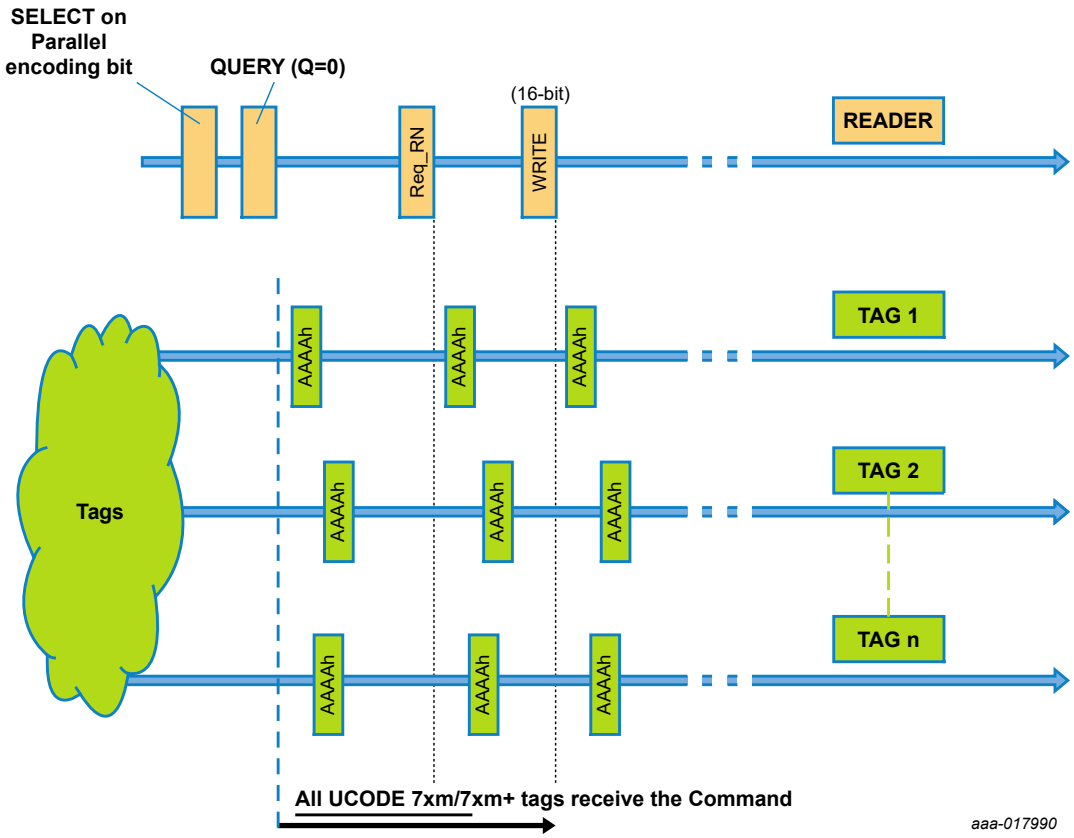


Figure 7. Illustration of Parallel encoding for 16-bit Write command

Use cases and benefits

Parallel encoding feature of UCODE 7xm/7xm+ can enable ultra fast bulk encoding.

Taking in addition advantage of the pre-serialization scheme of UCODE 7xm/7xm+, the same SKU can be encoded in multiple tags as the EPC will be delivered pre-serialized already.

In the case of only one tag answering (like in printer encoding), this feature could be used to save some overhead in commands to do direct EPC encoding after the handle reply.

Since this is a custom-specific feature of UCODE 7xm/7xm+ (taken over from our previous UHF tag IC UCODE 7/7m) the use of this feature requires the same support on the reader side as for previous UCODE products.

9.7.5 Tag Power Indicator

Description

Upon a SELECT command on the "Tag Power Indicator", located in the config word 204h, an internal power check on the chip is performed to see if the power level is sufficient to perform a WRITE command. The decision level is defined as nominal WRITE sensitivity minus 1 dB. In the case there is enough power, the SELECT command is matching and non-matching if not enough power. The tag can then be singulated by the standard inventory procedure.

Use cases and benefits

This feature gives the possibility to select only the tag(s) that receive enough power to be written during e.g. printer encoding in a dense environment of tags even though the reader may read more than one tag (see Figure 8 for illustration). The power level still needs to be adjusted to transmit enough writing power to one tag only to do one tag singulation.

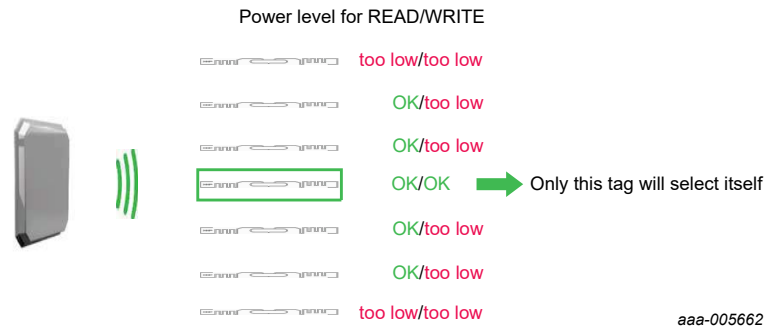


Figure 8. Selection of tags with Tag Power Indicator feature

9.7.6 Product Status Flag (PSF)

Description

The PSF is a general-purpose bit located in the Configuration word at address 20Fh with a value that can be freely changed.

Use cases and benefits

The PSF bit can be used as an EAS (Electronic Article Surveillance) flag, quality checked flag or similar.

In order to detect the tag with the PSF activated, an EPC SELECT command selecting the PSF flag of the Configuration word can be used. In the following inventory round, only PSF enabled chips will reply their EPC number.

9.7.7 Single-slit antenna solution

Description

In UCODE 7xm/7xm+, the test pads TP1 and TP2 are electrically disconnected meaning they are not electrically active and can be safely short-circuited to the RF pads RF1 and RF2 (see Figure 9).

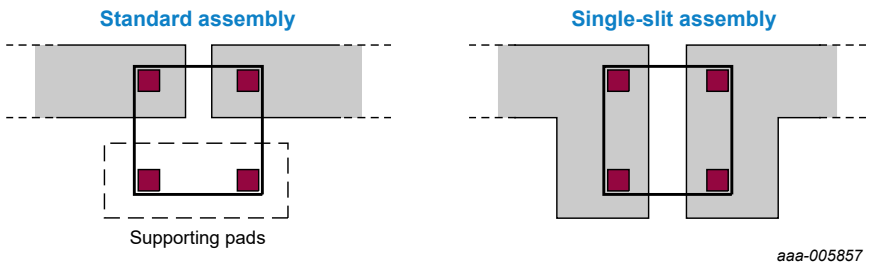


Figure 9. Standard antenna design versus single-slit antenna

Uses cases and benefits

Using single-slit antenna enables easier assembly and antenna design. Inlay manufacturer will only have to take care about one slit of the antenna instead of two in case all pads need to be disconnected from each other.

Additionally single-slit antenna assembly and the related increased input capacitance (see Table 17) can be used advantageously over the standard antenna design as additional room for optimization to different antenna design.

10 Limiting values

Table 16. Limiting values [1] [2]

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to RFN

Symbol	Parameter	Conditions		Min	Max	Unit
Bare die limitations						
T_{stg}	storage temperature			-55	+125	° C
T_{amb}	ambient temperature			-40	+85	° C
V_{ESD}	electrostatic discharge voltage	human body model (HBM) [3]	[4]	-	± 2	kV
Pad limitations						
P_i	input power	maximum power dissipation, RFP pad		-	100	mW

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.
[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
[3] According to ANSI/ESDA/JEDEC JS-001
[4] For ESD measurement, the die chip has been mounted into a CDIP20 package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

11 Characteristics

11.1 UCODE 7xm/7xm+ bare die characteristics

Table 17. UCODE 7xm/7xm+ RF interface characteristics (RF1, RF2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_i	input frequency			840	-	960	MHz
$P_{i(min)}$	minimum input power	READ sensitivity	[1] [2] [3]	-	-18.5	-	dBm
		WRITE sensitivity	[4]	-	-12	-	dBm
		Reduced operating range	[4]	-	+7	-	dBm
t	encoding speed (16-bit or 32-bit)	16-bit	[5]	-	1.5	-	ms
C_i	input capacitance	parallel	[2] [6]	-	0.63	-	pF
Z	impedance	866 MHz	[2] [6]	-	19-j284	-	Ω
		915 MHz	[2] [6]	-	17-j274	-	Ω
		953 MHz	[2] [6]	-	17-j265	-	Ω
Z	typical assembled impedance [7]	915 MHz	[8]	-	26-j235		Ω
Z	typical assembled impedance [7] in case of single-slit antenna assembly	915 MHz	[8] [9]	-	16-j181	-	Ω
Tag Power Indicator mode							
$P_{i(min)}$	minimum input power		[10]	-	-11	-	dBm

[1] Power to process a QUERY command
[2] Measured with a 50 Ω source impedance directly on the chip
[3] Results in approximately -19dBm tag sensitivity with a 2dBi gain antenna
[4] Tag sensitivity on a 2dBi gain antenna
[5] When the memory content is "0000...".
[6] At minimum operating power
[7] Assuming a 80fF additional input capacitance, 250fF in case of single slit antenna
[8] The antenna shall be matched to this impedance
[9] Depending on the specific assembly process, sensitivity losses of few tenths of dB might occur
[10] Tag sensitivity on a 2dBi gain antenna. Power level to select the tag

Table 18. UCODE 7xm/7xm+ memory characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
EEPROM characteristics							
t_{ret}	retention time	$T_{amb} \leq 55$ ° C		20	-	-	year
$N_{endu(W)}$	write endurance			100k	-	-	cycle

12 Package outline

This section is not applicable for this kind of device.

13 Packing information

13.1 Wafer

See Ref: [4]

14 Abbreviations

Table 19. Abbreviations

Acronym	Description
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DSB-ASK	Double Side Band-Amplitude Shift Keying
DC	Direct Current
EAS	Electronic Article Surveillance
EEPROM	Electrically Erasable Programmable Read Only Memory
EPC	Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number)
FM0	Bi phase space modulation
G2	Generation 2
IC	Integrated Circuit
PIE	Pulse Interval Encoding
PSF	Product Status Flag
RF	Radio Frequency
UHF	Ultra High Frequency
SECS	Semi Equipment Communication Standard
TID	Tag IDentifier

15 References

[1] GS1 EPCglobal: EPC™ Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (23 October 2008)

[2] EPCglobal: EPC Tag Data Standard Version 1.9, ratified Nov-2014

[3] RTCal is the Interrogator-to-Tag calibration symbol length defined in the EPCglobal specification

[4] Data sheet - Delivery type description – General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093** [1]

1 ** ... document version number

16 Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SL3S10x4 v.3.4	20200616	Product data sheet	-	SL3S10x4 v.3.3
Modifications:	• Section 3 "Applications": updated • Section 9.7.3 "Pre-serialization of the 96-bit EPC": updated			
SL3S10x4 v.3.3	20161130	Product data sheet	-	SL3S1004_1014 v.3.2
Modifications:	• Added UCODE 7xm-2k version (SL3S1024FUD)			
SL3S1004_1014 v.3.2	20160727	Product data sheet	-	SL3S1004_1014 v.3.1
Modifications:	• Update Automatic Pre-serialization functionality			
SL3S1004_1014 v.3.1	20150727	Product data sheet	-	SL3S1004_1014 v.3.0
Modifications:	• Update UCODE 7xm+ Public Key			
SL3S1004_1014 v.3.0	20150615	Product data sheet	-	SL3S1004_1014 v.1.0
Modifications:	• Update Write sensitivity • Digital Signature explanation and source code added • Update of final feature set • Editorial changes			
SL3S1004_1014 v.1.0	20150416	Objective data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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