



# PIC18(L)F2X/4X/5XK42

## Highly Integrated 8-Bit PIC<sup>®</sup> Microcontrollers in 28- to 48- Pins

### Description

The PIC18(L)F2X/4X/5XK42 microcontroller family is available in 28/40/44/48-pin devices. This family features a 12-bit ADC with Computation (ADC<sup>2</sup>) automating Capacitive Voltage Divider (CVD) techniques for advanced touch sensing, averaging, filtering, oversampling and threshold comparison. Additionally, Vectored Interrupt Controller with fixed latency for handling interrupts, System Bus Arbiter, Direct Memory Access capabilities, UART with support for Asynchronous, DMX, DALI and LIN protocols, SPI, I<sup>2</sup>C, memory features like Memory Access Partition (MAP) to support customers in data protection and bootloader applications, Device Information Area (DIA) which stores factory calibration values to help improve temperature sensor accuracy.

### Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - Up to 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Two Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User programmable source and destination sizes
  - Hardware and software triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed Interrupt latency
  - Programmable vector table base address
- 31-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-Out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware or software
- Programmable Code Protection:
  - Configurable Boot and App region sizes

### Memory

- Up to 128 KB Flash Program Memory
- Up to 8 KB Data SRAM Memory
- Up to 1 KB Data EEPROM
- Memory Access Partition (MAP):
  - Bootloader write-protect
  - Configurable partition
- Device Information Area (DIA) Stores:
  - Temp sensor factory calibrated data
  - Fixed Voltage Reference
  - Device ID

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC18LF2X/4X/5XK42)
  - 2.3V to 5.5V (PIC18F2X/4X/5XK42)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### Power-Saving Functionality

- DOZE mode: Ability to run CPU core slower than the system clock
- IDLE mode: Ability to halt CPU core while internal peripherals continue operating
- Sleep mode: Lowest power consumption
- Peripheral Module Disable (PMD):
  - Ability to disable peripherals to minimize power consumption

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Digital Peripherals

- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Four 16-Bit Timers (TMR0/1/3/5)
- Four Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complementary Waveform Generators (CWGs):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Four 16-Bit Capture/Compare/16-Bit PWM (CCP) modules
- Four 10-bit Pulse Width Modulators (PWMs)

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## Digital Peripherals (Continued)

- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock:  $0\text{ Hz} < f_{\text{NCO}} < 64\text{ MHz}$
  - Resolution:  $f_{\text{NCO}}/220$
- DSM: Data Signal Modulator:
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for fail-safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash
- Two UART Modules:
  - Asynchronous UART, RS-232, RS-485 compatible.
  - One of the UART modules supports LIN master and slave, DMX mode, DALI gear and device protocols
  - Automatic and user timed BREAK period generation
  - DMA compatible
  - Automatic checksums
  - Programmable 1, 1.5, and 2 Stop bits
  - Wake-up on BREAK reception
- One SPI module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Receive-without-transmit option
  - Transmit-without-receive option
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- Two I<sup>2</sup>C modules, SMBus, PMBus™ compatible:
  - Dedicated address, transmit and receive buffers
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I<sup>2</sup>C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Multi-Master mode, including self-addressing
- Device I/O Port Features:
  - 25 I/O pins (PIC18(L)F24/25/26/27K42)
  - 36 I/O pins (PIC18(L)F45/46/47K42)
  - 44 I/O pins (PIC18(L)F55/56/57K42)
  - One input-only pin
  - Individually programmable I/O direction, controlled current, open-drain, slew rate, weak pull-up control
  - Interrupt-on-change
  - Three external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler

## Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC<sup>2</sup>):
  - 12-bit with up to 43 external channels
  - Automated post-processing
  - Automates math functions on input signals: averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Temperature Sensor
    - Internal connection to ADC
    - Can be calibrated for improved accuracy
  - Hardware Capacitive Voltage Divider (CVD):
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
    - Adjustable sample and hold capacitor array
    - Two guard ring output drives
- Two Comparators:
  - Comparator Hysteresis enable
  - Invert output polarity
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Connection to ADC, Comp and DAC

## Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 64 MHz
  - Safe clock switching while running
  - $\pm 1\%$  at calibration (nominal)
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator
- External Oscillator Block with:
  - x4 PLL with external sources
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripherals clock stops
- Oscillator Start-up Timer (OST)
  - Ensures stability of crystal oscillator sources

TABLE 1: PIC18(L)F2X/4X/5XK42 FAMILY TYPES

| Device                         | Data Sheet Index | Program Flash Memory (KB) | Data EEPROM (B) | Data SRAM (bytes) | I/O Pins | 12-bit ADC <sup>2</sup><br>(ch) | 5-bit DAC | Comparator | 8-bit/16-bit Timer | Window Watchdog Timer<br>(WWDT) | Signal Measurement Timer<br>(SMT) | CCP/10-bit PWM | CWG | NCO | CLC | Zero-Cross Detect | Direct Memory Access (DMA)<br>(channels) | Memory Access Partition | Vectored Interrupts | UART/UART with LIN, DMX,<br>DALI Protocol Support | I <sup>2</sup> C/SPI | Peripheral Pin Select | Peripheral Module Disable | Debug <sup>(1)</sup> |
|--------------------------------|------------------|---------------------------|-----------------|-------------------|----------|---------------------------------|-----------|------------|--------------------|---------------------------------|-----------------------------------|----------------|-----|-----|-----|-------------------|------------------------------------------|-------------------------|---------------------|---------------------------------------------------|----------------------|-----------------------|---------------------------|----------------------|
| <a href="#">PIC18(L)F24K42</a> | A                | 16                        | 256             | 1024              | 25       | 24                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F25K42</a> | A                | 32                        | 256             | 2048              | 25       | 24                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F26K42</a> | B                | 64                        | 1024            | 4096              | 25       | 24                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F27K42</a> | C                | 128                       | 1024            | 8192              | 25       | 24                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F45K42</a> | B                | 32                        | 256             | 2048              | 36       | 35                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F46K42</a> | B                | 64                        | 1024            | 4096              | 36       | 35                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F47K42</a> | C                | 128                       | 1024            | 8192              | 36       | 35                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F55K42</a> | B                | 32                        | 1024            | 2048              | 44       | 43                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F56K42</a> | B                | 64                        | 1024            | 4096              | 44       | 43                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |
| <a href="#">PIC18(L)F57K42</a> | C                | 128                       | 1024            | 8192              | 44       | 43                              | 1         | 2          | 3/4                | Y                               | Y                                 | 4/4            | 3   | 1   | 4   | Y                 | 2                                        | Y                       | Y                   | 1/1                                               | 2/1                  | Y                     | Y                         | I                    |

**Note 1:** I – Debugging integrated on chip.

**Data Sheet Index:**

- A:** Future Release [PIC18\(L\)F24/44K42 Data Sheet, 28-Pin](#)  
**B:** Future Release [PIC18\(L\)F26/45/55/46/56K42 Data Sheet, 48-Pin](#)  
**C:** Future Release [PIC18\(L\)F27/47/57K42 Data Sheet, 48-Pin](#)

**Note:** For other small form-factor package availability and marking information, please visit [www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.

# PIC18(L)F2X/4X/5XK42

TABLE 2: PACKAGES

| Device         | (S)PDIP | SOIC | SSOP | UQFN<br>(4x4) | QFN<br>(6x6) | TQFP | QFN<br>(8x8) | UQFN<br>(5x5) | UQFN<br>(6x6) |
|----------------|---------|------|------|---------------|--------------|------|--------------|---------------|---------------|
| PIC18(L)F24K42 | X       | X    | X    | X             | X            | —    | —            | —             | —             |
| PIC18(L)F25K42 | X       | X    | X    | X             | X            | —    | —            | —             | —             |
| PIC18(L)F26K42 | X       | X    | X    | X             | —            | —    | —            | —             | —             |
| PIC18(L)F27K42 | X       | X    | X    | —             | X            | —    | —            | —             | —             |
| PIC18(L)F45K42 | X       | —    | —    | —             | —            | X    | X            | X             | —             |
| PIC18(L)F46K42 | X       | —    | —    | —             | —            | X    | X            | X             | —             |
| PIC18(L)F47K42 | X       | —    | —    | —             | —            | X    | X            | X             | —             |
| PIC18(L)F55K42 | X       | —    | —    | —             | —            | X    | X            | —             | X             |
| PIC18(L)F56K42 | X       | —    | —    | —             | —            | X    | X            | —             | X             |
| PIC18(L)F57K42 | X       | —    | —    | —             | —            | X    | X            | —             | X             |

**Note:** Pin details are subject to change.

## PIN DIAGRAMS

**FIGURE 1: 28-PIN SPDIP, SOIC, SSOP FOR PIC18(L)F2XK42**

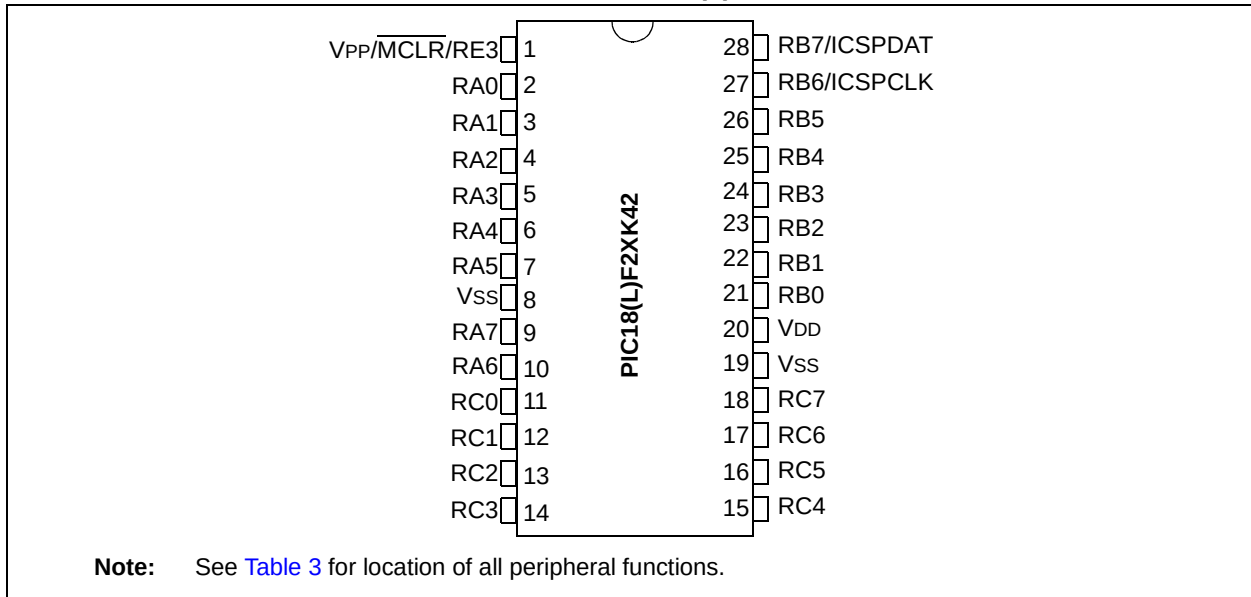
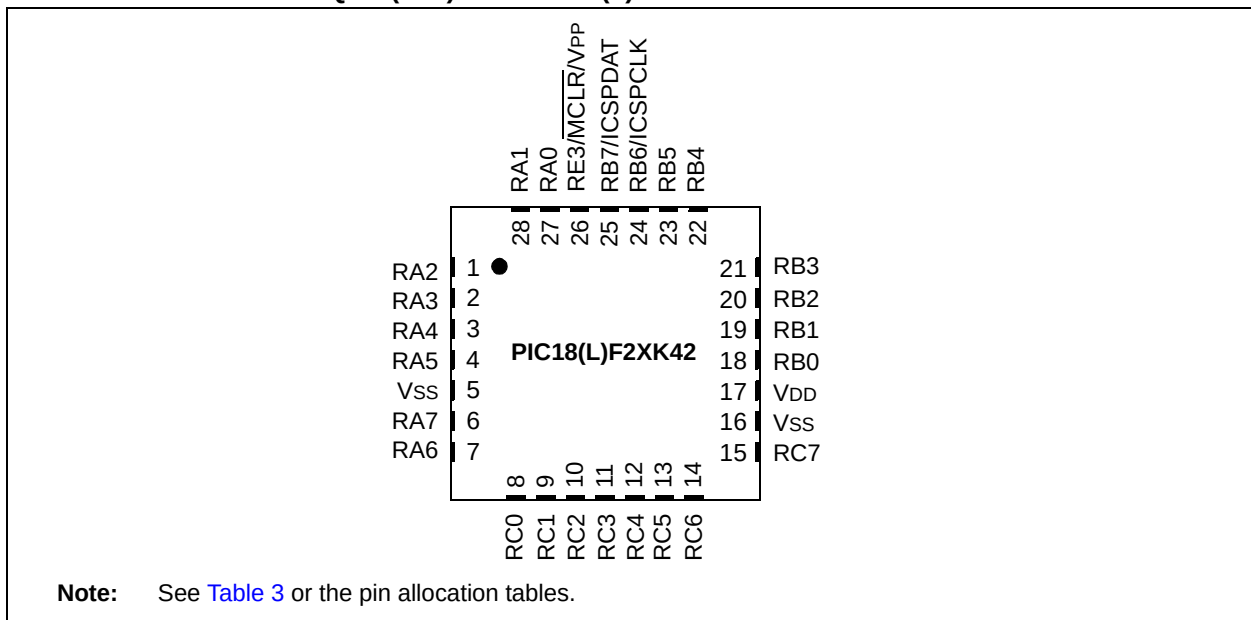


**FIGURE 2: 28-PIN UQFN (4X4) FOR PIC18(L)F2XK42**



# PIC18(L)F2X/4X/5XK42

FIGURE 3: 28-PIN QFN (6X6X0.9 mm) FOR PIC18(L)F2XK42

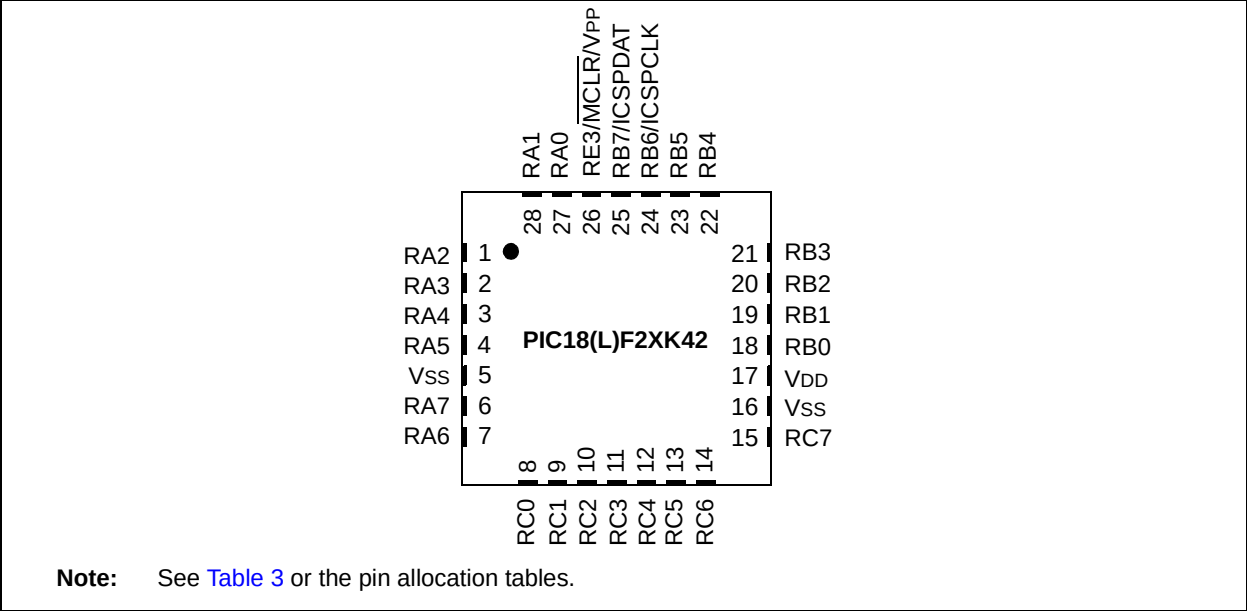
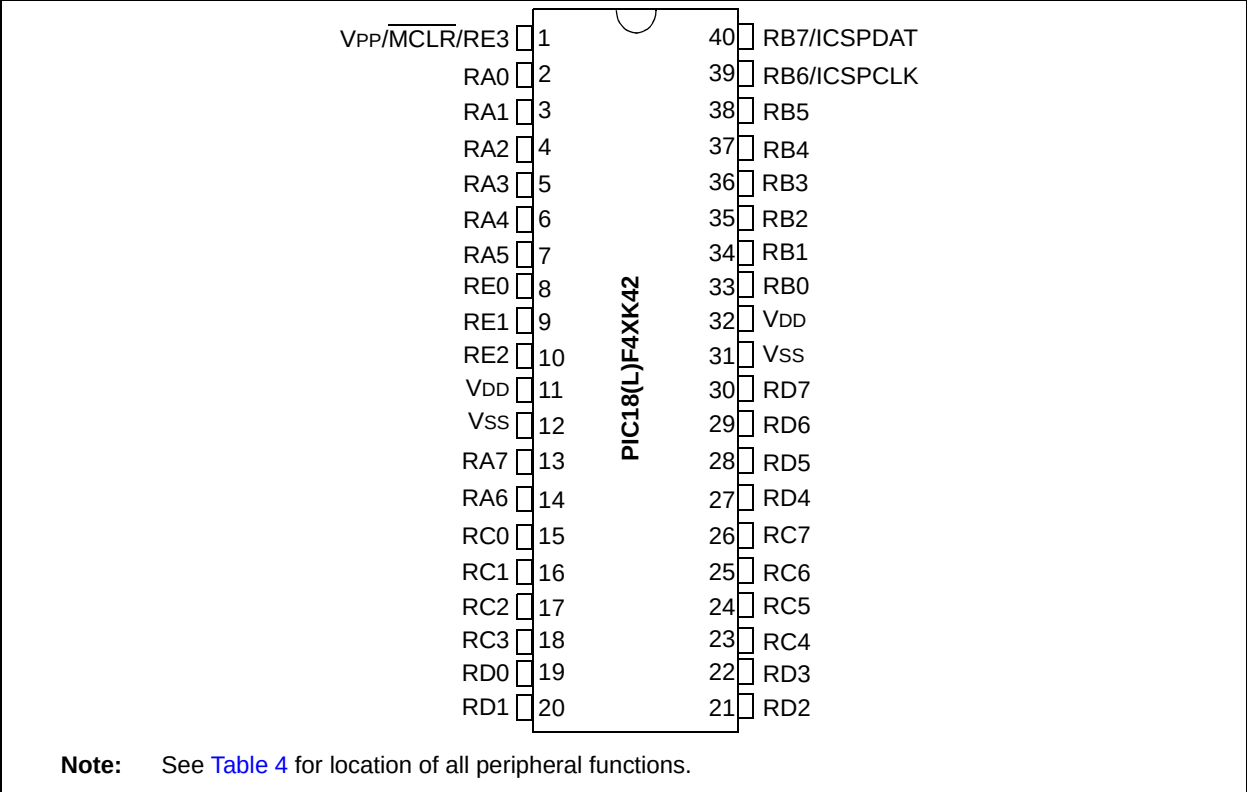


FIGURE 4: 40-PIN PDIP FOR PIC18(L)F4XK42



# PIC18(L)F2X/4X/5XK42

**FIGURE 5: 40-PIN UQFN (5X5X0.5 mm) FOR PIC18(L)F4XK42**

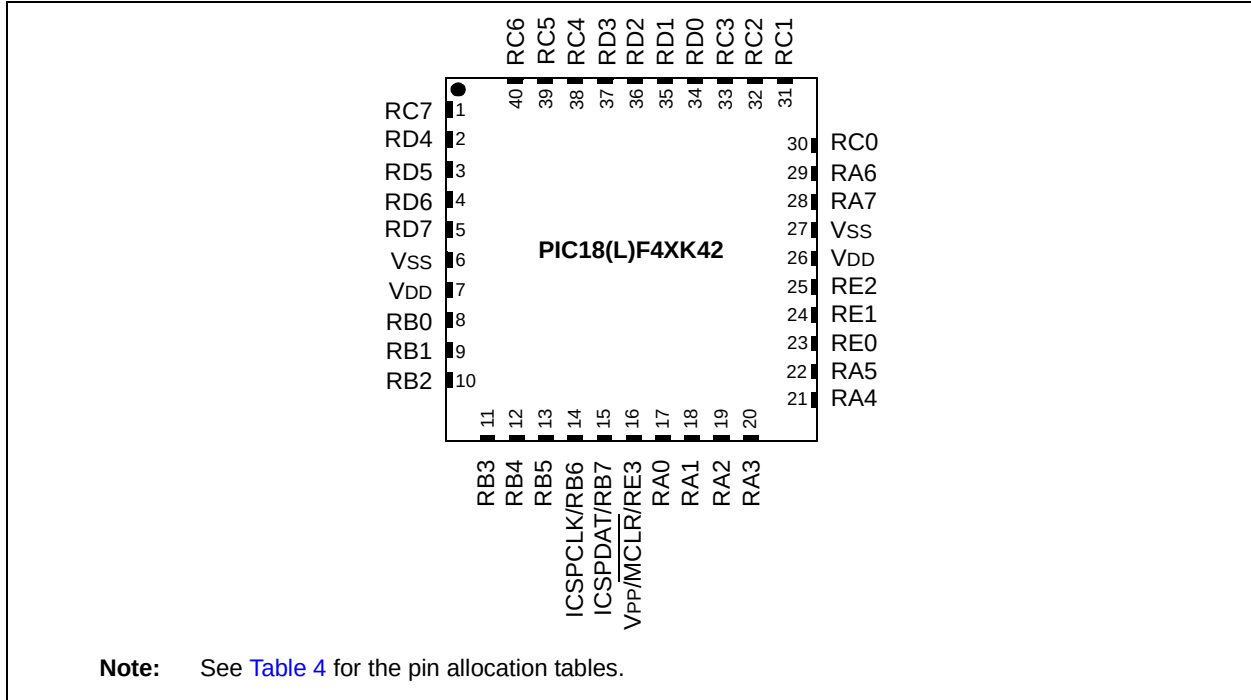
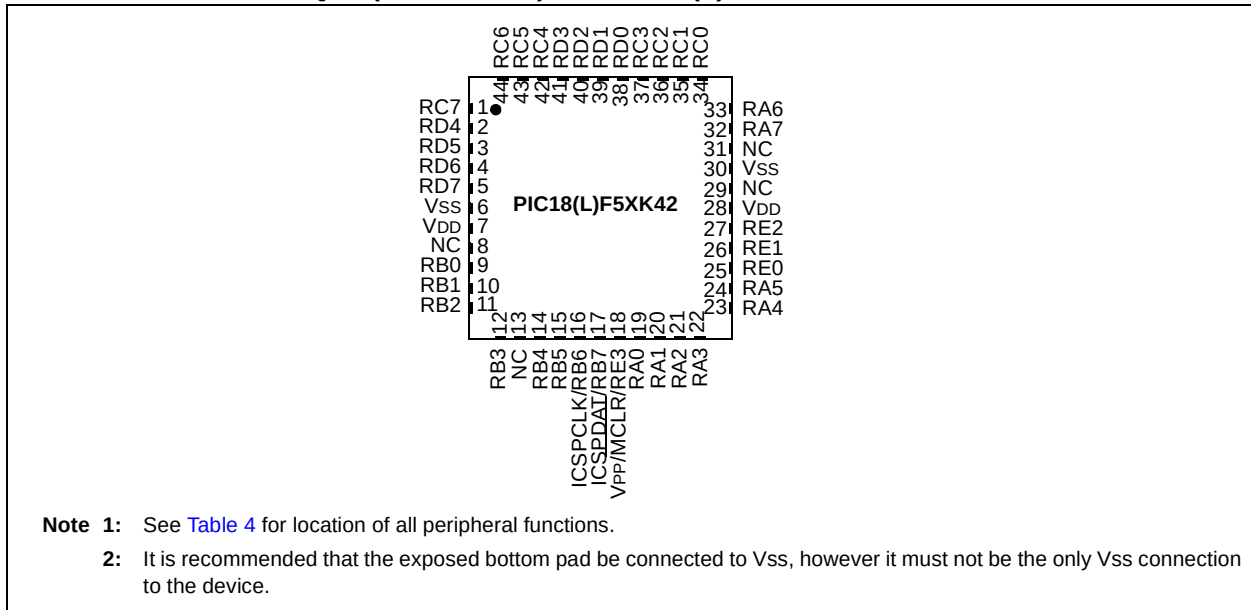


**FIGURE 6: 44-PIN QFN (8X8X0.9 mm) FOR PIC18(L)F5XK42**



# PIC18(L)F2X/4X/5XK42

FIGURE 7: 44-PIN TQFP FOR PIC18(L)F4XK42

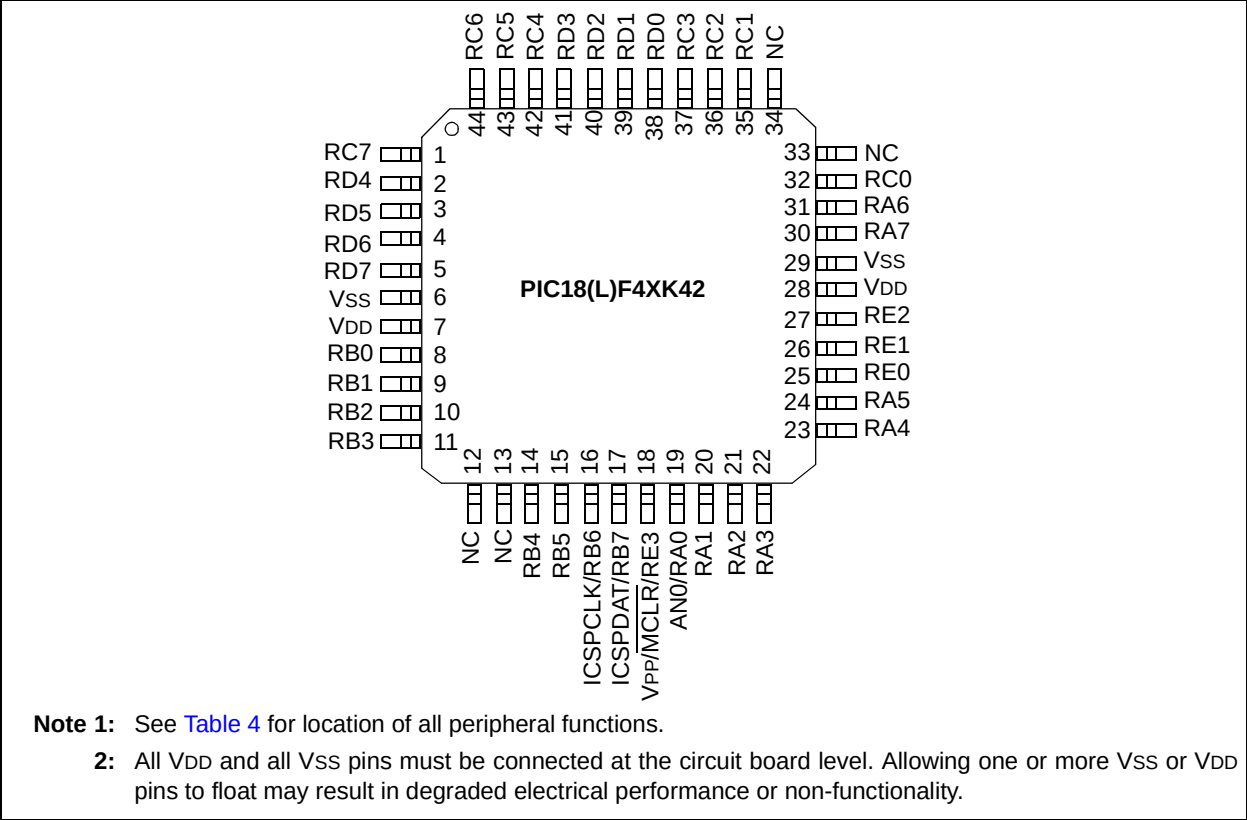
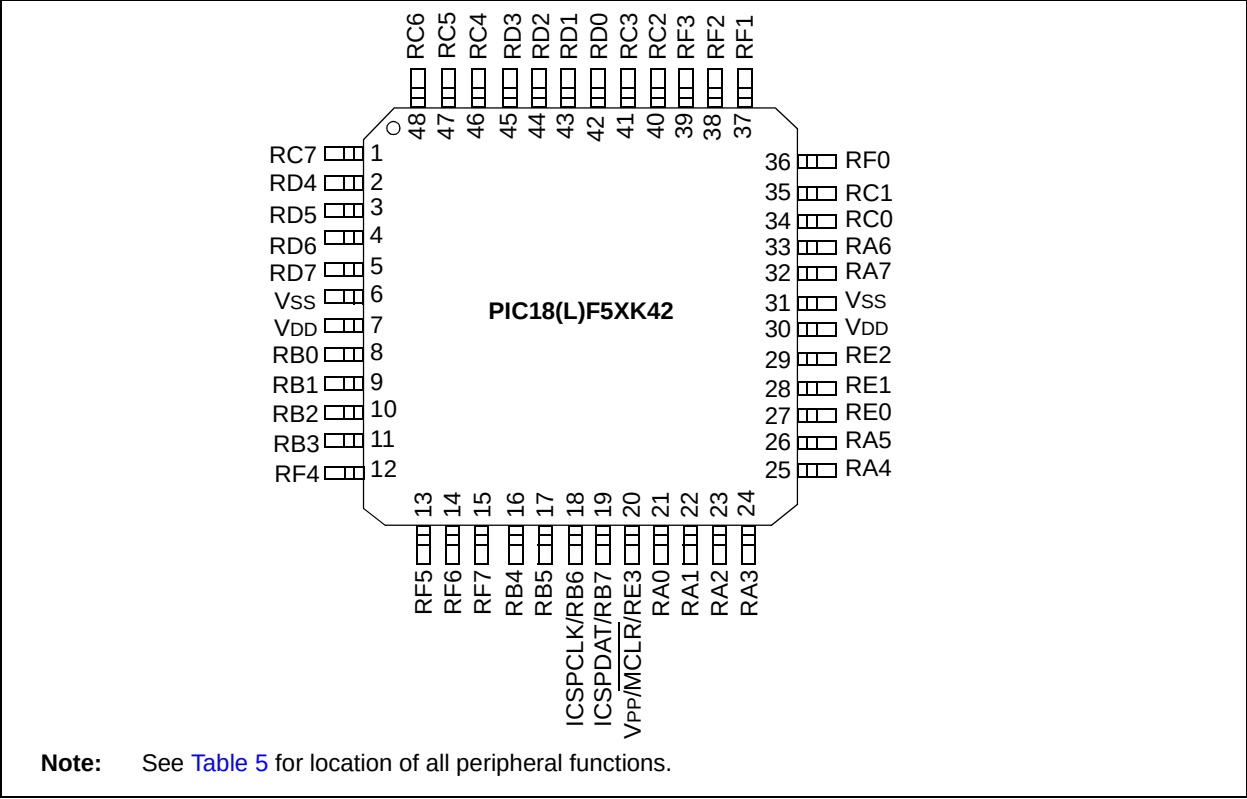


FIGURE 8: 48-PIN TQFP/UQFN FOR PIC18(L)F5XK42



## PIN ALLOCATION TABLES

TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK42)

| I/O | 28-Pin SPDIP/SOIC/SSOP | 28-Pin (U)QFN | ADC                        | Voltage Reference | DAC      | Comparators   | Zero Cross Detect | I <sup>2</sup> C      | SPI                | UART                | DSM                   | Timers/SMT           | CCP and PWM         | CWG                   | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change       | Basic       |
|-----|------------------------|---------------|----------------------------|-------------------|----------|---------------|-------------------|-----------------------|--------------------|---------------------|-----------------------|----------------------|---------------------|-----------------------|-----------------------|-----|------------------------|---------------------------|-------------|
| RA0 | 2                      | 27            | ANA0                       | —                 | —        | C1IN0-C2IN0-  | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | CLCIN0 <sup>(1)</sup> | —   | —                      | IOCA0                     | —           |
| RA1 | 3                      | 28            | ANA1                       | —                 | —        | C1IN1-C2IN1-  | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | CLCIN1 <sup>(1)</sup> | —   | —                      | IOCA1                     | —           |
| RA2 | 4                      | 1             | ANA2                       | VREF-             | DAC1OUT1 | C1IN0+ C2IN0+ | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | —                     | —   | —                      | IOCA2                     | —           |
| RA3 | 5                      | 2             | ANA3                       | VREF+             | —        | C1IN1+        | —                 | —                     | —                  | —                   | MDCARL <sup>(1)</sup> | —                    | —                   | —                     | —                     | —   | —                      | IOCA3                     | —           |
| RA4 | 6                      | 3             | ANA4                       | —                 | —        | —             | —                 | —                     | —                  | —                   | MDCARH <sup>(1)</sup> | T0CKI <sup>(1)</sup> | —                   | —                     | —                     | —   | —                      | IOCA4                     | —           |
| RA5 | 7                      | 4             | ANA5                       | —                 | —        | —             | —                 | —                     | SS1 <sup>(1)</sup> | —                   | MDSRC <sup>(1)</sup>  | —                    | —                   | —                     | —                     | —   | —                      | IOCA5                     | —           |
| RA6 | 10                     | 7             | ANA6                       | —                 | —        | —             | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | —                     | —   | —                      | IOCA6                     | OSC2 CLKOUT |
| RA7 | 9                      | 6             | ANA7                       | —                 | —        | —             | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | —                     | —   | —                      | IOCA7                     | OSC1 CLKIN  |
| RB0 | 21                     | 18            | ANB0                       | —                 | —        | C2IN1+        | ZCD               | —                     | —                  | —                   | —                     | —                    | CCP4 <sup>(1)</sup> | CWG1IN <sup>(1)</sup> | —                     | —   | —                      | INT0 <sup>(1)</sup> IOCB0 | —           |
| RB1 | 22                     | 19            | ANB1                       | —                 | —        | C1IN3-C2IN3-  | —                 | SCL2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                    | —                   | CWG2IN <sup>(1)</sup> | —                     | —   | —                      | INT1 <sup>(1)</sup> IOCB1 | —           |
| RB2 | 23                     | 20            | ANB2                       | —                 | —        | —             | —                 | SDA2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                    | —                   | CWG3IN <sup>(1)</sup> | —                     | —   | —                      | INT2 <sup>(1)</sup> IOCB2 | —           |
| RB3 | 24                     | 21            | ANB3                       | —                 | —        | C1IN2-C2IN2-  | —                 | —                     | —                  | —                   | —                     | —                    | —                   | —                     | —                     | —   | —                      | IOCB3                     | —           |
| RB4 | 25                     | 22            | ANB4 ADCACT <sup>(1)</sup> | —                 | —        | —             | —                 | —                     | —                  | —                   | —                     | T5G <sup>(1)</sup>   | —                   | —                     | —                     | —   | —                      | IOCB4                     | —           |
| RB5 | 26                     | 23            | ANB5                       | —                 | —        | —             | —                 | —                     | —                  | —                   | —                     | T1G <sup>(1)</sup>   | CCP3 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCB5                     | —           |
| RB6 | 27                     | 24            | ANB6                       | —                 | —        | —             | —                 | —                     | —                  | CTS2 <sup>(1)</sup> | —                     | —                    | —                   | —                     | CLCIN2 <sup>(1)</sup> | —   | —                      | IOCB6                     | ICSPCLK     |
| RB7 | 28                     | 25            | ANB7                       | —                 | DAC1OUT2 | —             | —                 | —                     | —                  | RX2 <sup>(1)</sup>  | —                     | T6IN(1)              | —                   | —                     | CLCIN3 <sup>(1)</sup> | —   | —                      | IOCB7                     | ICSPDAT     |

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All output signals shown in this row are PPS remappable.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

**TABLE 3: 28-PIN ALLOCATION TABLE (PIC18(L)F2XK42) (CONTINUED)**

| I/O                | 28-Pin SPDIP/SOIC/SSOP | 28-Pin (U)QFN | ADC              | Voltage Reference | DAC | Comparators    | Zero Cross Detect | I <sup>2</sup> C             | SPI                 | UART                                         | DSM | Timers/SMT                                                                                 | CCP and PWM                                                              | CWG                                                                                                      | CLC                                      | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic                   |
|--------------------|------------------------|---------------|------------------|-------------------|-----|----------------|-------------------|------------------------------|---------------------|----------------------------------------------|-----|--------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------|---------------------|-------------------------|
| RC0                | 11                     | 8             | ANC0             | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | T1CK <sup>(1)</sup><br>T3CK <sup>(1)</sup><br>T3G <sup>(1)</sup><br>SMTWIN1 <sup>(1)</sup> | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC0               | SOSCO                   |
| RC1                | 12                     | 9             | ANC1             | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | SMTSIG1 <sup>(1)</sup>                                                                     | CCP2 <sup>(1)</sup>                                                      | —                                                                                                        | —                                        | —   | —                      | IOCC1               | SOSCI                   |
| RC2                | 13                     | 10            | ANC2             | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | T5CK <sup>(1)</sup>                                                                        | CCP1 <sup>(1)</sup>                                                      | —                                                                                                        | —                                        | —   | —                      | IOCC2               | —                       |
| RC3                | 14                     | 11            | ANC3             | —                 | —   | —              | —                 | SCL1 <sup>(3,4)</sup>        | SCK1 <sup>(1)</sup> | —                                            | —   | T2IN <sup>(1)</sup>                                                                        | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC3               | —                       |
| RC4                | 15                     | 12            | ANC4             | —                 | —   | —              | —                 | SDA1 <sup>(3,4)</sup>        | SDI1 <sup>(1)</sup> | —                                            | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC4               | —                       |
| RC5                | 16                     | 13            | ANC5             | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | T4IN <sup>(1)</sup>                                                                        | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC5               | —                       |
| RC6                | 17                     | 14            | ANC6             | —                 | —   | —              | —                 | —                            | —                   | CTS1 <sup>(1)</sup>                          | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC6               | —                       |
| RC7                | 18                     | 15            | ANC7             | —                 | —   | —              | —                 | —                            | —                   | RX1 <sup>(1)</sup>                           | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCC7               | —                       |
| RE3                | 1                      | 26            | —                | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | IOCE3               | MCLR<br>V <sub>PP</sub> |
| VDD                | 20                     | 17            | —                | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | —                   | —                       |
| VSS                | 8,<br>19               | 5,<br>16      | —                | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | —                                                                                          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | —                   | —                       |
| OUT <sup>(2)</sup> | —                      | —             | ADGRDA<br>ADGRDB | —                 | —   | C1OUT<br>C2OUT | —                 | SDA1<br>SCL1<br>SDA2<br>SCL2 | SS1<br>SCK1<br>SDO1 | RTS1<br>TXDE1<br>TX1<br>RTS2<br>TXDE2<br>TX2 | DSM | TMR0                                                                                       | CCP1<br>CCP2<br>CCP3<br>CCP4<br>PWM5OUT<br>PWM6OUT<br>PWM7OUT<br>PWM8OUT | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D<br>CWG2A<br>CWG2B<br>CWG2C<br>CWG2D<br>CWG3A<br>CWG3B<br>CWG3C<br>CWG3D | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT | NCO | CLKR                   | —                   | —                       |

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All output signals shown in this row are PPS remappable.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

**TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42**

| I/O | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN | ADC                           | Voltage Reference | DAC      | Comparators      | Zero Cross Detect | I <sup>2</sup> C      | SPI                | UART                | DSM                   | Timers/SMT                                                                                   | CCP and PWM         | CWG                   | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change          | Basic          |
|-----|-------------|-------------|-------------|------------|-------------------------------|-------------------|----------|------------------|-------------------|-----------------------|--------------------|---------------------|-----------------------|----------------------------------------------------------------------------------------------|---------------------|-----------------------|-----------------------|-----|------------------------|------------------------------|----------------|
| RA0 | 2           | 19          | 17          | 19         | ANA0                          | —                 | —        | C1IN0-<br>C2IN0- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | CLCIN0 <sup>(1)</sup> | —   | —                      | IOCA0                        | —              |
| RA1 | 3           | 20          | 18          | 20         | ANA1                          | —                 | —        | C1IN1-<br>C2IN1- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | CLCIN1 <sup>(1)</sup> | —   | —                      | IOCA1                        | —              |
| RA2 | 4           | 21          | 19          | 21         | ANA2                          | VREF-             | DAC1OUT1 | C1IN0+<br>C2IN0+ | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA2                        | —              |
| RA3 | 5           | 22          | 20          | 22         | ANA3                          | VREF+             | —        | C1IN1+           | —                 | —                     | —                  | —                   | MDCARL <sup>(1)</sup> | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA3                        | —              |
| RA4 | 6           | 23          | 21          | 23         | ANA4                          | —                 | —        | —                | —                 | —                     | —                  | —                   | MDCARH <sup>(1)</sup> | T0CKI <sup>(1)</sup>                                                                         | —                   | —                     | —                     | —   | —                      | IOCA4                        | —              |
| RA5 | 7           | 24          | 22          | 24         | ANA5                          | —                 | —        | —                | —                 | —                     | SS1 <sup>(1)</sup> | —                   | MDSRC <sup>(1)</sup>  | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA5                        | —              |
| RA6 | 14          | 31          | 29          | 33         | ANA6                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA6                        | OSC2<br>CLKOUT |
| RA7 | 13          | 30          | 28          | 32         | ANA7                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA7                        | OSC1<br>CLKIN  |
| RB0 | 33          | 8           | 8           | 9          | ANB0                          | —                 | —        | C2IN1+           | ZCD               | —                     | —                  | —                   | —                     | —                                                                                            | CCP4 <sup>(1)</sup> | CWG1IN <sup>(1)</sup> | —                     | —   | —                      | INT0 <sup>(1)</sup><br>IOCB0 | —              |
| RB1 | 34          | 9           | 9           | 10         | ANB1                          | —                 | —        | C1IN3-<br>C2IN3- | —                 | SCL2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                                                                                            | —                   | CWG2IN <sup>(1)</sup> | —                     | —   | —                      | INT1 <sup>(1)</sup><br>IOCB1 | —              |
| RB2 | 35          | 10          | 10          | 11         | ANB2                          | —                 | —        | —                | —                 | SDA2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                                                                                            | —                   | CWG3IN <sup>(1)</sup> | —                     | —   | —                      | INT2 <sup>(1)</sup><br>IOCB2 | —              |
| RB3 | 36          | 11          | 11          | 12         | ANB3                          | —                 | —        | C1IN2-<br>C2IN2- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCB3                        | —              |
| RB4 | 37          | 14          | 12          | 14         | ANB4<br>ADCACT <sup>(1)</sup> | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T5G <sup>(1)</sup>                                                                           | —                   | —                     | —                     | —   | —                      | IOCB4                        | —              |
| RB5 | 38          | 15          | 13          | 15         | ANB5                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T1G <sup>(1)</sup>                                                                           | CCP3 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCB5                        | —              |
| RB6 | 39          | 16          | 14          | 16         | ANB6                          | —                 | —        | —                | —                 | —                     | —                  | CTS2 <sup>(1)</sup> | —                     | —                                                                                            | —                   | —                     | CLCIN2 <sup>(1)</sup> | —   | —                      | IOCB6                        | ICSPCLK        |
| RB7 | 40          | 17          | 15          | 17         | ANB7                          | —                 | DAC1OUT2 | —                | —                 | —                     | —                  | RX2 <sup>(1)</sup>  | —                     | T6IN <sup>(1)</sup>                                                                          | —                   | —                     | CLCIN3 <sup>(1)</sup> | —   | —                      | IOCB7                        | ICSPDAT        |
| RC0 | 15          | 32          | 30          | 34         | ANC0                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T3G <sup>(1)</sup><br>SMTWIN1 <sup>(1)</sup> | —                   | —                     | —                     | —   | —                      | IOCC0                        | SOSCO          |
| RC1 | 16          | 35          | 31          | 35         | ANC1                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | SMTSIG1 <sup>(1)</sup>                                                                       | CCP2 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCC1                        | SOSCI          |

**Note**

- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
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**TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42 (CONTINUED)**

| I/O | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN      | ADC  | Voltage Reference | DAC | Comparators | Zero Cross Detect | I <sup>2</sup> C      | SPI                 | UART                | DSM | Timers/SMT           | CCP and PWM         | CWG | CLC | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic                   |
|-----|-------------|-------------|-------------|-----------------|------|-------------------|-----|-------------|-------------------|-----------------------|---------------------|---------------------|-----|----------------------|---------------------|-----|-----|-----|------------------------|---------------------|-------------------------|
| RC2 | 17          | 36          | 32          | 36              | ANC2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | T5CKI <sup>(1)</sup> | CCP1 <sup>(1)</sup> | —   | —   | —   | —                      | IOCC2               | —                       |
| RC3 | 18          | 37          | 33          | 37              | ANC3 | —                 | —   | —           | —                 | SCL1 <sup>(3,4)</sup> | SCK1 <sup>(1)</sup> | —                   | —   | T2IN <sup>(1)</sup>  | —                   | —   | —   | —   | —                      | IOCC3               | —                       |
| RC4 | 23          | 42          | 38          | 42              | ANC4 | —                 | —   | —           | —                 | SDA1 <sup>(3,4)</sup> | SDI1 <sup>(1)</sup> | —                   | —   | —                    | —                   | —   | —   | —   | —                      | IOCC4               | —                       |
| RC5 | 24          | 43          | 39          | 43              | ANC5 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | T4IN <sup>(4)</sup>  | —                   | —   | —   | —   | —                      | IOCC5               | —                       |
| RC6 | 25          | 44          | 40          | 44              | ANC6 | —                 | —   | —           | —                 | —                     | —                   | CTS1 <sup>(1)</sup> | —   | —                    | —                   | —   | —   | —   | —                      | IOCC6               | —                       |
| RC7 | 26          | 1           | 1           | 1               | ANC7 | —                 | —   | —           | —                 | —                     | —                   | RX1 <sup>(1)</sup>  | —   | —                    | —                   | —   | —   | —   | —                      | IOCC7               | —                       |
| RD0 | 19          | 38          | 34          | 38              | AND0 | —                 | —   | —           | —                 | — <sup>(4)</sup>      | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD1 | 20          | 39          | 35          | 39              | AND1 | —                 | —   | —           | —                 | — <sup>(4)</sup>      | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD2 | 21          | 40          | 36          | 40              | AND2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD3 | 22          | 41          | 37          | 41              | AND3 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD4 | 27          | 2           | 2           | 2               | AND4 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD5 | 28          | 3           | 3           | 3               | AND5 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD6 | 29          | 4           | 4           | 4               | AND6 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD7 | 30          | 5           | 5           | 5               | AND7 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE0 | 8           | 25          | 23          | 25              | ANE0 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE1 | 9           | 26          | 24          | 26              | ANE1 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE2 | 10          | 27          | 25          | 27              | ANE2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE3 | 1           | 18          | 16          | 18              | —    | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | IOCE3               | MCLR<br>V <sub>PP</sub> |
| VDD | 11,<br>32   | 7,<br>28    | 7,<br>26    | 8,<br>28        | —    | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| VSS | 12,<br>31   | 6,<br>29    | 6,<br>27    | 6,<br>31,<br>30 | —    | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |

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**TABLE 4: 40/44-PIN ALLOCATION TABLE FOR PIC18(L)F4XK42, PIC18(L)F5XK42 (CONTINUED)**

| I/O                | 40-Pin PDIP | 44-Pin TQFP | 40-Pin UQFN | 44-Pin QFN | ADC              | Voltage Reference | DAC | Comparators    | Zero Cross Detect | I <sup>2</sup> C             | SPI                 | UART                                         | DSM | Timers/SMT | CCP and PWM                                                              | CWG                                                                                                      | CLC                                      | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic |
|--------------------|-------------|-------------|-------------|------------|------------------|-------------------|-----|----------------|-------------------|------------------------------|---------------------|----------------------------------------------|-----|------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------|---------------------|-------|
| OUT <sup>(2)</sup> | —           | —           | —           | —          | ADGRDA<br>ADGRDB | —                 | —   | C1OUT<br>C2OUT | —                 | SDA1<br>SCL1<br>SDA2<br>SCL2 | SS1<br>SCK1<br>SDO1 | RTS1<br>TXDE1<br>TX1<br>RTS2<br>TXDE2<br>TX2 | DSM | TMR0       | CCP1<br>CCP2<br>CCP3<br>CCP4<br>PWM5OUT<br>PWM6OUT<br>PWM7OUT<br>PWM8OUT | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D<br>CWG2A<br>CWG2B<br>CWG2C<br>CWG2D<br>CWG3A<br>CWG3B<br>CWG3C<br>CWG3D | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT | NCO | CLKR                   | —                   | —     |

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- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
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**TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42**

| I/O | 48-Pin TQFP | 48-Pin UQFN | ADC                           | Voltage Reference | DAC      | Comparators      | Zero Cross Detect | I <sup>2</sup> C      | SPI                | UART                | DSM                   | Timers/SMT                                                                                   | CCP and PWM         | CWG                   | CLC                   | NCO | Clock Reference (CLKR) | Interrupt-on-Change          | Basic          |
|-----|-------------|-------------|-------------------------------|-------------------|----------|------------------|-------------------|-----------------------|--------------------|---------------------|-----------------------|----------------------------------------------------------------------------------------------|---------------------|-----------------------|-----------------------|-----|------------------------|------------------------------|----------------|
| RA0 | 21          | 21          | ANA0                          | —                 | —        | C1IN0-<br>C2IN0- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | CLCIN0 <sup>(1)</sup> | —   | —                      | IOCA0                        | —              |
| RA1 | 22          | 22          | ANA1                          | —                 | —        | C1IN1-<br>C2IN1- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | CLCIN1 <sup>(1)</sup> | —   | —                      | IOCA1                        | —              |
| RA2 | 23          | 23          | ANA2                          | VREF-             | DAC1OUT1 | C1IN0+<br>C2IN0+ | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA2                        | —              |
| RA3 | 24          | 24          | ANA3                          | VREF+             | —        | C1IN1+           | —                 | —                     | —                  | —                   | MDCARL <sup>(1)</sup> | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA3                        | —              |
| RA4 | 25          | 25          | ANA4                          | —                 | —        | —                | —                 | —                     | —                  | —                   | MDCARH <sup>(1)</sup> | T0CKI <sup>(1)</sup>                                                                         | —                   | —                     | —                     | —   | —                      | IOCA4                        | —              |
| RA5 | 26          | 26          | ANA5                          | —                 | —        | —                | —                 | —                     | SS1 <sup>(1)</sup> | —                   | MDSRC <sup>(1)</sup>  | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA5                        | —              |
| RA6 | 33          | 33          | ANA6                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA6                        | OSC2<br>CLKOUT |
| RA7 | 32          | 32          | ANA7                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCA7                        | OSC1<br>CLKIN  |
| RB0 | 8           | 8           | ANB0                          | —                 | —        | C2IN1+           | ZCD               | —                     | —                  | —                   | —                     | —                                                                                            | CCP4 <sup>(1)</sup> | CWG1IN <sup>(1)</sup> | —                     | —   | —                      | INT0 <sup>(1)</sup><br>IOCB0 | —              |
| RB1 | 9           | 9           | ANB1                          | —                 | —        | C1IN3-<br>C2IN3- | —                 | SCL2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                                                                                            | —                   | CWG2IN <sup>(1)</sup> | —                     | —   | —                      | INT1 <sup>(1)</sup><br>IOCB1 | —              |
| RB2 | 10          | 10          | ANB2                          | —                 | —        | —                | —                 | SDA2 <sup>(3,4)</sup> | —                  | —                   | —                     | —                                                                                            | —                   | CWG3IN <sup>(1)</sup> | —                     | —   | —                      | INT2 <sup>(1)</sup><br>IOCB2 | —              |
| RB3 | 11          | 11          | ANB3                          | —                 | —        | C1IN2-<br>C2IN2- | —                 | —                     | —                  | —                   | —                     | —                                                                                            | —                   | —                     | —                     | —   | —                      | IOCB3                        | —              |
| RB4 | 16          | 16          | ANB4<br>ADCACT <sup>(1)</sup> | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T5G <sup>(1)</sup>                                                                           | —                   | —                     | —                     | —   | —                      | IOCB4                        | —              |
| RB5 | 17          | 17          | ANB5                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T1G <sup>(1)</sup>                                                                           | CCP3 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCB5                        | —              |
| RB6 | 18          | 18          | ANB6                          | —                 | —        | —                | —                 | —                     | —                  | CTS2 <sup>(1)</sup> | —                     | —                                                                                            | —                   | —                     | CLCIN2 <sup>(1)</sup> | —   | —                      | IOCB6                        | ICSPCLK        |
| RB7 | 19          | 19          | ANB7                          | —                 | DAC1OUT2 | —                | —                 | —                     | —                  | RX2 <sup>(1)</sup>  | —                     | T6IN <sup>(1)</sup>                                                                          | —                   | —                     | CLCIN3 <sup>(1)</sup> | —   | —                      | IOCB7                        | ICSPDAT        |
| RC0 | 34          | 34          | ANC0                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | T1CKI <sup>(4)</sup><br>T3CKI <sup>(4)</sup><br>T3G <sup>(1)</sup><br>SMTWIN1 <sup>(1)</sup> | —                   | —                     | —                     | —   | —                      | IOCC0                        | SOSCO          |
| RC1 | 35          | 35          | ANC1                          | —                 | —        | —                | —                 | —                     | —                  | —                   | —                     | SMTSIG1 <sup>(1)</sup>                                                                       | CCP2 <sup>(1)</sup> | —                     | —                     | —   | —                      | IOCC1                        | SOSCI          |

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**TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42 (CONTINUED)**

| I/O             | 48-Pin TQFP | 48-Pin UQFN | ADC  | Voltage Reference | DAC | Comparators | Zero Cross Detect | I <sup>2</sup> C      | SPI                 | UART                | DSM | Timers/SMT           | CCP and PWM         | CWG | CLC | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic                   |
|-----------------|-------------|-------------|------|-------------------|-----|-------------|-------------------|-----------------------|---------------------|---------------------|-----|----------------------|---------------------|-----|-----|-----|------------------------|---------------------|-------------------------|
| RC2             | 40          | 40          | ANC2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | T5CK1 <sup>(1)</sup> | CCP1 <sup>(1)</sup> | —   | —   | —   | —                      | IOCC2               | —                       |
| RC3             | 41          | 41          | ANC3 | —                 | —   | —           | —                 | SCL1 <sup>(3,4)</sup> | SCK1 <sup>(1)</sup> | —                   | —   | T2IN <sup>(1)</sup>  | —                   | —   | —   | —   | —                      | IOCC3               | —                       |
| RC4             | 46          | 46          | ANC4 | —                 | —   | —           | —                 | SDA1 <sup>(3,4)</sup> | SDI1 <sup>(1)</sup> | —                   | —   | —                    | —                   | —   | —   | —   | —                      | IOCC4               | —                       |
| RC5             | 47          | 47          | ANC5 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | T4IN <sup>(1)</sup>  | —                   | —   | —   | —   | —                      | IOCC5               | —                       |
| RC6             | 48          | 48          | ANC6 | —                 | —   | —           | —                 | —                     | —                   | CTS1 <sup>(1)</sup> | —   | —                    | —                   | —   | —   | —   | —                      | IOCC6               | —                       |
| RC7             | 1           | 1           | ANC7 | —                 | —   | —           | —                 | —                     | —                   | RX1 <sup>(1)</sup>  | —   | —                    | —                   | —   | —   | —   | —                      | IOCC7               | —                       |
| RD0             | 42          | 42          | AND0 | —                 | —   | —           | —                 | — <sup>(4)</sup>      | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD1             | 43          | 43          | AND1 | —                 | —   | —           | —                 | — <sup>(4)</sup>      | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD2             | 44          | 44          | AND2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD3             | 45          | 45          | AND3 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD4             | 2           | 2           | AND4 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD5             | 3           | 3           | AND5 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD6             | 4           | 4           | AND6 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RD7             | 5           | 5           | AND7 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE0             | 27          | 27          | ANE0 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE1             | 28          | 28          | ANE1 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE2             | 29          | 29          | ANE2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RE3             | 20          | 20          | —    | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | IOCE3               | MCLR<br>V <sub>PP</sub> |
| RF0             | 36          | 36          | ANF0 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF1             | 37          | 37          | ANF1 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF2             | 38          | 38          | ANF2 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF3             | 39          | 39          | ANF3 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF4             | 12          | 12          | ANF4 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF5             | 13          | 13          | ANF5 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF6             | 14          | 14          | ANF6 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| RF7             | 15          | 15          | ANF7 | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |
| V <sub>DD</sub> | 7,<br>30    | 7,<br>30    | —    | —                 | —   | —           | —                 | —                     | —                   | —                   | —   | —                    | —                   | —   | —   | —   | —                      | —                   | —                       |

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All output signals shown in this row are PPS remappable.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

**TABLE 5: 48-PIN ALLOCATION TABLE FOR PIC18(L)F5XK42 (CONTINUED)**

| I/O                | 48-Pin TQFP | 48-Pin UQFN | ADC              | Voltage Reference | DAC | Comparators    | Zero Cross Detect | I <sup>2</sup> C             | SPI                 | UART                                         | DSM | Timers/SMT | CCP and PWM                                                              | CWG                                                                                                      | CLC                                      | NCO | Clock Reference (CLKR) | Interrupt-on-Change | Basic |
|--------------------|-------------|-------------|------------------|-------------------|-----|----------------|-------------------|------------------------------|---------------------|----------------------------------------------|-----|------------|--------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|------------------------------------------|-----|------------------------|---------------------|-------|
| VSS                | 6, 31       | 6, 31       | —                | —                 | —   | —              | —                 | —                            | —                   | —                                            | —   | —          | —                                                                        | —                                                                                                        | —                                        | —   | —                      | —                   | —     |
| OUT <sup>(2)</sup> | —           | —           | ADGRDA<br>ADGRDB | —                 | —   | C1OUT<br>C2OUT | —                 | SDA1<br>SCL1<br>SDA2<br>SCL2 | SS1<br>SCK1<br>SDO1 | RTS1<br>TXDE1<br>TX1<br>RTS2<br>TXDE2<br>TX2 | DSM | TMR0       | CCP1<br>CCP2<br>CCP3<br>CCP4<br>PWM5OUT<br>PWM6OUT<br>PWM7OUT<br>PWM8OUT | CWG1A<br>CWG1B<br>CWG1C<br>CWG1D<br>CWG2A<br>CWG2B<br>CWG2C<br>CWG2D<br>CWG3A<br>CWG3B<br>CWG3C<br>CWG3D | CLC1OUT<br>CLC2OUT<br>CLC3OUT<br>CLC4OUT | NCO | CLKR                   | —                   | —     |

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All output signals shown in this row are PPS remappable.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C and SMBus 3.0/2.0 logic levels; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.

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