KAI-1020

1000 (H) x 1000 (V) Interline CCD Image Sensor

ON Semiconductor®

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Description

The KAI−1020 Image Sensor is a one megapixel interline CCD with integrated clock drivers and on-chip correlated double sampling. The progressive scan architecture and global electronic shutter provide excellent image quality for full motion video and still image capture.

The integrated clock drivers allow for easy integration with CMOS logic timing generators. The sensor features a fast line dump for high-speed sub-window readout and single (30 fps) or dual (48 fps) output operation.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	1028 (H) × 1008 (V)
Number of Effective Pixels	1004 (H) × 1004 (V)
Number of Active Pixels	1000 (H) × 1000 (V)
Pixel Size	7.4 μm (H) × 7.4 μm (V)
Active Image Size	7.4 mm (H) × 7.4 mm (V) 10.5 mm (Diagonal) 2/3″ Optical Format
Aspect Ratio	1:1
Number of Outputs	1 or 2
Saturation Signal	40,000 e^-
Output Sensitivity	12 μV/e^-
Quantum Efficiency ABA (500 nm) CBA (620 nm, 540 nm, 460 nm)	 44% 31%, 36%, 41%
Dark Noise	50 e^- rms
Dark Current (Typical)	< 0.5 nA/cm^2
Dynamic Range	58 dB
Blooming Suppression	100 X
Image Lag	< 10 e^-
Smear	< 0.03%
Maximum Data Rate	40 MHz/Channel (2 Channels)
Frame Rate Progressive Scan, One Output Progressive Scan, Dual Outputs Interlaced Scan, One Output	 30 fps 48 fps 49 fps
Integrated Vertical Clock Driver	
Integrated Correlated Double Sampling (CDS)	
Integrated Electronic Shutter Driver	
Package	68 pin PGA or 64 pin CLCC
Cover Glass	AR coated, 2 sides

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

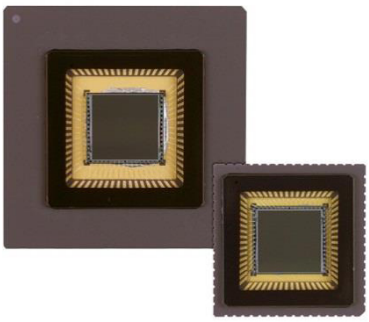

Figure 1. KAI−1020 Interline CCD Image Sensor

Features

- 10-Bits Dynamic Range at 40 MHz
- Large 7.4 μm Square Pixels for High Sensitivity
- Progressive Scan (Non-Interlaced)
- Integrated Correlated Double Sampling (CDS) Up to 40 MHz
- Integrated Electronic Shutter Driver
- Reversible HCCD Capable of 40 MHz Operation All Timing Inputs 0 to 5 V
- Single or Dual Video Output Operation
- Progressive Scan or Interlaced
- Fast Dump Gate for High Speed Sub-Window Readout
- Anti-Blooming Protection

Application

- Machine Vision
- Medical
- Scientific
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−1020 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−1020−AAA−JP−BA	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, No Coatings, Standard Grade	KAI−1020 Serial Number
KAI−1020−ABB−FD−AE	Monochrome, Telecentric Microlens, CLCC Package, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	KAI−1020−ABB Serial Number
KAI−1020−ABB−FD−BA	Monochrome, Telecentric Microlens, CLCC Package, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	
KAI−1020−ABB−JP−AE	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Engineering Sample	
KAI−1020−ABB−JP−BA	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass (No Coatings), Standard Grade	
KAI−1020−ABB−JB−AE	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass (No Coatings), Engineering Sample	
KAI−1020−ABB−JB−BA	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass (No Coatings), Standard Grade	
KAI−1020−ABB−JD−AE	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAI−1020−ABB−JD−BA	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	
KAI−1020−CBA−FD−AE	Color (Bayer RGB), Telecentric Microlens, CLCC Package, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	KAI−1020CM Serial Number
KAI−1020−CBA−FD−BA	Color (Bayer RGB), Telecentric Microlens, CLCC Package, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	
KAI−1020−CBA−JD−AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KAI−1020−CBA−JD−BA	Color (Bayer RGB), Telecentric Microlens, PGA Package, Clear Cover Glass with AR Coating (Both Sides), Standard Grade	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−1020−12−40−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

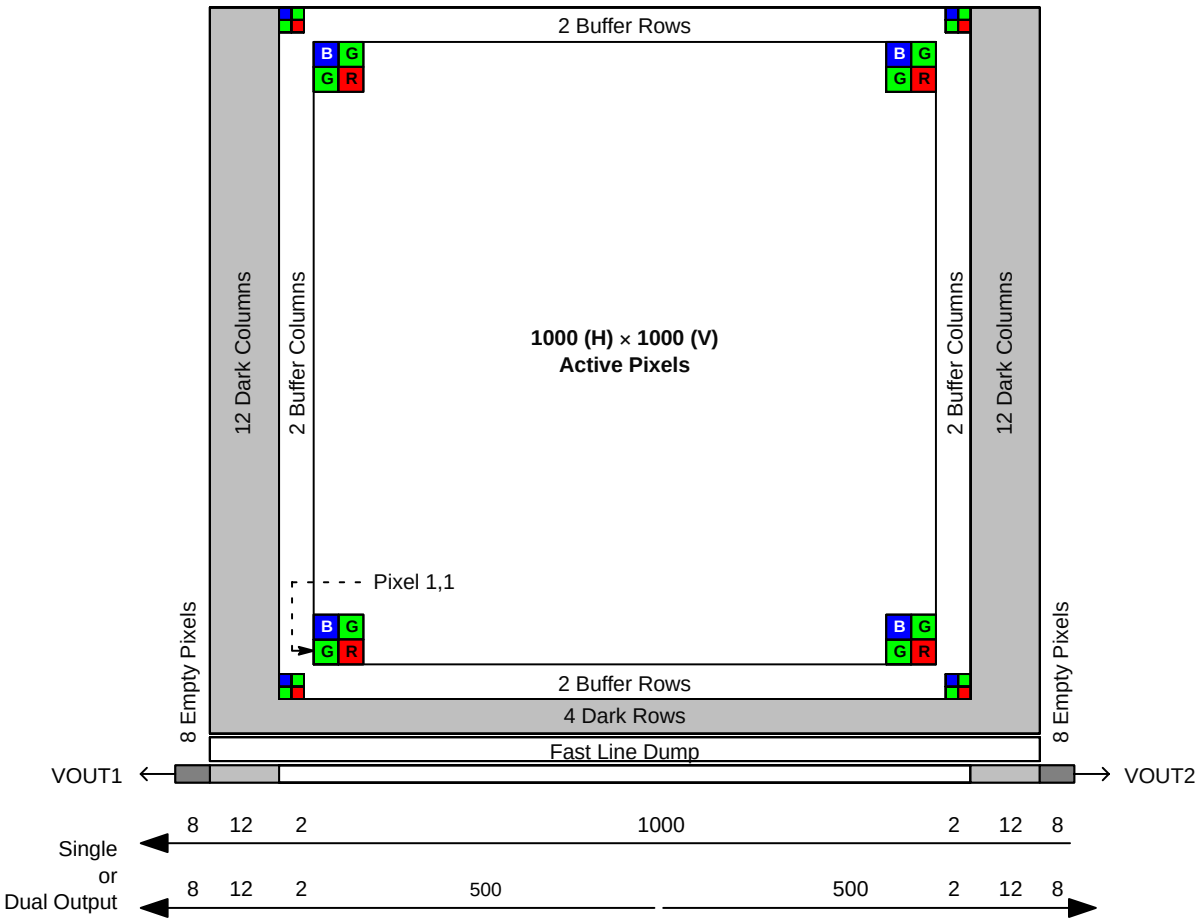


Figure 2. Block Diagram

There are 4 light shielded rows followed 1004 photoactive rows. The first 2 and the last 2 photoactive rows are buffer rows giving a total of 1000 lines of image data.

In the single output mode all pixels are clocked out of the Video 1 output in the lower left corner of the sensor. The first 8 empty pixels of each line do not receive charge from the vertical shift register. The next 12 pixels receive charge from the left light-shielded edge followed by 1004 photo-sensitive pixels and finally 12 more light shielded pixels from the right edge of the sensor. The first and last 2 photosensitive pixels are buffer pixels giving a total of 1000 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video 1 and the right half of the image is clocked out Video 2. Each row consists of 8 empty pixels followed by 12 light shielded pixels followed by 502 photosensitive pixels. When reconstructing the image, data from Video 2 will have to be reversed in a line buffer and appended to the Video 1 data.

Physical Description

Pin Description and Device Orientation

Pin Grid Array

When viewed from the top with the pin 1 index to the upper left, the center of the photoactive pixel array is offset 0.006″ above the physical center of the package. The pin 1 index is located in the corner of the package above pins L2 and K1. When operated in single output mode the first pixel out of the sensor will be in the corner closest to VOUT1B (pin L9). The HCCD is parallel to the row of pins A10 to L10. In the pictures below, the VCCD transfers charge down.

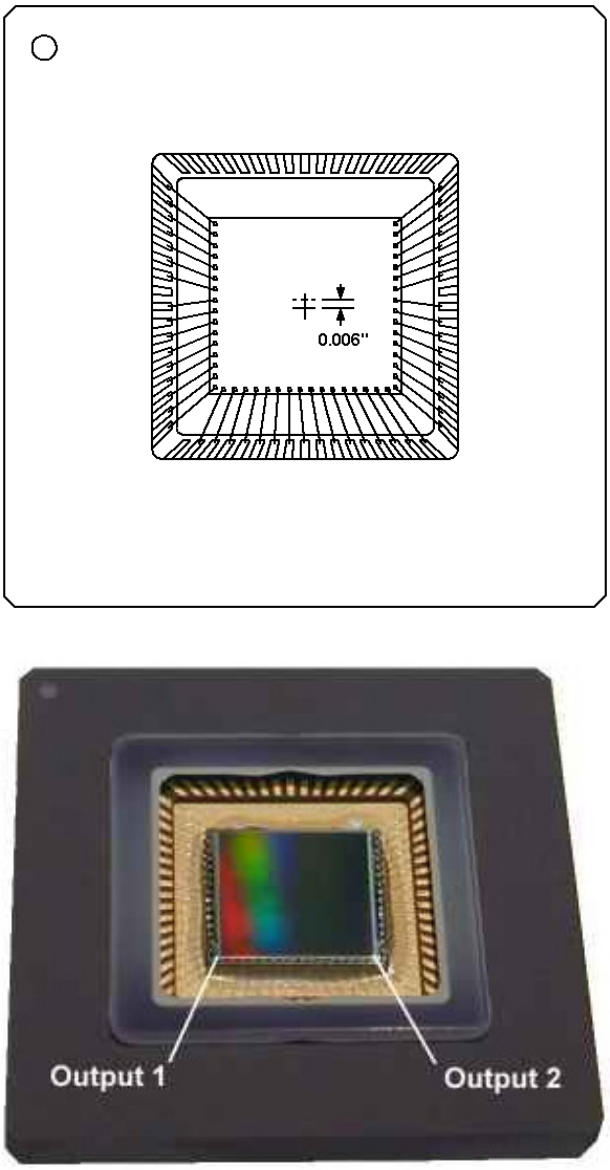


Figure 3. Pin 1 Location

Pin Grid Array Pin Description

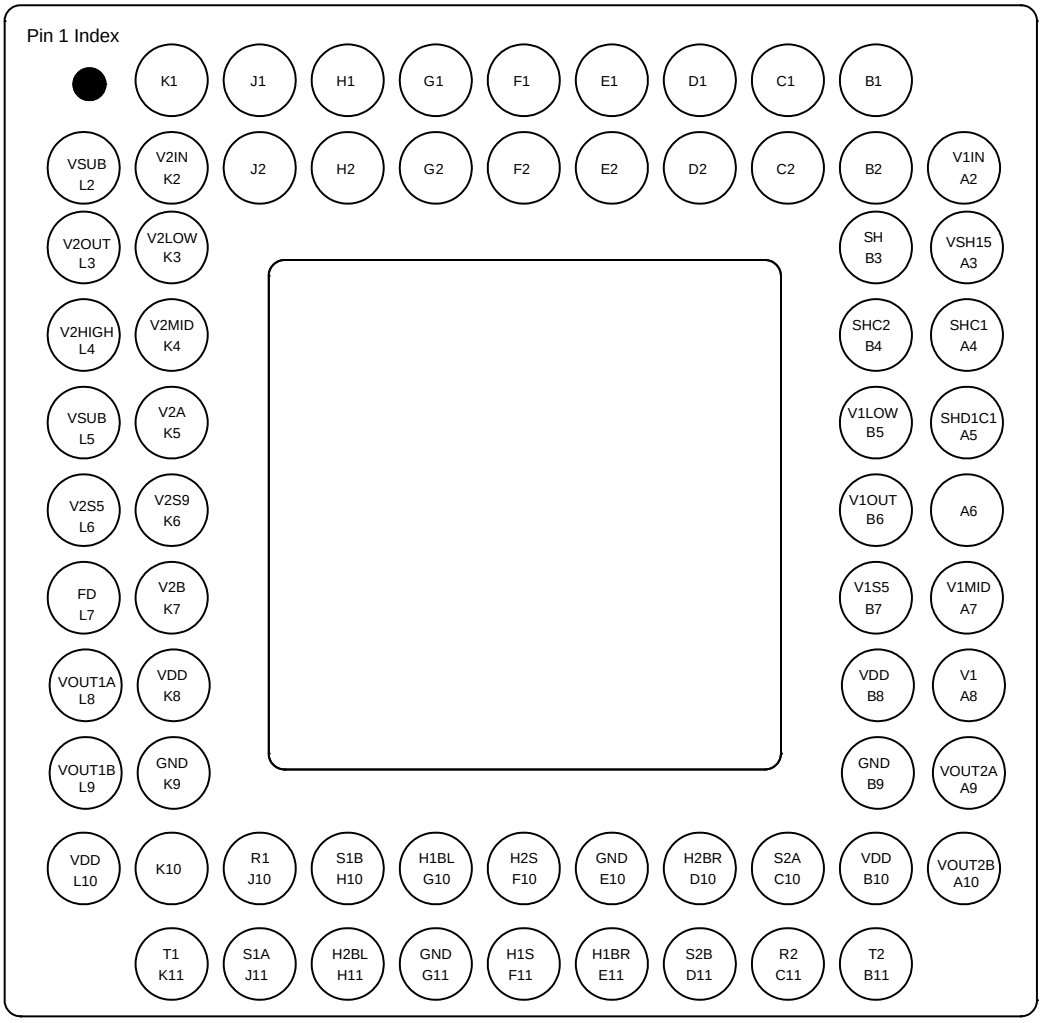


Figure 4. PGA Package Pin Description (Top View)

Table 4. PIN DESCRIPTION

Pin	Label	Function
K2	V2IN	VCCD Gate Phase 2 Input
L2	VSUB	Substrate Voltage Input
K3	V2LOW	VCCD Phase 2 Clock Driver Low
L3	V2OUT	VCCD Phase 2 Clock Driver Output
K4	V2MID	VCCD Phase 2 Clock Driver Mid
L4	V2HIGH	VCCD Phase 2 Clock Driver High
K5	ϕV2A	VCCD Phase 2 Clock Driver Input A
L5	VSUB	Substrate Voltage Input
K6	V2S9	VCCD Phase 2 Clock Driver +9 V
L6	V2S5	VCCD Phase 2 Clock Driver +5 V Fast Dump Clock Driver +5 V
K7	ϕV2B	VCCD Phase 2 Clock Driver Input B
L7	ϕFD	Fast Dump Clock Driver Input

Table 4. PIN DESCRIPTION (continued)

Pin	Label	Function
K8	VDD1	Video 1 CDS +15 V
L8	VOUT1A	Video 1 CDS Output A
K9	GND	Ground (0 V)
L9	VOUT1B	Video 1 CDS Output B
L10	VDD1	Video 1 CDS +15 V Supply
K11	ϕT1	Video 1 CDS Transfer Clock Input
J10	ϕR1	Video 1 CDS Reset Clock Input
J11	ϕS1A	Video 1 CDS Sample A Clock Input
H10	ϕS1B	Video 1 CDS Sample B Clock Input
H11	ϕH2BL	HCCD Left Phase 2 Barrier Clock Input
G10	ϕH1BL	HCCD Left Phase 1 Barrier Clock Input
G11	GND	Ground (0 V)
F10	ϕH2S	HCCD Storage Phase 2 Clock Input
F11	ϕH1S	HCCD Storage Phase 1 Clock Input
E10	GND	Ground (0 V)
E11	ϕH1BR	HCCD Right Phase 1 Barrier Clock Input
D10	ϕH2BR	HCCD Right Phase 2 Barrier Clock Input
D11	ϕS2B	Video 2 CDS Sample B Clock Input
C10	ϕS2A	Video 2 CDS Sample A Clock Input
C11	ϕR2	Video 2 CDS Reset Clock Input
B11	ϕT2	Video 2 CDS Transfer Clock Input
B10	VDD2	Video 2 CDS +15 V
A10	VOUT2B	Video 2 CDS Output B
B9	GND	Ground (0 V)
A9	VOUT2A	Video 2 CDS Output A
B8	VDD2	Video 2 CDS +15 V
A8	ϕV1	VCCD Phase 1 Clock Driver Input
B7	V1S5	VCCD Phase 1 Clock Driver +5 V
A7	V1MID	VCCD Phase 1 Clock Driver Mid
B6	V1OUT	VCCD Phase 1 Clock Driver Output
B5	V1LOW	VCCD Phase 1 Clock Driver Low
A5	SHD1C1	Shutter Driver Connection
B4	SHC2	Shutter Driver Connection
A4	SHC1	Shutter Driver Connection
B3	ϕSH	Shutter Driver Clock Input
A3	VSH15	Shutter Driver +15 V
A2	V1IN	VCCD Gate Phase 1 Input

1. All pins not listed must be unconnected.

Leadless Chip Carrier

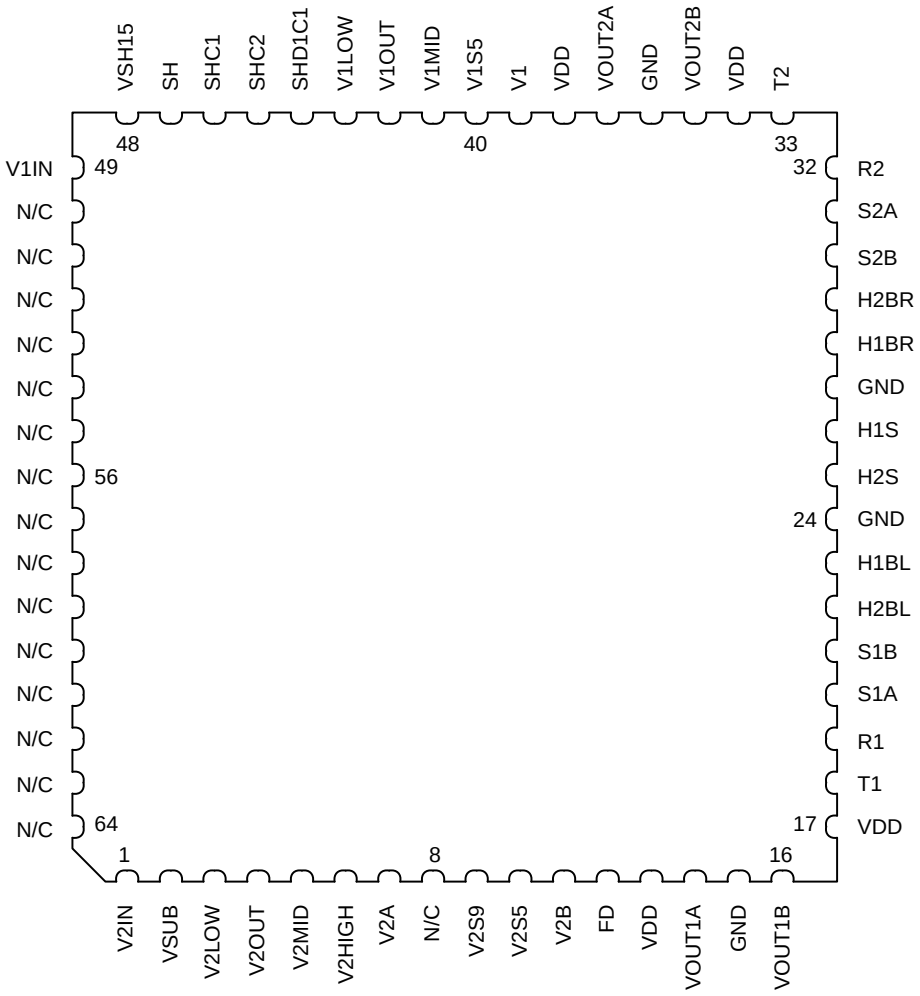


Figure 5. LCC Package Pin Description (Top View)

Table 5. PIN DESCRIPTION

Pin	Label	Function
1	V2IN	VCCD Gate Phase 2 Input
2	VSUB	Substrate Voltage Input
3	V2LOW	VCCD Phase 2 Clock Driver Low
4	V2OUT	VCCD Phase 2 Clock Driver Output
5	V2MID	VCCD Phase 2 Clock Driver Mid
6	V2HIGH	VCCD Phase 2 Clock Driver High
7	V2A	VCCD Phase 2 Clock Driver Input A
8	N/C	No Connect
9	V2S9	VCCD Phase 2 Clock Driver +9 V
10	V2S5	VCCD Phase 2 Clock Driver +5 V Fast Dump Clock Driver +5 V
11	V2B	VCCD Phase 2 Clock Driver Input B
12	FD	Fast Dump Clock Driver Input

Table 5. PIN DESCRIPTION (continued)

Pin	Label	Function
13	VDD	Video CDS +15 V
14	VOUT1A	Video 1 CDS Output A
15	GND	Ground (0 V)
16	VOUT1B	Video 1 CDS Output B
17	VDD	Video CDS +15 V
18	T1	Video 1 CDS Transfer Clock Input
19	R1	Video 1 CDS Reset Clock Input
20	S1A	Video 1 CDS Sample A Clock Input
21	S1B	Video 1 CDS Sample B Clock Input
22	H2BL	HCCD Left Phase 2 Barrier Clock Input
23	H1BL	HCCD Left Phase 1 Barrier Clock Input
24	GND	Ground (0 V)
25	H2S	HCCD Storage Phase 2 Clock Input
26	H1S	HCCD Storage Phase 1 Clock Input
27	GND	Ground (0 V)
28	H1BR	HCCD Right Phase 1 Barrier Clock Input
29	H2BR	HCCD Right Phase 2 Barrier Clock Input
30	S2B	Video 2 CDS Sample B Clock Input
31	S2A	Video 2 CDS Sample A Clock Input
32	R2	Video 2 CDS Reset Clock Input
33	T2	Video 2 CDS Transfer Clock Input
34	VDD	Video CDS +15 V
35	VOUT2B	Video 2 CDS Output B
36	GND	Ground (0 V)
37	VOUT2A	Video 2 CDS Output A
38	VDD	Video CDS +15 V
39	V1	VCCD Phase 1 Clock Driver Input
40	V1S5	VCCD Phase 1 Clock Driver +5 V
41	V1MID	VCCD Phase 1 Clock Driver Mid
42	V1OUT	VCCD Phase 1 Clock Driver Output
43	V1LOW	VCCD Phase 1 Clock Driver Low
44	SHD1C1	Shutter Driver Connection
45	SHC2	Shutter Driver Connection
46	SHC1	Shutter Driver Connection
47	SH	Shutter Driver Clock Input
48	VSH15	Shutter Driver +15 V
49	V1IN	VCCD Gate Phase 1 Input
50−64	N/C	No Connect

IMAGING PERFORMANCE

Table 6. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Sampling Plan*
OPTICAL SPECIFICATION							
Peak Quantum Efficiency	QE_{MAX}	42	45	−	%	1	Design
Peak Quantum Efficiency Wavelength	λQE	−	490	−	nm	1	Design
Microlens Acceptance Angle (Horizontal)	ΘQE_H	±12	±13	−	Degrees	2	Design
Microlens Acceptance Angle (Vertical)	ΘQE_V	±25	±30	−	Degrees	2	Design
Quantum Efficiency at 540 nm	$QE_{(540)}$	38	40	−	%	1	Design
Photoresponse Non-Uniformity	PNU	−	5	−	%		Design
Maximum Photoresponse Non-Linearity	NL	−	2	−	%	3, 4, 18	Die
Maximum Gain Difference Between Outputs	ΔG	−	10	−	%	3, 4, 18	Die
Maximum Signal Error caused by Non-Linearity Differences	ΔNL	−	1	−	%	3, 4, 18	Die
Dark Center Uniformity		−	−	12	e^- rms	19, 20	Die
Dark Global Uniformity		−	−	2	mV pp	19, 20	Die
Global Uniformity		−	−	5	% rms	19, 20	Die
Global Peak to Peak Uniformity		−	−	15	% pp	19, 20	Die
Center Uniformity		−	−	0.7	% rms	19, 20	Die
CCD SPECIFICATIONS							
Vertical CCD Charge Capacity	V_{ne}	54	60	−	ke^-		Design
Horizontal CCD Charge Capacity	H_{ne}	110	120	−	ke^-		Design
Photodiode Charge Capacity	P_{ne}	38	42	−	ke^-	5	Die
Dark Current	I_D	−	0.2	0.5	nA/cm^2	6	Die
Image Lag	Lag	−	< 10	50	e^-	7	Design
Anti-Blooming Factor	X_{AB}	100	300	−		1, 8, 9, 10, 11	Design
Vertical Smear	Smr	−	−75	−72	dB	1, 8, 9	Design
CDS OUTPUT SPECIFICATION							
Power Dissipation	P_D	−	213	−	mW	12	Design
Bandwidth	F_{-3dB}	−	140	−	MHz	12	Design
Max Off−chip Load	C_L	−	10	−	pF	13	Design
Gain	A_V	−	0.70	−		12	Design
Sensitivity	ΔV/ΔN	−	13	−	$\mu V/e^-$	12	Design
Output Impedance	R	−	160	−	Ω	12	Design
Saturation Voltage	V_{SAT}	−	500	−	mV	5, 12	Die
Output Bias Current	I_{OUT}	−	3.0	−	mA		Design
GENERAL − MONOCHROME							
Total Camera Noise	n_{e-T}	−	42	−	e^- rms	6, 14	Design
Dynamic Range	DR	−	60	−	dB	15	Design
GENERAL − COLOR							
Total Camera Noise	n_{e-T}	−	50	−	e^- rms	6, 14	Design
Dynamic Range	DR	−	58	−	dB	15	Design

Table 6. SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Notes	Sampling Plan*
POWER							
Single Channel CDS		−	213	−	mW	12	
VCCD clock driver		−	71	−	mW	16	
Electronic shutter driver		−	1.1	−	mW		
HCCD		−	122	−	mW	16, 17	
Total Power		−	407	−	mW	12, 16	

*Sampling plan defined as “Die” indicates that every device is verified against the specified performance limits. Sampling plan defined as “Design” indicates a sampled test or characterization, at the discretion of ON Semiconductor, against the specified performance limits.

1. Measured with F/4 imaging optics.
2. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QE_{MAX} at a wavelength of λQE. Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (ΘQE_H) or in a plane parallel to the vertical axis (ΘQE_V).
3. Value is over the range of 10% to 90% of photodiode saturation.
4. Value is for the sensor operated without binning.
5. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the anti-blooming specification. Substrate voltage will be specified with each part for 42 ke^-.
6. Measured at 40°C, 40 MHz HCCD frequency.
7. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame’s average pixel output in the dark.
8. Measured with a spot size of 100 vertical pixels, no electronic shutter.
9. Measured with green light (500 nm to 580 nm).
10. A blooming condition is defined as when the spot size doubles in size.
11. Anti-blooming factor is the light intensity which causes blooming divided by the light intensity which first saturates the photodiodes.
12. Single output power, 3 mA load.
13. With total output load capacitance of C_L= 10 pF between the outputs and AC ground.
14. Includes system electronics noise, dark pattern noise and dark current shot noise at 40 MHz. Total noise measured on the KAI−1020 evaluation board.
15. Uses 20LOG (P_{ne} / n_{e-T})
16. At 30 frames/sec, single output.
17. This includes the power of the external HCCD clock driver.
18. For the sampling plan, measured at 10 MHz
19. Tested at 27°C and 40°C
20. See Tests

TYPICAL PERFORMANCE CURVES

Monochrome Quantum Efficiency

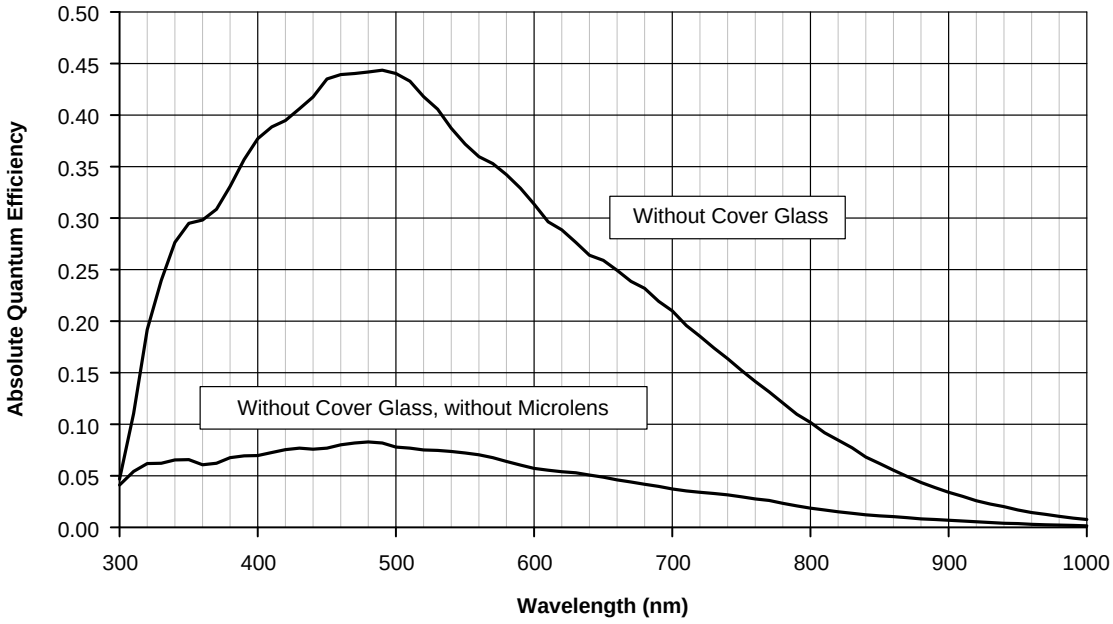


Figure 6. Monochrome Quantum Efficiency

Color (Bayer RGB) Quantum Efficiency

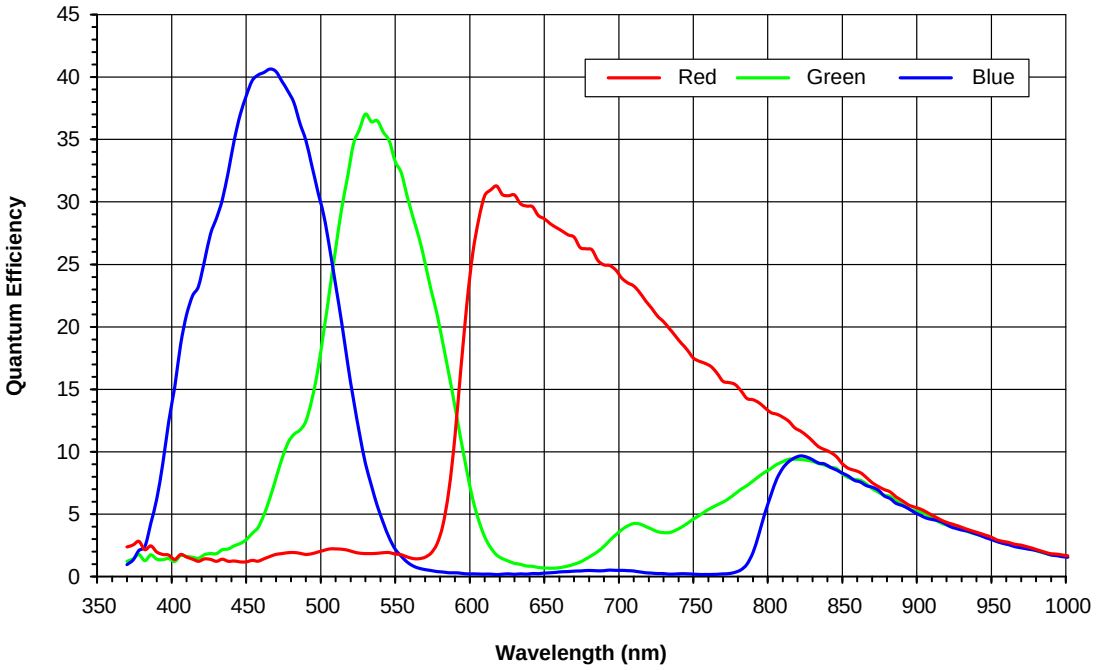


Figure 7. Color (Bayer RGB) Quantum Efficiency

Photoresponse vs. Angle

The horizontal curve is where the incident light angle is varied in a plane parallel to the HCCD.
The vertical curve is where the incident light angle is varied in a plane perpendicular to the HCCD.

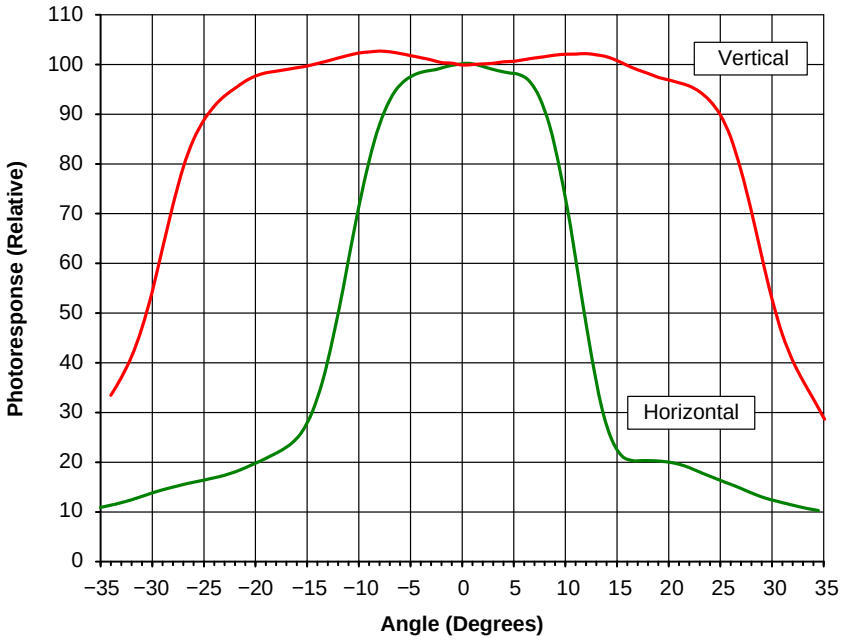


Figure 8. Photoresponse vs. Angle

Sensor Power

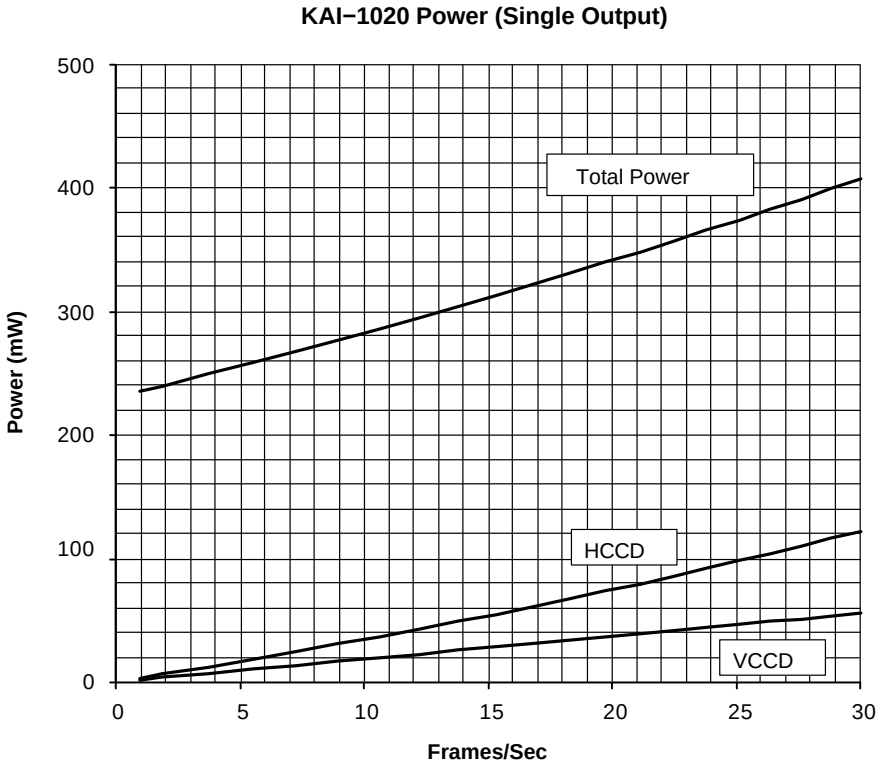


Figure 9. Power

Frame Rate

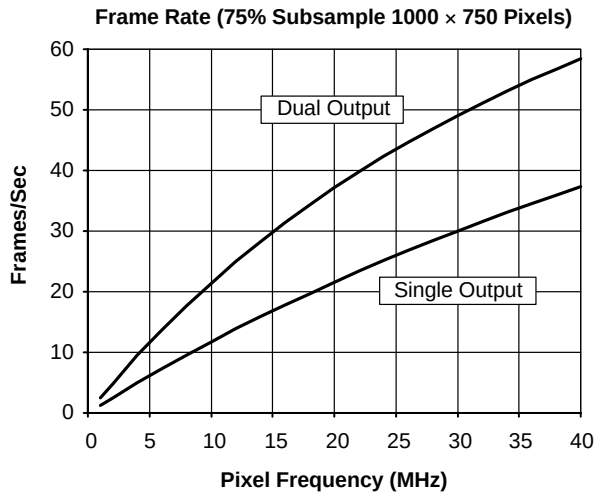


Figure 10. Frame Rate 1000 × 750 Pixels

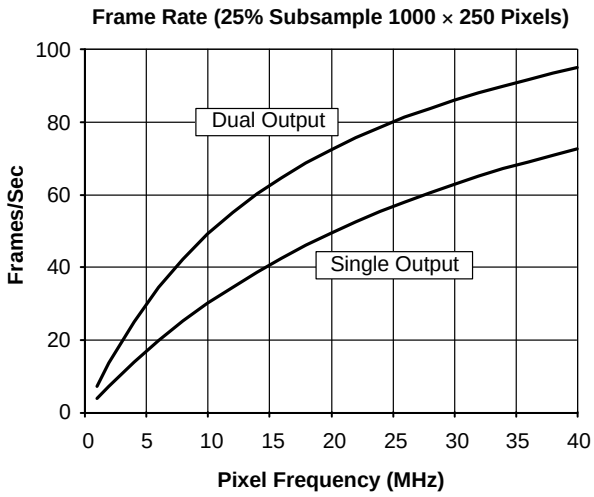


Figure 11. Frame Rate 1000 × 250 Pixels

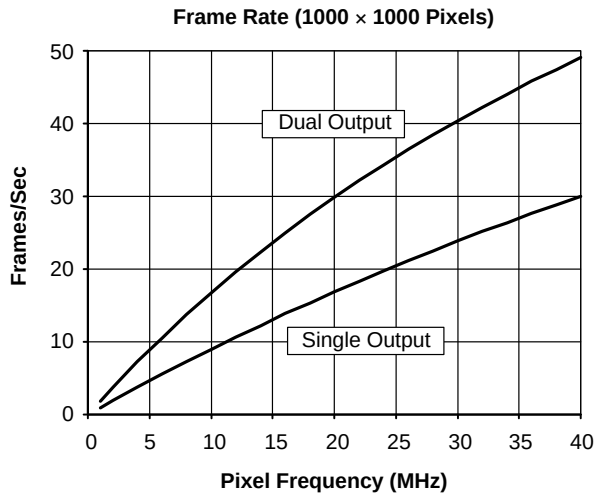


Figure 12. Frame Rate 1000 × 1000 Pixels

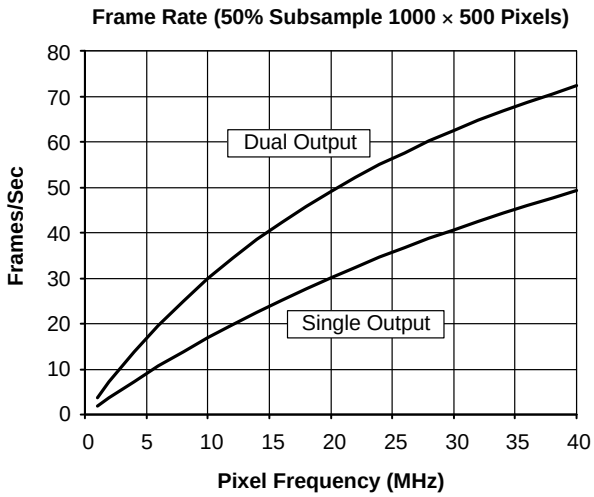


Figure 13. Frame Rate 1000 × 500 Pixels

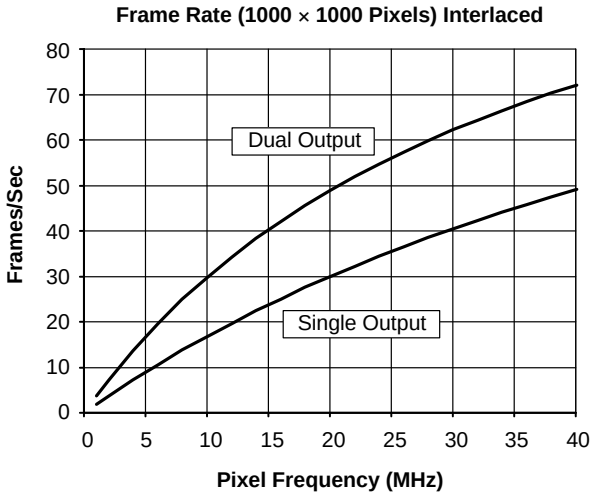


Figure 14. Frame Rate 1000 × 1000 Pixels Interlaced

DEFECT DEFINITIONS

Table 7. SPECIFICATIONS

Name	Definition	Maximum	Temperature(s) Tested at (°C)	Notes	Sampling Plan
Dark Field Major Bright Defective Pixel	Defect ≥ 28 mV	10	27, 40	1	Die
Bright Field Major Dark or Bright Defective Pixel	Defect ≥ 11%	10	27, 40		Die
Bright Field Minor Dark Defective Pixel	Defect ≥ 5%	20 in Zone 2	27, 40	8	Die
Dark Field Minor Bright Defective Pixel	Defect ≥ 14 mV	100	27, 40	2	Die
Bright Field Dead Dark Pixel	Defect ≥ 40%	0	27, 40	5	Die
Bright Field Nearly Dead Dark Pixel	Defect ≥ 20%	0 in Zone 1 1 in Zone 2	27, 40	5, 8	Die
Dark Field Saturated Bright Pixel	Defect ≥ 106 mV	0	27, 40	3	Die
Dark Field Minor Cluster Defect	A Group of 2 to 10 Contiguous Dark Field Minor Defective Pixels	0	27, 40	4	Die
Bright Field Minor Cluster Defect	A Group of 2 to 10 Contiguous Bright Field Minor Defective Pixels	2 in Zone 2	27, 40	4, 8	Die
Major Cluster Defect	A Group of 2 to 10 Contiguous Major Defective Pixels	0	27, 40	4	Die
Column Defect	A Group of More than 10 Contiguous Major Defective Pixels along a Single Column	0	27, 40		Die
Column Average Magnitude	Within ±0.4% of Regional Average (5 Columns)	0	27, 40	6, 7	Die

1. The defect threshold was determined by using a threshold of 8 mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 ms. [8 mV · (117 ms / 33 ms) = 28 mV]
2. The defect threshold was determined by using a threshold of 4mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 ms. [4 mV · (117 ms / 33 ms) = 14 mV]
3. The defect threshold was determined by using a threshold of 30 mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 ms. [30 mV · (117 ms / 33 ms) = 106 mV]
4. The maximum width of any cluster defect is 2 pixels.
5. Only dark defects.
6. Local average is centered on column.
7. See Test Regions of Interest for region used.
8. See Figure 18 for zone 1 and 2 definitions.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are referenced to pixel 1, 1 in the defect map (see Figure 16: Regions of Interest).

TEST DEFINITIONS

Table 8. TEST CONDITIONS

Name	Definition	Notes
Frame Time	117 ms	1
Horizontal Clock Frequency	10 MHz	
Light source (LED)	Continuous Green Illumination Centered at 530 nm	2
Operation	Nominal Operating Voltages and Timing	

1. Electronic shutter is not used. Integration time equals frame time.
2. Green LED used: Nichia NSPG500S.

Test System Conversion Factors

KAI−1020 Output Sensitivity: 13 μV per e^-

Test System Gain (Measured): 0.25 mV per ADU

Test System Gain (Calculated): 19 e^- per ADU

Tests

Dark Field Center Uniformity

This test is performed under dark field conditions. Only the center 100 by 100 pixels of the sensor are used for this test (pixels 431, 431 to pixel 530, 530). See Figure 17.

$$\text{Dark Field Center Uniformity} = \text{Standard Deviation of Center 100 by 100 Pixels in Electrons} \cdot \left(\frac{\text{DPS Integration Time}}{\text{Actual Integration Time Used}}\right)$$

Units: mV rms. DPS Integration Time: Device Performance Specification Integration Time = 33 ms.

Dark Field Global Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15. The average signal level of each of the 100 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in ADU} - \text{Horizontal Overclock Average in ADU}) \cdot \text{mV per Count}$$

Units : mVpp (millivolts Peak to Peak)

Where i = 1 to 100. During this calculation on the 100 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Global Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. Global uniformity is defined as:

$$\text{Global Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}}\right)$$

Units : % rms

Active Area Signal = Active Area Average − H. Overclock Average

Global Peak to Peak Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15. The average signal level of each of the 100 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in ADU} - \text{Horizontal Overclock Average in ADU}) \cdot \text{mV per Count}$$

Where i = 1 to 100. During this calculation on the 100 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = \frac{\text{Maximum Signal} - \text{Minimum Signal}}{\text{Active Area Signal}}$$

Units : % pp

Center Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. Defects are

excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Test Regions of Interest and Figure 17) of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 \cdot \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}}\right)$$

Units : % rms

Center ROI Signal = Center ROI Average − H. Overclock Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size (see Figure 15). In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified.

Bright Field Defect Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 15: Test Sub Regions of Interest. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 365 mV.
- Dark defect threshold: 365 mV · 11% = 40 mV
- Bright defect threshold: 365 mV · 11% = 40 mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 100,100.
  - Median of this region of interest is found to be 366 mV.
  - Any pixel in this region of interest that is ≥ (366 + 40 mV) 406 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is ≤ (366 − 40 mV) 324 mV in intensity will be marked defective.
- All remaining 99 sub regions of interest are analyzed for defective pixels in the same manner.

Bright Field Minor Defect Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. The average signal level of all active pixels is found. The dark threshold is set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 2500 sub regions of interest, each of which is 20 by 20 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for bright field minor defective pixels:

- Average value of all active pixels is found to be 365 mV.
- Dark defect threshold: 365 mV · 5% = 18 mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 20, 20.
  - Median of this region of interest is found to be 366 mV.
  - Any pixel in this region of interest that is ≤ (366 − 18 mV) 348 mV in intensity will be marked defective.
- All remaining 2499 sub regions of interest are analyzed for defective pixels in the same manner.

Bright Field Column Average Magnitude Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. A column is marked as defective if

$$100 \cdot \text{Abs}\left(\frac{\text{Avg(Column n)} - \text{Avg(Avg(Column x))}}{\text{Avg(Avg(Column x))}}\right) > 0.4$$

Where x = n−2 to n+2

Table 9. TEST REGIONS OF INTEREST

Name	Definition
Number of Pixels	1027 (H) × 1008 (V)
Number of Photo Sensitive Pixels	1004 (H) × 1004 (V)
Number of Active Pixels	1000 (H) × 1000 (V)
Active Area ROI	Pixel (1, 1) to Pixel (1000, 1000)
Column Magnitude Test ROI	Pixel (11, 11) to Pixel (990, 990)

1. Only the active pixels are used for performance and defect tests. See Figure 16.

Test Sub Regions of Interest

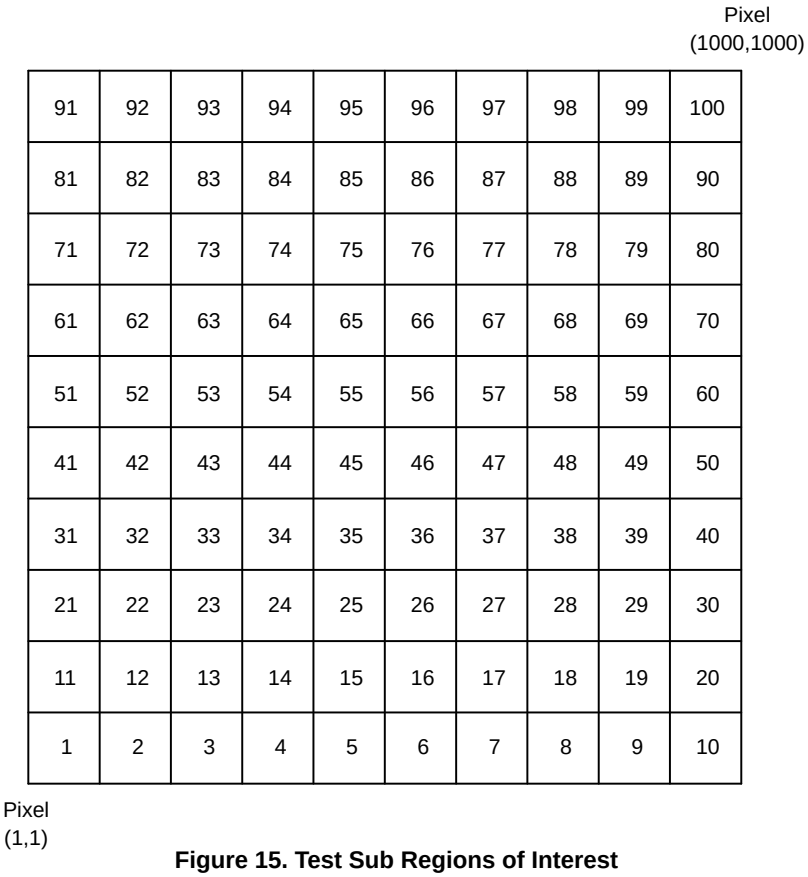


Figure 15. Test Sub Regions of Interest

Signal Level Calculation

Signal levels are calculated by using the average of the region of interest under test and subtracting off the horizontal overclock region. The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 16 for a pictorial representation of the regions.

Example: To determine the active area average in millivolts, the following calculation used:

$$\text{Active Area Signal (mV)} = (\text{Active Area Average} - \text{Horizontal Overclock Average}) \cdot \text{mV per Count}$$

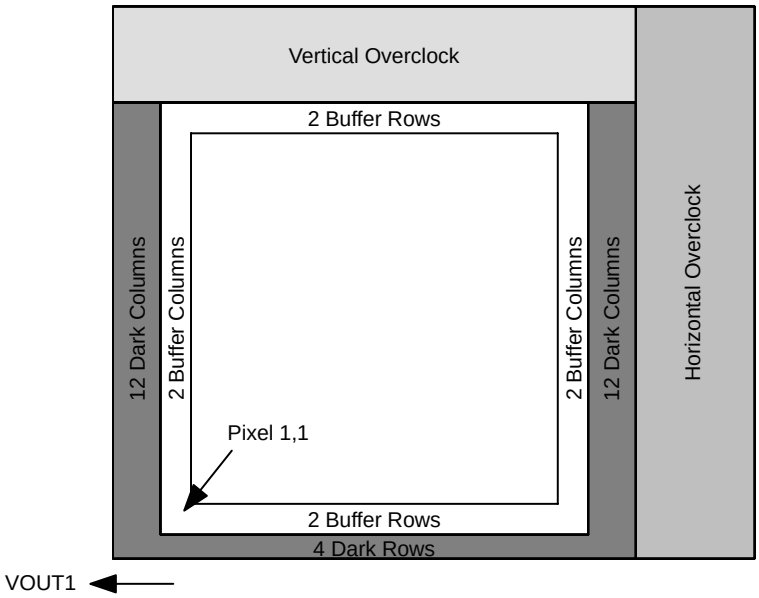


Figure 16. Regions of Interest

Center Region of Interest

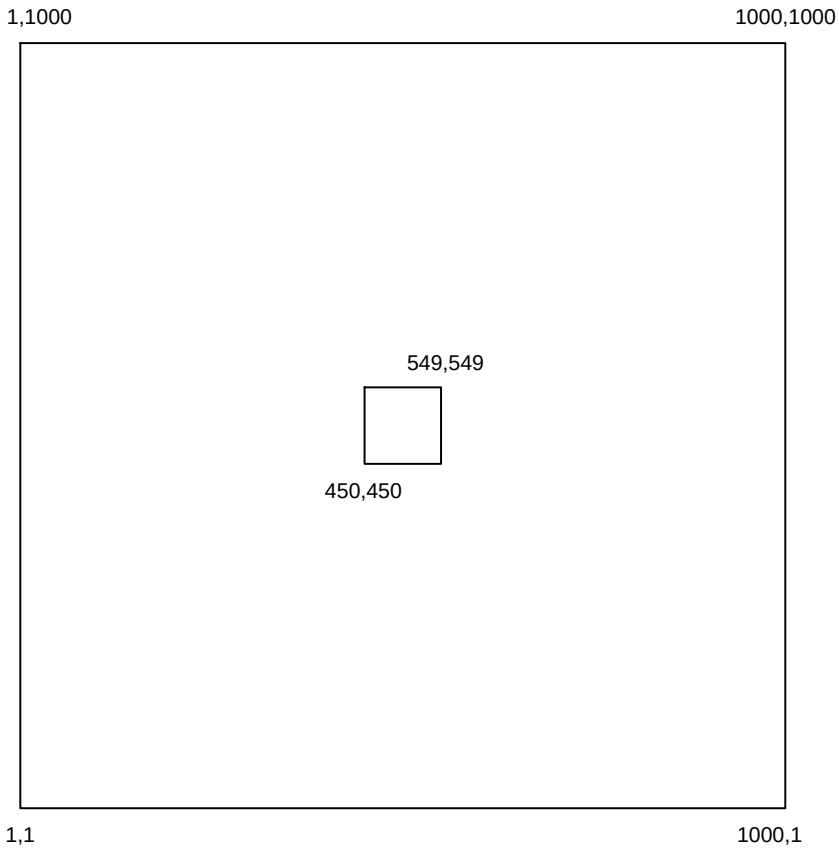


Figure 17. Center Region of Interest

Zones 1 and 2
Zone 2 includes zone 1

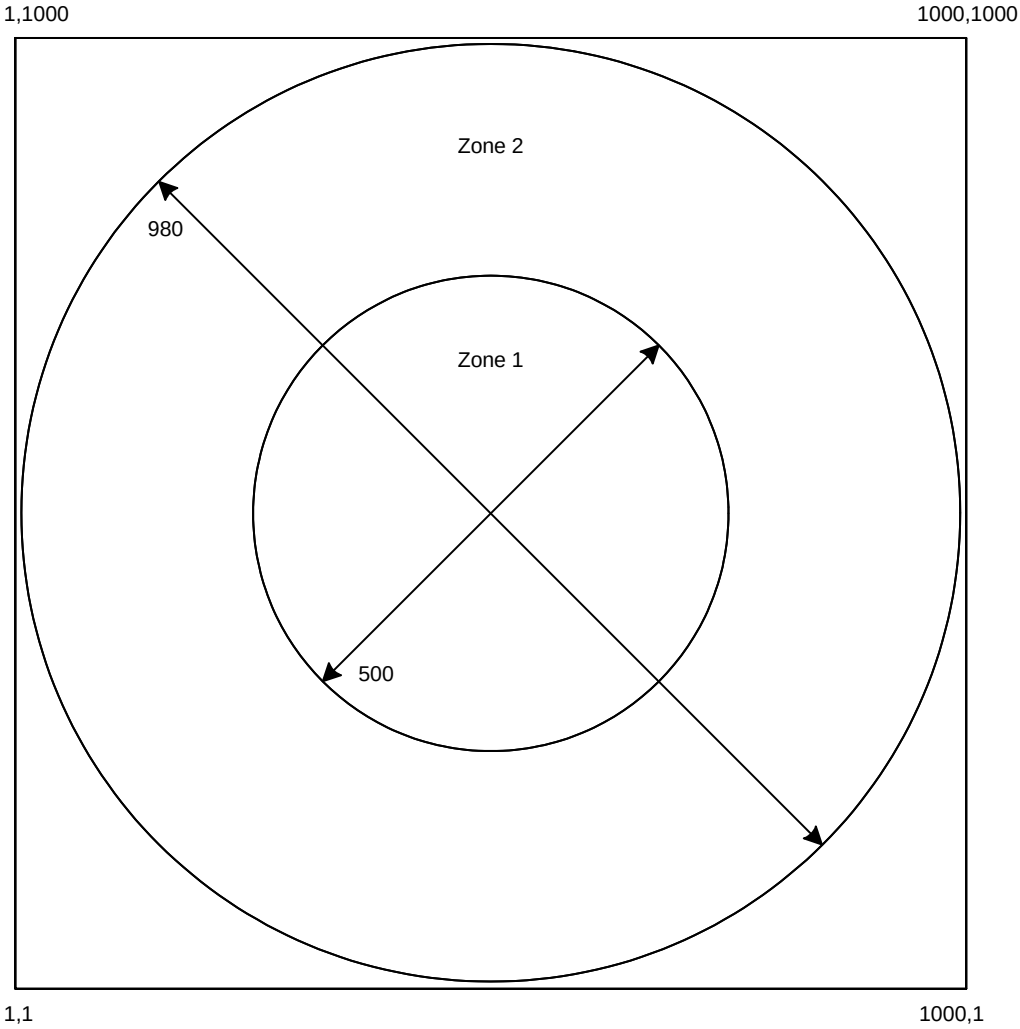


Figure 18. Zones 1 and 2

OPERATION

Single or Dual Output

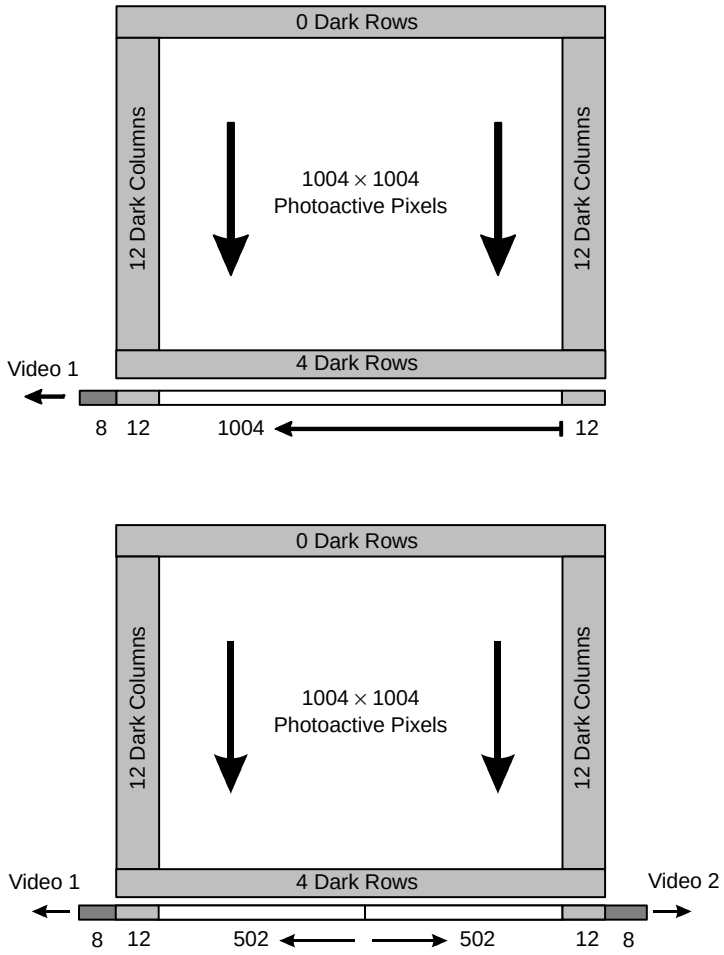


Figure 19. Single or Dual Output Mode of Operation

The KAI−1020 is designed to read the image out of one output at 30 frames/second or two outputs at 48 frames/second. In the dual output mode the right half of the horizontal shift register reverses its direction of charge transfer. The left half of the image is read out of video 1 and the right half of the image is read out of video 2.

There are no dark reference rows at the top and 4 dark rows at the bottom of the image sensor. The 4 dark rows should not be used for a dark reference level. The dark rows will contain smear signal from bright light sources. Use the 12 dark columns on the left or right side of the image sensor as a dark reference.

The KAI−1020 Pixel

The pixel is 7.4 μm square. It consists of a light sensitive photodiode and an optically shielded vertical shift register. The vertical shift register is a charge-coupled device (VCCD). Each pixel is covered by a microlens to increase the light gathering efficiency of the photodiode.

Under normal operation, the image capture process begins with a 4 μs long pulse on the electronic shutter trigger input ϕSH. The electronic shutter empties all charge from every photodiode in the pixel array.

The photodiodes start collecting light on the falling edge of the ϕSH pulse. For each photon that is incident upon the 7.4 μm square area of the pixel, the probability of an electron being generated in the photodiode is given by the quantum efficiency (QE). At the end of the desired integration time, a 10 μs pulse on ϕV2B transfers the charge (electrons) collected in the photodiode into the VCCD. The integration time ends on the falling edge of ϕV2B.

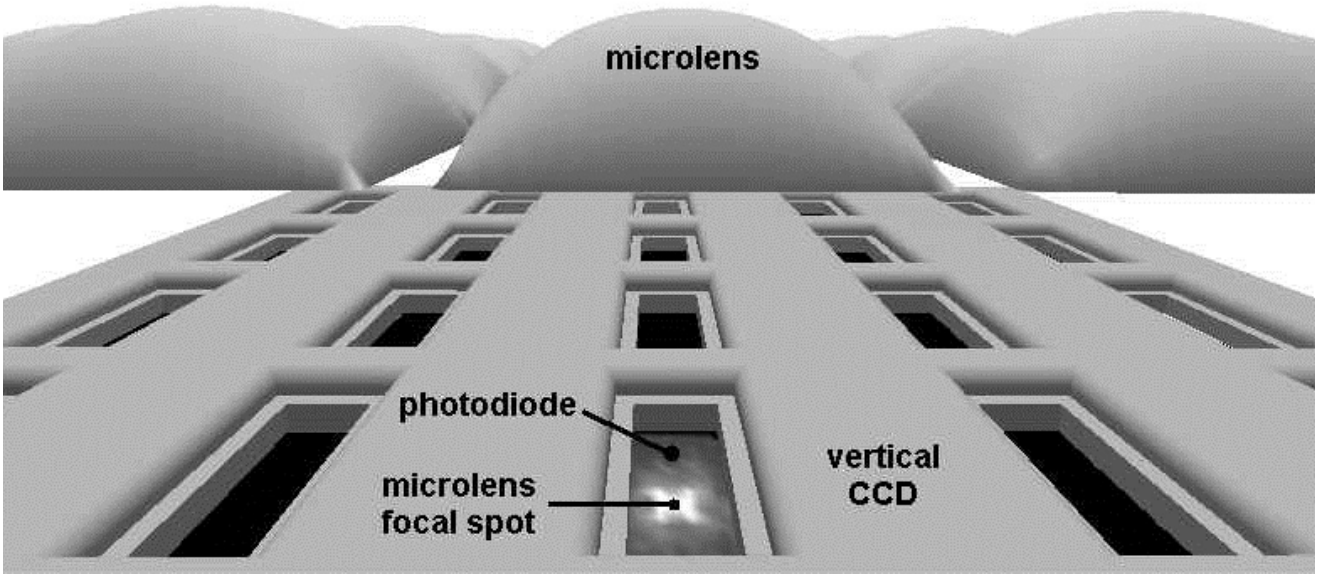


Figure 20. Pixel

High Level Block Diagram

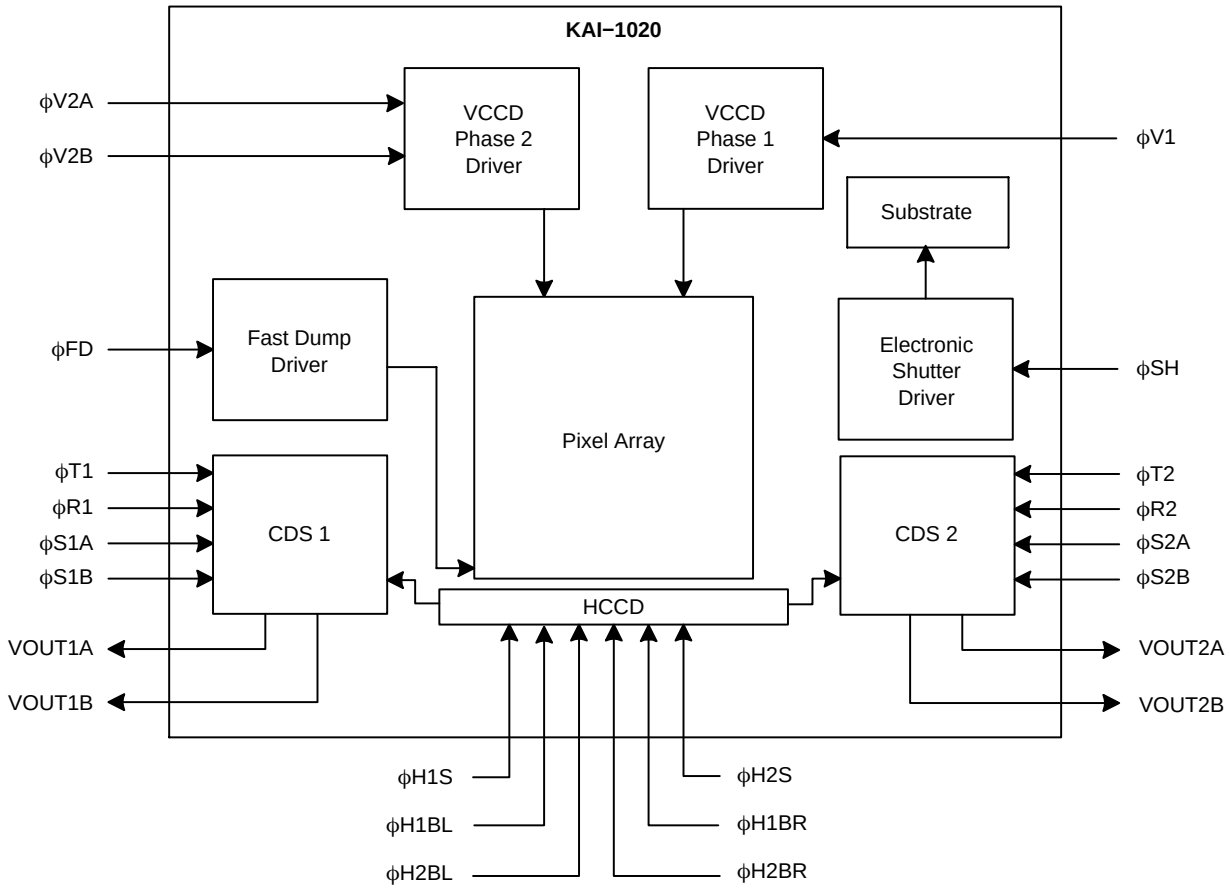


Figure 21. High Level Block Diagram

All timing inputs are driven by 5 V logic. The image sensor has integrated clock drivers to generate the proper voltages for the internal CCD gates. There are two VCCD clock drivers. Both the phase 1 and phase 2 VCCD drivers control the shifting of charge through the VCCD. The phase 2 driver also controls the transfer of charge from the photodiodes to the VCCD.

There is an integrated fast dump driver, which allows an entire row of pixels to be quickly discarded without clocking the row through the HCCD.

An integrated electronic shutter driver generates a > 30 V pulse on the substrate to simultaneously empty every photodiode on the image sensor.

Each of the two outputs has a correlated double sampling circuit to simplify the analog signal processing in the camera. The horizontal clock timing selects which outputs are active.

Main Timing

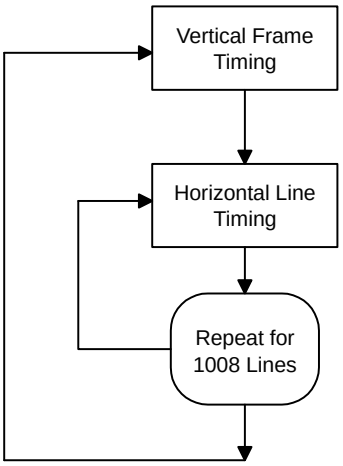


Figure 22. Timing Flow Chart

Vertical Frame Timing

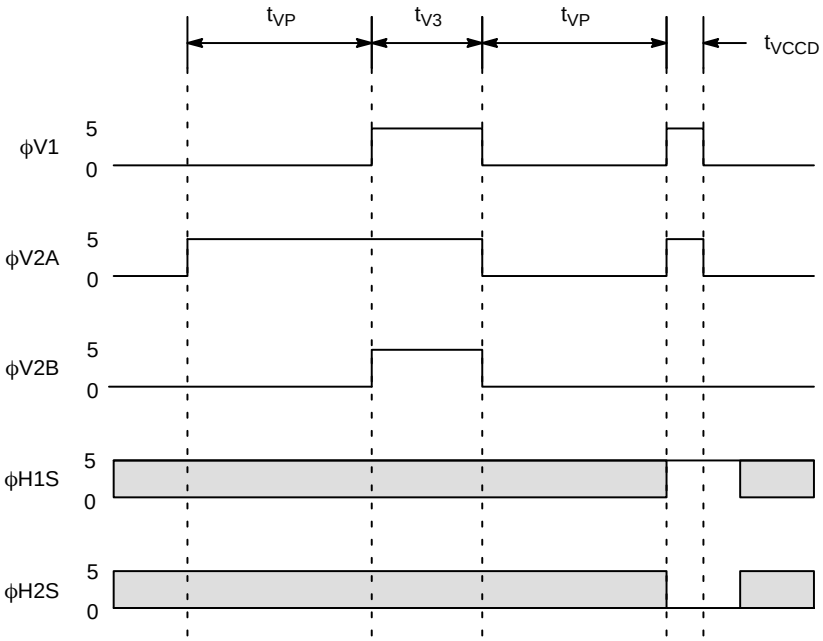


Figure 23. Vertical Frame Timing

The vertical frame timing may begin once the last pixel of the image sensor has been read out of the HCCD. The beginning of the vertical frame timing is at the rising edge of ϕV2A. After the rising edge of ϕV2A there must be a delay of t_{VP} µs before a pulse of t_{V3} µs on ϕV2B and ϕV1. The charge is transferred from the photodiodes to the VCCD during the time t_{V3}. The falling edge of ϕV2B marks the end of the photodiode integration time. After the pulse on ϕV2B the ϕV1 and ϕV2A should remain idle for t_{VP} µs before the horizontal line timing period begins. This allows the clock and well voltages time to settle for efficient charge transfer in the VCCD.

All HCCD and CDS timing inputs should run continuously through the vertical frame timing period. For an extremely short integration time, it is allowed to place an electronic shutter pulse on ϕSH at any time during the vertical frame timing. The ϕSH and ϕV2B pulses may be overlapped. The integration time will be from the falling edge of ϕSH to the falling edge of ϕV2B.

Horizontal Line Timing

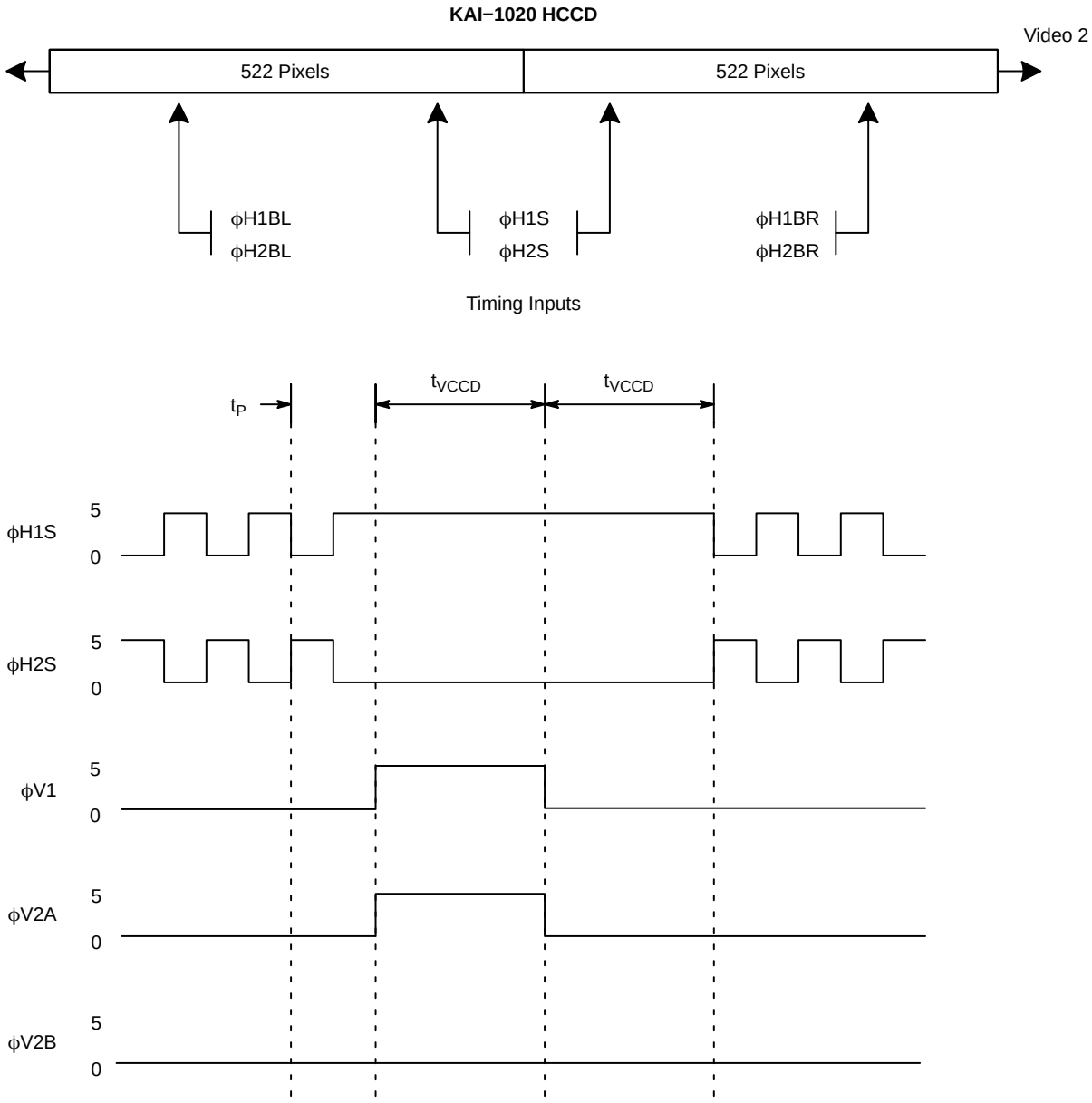


Figure 24. Horizontal Line Timing

When the ϕV2A and ϕV1 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. ϕH1S must be stopped in the high state and ϕH2S must be stopped in the low state. The HCCD clocking may begin t_{VCCD} μs after the falling edge of the ϕV2A and ϕV1 pulse. The timing inputs to the CDS should run continuously through the horizontal line timing.

The HCCD has a total of 1036 pixels. The 1028 vertical shift registers (columns) are shifted into the center 1028 pixels of the HCCD. There are 8 pixels at both ends of the HCCD which receive no charge from a vertical shift register. The first 8 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 1004 clock cycles will contain photo-electrons (image data). Finally, the last 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 12 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 10 columns of the 12 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter driver (ϕSH), VCCD driver

(ϕV2A, ϕV2B, ϕV1), and fast dump drivers (ϕFD) should be held at the low level. This prevents unwanted noise from being introduced into the CDS circuit.

The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video 1 output CDS, or to the video 2 output CDS (left/right image reversal). The HCCD is split into two equal halves of 522 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the ϕH1BL, ϕH2BL, ϕH1BR, and ϕH2BR timing inputs.

Single Output

To direct all pixels to the video 1 output make the following HCCD connections:

ϕH1S = ϕH1BL, ϕH2BR

ϕH2S = ϕfH2BL, ϕH1BR

To direct all pixels to the video 2 output make the following HCCD connections:

ϕH1S = ϕH2BL, ϕH1BR

ϕH2S =ϕfH1BL, ϕH2BR

In each case the first 8 pixels will contain no electrons, followed by 12 dark reference pixels containing only electrons generated by dark current, followed by 1004 photo-active pixels, followed by 12 dark reference pixels. The HCCD must be clocked for at least 1028 cycles. The VCCD may be clocked immediately after the 1028th HCCD clock cycle.

If the sensor is to be permanently operated in single output mode through video 1, then VDD2 (pins B8, and B10) may be connected to GND. This disables the video 2 CDS and lowers the power consumption.

If the sensor is to be permanently operated in single output mode through video 2, then VDD1 and VDD2 supplies must be +15 V. The VDD1 supplies must always be at +15 V for the sensor to operate properly.

Dual Output

To use both outputs for faster image readout, make the following HCCD connections:

ϕH1S = ϕH1BL, ϕH1BR

ϕH2S = ϕH2BL, ϕH2BR

For both outputs the first 8 HCCD clock cycles contain no electrons, followed by 12 dark reference pixels containing only dark current electrons, followed by 502 photo-active pixels. This adds up to 522 pixels, but the HCCD should be clocked for at least 523 cycles before the next VCCD line shift takes place. The extra HCCD clock cycle ensures that the signal from the last pixel exits the CDS circuit before the VCCD drivers switch the gate voltages. This extra cycle is not needed for the single output modes because in that case, the last pixel is from a column of the dark reference which is not used. See the section on correlated double sampling for a description of the one pixel delay in the CDS ci rcuit.

Electronic Shutter

Substrate Voltage

The voltage on the substrate, pins L1 and L5, determines the charge capacity of the photodiodes. When VSUB is 8 V the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 V decreases the charge capacity of the photodiodes until 30 V when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on VSUB, with a peak amplitude greater than 30 V, empties all photodiodes and provides the electronic shuttering action.

Substrate Voltage and Anti-Blooming

It may appear the optimal substrate voltage setting is 8 V to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 V will provide the maximum dynamic range, it will also provide the minimum anti-blooming protection.

The KAI−1020 VCCD has a charge capacity of 60,000 electrons (60 ke^-). If the VSUB voltage is set such that the photodiode holds more than 60 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on VSUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate.

If that maximum rate is exceeded, (say, for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of anti-blooming protection also decreases when the integration time is decreased.

There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of

anti-blooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) anti-blooming protection. A high VSUB voltage provides lower dynamic range and maximum anti-blooming protection. The optimal setting of VSUB is written on the container in which each KAI−1020 is shipped. The given VSUB voltage for each sensor is selected to provide anti-blooming protection for bright spots at least 100 times saturation, while maintaining at least 500 mV of dynamic range.

A detailed discussion of anti-blooming and smear may be found in IEEE Transactions on Electron Devices vol. 39 no. 11, pg. 2508.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Electronic Shutter Timing

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of t_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 30 V t_{INT} seconds before the photodiode to VCCD transfer pulse on ϕV2B. The large substrate voltage pulse is generated by the KAI−1020. The electronic shutter is triggered by a 5 V pulse on ϕSH. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD. The electronic shutter pulse may be added to the end of the horizontal line timing and just after the last pixel has been read out of the HCCD. ϕH1S and ϕH2S must be clocked during the electronic shutter pulse.

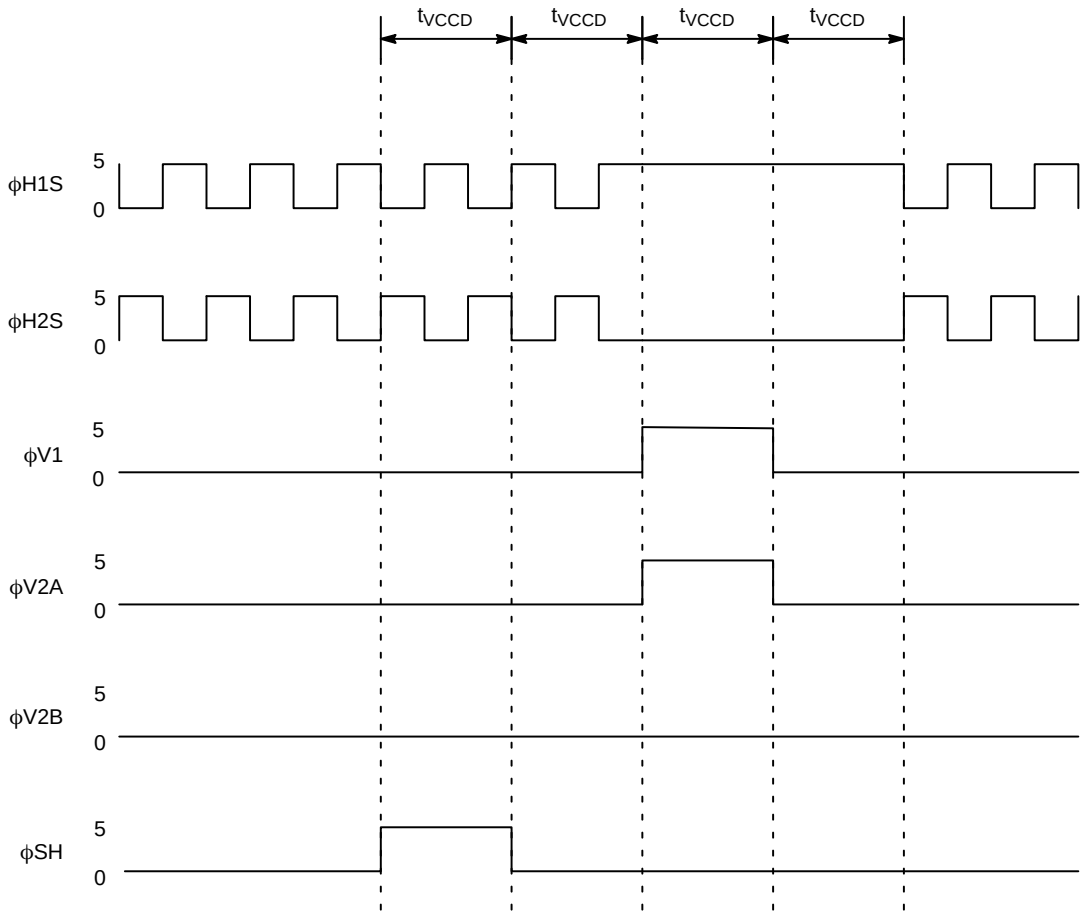


Figure 25. Electronic Shutter Timing

Fast Dump

The KAI−1020 has the ability to rapidly discard (fast dump, FD) entire lines of the image. The fast dump is a drain attached to the last row of the VCCD just before the HCCD. When the fast dump is activated by taking ϕFD high, charge from the VCCD goes into the drain instead of into the HCCD.

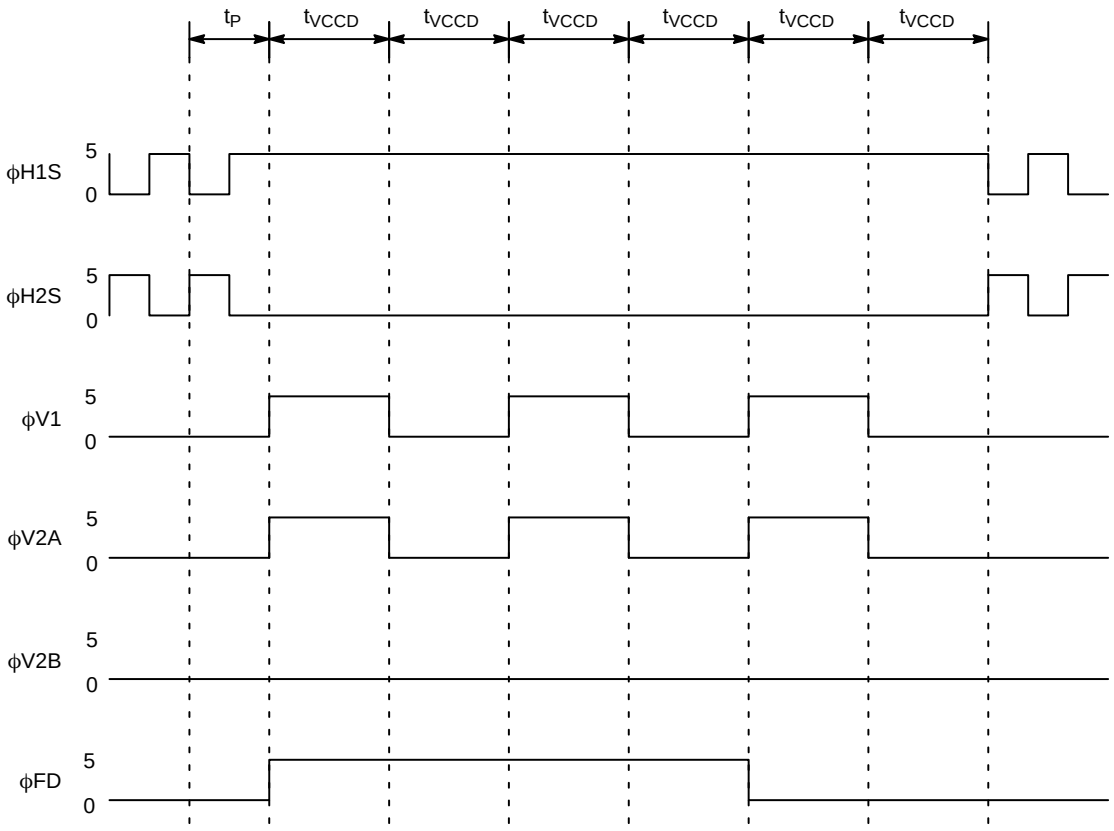


Figure 26. Fast Dump Timing

This timing diagram shows how two lines are dumped and the third is read out. ϕFD should go high once the last pixel of the preceding line has been read out. Cycle the VCCD for the number of rows to be dumped. The above timing diagrams shows two rows being dumped. When the proper number of rows have been dumped bring ϕFD low. Then clock the VCCD through one more cycle to shift a row into the HCCD.

The fast dump can be used to sub-sample the image for increased frame rates. For example, by dumping the even numbered lines, the image will be sub-sampled by a factor of 2 and the frame rate will almost increase by a factor of 2. Horizontal sub-sampling is not possible. The HCCD must always be cycled for the entire number of pixels in one line.

Another way to increase the frame rate is through sub-windowing. For example, suppose only the center 512 lines of the image are needed. Turn on the fast dump and clock the VCCD for 256 lines. Then turn off the fast dump and clock the VCCD (and HCCD) for 512 lines. Finally, turn the fast dump on again and clock the VCCD for 240 lines.

Binning and Interlaced Modes

Binning is a readout mode of progressive scan CCD image sensors where more than one row at a time is clocked into the HCCD before reading out the HCCD. This timing mode sums two or more rows together. It increases the frame rate because there are fewer total rows to read out of the HCCD. The following timing diagram shows how two rows are summed together:

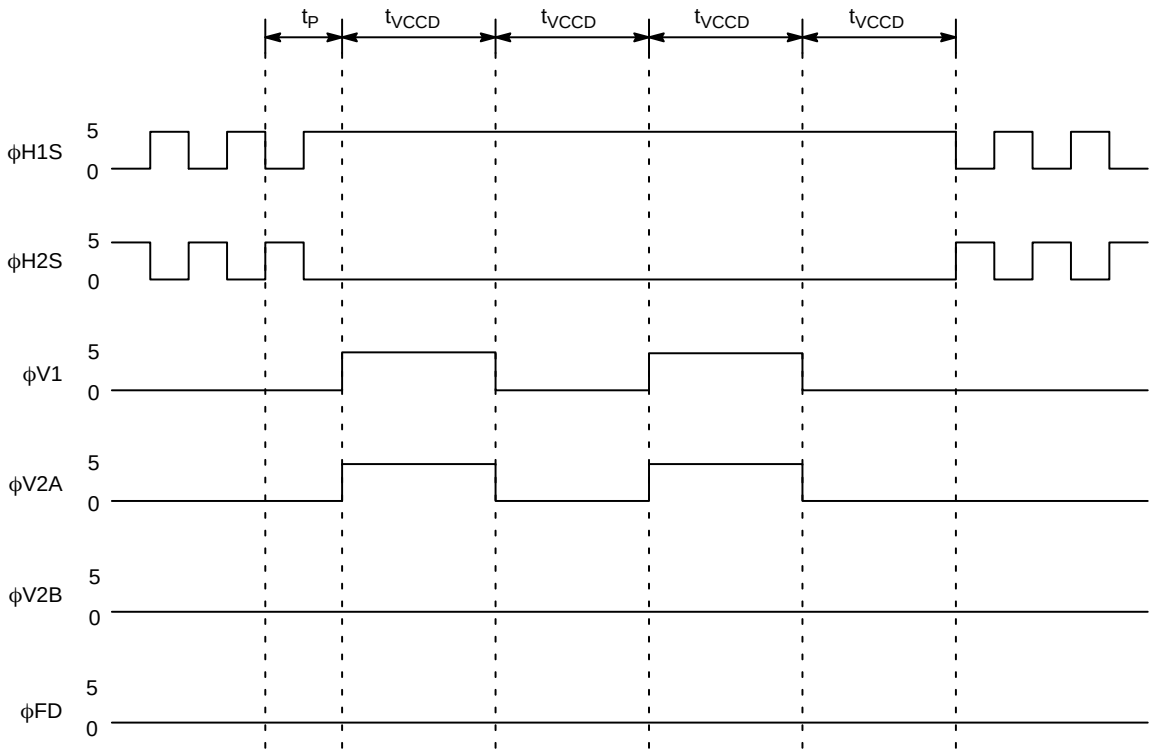


Figure 27. Binning Line Timing

When binning two rows together only 504 rows need to be read out of the HCCD instead of the normal 1008 rows. The HCCD will hold up to two VCCD rows of full signal without blooming. Binning more than two rows may cause horizontal blooming for saturated signal levels.

Interlaced readout is a form of binning. To read out the even field use binning to sum together rows 0+1, rows 2+3, ... rows 1006+1007. To read out the odd field use binning to read out rows 0+1+2, rows 3+4, rows 5+6, ... rows 1005+1006, rows 1007+1008. The odd field may also be read out as row 0, rows 1+2, rows 3+4, ... rows 1005+1006. See the Interlaced – Field Integration section for an example of interlaced timing.

Correlated Double Sampling (CDS)

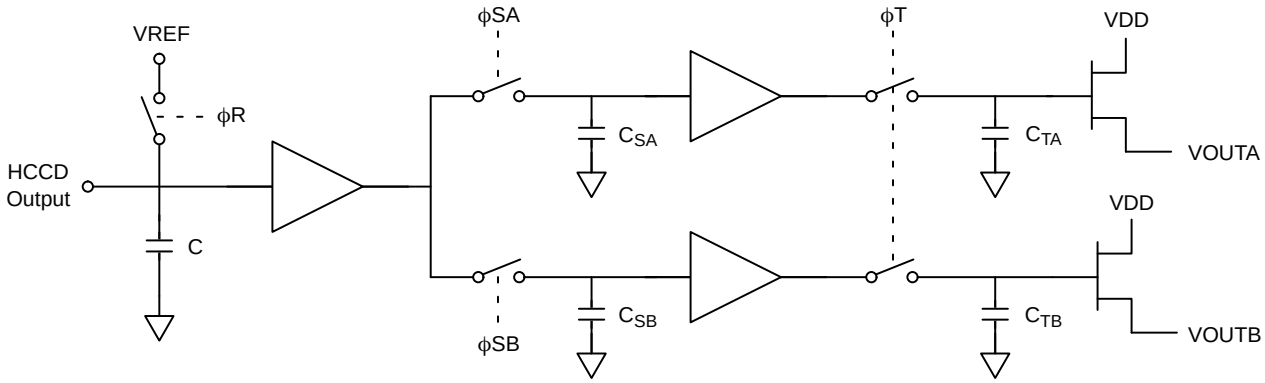


Figure 28. Correlated Double Sampling Block Diagram

Correlated double sampling is a method of measuring the amount of charge in each pixel. The electrons in the last pixel of the HCCD are transferred onto a very small sensing capacitor, C, on the falling edge of ϕH2S. The voltage on C will change by about 20 μV for each electron that was in the HCCD. The process of measuring the amount of charge begins by resetting the value of C to an internally generated reference voltage, Vref. A short pulse on ϕR at the rising edge of ϕH2S will reset C. After C has been reset, its voltage is sampled and stored on C_{SA} by a short pulse on switch ϕSA. Then on the falling edge of ϕH2S, electrons are transferred onto the capacitor, C. The new voltage on C is sampled and stored on C_{SB} by a short pulse on switch ϕSB. These two sampled voltages are then transferred to capacitors C_{TA} and C_{TB} by a short pulse on ϕT. ϕT and ϕR generally occur at the same time. An external operational amplifier is used to subtract the two voltages on VOUTA and VOUTB. The output of the op-amp will be proportional to the number of electrons contained in one pixel. Note that it takes one entire pixel clock cycle for the value of the pixel to appear on VOUTA and VOUTB. The A and B outputs of the CDS circuit will be in the range of 7 to 11 V.

CDS Timing Edge Alignment

1. The edge alignments of the CDS timing pulses ϕSA, ϕSB, ϕT, and ϕR are critical to proper operation of the CDS circuit.
2. The falling edge of ϕR must not overlap the rising edge of ϕSA
3. The falling edge of ϕSA must come at the same time or before the falling edge of ϕH2
4. The rising edge of ϕSB must come after the falling edge of ϕH2
5. The falling edge of ϕSB must come before the rising edge of ϕR
6. The rising edge of ϕR may come before the rising edge of ϕH2
7. ϕT should always be driven by the same timing signal as ϕR
8. The pulse widths should be set such that ϕR, ϕSA, and ϕSB are 1/3 of t_P

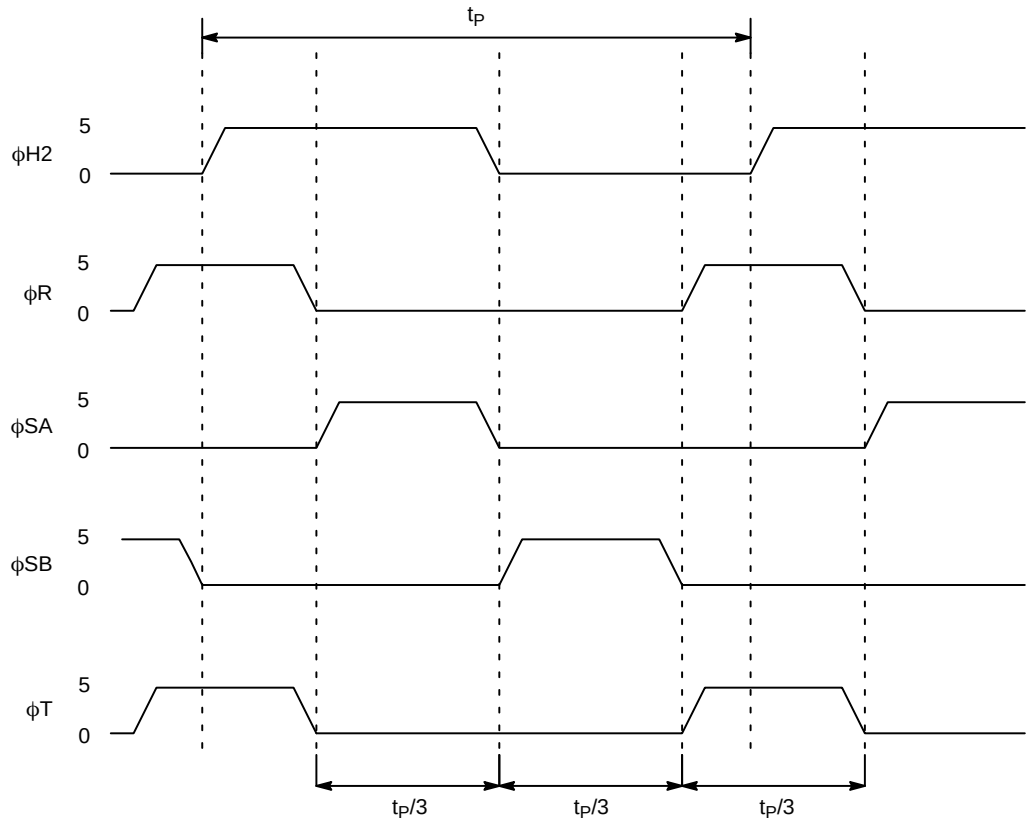


Figure 29. Correlated Double Sampling Timing

Disabling the CDS

There may be instances when the camera designer may want to use an external CDS. Such cases may occur at pixel clock frequencies 20 MHz or slower where integrated CDS, analog to digital converter (A/D), and auto offset/gain circuits are available. These external CDS circuits require the raw unprocessed video waveform. The raw video can be obtained by permanently turning on the ϕSA, ϕSB, and ϕT switches by connecting them to a voltage in the range of 8 to 10 V (the V2HIGH supply voltage, for example). Then place a load of 4 mA to 5 mA on VOUTA and a load of 0.1 mA on VOUTB. VOUTA will be the raw video output suitable for external CDS circuits. The 5 mA load may be a 2.0 kΩ resistor and the 0.1 mA load may be an 80 kΩ resistor to GND. An external CDS is not recommended for pixel frequencies above 20 MHz.

Timing and Voltage Specifications

Table 10. ABSOLUTE MAXIMUM RATINGS

		Minimum	Maximum	Units	Notes
Temperature	Operation without Damage	−50	70	°C	
	Storage	−55	70	°C	
Voltage between Pins	VSUB to GND	8	20	V	
	VDD to GND	0	17	V	
	ϕV1 to ϕV2, ϕFD to ϕV1, ϕV2	−10	10	V	
	ϕH1 to ϕH2	−8	8	V	
	ϕR, ϕT, ϕSA, ϕSB to GND	−9	12	V	
	ϕH1, ϕH2 to ϕV1, ϕV2	−9	10	V	
Current	Video Output Bias Current	0	7	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For electronic shuttering V_{SUB} may be pulsed to 35 V for up to 10 μs.
2. Note that the current bias affects the amplifier bandwidth.

Table 11. TIMING

Time	Minimum	Nominal	Maximum	Units
t_P	25	25	500	ns
t_{VCCD}	3.6	3.6	10	μs
t_{VP}	20	25	40	μs
t_{V3}	8	10	15	μs

Table 12. BIAS VOLTAGES

Bias	Minimum (V)	Nominal (V)	Maximum (V)	Peak Current (mA)	Peak Current Frequency	Avg. Current (mA)
V1S5	4	5	6	2	2L	0.13
V1MID	−1.5	−1.2	−1.0	110	L	3
V1LOW	−9.5	−9	−8.5	110	L	3
V2S5	4	5	6	2	2L	0.5
V2S9	8	9	10	2	F	0.3
V2HIGH	8	9	10	110	L	0.01
V2MID	−1.5	−1.2	−1.0	110	L	3
V2LOW	−9.5 −9.5	−9 −9	−8.5 −8.5	110 220	L F	3.8 3.8
VDD1	14.5	15	15.5	−	−	14
VDD2	14.5	15	15.5	−	−	14
VSH15	14	15	16	1	F	0.08
VSUB	8	*	14	−	−	0.03

1. Average currents are for 30 frames/second.
2. Peak switching currents are for less than 1 μs duration.
3. L = once per line time, 2L = twice per line time, F = once per frame time.
4. Substrate bias voltage for a 500 mV output range is written on the shipping container for each part.

Power Up Sequence

1. Power up VSUB, V1LOW, V2LOW first
2. Then power up VDD, VSH15, V2S5, V1S5, V1MID, V2MID and V2HIGH
3. Then after the coupling capacitors on all of the timing inputs have charged, begin clocking the timing inputs.

Any positive voltage should never be allowed to go negative. Any negative voltage should never be allowed to go positive.

Note that the shutter driver clock input does not use a coupling capacitor. It must be driven directly from a 5 V logic buffer as shown in the evaluation board schematic.

Table 13. PULSE AMPLITUDES

Clock	Min. Amplitude (V)	Coupling	Min. Coupling Capacitor Value (μF)	Max. Coupling Capacitor Value (μF)
ϕSH	3.5	DC	–	–
ϕH1	4.7	AC	0.1	0.47
ϕH2	4.7	AC	0.1	0.47
ϕSA	4.7	AC	0.01	0.47
ϕSB	4.7	AC	0.01	0.47
ϕR	4.7	AC	0.01	0.47
ϕT	4.7	AC	0.01	0.47
ϕV1	4.0	AC	0.01	0.47
ϕV2A	4.0	AC	0.01	0.47
ϕV2B	4.0	AC	0.01	0.47
ϕFD	4.0	AC	0.1	0.47

Timing Examples

Progressive Scan

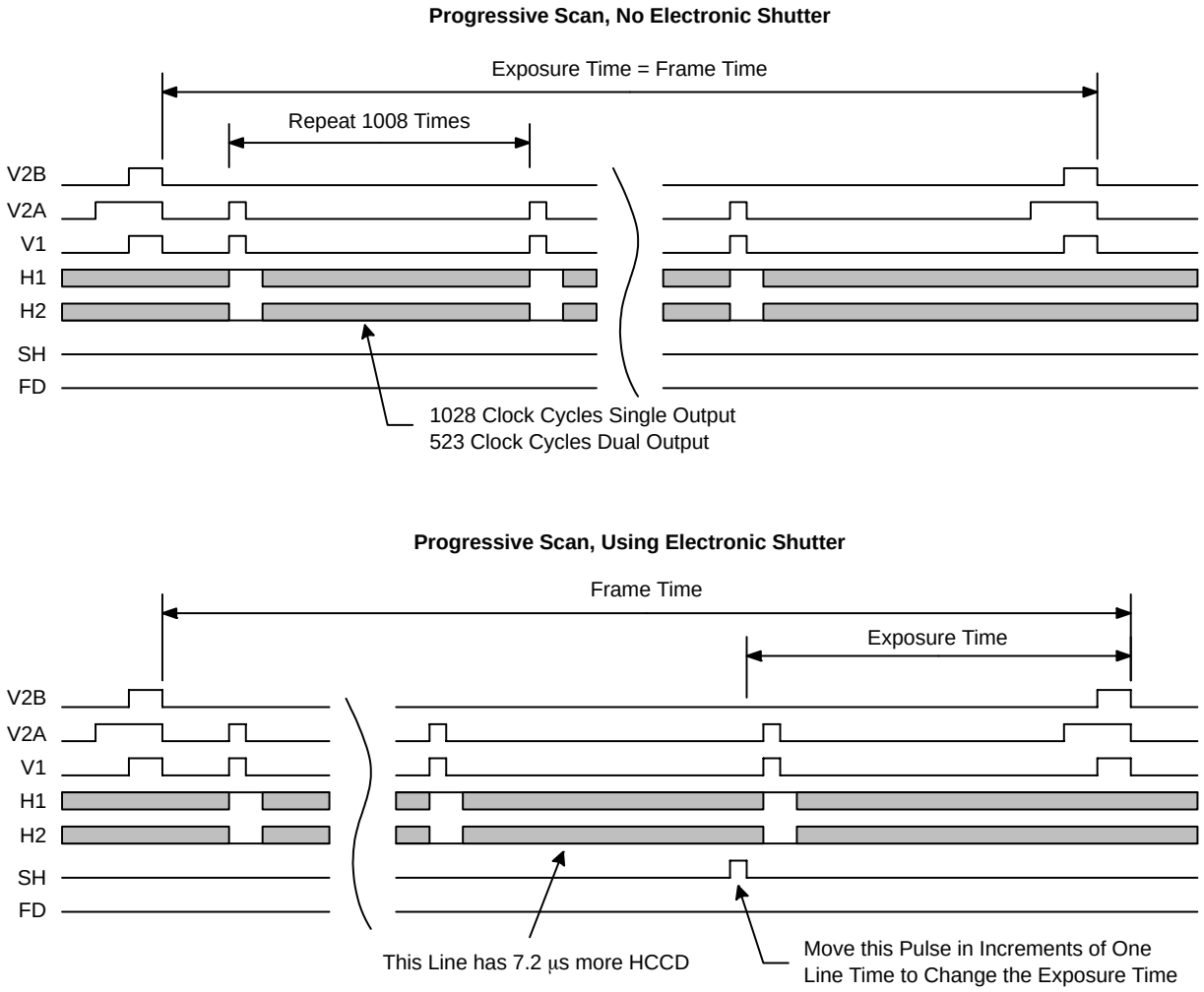
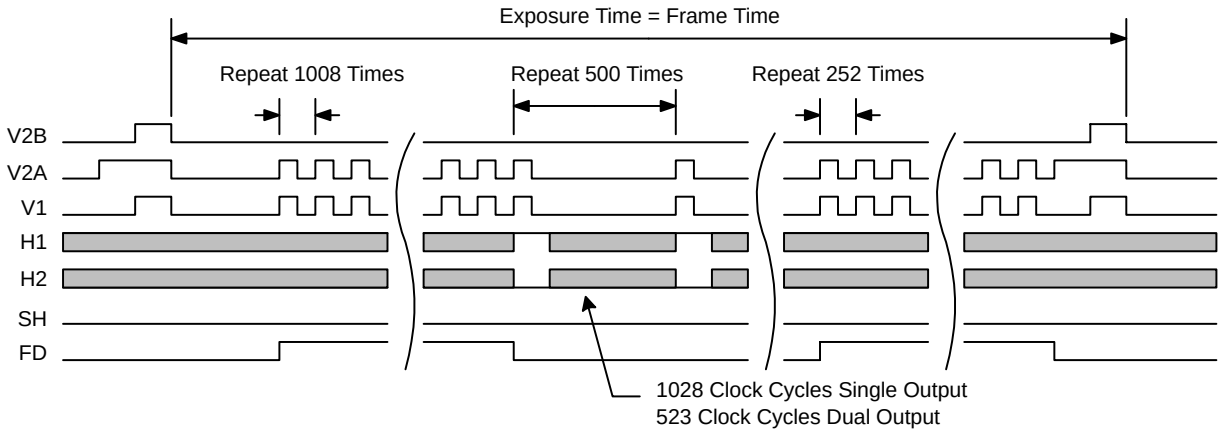


Figure 30. Progressive Scan Timing Example

Fast Line Dump

Fast Dump Timing, Reads Out the Center 500 Rows



Fast Dump Timing with Electronic Shutter, Reads Out the Center 500 Rows

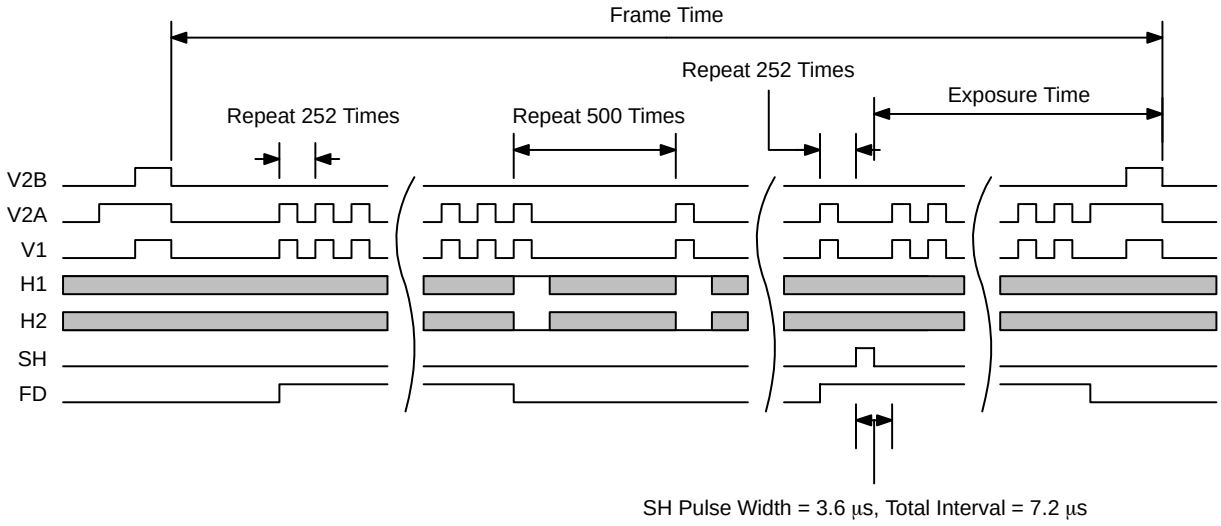


Figure 31. Fast Line Dump Timing Example

Interlaced − Field Integration

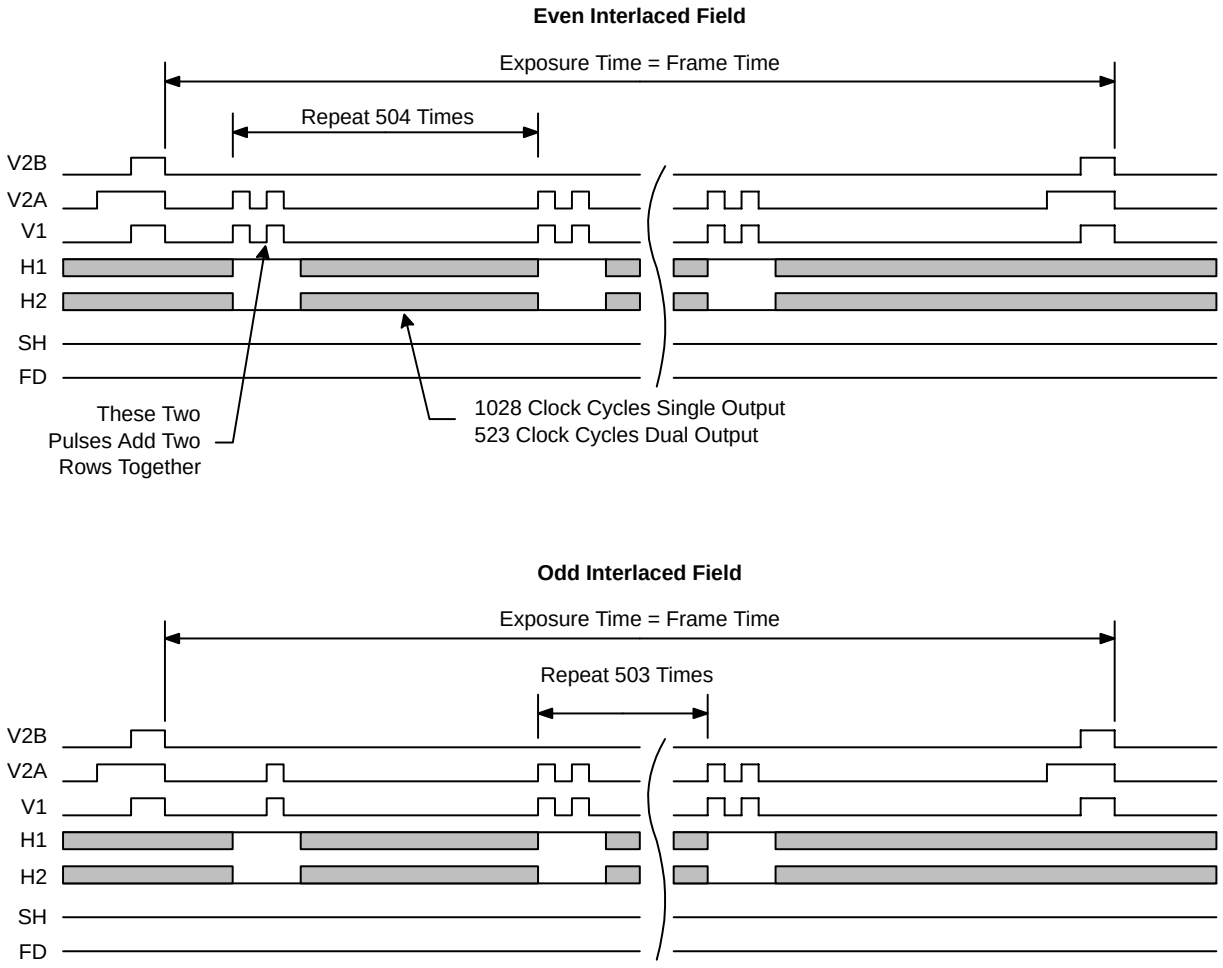


Figure 32. Interlaced − Field Integration Timing Example

CAMERA DESIGN

Low Level Block Diagram

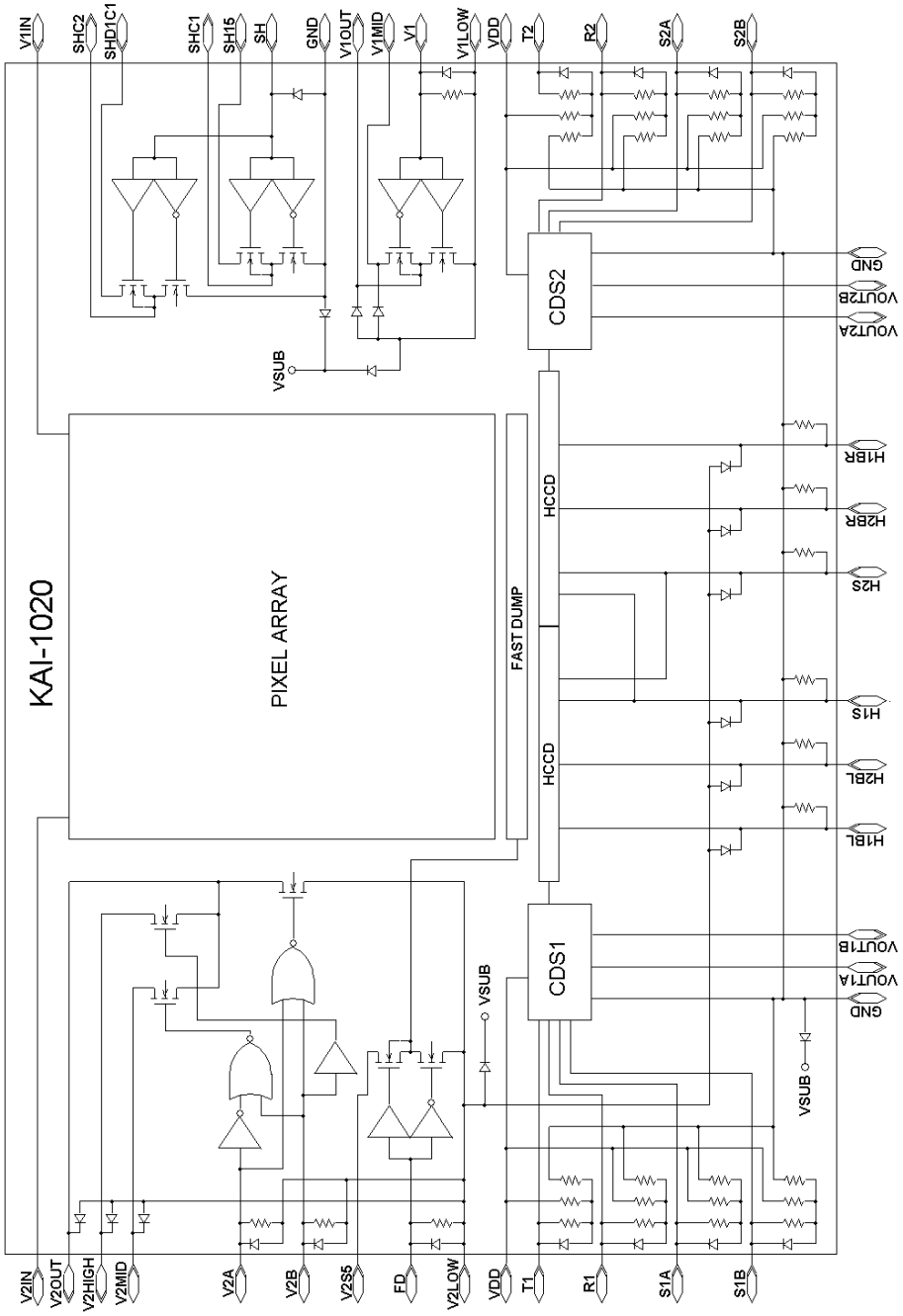
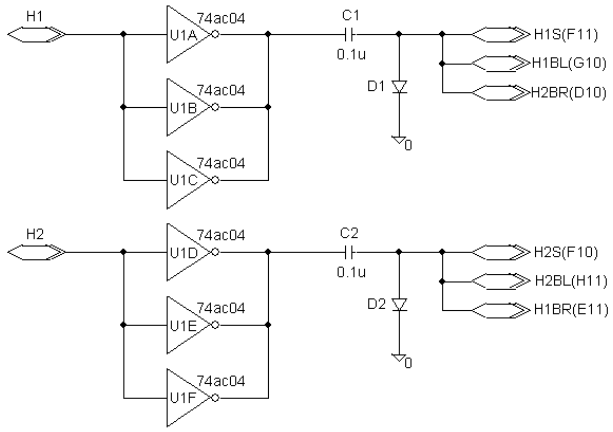


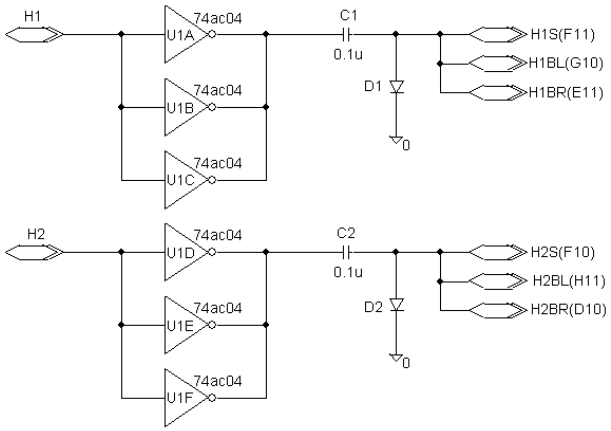
Figure 33. Low Level Block Diagram

Horizontal CCD Drive Circuit

Single Output Only



Dual Output Only



Selectable Single or Dual Output

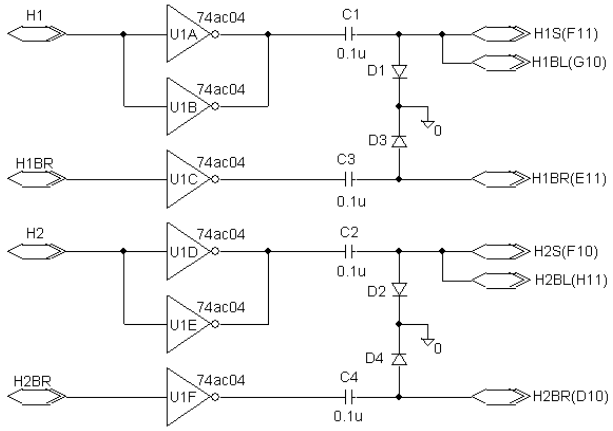


Figure 34. HCCD Drive Block Diagram

The HCCD clock inputs should be driven by buffers capable of driving a capacitance of 60 pF and having a full voltage swing of at least 4.7 V. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a 0 V to –5 V clock. A negative clock level is easily obtained by capacitive coupling and a diode to clamp the high level to GND. Every HCCD clock input has a 300 kΩ on chip resistor to GND.

The inputs to the above circuits, H1 and H2, are 5 V logic from the timing generator (a programmable gate array for example). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the H1BR and H2BR timing. For single output mode program the timing such that H1BR = H2 and H2BR = H1. For dual output mode program the timing such that H1BR = H1 and H2BR = H2.

Vertical CCD

The VCCD clock inputs, ϕV2A, ϕV2B, ϕV1, and ϕFD have a capacitive load of approximately 10 pF. Each input is connected to V2LOW and V1LOW by a 60 kΩ internal resistor. There is also an internal diode connected to V2LOW and V1LOW. The 5 V logic drivers must be connected to the sensor inputs through capacitors. These inputs require a clock of at least 4 V amplitude. Most PGA's can drive these inputs directly. The external capacitor and internal diode level shift the 0 V to 5 V input to V2LOW to V2LOW + 5.

The on chip VCCD clock drivers switch their outputs, V1OUT and V2OUT, between the supply voltages V1LOW, V1MID, V2LOW, V2MID, and V2HIGH. The truth table correlating the voltage on V1OUT and V2OUT to the timing inputs is:

Table 14.

ϕV1	**V1OUT**
H	V1MID
L	V1LOW

ϕV2A	**ϕV2B**	**V2OUT**
L	L	V2LOW
H	L	V2MID
L	H	V2HIGH
H	H	V2HIGH

NOTE: L = Logic Low level; H = Logic High level

The output of the VCCD driver is connected to the VCCD gates by wiring V1OUT to V1IN and V2OUT to V2IN. The fast dump driver has no external output. It is wired internally to the VCCD fast dump gate.

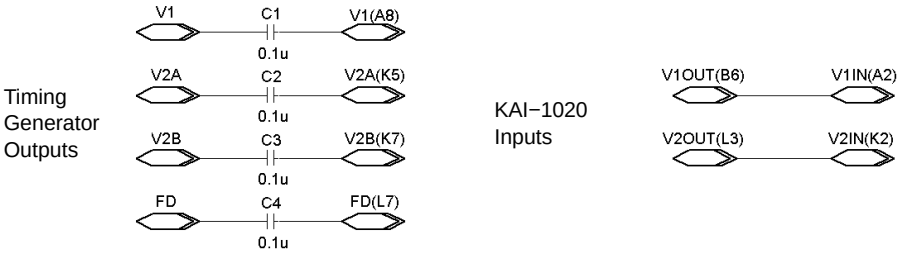


Figure 35. VCCD Block Diagram

Electronic Shutter

The electronic shutter input, ϕSH, is the only input driven directly by CMOS logic. No capacitive coupling is required. ϕSH (pin B3) has approximately a 10 pF load. The logic low level must be less than 0.5 V and the logic high level must be greater than 3.5 V. Most programmable gate arrays can drive ϕSH directly. The on chip electronic shutter driver is a charge pumping circuit. It uses C1, C2, D1, and D2 to generate a > 25 V pulse that is added onto the substrate DC bias voltage. The substrate bias voltage is set by a trim-pot R2 or by some programmable voltage source. The substrate bias voltage absolutely MUST be adjustable. The camera designer CAN NOT rely on every KAI−1020 image sensor requiring the same substrate bias. An adjustment range of 8 to 13 V must be allowed. Each image sensor has the optimal substrate bias voltage (as measured on the VSUB pin) printed on the shipping container.

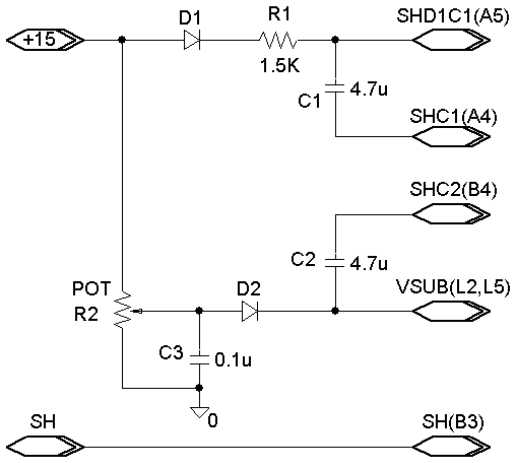


Figure 36. Electronic Shutter Block Diagram

The minimum allowed voltage on VSUB is 8 V. Lower voltages may destroy the CDS and clock driver circuits.

NOTE: Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note Us*ing Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

CDS Timing Inputs

The CDS timing inputs ϕR, ϕT, ϕSA, and ϕSB should be driven by CMOS logic with fast rise and fall times and an amplitude of at least 4.7 V. The capacitance of each pin on the sensor is approximately 10 pF. The pulses are level shifted positive by 1 V or 2 V on the sensor. If driving this input directly from a programmable gate array, be aware that some PGA's do not have outputs with amplitudes of 4.7 V. It is recommended that the CDS timing inputs be driven by a 74AC04 to insure a 5 V pulse amplitude with fast edges.

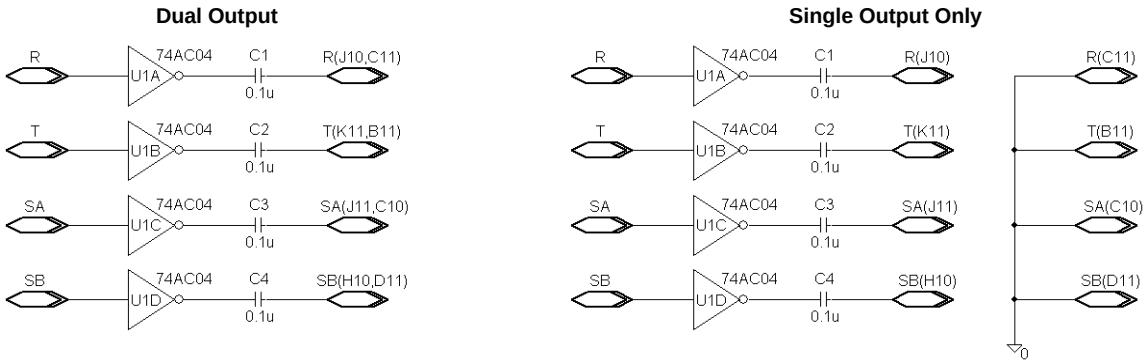


Figure 37. Correlated Double Sampling Block Diagram

If the camera will only operate in single output mode then the ϕR2, ϕT2, ϕS2A, and ϕS2B inputs should be connected to GND. All CDS timing inputs must be coupled with a capacitor.

CDS Output Circuit

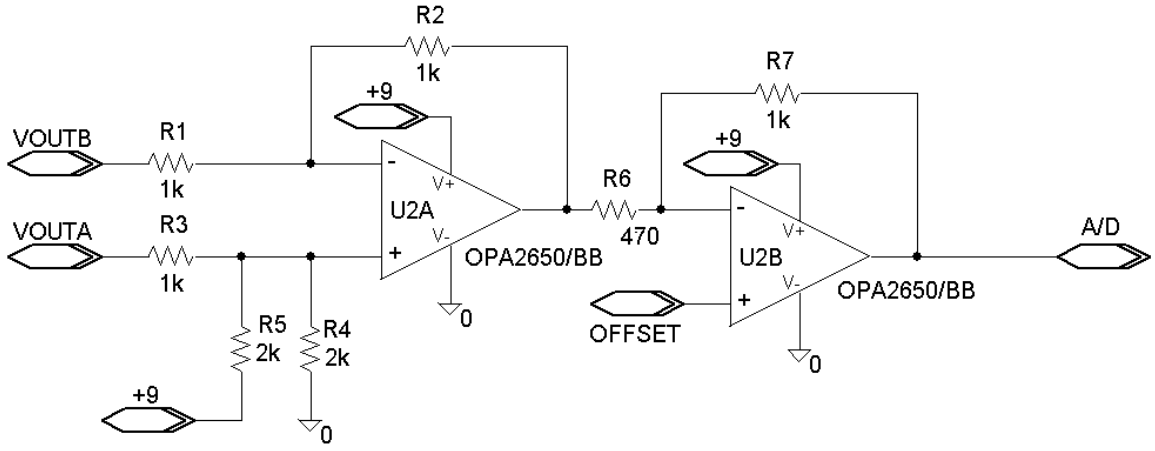


Figure 38. Correlated Double Sampling Output Circuit Block Diagram

In the above schematic the differential video outputs VOUTB and VOUTA are subtracted by op-amp U2A. The video outputs will have a DC level of 7 to 11 V. U2B then inverts the signal and applies a gain of 2.1 relative to the offset voltage. The output of U2B will match the 500 mV output range of the KAI−1020 to the 1 V input range of the analog to digital converter (A/D).

VOUTB will swing in the negative direction with increasing light level. The output of U2A will swing in the positive direction with increasing light level. The output of U2B (input to the A/D) will swing in the negative direction. This means the A/D output will be 0 counts when the image sensor is saturated. The digital data will have to be inverted before being transmitted to a digital image capture device. See the KAI−1020 evaluation board schematic for a simple method of inverting the data with no additional components.

The offset will have to be dynamically adjusted to match the zero light level of the image sensor. A circuit should examine the digital data in the dark reference columns and adjust the offset voltage of U2B to maintain a constant zero reference level in the A/D converter. The dynamic adjustment of the offset voltage will remove most temperature dependent drifts. Small temperature-dependent gain changes will still be present. See the KAI−1020 evaluation board schematic for an example of a circuit to generate the offset voltage.

This output circuit provides 10 bits of dynamic range on the KAI−1020 evaluation board. It is not the optimum circuit. For optimum differential common mode noise rejection and linearity, the CDS output circuit should take into account the 160 Ω impedance of the CDS output drive transistor.

Power Supplies

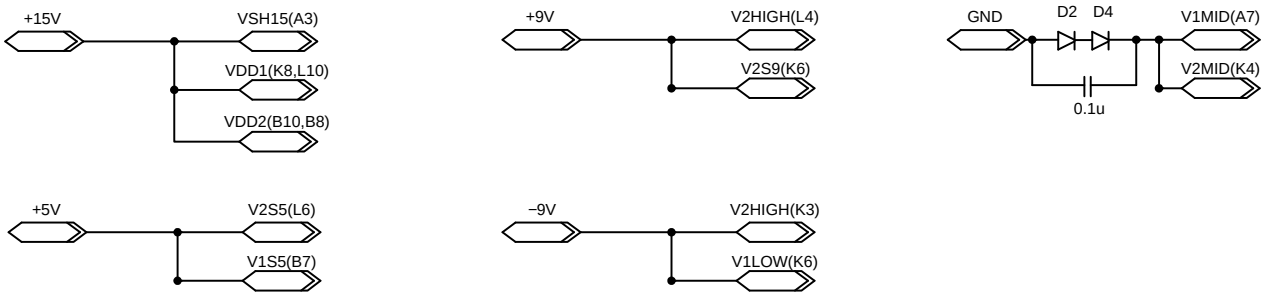


Figure 39. Power Supply Block Diagram

The V1MID and V2MID connections must be set to –1.0 to –1.5 V. Since V1MID and V2MID only sink current, two diodes can be used to set this voltage.

If the sensor is to use only the single output mode, then VDD2(B10,B8) can be connected to GND. VOUT2A(A9) and VOUT2B(A10) also should be connected to GND in the single output only mode.

KAI−1020 EVALUATION BOARD

Front Side

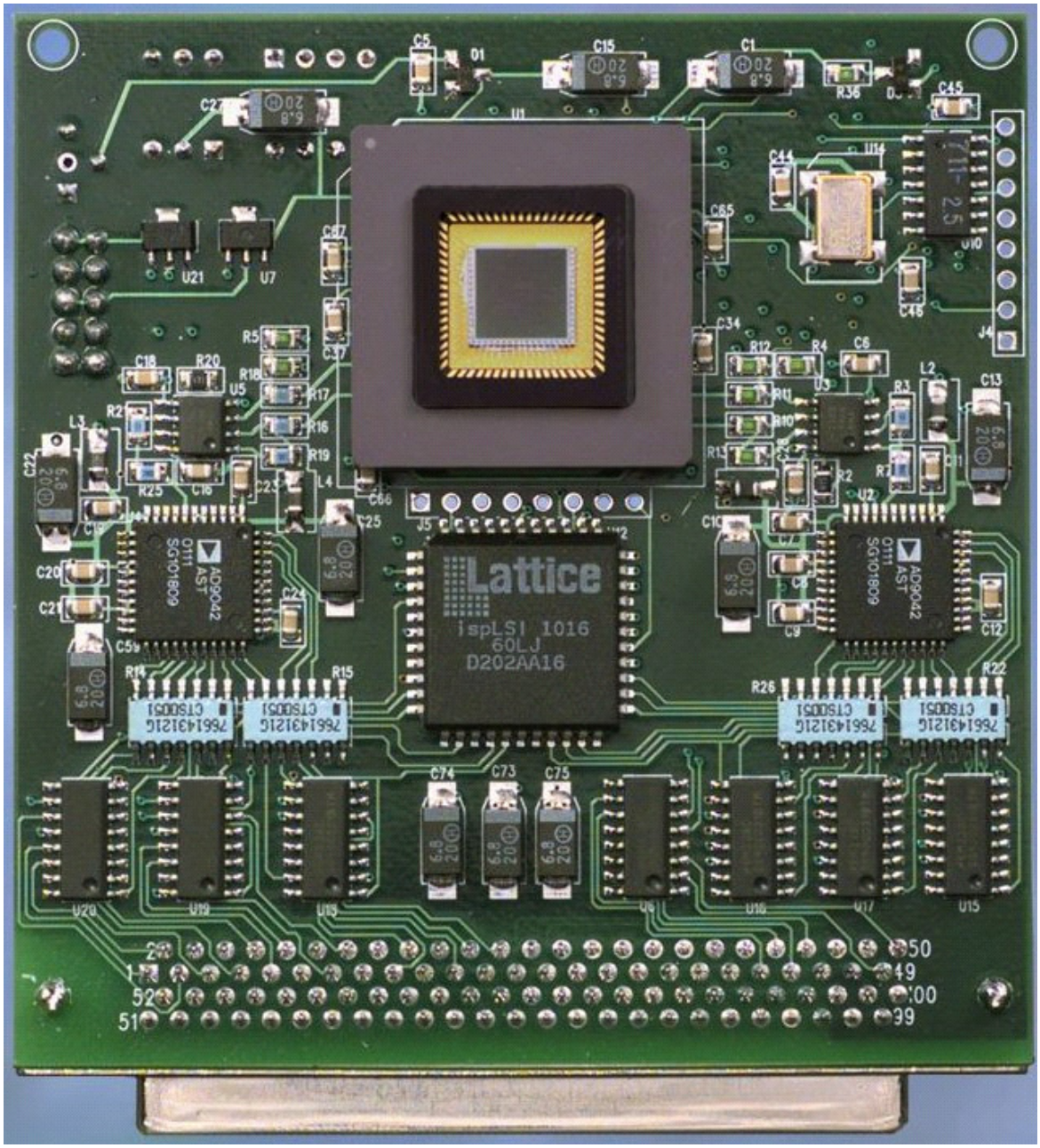


Figure 40. Evaluation Board (Front Side)

Back Side

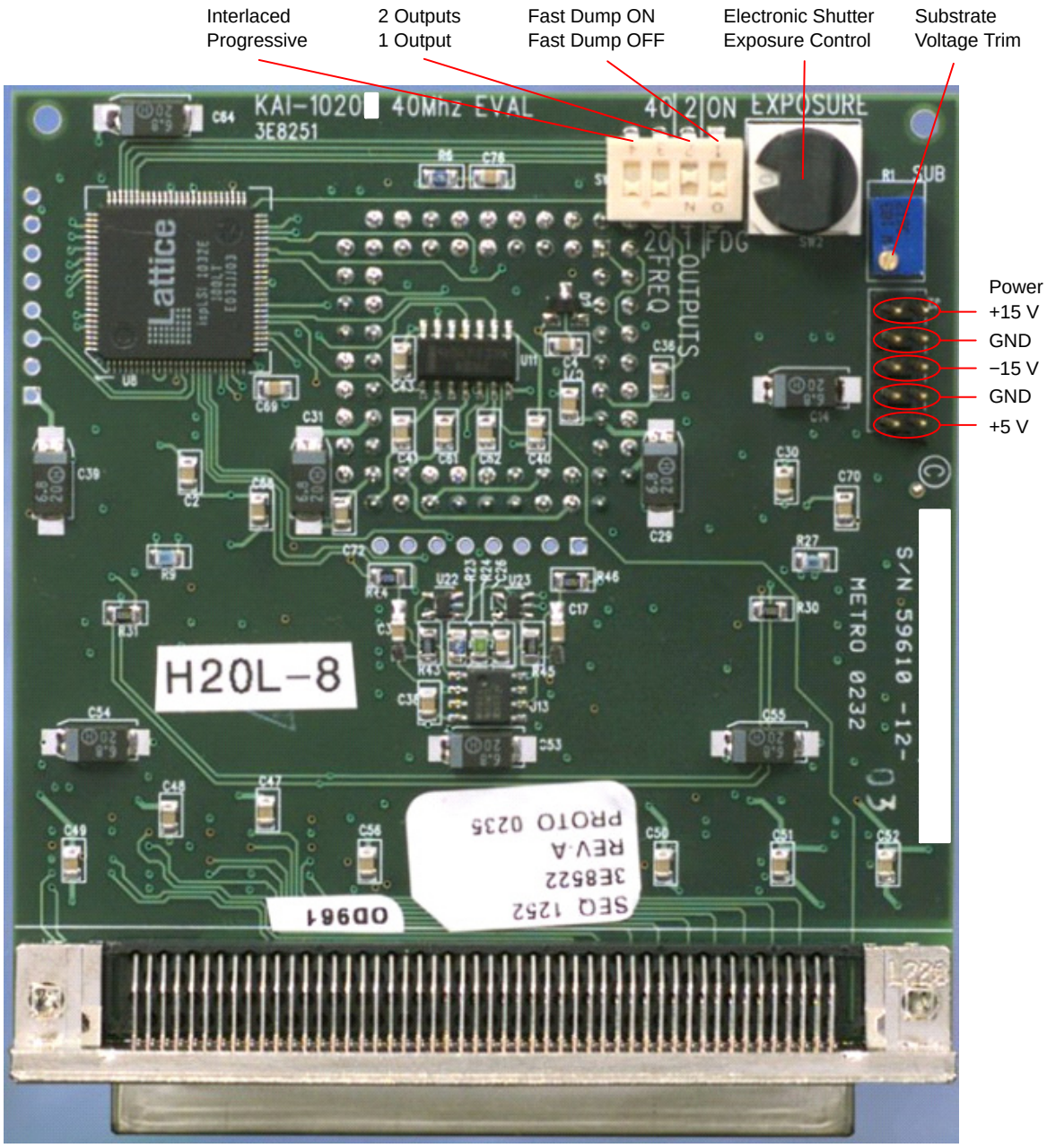


Figure 41. Evaluation Board (Back Side)

Schematics

KAI−1020

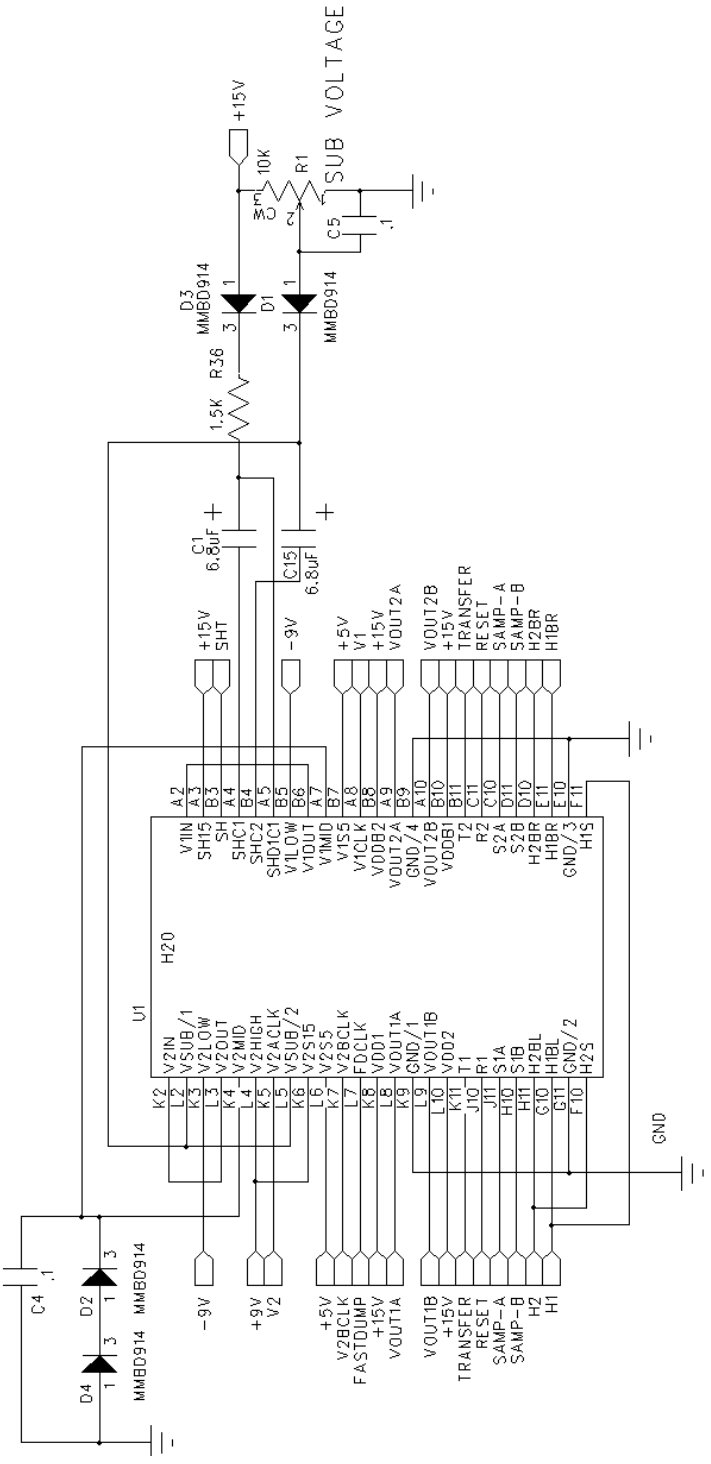


Figure 42. KAI−1020 Schematic

Timing Logic

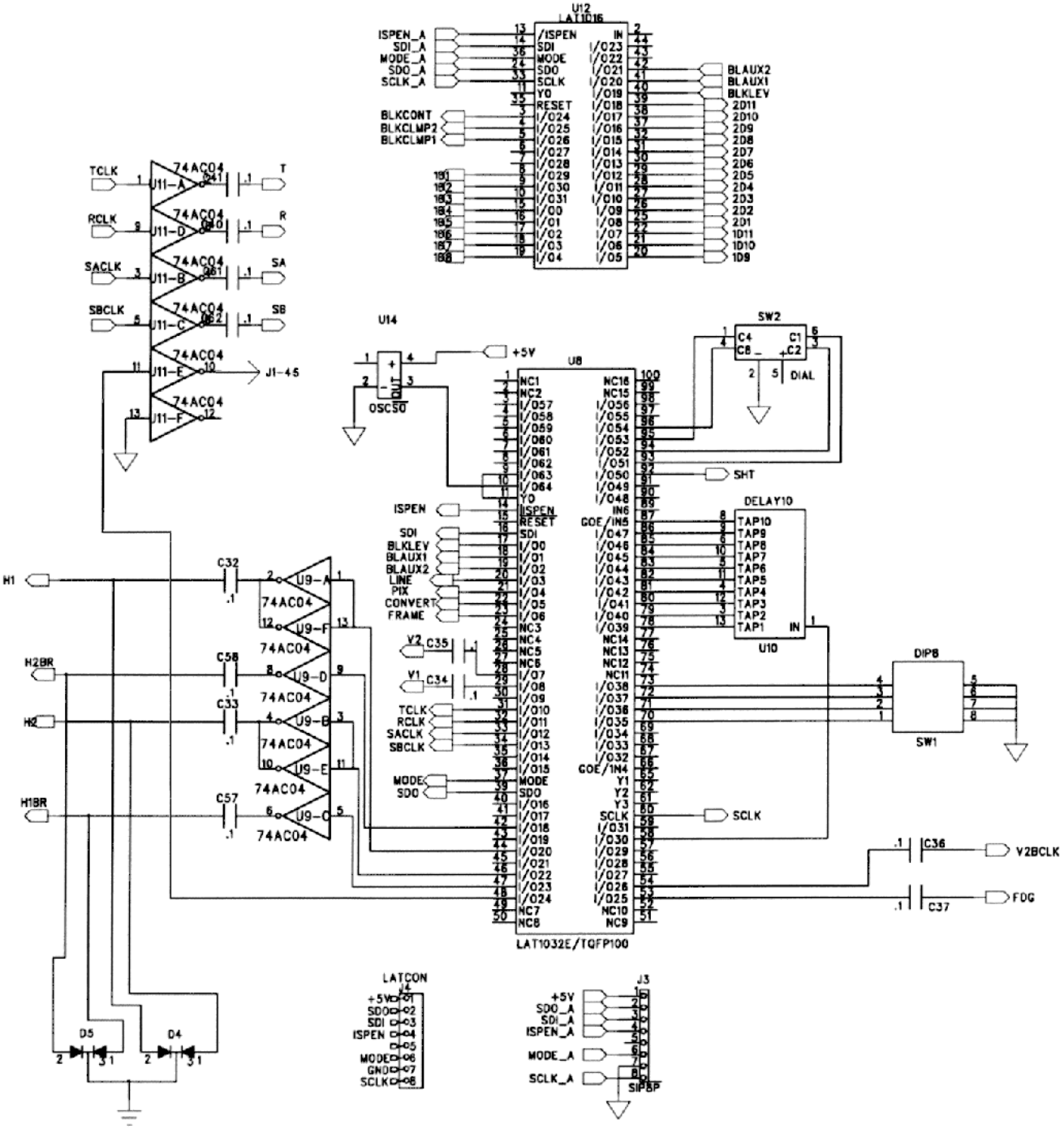


Figure 43. Timing Logic Schematic

Output 1

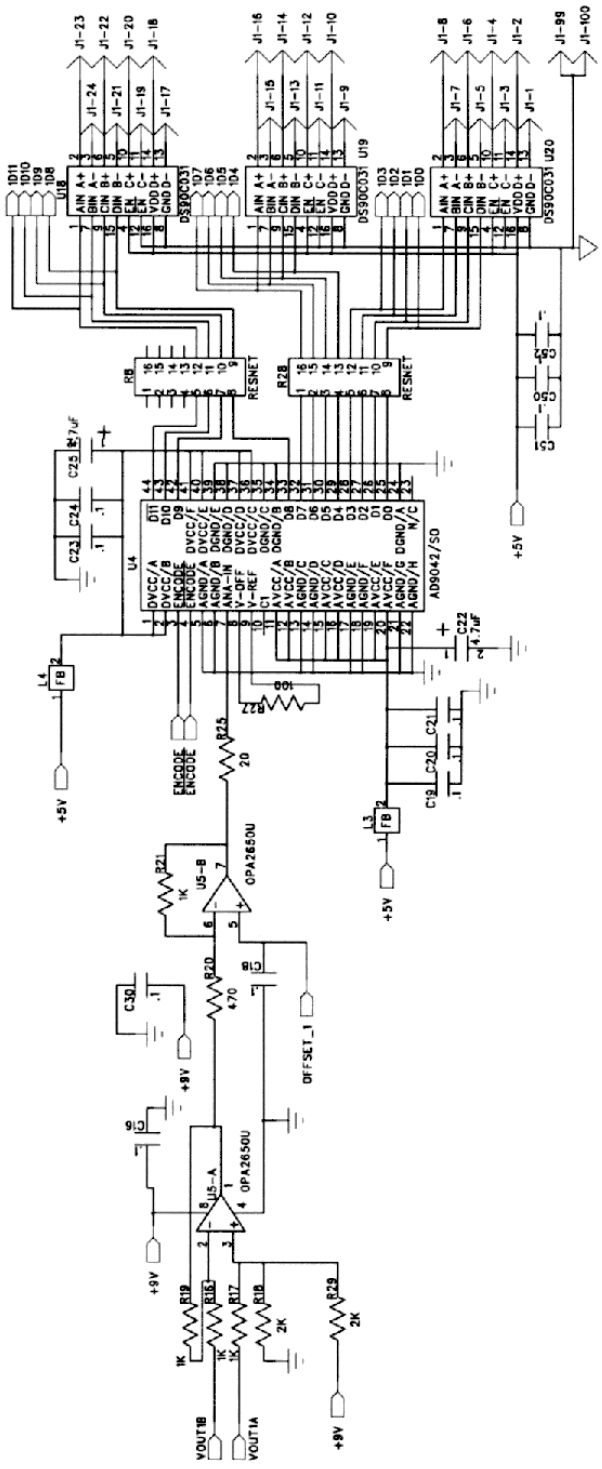


Figure 44. Output 1 Schematic

Output 2

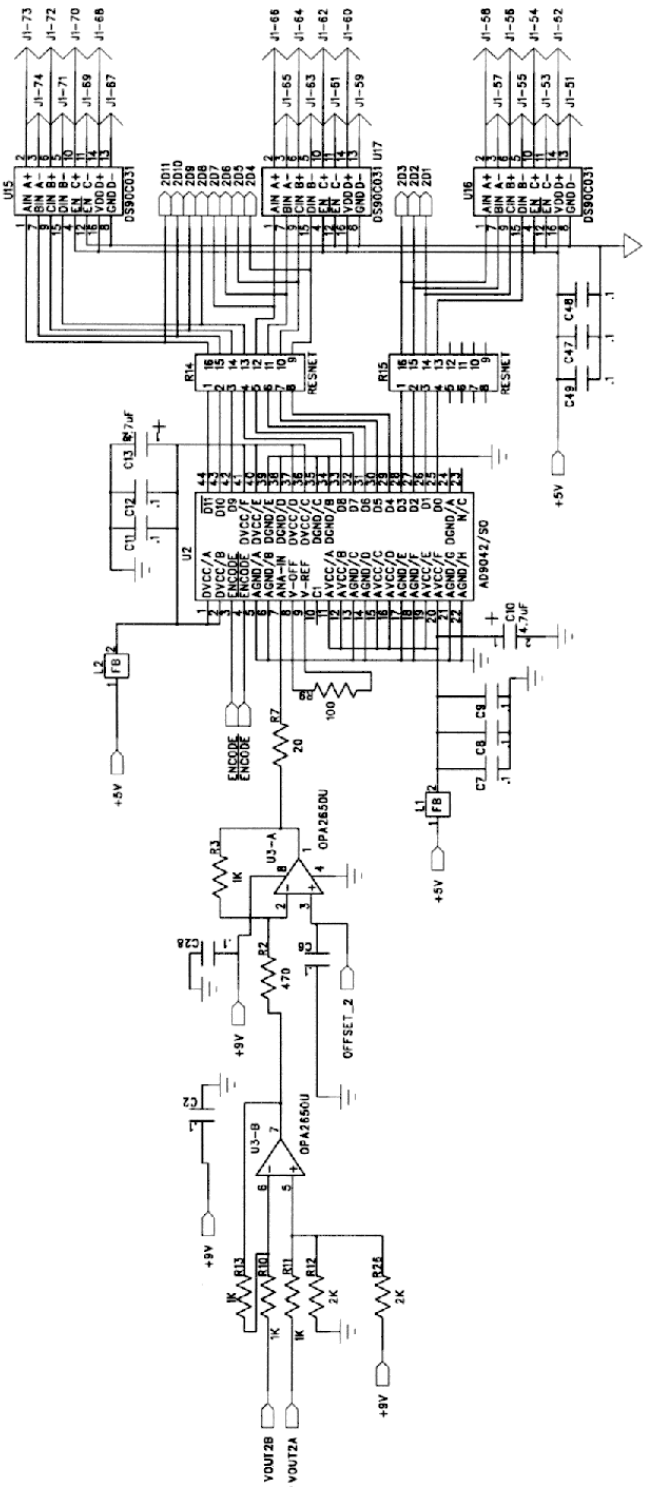


Figure 45. Output 2 Schematic

Automatic Offset and Power Supply

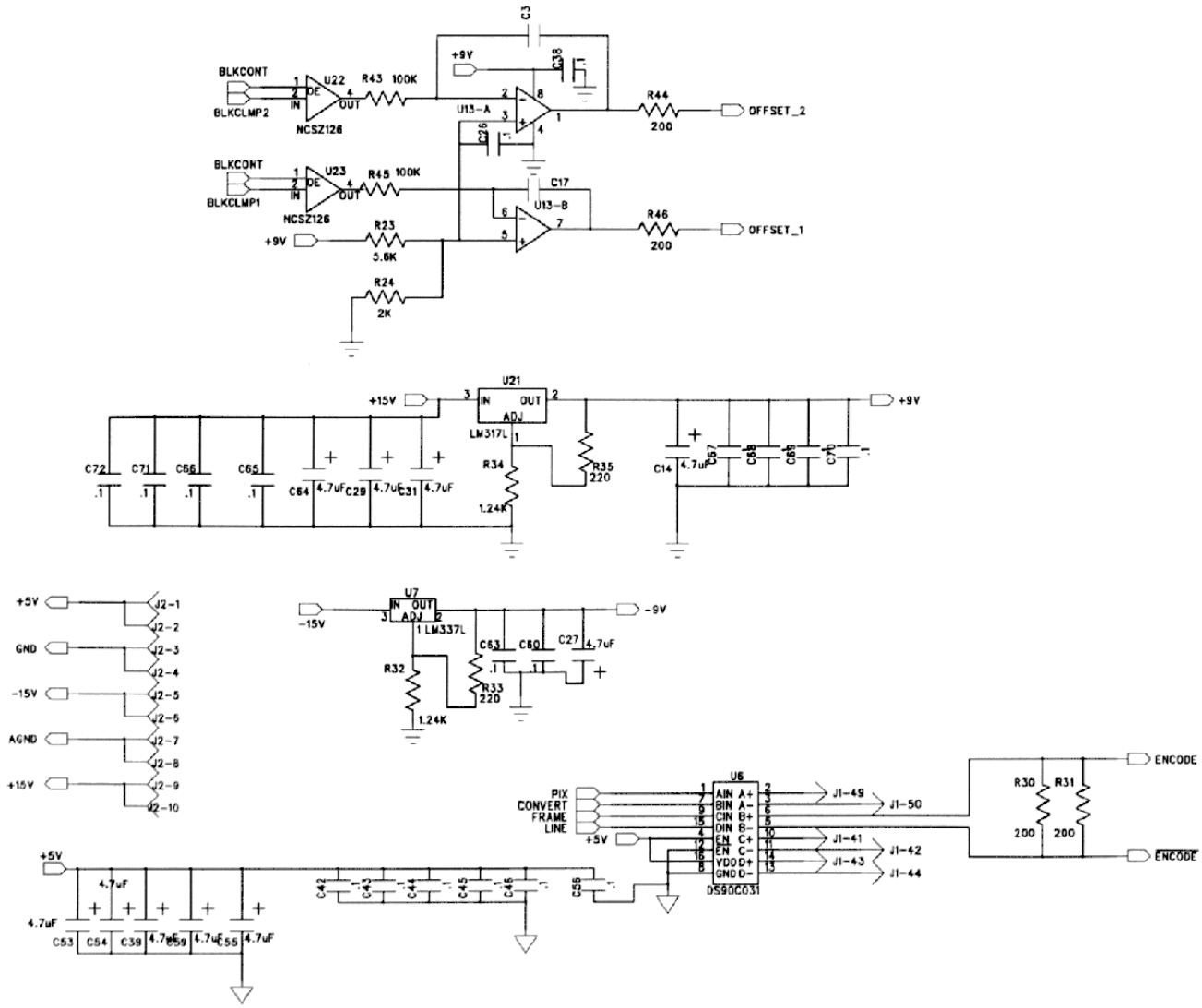


Figure 46. Automatic Offset and Power Supply Schematic

Parts List

Table 15. PARTS LIST

C1	PCAP, 4.7 μF	
C2	CAP, 0.1 μF	
C3	CAP, 1 μF	
C4−9	CAP, 0.1 μF	
C10	CAP, 4.7 μF	
C11, C12	CAP, 0.1 μF	
C13−15	CAP, 4.7 μF	
C16	CAP, 0.1 μF	
C17	CAP, 1 μF	
C18−21	CAP, 0.1 μF	
C22	CAP, 4.7 μF	
C23, C24	CAP, 0.1 μF	
C25	CAP, 4.7 μF	
C26	CAP, 0.1 μF	
C27	CAP, 4.7 μF	
C28	CAP, 0.1 μF	
C29	CAP, 4.7 μF	
C30	CAP, 0.1 μF	
C31	CAP, 4.7 μF	
C32−38	CAP, 0.1 μF	
C39	CAP, 4.7 μF	
C40−52	CAP, 0.1 μF	
C53−55	CAP, 4.7 μF	
C56−58	CAP, 0.1 μF	
C59	CAP, 4.7 μF	
C60−63	CAP, 0.1 μF	
C64	CAP, 4.7 μF	
C65−72	CAP, 0.1 μF	
D1−3	MMBD914	
D4, D5	MMBD2837	
R1	VRES, 10 kΩ	
R2	RES, 470 Ω	
R3	RES, 1 kΩ	
R7	RES, 20 Ω	
R8	RESNET	
R9	RES, 100 Ω	
R10, R11	RES, 1 kΩ	
R12	RES, 2 kΩ	
R13	RES, 1 kΩ	
R14	RESNET	
R15	RESNET	
R16, R17	RES, 1 kΩ	
R18	RES, 2 kΩ	
R19	RES, 1 kΩ	
R20	RES, 470 Ω	
R21	RES, 1 kΩ	
R23	RES, 5.6 kΩ	
R24	RES, 2 kΩ	
R25	RES, 20 Ω	
R26	RES, 2 kΩ	
R27	RES, 100 Ω	
R28	RESNET	
R29	RES, 2 kΩ	
R30	RES, 200 Ω	
R31	RES, 200 Ω	
R32	RES, 1.24 kΩ	
R33	RES, 220 Ω	
R34	RES, 1.24 kΩ	
R35	RES, 220 Ω	
R36	RES, 1.5 kΩ	
R43	RES, 100 kΩ	
R44	RES, 200 Ω	
R45	RES, 100 kΩ	
R46	RES, 200 Ω	
SW1	DIP8	4 POS DIP SW
SW2	DIAL	16 POS ROTARY
U1	KAI1020	IMAGE SENSOR
U2	AD9042/SO	A/D ANALOG DEV
U3	OPAMP DUAL, OPA2650U	BURR BROWN
U4	AD9042/SO	A/D ANALOG DEV
U5	OPAMP DUAL, OPA2650U	BURR BROWN
U6	DS90C031	NATIONAL
U7	LM337L	
U8	LAT1032E TQFP100	LATTICE SEMI
U9	74AC04	
U10	DELAY10	DATA DELAY DEV 711 2.5 ns
U11	74AC04	
U12	LAT1016	LATTICE SEMI
U13	OPAMP−DUAL, LMC6492BEM	NATIONAL
U14	OSC\SO	80 MHz
U15−20	DS90C031	NATIONAL
U21	LM317L	
U22, U23	NC7SZ126	FAIRCHILD
L1−4	FB	FERRITE BEAD
J1	SCSI−100	
J2	HEADER10	POWER CONN
J3	SIP\8P	PROGRAM CONN
J4	LATCON	PROGRAM CONN

Digital Output Connector

The output connector is a 100 pin female SCSI type connector, pin compatible with the National Instruments PCI−1424 digital frame grabber, part number 777662−02. The interface cable is available from National Instruments, part number 185012−02.

Output 1	Pin
Data 0+	1
Data 0−	2
Data 1+	3
Data 1−	4
Data 2+	5
Data 2−	6
Data 3+	7
Data 3−	8
Data 4+	9
Data 4−	10
Data 5+	11
Data 5−	12
Data 6+	13
Data 6−	14
Data 7+	15
Data 7−	16
Data 8+	17
Data 8−	18
Data 9+	19
Data 9−	20
Data 10+	21
Data 10−	22
Data 11+	23
Data 11−	24

Output 2	Pin
Data 0+	51
Data 0−	52
Data 1+	53
Data 1−	54
Data 2+	55
Data 2−	56
Data 3+	57
Data 3−	58
Data 4+	59
Data 4−	60
Data 5+	61
Data 5−	62
Data 6+	63
Data 6−	64
Data 7+	65
Data 7−	66
Data 8+	67
Data 8−	68
Data 9+	69
Data 9−	70
Data 10+	71
Data 10−	72
Data 11+	73
Data 11−	74

Sync	Pin
Pixel+	49
Pixel−	50
Line+	43
Line−	44
Frame+	41
Frame−	42
Field Index	45
GND	99
GND	100

All other pins have no connection. All outputs are driven by low voltage differential line drivers (LVDS) except for the field index which is TTL.

Power Connector

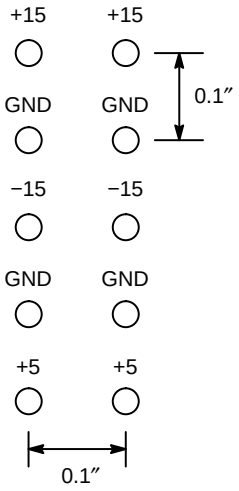


Figure 47. Power Connector Block Diagram

The evaluation board requires +15 V, −15 V, and +5 V. The current draw for each supply is:

Table 16.

Supply	Current (mA)
+15	62
−15	18
+5	780

Table 17. MODE SWITCH

Switch	ON	OFF
1	Fast Dump OFF	Fast Dump ON
2	1 Output	2 Outputs
3	−	−
4	Progressive Scan	Interlaced

When the fast dump is activated the timing dumps the first 256 lines, then reads out 512 lines of image data, and finally it dumps the last 240 lines. The resulting image is 1000 columns by 512 rows. The interlaced mode timing is not programmed to support fast dumping.

Table 18. EXPOSURE SWITCH

(All exposure times are in μs. Electronic shuttering is not programmed into the timing generator for interlaced mode.)

Exposure Setting	FD OFF: 1 Output	FD OFF: 2 Outputs	FD ON: 1 Output	FD ON: 2 Outputs
0	33,300	20,600	20,600	14,160
1	16,400	10,160	6,000	4,400
2	7,960	4,960	3,000	2,540
3	3,740	2,320	1,860	1,840
4	1,616	1,016	1,700	1,700
5	564	362	824	824
6	298	198	460	460
7	68	55	93	93

Substrate Voltage Trim

This variable resistor allows the substrate voltage to be varied from 0 V to 15 V. Adjusting this voltage will change the charge capacity and anti-blooming of the pixel photodiodes. Do not adjust the voltage below 8 V.

Evaluation Board Notes

Timing

The main timing is generated by a programmable gate array U8. The HCCD drive is setup for selectable single or dual output by inverting the H2BR and H2BL timing signals depending on the setting of the mode switch SW1.

The short pulses for ϕR, ϕT, ϕSA, and ϕSB are generated by combining (logical and/or) the outputs of the delay line U10. Each tap on U10 delays the system clock by 2.5 ns.

The amount of noise in the KAI−1020 will have a strong dependence on the stability of the timing inputs. The most sensitive inputs are the HCCD and the CDS timing inputs. The evaluation board uses one PGA (U8) to hold all of the counters and to generate the CDS timing. This is not the optimum arrangement. Though gray code counters were used, some fixed pattern column noise can be seen in the image from the counters inside U8. The counters inside U8 cause small disturbances of the HCCD and CDS timing. One solution to eliminate this noise source is to separate the counters and CDS pulse generation into two separate PGA's. One PGA would contain all of the counters for the rows and columns, and send a HCCD gating signal to a second PGA. The second PGA would output the HCCD clock as well as form the CDS timing pulses from the multi-tap delay line U10. This second PGA would contain no counters.

Output Channel

The output circuit is identical to section 0. The two op-amps U5A and U5B present an inverted signal to the ADC U4. The offset circuit will maintain the digital output of U4 at 4080 when the image sensor is in the dark. The output of U4 will be zero when the image sensor is saturated with light. The digital data is inverted by swapping the high and low outputs of the differential line drivers on the output connector.

Automatic Offset

U12 is used to control the automatic offset circuit. U8 sends a signal to U12 on the line BLKLEV when the output of the analog to digital converter corresponds to the center 10 columns of the KAI1020 dark reference. When U12 receives the signal from U8, U12 compares the outputs of the A/D converters to the number 4080. If the output is above or below 4080, U12 enables the buffers U22 and U23 and sets their inputs to cause the integrators U13A and U13B to raise or lower the offset voltages.

A separate PGA (U12) is used to monitor the output of the A/D converters. This function should not be combined with U8 into one PGA. If only one PGA is used then the digital data will cause noise in the timing outputs to the image sensor. This is especially true when the A/D outputs are near a major bit boundary, such as 2048 or 1024. At these bit boundaries there are a large number of bits changing value that would disturb the stability of the HCCD and CDS clocking.

The automatic offset updates the offset every line. This does cause some noise in the image because the offset changes slightly each line time. An improved offset circuit would measure the offset error along the entire column and then correct the offset voltage once per frame.

Oscilloscope Traces

This section contains oscilloscope traces of signals measured on the KAI−1020 pins. Some of the timing signals are not 0 to 5 V because the KAI−1020 has level shifted the signals. All signals were measured on the KAI−1020 evaluation board.

CDS Timing

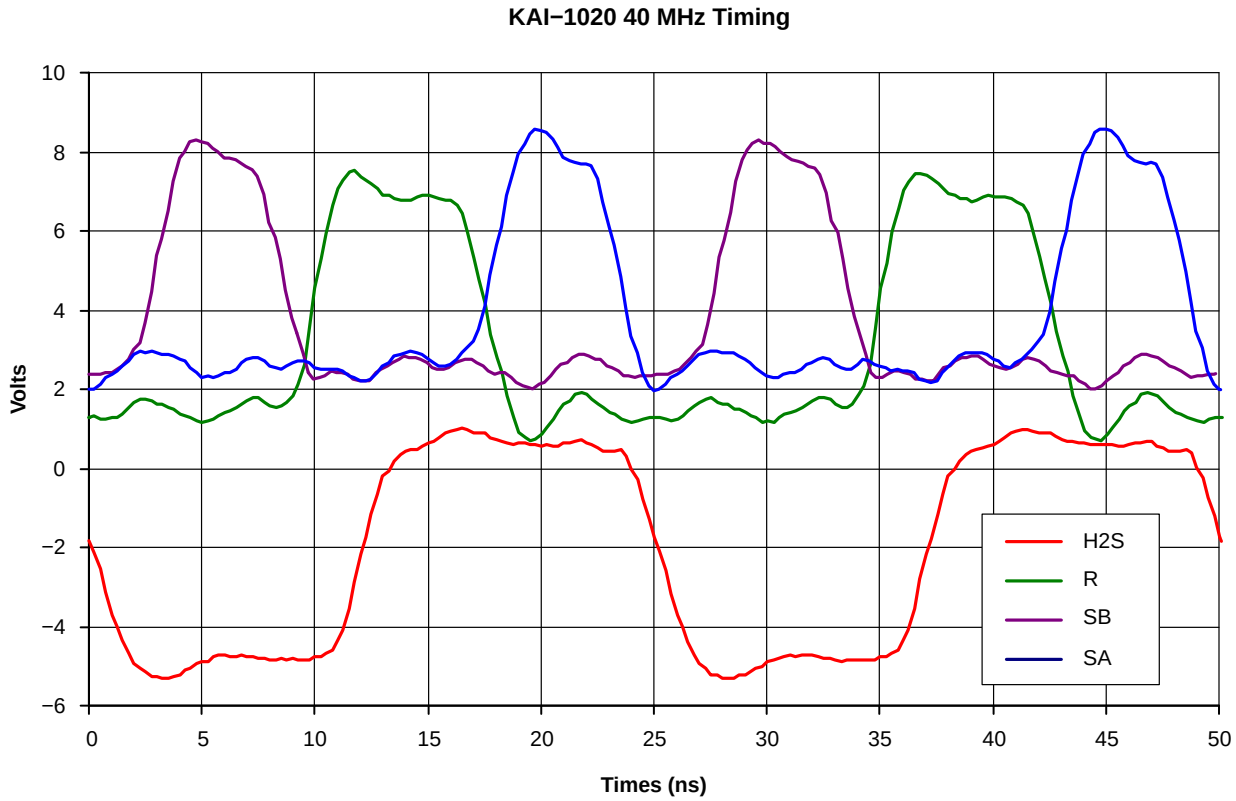


Figure 48. CDS Timing Oscilloscope Traces

Vertical Retrace

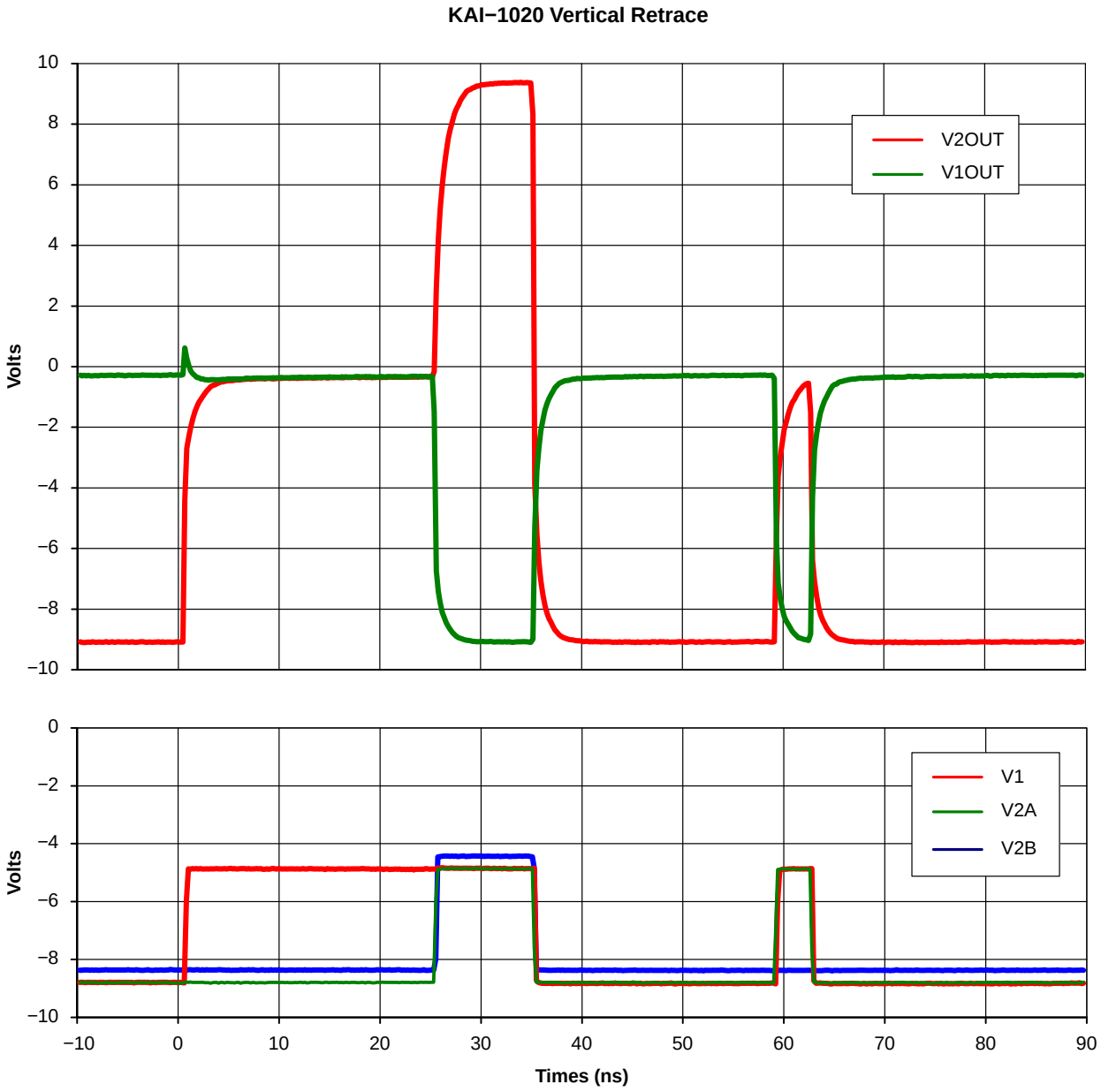


Figure 49. Vertical Retrace Oscilloscope Traces

Horizontal Retrace

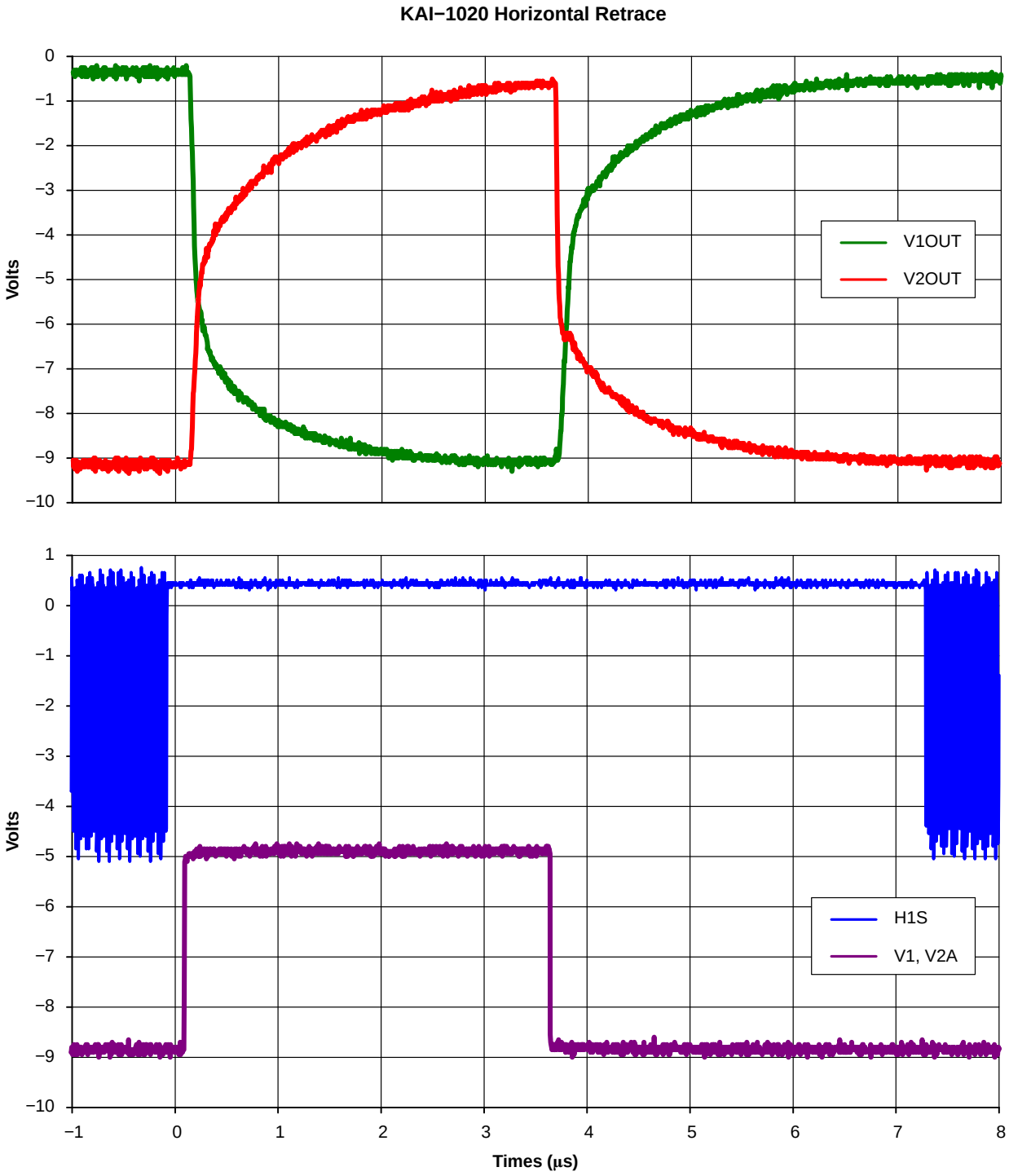


Figure 50. Horizontal Retrace Oscilloscope Traces

STORAGE AND HANDLING

Table 19. CLIMATIC REQUIREMENTS

Description	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_{ST}	−55	70	°C	1
Humidity	RH	5	90	%	2

1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

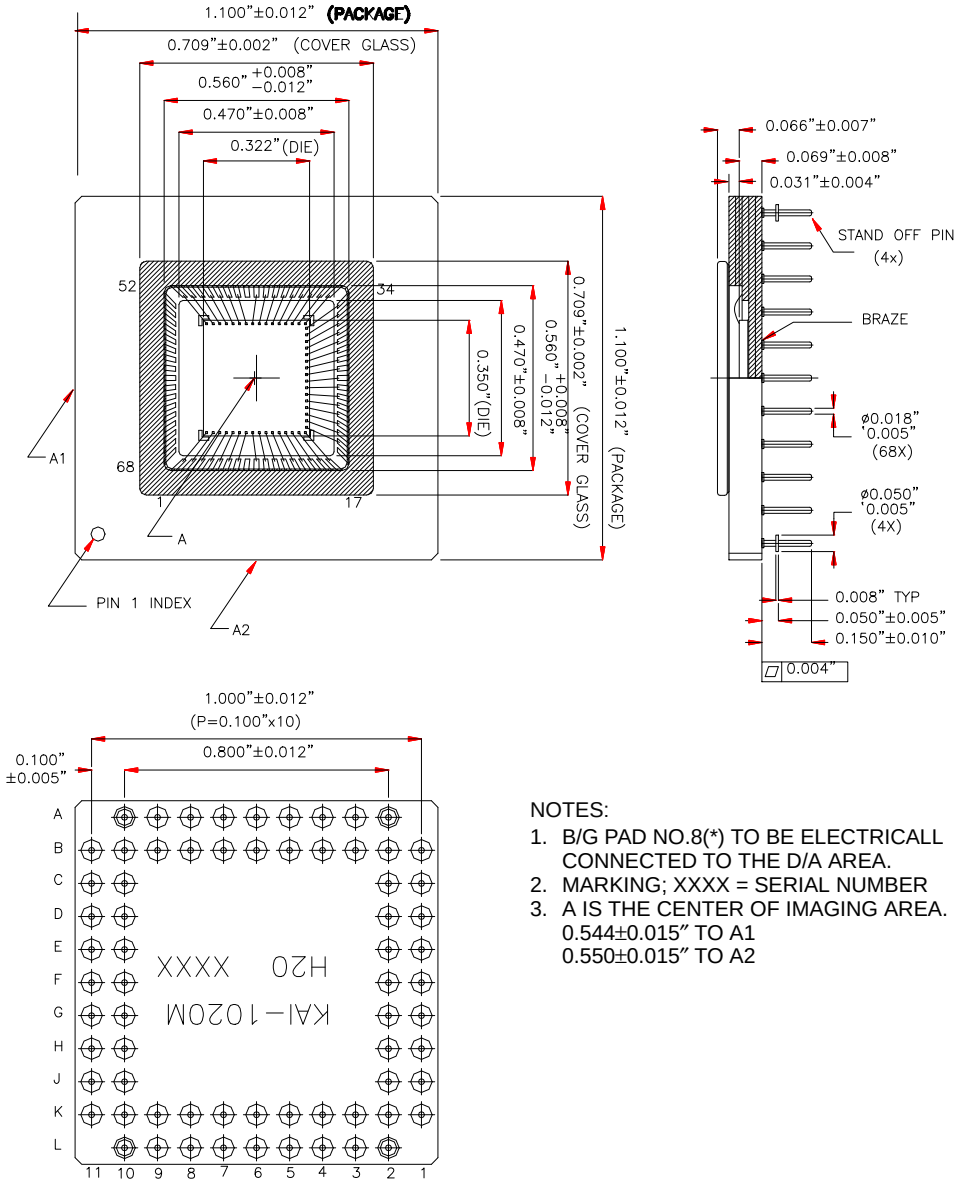
For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL DRAWINGS

Completed Assembly

Pin Grid Array



NOTES:
1. B/G PAD NO.8(*) TO BE ELECTRICALL CONNECTED TO THE D/A AREA.
2. MARKING; XXXX = SERIAL NUMBER
3. A IS THE CENTER OF IMAGING AREA.
   0.544±0.015″ TO A1
   0.550±0.015″ TO A2

Figure 51. PGA Completed Assembly

Leadless Chip Carrier

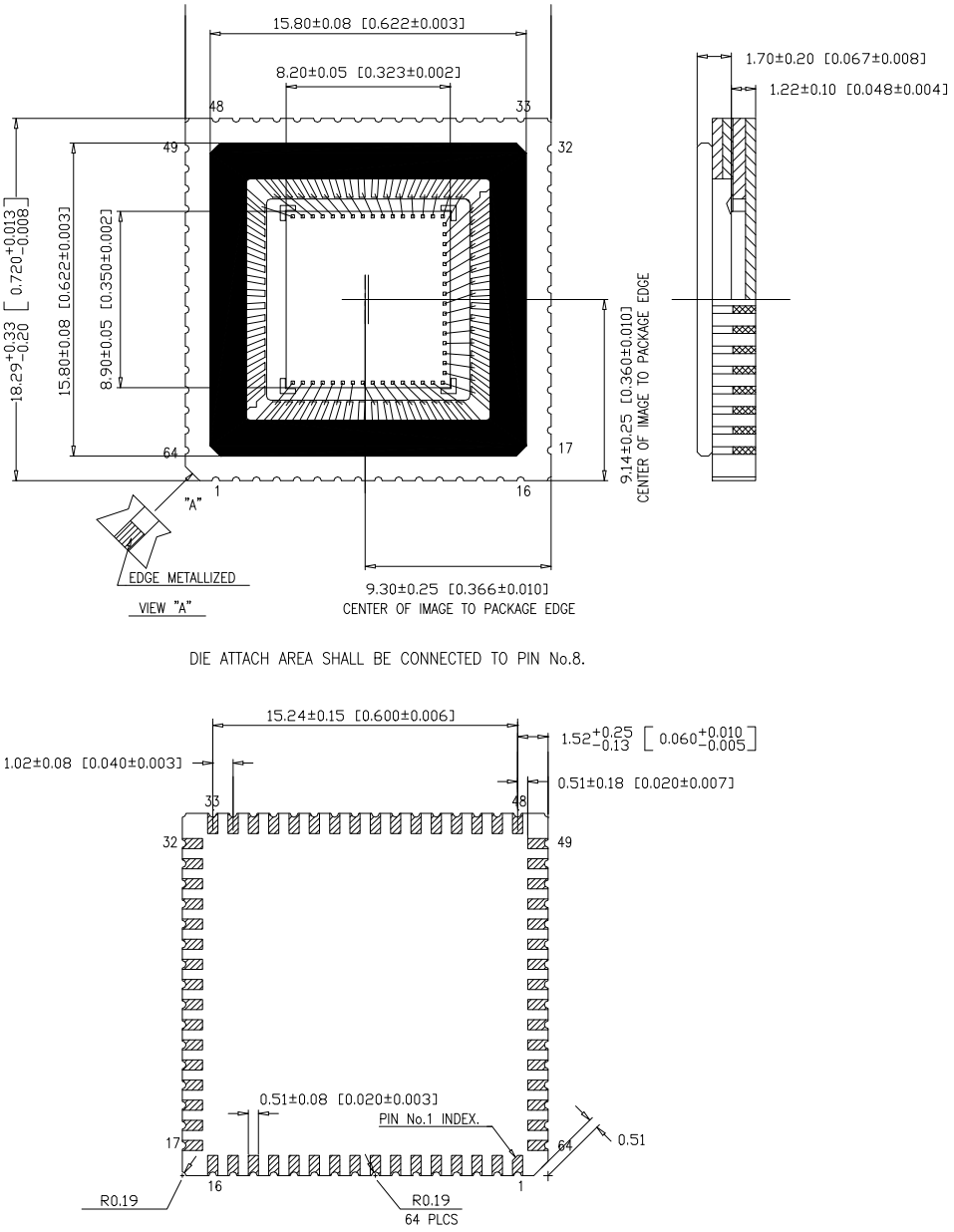


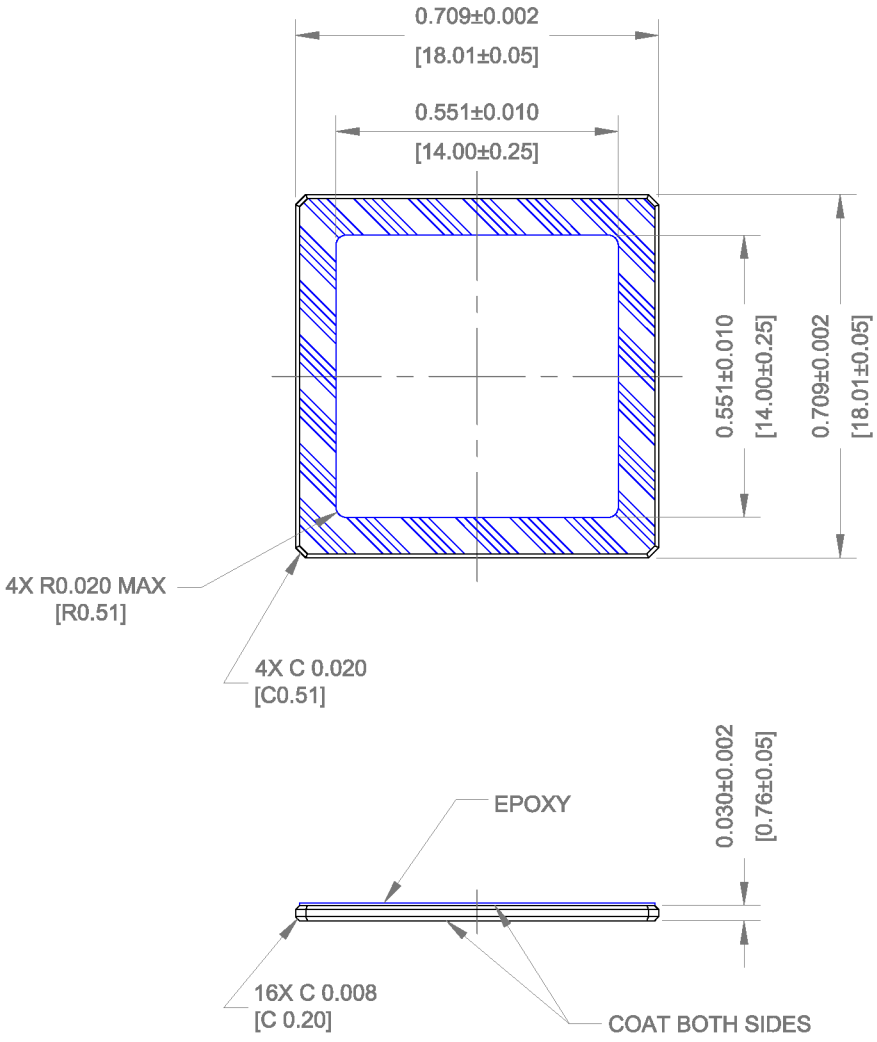
Figure 52. LCC Completed Assembly

Leadless Chip Carrier and Soldering

Care should be taken when using reflow ovens to solder the KAI−1020 to circuit boards. Extreme temperatures may cause degradation to the color filters or microlens material.

Cover Glass

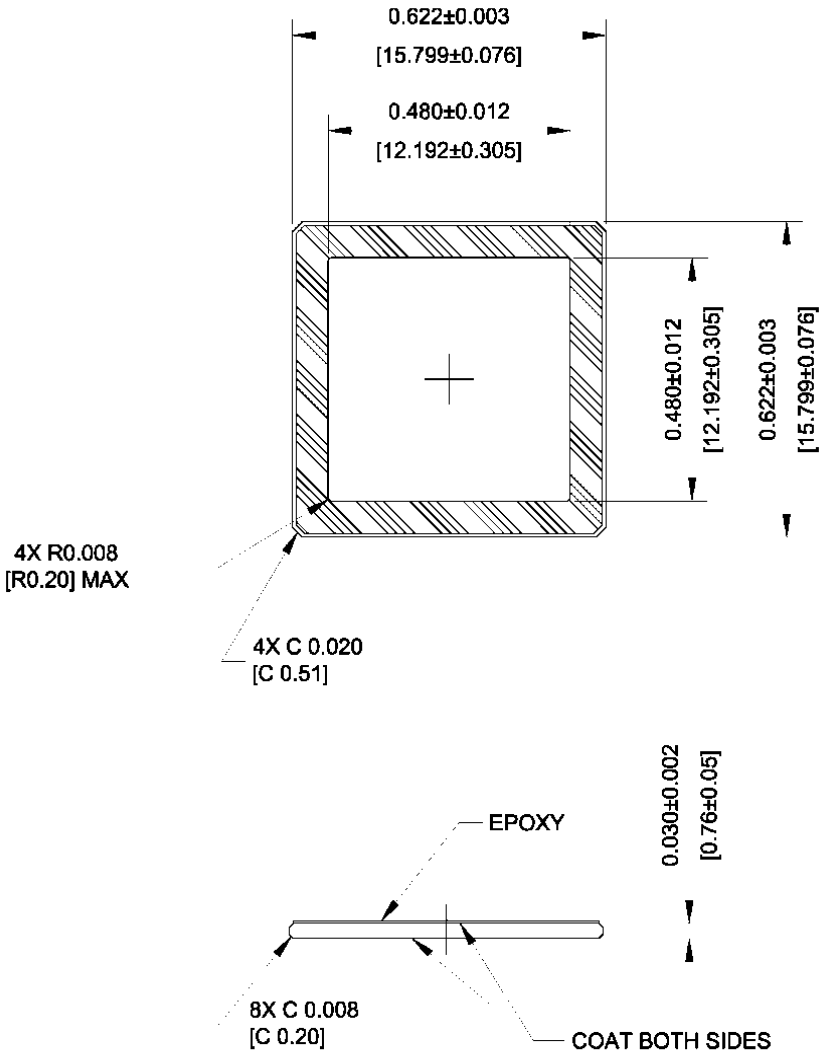
Pin Grid Array Cover Glass



NOTES:
1. Dust/Scratch 10 microns max
2. Substrate: SCHOTT D−263T eco or Equivalent
3. Epoxy: NCO−150HB
   Thickness 0.002−0.005″ [0.05−0.13]
4. Double-Side AR Coating Reflectance
   a. 420−435 nm < 2.0%
   b. 435−630 nm < 0.8%
   c. 630−680 nm < 2.0%
5. Units: IN [MM]

Figure 53. PGA Cover Glass

Leadless Chip Carrier Cover Glass



NOTES:
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3. Epoxy: NCO−150HB
   Thickness 0.002−0.005″ [0.05−0.13]
4. Double-Side AR Coating Reflectance
   a. 420−435 nm < 2.0%
   b. 435−630 nm < 0.8%
   c. 630−680 nm < 2.0%
5. Units: IN [MM]

Figure 54. LCC Cover Glass

Cover Glass Transmission

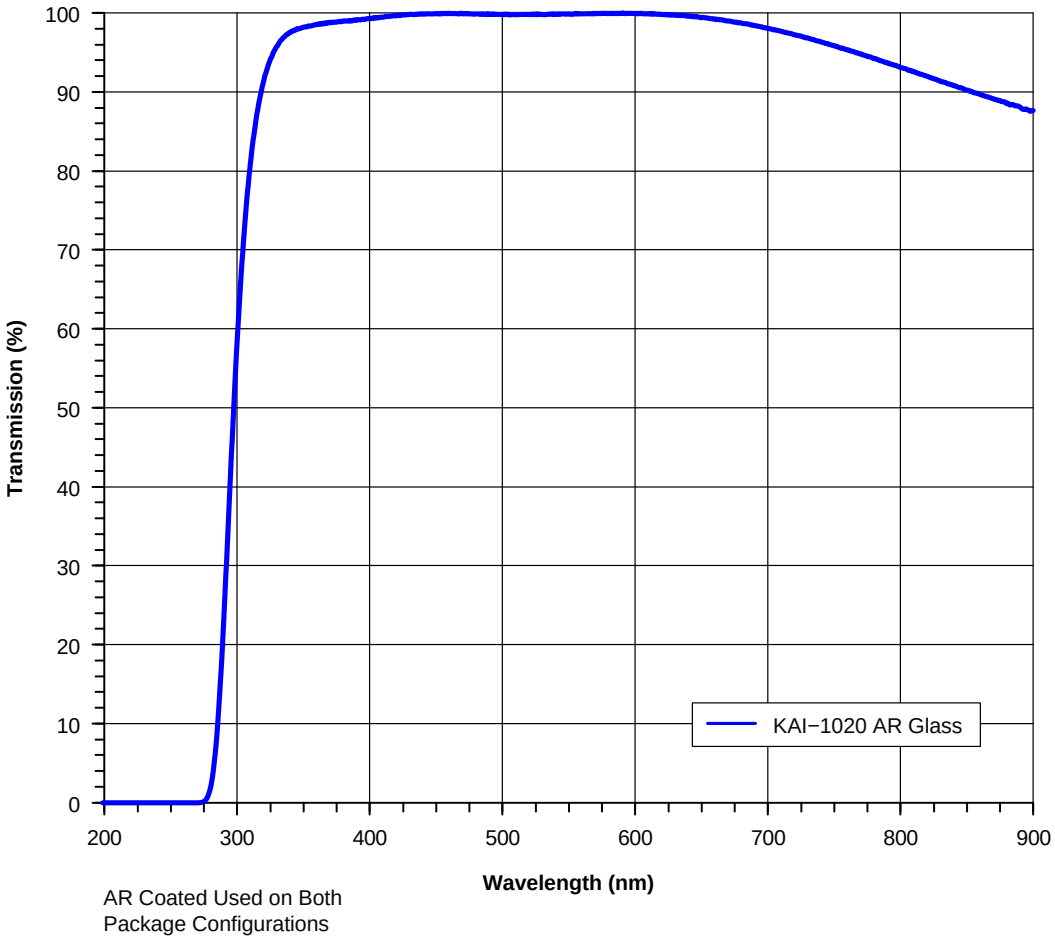

Figure 55. Cover Glass Transmission

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