LED Drivers for LCD Backlights

White LED Driver for large LCD Panels (DCDC Converter type)

BD9483F,FV

●General Description

BD9483F,FV is a high efficiency driver for white LEDs and designed for large LCDs. This IC is built-in 2ch boost DCDC converters that employ an array of LEDs as the light source. BD9483F,FV has some protect function against fault conditions, such as the over-voltage protection (OVP), the over current limit protection of DCDC (OCP), Max duty protection, LED OCP protection. Therefore BD9483F,FV is available for the fail-safe design over a wide range output voltage.

●Key Specification

- Operating power supply voltage range: 11.0V to 35.0V
- Oscillator frequency: 150kHz (RT=100kΩ)
- Operating Current: 3mA (typ.)
- Operating temperature range: -40°C to +85°C

●Applications

TV, Computer Display, Notebook, LCD Backlighting

●Features

- 2ch boost DCDC converter with current mode
- LED protection circuit (Max duty protection, LED OCP protection)
- Over-voltage protection (OVP) for the output voltage Vout
- Adjustable soft start
- The wide range of analog dimming 0.2V-3.0V
- 2ch independent PWM dimming input
- The UVLO detection for the input voltage of the power stage
- FAIL logic output

●Package

	W(Typ.)	D(Typ.)	H(Max.)
SOP-24:	15.00mm	x 7.80mm	x 2.01mm
Pin Pitch:			1.27mm

Figure 2-1. SOP-24

	W(Typ.)	D(Typ.)	H(Max.)
SSOP-B24:	7.80mm	x 7.60mm	x 1.35mm
Pin Pitch:			0.65mm

Figure 2-2. SSOP-B24

●Typical Application Circuit

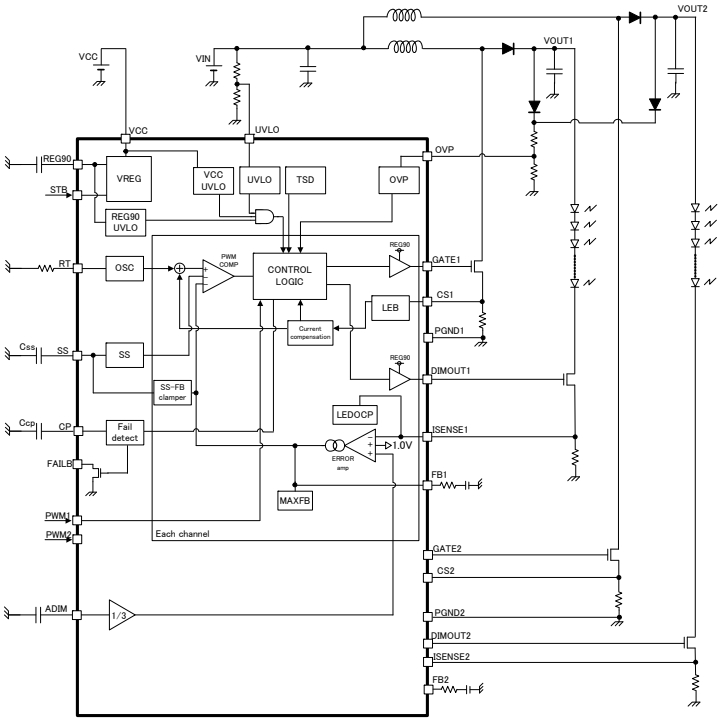


Figure 1. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●**Absolute maximum ratings** (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Operating Temperature Range	Ta(opr)	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Power Dissipation *1 (SOP24)	Pd1	687	mW
Power Dissipation *2 (SSOP-B24)	Pd2	1024	mW

*1 In the case of mounting 1 layer glass epoxy base-plate of 70mm×70mm×1.6mm, 5.5mW is reduced at 1°C above Ta=25°C.

*2 In the case of mounting 1 layer glass epoxy base-plate of 70mm×70mm×1.6mm, 8.2mW is reduced at 1°C above Ta=25°C

●**Operating Ratings** (Ta = 25°C)

Parameter	Symbol	Range	Unit
Power supply voltage	VCC	11.0 to 35.0	V
DC/DC oscillation frequency	fsw	50 to 800	kHz
The effective range of ADIM signal	VADIM	0.2 to 3.0	V
PWM input frequency	FPWM	40 to 50k	Hz

The operating conditions written above are constants of the IC unit. Be careful enough when setting the constant in the actual set.

●**External Components Recommended Range**

Item	Symbol	Setting Range	Unit
REG90 pin connection capacitance	CREG90	1.0 to10	μF
Soft start connection capacitance	CSS	0.001 to 4.7	μF
RT pin connection resistance	RRT	15 to 300	kΩ
The assumed capacitance of GATE pin	CGATE	to 1000	pF

The values described above are constants for a single IC. Adequate attention must be paid to setting of a constant for an actual set of parts

●**Pin Configuration**

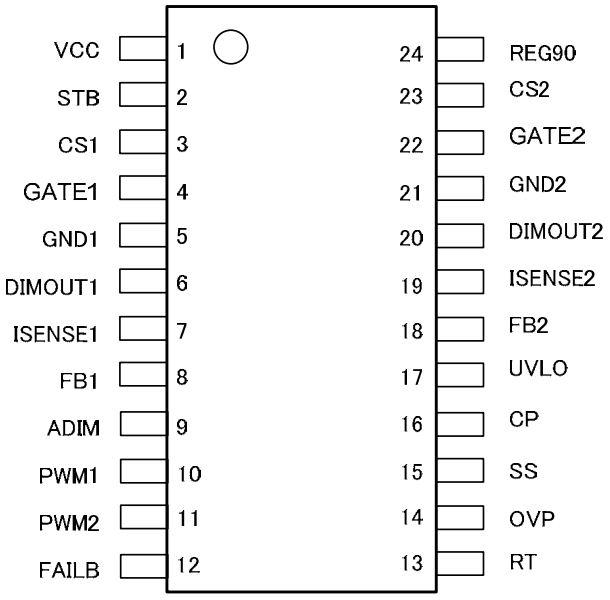


Figure 3.

●**Physical Dimension Tape and Marking Diagram**

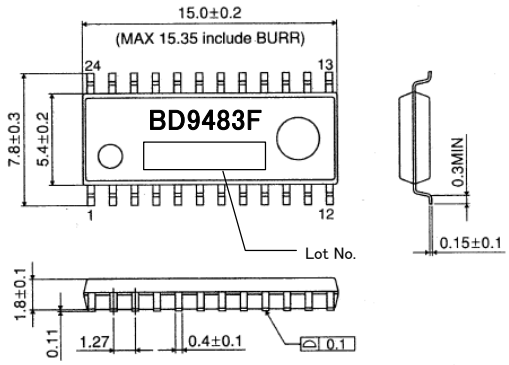


Figure 4-1. SOP-24

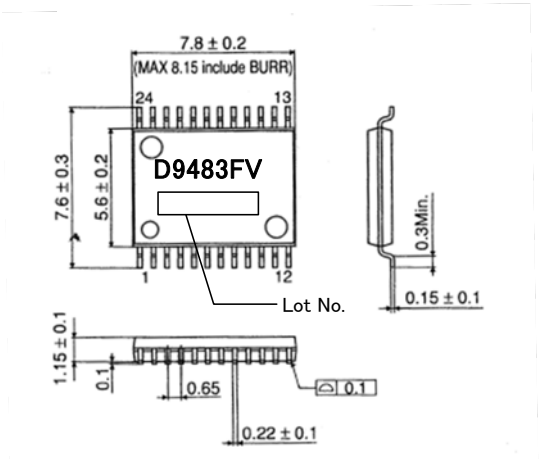


Figure 4-2. SSOP-B24

●**1.1 Electrical Characteristics 1**(Unless otherwise specified, Ta=25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Total current consumption】						
Circuit current	Icc	−	3	6	mA	VSTB=3V
Circuit current (stand-by)	Ist	−	25	50	μA	VSTB=0V
【UVLO block】						
Operation voltage（VCC）	VUVLO_VCC	6.0	7.0	8.0	V	VCC=SWEEP UP
Hysteresis Voltage（VCC）	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO release voltage	VUVLO	2.91	3.00	3.09	V	VUVLO=SWEEP UP
UVLO hysteresis voltage	VUHYS	150	200	250	mV	VUVLO=SWEEP DOWN
UVLO pin leak current	UVLO_LK	-2	0	2	μA	VUVLO=4V
【DC/DC block】						
ISENSE threshold voltage 1	VLED1	0.225	0.233	0.242	V	VADIM=0.7V
ISENSE threshold voltage 2	VLED2	0.988	1.000	1.012	V	VADIM=3.0V
ISENSE threshold voltage 3	VLED3	0.989	1.015	1.040	V	VADIM=3.3V
Oscillation frequency	FCT	142.5	150	157. 5	KHz	RT=100kohm
GATE pin MAX DUTY output	NMAX_DUTY	90	95	99	%	RT=100kohm
GATE pin ON resistance (as source)	RONSO	2.0	4.0	8.0	Ω	ION=-10mA
GATE pin ON resistance (as sink)	RONSI	1.2	2.5	5.0	Ω	ION=10mA
SS pin source current	ISSSO	-3.75	-3.0	-2.25	μA	VSS=2V
SS pin ON resistance	RSS_L	-	3.0	5.0	kΩ	VSTB=0V, Ioss=50uA
Soft start ended voltage	VSS_END	3.6	4.0	4.4	V	SS=SWEEP UP
FB source current	IFBSO	-115	-100	-85	μA	VISENSE=0.2V, VADIM=3.0V, VFB=1.0V
FB sink current	IFBSI	85	100	115	μA	VISENSE=2.0V, VADIM=3.0V, VFB=1.0V
OCP detect voltage	VCS	360	400	440	mV	CS=SWEEP UP
【DC/DC protection block】						
OVP detect voltage	VOVP	2.88	3.00	3.12	V	VOVP SWEEP UP
OVP detect hysteresis	VOVP_HYS	50	100	150	mV	VOVP SWEEP DOWN
OVP pin leak current	OVP_LK	-2	0	2	μA	VOVP=4V

●**1.2 Electrical Characteristics 2**(Unless otherwise specified, Ta=25°C, VCC=24V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【LED protection block】						
LED OCP detect voltage	VLEDOCP	2.88	3.0	3.12	V	VISENSE=SWEEP UP
MAX duty detect voltage	VFBMAX	3.84	4.0	4.16	V	VFB=SWEEP UP
【Dimming block】						
ADIM pin leak current	ILADIM	-2	0	2	μA	VADIM=2.0V
ISENSE pin leak current	IL_ISENSE	-2	0	2	μA	VISENSE=4V
DIMOUT source on-resistance	RONSO	4.0	8.0	16.0	Ω	ION=-10mA
DIMOUT sink on-resistance	RONSI	2.5	5.0	10.0	Ω	ION=10mA
【REG90 block】						
REG90 output voltage	VREG90	8.91	9.00	9.09	V	IO=0mA,VCC>11V
REG90 available current	|IREG90|	15	-	-	mA	
REG90_UVLO detect voltage	REG90_TH	5.4	6.0	6.6	V	REG90=SWEEP DOWN
REG90_UVLO hysteresis	REG90_HYS	250	500	750	mV	VSTB=H->L, REG90=SWEEP UP
REG90 discharge resistance	REG90_DIS	325	500	675	kΩ	VSTB=H->L, REG90=9.0V
【STB block】						
STB pin HIGH voltage	STBH	2.0	-	35	V	VSTB=SWEEP UP
STB pin LOW voltage	STBL	-0.3	-	0.8	V	VSTB=SWEEP DOWN
STB pull down resistor	ISTB	600	1000	1400	kΩ	VSTB=3.0V
【PWM block】						
PWMx pin HIGH Voltage	PWM_H	2.0	-	5.5	V	VPWMx=SWEEP UP
PWMx pin LOW Voltage	PWM_L	-0.3	-	0.8	V	VPWMx=SWEEP DOWN
PWMx pin Pull Down resistance	RPWM	600	1000	1400	kΩ	VPWMx=3.0V
【FAIL block (OPEN DRAIN)】						
FAILB pin on-resistance	RFAIL	250	500	1000	Ω	VFAIL=1.0V
FAILB pin leak current	ILFAIL	-2	0	2	μA	VFAIL=15V
CP detect voltage	VCP	2.85	3.0	3.15	V	VCP=SWEEP UP
CP charge current	ICP	2.7	3.0	3.3	μA	

●1.3 Pin Descriptions

Pin No	Pin Name	In/Out	Function	Rating [V]
1	VCC	-	Power supply pin	-0.3 to 36
2	STB	In	IC ON/OFF pin	-0.3 to 36
3	CS1	In	DC/DC output current detect pin for ch1,OCP input pin for ch1	-0.3 to 7
4	GATE1	Out	DC/DC switching output pin for ch1	-0.3 to 14
5	GND1	-	Ground for ch1	-
6	DIMOUT1	Out	Dimming signal output for NMOS for ch1	-0.3 to 14
7	ISENSE1	In	Current detection input pin for ch1	-0.3 to 7
8	FB1	Out	Error amplifier output pin for ch1	-0.3 to 7
9	ADIM	In	ADIM signal input-output pin	-0.3 to 20
10	PWM1	In	External PWM dimming signal input pin ch1	-0.3 to 20
11	PWM2	In	External PWM dimming signal input pin ch2	-0.3 to 20
12	FAILB	Out	Abnormality detection output pin	-0.3 to 36
13	RT	Out	For DC/DC switching frequency setting pin	-0.3 to 7
14	OVP	In	Over voltage protection detection pin	-0.3 to 20
15	SS	Out	Slow start setting pin	-0.3 to 7
16	CP	Out	Charge timer for abnormal state.	-0.3 to 7
17	UVLO	In	Under voltage lock out detection pin	-0.3 to 20
18	FB2	Out	Error amplifier output pin for ch2	-0.3 to 7
19	ISENSE2	In	Current detection input pin for ch2	-0.3 to 7
20	DIMOUT2	Out	Dimming signal output for NMOS for ch2	-0.3 to 14
21	GND2	-	Ground for ch2	-
22	GATE2	Out	DC/DC switching output pin for ch2	-0.3 to 14
23	CS2	In	DC/DC output current detect pin for ch2,OCP input pin for ch2	-0.3 to 7
24	REG90	Out	9.0V output voltage	-0.3 to 14

●1.4.1 Pin ESD Type1

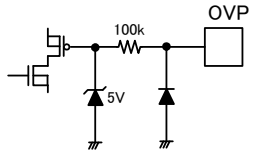
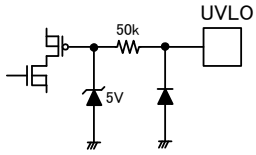
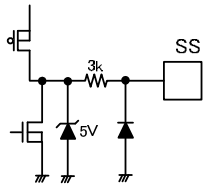
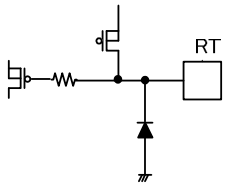
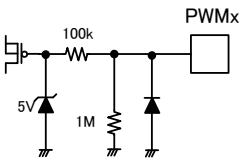
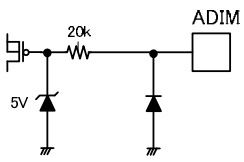
OVP	UVLO	SS
		
RT	**PWM1 / PWM2**	**ADIM**
		

Figure 5. Pin ESD Type

●1.4.2 Pin ESD Type2

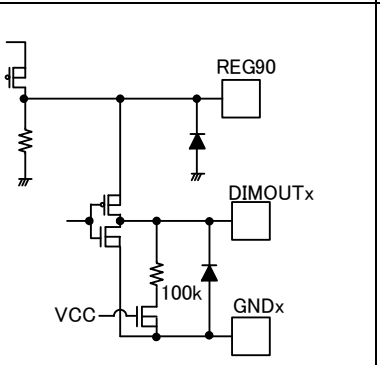
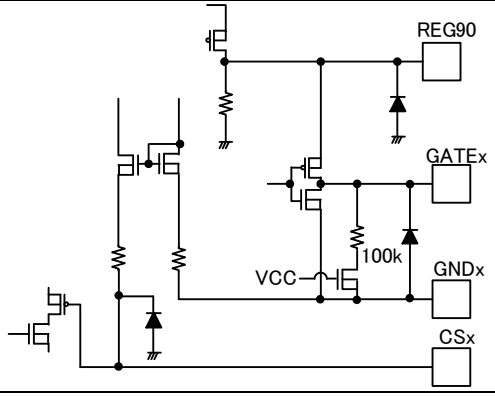
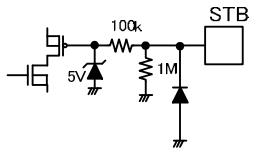
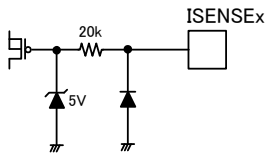
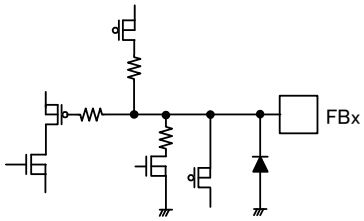
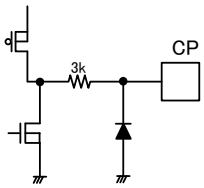
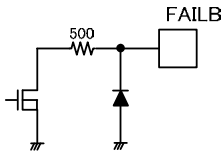
DIMOUT1 / DIMOUT2 / REG90	GATE1 / GATE2 / REG90 / CS1 / CS2	STB
		
ISENSE1 / ISENSE2	**FB1 / FB2**	**CP**
		
FAILB		
		

Figure 6. Pin ESD Type

●1.5 Typical Performance Curves (Reference data)

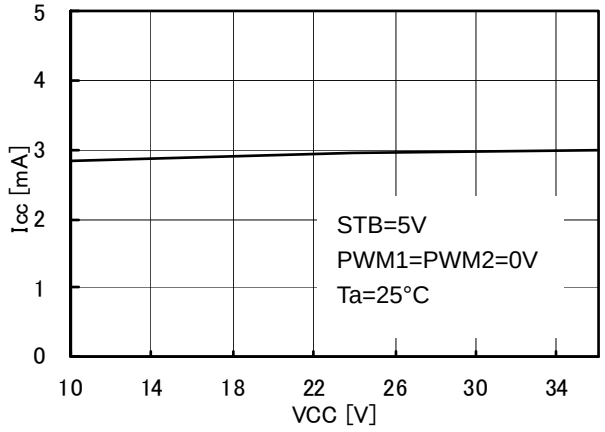


Figure 7. Circuit current (operating mode)

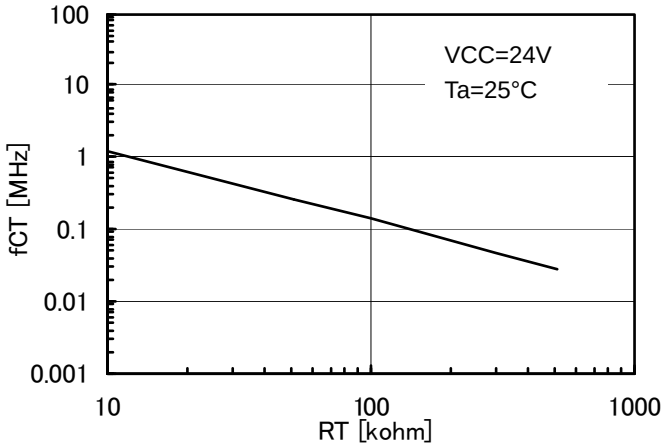


Figure 8. fCT v.s. RT

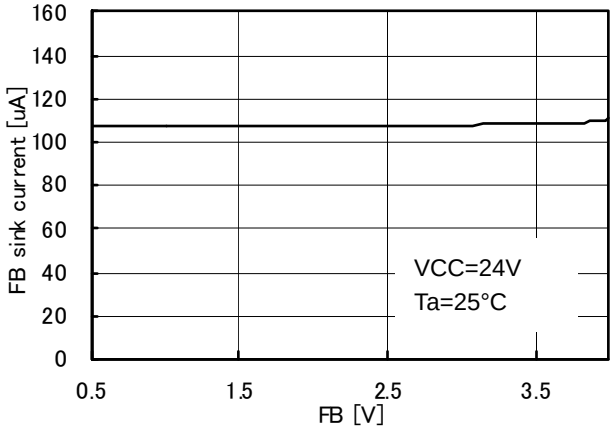


Figure 9. FB sink current v.s. FB voltage

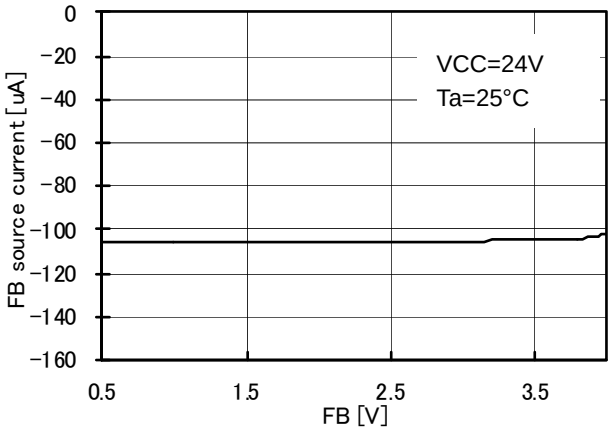


Figure 10. FB source current v.s. FB voltage

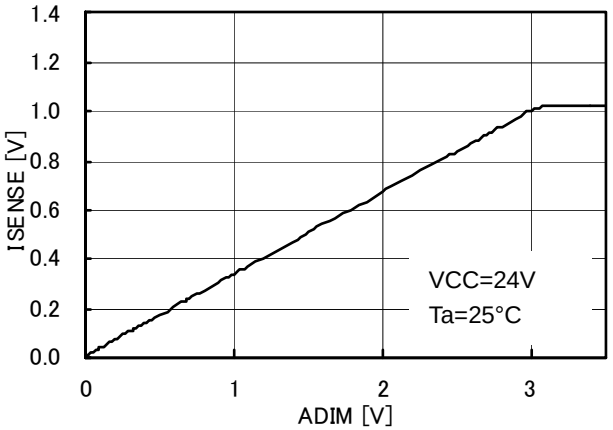


Figure 11. ISENSE feedback voltage v.s. ADIM

●2 Block Diagram

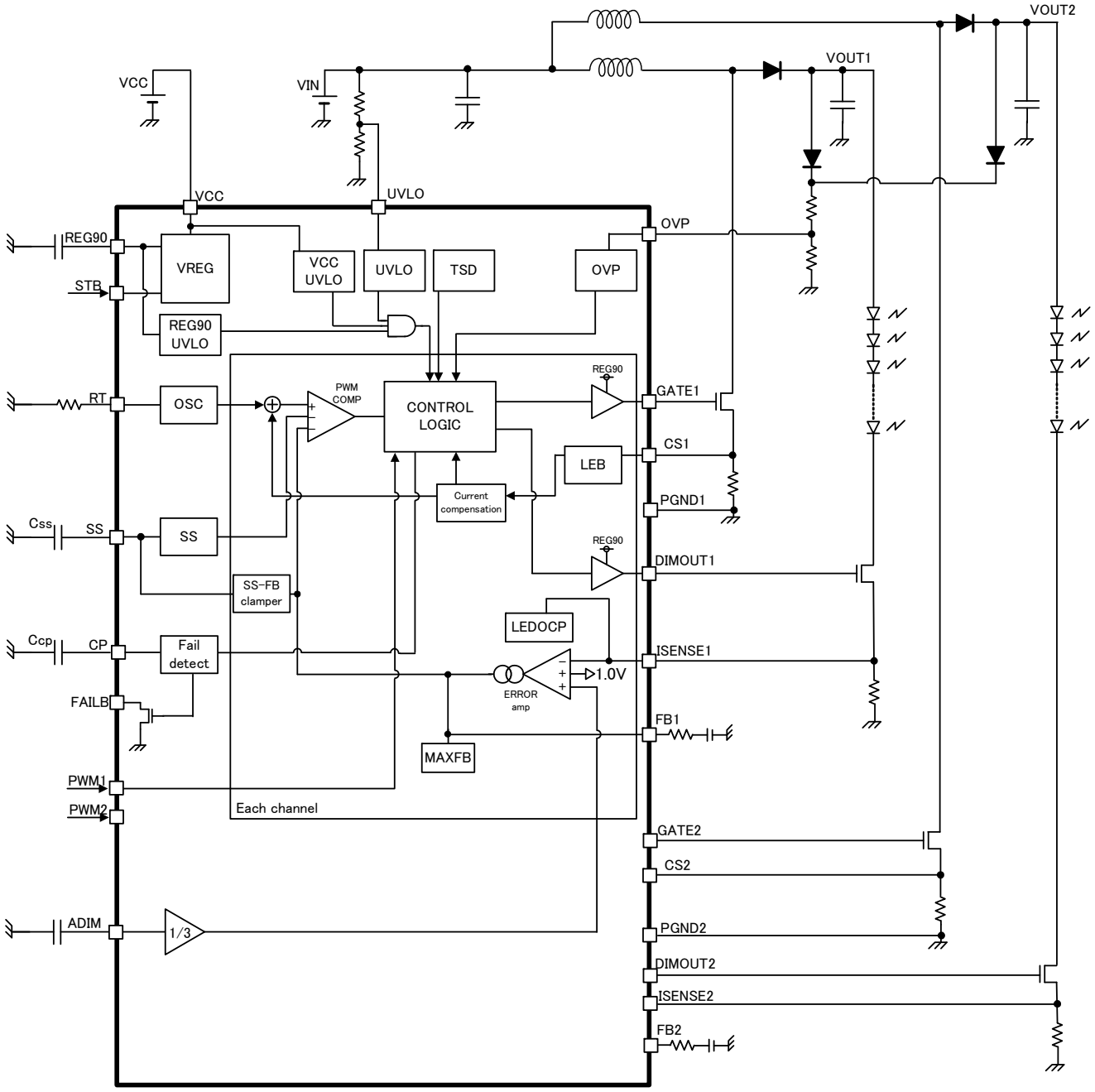


Figure 12. Block Diagram

●3.1 Pin Function

VCC（1 PIN）

Power supply pin of IC. Input range is from 11V to 35.0V.
The operation starts more than 7.0V(typ.) and shuts down less than 6.7V(typ.) by VCCUVLO.
In the lower VCC than 7.6V(typ.), IC stops switching by REG90UVLO, which detect the lower voltage of VCC earlier than VCCUVLO.

STB（2 PIN）

STB can be used to perform the reset of latch off or soft start. The power control of REG90 is depend on STB pin and the VCCUVLO.
Regarding of the sequence of turning on, after the positive edge of PWM is input, BD9483F,FV starts the boost operation and the soft start.
The input voltage of STB pin toggles the IC state(IC ON/OFF). Please avoid the use of the intermediate level (from 0.8V to 2.0V).

CS1（3 PIN）, CS2 (23 PIN)

The CS pin has two functions.
1. DC / DC current mode Feedback terminal
The inductor current is converted to the CS pin voltage by the sense resistor R_{CS} and this CS pin voltage controls the gate duty.

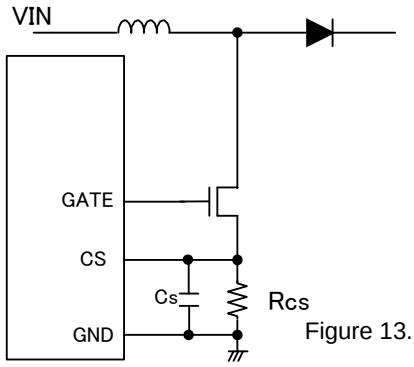


Figure 13.

2. Inductor current limit (OCP) terminal
The CS terminal also has an over current protection (OCP), if it voltage is more than 0.4V, the switching operation will be stopped compulsorily. And the next boost pulse will be restart in normal frequency.
If the capacitance Cs in the right Figure is increased to a micro orders, please be careful that the limited value of NMOS drain current Id is much than the simple calculation. Because the current Id flow not only Rcs but also Cs, as the CS pin voltage move according to Id.
Both of above functions are enable after 300ns (typ.) when GATE pin asserts high, because the leading Edge Blanking function is included into this IC to prevent the noise affection. Please refer to the section "**●3.5.1** how to set OCP / the calculation method for the current rating of DCDC parts", for detail explanation.

GATE1（4 PIN）, GATE2 (22 PIN)

This is the output terminal for driving the gate of the boost MOSFET. The high level is REG90 of IC. Frequency can be set by the resistor connected to RT. Please refer to the <RT> pin description for the frequency setting.
In the condition of approximately VCC<9.8V, the high level of the GATE pin is about VCC-0.8V, which lower than 9.0V.
The phase lag of GATE1 and GATE2 is shown in Figure below. This Figure illustrates the waveform as both GATE pin output the maximum duty. The inrush current of the VIN terminal can be suppressed because each channel turns on alternately.

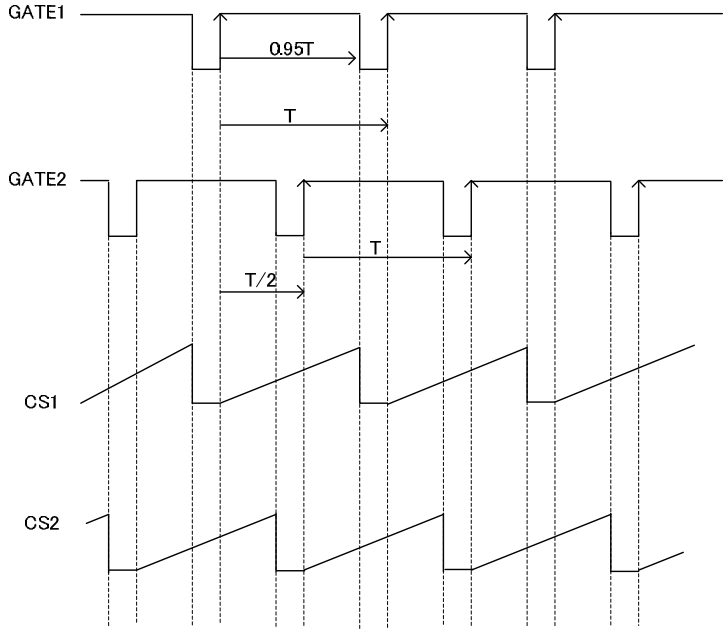


Figure 14.

GND1（5 PIN）, GND2 (21 PIN)

GND pin of IC. GND1 is the ground pin of channel 1.

DIMOUT1 (6 PIN), DIMOUT2 (20 PIN)

This is the output pin for external NMOS of dimming. The below table shows the rough output logic of each operation state, and the output H level is REG90. DIMOUT1 and DIMOUT2 are the output corresponding to PWM1 and PWM2. Please refer to the time chart in the section 3.7 for detail explanations, because The DIMOUT logic has the exceptional behavior. Please insert the resistance between the dimming MOS gate to improve the over shoot of LED current, as PWM turns from low to high.

Status	DIMOUT1 output	DIMOUT2 output
Normal	PWM1	PWM2
Abnormal	Low Level	Low Level

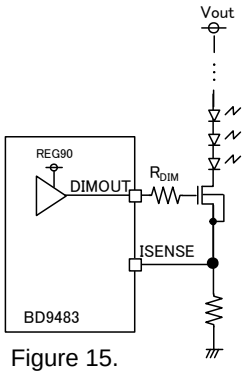


Figure 15.

ISENSE1 (7 PIN), ISENSE2 (19 PIN)

This is the input terminal for the current detection. The error amplifier compares the ISENSE and the 1/3 of ADIM pin voltage. And the clamped level of ISENSE feedback is 1.0V.

○LED OCP Protection Function

More than ISENSE = 3.0V (typ.), the over current of LED (LEDOCP) will be detected. The GATE pulse will be stopped, the DIMOUT is forced to output high level to monitor the error state. If the detection continues to 4 count of GATE frequency, IC will be latched off. (Please refer to the time chart **3.7.6**)

FB1 (8 PIN), FB2 (18 PIN)

This is the output terminal of error amplifier. The input pin of error amplifier is ISENSE and ADIM.

After the completion of the soft start, this pin outputs high impedance as the corresponding PWM pin asserts low. FB voltage is hold to the external capacitance.

○FBMAX Protection Function

More than FB = 4.0V (typ.), the error state for the GATE pin duty will be detected, and the CP charge is started. If the CP charge continues to 3.0V, IC will be latched off. Please refer to the time chart **3.7.5**

(The loop compensation setting is described in the section " ●**3.6** loop compensation".)

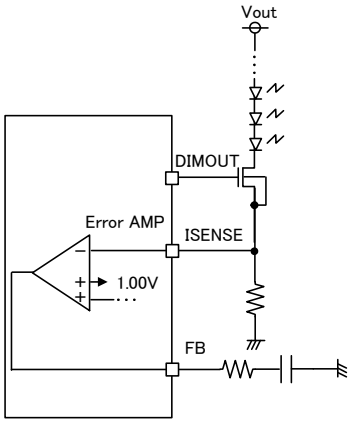


Figure 16.

ADIM (9 PIN)

The input pin for analog dimming signal. The ISENSE feedback point is set as 1/3 of this pin bias. If more than 3.0V is input, ISENSE threshold is clamped as the below diagram.

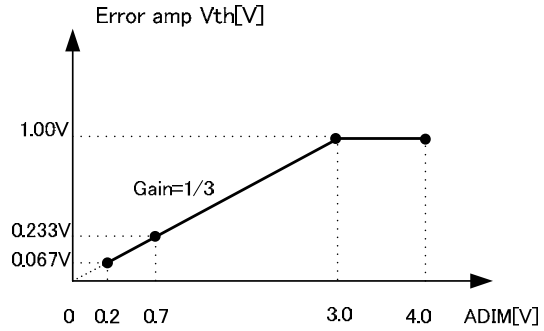


Figure 17.

PWM1 (10 PIN), PWM2 (11 PIN)

The ON / OFF input of the LED light. PWM1 and PWM2 controls each LED strings individually. The Duty signal of this pin can control the PWM dimming.

The high / low level of PWM pins are following.

State	PWM input voltage
PWMx=H	PWMx=2.0V to 5.5V
PWMx=L	PWMx=-0.3V to 0.8V

FAILB (12 PIN)

FAIL signal output pin (open drain). As abnormal, the internal NMOS turn on.

Status	FAILB output
Normal	OPEN
Abnormal	GND Level

RT（13 PIN）

DC/DC switching frequency setting pin. RT set the oscillation frequency inside IC.

○The relationship between the frequency and RT resistance value **(ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

The oscillation setting range from 50kHz to 800kHz.

The setting examples is separately described in the section " **●3.4.4 how to set DCDC oscillation frequency**"

OVP（14 PIN）

The OVP terminal is the input for over-voltage protection. As OVP is more than 3.0V, the over-voltage protection (OVP) will work. At the moment of these detections, the BD9483F,FV stops the switching of the output GATE and starts to count up the abnormal interval, but IC doesn't reach latch off state instantaneously until the detection continues up to 4 counts of GATE terminals. (Please refer to the time chart **3.7.4**)

As the latch off by OVP, both channels stop. (GATE1=GATE2=L, DIMOUT1=DIMOUT2=L)

The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.

The setting examples is separately described in the section "**●3.4.6** how to set OVP"

SS（15 PIN）

The pin which sets soft start interval of DC/DC converter. It performs the constant current charge of 3.0 μA to external capacitance Css(0.001μF to 4.7μF). The switching duty of GATE output will be limited during 0V to 4.0V of the SS voltage.

So the equality of the soft start interval can be expressed as following

Tss = 1.33*10^6*Css **Css: the external capacitance of the SS pin**.

Regarding of the logic of SS=L

(SS=L) = (PWM1orPWM2 have not asserted H since ResetB=L->H) or (latch off state)

where ResetB = (STB=H) and (VCCUVLO=H) and (REG90UVLO=H)

Please refer to the time chart **3.7.3** on soft start behavior

CP（16 PIN）

Timer pin for counting the abnormal state of the FBMAX protection. If the abnormal state is detected, The CP pin start charging by 3μA to the external capacitance. As the CP voltage reaches to 3.0V, IC will be latched off. In latch off both channels will be stopped (GATE1=GATE2=L, DIMOUT1=DIMOUT2=L).

Please refer to the section "**●3.4.7** how to set the interval until latch off (CP pin)" for more detail.

UVLO（17 PIN）

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts the boost operation and stops lower than 2.8V(typ.).

The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.

So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.

As the latch off by UVLO, both channels stop. (GATE1=GATE2=L, DIMOUT1=DIMOUT2=L)

The setting examples is separately described in the section "**●3.4.5** how to set UVLO"

REG90（24 PIN）

This is the 9.0V (typ.) output pin that is used for the power supply of DIMOUT, GATE. Available current is 15mA (min.).

When VCC<11V , REG90 output voltage decreases because of the saturation.

●3.2 The detection condition list of the protection (TYP. Condition)

Protection	Detection pin	Detect condition			Release condition	Timer operation	Protection type
		pin condition	PWM	SS			
FBMAX	FB	FB > 4.0V	H(8clk)	SS>4.0V	FB < 4.0V	CP charge	Latch off
LED OCP	ISENSE	ISENSE > 3.0V	-	-	ISENSE < 3.0V	4clk	Latch off
UVLO	UVLO	UVLO<2.8V	-	-	UVLO>3.0V	NO	Auto recovery
REG90UVLO	REG90	REG90<6.0V	-	-	REG90>6.5V	NO	Auto recovery
VCC UVLO	VCC	VCC<6.7V	-	-	VCC>7.0V	NO	Auto recovery
OVP	OVP	OVP>3.0V	-	-	OVP<2.9V	4clk	Latch off
OCP	CS	CS>0.4V	-	-	-	NO	Pulse by Pulse

To reset the latch type protection, please input of STB logic to 'L' once. Otherwise the detection of VCCUVLO, REG90UVLO is required.
In the latch off mode, both channels will be stopped. (GATE1=GATE2=L, DIMOUT1=DIMOUT2=L)
The clock number of timer operation is the correspond to the boost pulse clock.

●3.3 The behavior list of the protection

Protect Function	The operation of the protection			
	DC/DC Gate output	Dimming transistor (DIMOUT) logic	SS pin	FAILB pin (NORMAL=open)
FBMAX	Stops after latch	L after latch	discharge after latch	L after latch
LED OCP	Stops immediately	H immediately, L after latch	discharge after latch	L after latch
STB	Stops immediately	L after REG90UVLO detects	discharge immediately	OPEN
UVLO	Stops immediately	immediately L	discharge immediately	Low
REG90UVLO	Stops immediately	immediately L	discharge immediately	OPEN
VCC UVLO	Stops immediately	immediately L	discharge immediately	Low
OVP	Stops immediately	immediately L	discharge after latch	L after latch
OCP	Stops immediately	Normal operation	Not discharge	OPEN

Please refer to the timing chart for the detail.

•3.4 External components selection

•3.4.1 The start up operation and the setting of Soft Start external capacitance

The below explanations are the start up sequency of BD9483F,FV.

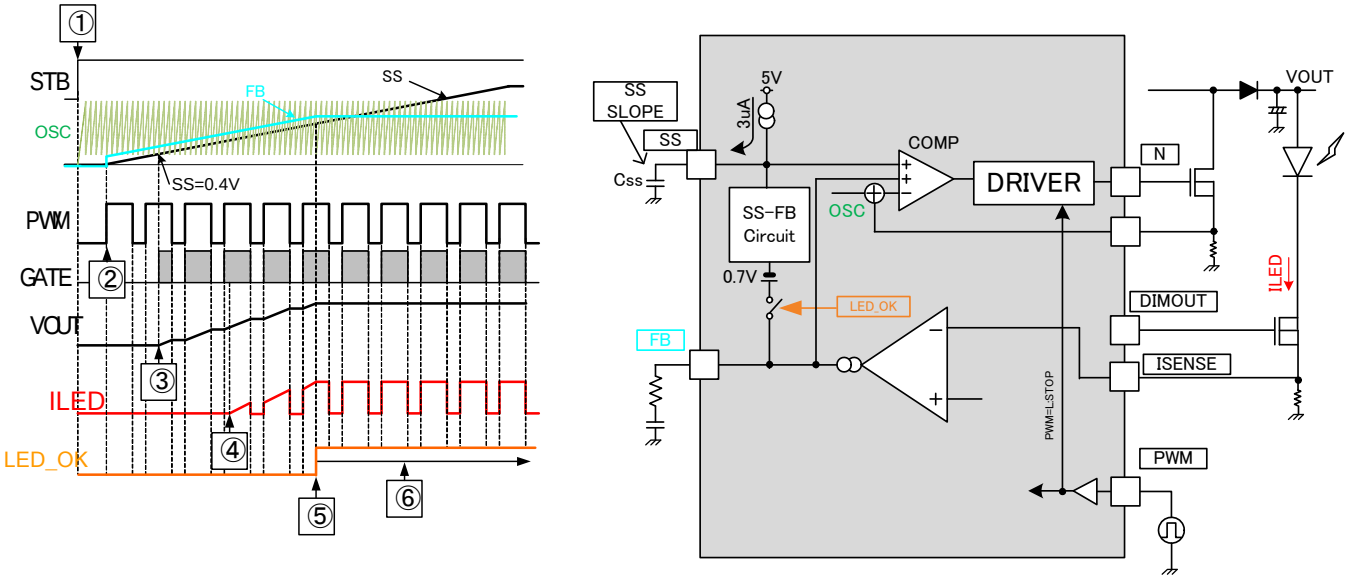


Figure 19.

○**The explanation of start up sequency**

①The internal bias voltage of REG90 turns on by VCCUVLO. And as STB is H, the reset signal is released.

②With the first PWM=H, BD9483F,FV enables to output the boost pulse, and the SS start to charge to the external capacitance. At this moment, the voltage of FB will be clamped to SS+0.7V voltage regardless of the PWM logic.

③The boost of VOUT (GATE pulse) is started as SS=0.4V(typ), because the internal ramp reaches the bottom voltage of saw-toothed wave and the DC/DC start to output the pulse signal.

④VOUT is boosted to a certain level, and the LED current is rising.

⑤When the LED current reached to a certain level, FB is removed from SS+0.7V internally. And the start up operation completed. By this SS-FB clamped circuit, turning on can be completed quickly in spite of small PWM duty.

⑥IC start the normal operation by sensing the voltage of ISENSE pin. FBMAX detection starts monitoring.

○**The setting method of SS external capacitance**

As above described, SS continues to be charged in spite of PWM logic or VOUT level, and FB level is clamped by SS+0.7V.

T_{FB} is defined as the time for the SS voltage to reach to the FB feedback voltage.

When the FB voltage during LED turns on is expressed VFB, the equality on T_{FB} is the following.

$$T_{FB} = \frac{C_{ss}[F] \times VFB[V]}{3[\mu A]} \quad [Sec]$$

•3.4.2 Shutdown method and the setting of REG90 capacitance

When this IC shuts down, VOUT discharge function works. Indicate the sequence.

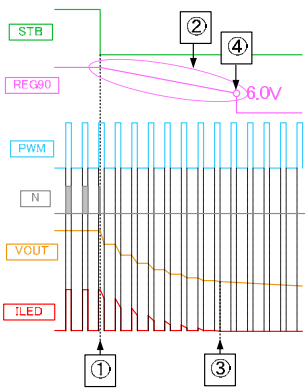


Figure 20.

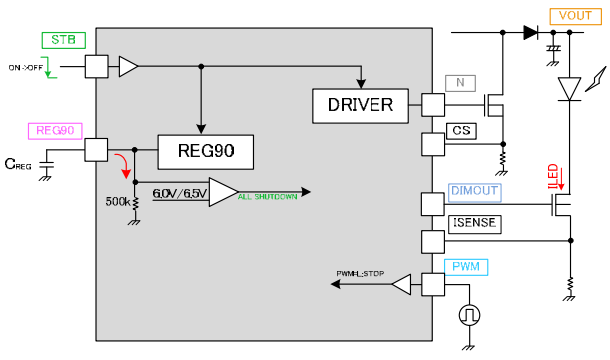


Figure 21.

○**Sequence explanation of shut down**

1. When ENA=L, DCDC and REG90 is stopped.
2. While ENA=L and REG90UVLO=H, DIMOUT asserts the same logic of PWM. And VOUT is discharged until REG90=9.0V is reached to 6.0V by 500kΩ.
3. VOUT is enough discharged by ILED, ILED don't get to flow.
4. REG90 voltage is reached under 6.0V(typ.), whole system is shutdown.

○**Setting method of REG90 capacitance**

Shutdown time TOFF is decided by the following equation.

$$T_{OFF}[sec] = C_{REG}[F] \cdot R_{REG}[\Omega] \cdot In\frac{REG90_{t=0}[V]}{REG90_{UVLO}[V]} = C_{REG}[F] \cdot 500[k\Omega] \cdot in\frac{9.0[V]}{6.0[V]} = 20.2 \cdot 10^{5} \cdot C_{REG}[sec]$$

When discharge function is used, PWM signal must be continued to input after ENA=L.
VOUT discharge time is longest when PWM is set on mininum DUTY.
Please set CREG capacitance value with margin so that the system is shutdown after VOUT is enough discharged.

●3.4.3 The LED current setting

LED current can be adjusted by setting the resistance R_{ISENSE} which connects to ISENSE pin.

○**the relationship between R_{ISENSE} and ILED current**

With DC dimming (ADIM<3.0V)

$$R_{ISENSE} = \frac{ADIM[V]/3}{I_{LED}[A]}[\Omega]$$

Without DC dimming (ADIM>3.0V)

$$R_{ISENSE} = \frac{1.0[V]}{I_{LED}[A]}[\Omega]$$

[setting example]

If ILED current is 400mA as ADIM is 3.0V, we can calculate R_{ISENSE} as below.

$$R_{ISENSE} = \frac{ISENSE[V]}{I_{LED}[A]} = \frac{ADIM/3[V]}{I_{LED}[A]} = \frac{3.0/3[V]}{0.4[A]} = 2.5[\Omega]$$

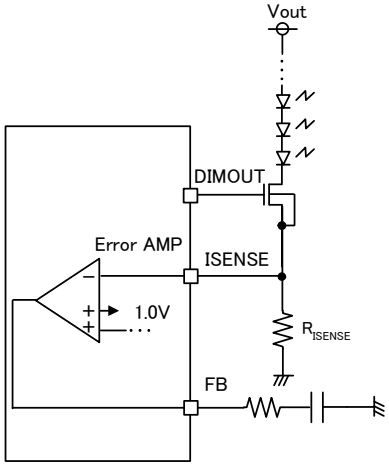


Figure 22.

●3.4.4 how to set DCDC oscillation frequency

R_{RT} which connects to RT pin set the oscillation frequency of DCDC.

○ **the relationship between OSC and R_{RT} (ideal)**

$$R_{RT} = \frac{15000}{f_{SW}[kHz]} \quad [k\Omega]$$

where fsw is the oscillation frequency of DCDC [kHz]

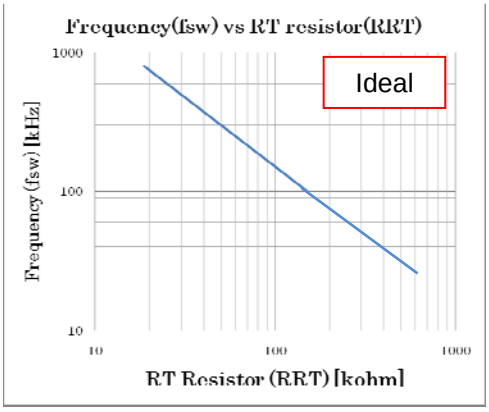


Figure 23.

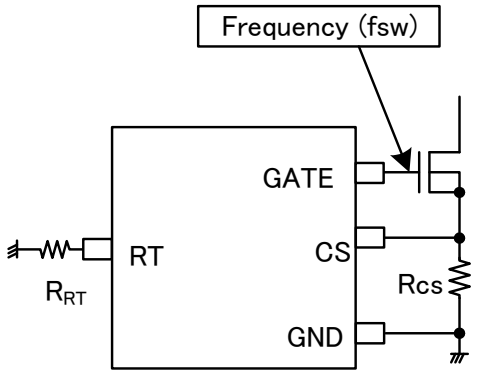


Figure 24.

This equation is an ideal equation in which correction factors are not applied.
The adequate verification with an actual set needs to be performed to set frequency precisely.

[setting example]
If DCDC oscillation frequency is 200kHz, we can calculate the R_{RT} as below.

$$R_{RT} = \frac{15000}{f_{sw}[kHz]} = \frac{15000}{200[kHz]} = 75\ [k\Omega]$$

●3.4.5 how to set UVLO

Under voltage lock out pin for the input voltage of the power stage. More than 3.0V(typ.), IC starts boost operation and stops lower than 2.8V(typ.).
The UVLO pin is high impedance, because the internal resistance to a certain bias is not connected.
So, the bias by the external components is required, even if UVLO function is not used, because the open connection of this pin is not fixed the potential.
The resistor value can be calculated by the below formula.

○UVLO detection equality

As VIN is decreases, R1, R2 value is expressed the following formula by the VINdet, the detect voltage of UVLO.

$$R1 = R2[k\Omega] \times \frac{(VIN_{DET}[V] - 2.8[V])}{2.8[V]} \quad [k\Omega]$$

○UVLO release equality

By using the R1, R2 in the above equality, the release voltage of UVLO can be expressed as following.

$$VIN_{CAN} = 3.0V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

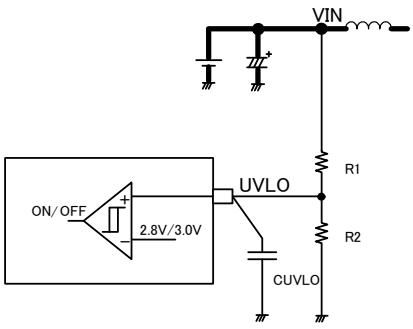


Figure 25.

[setting example]
If the normal input voltage, VIN is 24V, the detect voltage of UVLO is 18V, R2 is 30k ohm, R1 is calculated as following.

$$R1 = R2[k] \times \frac{(VIN_{DET}[V] - 2.8[V])}{2.8[V]} = 30[k\Omega] \times \frac{(18[V] - 2.8[V])}{2.8[V]} = 162.9[k\Omega]$$

By using these R1, R2, the release voltage of UVLO, VINcan can be calculated too as following.

$$VIN_{CAN} = 3.0[V] \times \frac{R1[k\Omega] + R2[k\Omega]}{R2[k\Omega]} = 3.0[V] \times \frac{162.9[k\Omega] + 30[k\Omega]}{30[k\Omega]}[V] = 19.29[V]$$

●3.4.6 how to set OVP

The OVP terminal is the input for over-voltage protection of output voltage.
The OVP pin is high impedance, because the internal resistance to a certain bias is not connected.
So, the bias by the external components is required, even if OVP function is not used, because the open connection of this pin is not fixed the potential.
The resistor value can be calculated by the below formula.

○OVP detection equality

If the VOUT is boosted abnormally, VOVPdet is the detect voltage of OVP, R1, R2 can be expressed by the following formula.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} \quad [k\Omega]$$

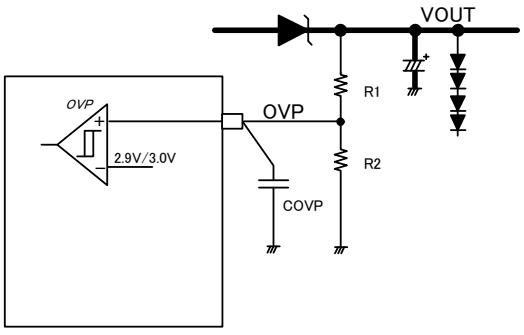


Figure 26.

○OVP release equality

By using the R1, R2 in the above equality, the release voltage of OVP, VOVPcan can be expressed as following.

$$VOVP_{CAN} = 2.9V \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} \quad [V]$$

[setting example]
If the normal output voltage, VOUT is 40V, the detect voltage of OVP is 48V, R2 is 10k ohm, R1 is calculated as following.

$$R1 = R2[k\Omega] \times \frac{(VOVP_{DET}[V] - 3.0[V])}{3.0[V]} = 10[k\Omega] \times \frac{(48[V] - 3[V])}{3[V]} = 150 \quad [k\Omega]$$

By using these R1, R2, the release voltage of OVP, VOVPcan can be calculated as following.

$$VOVP_{CAN} = 2.9[V] \times \frac{(R1[k\Omega] + R2[k\Omega])}{R2[k\Omega]} = 2.9[V] \times \frac{10[k\Omega] + 150[k\Omega]}{10[k\Omega]}[V] = 46.4 \quad [V]$$

●3.4.7 how to set the interval until latch off (CP pin)
BD9483F,FV starts the counting up (charging CP pin) by the detection of FBMAX abnormal state, and BD9483F,FV falls to the latch off state when the following interval has passed.
Only PWM=L input does not reset the timer counter, as the abnormal state continues.

$LATCH_{TIME} = 1.0 * 10^6 * C_{cp}$ [sec]

Where $LATCH_{TIME}$ is the interval until latch off state

C_{CP} is the external capacitor of CP pin.

[setting example]
If the capacitor of CP pin is 0.47uF, the timer latch interval is as following.

$LATCH_{TIME} = 1.0 * 10^6 * C_{cp}$ [sec] = $1.0 * 10^6 * 0.47 * 10^{-6}$ [sec] = 470 [msec]

●3.5 DCDC parts selection

●3.5.1 how to set OCP / the calculation method for the current rating of DCDC parts

BD9483F,FV stops the switching by the OCP detect, when the CS pin voltage is more than 0.4V. The resistor value of CS pin, R_{CS} need to be considered by the coil L current. And the current rating of DCDC external parts is required more than the peak current of the coil.
It is shown below that the calculation method of the coil peak current, the selection method of Rcs (the resistor value of CS pin) and the current rating of the external DCDC parts.

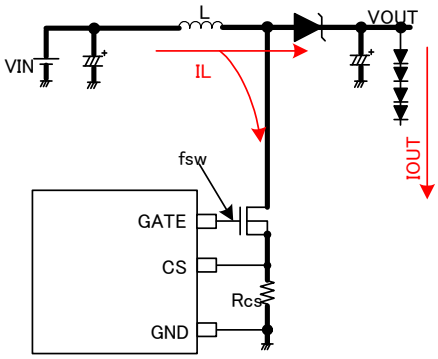


Figure 27.

(the calculation method of the coil peak current, Ipeak)
At first, since the ripple voltage at CS pin depend on the application condition of DCDC, those put onto the equality to calculate as following.
The output voltage = VOUT [V]
LED total current = IOUT [A]
The DCDC input voltage of the power stage = VIN [V]
The efficiency of DCDC =η[%]
And then, the averaged input current IIN is calculated by the following equality

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated by using DCDC the switching frequency, fsw, as following.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

On the other hand, the peak current of the inductor Ipeak can be expressed as the following equality.

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A] \qquad \cdots (1)$$

Therefore, the bottom of the ripple current Imin is

$$Imin = I_{IN}[A] - \frac{\Delta IL[A]}{2} \text{ or } 0$$

As Imin>0, that operation mode is CCM (Continuous Current Mode), otherwise another mode is DCM (Discontinuous Current Mode).

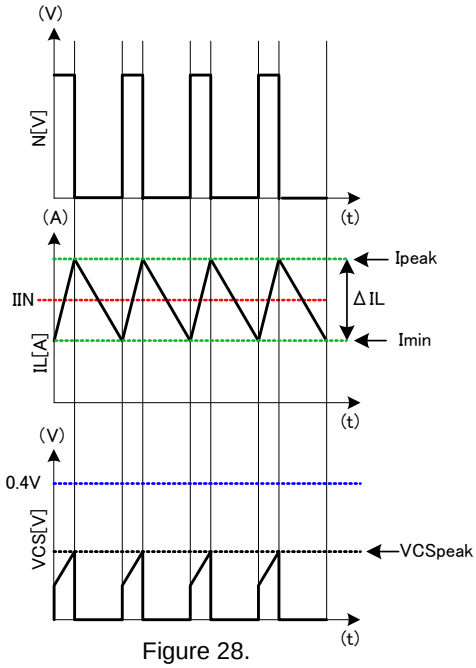


Figure 28.

(the selection method of Rcs)
Ipeak flows into Rcs and that cause the voltage signal to CS pin. (Please refer the right timing chart)
That peak voltage VCSpeak is as following.

$$VCS_{peak} = Rcs \times Ipeak \quad [V]$$

As this VCSpeak reaches to 0.4V, the DCDC output stops the switching.
Therefore, Rcs value is necessary to meet the under condition.

$$\boxed{Rcs \times Ipeak[V] << 0.4[V]}$$

(the current rating of the external DCDC parts)
The peak current as the CS voltage reaches to OCP level (0.4V) is defined as Ipeak_det.

$$I_{peak\_det} = \frac{0.4[V]}{Rcs[\Omega]} \quad [A] \qquad \cdots (2)$$

The relation among Ipeak (equality (1)), Ipeak_det (equality (2)) and the current rating of parts is required to meet the following

$$\boxed{I_{peak} << I_{peak\_det} << \text{ The current rating of parts}}$$

Please make the selection of the external parts to meet the above condition such as FET, Inductor, diode.

[setting example]
The output voltage = VOUT [V] = 40V
LED total current = IOUT [A] = 0.48V
The DCDC input voltage of the power stage = VIN [V] = 24V
The efficiency of DCDC =η[%] = 90%
The averaged input current IIN is calculated as the following.

$$I_{IN}[A] = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} = \frac{40[V] \times 0.48[A]}{24[V] \times 90[\%]} = 0.89 \quad [A]$$

And the ripple current of the inductor L (ΔIL[A]) can be calculated if the switching frequency, fsw = 200kHz, the inductor, L=100μH.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} = \frac{(40[V] - 24[V]) \times 24[V]}{100 \times 10^{-6}[H] \times 40[V] \times 200 \times 10^{3}[Hz]} = 0.48 \quad [A]$$

Therefore the inductor peak current, Ipeak is

$$\boxed{Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} = 0.89[A] + \frac{0.48[A]}{2} = 1.13[A]}$$ ...The calculation result of the peak current

If Rcs is assume to be 0.3 ohm

$$\boxed{VCS_{peak} = Rcs \times Ipeak = 0.3[\Omega] \times 1.13[A] = 0.339[V] << 0.4V}$$

…The Rcs value confirmation

The above condition is met.
And Ipeak_det, the current OCP works is

$$I_{peak\_det} = \frac{0.4[V]}{0.3[\Omega]} = 1.33[A]$$

If the current rating of the used parts is 2A,

$$I_{peak} << I_{peak\_det} << \text{ The current rating} \qquad \boxed{= 1.13[A] << 1.33[A] << 2.0[A]}$$ …

The current rating confirmation of DCDC parts

This inequality meets the above relationship. The parts selection is proper.
And Imin, the bottom of the IL ripple current can be calculated as following.

$$I_{MIN} = I_{IN}[A] - \frac{\Delta IL[A]}{2}[A] = 1.13[A] - 0.48[A] = 0.65[A] >> 0$$

This inequality implies the operation is the continuous current mode.

●3.5.2 Inductor selection

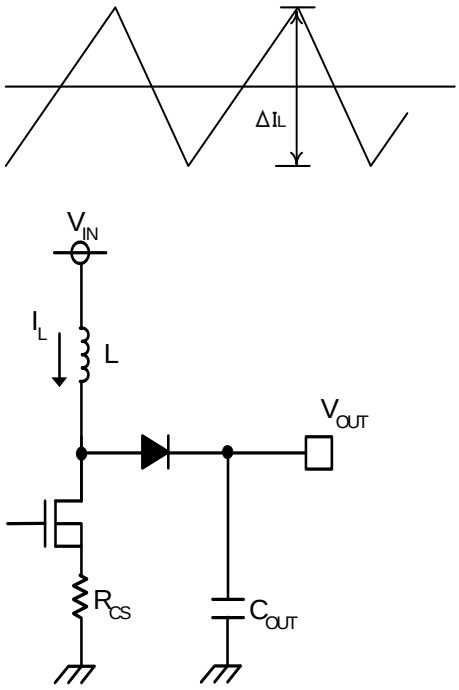


Figure 29.

The inductor value affects the input ripple current.

$$\Delta IL = \frac{(V_{OUT}[V] - V_{IN}[V]) \times V_{IN}[V]}{L[H] \times V_{OUT}[V] \times f_{SW}[Hz]} \quad [A]$$

$$I_{IN} = \frac{V_{OUT}[V] \times I_{OUT}[A]}{V_{IN}[V] \times \eta[\%]} \quad [A]$$

$$Ipeak = I_{IN}[A] + \frac{\Delta IL[A]}{2} \quad [A]$$

Where
L: the coil inductance [H] Vout: the DCDC output voltage [V]
Vin: the input voltage [V]
Iout: the output load current (the summation of LED current) [A]
Iin: the input current [A] Fsw: the oscillation frequency [Hz]

* The current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, results in decreasing in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.

* To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected

●3.5.3 Output capacitance Cout selection

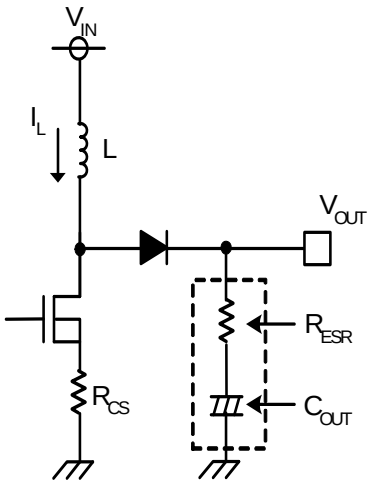


Figure 30.

Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple component is high.
Output ripple voltage V_{OUT} is determined by Equation (4):

$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} \quad [V] \quad \cdots\cdots \quad (4)$$

where, R_{ESR} is the equivalent series resistance of Cout.

* Rating of capacitor needs to be selected to have adequate margin against output voltage.

* To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that the LED current is larger than the set value transitionally in case that LED is provided with PWM dimming especially.

●3.5.4 MOSFET selection

Though there is no problem if the absolute maximum rating is larger than the rated current of the inductor L, or is larger than the sum of the tolerance voltage of C_{OUT} and the rectifying diode V_F. The product with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* The selection of one with small on resistance results in high efficiency.

●3.5.5 Rectifying diode selection

A schottky barrier diode which has current ability higher than the rated current of L, the reverse voltage larger than the tolerance voltage of C_{OUT}, and the low forward voltage VF especially needs to be selected.

●3.6 Loop compensation

A current mode DCDC converter has each one pole (phase lag) f_p due to CR filter composed of the output capacitor and the output resistance (= LED current) and zero (phase lead) f_Z by the output capacitor and the ESR of the capacitor.

Moreover, a step-up DCDC converter has RHP zero (right-half plane zero point) f_{ZRHP} which is unique with the boost converter. This zero may cause the unstable feedback. To avoid this by RHP zero, the loop compensation that the cross-over frequency f_c set as following, is suggested.

fc = f_{ZRHP} /5 (f_{ZRHP}: RHP zero frequency)

Considering the response speed, the below calculated constant is not always optimized completely. It needs to be adequately verified with an actual device.

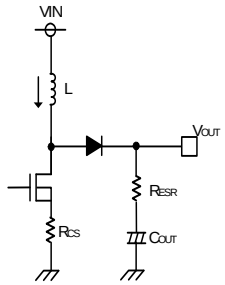


Figure 31.

The output voltage block

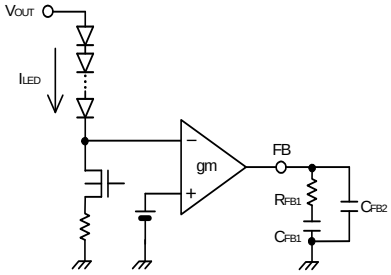


Figure 32.

The error amp block

i. Calculate the pole frequency fp and the RHP zero frequency f_{ZRHP} of DC/DC converter

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} \quad [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} \quad [Hz]$$

Where I_{LED} = the summation of LED current, $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$ (Continuous Current Mode)

ii. Calculate the phase compensation of the error amp output (f_c = f_{ZRHP}/5)

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} \quad [\Omega] \qquad C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_p} \quad [F]$$

Where $gm = 4.0 \times 10^{-4} [S]$

iii. Calculate zero to compensate ESR (R_{ESR}) of C_{OUT} (electrolytic capacitor)

$$C_{FB2} = \frac{R_{ESR} \times C_{OUT}}{R_{FB1}} \quad [F]$$

*When a ceramic capacitor (with R_{ESR} of the order of milliohm) is used to C_{OUT}, the operation is stabilized by insertion of C_{FB2}.

To improve the transient response, R_{FB1} need to be increase, C_{FB1} need to be decrease. It needs to be adequately verified with an actual device in consideration of vary from parts to parts since phase margin is decreased.

●3.7 Timing chart

●**3.7.1** starting up 1 (STB inputs and PWM signal succeeds)

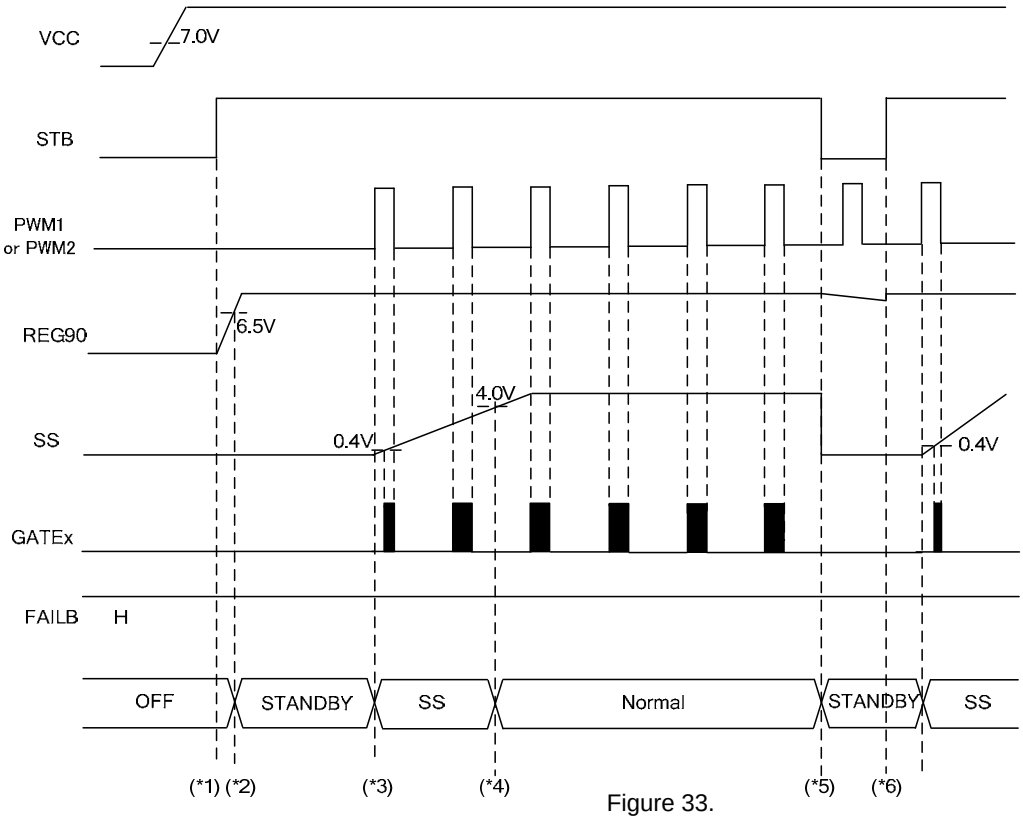


Figure 33.

(*1)…REG90 starts up when VCC is more than 7.0V and STB=H.
(*2)…When REG90 is more than 6.5V, the reset signal is released. The pin SS is not charged in the state that the PWM signal is not input, the boost is not started.
(*3)…The charge of the pin SS starts by the positive edge of PWM1orPWM2=L to H, and the soft start starts. The GATEx pulse outputs only during the corresponding PWMx=H. And as the SS is less than 0.4V(typ), the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
Please refer to the section "●**3.1** Pin Function/SS".
(*4)…The soft start interval will end if the voltage of the pin SS, Vss reaches to 4.0V. By this time, BD9483F,FV boost Vout to the voltage where the set LED current flows. It is started to monitor the abnormal detection of FBMAX.
(*5)…As STB=L, instantaneously the boost operation is stopped. (GATEx=L, SS=L)
(*6)…As STB=H again, the boost operation restarts by the next PWM=H. It is the same operation as the timing of (*2).

●**3.7.2** starting up 2 (PWM signal inputs and STB succeeds)

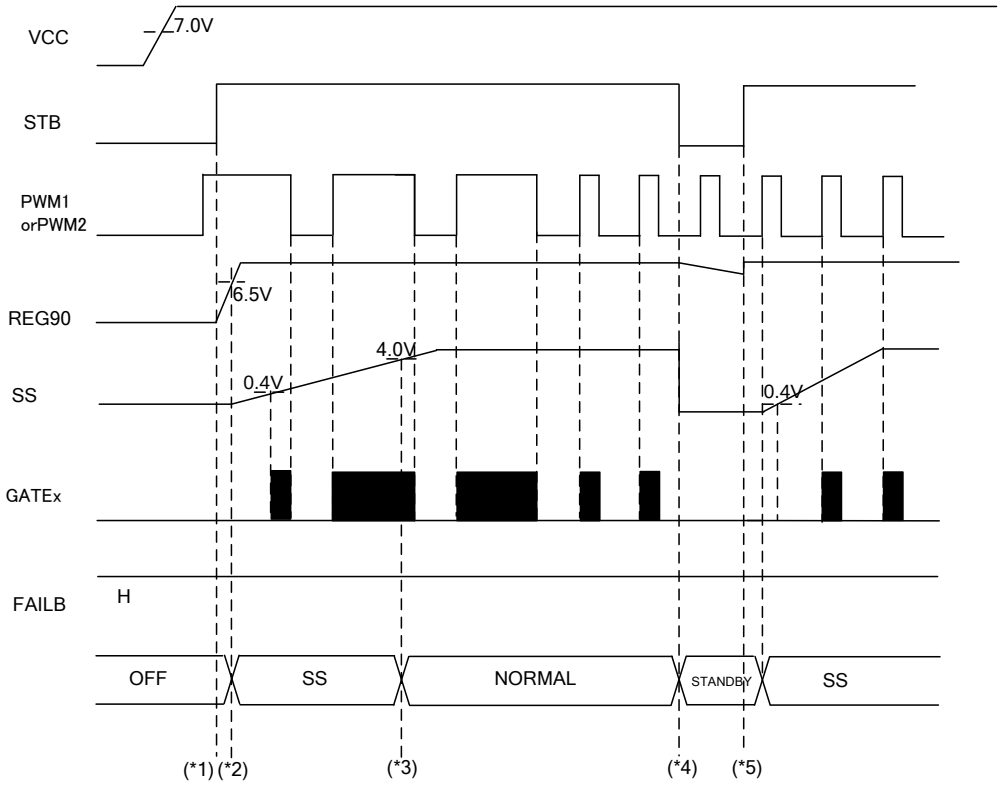


Figure 34.

(*1)…REG90 starts up when STB=H.
(*2)…When REG90 is more than 6.5V, the reset signal is released. In the first PWM=H the soft-start begins the changing immediately. The GATEx pulse outputs only during the corresponding PWMx=H. And as the SS is less than 0.4V(typ), the pulse does not output. The pin SS continues charging in spite of the assertion of PWM or OVP level.
(*3)…The soft start interval will end if the voltage of the pin SS, Vss reaches to 4.0V. By this time, BD9483F,FV boost Vout to the point where the set LED current flows. It is started to monitor the abnormal detection of FBMAX.
(*4)…As STB=L, instantaneously the boost operation is stopped. (GATE=L, SS=L)
(*5)…As STB=H again, it is the same operation as the timing of (*1).

●**3.7.3** the soft start function

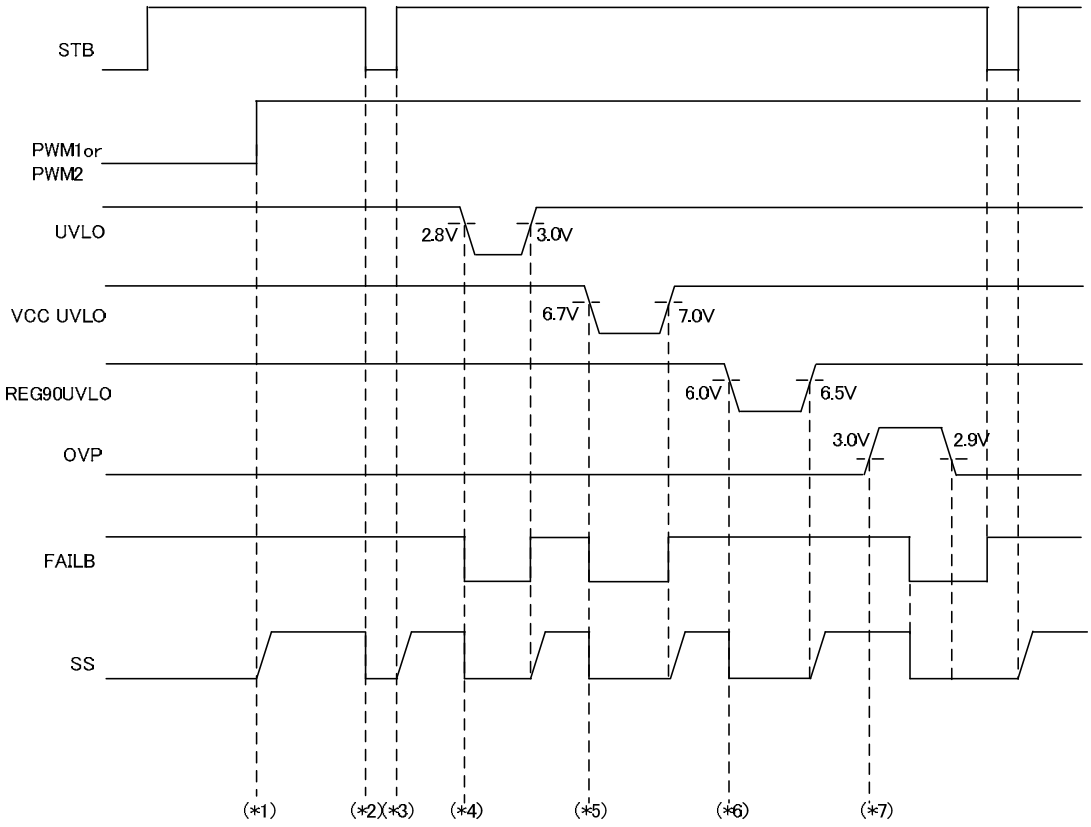


Figure 35.

(*1)…The SS pin charge does not start by just STB=H. “PWM1=H or PWM2=H” is required to start the soft start. In the low SS voltage, the GATE pin duty is depend on the SS voltage. And as the SS is less than 0.1V, the pulse does not output.
(*2)…By the low STB=L, the SS pin is discharged immediately.
(*3)…As the STB recovered to STB=H, The SS charge starts immediately by the logic “PWM1 or PWM2=H” in this chart.
(*4)…The SS pin is discharged immediately by the UVLO=L and FAILB is changed OPEN to Low.
(*5)…The SS pin is discharged immediately by the VCCUVLO=L and FAILB is changed OPEN to Low.
(*6)…The SS pin is discharged immediately by the REG90UVLO=L and FAILB keeps OPEN.
(*7)…The SS pin is not discharged by the abnormal detection of the latch off type such as OVP until the latch off.

●**3.7.4** the OVP detection

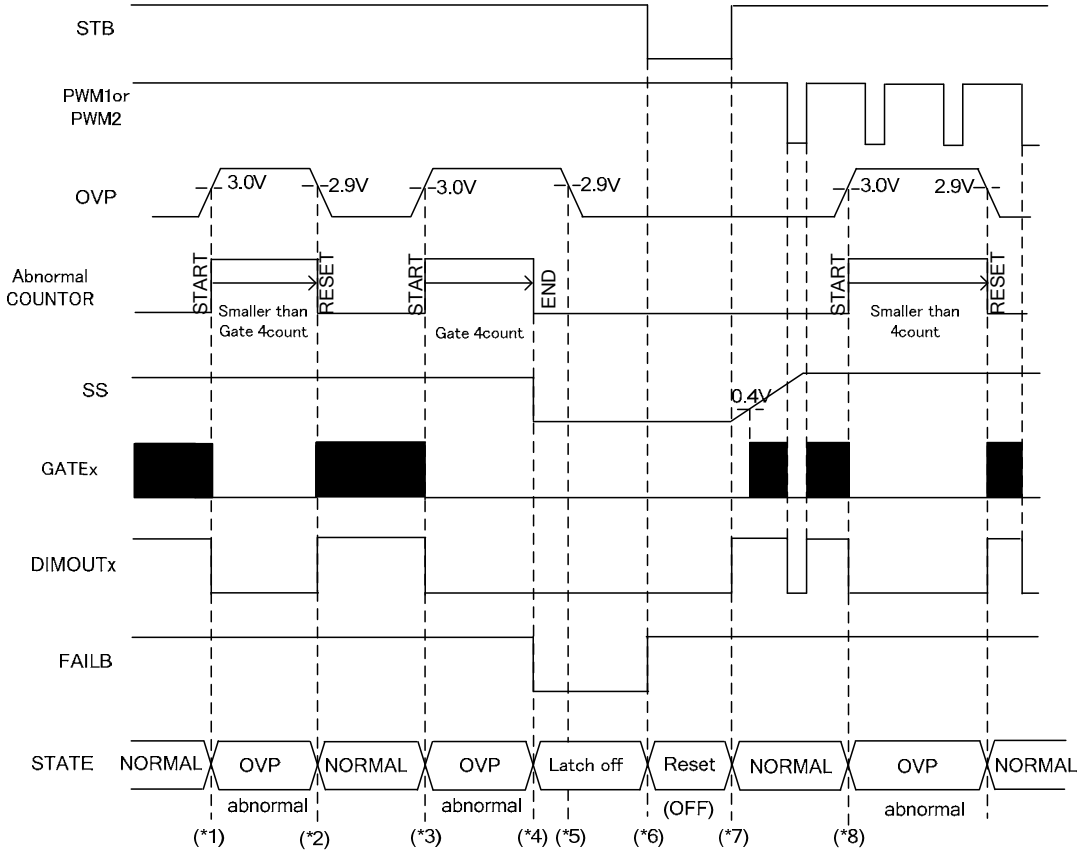


Figure 36.

(*1)…As OVP is detected, the output GATE=L, DIMOUT=L, and the abnormal counter starts
(*2)…If OVP is released within 4 clock of abnormal counter of the GATE pin frequency, the boost operation restarts.
(*3)…As the OVP is detected again, the boost operation is stopped.
(*4)…As the OVP detection continues up to 4 count by the abnormal counter, IC will be latched off. Both channels will be stopped. (GATE1=GATE2=L, DIMOUT1=DIMOUT2=L)
(*5)…As the latched off, the boost operation doesn't restart even if OVP is released.
(*6)…The STB=L input can make IC reset.
(*7)…It normally starts as STB turns L to H.
(*8)…The operation of the OVP detection is not related to the logic of PWM.

●**3.7.5** FBMAX detection

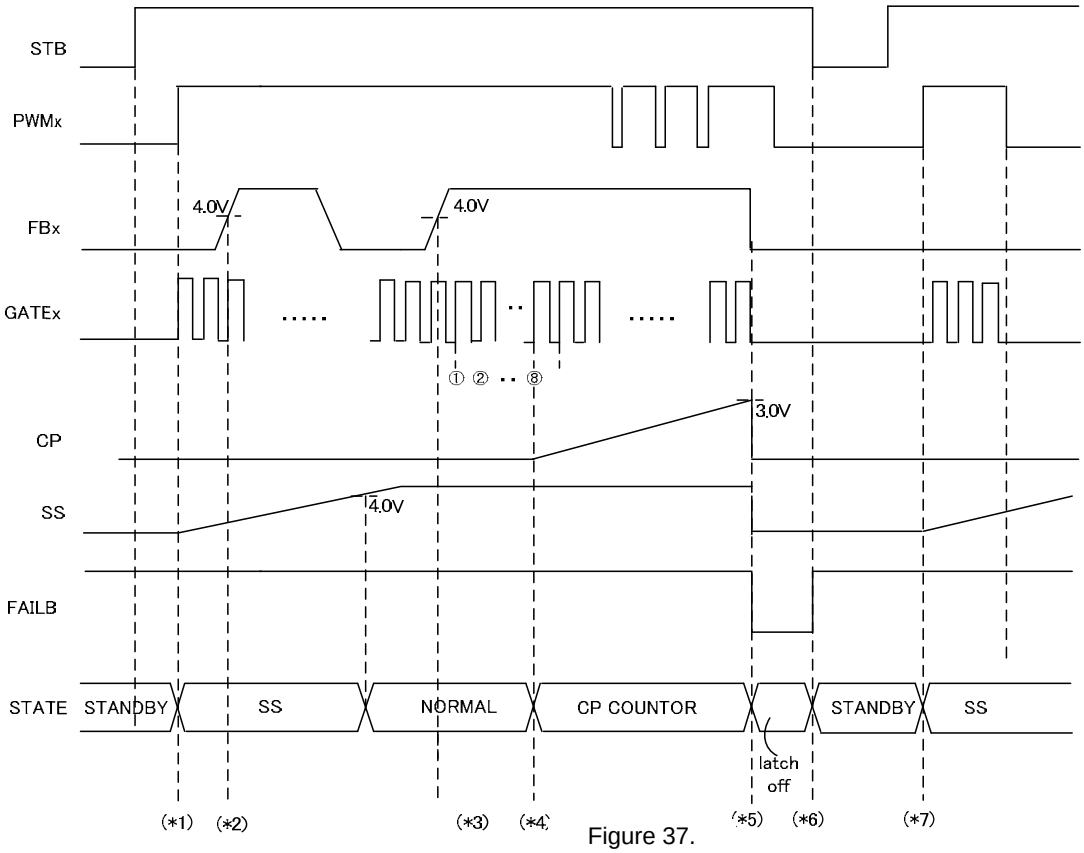


Figure 37.

(*2)…During the soft start, it is not judged to the abnormal state even if the FB=H(FB>4.0V).
(*3)…When the PWM=H and FB=H, the abnormal counter doesn't start immediately.
(*4)…The CP charge will start if the PWM=H and the FB=H detection continues 8 clock of the GATE frequency. Once the count starts, only FB level is monitored.
(*5)…When the FBMAX detection continues till the CP charge reaches to 3.0V, IC will be latched off. The latch off interval can be calculated by the external capacitance of CP pin. (Please refer the section 3.4.7.) In latch off mode, both CH1 and CH2 will be stopped.
(*6)…The latch off state can be reset by the STB=L.
(*7)…It is normally started by PWM=L to H, in this Figure.

●**3.7.6** LED OCP detection

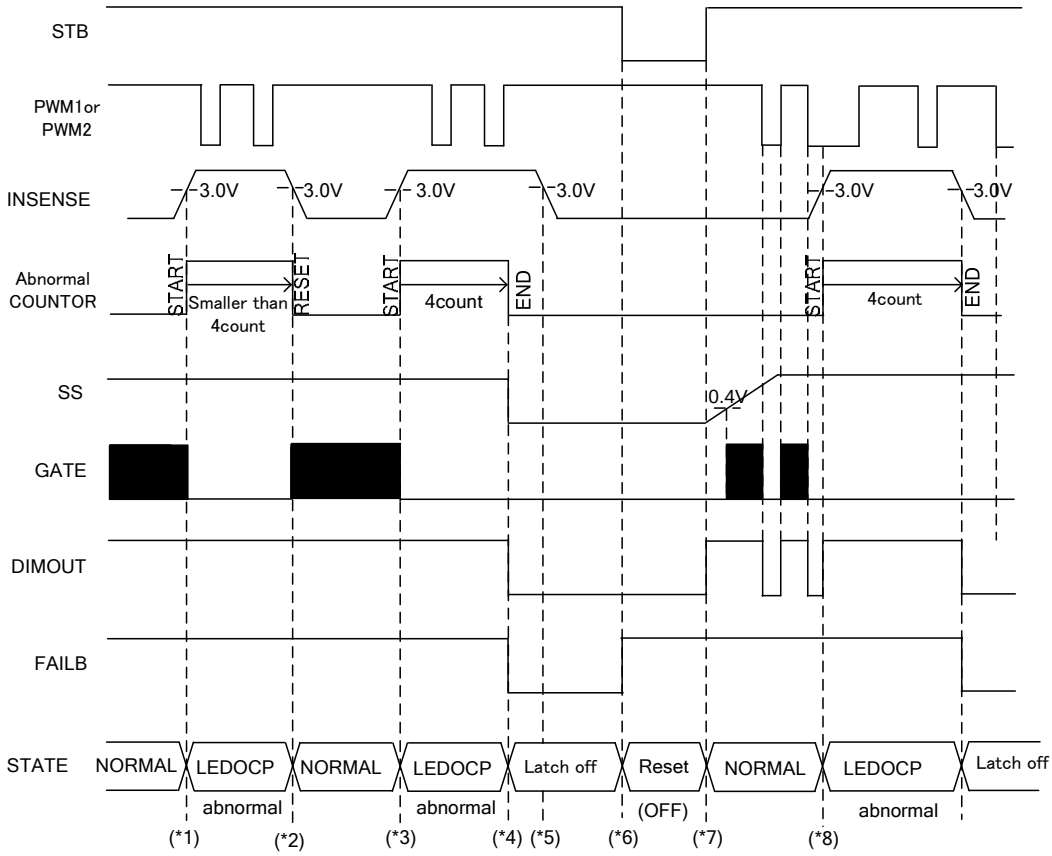


Figure 38.

(*1)…If ISENSE>3.0V, LEDOCP is detected, it becomes GATE=L. To detect LEDOCP continuously, The DIMOUT is compulsorily high, regardless of the PWM dimming signal.
(*2)…When the LEDOCP releases within 4 counts of the GATE frequency, the boost operation restarts.
(*3) …As the LEDOCP is detected again, the boost operation is stopped, too.
(*4)…If the LEDOCP detection continues up to 4 counts of GATE frequency. IC will be latched off.
(*5)…Once IC is latched off, the boost operation doesn't restart even if the LEDOCP releases. And both CH1 and CH2 will be stopped.
(*6)…The latch off state can be reset by the STB=L.
(*7)…It normally starts by STB=L to H.
(*8)…The operation of the LEDOCP detection is not related to the logic of the PWM.

●**3.7.7** the spontaneous detection OVP and FBMAX.

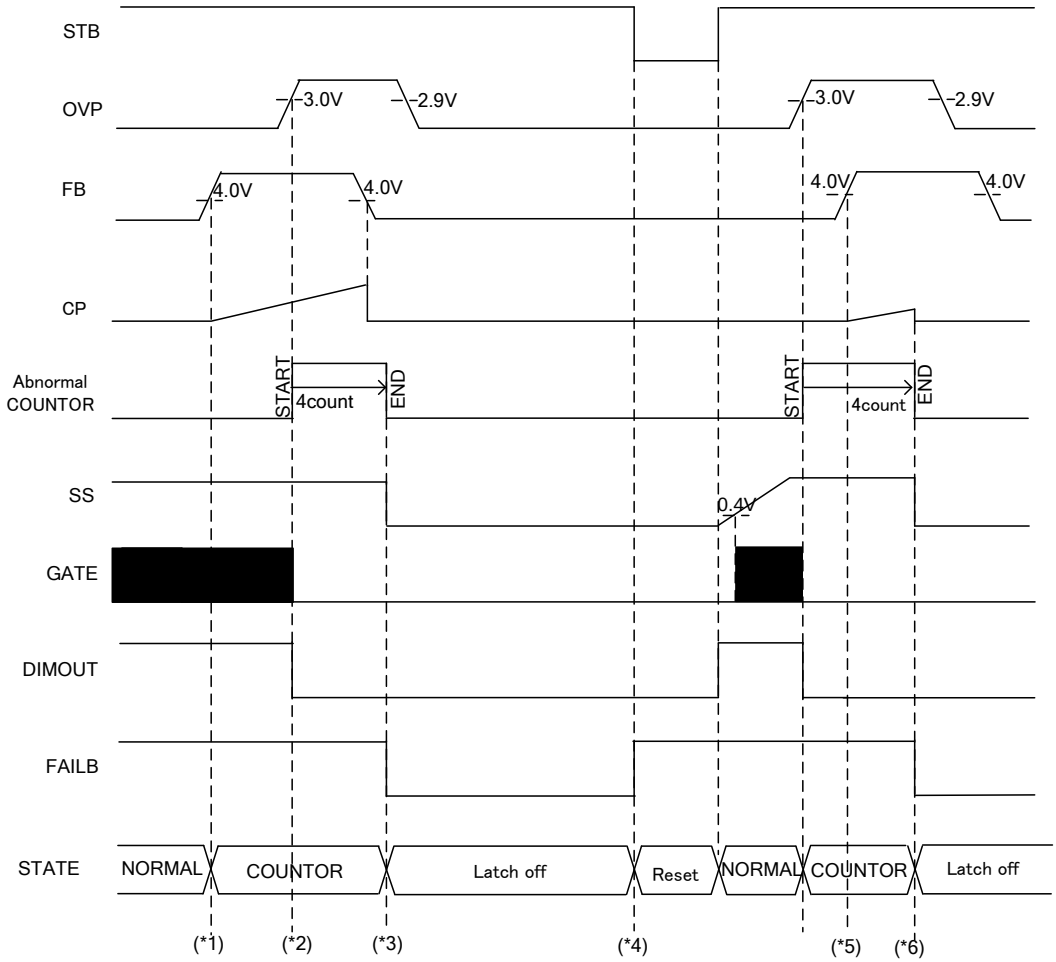


Figure 39.

(*1)…As the FBMAX is detected, the CP charge is started.
(*2)…As the OVP is detected, the abnormal counter is started, the CP charge is not reset.
(*3)…IC is latched off by OVP.
(*4)…The latch mode is reset by STB=L
(*5)…If the FBMAX is detected during OVP, the CP charge is started.
(*6)…The OVP counties to 4clk, IC is latched off. And the CP charge is reset.

●Operational Notes

1.) This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings including the range of applied voltage or operation temperature. Failure status such as short-circuit mode or open mode can not be estimated. If a special mode beyond the absolute maximum ratings is estimated, physical safety countermeasures like fuse needs to be provided.

2.) Connecting the power line to IC in reverse polarity (from that recommended) may cause damage to IC. For protection against damage caused by connection in reverse polarity, countermeasures, installation of a diode between external power source and IC power terminal, for example, needs to be taken.

3.) When this product is installed on a printed circuit board, attention needs to be paid to the orientation and position of IC. Wrong installation may cause damage to IC. Short circuit caused by problems like foreign particles entering between outputs or between an output and power GND also may cause damage.

4.) Since the back electromotive force of external coil causes regenerated current to return, countermeasures like installation of a capacitor between power source and GND as the path for regenerated current needs to be taken. The capacitance value must be determined after it is adequately verified that there is no problem in properties such that the capacity of electrolytic capacitor goes down at low temperatures. Thermal design needs to allow adequate margin in consideration of allowable loss (Pd) in actual operation state.

5.) The GND pin needs to be at the lowest potential in any operation state.

6.) Thermal design needs to be done with adequate margin in consideration of allowable loss (Pd) in actual operation state.

7.) Use in a strong magnetic field may cause malfunction.

8.) Output Tr needs to not exceed the absolute maximum rating and ASO while using this IC. As CMOS IC and IC which has several power sources may undergo instant flow of rush current at turn-on, attention needs to be paid to the capacitance of power source coupling, power source, and the width and run length of GND wire pattern.

9.) This IC includes temperature protection circuit (TSD circuit). Temperature protection circuit (TSD circuit) strictly aims blockage of IC from thermal runaway, not protection or assurance of IC. Therefore use assuming continuous use and operation after this circuit is worked needs to not be done.

10.) As connection of a capacitor with a pin with low impedance at inspection of a set board may cause stress to IC, discharge needs to be performed every one process. Before a jig is connected to check a process, the power needs to be turned off absolutely. Before the jig is removed, as well, the power needs to be turned off.

11.) This IC is a monolithic IC which has P+ isolation for separation of elements and P board between elements.
A P-N junction is formed in this P layer and N layer of elements, composing various parasitic elements.
For example, a resistance and transistor are connected to a terminal as shown in the figure,
   - ○ When GND>(Terminal A) in the resistance and when GND>(Terminal B) in the transistor (NPN), P-N junction operates as a parasitic diode.
   - ○ When GND>(Terminal B) in the transistor (NPN), parasitic NPN transistor operates in N layer of other elements nearby the parasitic diode described before.

Parasitic elements are formed by the relation of potential inevitably in the structure of IC. Operation of parasitic elements can cause mutual interference among circuits , malfunction as well as damage. Therefore such use as will cause operation of parasitic elements like application of voltage on the input terminal lower than GND (P board) need to not be done.

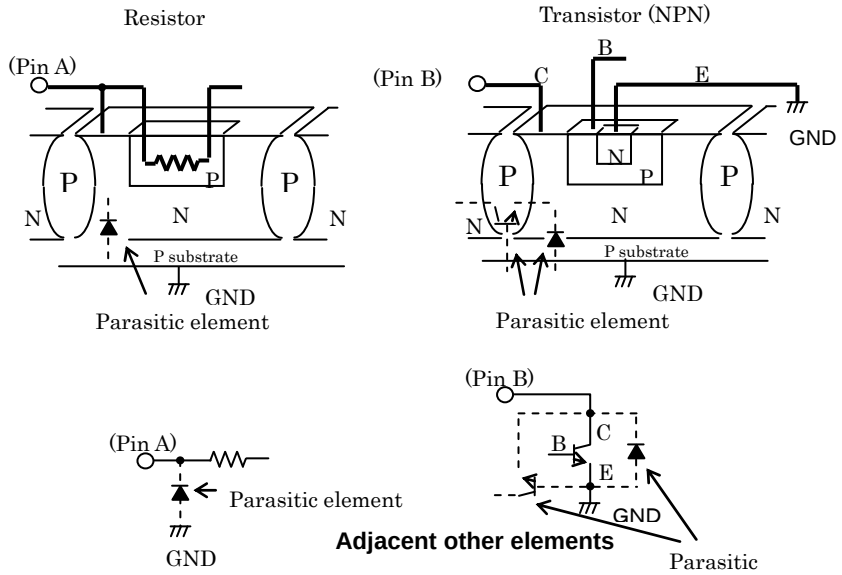


Figure 40. Example of Simple Structure of Monolithic IC

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

●**Ordering Information**

B D 9 4 8 3 F	-	XX

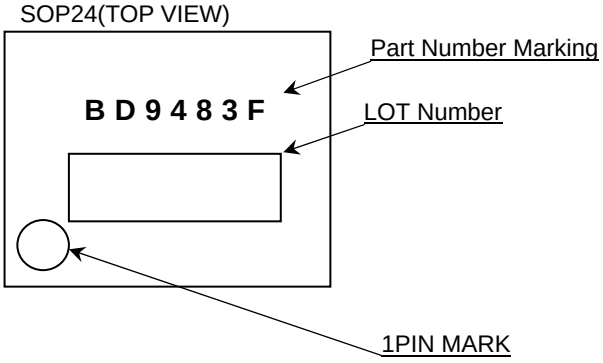
Part Number

Package
F:SOP
FV:SSOP

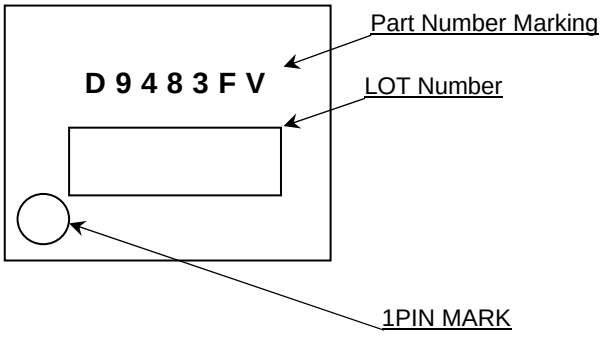
Packaging and forming specification
XX: Please confirm the formal name to our sales.

●**Marking Diagram**

SOP24(TOP VIEW)

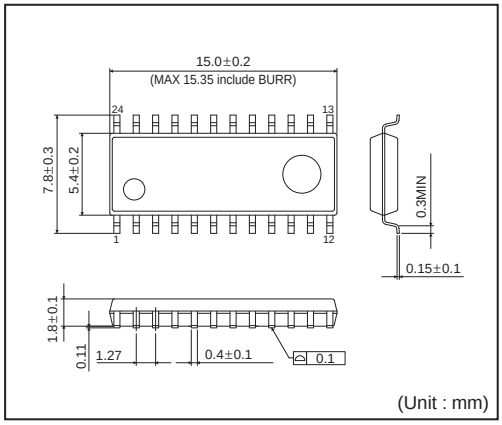


SSOP-B24(TOP VIEW)



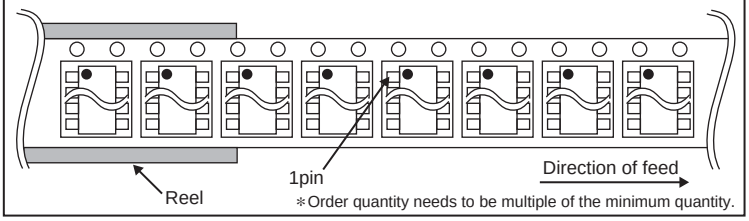
●**Physical Dimension Tape and Reel Information**

SOP24



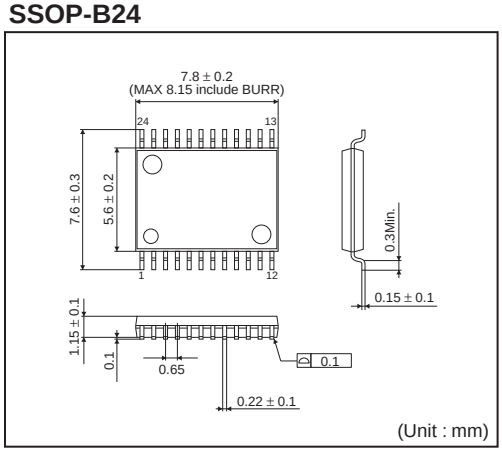
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



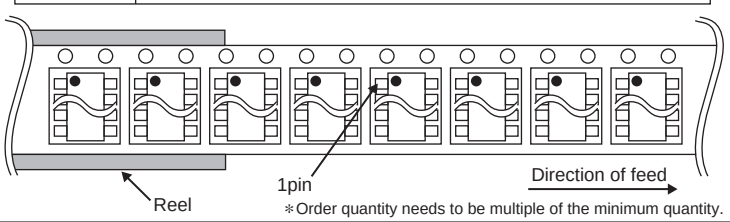
∗Order quantity needs to be multiple of the minimum quantity.

SSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
18.Sep.2012	001	New Release
16.Oct.2012	002	p.7 Item arrangement of Typical Performance Curves
28.Nov.2013	003	p.5 1.3 Pin Descriptions In/Out GATE1：In→Out p.13 Diagram of start-up sequence SS=0.1V → SS=0.4V p.13 Explanation of start-up sequence SS=0.1V → SS=0.4V(typ) p.20 3.7.1 diagram SS 0.1V → 0.4V p.20 3.7.1 explanation(*3) less than 0.1V → less than 0.4V(typ) p.21 3.7.2 diagram SS 0.1V → 0.4V p.21 3.7.2 explanation (*2) less than 0.1V → less than 0.4V(typ) p.23 3.7.4 diagram SS 0.1V → 0.4V p.25 3.7.6 diagram SS 0.1V → 0.4V p.26 3.7.7 diagram SS 0.1V → 0.4V

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

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LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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