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- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree<sup>(1)</sup>
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- High Slew Rate . . . 10.5 V/μs Typ
- High-Gain Bandwidth . . . 5.1 MHz Typ
- Supply Voltage Range 2.5 V to 5.5 V

- Rail-to-Rail Output
- 360 μV Input Offset Voltage
- Low Distortion Driving 600-Ω
   0.005% THD+N
- 1 mA Supply Current (Per Channel)
- 17 nV/√Hz Input Noise Voltage
- 2 pA Input Bias Current
- Characterized From  $T_{\Delta} = -55^{\circ}C$  to  $125^{\circ}C$
- Micropower Shutdown Mode . . . I<sub>DD</sub> < 1 μA</li>

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### description

The TLV277x CMOS operational amplifier family combines high slew rate and bandwidth, rail-to-rail output swing, high output drive, and excellent dc precision. The device provides 10.5 V/ $\mu$ s of slew rate and 5.1 MHz of bandwidth while only consuming 1 mA of supply current per channel. This ac performance is much higher than current competitive CMOS amplifiers. The rail-to-rail output swing and high output drive make these devices a good choice for driving the analog input or reference of analog-to-digital converters (ADCs) . These devices also have low distortion while driving a 600- $\Omega$  load for use in telecom systems.

These amplifiers have a  $360-\mu V$  input offset voltage, a 17 nV/ $\sqrt{\text{Hz}}$  input noise voltage, and a 2-pA input bias current for measurement, medical, and industrial applications. The TLV277x family is also specified across an extended temperature range (–55°C to 125°C), making it useful for military and avionics systems.

These devices operate from a 2.5-V to 5.5-V single supply voltage and are characterized at 2.7 V and 5 V. The single-supply operation and low power consumption make these devices a good solution for portable applications. The following table lists the packages available.

### **FAMILY PACKAGE TABLE**

DEVICE	NUMBER OF		KAGE PES	SHUTDOWN	UNIVERSAL EVM BOARD
	CHANNELS	SOIC	TSSOP		EVIVI BOARD
TLV2770	1	8	_	Yes	
TLV2771	1	8	_	_	
TLV2772	2	8	8	_	See the EVM Selection Guide
TLV2773	2	14	_	Yes	(SLOU060)
TLV2774	4	14	14	_	(= = = = = ,
TLV2775	4	16	16	Yes	



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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### SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS<sup>†</sup>

DEVICE	V <sub>DD</sub> (V)	BW SLEW RATE (V/μs)		I <sub>DD</sub> (per channel) (μA)	RAIL-TO-RAIL
TLV277X	2.5 to 6	5.1	10.5	1000	0
TLV247X	2.7 to 6	2.8	1.5	600	I/O
TLV245X	2.7 to 6	0.22	0.11	23	I/O
TLV246X	2.7 to 6	6.4	1.6	550	I/O

<sup>†</sup> All specifications measured at 5 V.

### **ORDERING INFORMATION†**

TA	V <sub>IO</sub> MAX AT 25°C (mV)	PACK	(AGE <sup>‡</sup>	ORDERABLE PART NUMBER	TOP SIDE MARKING
	2.5	SOIC (D)	Tape and reel	TLV2770MDREP§	
	1.6	SOIC (D)	Tape and reel	TLV2770AMDREP§	
	2.5	SOIC (D)	Tape and reel	TLV2771MDREP§	
	1.6	SOIC (D)	Tape and reel	TLV2771AMDREP§	
	0.5	SOIC (D)	Tape and reel	TLV2772MDREP§	
	2.5	TSSOP (PW)	Tape and reel	TLV2772MPWREP§	
	1.6	SOIC (D)	Tape and reel	TLV2772AMDREP	2772AE
		TSSOP (PW)	Tape and reel	TLV2772AMPWREP§	
5500 / 40500	2.5	SOIC (D)	Tape and reel	TLV2773MDREP§	
−55°C to 125°C	1.6	SOIC (D)	Tape and reel	TLV2773AMDREP§	
		SOIC (D)	Tape and reel	TLV2774MDREP	2774EP
	2.7	TSSOP (PW)	Tape and reel	TLV2774MPWREP§	
	0.4	SOIC (D)	Tape and reel	TLV2774AMDREP	2774AEP
	2.1	TSSOP (PW)	Tape and reel	TLV2774AMPWREP§	
	0.7	SOIC (D)	Tape and reel	TLV2775MDREP§	
	2.7	TSSOP(PW)	Tape and reel	TLV2775MPWREP§	
	0.4	SOIC (D)	Tape and reel	TLV2775AMDREP§	
	2.1	TSSOP (PW)	Tape and reel	TLV2775AMPWREP§	

T For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

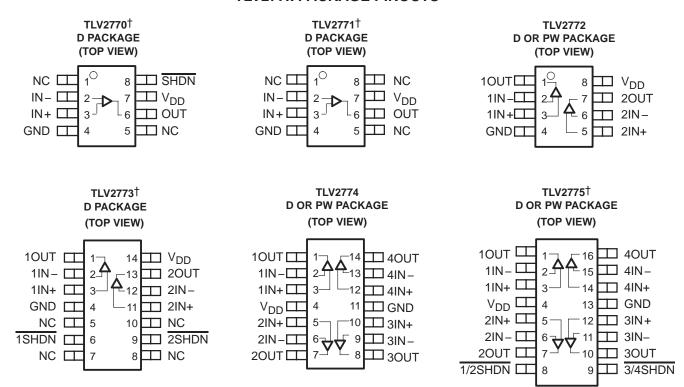


<sup>‡</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

<sup>§</sup> Product Preview

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### **TLV277x PACKAGE PINOUTS**



NC - No internal connection

<sup>†</sup> This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>DD</sub> (see Note 1)	
Differential input voltage, V <sub>ID</sub> (see Note 2)	
Input voltage range, V <sub>I</sub> (any input, see Note 1)	0.3 V to V <sub>DD</sub>
Input current, I <sub>I</sub> (any input)	±4 mA
Output current, IO	±50 mA
Total current into V <sub>DD+</sub>	±50 mA
Total current out of GND	±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub> : M suffix	–55°C to 125°C
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
  - 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below GND 0.3 V.
  - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

#### **DISSIPATION RATING TABLE**

DAOKAGE	ΘJC (°	C/W)	Θ <sub>JA</sub> (°C/W, 0 AIR FLOW)				
PACKAGE	HIGH K	LOW K	HIGH K	LOW K			
D(8)	39.4	42.4	97.1	165.5			
D(14)	51.5	53.7	86.2	133.5			
D(16)	36.9	38.4	73.1	111.6			
PW(8)	65.1	69.4	149.4	230.5			
PW(14)	45.8	46.6	111.7	131.4			
PW(16)	33.6	35	108.4	147.0			

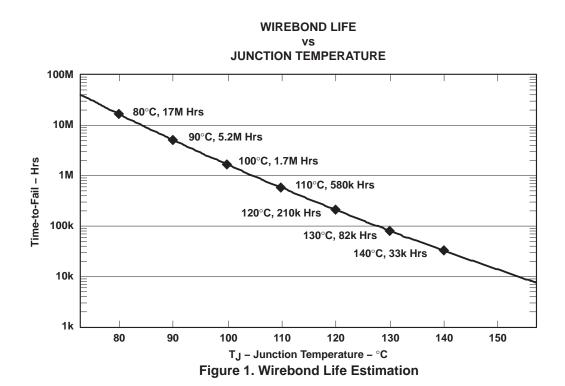
NOTE 4: Thermal resistances are not production tested and are for informational purposes only.

### recommended operating conditions

	M	SUFFIX	
	MIN	UNIT	
Supply voltage, V <sub>DD</sub>	2.5	6	V
Input voltage range, V <sub>I</sub>	GND	V <sub>DD+</sub> -1.3	V
Common-mode input voltage, V <sub>IC</sub>	GND	V <sub>DD+</sub> -1.3	V
Operating free-air temperature, T <sub>A</sub>	-55	125	°C



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## TLV277x-EP, TLV277xA-EP FAMILY OF 2.7-V HIGH-SLEW-RATE RAIL-TO-RAIL OUTPUT **OPERATIONAL AMPLIFIERS WITH SHUTDOWN** SGLS317A – OCTOBER 2005 – REVISED SEPTEMBER 2007

## electrical characteristics at specified free-air temperature, $V_{DD}$ = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONE	OITIONS	T <sub>A</sub> †	Τl	.V277x <b>i</b>	VI	TL	V277xA	M	UNIT	
'	PARAMETER	TEST CONL	DITIONS	'A'	MIN	TYP	MAX	MIN	TYP	MAX	UNII	
			TLV2770/1/2/3	25°C		0.44	2.5		0.44	1.6		
\/	Innut offeet valtege	$V_{DD} = \pm 1.35 \text{ V},$	1LV2/10/1/2/3	Full range			2.7			1.9	m)/	
VIO	Input offset voltage	$V_{IC} = 0, V_{O} = 0,$ $R_{S} = 50 \Omega$	TLV2774/5	25°C		0.8	2.7		0.8	2.1	mV	
		0 11	1LV2/74/5	Full range			3.0			2.4		
ανιο	Temperature coefficient of input offset voltage	$V_{DD} = \pm 1.35 \text{ V},$ $V_{IC} = 0, V_{O} = 0,$ $R_{S} = 50 \Omega$		25°C to 125°C		2			2		μV/°C	
		$V_{DD} = \pm 1.35 \text{ V},$		25°C		1	60		1	60		
IIO	Input offset current	$V_{IC} = 0, V_{O} = 0,$	TL2770/1/2/3				125			125	pА	
		$R_S = 50 \Omega$	TLV2774/5	Full range			200			200		
		Vpp = ±1.35 V,		25°C		2	60		2	60		
I <sub>IB</sub>	Input bias current	$V_{IC} = 0, V_{O} = 0,$	TLV2770/1/2/3	- "			350			350	pА	
		$R_S = 50 \Omega$	TLV2774/5	Full range			500			500		
	Common-mode			25°C	0 to 1.4	-0.3 to 1.7		0 to 1.4	-0.3 to 1.7			
VICR	VICR input voltage range CMRR > 60 dB,		$R_S = 50 \Omega$	Full range	0 to 1.4	-0.3 to 1.7		0 to 1.4	-0.3 to 1.7		V	
				25°C		2.6			2.6			
	High-level output	$I_{OH} = -0.675 \text{ mA}$		Full range	2.45			2.45				
VOH	voltage		25°C		2.4			2.4		V		
		$I_{OH} = -2.2 \text{ mA}$		Full range	2.1			2.1				
				25°C		0.1			0.1			
l.,	Low-level output	V <sub>IC</sub> = 1.35 V,	$I_{OL} = 0.675 \text{ mA}$	Full range			0.2			0.2	.,	
VOL	voltage			25°C		0.21			0.21		V	
		V <sub>IC</sub> = 1.35 V,	$I_{OL} = 2.2 \text{ mA}$	Full range			0.6			0.6		
	Large-signal	V <sub>IC</sub> = 1.35 V,	R <sub>L</sub> = 10 kΩ,‡	25°C	20	380		20	380			
AVD	differential voltage amplification	$V_0 = 0.6 \text{ V to } 2.1 \text{ V}$	K[ = 10 K52,+	Full range	13			13			V/mV	
r <sub>i(d)</sub>	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω	
Ci(c)	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF	
z <sub>O</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		25			25		Ω	
	Common-mode	$V_{IC} = V_{ICR}$ (min),	V <sub>O</sub> = 1.5 V,	25°C	60	84		60	84			
CMRR	rejection ratio	$R_S = 50 \Omega$	,	Full range	60	82		60	82		dB	
leas :=	Supply voltage rejection ratio	V <sub>DD</sub> = 2.7 V to 5 V,	$V_{IC} = V_{DD}/2$ ,	25°C	70	89		70	89		40	
ksvr	(ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	No load		Full range	70	84		70	84		dB	
I <sub>DD</sub>	Supply current	V <sub>O</sub> = 1.5 V,	No load	25°C		1	2		1	2	mA	
טט.	(per channel)	VU = 1.5 V,	110 1000	Full range			2			2	111/4	

<sup>†</sup>Full range is -55°C to 125°C for M level part.



<sup>‡</sup>Referenced to 1.35 V

# TLV277x-EP, TLV277xA-EP FAMILY OF 2.7-V HIGH-SLEW-RATE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN SGLS317A - OCTOBER 2005 - REVISED SEPTEMBER 2007

## operating characteristics at specified free-air temperature, $V_{DD}$ = 2.7 V (unless otherwise noted)

	D. D. A. W. ETED	TEOT 001		_ +	Τι	_V277xM		TL	LINUT		
	PARAMETER	TEST CONI	DITIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		V 0.0V	25°C	5	9		5	9			
SR	Slew rate at unity gain	$V_{O(PP)} = 0.8 \text{ V},$ $R_{L} = 10 \text{ k}\Omega$	CL = 100 pF,	Full range	4.7	6		4.7	6		V/μs
	Equivalent input	f = 1 kHz		0500		21			21		->/// <del>  </del>
V <sub>n</sub>	noise voltage	f = 10 kHz		25°C		17			17		nV/√Hz
,,	Peak-to-peak	f = 0.1 Hz to 1 Hz		0500		0.33			0.33		μV
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 H	lz	25°C		0.86			0.86		μV
In	Equivalent input noise current	f = 100 Hz		25°C		0.6		0.6			fA/√ <del>Hz</del>
			A <sub>V</sub> = 1		C	0.0085%		C	0.0085%		
THD + N	Total harmonic distortion plus noise	$R_L = 600 \Omega$ , f = 1  kHz	A <sub>V</sub> = 10	25°C		0.025%			0.025%		
	alotoritori piao ilioto		$A_{V} = 100$			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF	$R_L = 600 \Omega$ ,	25°C		4.8			4.8		MHz
	Oattle without	$A_V = -1$ , Step = 0.85 V to 1.85 V,	0.1%	0500		0.186			0.186		
t <sub>S</sub>	Settling time	$R_L = 600 \Omega$ , $C_L = 100 pF$	0.01%	25°C		3.92			3.92		μs
φm	Phase margin at unity gain	R <sub>L</sub> = 600 Ω,	C <sub>L</sub> = 100 pF	25°C		46°			46°		
	Gain margin			25°C		12			12		dB

<sup>†</sup> Full range is –55°C to 125°C for M level part.



## TLV277x-EP, TLV277xA-EP FAMILY OF 2.7-V HIGH-SLEW-RATE RAIL-TO-RAIL OUTPUT **OPERATIONAL AMPLIFIERS WITH SHUTDOWN** SGLS317A – OCTOBER 2005 – REVISED SEPTEMBER 2007

## electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST COND	PIONE	T <sub>A</sub> †	TL	_V277xl	M	TL	V277xA	M	UNIT
	FARAMETER	TEST COND	THONS	'A'	MIN	TYP	MAX	MIN	TYP	MAX	UNII
			TLV2770/1/2/3	25°C		0.36	2.5		0.36	1.6	
V/10	Input offset voltage	$V_{DD} = \pm 2.5 \text{ V},$ $V_{IC} = 0, V_{O} = 0,$	TEV2770/1/2/3	Full range			2.7			1.9	mV
VIO	input onset voltage	$R_S = 50 \Omega$	TLV2774/5	25°C		8.0	2.5		8.0	2.1	IIIV
		0 2	TLV2774/5	Full range			2.7			2.4	
	Temperature	$V_{DD} = \pm 2.5 V$ ,		25°C							
$\alpha$ VIO	coefficient of input offset voltage	$V_{IC} = 0, V_{O} = 0,$		to 125°C		2			2		μV/°C
	Unser voltage	$R_S = 50 \Omega$	1				00				
١.	Lancet office to comment	$V_{DD} = \pm 2.5 \text{ V},$	TLV/2770/4/2/2	25°C		1	60		1	60	^
liO	Input offset current	$V_{IC} = 0, V_{O} = 0,$ $R_{S} = 50 \Omega$	TLV2770/1/2/3	Full range			125			125	pA
			TLV2774/5	25°C		2	200 60		2	200	
١.		$V_{DD} = \pm 2.5 \text{ V},$	TI V2770/4/2/2	25 0			350			350	
lΒ	Input bias current	$V_{IC} = 0, V_{O} = 0,$ $R_{S} = 50 \Omega$	TLV2770/1/2/3 TLV2774/5	Full range			500			500	pА
-		1.5 - 00 11	TLV2//4/5			0.0	500	0	0.0	500	
				25°C	0 to	-0.3 to		0 to	-0.3 to		
l.,	Common-mode			200	3.7	3.8		3.7	3.8		.,
VICR	input voltage range	CMRR > 60 dB,	$R_S = 50 \Omega$		0	-0.3		0	-0.3		V
			Full range	to	to		to	to			
-				2700	3.7	3.8		3.7	3.8		
		I <sub>OH</sub> = -1.3 mA		25°C	4.0	4.9		4.0	4.9		
Vон	High-level output voltage			Full range	4.8	4.7		4.8	4.7		V
	voltage	$I_{OH} = -4.2 \text{ mA}$	25°C	4.4	4.7		4.4	4.7			
				Full range 25°C	4.4	0.1		4.4	0.1		
		$V_{IC} = 2.5 V$ ,	$I_{OL} = 1.3 \text{ mA}$	Full range		0.1	0.2		0.1	0.2	
VOL	Low-level output voltage			25°C		0.21	0.2		0.21	0.2	V
	· · · · · · · · · · · · · · · · · · ·	$V_{IC} = 2.5 V$ ,	$I_{OL} = 4.2 \text{ mA}$	Full range		0.21	0.6		0.21	0.6	
	Large-signal			25°C	20	450	0.0	20	450	0.0	
A <sub>VD</sub>	differential voltage	$V_{IC} = 2.5 \text{ V},$	$R_L = 10 \text{ k}\Omega,^{\ddagger}$		20	450		20	450		V/mV
V.D	amplification	V <sub>O</sub> = 1 V to 4 V		Full range	13			13			
r <sub>i(d)</sub>	Differential input resistance			25°C		1012			1012		Ω
c <sub>i(c)</sub>	Common-mode input capacitance	f = 10 kHz,		25°C		8			8		pF
z <sub>0</sub>	Closed-loop output impedance	f = 100 kHz,	A <sub>V</sub> = 10	25°C		20			20		Ω
	Common-mode	$V_{IC} = V_{ICR}$ (min),	V <sub>O</sub> = 3.7 V,	25°C	60	96		60	96		
CMRR	rejection ratio	$R_S = 50 \Omega$	<b>5</b> ,	Full range	60	93		60	93		dB
	Supply voltage	V <sub>DD</sub> = 2.7 V to 5 V,	V <sub>IC</sub> = V <sub>DD</sub> /2,	25°C	70	89		70	89		
ksvr	rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	No load	<u> </u>	Full range	70	84		70	84		dB
1	Supply current	Vo = 1.5.V	No lood	25°C		1	2		1	2	m ^
lDD	(per channel)	$V_{O} = 1.5 \text{ V},$	No load	Full range			2			2	mA

<sup>†</sup> Full range is –55°C to 125°C for M level part. ‡ Referenced to 2.5 V



# TLV277x-EP, TLV277xA-EP FAMILY OF 2.7-V HIGH-SLEW-RATE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN SGLS317A - OCTOBER 2005 - REVISED SEPTEMBER 2007

## operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

	D. D. A. W. ETED	TEOT 001	_ +	TI	LV277xM		TLV	/2772xAI	/I	LINUT	
	PARAMETER	TEST CON	DITIONS	T <sub>A</sub> †	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		V 45V	0 400 - 5	25°C	5	10.5		5	10.5		
SR	Slew rate at unity gain	$V_{O(PP)} = 1.5 \text{ V},$ $R_{L} = 10 \text{ k}\Omega$	CL = 100 pr,	Full range	4.7	6		4.7	6		V/μs
	Equivalent input	f = 1 kHz		0500		17			17		->/// <del>  </del>
V <sub>n</sub>	noise voltage	f = 10 kHz		25°C		12			12		nV/√Hz
,,	Peak-to-peak	f = 0.1 Hz to 1 Hz		0500		0.33			0.33		μV
V <sub>N(PP)</sub>	equivalent input noise voltage	f = 0.1 Hz to 10 H	lz	25°C		0.86			0.86		μV
In	Equivalent input noise current	f = 100 Hz		25°C		0.6		0.6			fA/√ <del>Hz</del>
			A <sub>V</sub> = 1			0.005%			0.005%		
THD + N	Total harmonic distortion plus noise	$R_L = 600 \Omega$ , f = 1  kHz	A <sub>V</sub> = 10	25°C		0.016%			0.016%		
	alotoritori piao ilioto		$A_{V} = 100$			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, C <sub>L</sub> = 100 pF	$R_L = 600 \Omega$ ,	25°C		5.1			5.1		MHz
	Outline the	$A_V = -1$ , Step = 1.5 V to 3.5 V.	0.1%	0500		0.134			0.134		
t <sub>S</sub>	Settling time	$R_L = 600 \Omega$ , $C_L = 100 pF$	0.01%	25°C		1.97			1.97		μs
φm	Phase margin at unity gain	R <sub>L</sub> = 600 Ω,	C <sub>L</sub> = 100 pF	25°C		46°			46°		
	Gain margin		-	25°C		12			12		dB

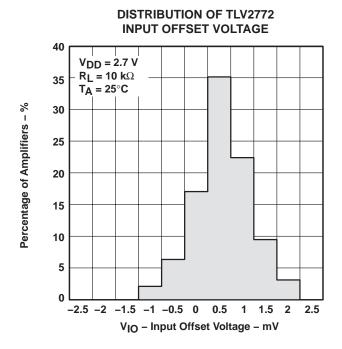
<sup>†</sup> Full range is –55°C to 125°C for M level part.



### **Table of Graphs**

			FIGURE
VIO	Input offset voltage	Distribution vs Common-mode input voltage Distribution	1,2 3,4 5,6
I <sub>IB</sub> /I <sub>IO</sub>	Input bias and input offset currents	vs Free-air temperature	7
Vон	High-level output voltage	vs High-level output current	8,9
VOL	Low-level output voltage	vs Low-level output current	10,11
V <sub>O(PP)</sub>	Maximum peak-to-peak output voltage	vs Frequency	12,13
los	Short-circuit output current	vs Supply voltage vs Free-air temperature	14 15
VO	Output voltage	vs Differential input voltage	16
AVD	Large-signal differential voltage amplification and phase margin	vs Frequency	17,18
AVD	Differential voltage amplification	vs Load resistance vs Free-air temperature	19 20,21
z <sub>O</sub>	Output impedance	vs Frequency	22,23
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	24 25
ksvr	Supply-voltage rejection ratio	vs Frequency	26,27
I <sub>DD</sub>	Supply current (per channel)	vs Supply voltage	28
SR	Slew rate	vs Load capacitance vs Free-air temperature	29 30
VO	Voltage-follower small-signal pulse response		31,32
٧o	Voltage-follower large-signal pulse response		33,34
VO	Inverting small-signal pulse response		35,36
VO	Inverting large-signal pulse response		37,38
V <sub>n</sub>	Equivalent input noise voltage	vs Frequency	39,40
	Noise voltage (referred to input)	Over a 10 second period	41
THD + N	Total harmonic distortion plus noise	vs Frequency	42,43
	Gain-bandwidth product	vs Supply voltage	44
B <sub>1</sub>	Unity-gain bandwidth	vs Load capacitance	45
φm	Phase margin	vs Load capacitance	46
	Gain margin	vs Load capacitance	47
	Amplifier with shutdown pulse turnon/off characteristics		48 – 50
	Supply current with shutdown pulse turnon/off characteristics		51 – 53
	Shutdown supply current	vs Free-air temperature	54
	Shutdown forward/reverse isolation	vs Frequency	55, 56





DISTRIBUTION OF TLV2772 INPUT OFFSET VOLTAGE

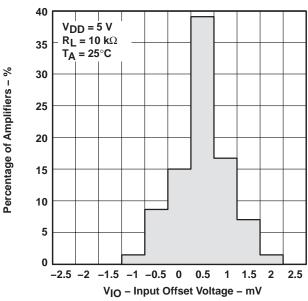
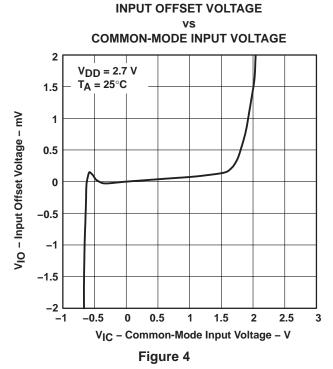


Figure 2

Figure 3



INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

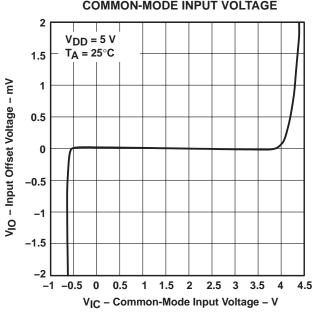


Figure 5

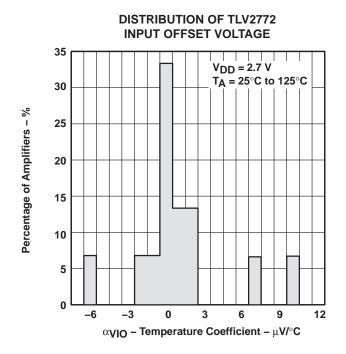


Figure 6

## **INPUT BIAS AND OFFSET CURRENT** vs FREE-AIR TEMPERATURE IB and IIO - Input Bias and Input Offset Currents - nA 0.20 $V_{DD} = 5 V$ $V_{IC} = 0$ $V_O = 0$ $R_S = 50 \Omega$ 0.15 lιΒ 0.10 0.05 lΙΟ

**DISTRIBUTION OF TLV2772 INPUT OFFSET VOLTAGE** 

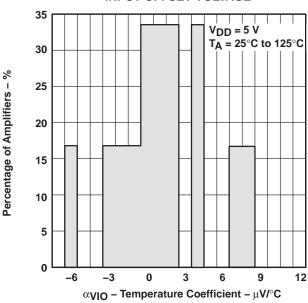
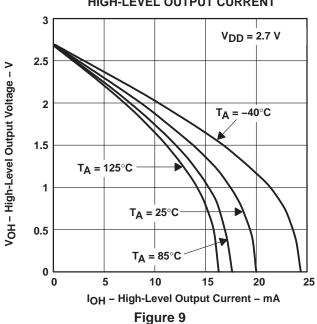


Figure 7

### **HIGH-LEVEL OUTPUT VOLTAGE** vs **HIGH-LEVEL OUTPUT CURRENT**



-75

-50

-25

0

Figure 8

25

 $T_A$  – Free-Air Temperature –  $^{\circ}C$ 

50

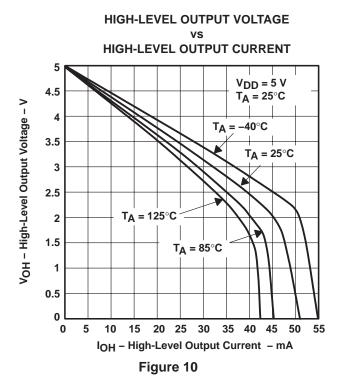
75

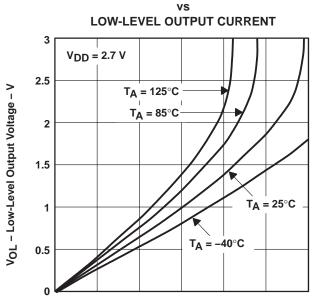
100

125

**LOW-LEVEL OUTPUT VOLTAGE** 

### TYPICAL CHARACTERISTICS



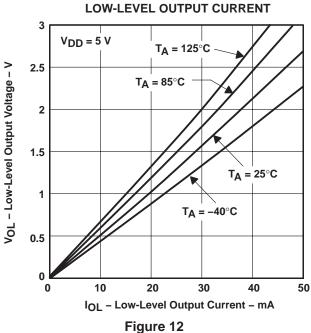


10

Figure 11

0





MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE

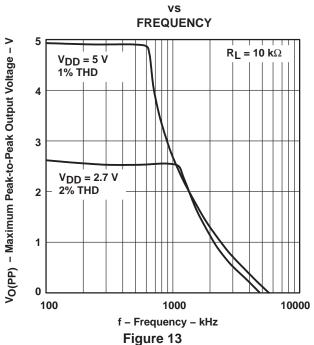
15

IOL - Low-Level Output Current - mA

20

25

30



### **MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE**

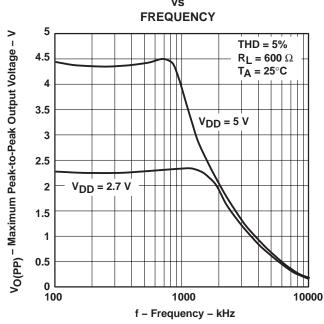
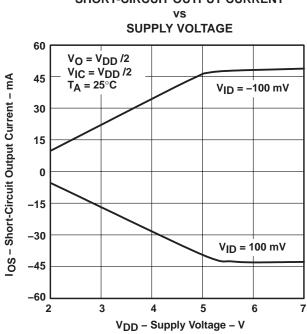


Figure 14

### SHORT-CIRCUIT OUTPUT CURRENT



### SHORT-CIRCUIT OUTPUT CURRENT



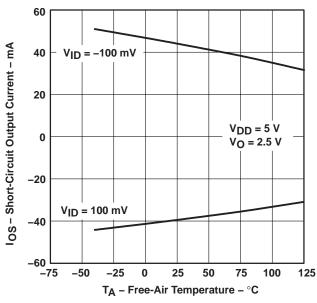


Figure 16

### **OUTPUT VOLTAGE DIFFERENTIAL INPUT VOLTAGE**

Figure 15

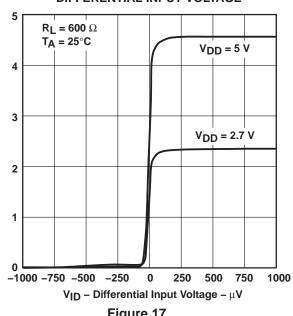


Figure 17

Vo - Output Voltage - V

## LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

vs **FREQUENCY** 100 300 A VD - Large-Signal Differential Amplification - dB  $V_{DD} = 2.7 \text{ V}$  $R_L = 600 \Omega$  $C_{L} = 600 \text{ pF}$ 80 240 T<sub>A</sub> = 25°C AVD m - Phase Margin - degrees 60 180 40 120 Phase 60 20 0 0 -20 -60 -90 -40 100 1k 10k 100k 1M 10M

f – Frequency – Hz Figure 18

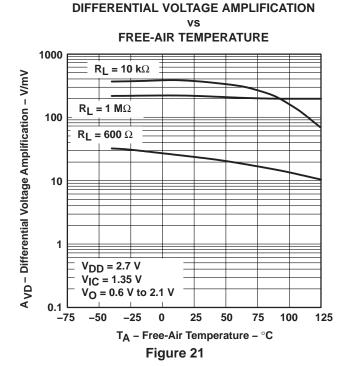
## LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN

٧S **FREQUENCY** 100 300 A<sub>VD</sub> - Large-Signal Differential Amplification - dB  $V_{DD} = 5 V$  $R_L = 600 \Omega$  $C_{L}^{-} = 600 \text{ pF}$ 80 240 T<sub>A</sub> = 25°C Phase Margin – degrees  $A_{VD}$ 60 180 40 120 **Phase** 20 60 0 0 **₽** -20 -60 -90 -40 10k 100k 100 1k 1M 10M f - Frequency - Hz

Figure 19

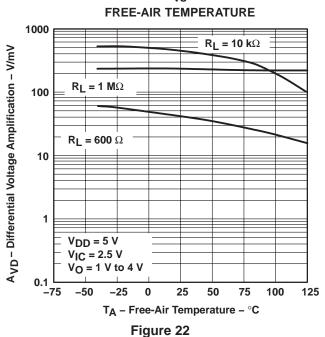


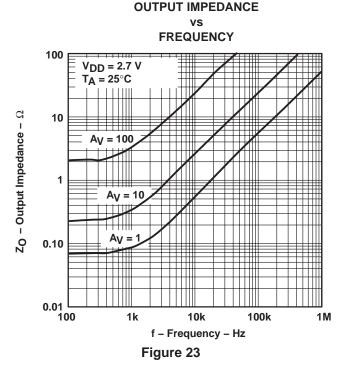
### **DIFFERENTIAL VOLTAGE AMPLIFICATION** LOAD RESISTANCE 250 T<sub>A</sub> = 25°C A<sub>VD</sub> - Differential Voltage Amplification - V/mV 200 $V_{DD} = 2.7 \text{ V}$ $V_{DD} = 5 V$ 150 100 50 0.1 10 100 1000 $R_L$ – Load Resistance – $k\Omega$



## DIFFERENTIAL VOLTAGE AMPLIFICATION vs

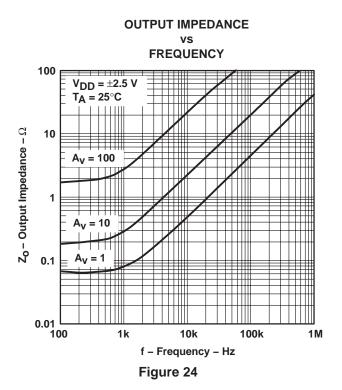
Figure 20





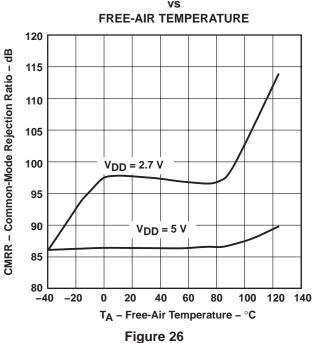
**COMMON-MODE REJECTION RATIO** 

### TYPICAL CHARACTERISTICS



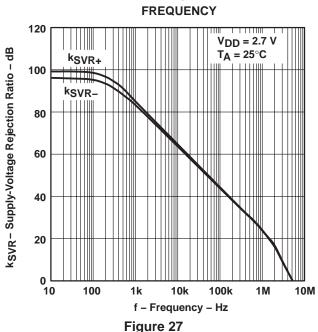
### **FREQUENCY** 90 V<sub>DD</sub> = 2.7 V $V_{IC} = 1.35 \text{ V}$ CMRR - Common-Mode Rejection Ratio - dB and 2.5 V 1.1111111 T<sub>A</sub> = 25°C $V_{DD} = 5 V$ 80 70 60 50 40 10 100 1k 10k 100k 1M 10M f - Frequency - Hz

## COMMON-MODE REJECTION RATIO



## SUPPLY-VOLTAGE REJECTION RATIO VS

Figure 25



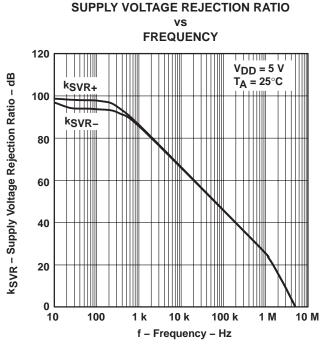


Figure 28



**SUPPLY CURRENT (PER CHANNEL)** 

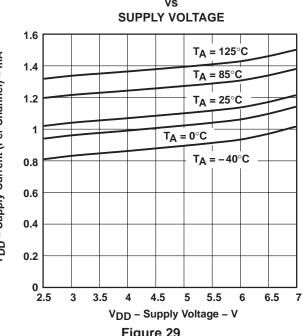
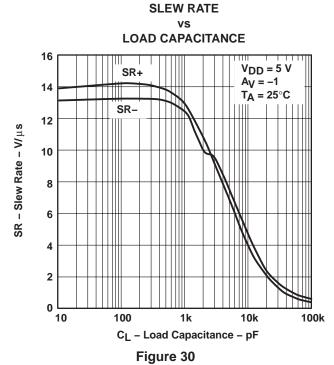
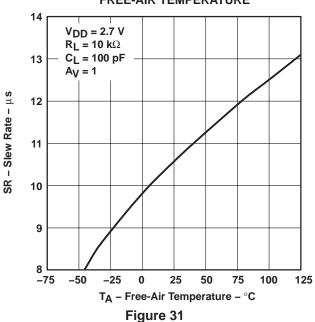


Figure 29



**SLEW RATE** FREE-AIR TEMPERATURE

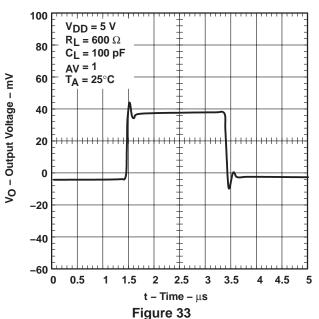


### TYPICAL CHARACTERISTICS

### **VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE** 100 $V_{DD} = 2.7 V$ $R_L = 600 \Omega$ 80 $C_L = 100 pF$ AV = 1Vo - Output Voltage - mV 60 T<sub>A</sub> = 25°C 40 20 0 -20 -40 -60 0.5 2.5 4 4.5 5 0 1 1.5 2 3 3.5 $\textbf{t-Time}-\mu\textbf{s}$

Figure 32

### **VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE**



**VOLTAGE-FOLLOWER** LARGE-SIGNAL PULSE RESPONSE

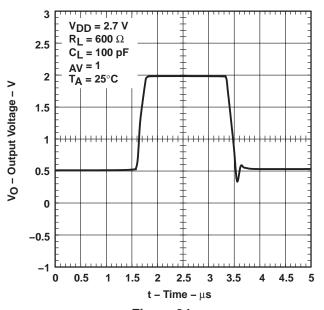


Figure 34

### **VOLTAGE-FOLLOWER** LARGE-SIGNAL PULSE RESPONSE

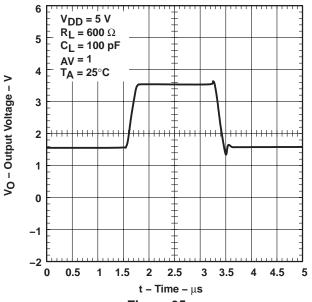


Figure 35

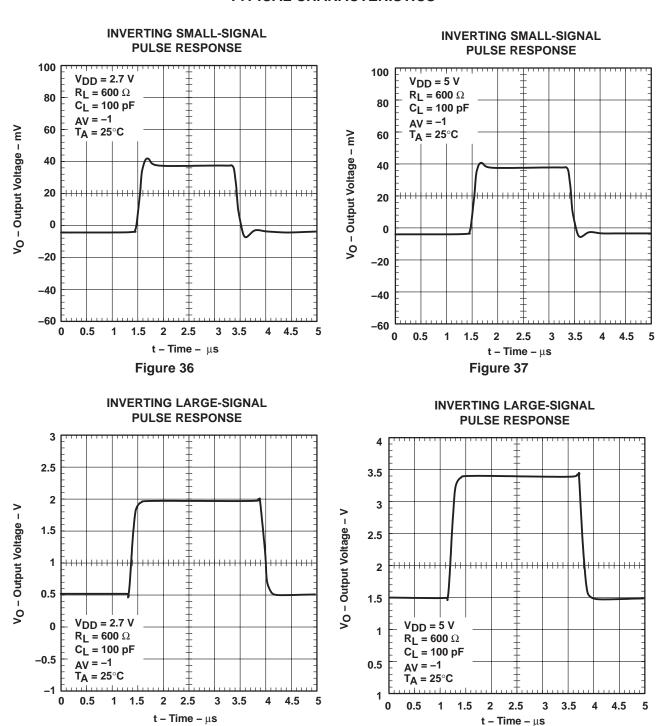
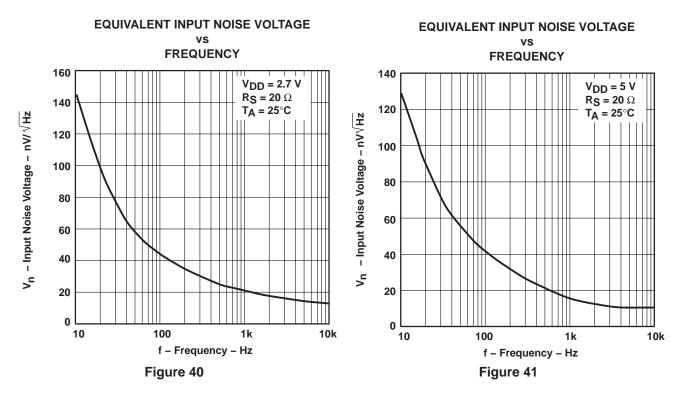




Figure 38

Figure 39

### **TYPICAL CHARACTERISTICS**



### NOISE VOLTAGE OVER A 10 SECOND PERIOD

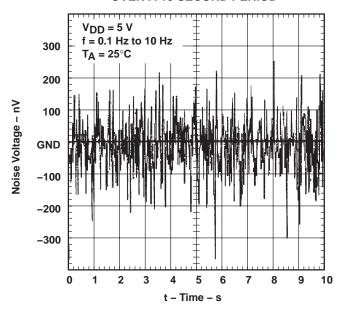
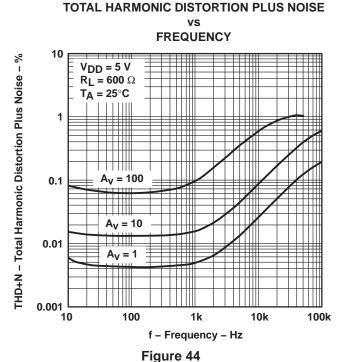


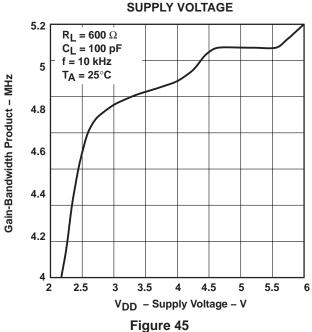
Figure 42

### TOTAL HARMONIC DISTORTION PLUS NOISE vs **FREQUENCY** THD+N – Total Harmonic Distortion Plus Noise – % $V_{DD} = 2.7 V$ $R_L = 600 \Omega$ $T_A = 25^{\circ}C$ $A_{V} = 100$ 0.1 $A_{V} = 10$ $A_V = 1$ 0.01 0.001 10 100 1k 10k 100k f - Frequency - Hz

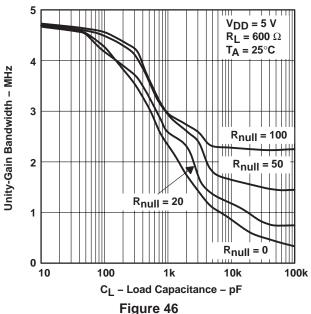


## **GAIN-BANDWIDTH PRODUCT**

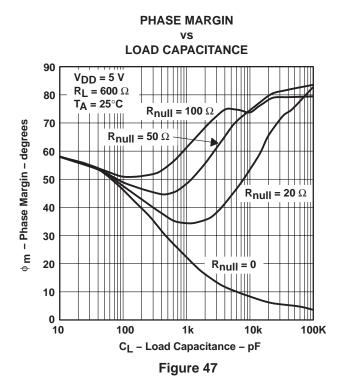
Figure 43

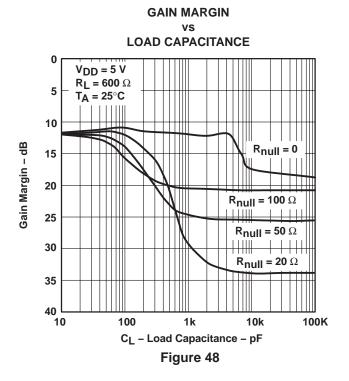


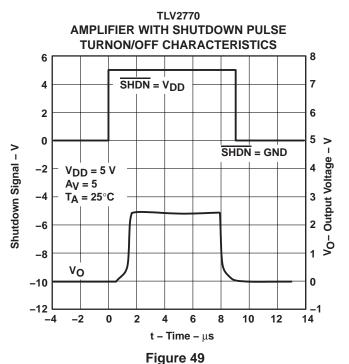
## **UNITY-GAIN BANDWIDTH** LOAD CAPACITANCE

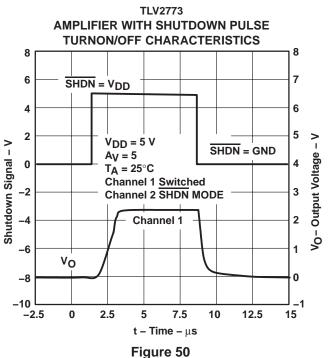


### TYPICAL CHARACTERISTICS

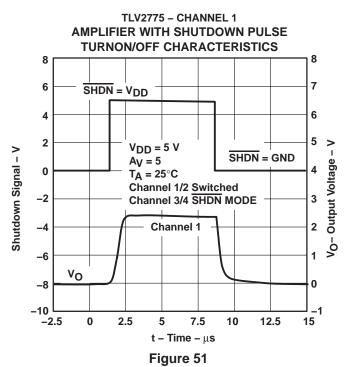


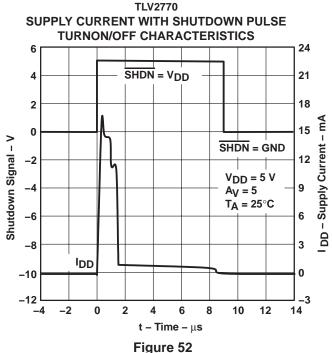


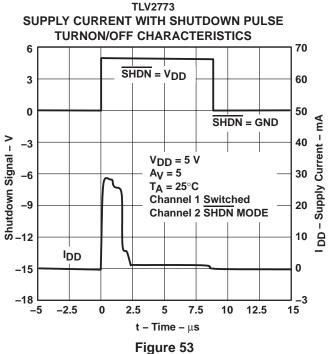




### TYPICAL CHARACTERISTICS







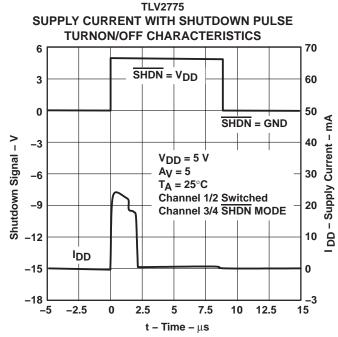
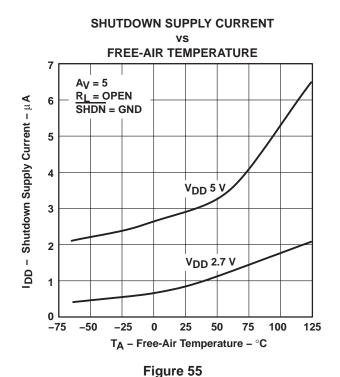


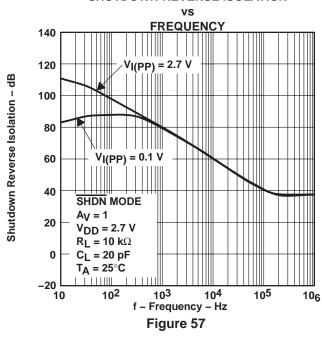
Figure 54

### **TYPICAL CHARACTERISTICS**



TLV2770 SHUTDOWN FORWARD ISOLATION vs **FREQUENCY** 140 120 Shutdown Forward Isolation - dB 100 80 60 40 SHDN MODE  $A_V = 1$ 20  $V_{DD} = 2.7 V$  $R_L = 10 \text{ k}\Omega$  $C_L = 20 pF$ 0 TA = 25°C 1.1111111 -20102 103 104 105 10 106 f - Frequency - Hz Figure 56

TLV2770 SHUTDOWN REVERSE ISOLATION



### PARAMETER MEASUREMENT INFORMATION

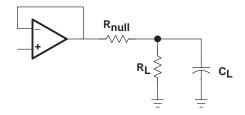


Figure 58

### driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ( $R_{NULL}$ ) with the output of the amplifier (See Figure 59). A minimum value of 20  $\Omega$  should work well for most applications.

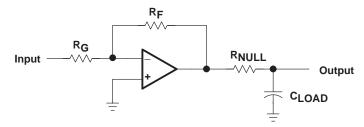


Figure 59. Driving a Capacitive Load



### APPLICATION INFORMATION

### offset voltage

The output offset voltage,  $(V_{OO})$  is the sum of the input offset voltage  $(V_{IO})$  and both input bias currents  $(I_{IB})$  times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

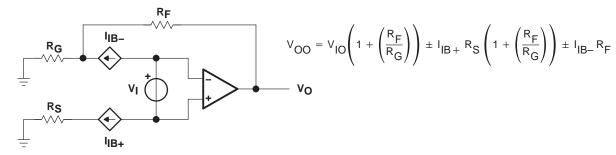


Figure 60. Output Offset Voltage Model

### general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 61).

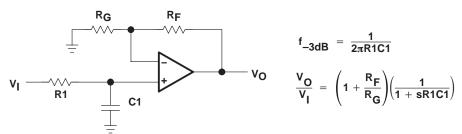


Figure 61. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

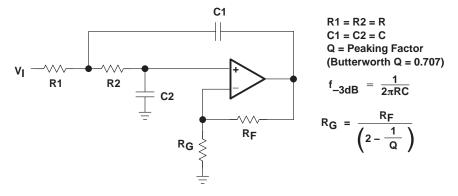


Figure 62. Two Pole Low Pass Sallen Key Filter

### **APPLICATION INFORMATION**

### using the TLV2772 as an accelerometer interface

The schematic (see Figure 63) shows the ACH04-08-05 interfaced to the TLV1544 10-bit analog-to-digital converter (ADC).

The ACH04-08-05 is a shock sensor designed to convert mechanical acceleration into electrical signals. The sensor contains three piezoelectric sensing elements oriented to simultaneously measure acceleration in three orthogonal, linear axes (x, y, z). The operating frequency is 0.5 Hz to 5 kHz. The output is buffered with an internal JFET and has a typical output voltage of 1.80 mV/g for the x and y axis and 1.35 mV/g for the z axis.

Amplification and frequency shaping of the shock sensor output is done by the TLV2772 rail-to-rail operational amplifier. The TLV2772 is ideal for this application as it offers high input impedance, good slew rate, and excellent dc precision. The rail-to-rail output swing and high output drive are perfect for driving the analog input of the TLV1544 ADC.

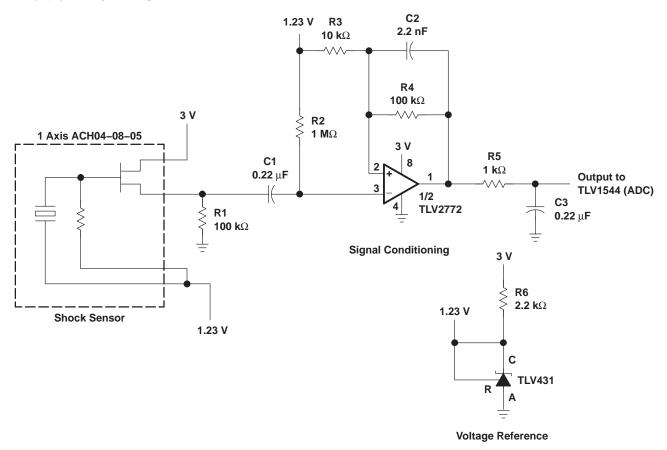


Figure 63. Accelerometer Interface Schematic

The sensor signal must be amplified and frequency-shaped to provide a signal the ADC can properly convert into the digital domain. Figure 63 shows the topology used in this application for one axis of the sensor. This system is powered from a single 3-V supply. Configuring the TLV431 with a 2.2-k $\Omega$  resistor produces a reference voltage of 1.23 V. This voltage is used to bias the operational amplifier and the internal JFETs in the shock sensor.



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### APPLICATION INFORMATION

### gain calculation

Since the TLV2772 is capable of rail-to-rail output using a 3-V supply,  $V_O = 0$  (min) to 3 V (max). With no signal from the sensor, nominal  $V_O =$  reference voltage = 1.23 V. Therefore, the maximum negative swing from nominal is 0 V - 1.23 V = -1.23 V and the maximum positive swing is 3 V - 1.23 V = 1.77 V. By modeling the shock sensor as a low impedance voltage source with output of 2.25 mV/g (max) in the x and y axis and 1.70 mV/g (max) in the z axis, the gain of the circuit is calculated by equation 1.

$$Gain = \frac{Output Swing}{Sensor Signal \times Acceleration}$$
 (1)

To avoid saturation of the operational amplifier, the gain calculations are based on the maximum negative swing of -1.23 V and the maximum sensor output of 2.25 mV/g (x and y axis) and 1.70 mV/g (z axis).

Gain (x, y) = 
$$\frac{-1.23 \text{ V}}{2.25 \text{ mV/g} \times -50 \text{ g}}$$
 = 10.9 (2)

and

Gain (z) = 
$$\frac{-1.23 \text{ V}}{1.70 \text{ mV/g} \times -50 \text{ g}}$$
 = 14.5 (3)

By selecting R3 = 10 k $\Omega$  and R4 = 100 k $\Omega$ , in the x and y channels, a gain of 11 is realized. By selecting R3 = 7.5 k $\Omega$  and R4 = 100 k $\Omega$ , in the z channel, a gain of 14.3 is realized. The schematic shows the configuration for either the x or y axis.

#### bandwidth calculation

To calculate the component values for the frequency shaping characteristics of the signal conditioning circuit, 1 Hz and 500 Hz are selected as the minimum required 3-dB bandwidth.

To minimize the value of the input capacitor (C1) required to set the lower cutoff frequency requires a large value resistor for R2. A 1-M $\Omega$  resistor is used in this example. To set the lower cutoff frequency, the required capacitor value for C1 is:

$$C1 = \frac{1}{2\pi f_{1,OW} R_2} = 0.159 \,\mu\text{F} \tag{4}$$

Using a value of 0.22 μF, a more common value of capacitor, the lower cutoff frequency is 0.724 Hz.

To minimize the phase shift in the feedback loop caused by the input capacitance of the TLV2772, it is best to minimize the value of the feedback resistor R4. However, to reduce the required capacitance in the feedback loop a large value for R4 is required. Therefore, a compromise for the value of R4 must be made. In this circuit, a value of  $100 \text{ k}\Omega$  has been selected. To set the upper cutoff frequency, the required capacitor value for C2 is:

$$C2 = \frac{1}{2\pi f_{HIGH} R_4} = 3.18 \,\mu\text{F} \tag{5}$$

Using a 2.2-nF capacitor, the upper cutoff frequency is 724 Hz.

R5 and C3 also cause the signal response to roll off. Therefore, it is beneficial to design this roll-off point to begin at the upper cutoff frequency. Assuming a value of 1 k $\Omega$  for R5, the value for C3 is calculated to be 0.22  $\mu$ F.

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### **APPLICATION INFORMATION**

### circuit layout considerations

To achieve the levels of high performance of the TLV277x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all
  components with a low inductive ground connection. However, in the areas of the amplifier inputs and
  output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins
  will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board
  is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series
  inductance has been minimized. To realize this, the circuit layout should be made as compact as possible,
  thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of
  the amplifier. Its length should be kept as short as possible. This minimizes stray capacitance at the input
  of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high
  performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of
  surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small
  size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray
  inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be
  kept as short as possible.



### APPLICATION INFORMATION

### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 64 and is calculated by the following formula:

$$P_{D} = \left(\frac{T_{MAX} - T_{A}}{\theta_{JA}}\right)$$

Where:

P<sub>D</sub> = Maximum power dissipation of TLV277x IC (watts)

T<sub>MAX</sub> = Absolute maximum junction temperature (150°C)

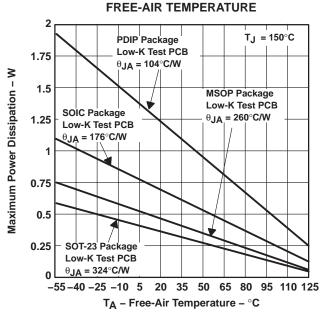
 $T_A$  = Free-ambient air temperature (°C)

 $\theta_{JA} = \theta_{JC} + \theta_{CA}$ 

 $\theta_{JC}$  = Thermal coefficient from junction to case

 $\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)

## MAXIMUM POWER DISSIPATION vs



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 64. Maximum Power Dissipation vs Free-Air Temperature

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### **APPLICATION INFORMATION**

### shutdown function

Three members of the TLV277x family (TLV2770/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.8  $\mu$ A/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care must be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to  $V_{DD}$ /2. Therefore, when operating the device with split supply voltages (e.g.  $\pm 2.5$  V), the shutdown terminal must be pulled to  $V_{DD}$ -(not GND) to disable the operational amplifier.

The amplifier output with a shutdown pulse is shown in Figures 48, 49, and 50. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables. The bump on the rising edge of the TLV2770 output waveform is due to the start-up circuit on the bias generator. For the dual and quad (TLV2773/5), this bump is attributed to the bias generator's start-up circuit as well as the crosstalk between the other channel(s), which are in shutdown.

Figures 55 and 56 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by  $\pm 1.35$ -V supplies and configured as a voltage follower ( $A_V = 1$ ). The isolation performance is plotted across frequency for both 0.1 V<sub>PP</sub> and 2.7 V<sub>PP</sub> input signals. During normal operation, the amplifier would not be able to handle a 2.7-V<sub>PP</sub> input signal with a supply voltage of  $\pm 1.35$  V since it exceeds the common-mode input voltage range ( $V_{ICR}$ ). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.



### APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim  $Parts^{TM}$  Release 8, the model generation software used with Microsim  $PSpice^{TM}$ . The Boyle macromodel (see Note 5) and subcircuit in Figure 65 are generated using the TLV2772 typical electrical and operating characteristics at  $T_A = 25^{\circ}C$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

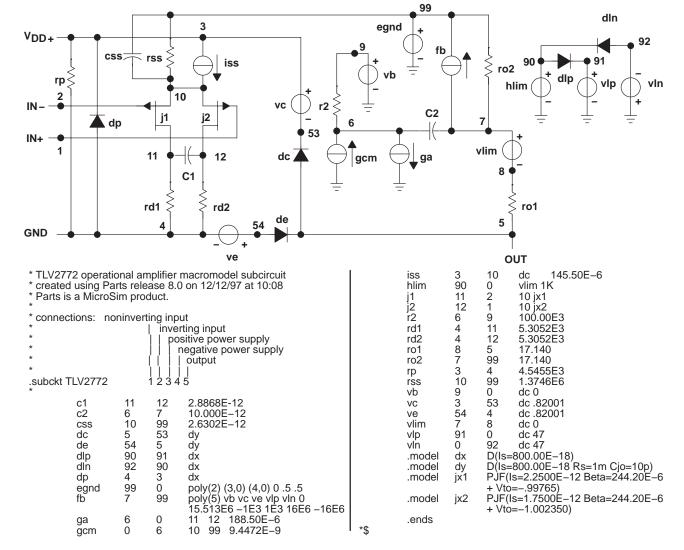


Figure 65. Boyle Macromodel and Subcircuit

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31-May-2014

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	_	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLV2772AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2772AE	Samples
TLV2774AMDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2774AEP	Samples
TLV2774MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2774EP	Samples
V62/06607-02XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2772AE	Samples
V62/06607-03YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2774EP	Samples
V62/06607-04YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2774AEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.







31-May-2014

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF TLV2772A-EP, TLV2774-EP, TLV2774A-EP:

Automotive: TLV2772A-Q1

Military: TLV2772AM

### NOTE: Qualified Version Definitions:

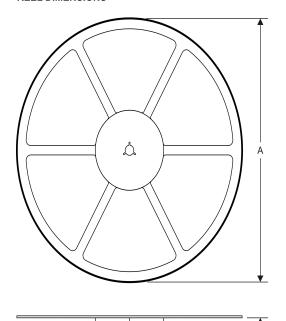
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military QML certified for Military and Defense Applications

### PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION

### **REEL DIMENSIONS**



### **TAPE DIMENSIONS**



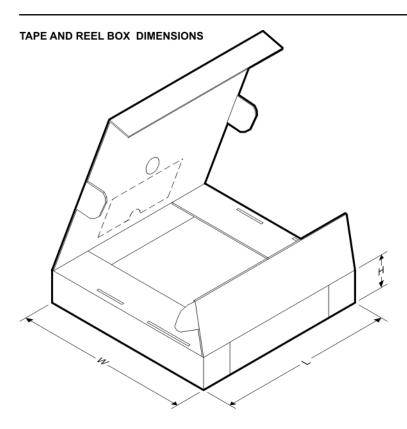
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2772AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2774AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2774MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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\*All dimensions are nominal

7 III dimensione die nomina									
Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)		
TLV2772AMDREP	SOIC	D	8	2500	367.0	367.0	35.0		
TLV2774AMDREP	SOIC	D	14	2500	333.2	345.9	28.6		
TLV2774MDREP	SOIC	D	14	2500	333.2	345.9	28.6		

### D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



## D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### D (R-PDSO-G8)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



## D (R-PDSO-G8)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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