Features



Single-Phase, Synchronous MOSFET Drivers

General Description

The MAX8791/MAX8791B are single-phase, synchronous, noninverting MOSFET drivers. The MAX8791/ MAX8791B are intended to work with controller ICs like the MAX8736 or MAX8786, in multiphase notebook CPU core regulators.

The regulators can either step down directly from the battery voltage to create the core voltage, or step down from the main system supply. The single-stage conversion method allows the highest possible efficiency, while the 2-stage conversion at higher switching frequency provides the minimum possible physical size.

The low-side drivers are optimized to drive 3nF capacitive loads with 4ns/8ns typical fall/rise times, and the high-side driver with 8ns/10ns typical fall/rise times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency.

The MAX8791/MAX8791B are available in a small, leadfree, 8-pin, 3mm x 3mm TQFN package.

Applications

Notebooks/Desktops/Servers **CPU Core Power Supplies** Multiphase Step-Down Converters

♦ Single-Phase, Synchronous MOSFET Drivers

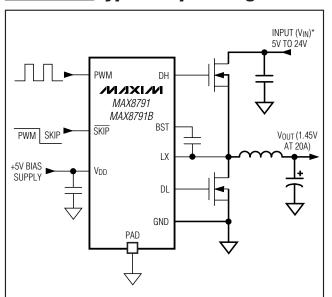
- ♦ 0.5Ω Low-Side On-Resistance
- ♦ 0.7Ω High-Side On-Resistance
- ♦ 8ns Propagation Delay
- **♦ 15ns Minimum Guaranteed Dead Time**
- ♦ Integrated Boost "Diode"
- ♦ 2V to 24V Input Voltage Range
- ♦ Selectable Pulse-Skipping Mode
- ♦ Low-Profile TQFN Package

Ordering Information

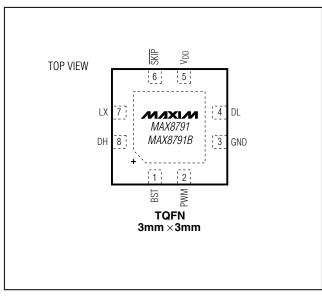
PART	TEMP RANGE	PIN-PACKAGE
MAX8791GTA+	-40°C to +105°C	8 TQFN-EP*
MAX8791BGTA+	-40°C to +105°C	8 TQFN-EP*

⁺Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



Pin Configuration



MIXIM

Maxim Integrated Products 1

^{*}EP = Exposed pad.

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	0.3V to +6V	Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
SKIP to GND	0.3V to +6V	8-Pin 3mm x 3mm TQFN	
PWM to GND	0.3V to +6V	(derate 23.8mW/°C above +70°C)	1904mW
DL to GND	$0.3V \text{ to } (V_{DD} + 0.3V)$	Operating Temperature Range	40°C to +105°C
BST to GND	0.3V to +36V	Junction Temperature	+150°C
DH to LX0	.3V to (V _{BST} + 0.3V)	Storage Temperature Range	65°C to +150°C
BST to V _{DD}	0.3V to +30V	Lead Temperature (soldering, 10s)	+300°C
BST to LX	0.3V to +6V	Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = V_{SKIP} = 5V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V _{DD}			4.20		5.50	V
V _{DD} Undervoltage		Rising edge, PWM disabled below this level			3.7		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Lockout Threshold	V _{UVLO(VDD)}	Falling edge, PWM disable	d below this level	3.0	3.5	4.0	V
		PWM = open; after the shutdown hold time has expired			0.08	0.2	
Quiescent Supply Current (V _{DD})	I _{DD}	SKIP = GND, PWM = GND, LX = GND (after zero crossing)		0	0.25	0.5	mA
(188)		$\overline{\text{SKIP}} = \text{GND or V}_{\text{DD}}, \text{PWM}$	<u> </u>		0.6	1.5	1
DRIVERS		CINI - GIND OF VDD, I WIN	- vbb, vb31 - 3v	<u> </u>	0.0	1.0	
	ton(MIN)	Minimum on-time			50		
PWM Pulse Width	toff(MIN)	Minimum off-time			300		ns
DL Propagation Delay	tpwm-DL	PWM high to DL low			10		ns
DH Propagation Delay	tpwm-DH	PWM low to DH low			14		ns
	t _{DL-DH}	DL falling to DH rising	$T_A = 0$ °C to +85°C	15	30		ns
DL-to-DH Dead Time			$T_A = -40^{\circ}\text{C to} + 105^{\circ}\text{C}$	15			
	t _{DH-DL}	DH falling to DL rising	$T_A = 0$ °C to +85°C	15	30		ns
DH-to-DL Dead Time			$T_A = -40^{\circ}C \text{ to } +105^{\circ}C$	15			
DI T :: T	t _{F_DL}	Falling, 3.0nF load			12		
DL Transition Time	t _{R_DL}	Rising, 3.0nF load			14		ns
DH Transition Time	tF_DH	Falling, 3.0nF load			8		
DH Transition Time	t _{R_DH}	Rising, 3.0nF load			10		ns
DI I Driver On Decistores	D	DCT I V foresed to CV	DH, high state (pullup)		0.9 2.5	-	
DH Driver On-Resistance	Ron(dh)	BST-LX forced to 5V	DH, low state (pulldown)		0.7	2.3	Ω
DL Driver On-Resistance	Powpu	DL, high state (pullup) DL, low state (pulldown)			0.7	1.8	Ω
DL DIIVEI OII-NESISIAIICE	Ron(dl)				0.5	1.2	52
DH Driver Source Current	IDH_SOURCE	DH forced to 2.5V, BST - LX forced to 5V			2.2		А
DH Driver Sink Current	IDH_SINK	DH forced to 2.5V, BST - LX forced to 5V			2.7		А
DL Driver Source Current	I _{DL_} SOURCE	DL forced to 2.5V			2.7		Α
DL Driver Sink Current	I _{DL_SINK}	DL forced to 2.5V			8		А
Zero-Crossing Threshold	V_{ZX}	GND - LX, SKIP = GND			3		mV
Boost On-Resistance	RON(BST)	$V_{DD} = 5V$, DH = LX = GND (pulldown state), $I_{BST} = 10$ mA			5	12	Ω

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ELECTRICAL CHARACTERISTICS (continued)

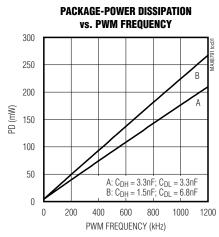
(Circuit of Figure 1, $V_{DD} = V_{\overline{SKIP}} = 5V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

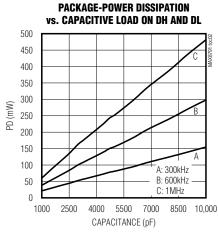
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		High (DH = high; DL = low)	V _{DD} - 0.4			
PWM Input Levels		Midlevel	V _{DD} /2 - 0.4		V _{DD} /2 + 0.4	V
		Low (DH = low; DL = high)			0.4	
DWM Input Current	IPWM	Sink; PWM forced to V _{DD}	-400	-200	-80	μА
PWM Input Current		Source; PWM forced to GND	80	+200	400	
Midlevel Shutdown Hold Time	t _{MID}		120	300	600	ns
CI/ID Invest Threehold		Rising edge		1.7	2.4	V
SKIP Input Threshold		Falling edge	0.8	1.5]
SKIP Input Current	ISKIP	Sink; SKIP forced to 0.8V to V _{DD} , T _A = +25°C	-4	-2	-0.5	μΑ
Thermal-Shutdown Threshold	T _{SHDN}	Hysteresis = 20°C		+160		°C

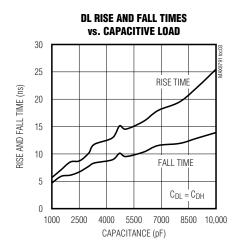
Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed through correlation using statistical-quality-control (SQC) methods.

Typical Operating Characteristics

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_{A} = +25°C, unless otherwise noted.)

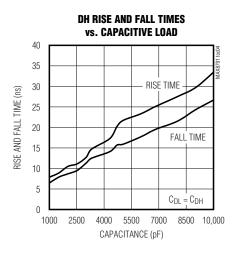


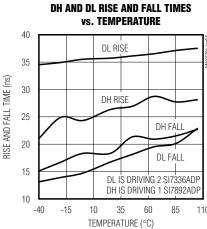


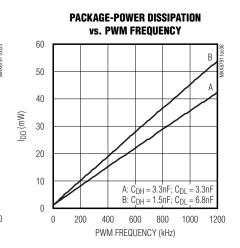


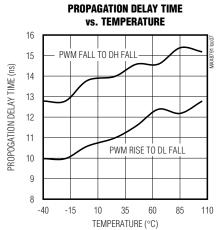
Typical Operating Characteristics (continued)

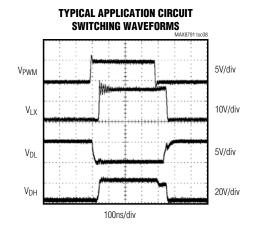
(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)

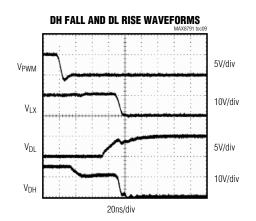


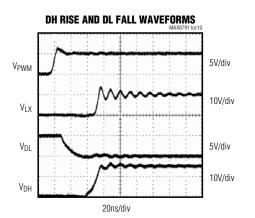






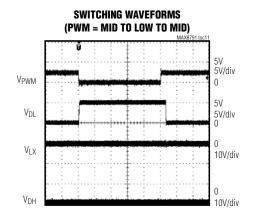


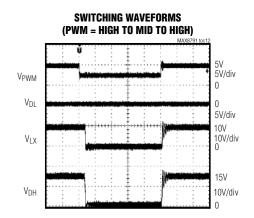




Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DD} = 5V, C_{DH} = 3nF, C_{DL} = 3nF, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	BST	Boost Flying-Capacitor Connection. Gate-drive power supply for DH high-side gate driver. Connect a 0.1µF or 0.22µF capacitor between BST and LX.
2	PWM	PWM Input Pin. Noninverting DH control input from the controller IC: Logic high: DH = high (BST), DL = low (PGND). Midlevel: After the midlevel hold time expires, the controller enters standby mode. DH and DL pulled low. Logic low: DH = low (LX), DL = high (VDD) when SKIP = high. Internal pullup and pulldown resistors create the midlevel and prevent the controller from triggering an on-time if this input is left unconnected (not soldered properly) or driven by a high impedance.
3	GND	Power Ground for the DL Gate Drivers and Analog Ground. Connect exposed pad to GND.
4	DL	PWM Low-Side Gate-Driver Output. Swings between GND and VDD. DL forced high in shutdown.
5	V _{DD}	Supply Voltage Input for the DL Gate Drivers. Connect to 4.2V to 5.5V supply and bypass to GND with a 1µF ceramic capacitor.
6	SKIP	Pulse-Skipping Mode Pin. Enable pulse-skipping mode (zero-crossing comparator enabled) when the driver is operating in SKIP mode: SKIP = V _{DD} PWM mode SKIP = GND SKIP mode An internal pulldown current pulls the controller into the low-power pulse-skipping state if this input is left unconnected (not soldered properly) or driven by a high impedance.
7	LX	Switching Node and Inductor Connection. Low-power supply for the DH high-side gate driver. LX connects to the skip-mode zero-crossing comparator.
8	DH	External High-Side nMOSFET Gate-Driver Output. Swings between LX and BST.
_	EP	Exposed Pad. Connect to ground through multiple vias to reduce the thermal impedance.

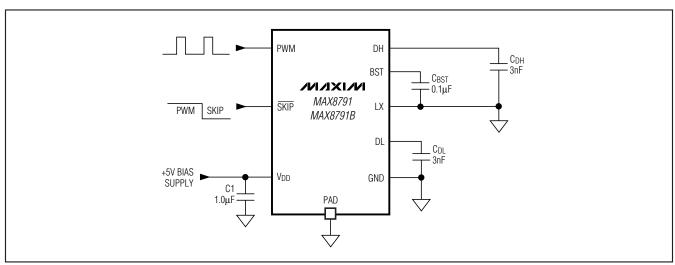


Figure 1. Test Circuit

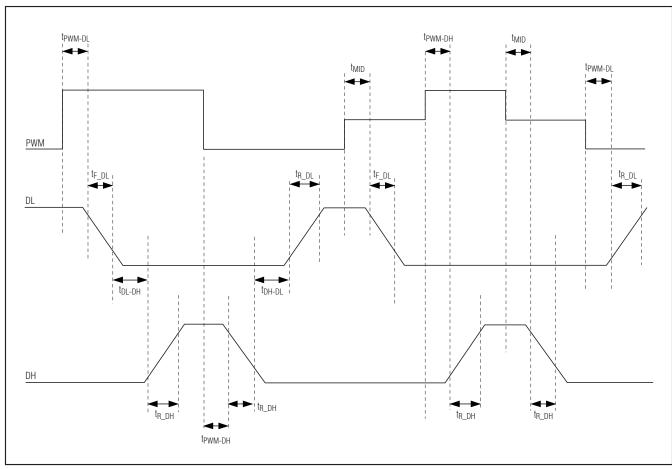


Figure 2. Timing Diagram

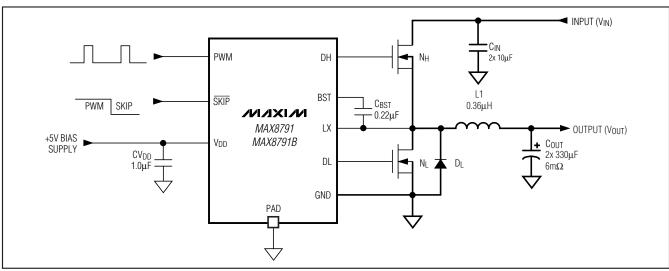


Figure 3. Typical MOSFET-Driver Application Circuit

Table 1. Typical Components

DESIGNATION	QTY	COMPONENT SUPPLIERS
NH	1 per phase	Siliconix Si4860DY
NL	1–2 per phase	Siliconix Si4336DY
BST Capacitor (C _{BST})	1 per phase	0.1µF or 0.22µF ceramic capacitor
Schottky Diode	Optional	3A, 40V Schottky diode
Inductor (L1)	1 per phase	$0.36\mu H$, $26A$, $0.9m\Omega$ power inductor
Output Capacitors (C _{OUT})	1–2 per phase	330μF, 6m Ω per phase
Input Capacitors (C _{IN})	1-2 per phase	10μF, 25V X5R ceramic capacitors

Detail Description

The MAX8791/MAX8791B single-phase gate drivers, along with the MAX8736 or MAX8786 multiphase controllers, provide flexible multiphase CPU core-voltage supplies. The low driver resistance allows up to 7A output peak current. Each MOSFET driver in the MAX8791/MAX8791B is capable of driving 3nF capacitive loads with only 9ns propagation delay and 4ns/8ns (typ) fall/rise times, allowing operation up to 3MHz per phase. Larger capacitive loads are allowable but result in longer propagation and transition times. Adaptive dead-time control prevents shoot-through currents and maximizes converter efficiency while allowing operation with a variety of MOSFETs and PWM controllers. An input undervoltage lockout (UVLO) circuit allows proper power-on sequencing.

PWM Input

The drivers for the MAX8791/MAX8791B are disabled—DH and DL pulled low—if the PWM input remains in the midlevel window for at least 300ns (typ). Once the PWM signal is driven high or low, the MAX8791/MAX8791B immediately exit the low-current shutdown state and resume active operation. Outside the shutdown state, the drivers are enabled based on the rising and falling thresholds specified in the *Electrical Characteristics*.

MOSFET Gate Drivers (DH, DL)

The high-side driver (DH) has a 0.9Ω sourcing resistance and 0.7Ω sinking resistance, resulting in 2.2A peak sourcing current and 2.7A peak sinking current with a 5V supply voltage. The low-side driver (DL) has a typical 0.7Ω sourcing resistance and 0.3Ω sinking resistance, yielding 2.7A peak sourcing current and 8A peak sinking current. This reduces switching losses, making the MAX8791/MAX8791B ideal for both high-frequency and high output-current applications.

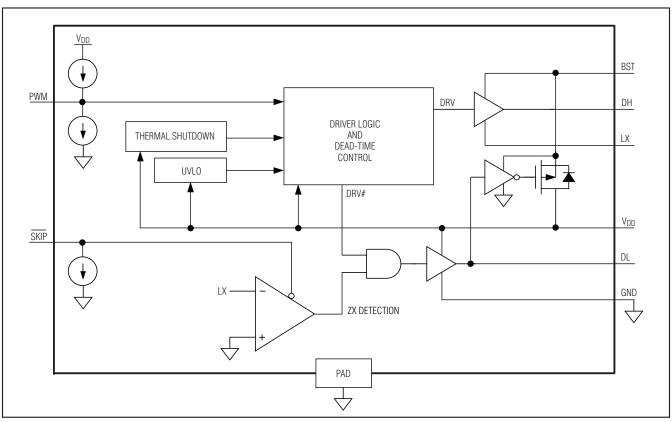


Figure 4. Overview Block Diagram

Adaptive Shoot-Through Protection

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large VIN - VOUT differential exists. Two adaptive dead-time circuits monitor the DH and DL outputs and prevent the opposite-side FET from turning on until the other is fully off. The MAX8791/MAX8791B constantly monitor the low-side driver output (DL) voltage, and only allow the high-side driver to turn on when DL drops below the adaptive threshold. Similarly, the controller monitors the high-side driver output (DH), and prevents the low side from turning on until DH falls below the adaptive threshold before allowing DL to turn on.

The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8791/MAX8791B interprets the

MOSFET gates as off while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

Internal Boost Switch

The MAX8791/MAX8791B use a bootstrap circuit to generate the necessary drive voltage to fully enhance the high-side n-channel MOSFET. The internal p-channel MOSFET creates an ideal diode, providing a low voltage drop between V_{DD} and BST.

The selected high-side MOSFET determines appropriate boost capacitance values (C_{BST} in Figure 1), according to the following equation:

$$C_{BST} = Q_{GATE}/\Delta V_{BST}$$

where QGATE is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver. Choose $\Delta V_{BST}=0.1V$ to 0.2V when determining CBST. The boost flying capacitor should be a low equivalent-series resistance (ESR) ceramic capacitor.

5V Bias Supply (V_{DD})

V_{DD} provides the supply voltage for the internal logic circuits. Bypass V_{DD} with a 1µF or larger ceramic capacitor to GND to limit noise to the internal circuitry. Connect these bypass capacitors as close as possible to the IC.

Input Undervoltage Lockout

When V_{DD} is below the UVLO threshold, DH and DL are held low. Once V_{DD} is above the UVLO threshold and while PWM is low, DL is driven high and DH is driven low. This prevents the output of the converter from rising before a valid PWM signal is applied.

Low-Power Pulse Skipping

The MAX8791/MAX8791B enter into low-power pulseskipping mode when SKIP is pulled low. In skip mode, an inherent automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. A zerocrossing comparator truncates the low-side switch ontime at the inductor current's zero crossing. The comparator senses the voltage across LX and GND. Once V_I x - V_{GND} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peakto-peak ripple current, which is a function of the inductor value. For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The switching waveforms may appear noisy and asynchronous when light loading activates the pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency.

_Applications Information

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention. The high-side MOSFET (NH) must be able to dissipate the resistive losses plus the switching losses at both VIN(MIN) and VIN(MAX). Calculate both these sums. Ideally, the losses at VIN(MIN) should be roughly equal to losses at VIN(MIN), with lower losses in between. If the losses at VIN(MIN) are significantly higher than the losses at VIN(MAX), consider increasing the size of NH (reducing RDS(ON) but increasing CGATE). Conversely, if the losses at VIN(MAX) are significantly higher than the

losses at V_{IN(MIN)}, consider reducing the size of N_H (increasing R_{DS(ON)} but reducing C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance (R_{DS(ON)}), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D2PAK), and is reasonably priced. Ensure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

PD (N_H RESISTIVE) =
$$\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases. Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the RDS(ON) required to stay within package-power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction (RDS(ON)) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics.

The following switching-loss calculation provides only a very rough estimate and is no substitute for prototype evaluation, preferably including verification using a thermocouple mounted on N_{H} :

PD (N_H SWITCHING) =
$$\left(\frac{V_{IN(MAX)}I_{LOAD}f_{SW}}{n_{TOTAL}}\right)\left(\frac{Q_{G(SW)}}{I_{GATE}}\right) + \frac{C_{OSS}V_{IN}^{2}f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, Q_G(sw) is the charge needed to turn on the high-side MOSFET, and I_{GATE} is the peak gate-drive source/sink current (5A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied due to the squared term in the switching-loss equation above. If the high-side MOSFET chosen for adequate $R_{\mbox{\footnotesize{DS(ON)}}}$ at low battery voltages becomes extraordinarily hot when biased from $V_{\mbox{\footnotesize{IN(MAX)}}}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at the maximum input voltage:

PD (NL RESISTIVE) =
$$\left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right] \left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy load conditions that are greater than ILOAD(MAX), but are not quite high enough to exceed the current limit and cause the fault latch to trip. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation. The heat sink can be a large copper field on the PCB or an externally mounted device.

An optional Schottky diode only conducts during the dead time when both the high-side and low-side MOSFETs are off. Choose a Schottky diode with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time, and a peak current rating higher than the peak inductor current. The Schottky diode must be rated to handle the average power dissipation per switching cycle. This diode is optional and can be removed if efficiency is not critical.

IC Power Dissipation and Thermal Considerations

Power dissipation in the IC package comes mainly from driving the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$PD(IC) = I_{BIAS} \times 5V$$

where IBIAS is the bias current of the 5V supply calculated in the 5V Bias Supply (VDD) section. The rise in die temperature due to self-heating is given by the following formula:

$$\Delta T_J = \Theta_{JA} \times PD(IC)$$

where PD(IC) is the power dissipated by the device, and Θ_{JA} is the package's thermal resistance. The typical thermal resistance is 42°C/W for the 3mm x 3mm TQFN package.

Avoiding dV/dt Turning on the Low-Side MOSFET

At high input voltages, fast turn-on of the high-side MOSFET can momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (CRSS) and the input capacitance (CISS) of the low-side MOSFET. Improper selection of the low-side MOSFET that results in a high ratio of CRSS/CISS makes the problem more severe. To avoid this problem, minimize the ratio of CRSS/CISS when selecting the low-side MOSFET. Adding a 1Ω to 4.7Ω resistor between BST and CBST can slow the high-side MOSFET turn-on. Similarly, adding a small capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods work at the expense of increased switching losses.

Layout Guidelines

The MAX8791/MAX8791B MOSFET driver sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PCB layout guidelines are recommended when designing with the MAX8791/MAX8791B:

- 1) Place all decoupling capacitors as close as possible to their respective IC pins.
- Minimize the length of the high-current loop from the input capacitor, the upper switching MOSFET, and the low-side MOSFET back to the input-capacitor negative terminal.
- Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
- 4) Connect GND of the MAX8791/MAX8791B as close as possible to the source of the low-side MOSFETs.

A sample layout is available in the MAX8786 evaluation kit.

_____Chip Information
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TDFN-EP	TQ833+1	<u>21-0136</u>

NIXIN

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/06	Initial release	_
1	11/06	Updated Electrical Characteristics and PWM Input section.	3, 7
2	1/10	Added the MAX8791B to entire data sheet.	1–12

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ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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