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Note: Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp. Customer Support Dept. April 1, 2003



Description

The M16C/62A group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. They also feature a built-in multiplier and DMAC, making them ideal for controlling office, communications, industrial equipment, and other high-speed processing applications.

The M16C/62A group includes a wide range of products with different internal memory types and sizes and various package types.

Features

Memory capacity	ROM (See Figure 1.1.4. ROM Expansion)
	RAM 3K to 20K bytes
• Shortest instruction execution time	62.5ns (f(XIN)=16MHz, VCC=5V)
	100ns (f(XIN)=10MHz, Vcc=3V, with software one-wait): Mask ROM, flash memory 5V version
Supply voltage	4.2V to 5.5V (f(XIN)=16MHz, without software wait) : Mask ROM, flash memory 5V version
	2.7V to 5.5V (f(XIN)=10MHz with software one-wait) : Mask ROM, flash memory 5V version
Low power consumption	25.5mW (f(XIN)=10MHz, with software one-wait, Vcc = 3V)
Interrupts	25 internal and 8 external interrupt sources, 4 software
	interrupt sources; 7 levels (including key input interrupt)
Multifunction 16-bit timer	5 output timers + 6 input timers
• Serial I/O	5 channels (3 for UART or clock synchronous, 2 for clock synchro-
	nous)
• DMAC	2 channels (trigger: 24 sources)
A-D converter	10 bits X 8 channels (Expandable up to 10 channels)
D-A converter	8 bits X 2 channels
CRC calculation circuit	1 circuit
Watchdog timer	1 line
Programmable I/O	87 lines
• Input port	1 line (P85 shared with NMI pin)
Memory expansion	Available (to a maximum of 1M bytes)
Chip select output	4 lines
Clock generating circuit	2 built-in clock generation circuits
	(built-in feedback resistor, and external ceramic or quartz oscillator)

Applications

Audio, cameras, office equipment, communications equipment, portable equipment

-----Table of Contents-----

Central Processing Unit (CPU)11	Timer	77
Reset14	Serial I/O	107
Processor Mode21	A-D Converter	148
Clock Generating Circuit35	D-A Converter	158
Protection44	CRC Calculation Circuit	160
Interrupts45	Programmable I/O Ports	162
Watchdog Timer65	Electrical characteristic	173
DMAC67	Flash memory version	216



Pin Configuration

Figures 1.1.1 and 1.1.2 show the pin configurations (top view).

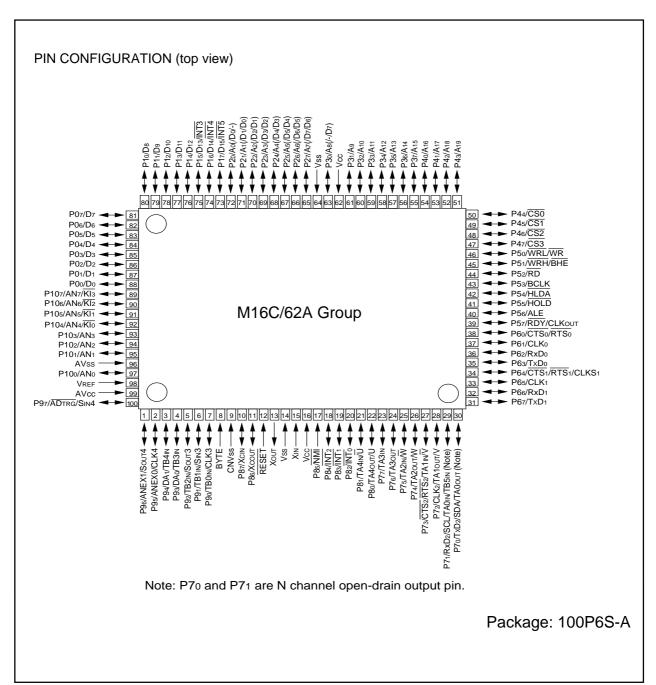


Figure 1.1.1. Pin configuration (top view)

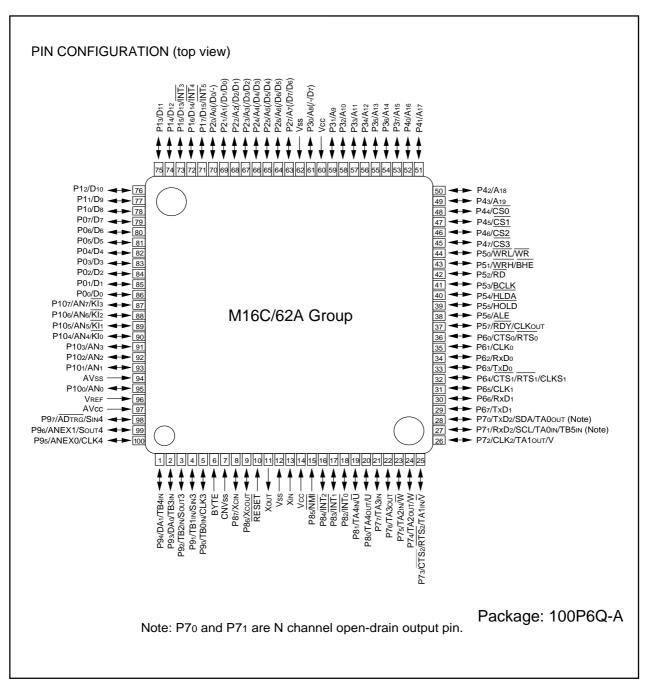


Figure 1.1.2. Pin configuration (top view)

Block Diagram

Figure 1.1.3 is a block diagram of the M16C/62A group.

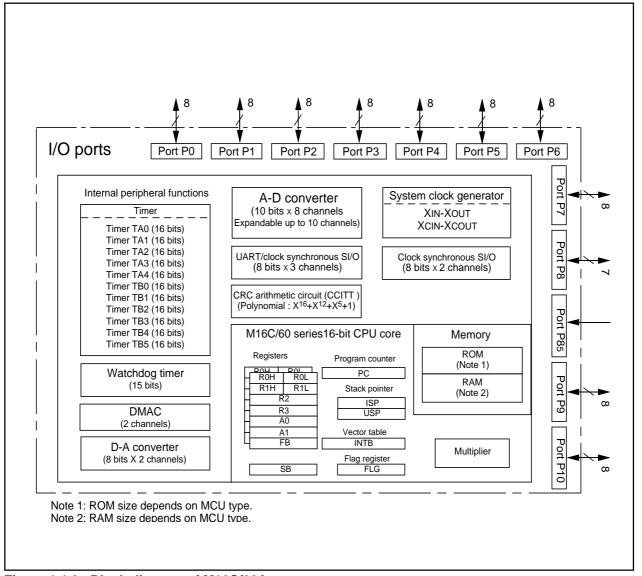


Figure 1.1.3. Block diagram of M16C/62A group

Performance Outline

Table 1.1.1 is a performance outline of M16C/62A group.

Table 1.1.1. Performance outline of M16C/62A group

Item		Performance	
Number of ba	sic instructions	91 instructions	
Shortest instruction execution time		62.5ns(f(XIN)=16MHz, Vcc=5V)	
		100ns (f(XIN)=10MHz, Vcc=3V, with software one-wait)	
		: Mask ROM, flash memory 5V version	
Memory	ROM	(See the figure 1.1.4. ROM Expansion)	
capacity	RAM	3K to 20K bytes	
I/O port	P0 to P10 (except P85)	8 bits x 10, 7 bits x 1	
Input port	P85	1 bit x 1	
Multifunction	TA0, TA1, TA2, TA3, TA4	16 bits x 5	
timer	TB0, TB1, TB2, TB3, TB4, TB5	16 bits x 6	
Serial I/O	UARTO, UART1, UART2	(UART or clock synchronous) x 3	
	SI/O3, SI/O4	(Clock synchronous) x 2	
A-D converter		10 bits x (8 + 2) channels	
D-A converter	•	8 bits x 2	
DMAC		2 channels (trigger: 24 sources)	
CRC calculati	on circuit	CRC-CCITT	
Watchdog tim	er	15 bits x 1 (with prescaler)	
Interrupt		25 internal and 8 external sources, 4 software sources, 7 levels	
Clock generat	ing circuit	2 built-in clock generation circuits	
		(built-in feedback resistor, and external ceramic or quartz oscillator)	
Supply voltage	е	4.2V to 5.5V (f(XIN)=16MHz, without software wait)	
		: Mask ROM, flash memory 5V version	
		2.7V to 5.5V (f(XIN)=10MHz with software one-wait)	
		: Mask ROM, flash memory 5V version	
Power consur	nption	25.5mW (f(XIN) = 10MHz, Vcc=3V with software one-wait)	
I/O	I/O withstand voltage	5V	
characteristics	Output current	5mA	
Memory expa	nsion	Available (to a maximum of 1M bytes)	
Device config	uration	CMOS high performance silicon gate	
Package		100-pin plastic mold QFP	



Mitsubishi plans to release the following products in the M16C/62A group:

- (1) Support for mask ROM version, external ROM version, and flash memory version
- (2) ROM capacity
- (3) Package

100P6S-A : Plastic molded QFP (mask ROM, and flash memory versions) 100P6Q-A : Plastic molded QFP(mask ROM, and flash memory versions)

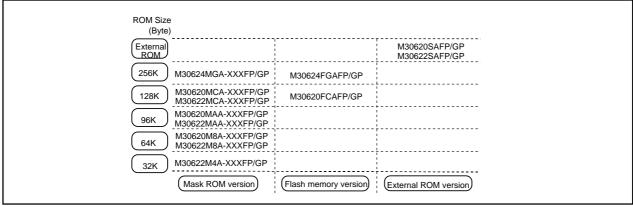


Figure 1.1.4. ROM expansion

The M16C/62A group products currently supported are listed in Table 1.1.2.

Table 1.1.2. M16C/62A group

March. 2001

	_			Water: 2001
Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30622M4A-XXXFP	32K byte	3K byte	100P6S-A	
M30622M4A-XXXGP	021 Oylo	OK Byte	100P6Q-A	
M30620M8A-XXXFP		10K byte	100P6S-A	
M30620M8A-XXXGP	64K byte	Tore byte	100P6Q-A	
M30622M8A-XXXFP	04K byte	4K byto	100P6S-A	
M30622M8A-XXXGP		4K byte	100P6Q-A	
M30620MAA-XXXFP		10K byte	100P6S-A	
M30620MAA-XXXGP	96K byte	Tore byte	100P6Q-A	Mask ROM version
M30622MAA-XXXFP	90K byte	5K byte	100P6S-A	Wask ROW Version
M30622MAA-XXXGP		Ol Caylo	100P6Q-A	
M30620MCA-XXXFP		40161515	100P6S-A	
M30620MCA-XXXGP	128K byte	10K byte	100P6Q-A	
M30622MCA-XXXFP		EIZ b. (a	100P6S-A	
M30622MCA-XXXGP		5K byte	100P6Q-A	
M30624MGA-XXXFP	256K byte	20K byte	100P6S-A	
M30624MGA-XXXGP	230K byte	2010 Byte	100P6Q-A	
M30620FCAFP	129K byto	4016 1- 1-	100P6S-A	
M30620FCAGP	128K byte	10K byte	100P6Q-A	Flash memory
M30624FGAFP	256K byte	20K byte	100P6S-A	5V version
M30624FGAGP	256K byte	20K byte	100P6Q-A	
M30620SAFP		4014 5.45	100P6S-A	
M30620SAGP		10K byte	100P6Q-A	External ROM
M30622SAFP		OK byto	100P6S-A	version
M30622SAGP		3K byte	100P6Q-A	



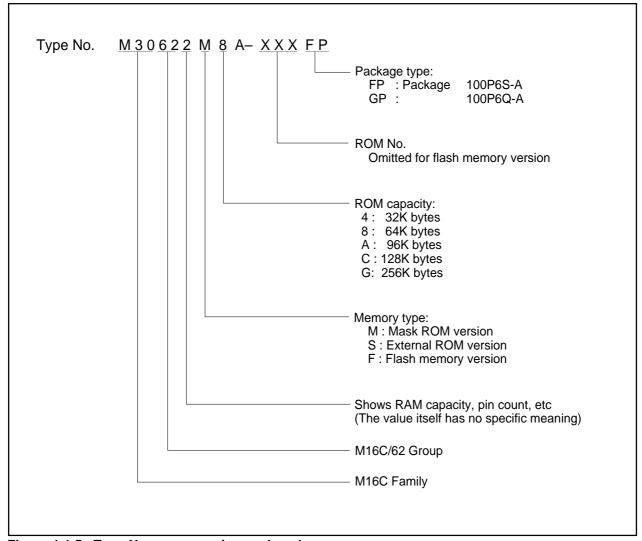


Figure 1.1.5. Type No., memory size, and package

Pin Description

Pin name	Signal name	I/O type	Function		
Vcc, Vss	Power supply input		Supply 2.7V to 5.5 V to the VCC pin. Supply 0 V to the Vss pin.		
CNVss	CNVss	Input	This pin switches between processor modes. Connect this pin to the Vss pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the Vcc pin when starting operation in microprocessor mode.		
RESET	Reset input	Input	A "L" on this input resets the microcomputer.		
XIN	Clock input	Input	These pins are provided for the main clock generating circuit.Connect		
Xout	Clock output	Output	a ceramic resonator or crystal between the XIN and the XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.		
BYTE	External data bus width select input	Input	This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the Vss pin when not using external data bus.		
AVcc	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to Vcc.		
AVss	Analog power supply input		This pin is a power supply input for the A-D converter. Connect this pin to Vss.		
VREF	Reference voltage input	Input	This pin is a reference voltage input for the A-D converter.		
P00 to P07	I/O port P0	Input/output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input in single-chip mode, the port can be set to have or not have a pull-up resistor in units of four bits by software. In memory expansion and microprocessor modes, selection of the internal pull-resistor is not available.		
Do to D7		Input/output	When set as a separate bus, these pins input and output data (Do-D7)		
P10 to P17	I/O port P1	Input/output	This is an 8-bit I/O port equivalent to P0. P15 to P17 also function as external interrupt pins as selected by software.		
D8 to D15		Input/output	When set as a separate bus, these pins input and output data (D8-D15)		
P20 to P27	I/O port P2	Input/output	This is an 8-bit I/O port equivalent to P0.		
Ao to A7		Output	These pins output 8 low-order address bits (A ₀ –A ₇).		
A0/D0 to A7/D7		Input/output	If the external bus is set as an 8-bit wide multiplexed bus, these pins input and output data (D0–D7) and output 8 low-order address bits (A0–A7) separated in time by multiplexing.		
A0 A1/D0 to A7/D6		Output Input/output	If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D0–D6) and output address (A1–A7) separated in time by multiplexing. They also output address (A0).		
P30 to P37	I/O port P3	Input/output	This is an 8-bit I/O port equivalent to P0.		
A8 to A15		Output	These pins output 8 middle-order address bits (A8–A15).		
A8/D7, A9 to A15		Input/output Output	If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D7) and output address (A8) separated in time by multiplexing. They also output address (A9–A15).		
P40 to P47	I/O port P4	Input/output	This is an 8-bit I/O port equivalent to P0.		
A16 to A19, CS0 to CS3		Output Output	These pins output A16–A19 and CS0–CS3 signals. A16–A19 are 4 high order address bits. CS0–CS3 are chip select signals used to specify at access space.		



Pin Description

Pin name	Signal name	I/O type	Function
P50 to P57	I/O port P5	Input/output	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P57 in this port outputs a divide-by-8 or divide-by-32 clock of XIN or a clock of the same frequency as XCIN as selected by software.
WRL/WR, WRH/BHE, RD, BCLK, HLDA, HOLD,		Output Output Output Output Output Input Output	Output WRL, WRH (WR and BHE), RD, BCLK, HLDA, and ALE signals. WRL and WRH, and BHE and WR can be switched using software control. WRL, WRH, and RD selected With a 16-bit external data bus, data is written to even addresses when the WRL signal is "L" and to the odd addresses when the WRH signal is "L". Data is read when RD is "L". WR, BHE, and RD selected Data is written when WR is "L". Data is read when RD is "L". Odd addresses are accessed when BHE is "L". Use this mode when using an 8-bit external data bus. While the input level at the HOLD pin is "L", the microcomputer is placed in the hold state. While in the hold state, HLDA outputs a "L" level. ALE is used to latch the address. While the input level of the RDY pin is "L", the microcomputer is in the ready state.
P60 to P67	I/O port P6	Input/output	This is an 8-bit I/O port equivalent to P0. When used for input in single-chip, memory expansion, and microprocessor modes, the port can be set to have or not have a pull-up resistor in units of four bits by software. Pins in this port also function as UART0 and UART1 I/O pins as selected by software.
P70 to P77	I/O port P7	Input/output	This is an 8-bit I/O port equivalent to P6 (P70 and P71 are N channel open-drain output). Pins in this port also function as timer A0–A3, timer B5 or UART2 I/O pins as selected by software.
P80 to P84, P86, P87, P85	I/O port P8	Input/output Input/output Input/output Input	P80 to P84, P86, and P87 are I/O ports with the same functions as P6. Using software, they can be made to function as the I/O pins for timer A4 and the input pins for external interrupts. P86 and P87 can be set using software to function as the I/O pins for a sub clock generation circuit. In this case, connect a quartz oscillator between P86 (XCOUT pin) and P87 (XCIN pin). P85 is an input-only port that also functions for NMI. The NMI interrupt is generated when the input at this pin changes from "H" to "L". The NMI function cannot be cancelled using software. The pull-up cannot be set for this pin.
P90 to P97	I/O port P9	Input/output	This is an 8-bit I/O port equivalent to P6. Pins in this port also function as SI/O3, 4 I/O pins, Timer B0–B4 input pins, D-A converter output pins, A-D converter extended input pins, or A-D trigger input pins as selected by software.
P100 to P107	I/O port P10	Input/output	This is an 8-bit I/O port equivalent to P6. Pins in this port also function as A-D converter input pins as selected by software. Furthermore, P104 –P107 also function as input pins for the key input interrupt function.



Operation of Functional Blocks

The M16C/62A group accommodates certain units in a single chip. These units include ROM and RAM to store instructions and data and the central processing unit (CPU) to execute arithmetic/logic operations. Also included are peripheral units such as timers, serial I/O, D-A converter, DMAC, CRC calculation circuit, A-D converter, and I/O ports.

The following explains each unit.

Memory

Figure 1.3.1 is a memory map of the M16C/62A group. The address space extends the 1M bytes from address 0000016 to FFFF16. From FFFF16 down is ROM. For example, in the M30622MCA-XXXFP, there is 128K bytes of internal ROM from E000016 to FFFF16. The vector table for fixed interrupts such as the reset and $\overline{\text{NMI}}$ are mapped to FFFDC16 to FFFFF16. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 0040016 up is RAM. For example, in the M30622MCA-XXXFP, 5K bytes of internal RAM is mapped to the space from 0040016 to 017FF16. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 0000016 to 003FF16. This area accommodates the control registers for peripheral devices such as I/O ports, A-D converter, serial I/O, and timers, etc. Figures 1.6.1 to 1.6.3 are location of peripheral unit control registers. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to FFE0016 to FFFDB16. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.

In memory expansion mode and microprocessor mode, a part of the spaces are reserved and cannot be used. For example, in the M30622MCA-XXXFP, the following spaces cannot be used.

- The space between 0180016 and 03FFF16 (Memory expansion and microprocessor modes)
- The space between D000016 and DFFFF16 (Memory expansion mode)

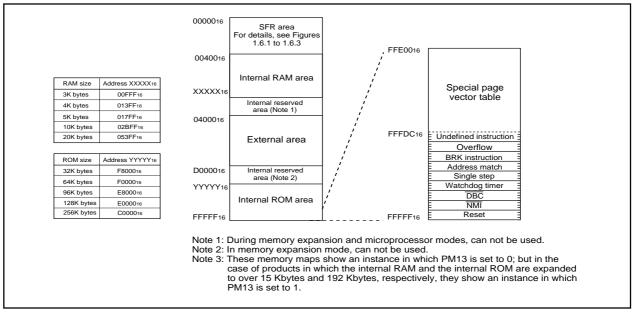


Figure 1.3.1. Memory map



Central Processing Unit (CPU)

The CPU has a total of 13 registers shown in Figure 1.4.1. Seven of these registers (R0, R1, R2, R3, A0, A1, and FB) come in two sets; therefore, these have two register banks.

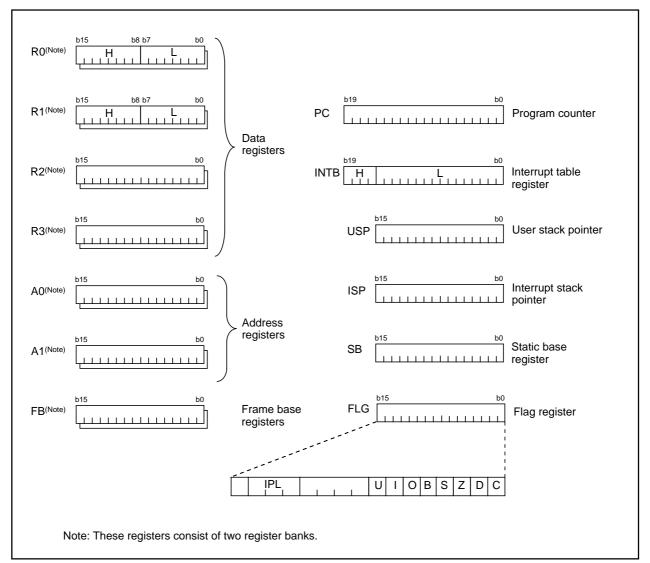


Figure 1.4.1. Central processing unit register

(1) Data registers (R0, R0H, R0L, R1, R1H, R1L, R2, and R3)

Data registers (R0, R1, R2, and R3) are configured with 16 bits, and are used primarily for transfer and arithmetic/logic operations.

Registers R0 and R1 each can be used as separate 8-bit data registers, high-order bits as (R0H/R1H), and low-order bits as (R0L/R1L). In some instructions, registers R2 and R0, as well as R3 and R1 can use as 32-bit data registers (R2R0/R3R1).

(2) Address registers (A0 and A1)

Address registers (A0 and A1) are configured with 16 bits, and have functions equivalent to those of data registers. These registers can also be used for address register indirect addressing and address register relative addressing.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).



(3) Frame base register (FB)

Frame base register (FB) is configured with 16 bits, and is used for FB relative addressing.

(4) Program counter (PC)

Program counter (PC) is configured with 20 bits, indicating the address of an instruction to be executed.

(5) Interrupt table register (INTB)

Interrupt table register (INTB) is configured with 20 bits, indicating the start address of an interrupt vector table.

(6) Stack pointer (USP/ISP)

Stack pointer comes in two types: user stack pointer (USP) and interrupt stack pointer (ISP), each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by a stack pointer select flag (U flag). This flag is located at the position of bit 7 in the flag register (FLG).

(7) Static base register (SB)

Static base register (SB) is configured with 16 bits, and is used for SB relative addressing.

(8) Flag register (FLG)

Flag register (FLG) is configured with 11 bits, each bit is used as a flag. Figure 1.4.2 shows the flag register (FLG). The following explains the function of each flag:

• Bit 0: Carry flag (C flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

• Bit 1: Debug flag (D flag)

This flag enables a single-step interrupt.

When this flag is "1", a single-step interrupt is generated after instruction execution. This flag is cleared to "0" when the interrupt is acknowledged.

• Bit 2: Zero flag (Z flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, cleared to "0".

• Bit 3: Sign flag (S flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, cleared to "0".

Bit 4: Register bank select flag (B flag)

This flag chooses a register bank. Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

• Bit 5: Overflow flag (O flag)

This flag is set to "1" when an arithmetic operation resulted in overflow; otherwise, cleared to "0".

• Bit 6: Interrupt enable flag (I flag)

This flag enables a maskable interrupt.

An interrupt is disabled when this flag is "0", and is enabled when this flag is "1". This flag is cleared to "0" when the interrupt is acknowledged.



• Bit 7: Stack pointer select flag (U flag)

Interrupt stack pointer (ISP) is selected when this flag is "0"; user stack pointer (USP) is selected when this flag is "1".

This flag is cleared to "0" when a hardware interrupt is acknowledged or an INT instruction of software interrupt Nos. 0 to 31 is executed.

• Bits 8 to 11: Reserved area

• Bits 12 to 14: Processor interrupt priority level (IPL)

Processor interrupt priority level (IPL) is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than the processor interrupt priority level (IPL), the interrupt is enabled.

• Bit 15: Reserved area

The C, Z, S, and O flags are changed when instructions are executed. See the software manual for details.

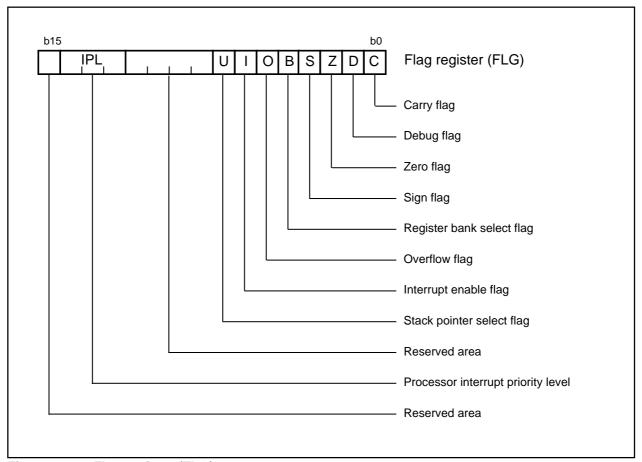


Figure 1.4.2. Flag register (FLG)

Reset

There are two kinds of resets; hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for details of software resets.) This section explains on hardware resets.

When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2Vcc max.) for at least 20 cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.

Figure 1.5.1 shows the example reset circuit. Figure 1.5.2 shows the reset sequence.

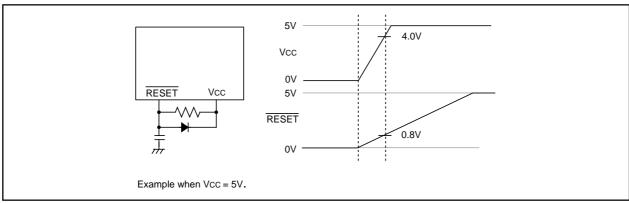


Figure 1.5.1. Example reset circuit

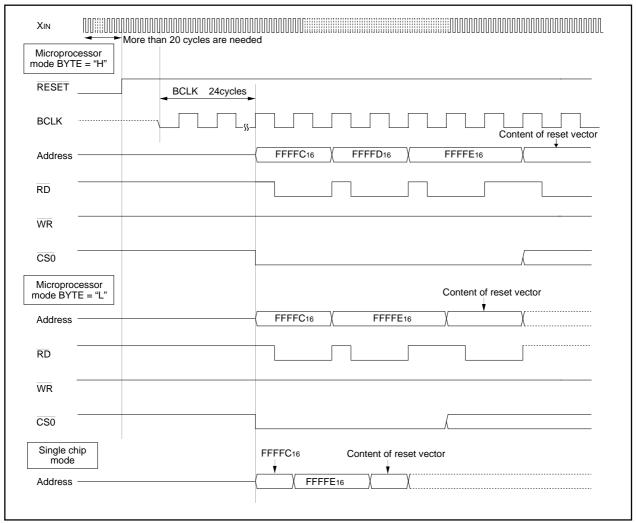


Figure 1.5.2. Reset sequence



Table 1.5.1 shows the statuses of the other pins while the $\overline{\text{RESET}}$ pin level is "L". Figures 1.5.3 and 1.5.4 show the internal status of the microcomputer immediately after the reset is cancelled.

Table 1.5.1. Pin status when RESET pin level is "L"

	Status				
Pin name	CNIVes Ves	CNVss = Vcc			
	CNVss = Vss	BYTE = Vss	BYTE = Vcc		
P0	Input port (floating)	Data input (floating)	Data input (floating)		
P1	Input port (floating)	Data input (floating)	Input port (floating)		
P2, P3, P40 to P43	Input port (floating)	Address output (undefined)	Address output (undefined)		
P44	Input port (floating)	CS0 output ("H" level is output)	CS0 output ("H" level is output)		
P45 to P47	Input port (floating)	Input port (floating) (pull-up resistor is on)	Input port (floating) (pull-up resistor is on)		
P50	Input port (floating)	WR output ("H" level is output)	WR output ("H" level is output)		
P51	Input port (floating)	BHE output (undefined)	BHE output (undefined)		
P52	Input port (floating)	RD output ("H" level is output)	RD output ("H" level is output)		
P53	Input port (floating)	BCLK output	BCLK output		
P54	Input port (floating)	HLDA output (The output value depends on the input to the HOLD pin)	HLDA output (The output value depends on the input to the HOLD pin)		
P55	Input port (floating)	HOLD input (floating)	HOLD input (floating)		
P56	Input port (floating)	ALE output ("L" level is output)	ALE output ("L" level is output)		
P57	Input port (floating)	RDY input (floating)	RDY input (floating)		
P6, P7, P80 to P84, P86, P87, P9, P10	Input port (floating)	Input port (floating)	Input port (floating)		



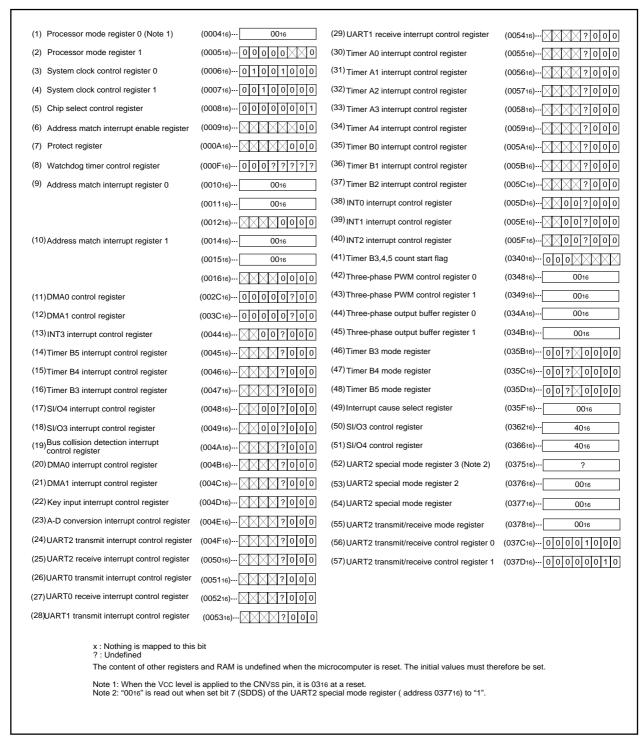


Figure 1.5.3. Device's internal status after a reset is cleared

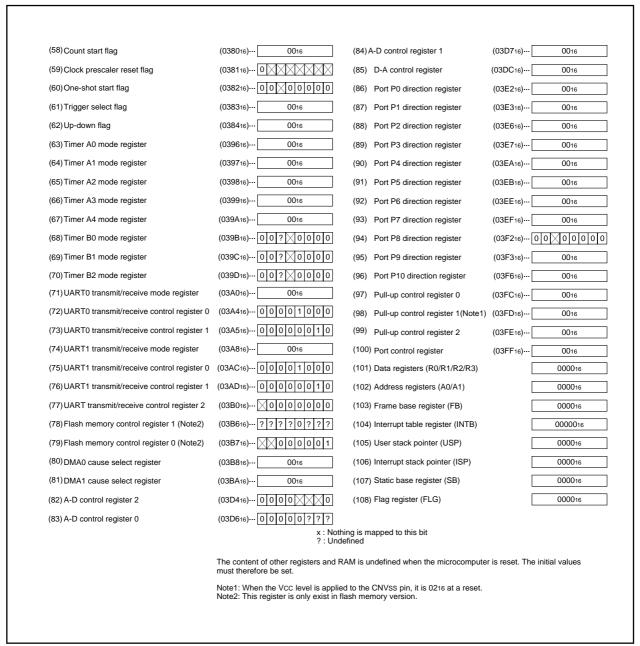


Figure 1.5.4. Device's internal status after a reset is cleared

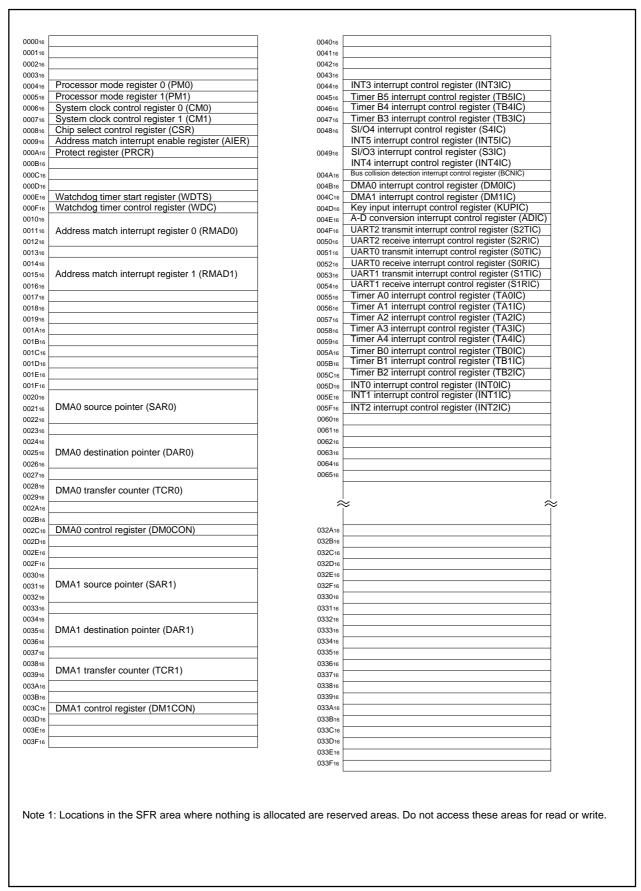


Figure 1.6.1. Location of peripheral unit control registers (1)



4016	Timer B3, 4, 5 count start flag (TBSR)	038016	Count start flag (TABSR)
4116		038116	Clock prescaler reset flag (CPSRF)
4216	Times AA A resistan (TAAA)	038216	One-shot start flag (ONSF)
4316	Timer A1-1 register (TA11)	038316	Trigger select register (TRGSR)
4416	Time and A. A. maniatan (TACA)	038416	Up-down flag (UDF)
4516	Timer A2-1 register (TA21)	038516	
4616		038616	
4716	Timer A4-1 register (TA41)	038716	Timer A0 (TA0)
4816	Three-phase PWM control register 0(INVC0)	038816	
- +	Three-phase PWM control register 0(INVC0)	038916	Timer A1 (TA1)
4916			
4A16	Three-phase output buffer register 0(IDB0)	038A ₁₆	Timer A2 (TA2)
4B16	Three-phase output buffer register 1(IDB1)	038B ₁₆	<u> </u>
4C16	Dead time timer(DTT)	038C ₁₆	Timer A3 (TA3)
4D16	Timer B2 interrupt occurrence frequency set counter(ICTB2)	038D16	
4E16		038E ₁₆	Timer A4 (TA4)
4F16		038F16	TIIICI AT (TAT)
5016	Time and DO are minted (TDO)	039016	Timor PO (TPO)
5116	Timer B3 register (TB3)	039116	Timer B0 (TB0)
5216		039216	Times D4 (TD4)
5316	Timer B4 register (TB4)	039316	Timer B1 (TB1)
5416		039416	
5516	Timer B5 register (TB5)	039516	Timer B2 (TB2)
		039616	Timer A0 mode register (TA0MR)
5616		039616	
5716			Timer A1 mode register (TA1MR)
5816		039816	Timer A2 mode register (TA2MR)
5916		039916	Timer A3 mode register (TA3MR)
5A16		039A ₁₆	Timer A4 mode register (TA4MR)
5B16	Timer B3 mode register (TB3MR)	039B ₁₆	Timer B0 mode register (TB0MR)
5C16	Timer B4 mode register (TB4MR)	039C ₁₆	Timer B1 mode register (TB1MR)
5D16	Timer B5 mode register (TB5MR)	039D16	Timer B2 mode register (TB2MR)
5E16	······································	039E ₁₆	<u> </u>
5F16	Interrupt cause select register (IFSR)	039F ₁₆	
6016	SI/O3 transmit/receive register (S3TRR)	03A016	UART0 transmit/receive mode register (U0MR)
- F	Circo transmitreceive register (GOTTATA)	03A1 ₁₆	UARTO bit rate generator (U0BRG)
6116	SI/O3 control register (S3C)	03A216	Critero bil rato generator (COBICO)
6216		03A316	UART0 transmit buffer register (U0TB)
6316	SI/O3 bit rate generator (S3BRG)		LIADTO transport/passing approximation of (LIACO)
6416	SI/O4 transmit/receive register (S4TRR)	03A416	UART0 transmit/receive control register 0 (U0C0)
6516		03A516	UART0 transmit/receive control register 1 (U0C1)
6616	SI/O4 control register (S4C)	03A616	UART0 receive buffer register (U0RB)
6716	SI/O4 bit rate generator (S4BRG)	03A7 ₁₆	<u> </u>
6816		03A8 ₁₆	UART1 transmit/receive mode register (U1MR)
6916		03A9 ₁₆	UART1 bit rate generator (U1BRG)
6A16		03AA16	HADTA (
6B ₁₆		03AB ₁₆	UART1 transmit buffer register (U1TB)
6C ₁₆		03AC16	UART1 transmit/receive control register 0 (U1C0)
6D16		03AD16	UART1 transmit/receive control register 1 (U1C1)
- 1		03AE16	
6E16		03AF16	UART1 receive buffer register (U1RB)
6F16			LIART transmit/receive control register 2 (LICON)
7016		03B016	UART transmit/receive control register 2 (UCON)
7116		03B1 ₁₆	
7216		03B216	
7316		03B316	
7416		03B416	
7516	UART2 special mode register 3(U2SMR3)	03B516	
7616	UART2 special mode register 2(U2SMR2)	03B616	Flash memory control register 1 (FMR1) (Note1
7716	UART2 special mode register (U2SMR)	03B7 ₁₆	Flash memory control register 0 (FMR0) (Note1
7816	UART2 transmit/receive mode register (U2MR)	03B816	DMA0 request cause select register (DM0SL)
7916	UART2 bit rate generator (U2BRG)	03B916	, , , , , , , , , , , , , , , , , , , ,
T T	571112 bit rate generator (OZDITO)	03BA ₁₆	DMA1 request cause select register (DM1SL)
7A16	UART2 transmit buffer register (U2TB)	03BB16	2 (1 Toquoti Saudo Solloti Tegister (DIVITOL)
7B16	<u> </u>		
7C16	UART2 transmit/receive control register 0 (U2C0)	03BC16	CRC data register (CRCD)
7D16	UART2 transmit/receive control register 1 (U2C1)	03BD16	
7E16	UART2 receive buffer register (U2RB)	03BE16	CRC input register (CRCIN)
7F16	22.1000.10 2801 Toglotor (02110)	03BF16	
_			
ote 1	1: This register is only exist in flash memory ver	sion.	
			served areas. Do not access these areas for

Figure 1.6.2. Location of peripheral unit control registers (2)

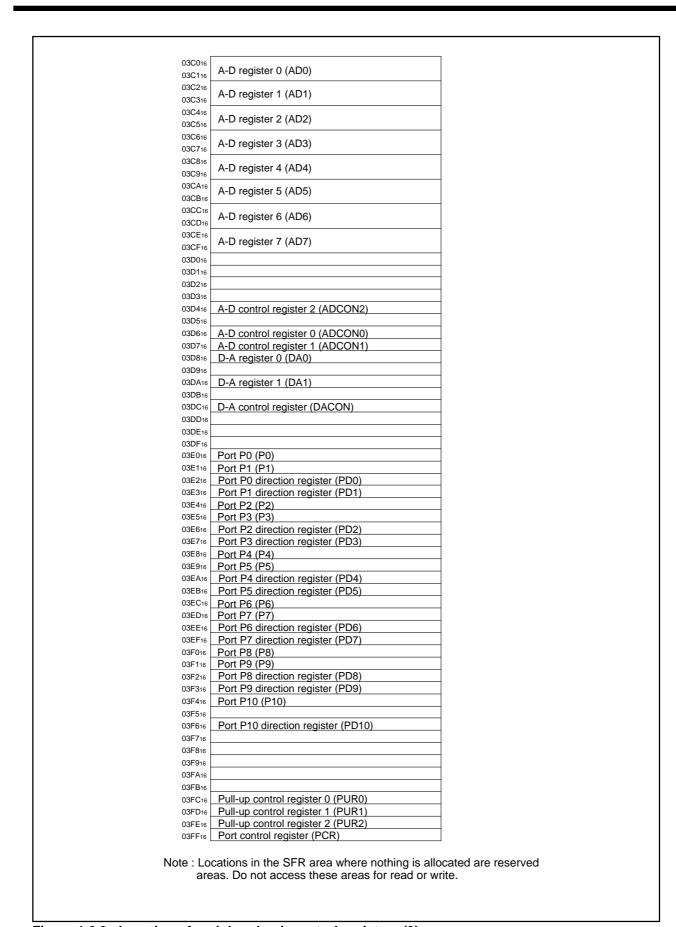


Figure 1.6.3. Location of peripheral unit control registers (3)



Software Reset

Writing "1" to bit 3 of the processor mode register 0 (address 000416) applies a (software) reset to the microcomputer. A software reset has the same effect as a hardware reset. The contents of internal RAM are preserved.

Processor Mode

(1) Types of Processor Mode

One of three processor modes can be selected: single-chip mode, memory expansion mode, and microprocessor mode. The functions of some pins, the memory map, and the access space differ according to the selected processor mode.

Single-chip mode

In single-chip mode, only internal memory space (SFR, internal RAM, and internal ROM) can be accessed. However, after the reset has been released and the operation of shifting from the microprocessor mode has started ("H" applied to the CNVss pin), the internal ROM area cannot be accessed even if the CPU shifts to the single-chip mode.

Ports P0 to P10 can be used as programmable I/O ports or as I/O ports for the internal peripheral functions.

Memory expansion mode

In memory expansion mode, external memory can be accessed in addition to the internal memory space (SFR, internal RAM, and internal ROM). However, after the reset has been released and the operation of shifting from the microprocessor mode has started ("H" applied to the CNVss pin), the internal ROM area cannot be accessed even if the CPU shifts to the memory expansion mode.

In this mode, some of the pins function as the address bus, the data bus, and as control signals. The number of pins assigned to these functions depends on the bus and register settings. (See "Bus Settings" for details.)

Microprocessor mode

In microprocessor mode, the SFR, internal RAM, and external memory space can be accessed. The internal ROM area cannot be accessed.

In this mode, some of the pins function as the address bus, the data bus, and as control signals. The number of pins assigned to these functions depends on the bus width and register settings. (See "Bus Settings" for details.)

(2) Setting Processor Modes

The processor mode is set using the CNVss pin and the processor mode bits (bits 1 and 0 at address 000416). Do not set the processor mode bits to "102".

Regardless of the level of the CNVss pin, changing the processor mode bits selects the mode. Therefore, never change the processor mode bits when changing the contents of other bits. Do not change the processor mode bits simultaneously with other bits when changing the processor mode bits "012" or "112". Change the processor mode bits after changing the other bits. Also do not attempt to shift to or from the microprocessor mode within the program stored in the internal ROM area.

Applying Vss to CNVss pin

The microcomputer begins operation in single-chip mode after being reset. Memory expansion mode is selected by writing "012" to the processor mode bits.

Applying Vcc to CNVss pin

The microcomputer starts to operate in microprocessor mode after being reset.



Figure 1.7.1 shows the processor mode register 0 and 1.

Figure 1.7.2 shows the memory maps applicable for each of the modes.

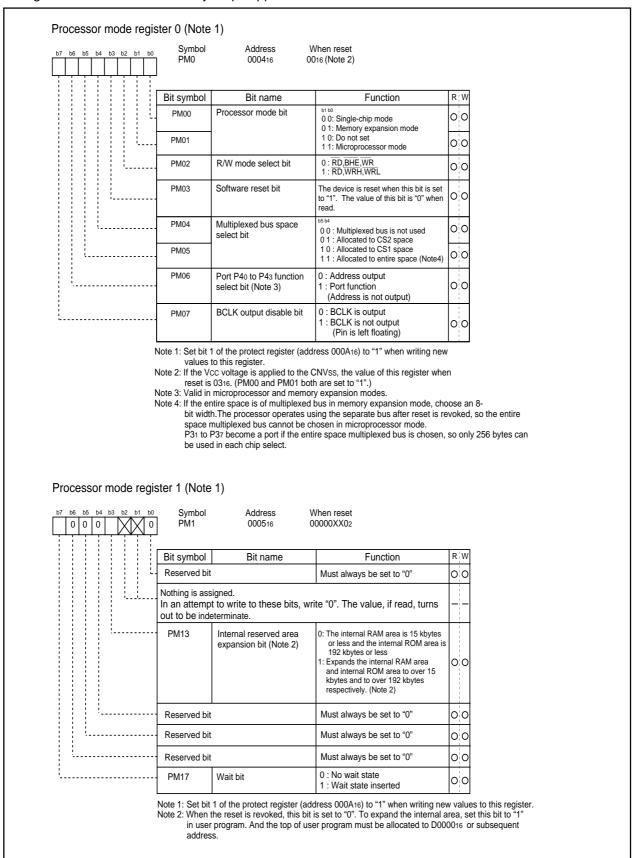


Figure 1.7.1. Processor mode register 0 and 1



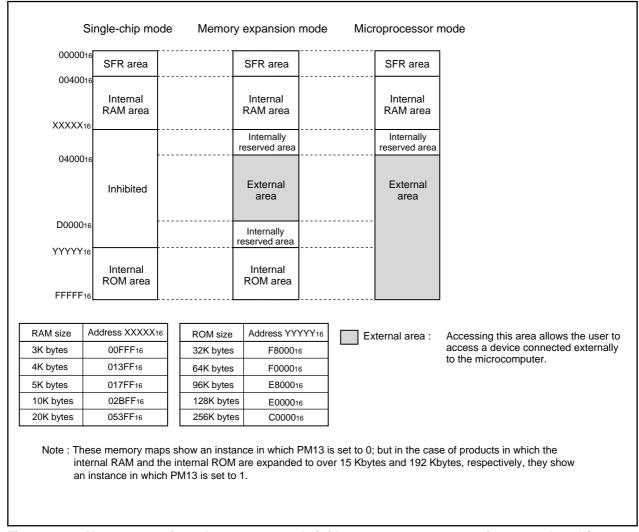


Figure 1.7.2. Memory maps in each processor mode (without memory area expansion, normal mode)

Internal Reserved Area Expansion Bit (PM13)

This bit expands the internal RAM area and the internal ROM area, and changes the chip select area. In M30624MGA/FGA, for example, to set this bit to "1" expands the internal RAM area and the internal ROM area to 20 Kbytes and 256 Kbytes respectively. Refer to Figure 1.7.3 for the chip select area. When the reset is revoked, this bit is set to "0". To expand the internal area, set this bit to "1" in user program. And the top of user program must be allocated to D000016 or subsequent address.

In the case of the product in which the internal ROM is 192 Kbytes or less and the internal RAM is 15 Kbytes or less, set this bit to "0" when this product is used in the memory expansion mode or the microprocessor mode. When the product is used in the single chip mode, the internal area is not expanded and any action is not affected, even if this bit is set to "1".

Figure 1.7.3 shows the memory maps and the chip selection areas effected by PM13 (the internal reserved area expansion bit) in each processor mode for the product having an internal RAM of more than 15K bytes and a ROM of more than 192K bytes.

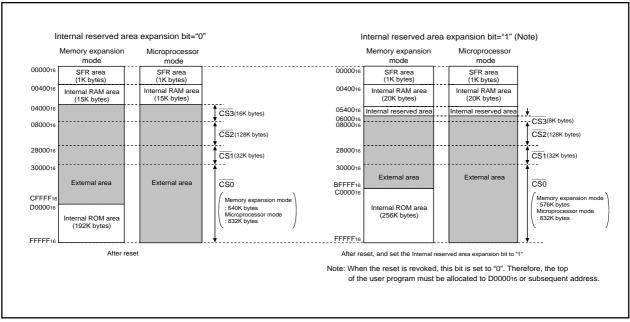


Figure 1.7.3. Memory location and chip select area in each processor mode

Bus Settings

The BYTE pin and bits 4 to 6 of the processor mode register 0 (address 000416) are used to change the bus settings. Table 1.8.1 shows the factors used to change the bus settings.

Table 1.8.1. Factors for switching bus settings

Bus setting	Switching factor
Switching external address bus width	Bit 6 of processor mode register 0
Switching external data bus width	BYTE pin
Switching between separate and multiplex bus	Bits 4 and 5 of processor mode register 0

(1) Selecting external address bus width

The address bus width for external output in the 1M bytes of address space can be set to 16 bits (64K bytes address space) or 20 bits (1M bytes address space). When bit 6 of the processor mode register 0 is set to "1", the external address bus width is set to 16 bits, and P2 and P3 become part of the address bus. P40 to P43 can be used as programmable I/O ports. When bit 6 of processor mode register 0 is set to "0", the external address bus width is set to 20 bits, and P2, P3, and P40 to P43 become part of the address bus.

(2) Selecting external data bus width

The external data bus width can be set to 8 or 16 bits. (Note, however, that only the separate bus can be set.) When the BYTE pin is "L", the bus width is set to 16 bits; when "H", it is set to 8 bits. (The internal bus width is permanently set to 16 bits.) While operating, fix the BYTE pin either to "H" or to "L".

(3) Selecting separate/multiplex bus

The bus format can be set to multiplex or separate bus using bits 4 and 5 of the processor mode register 0.

Separate bus

In this mode, the data and address are input and output separately. The data bus can be set using the BYTE pin to be 8 or 16 bits. When the BYTE pin is "H", the data bus is set to 8 bits and P0 functions as the data bus and P1 as a programmable I/O port. When the BYTE pin is "L", the data bus is set to 16 bits and P0 and P1 are both used for the data bus.

When the separate bus is used for access, a software wait can be selected.

Multiplex bus

In this mode, data and address I/O are time multiplexed. With the BYTE pin = "H", the 8 bits from D0 to D7 are multiplexed with A0 to A7.

With the BYTE pin = "L", the 8 bits from Do to D7 are multiplexed with A1 to A8. D8 to D15 are not multiplexed. In this case, the external devices connected to the multiplexed bus are mapped to the microcomputer's even addresses (every 2nd address). To access these external devices, access the even addresses as bytes.

The ALE signal latches the address. It is output from P56.

Before using the multiplex bus for access, be sure to insert a software wait.

If the entire space is of multiplexed bus in memory expansion mode, choose an 8-bit width.

The processor operates using the separate bus after reset is revoked, so the entire space multiplexed bus cannot be chosen in microprocessor mode.

P31 to P37 become a port if the entire space multiplexed bus is chosen, so only 256 bytes can be used in each chip select.



Table 1.8.2. Pin functions for each processor mode

Processor mode	Single-chip mode	Memory expansion mode/microprocessor modes				Memory expansion mode
Multiplexed bus space select bit		"01", "10" Either CS1 or CS2 is for multiplexed bus and others are for separate bus		"00" (separate bus)		"11" (Note 1) multiplexed bus for the entire space
Data bus width BYTE pin level		8 bits "H"	16 bits "L"	8 bits "H"	16 bits "L"	8 bit "H"
P00 to P07	I/O port	Data bus	Data bus	Data bus	Data bus	I/O port
P10 to P17	I/O port	I/O port	Data bus	I/O port	Data bus	I/O port
P20	I/O port	Address bus /data bus(Note 2)	Address bus	Address bus	Address bus	Address bus /data bus
P21 to P27	I/O port	Address bus /data bus(Note 2)	Address bus /data bus(Note 2)	Address bus	Address bus	Address bus /data bus
P30	I/O port	Address bus	Address bus /data bus(Note 2)	Address bus	Address bus	A8/D7
P31 to P37	I/O port	Address bus	Address bus	Address bus	Address bus	I/O port
P40 to P43 Port P40 to P43 function select bit = 1	I/O port	I/O port	I/O port	I/O port	I/O port	I/O port
P40 to P43 Port P40 to P43 function select bit = 0	I/O port	Address bus	Address bus	Address bus	Address bus	I/O port
P44 to P47	I/O port) or programmat tails, refer to "Bu			
P50 to P53	I/O port	Outputs RD, WRL, WRH, and BCLK or RD, BHE, WR, and BCLK (For details, refer to "Bus control")				
P54	I/O port	HLDA	HLDA	HLDA	HLDA	HLDA
P55	I/O port	HOLD	HOLD	HOLD	HOLD	HOLD
P56	I/O port	ALE	ALE	ALE	ALE	ALE
P57	I/O port	RDY	RDY	RDY	RDY	RDY

Note 1: If the entire space is of multiplexed bus in memory expansion mode, choose an 8-bit width.

The processor operates using the separate bus after reset is revoked, so the entire space multiplexed bus cannot be chosen in microprocessor mode.

P31 to P37 become a port if the entire space multiplexed bus is chosen, so only 256 bytes can be used in each chip select.

Note 2: Address bus when in separate bus mode.



Bus Control

The following explains the signals required for accessing external devices and software waits. The signals required for accessing the external devices are valid when the processor mode is set to memory expansion mode and microprocessor mode. The software waits are valid in all processor modes.

(1) Address bus/data bus

The address bus consists of the 20 pins A₀ to A₁₉ for accessing the 1M bytes of address space.

The data bus consists of the pins for data I/O. When the BYTE pin is "H", the 8 ports D₀ to D₇ function as the data bus. When BYTE is "L", the 16 ports D₀ to D₁₅ function as the data bus.

When a change is made from single-chip mode to memory expansion mode, the value of the address bus is undefined until external memory is accessed.

(2) Chip select signal

The chip select signal is output using the same pins as P44 to P47. Bits 0 to 3 of the chip select control register (address 000816) set each pin to function as a port or to output the chip select signal. The chip select control register is valid in memory expansion mode and microprocessor mode. In single-chip mode, P44 to P47 function as programmable I/O ports regardless of the value in the chip select control register.

In microprocessor mode, only $\overline{\text{CS0}}$ outputs the chip select signal after the reset state has been cancelled. $\overline{\text{CS1}}$ to $\overline{\text{CS3}}$ function as input ports. Figure 1.9.1 shows the chip select control register.

The chip select signal can be used to split the external area into as many as four blocks. Tables 1.9.1 and 1.9.2 show the external memory areas specified using the chip select signal.

Table 1.9.1. External areas specified by the chip select signals

(A product having an internal RAM equal to or less than 15K bytes and a ROM equal to or less than 192K bytes)(Note)

Processor mode	Chip select signal				
1 Toccssor mode	CS0	CS1	CS2	CS3	
Memory expansion mode	3000016 to CFFFF16 (640K bytes)	2800016 to	0800016 to	0400016 to	
Microprocessor mode	3000016 to FFFFF16 (832K bytes)	2FFFF16 (32K bytes)	27FFF ₁₆ (128K bytes)	07FFF ₁₆ (16K bytes)	

Note: Be sure to set bit 3 (PM13) of processor mode register 1 to "0".



Table 1.9.2. External areas specified by the chip select signals
(A product having an internal RAM of more than 15K bytes and a ROM of more than 192K bytes)

Processor mode	Chip select signal				
	CS0	CS1	CS2	CS3	
Memory expansion mode	When PM13=0 3000016 to CFFFF16 (640K bytes) When PM13=1 3000016 to BFFFF16 (576K bytes)	2800016 to 2FFFF16 (32K bytes)	0800016 to 27FFF16 (128K bytes)	When PM13=0 0400016 to 07FFF16 (16K bytes) When PM13=1	
Microprocessor mode	0300016 to FFFFF16 (816K bytes)			0600016 to 07FFF16 (8K bytes)	

b7 b6 b5 b4 b3 b2 b1 b0	Symbol CSR	Address 000816	When reset 0116	
	Bit symbol	Bit name	Function	RW
	CS0	CS0 output enable bit	0 : Chip select output disabled (Normal port pin)	00
1	CS1	CS1 output enable bit		00
	CS2	CS2 output enable bit	1 : Chip select output enabled	00
	CS3	CS3 output enable bit		0:0
	CS0W	CS0 wait bit	0 : Wait state inserted	0:0
	CS1W	CS1 wait bit	1 : No wait state	0:0
	CS2W	CS2 wait bit		00
·	CS3W	CS3 wait bit		0.0

Figure 1.9.1. Chip select control register

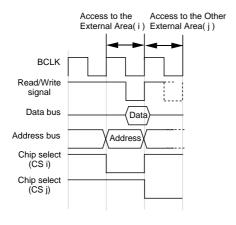
The timing of the chip select signal changing to "L"(active) is synchronized with the address bus. But the timing of the chip select signal changing to "H" depends on the area which will be accessed in the next cycle. Figure 1.9.2 shows the output example of the address bus and chip select signal.

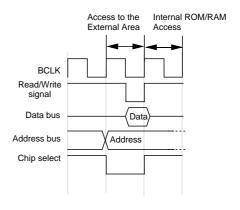
Example 1) After access the external area, both the address signal and the chip select signal change concurrently in the next cycle.

Example 2) After access the external area, only the chip select signal changes in the next cycle (the address bus does not change).

In this example, after access to the external area(i), an access to the area indicated by the other chip select signal(j) will occur in the next cycle. In this case, both the address bus and the chip select signal change between the two cycles.

In this example, an access to the internal ROM or the internal RAM in the next cycle will occur, after access to the external area. In this case, the chip select signal changes between the two cycles, but the address does not change.



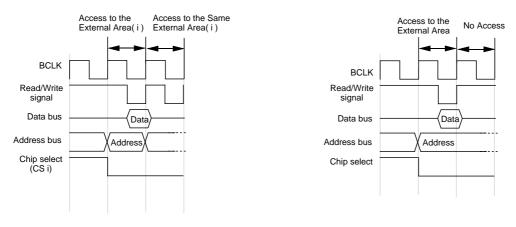


Example 3) After access the external area, only the address bus changes in the next cycle (the chip select signal does not change).

Example 4) After access the external area, either the address signal and the chip select signal do not change in the next cycle.

In this example, after access to the external area(i), an access to the area indicated by the same chip select signal(i) will occur in the next cycle. In this case, the address bus changes between the two cycles, but the chip select signal does not change.

In this example, any access to any area does not occur in the next cycle (either instruction prefetch does not occur). In this case, either the address bus and chip select signal do not change between the two cycles.



Note: These examples show the address bus and chip select signal within the successive two cycles. According to the combination of these examples, the chip select can be elongated to over 2cycles.

Figure 1.9.2. Output Examples about Address Bus and Chip Select Signal (Separated Bus without Wait)



(3) Read/write signals

With a 16-bit data bus (BYTE pin = "L"), bit 2 of the processor mode register 0 (address 000416) select the combinations of \overline{RD} , \overline{BHE} , and \overline{WR} signals or \overline{RD} , \overline{WRL} , and \overline{WRH} signals. With an 8-bit data bus (BYTE pin = "H"), use the combination of \overline{RD} , \overline{WR} , and \overline{BHE} signals. (Set bit 2 of the processor mode register 0 (address 000416) to "0".) Tables 1.9.3 and 1.9.4 show the operation of these signals.

After a reset has been cancelled, the combination of \overline{RD} , \overline{WR} , and \overline{BHE} signals is automatically selected. When switching to the \overline{RD} , \overline{WRL} , and \overline{WRH} combination, do not write to external memory until bit 2 of the processor mode register 0 (address 000416) has been set (Note).

Note: Before attempting to change the contents of the processor mode register 0, set bit 1 of the protect register (address 000A₁₆) to "1".

Data bus width	RD	WRL	WRH	Status of external data bus
	L	Н	Н	Read data
16-bit (BYTE = "L")	Н	L	Н	Write 1 byte of data to even address
	Н	Н	L	Write 1 byte of data to odd address
	Н	L	L	Write data to both even and odd addresses

Table 1.9.4. Operation of RD, WR, and BHE signals

Data bus width	RD	WR	BHE	A0	Status of external data bus
16-bit (BYTE = "L")	Н	L	L	Н	Write 1 byte of data to odd address
	L	Н	L	Н	Read 1 byte of data from odd address
	Н	L	Н	L	Write 1 byte of data to even address
	L	Н	Н	L	Read 1 byte of data from even address
	Н	L	L	L	Write data to both even and odd addresses
	L	Н	L	L	Read data from both even and odd addresses
8-bit (BYTE = "H")	Н	L	Not used	H/L	Write 1 byte of data
	L	Н	Not used	H/L	Read 1 byte of data

(4) ALE signal

The ALE signal latches the address when accessing the multiplex bus space. Latch the address when the ALE signal falls.

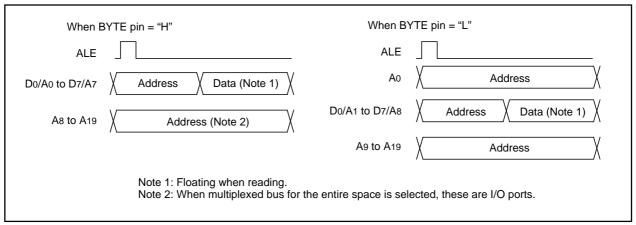


Figure 1.9.3. ALE signal and address/data bus



(5) The RDY signal

 \overline{RDY} is a signal that facilitates access to an external device that requires long access time. As shown in Figure 1.9.4, if an "L" is being input to the \overline{RDY} at the BCLK falling edge, the bus turns to the wait state. If an "H" is being input to the \overline{RDY} pin at the BCLK falling edge, the bus cancels the wait state. Table 1.9.5 shows the state of the microcomputer with the bus in the wait state, and Figure 1.9.4 shows an example in which the \overline{RD} signal is prolonged by the \overline{RDY} signal.

The \overline{RDY} signal is valid when accessing the external area during the bus cycle in which bits 4 to 7 of the chip select control register (address 000816) are set to "0". The \overline{RDY} signal is invalid when setting "1" to all bits 4 to 7 of the chip select control register (address 000816), but the \overline{RDY} pin should be treated as properly as in non-using.

Table 1.9.5. Microcomputer status in wait state (Note)

Item	Status	
Oscillation	On	
R/W signal, address bus, data bus, CS	Maintain status when RDY signal received	
ALE signal, HLDA, programmable I/O ports		
Internal peripheral circuits	On	

Note: The RDY signal cannot be received immediately prior to a software wait.

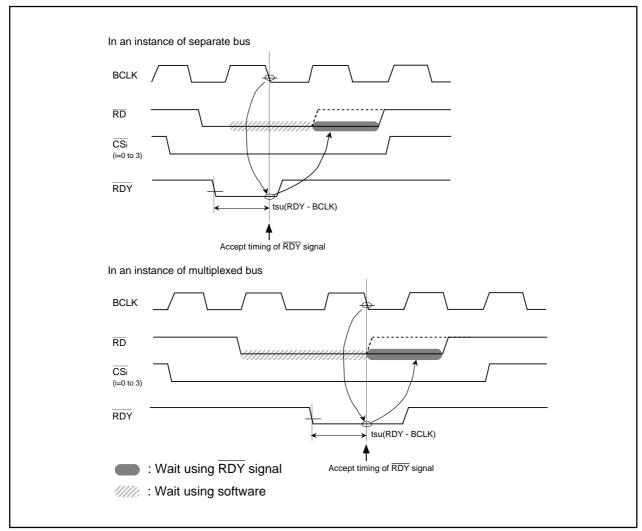


Figure 1.9.4. Example of RD signal extended by RDY signal



(6) Hold signal

The hold signal is used to transfer the bus privileges from the CPU to the external circuits. Inputting "L" to the $\overline{\text{HOLD}}$ pin places the microcomputer in the hold state at the end of the current bus access. This status is maintained and "L" is output from the $\overline{\text{HLDA}}$ pin as long as "L" is input to the $\overline{\text{HOLD}}$ pin. Table 1.9.6 shows the microcomputer status in the hold state.

Bus-using priorities are given to HOLD, DMAC, and CPU in order of decreasing precedence.

HOLD > DMAC > CPU

Figure 1.9.5. Bus-using priorities

Table 1.9.6. Microcomputer status in hold state

Ite	m	Status	
Oscillation		ON	
R/W signal, address bus, data l	ous, CS, BHE	Floating	
Programmable I/O ports P0, P1, P2, P3, P4, P5		Floating	
	P6, P7, P8, P9, P10	Maintains status when hold signal is received	
HLDA		Output "L"	
Internal peripheral circuits		ON (but watchdog timer stops)	
ALE signal		Undefined	

(7) External bus status when the internal area is accessed

Table 1.9.7 shows the external bus status when the internal area is accessed.

Table 1.9.7. External bus status when the internal area is accessed

Item SFF		SFR accessed	Internal ROM/RAM accessed	
Address bus		Address output	Maintain status before accessed	
			address of external area	
Data bus When read		Floating	Floating	
	When write Output data		Undefined	
$\overline{RD}, \overline{WR}, \overline{WF}$	RL, WRH	RD, WR, WRL, WRH output	Output "H"	
BHE		BHE output	Maintain status before accessed	
			status of external area	
CS		Output "H"	Output "H"	
ALE		Output "L"	Output "L"	

(8) BCLK output

The user can choose the BCLK output by use of bit 7 of processor mode register 0 (000416) (Note). When set to "1", the output floating.

Note: Before attempting to change the contents of the processor mode register 0, set bit 1 of the protect register (address 000A₁₆) to "1".

(9) Software wait

A software wait can be inserted by setting the wait bit (bit 7) of the processor mode register 1 (address 000516) (Note) and bits 4 to 7 of the chip select control register (address 000816).

A software wait is inserted in the internal ROM/RAM area and in the external memory area by setting the wait bit of the processor mode register 1. When set to "0", each bus cycle is executed in one BCLK cycle. When set to "1", each bus cycle is executed in two or three BCLK cycles. After the microcomputer has been reset, this bit defaults to "0". When set to "1", a wait is applied to all memory areas (two or three BCLK cycles), regardless of the contents of bits 4 to 7 of the chip select control register. Set this bit after referring to the recommended operating conditions (main clock input oscillation frequency) of the electric characteristics. However, when the user is using the RDY signal, the relevant bit in the chip select control register's bits 4 to 7 must be set to "0".

When the wait bit of the processor mode register 1 is "0", software waits can be set independently for each of the 4 areas selected using the chip select signal. Bits 4 to 7 of the chip select control register correspond to chip selects $\overline{CS0}$ to $\overline{CS3}$. When one of these bits is set to "1", the bus cycle is executed in one BCLK cycle. When set to "0", the bus cycle is executed in two or three BCLK cycles. These bits default to "0" after the microcomputer has been reset.

The SFR area is always accessed in two BCLK cycles regardless of the setting of these control bits. Also, insert a software wait if using the multiplex bus to access the external memory area.

Table 1.9.8 shows the software wait and bus cycles. Figure 1.9.6 shows example of bus timing when using software waits.

Note: Before attempting to change the contents of the processor mode register 1, set bit 1 of the protect register (address 000A₁₆) to "1".

Table 1.9.8. Software waits and bus cycles

Area	Bus status	Wait bit	Bits 4 to 7 of chip select control register	Bus cycle
SFR		Invalid	Invalid	2 BCLK cycles
Internal ROM/RAM		0	Invalid	1 BCLK cycle
		1	Invalid	2 BCLK cycles
External memory area	Separate bus	0	1	1 BCLK cycle
	Separate bus	0	0	2 BCLK cycles
	Separate bus	1	0 (Note)	2 BCLK cycles
	Multiplex bus	0	0	3 BCLK cycles
	Multiplex bus	1	0 (Note)	3 BCLK cycles

Note: When using the RDY signal, always set to "0".



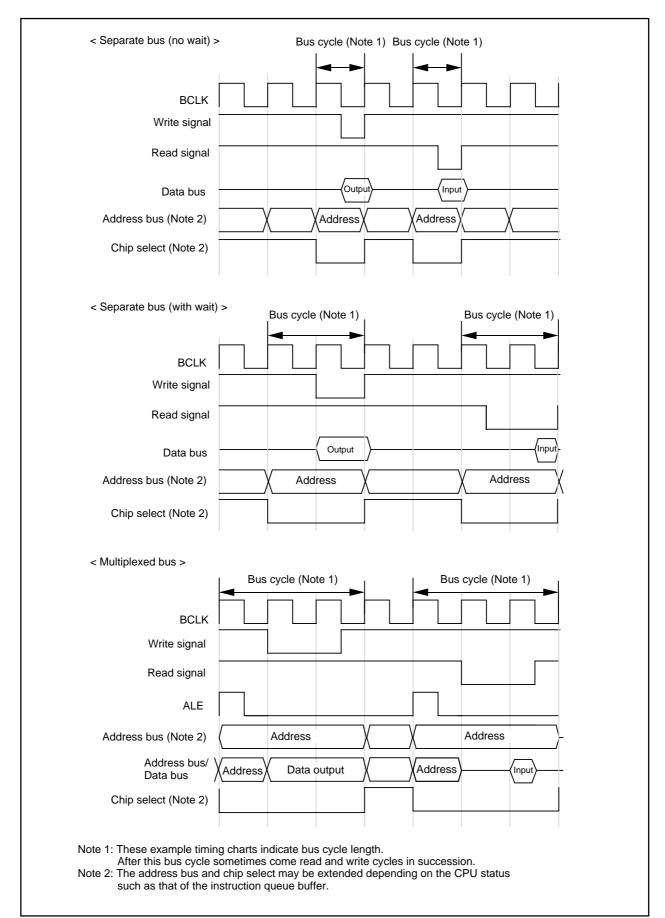


Figure 1.9.6. Typical bus timings using software wait



Clock Generating Circuit

The clock generating circuit contains two oscillator circuits that supply the operating clock sources to the CPU and internal peripheral units.

Table 1.10.1. Main clock and sub-clock generating circuits

	Main clock generating circuit	Sub-clock generating circuit	
Use of clock	• CPU's operating clock source • CPU's operating clock		
	Internal peripheral units'	Timer A/B's count clock	
	operating clock source	source	
Usable oscillator	Ceramic or crystal oscillator	Crystal oscillator	
Pins to connect oscillator	XIN, XOUT	Xcin, Xcout	
Oscillation stop/restart function	Available	Available	
Oscillator status immediately after reset	t Oscillating Stopped		
Other	Externally derived clock can be input		

Example of oscillator circuit

Figure 1.10.1 shows some examples of the main clock circuit, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Figure 1.10.2 shows some examples of sub-clock circuits, one using an oscillator connected to the circuit, and the other one using an externally derived clock for input. Circuit constants in Figures 1.10.1 and 1.10.2 vary with each oscillator used. Use the values recommended by the manufacturer of your oscillator.

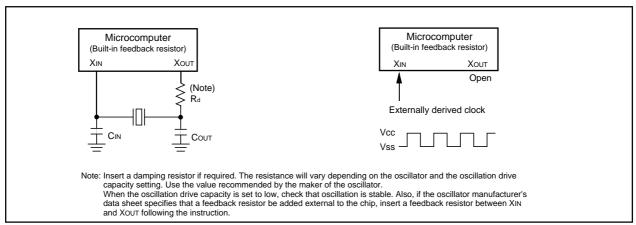


Figure 1.10.1. Examples of main clock

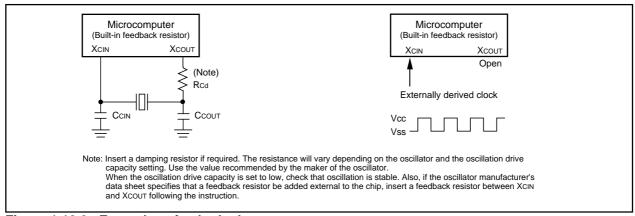


Figure 1.10.2. Examples of sub-clock

Clock Control

Figure 1.10.3 shows the block diagram of the clock generating circuit.

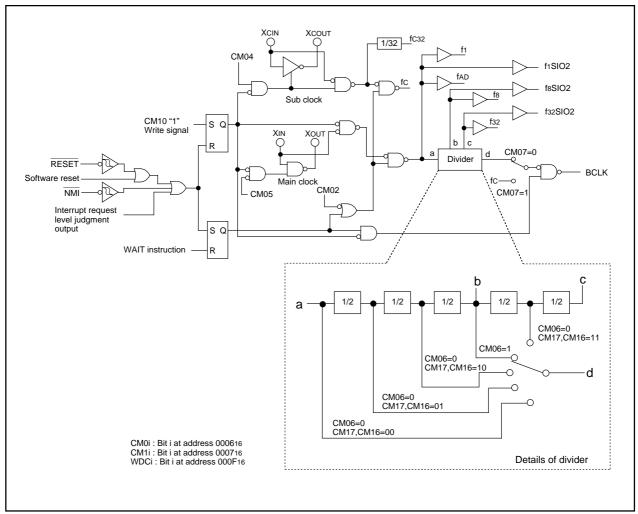


Figure 1.10.3. Clock generating circuit

The following paragraphs describes the clocks generated by the clock generating circuit.

(1) Main clock

The main clock is generated by the main clock oscillation circuit. After a reset, the clock is divided by 8 to the BCLK. The clock can be stopped using the main clock stop bit (bit 5 at address 000616). Stopping the clock, after switching the operating clock source of CPU to the sub-clock, reduces the power dissipation. After the oscillation of the main clock oscillation circuit has stabilized, the drive capacity of the main clock oscillation circuit can be reduced using the XIN-XOUT drive capacity select bit (bit 5 at address 000716). Reducing the drive capacity of the main clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting from high-speed/medium-speed mode to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

(2) Sub-clock

The sub-clock is generated by the sub-clock oscillation circuit. No sub-clock is generated after a reset. After oscillation is started using the port XC select bit (bit 4 at address 000616), the sub-clock can be selected as the BCLK by using the system clock select bit (bit 7 at address 000616). However, be sure that the sub-clock oscillation has fully stabilized before switching.

After the oscillation of the sub-clock oscillation circuit has stabilized, the drive capacity of the sub-clock oscillation circuit can be reduced using the XCIN-XCOUT drive capacity select bit (bit 3 at address 000616). Reducing the drive capacity of the sub-clock oscillation circuit reduces the power dissipation. This bit changes to "1" when shifting to stop mode and at a reset.

When the XCIN/XCOUT is used, set ports P86 and P87 as the input ports without pull-up.

(3) **BCLK**

The BCLK is the clock that drives the CPU, and is fc or the clock is derived by dividing the main clock by 1, 2, 4, 8, or 16. The BCLK is derived by dividing the main clock by 8 after a reset. The BCLK signal can be output from BCLK pin by the BCLK output disable bit (bit 7 at address 000416) in the memory expansion and the microprocessor modes.

The main clock division select bit 0(bit 6 at address 000616) changes to "1" when shifting from high-speed/medium-speed to stop mode and at reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

(4) Peripheral function clock(f1, f8, f32, f1SIO2, f8SIO2, f32SIO2, fAD)

The clock for the peripheral devices is derived from the main clock or by dividing it by 1, 8, or 32. The peripheral function clock is stopped by stopping the main clock or by setting the WAIT peripheral function clock stop bit (bit 2 at 000616) to "1" and then executing a WAIT instruction.

(5) fC32

This clock is derived by dividing the sub-clock by 32. It is used for the timer A and timer B counts.

(6) fc

This clock has the same frequency as the sub-clock. It is used for the BCLK and for the watchdog timer.



Figure 1.10.4 shows the system clock control registers 0 and 1.

b7 b6 b5 b4 b3 b2 b1 b0	Symbol CM0	Address 000616	When reset 4816	
	Bit symbol	Bit name	Function	RW
	CM00	Clock output function select bit	0 0 : I/O port P57 0 1 : fc output	00
	CM01	(Valid only in single-chip mode)	1 0 : f8 output 1 1 : f32 output	00
	CM02	WAIT peripheral function clock stop bit	0 : Do not stop peripheral function clock in wait mode 1 : Stop peripheral function clock in wait mode (Note 8)	00
	CM03	XCIN-XCOUT drive capacity select bit (Note 2)	0 : LOW 1 : HIGH	00
	CM04	Port Xc select bit	0 : I/O port 1 : ХСІN-ХСОUT generation (Note 9)	00
	CM05	Main clock (XIN-XOUT) stop bit (Note 3, 4, 5)	0 : On 1 : Off	00
	CM06	Main clock division select bit 0 (Note 7)	0 : CM16 and CM17 valid 1 : Division by 8 mode	00
	CM07	System clock select bit (Note 6)	0 : XIN, XOUT 1 : XCIN, XCOUT	00

- Note 1: Set bit 0 of the protect register (address 000A16) to "1" before writing to this register.
- Note 2: Changes to "1" when shiffing to stop mode and at a reset.
- Note 3: When entering low power dissipation mode, main clock stops by using this bit. To stop the main clock, when the sub clock oscillation is stable, set system clock select bit (CM07) to "1" before setting this bit to "1".
- Note 4: When inputting external clock, only clock oscillation buffer is stopped and clock input is acceptable.

 Note 5: If this bit is set to "1", XOUT turns "H". The built-in feedback resistor remains being connected, so XIN turns pulled up to XOUT ("H") via the feedback resistor.

 Note 6: Set port XC select bit (CM04) to "1" and stabilize the sub-clock oscillating before setting this bit from "0" to "1".
- Do not write to both bits at the same time. And also, set the main clock stop bit (CM05) to "0" and stabilize the main clock oscillating before setting this bit from "1" to "0".
- Note 7: This bit changes to "1" when shifting from high-speed/medium-speed mode to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.
- Note 8: fc32 is not included. Do not set to "1" when using low-speed or low power dissipation mode. Note 9: When the XCIN/XCOUT is used, set ports P86 and P87 as the input ports without pull-up.
- System clock control register 1 (Note 1)

b7 b6 b5 b4 b3 b2 b1 b0 0 0 0 0 0	Symbol CM1	Address 000716	When reset 2016	
	Bit symbol	Bit name	Function	R W
1	CM10	All clock stop control bit (Note4)	0 : Clock on 1 : All clocks off (stop mode)	00
	Reserved	bit	Always set to "0"	00
Reserved b		bit	Always set to "0"	00
	Reserved bit		Always set to "0"	00
	Reserved bit		Always set to "0"	00
[CM15	XIN-XOUT drive capacity select bit (Note 2)	0 : LOW 1 : HIGH	00
	CM16	Main clock division select bit 1 (Note 3)	0 0 : No division mode 0 1 : Division by 2 mode	00
·	CM17		1 0 : Division by 4 mode 1 1 : Division by 16 mode	

- Note 1: Set bit 0 of the protect register (address 000A₁₆) to "1" before writing to this register.
- Note 2: This bit changes to "1" when shifting from high-speed/medium-speed mode to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

 Note 3: Can be selected when bit 6 of the system clock control register 0 (address 000616) is "0". If "1", division mode is
- fixed at 8.
- Note 4: If this bit is set to "1", XOUT turns "H", and the built-in feedback resistor is cut off. XCIN and XCOUT turn highimpedance state.

Figure 1.10.4. Clock control registers 0 and 1



Clock Output

In single-chip mode, the clock output function select bits (bits 0 and 1 at address 000616) enable f8, f32, or fc to be output from the P57/CLKOUT pin. When the WAIT peripheral function clock stop bit (bit 2 at address 000616) is set to "1", the output of f8 and f32 stops when a WAIT instruction is executed.

Stop Mode

Writing "1" to the all-clock stop control bit (bit 0 at address 000716) stops all oscillation and the microcomputer enters stop mode. In stop mode, the content of the internal RAM is retained provided that VCC remains above 2V.

Because the oscillation , BCLK, f1 to f32, f1sIO2 to f32sIO2, fc, fC32, and fAD stops in stop mode, peripheral functions such as the A-D converter and watchdog timer do not function. However, timer A and timer B operate provided that the event counter mode is set to an external pulse, and UARTi(i = 0 to 2), SI/O3,4 functions provided an external clock is selected. Table 1.10.2 shows the status of the ports in stop mode. Stop mode is cancelled by a hardware reset or an interrupt. If an interrupt is to be used to cancel stop mode, that interrupt must first have been enabled, and the priority level of the interrupt which is not used to cancel must have been changed to 0. If returning by an interrupt, that interrupt routine is executed. If only a hardware reset or an $\overline{\text{NMI}}$ interrupt is used to cancel stop mode, change the priority level of all interrupt to 0, then shift to stop mode.

When shifting from high-speed/medium-speed mode to stop mode and at a reset, the main clock division select bit 0 (bit 6 at address 000616) is set to "1". When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained.

Table 1.10.2. Port status during stop mode

Pin		Memory expansion mode	Single-chip mode
		Microprocessor mode	
Address bus, data bus, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$,		Retains status before stop mode	
BHE			
RD, WR, WRL, WRH		"H"	
HLDA, BCLK		"H"	
ALE		"H"	
Port		Retains status before stop mode	Retains status before stop mode
CLKout	When fc selected	Valid only in single-chip mode	"H"
	When f8, f32 selected	Valid only in single-chip mode	Retains status before stop mode



Wait Mode

When a WAIT instruction is executed, the BCLK stops and the microcomputer enters the wait mode. In this mode, oscillation continues but the BCLK and watchdog timer stop. Writing "1" to the WAIT peripheral function clock stop bit and executing a WAIT instruction stops the clock being supplied to the internal peripheral functions, allowing power dissipation to be reduced. However, peripheral function clock fc32 does not stop so that the peripherals using fc32 do not contribute to the power saving. When the MCU running in low-speed or low power dissipation mode, do not enter WAIT mode with this bit set to "1". Table 1.10.3 shows the status of the ports in wait mode.

Wait mode is cancelled by a hardware reset or an interrupt. If an interrupt is used to cancel wait mode, that interrupt must first have been enabled, and the priority level of the interrupt which is not used to cancel must have been changed to 0. If returning by an interrupt, the clock in which the WAIT instruction executed is set to BCLK by the microcomputer, and the action is resumed from the interrupt routine. If only a hardware reset or an $\overline{\text{NMI}}$ interrupt is used to cancel wait mode, change the priority level of all interrupt to 0,then shift to wait mode.

Table 1.10.3. Port status during wait mode

Pin		Memory expansion mode	Single-chip mode
		Microprocessor mode	
Address bus, dat	a bus, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$,	Retains status before wait mode	
BHE			
\overline{RD} , \overline{WR} , \overline{WRL} , \overline{V}	VRH	"H"	
HLDA,BCLK		"H"	
ALE		"H"	
Port		Retains status before wait mode	Retains status before wait mode
CLKout	When fc selected	Valid only in single-chip mode	Does not stop
	When f8, f32 selected	Valid only in single-chip mode	Does not stop when the WAIT
			peripheral function clock stop
			bit is "0".
			When the WAIT peripheral
			function clock stop bit is "1",
			the status immediately prior
			to entering wait mode is main-
			tained.



Status Transition of BCLK

Power dissipation can be reduced and low-voltage operation achieved by changing the count source for BCLK. Table 1.10.4 shows the operating modes corresponding to the settings of system clock control registers 0 and 1.

When reset, the device starts in division by 8 mode. The main clock division select bit 0(bit 6 at address 000616) changes to "1" when shifting from high-speed/medium-speed to stop mode and at a reset. When shifting from low-speed/low power dissipation mode to stop mode, the value before stop mode is retained. The following shows the operational modes of BCLK.

(1) Division by 2 mode

The main clock is divided by 2 to obtain the BCLK.

(2) Division by 4 mode

The main clock is divided by 4 to obtain the BCLK.

(3) Division by 8 mode

The main clock is divided by 8 to obtain the BCLK. When reset, the device starts operating from this mode. Before the user can go from this mode to no division mode, division by 2 mode, or division by 4 mode, the main clock must be oscillating stably. When going to low-speed or lower power consumption mode, make sure the sub-clock is oscillating stably.

(4) Division by 16 mode

The main clock is divided by 16 to obtain the BCLK.

(5) No-division mode

The main clock is divided by 1 to obtain the BCLK.

(6) Low-speed mode

fC is used as the BCLK. Note that oscillation of both the main and sub-clocks must have stabilized before transferring from this mode to another or vice versa. At least 2 to 3 seconds are required after the sub-clock starts. Therefore, the program must be written to wait until this clock has stabilized immediately after powering up and after stop mode is cancelled.

(7) Low power dissipation mode

fc is the BCLK and the main clock is stopped.

Note: Before the count source for BCLK can be changed from XIN to XCIN or vice versa, the clock to which the count source is going to be switched must be oscillating stably. Allow a wait time in software for the oscillation to stabilize before switching over the clock.

Table 1.10.4. Operating modes dictated by settings of system clock control registers 0 and 1

CM17	CM16	CM07	CM06	CM05	CM04	Operating mode of BCLK
0	1	0	0	0	Invalid	Division by 2 mode
1	0	0	0	0	Invalid	Division by 4 mode
Invalid	Invalid	0	1	0	Invalid	Division by 8 mode
1	1	0	0	0	Invalid	Division by 16 mode
0	0	0	0	0	Invalid	No-division mode
Invalid	Invalid	1	Invalid	0	1	Low-speed mode
Invalid	Invalid	1	Invalid	1	1	Low power dissipation mode



Power control

The following is a description of the three available power control modes:

Modes

Power control is available in three modes.

(a) Normal operation mode

High-speed mode

Divide-by-1 frequency of the main clock becomes the BCLK. The CPU operates with the BCLK. Each peripheral function operates according to its assigned clock.

Medium-speed mode

Divide-by-2, divide-by-4, divide-by-8, or divide-by-16 frequency of the main clock becomes the BCLK. The CPU operates with the BCLK. Each peripheral function operates according to its assigned clock.

Low-speed mode

fc becomes the BCLK. The CPU operates according to the fc clock. The fc clock is supplied by the subclock. Each peripheral function operates according to its assigned clock.

Low power dissipation mode

The main clock operating in low-speed mode is stopped. The CPU operates according to the fc clock. The fc clock is supplied by the subclock. The only peripheral functions that operate are those with the subclock selected as the count source.

(b) Wait mode

The CPU operation is stopped. The oscillators do not stop.

(c) Stop mode

All oscillators stop. The CPU and all built-in peripheral functions stop. This mode, among the three modes listed here, is the most effective in decreasing power consumption.

Figure 1.10.5 is the state transition diagram of the above modes.



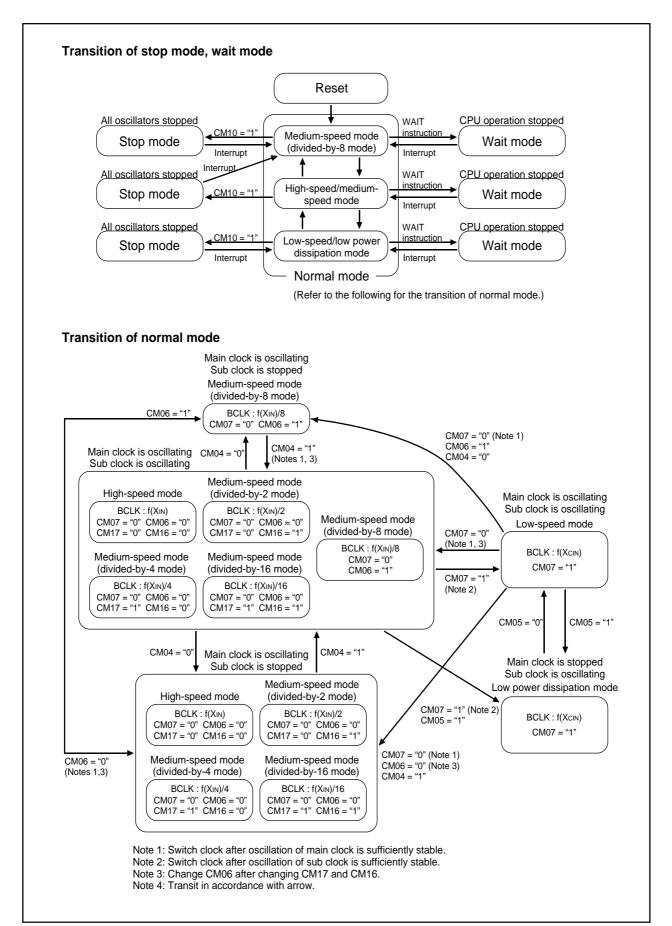


Figure 1.10.5. State transition diagram of Power control mode



Protection

The protection function is provided so that the values in important registers cannot be changed in the event that the program runs out of control. Figure 1.10.6 shows the protect register. The values in the processor mode register 0 (address 000416), processor mode register 1 (address 000516), system clock control register 0 (address 000616), system clock control register 1 (address 000716), port P9 direction register (address 03F316), SI/O3 control register (address 036216) and SI/O4 control register (address 036616) can only be changed when the respective bit in the protect register is set to "1". Therefore, important outputs can be allocated to port P9.

If, after "1" (write-enabled) has been written to the port P9 direction register and SI/Oi control register (i=3,4) write-enable bit (bit 2 at address 000A16), a value is written to any address, the bit automatically reverts to "0" (write-inhibited). However, the system clock control registers 0 and 1 write-enable bit (bit 0 at 000A16) and processor mode register 0 and 1 write-enable bit (bit 1 at 000A16) do not automatically return to "0" after a value has been written to an address. The program must therefore be written to return these bits to "0".

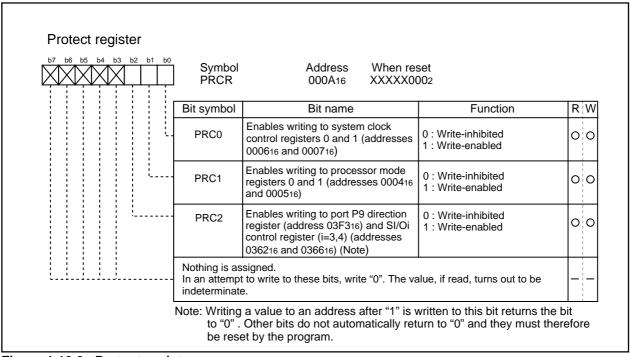


Figure 1.10.6. Protect register

Overview of Interrupt

Type of Interrupts

Figure 1.11.1 lists the types of interrupts.

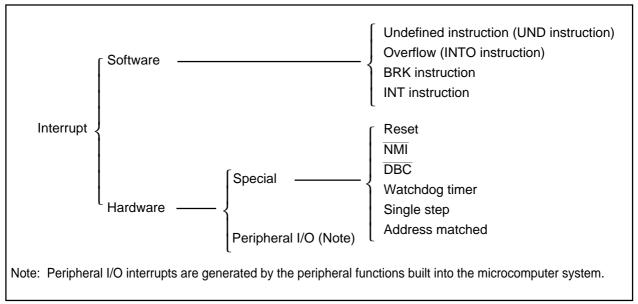


Figure 1.11.1. Classification of interrupts

• Maskable interrupt : An interrupt which can be enabled (disabled) by the interrupt enable flag

(I flag) or whose interrupt priority can be changed by priority level.

• Non-maskable interrupt : An interrupt which cannot be enabled (disabled) by the interrupt enable flag

(I flag) or whose interrupt priority cannot be changed by priority level.

Software Interrupts

A software interrupt occurs when executing certain instructions. Software interrupts are non-maskable interrupts.

• Undefined instruction interrupt

An undefined instruction interrupt occurs when executing the UND instruction.

Overflow interrupt

An overflow interrupt occurs when executing the INTO instruction with the overflow flag (O flag) set to "1". The following are instructions whose O flag changes by arithmetic:

ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, SUB

BRK interrupt

A BRK interrupt occurs when executing the BRK instruction.

INT interrupt

An INT interrupt occurs when specifying one of software interrupt numbers 0 through 63 and executing the INT instruction. Software interrupt numbers 0 through 31 are assigned to peripheral I/O interrupts, so executing the INT instruction allows executing the same interrupt routine that a peripheral I/O interrupt does.

The stack pointer (SP) used for the INT interrupt is dependent on which software interrupt number is involved.

So far as software interrupt numbers 0 through 31 are concerned, the microcomputer saves the stack pointer assignment flag (U flag) when it accepts an interrupt request. If change the U flag to "0" and select the interrupt stack pointer (ISP), and then execute an interrupt sequence. When returning from the interrupt routine, the U flag is returned to the state it was before the acceptance of interrupt request. So far as software numbers 32 through 63 are concerned, the stack pointer does not make a shift.



Hardware Interrupts

Hardware interrupts are classified into two types — special interrupts and peripheral I/O interrupts.

(1) Special interrupts

Special interrupts are non-maskable interrupts.

Reset

Reset occurs if an "L" is input to the RESET pin.

• NMI interrupt

An $\overline{\text{NMI}}$ interrupt occurs if an "L" is input to the $\overline{\text{NMI}}$ pin.

• DBC interrupt

This interrupt is exclusively for the debugger, do not use it in other circumstances.

Watchdog timer interrupt

Generated by the watchdog timer.

• Single-step interrupt

This interrupt is exclusively for the debugger, do not use it in other circumstances. With the debug flag (D flag) set to "1", a single-step interrupt occurs after one instruction is executed.

Address match interrupt

An address match interrupt occurs immediately before the instruction held in the address indicated by the address match interrupt register is executed with the address match interrupt enable bit set to "1". If an address other than the first address of the instruction in the address match interrupt register is set, no address match interrupt occurs.

(2) Peripheral I/O interrupts

A peripheral I/O interrupt is generated by one of built-in peripheral functions. Built-in peripheral functions are dependent on classes of products, so the interrupt factors too are dependent on classes of products. The interrupt vector table is the same as the one for software interrupt numbers 0 through 31 the INT instruction uses. Peripheral I/O interrupts are maskable interrupts.

Bus collision detection interrupt

This is an interrupt that the serial I/O bus collision detection generates.

DMA0 interrupt, DMA1 interrupt

These are interrupts that DMA generates.

Key-input interrupt

A key-input interrupt occurs if an "L" is input to the KI pin.

• A-D conversion interrupt

This is an interrupt that the A-D converter generates.

• UART0, UART1, UART2/NACK, SI/O3 and SI/O4 transmission interrupt

These are interrupts that the serial I/O transmission generates.

• UART0, UART1, UART2/ACK, SI/O3 and SI/O4 reception interrupt

These are interrupts that the serial I/O reception generates.

Timer A0 interrupt through timer A4 interrupt

These are interrupts that timer A generates

Timer B0 interrupt through timer B5 interrupt

These are interrupts that timer B generates.

• INTO interrupt through INT5 interrupt

An INT interrupt occurs if either a rising edge or a falling edge or a both edge is input to the INT pin.



Interrupts and Interrupt Vector Tables

If an interrupt request is accepted, a program branches to the interrupt routine set in the interrupt vector table. Set the first address of the interrupt routine in each vector table. Figure 1.11.2 shows the format for specifying the address.

Two types of interrupt vector tables are available — fixed vector table in which addresses are fixed and variable vector table in which addresses can be varied by the setting.

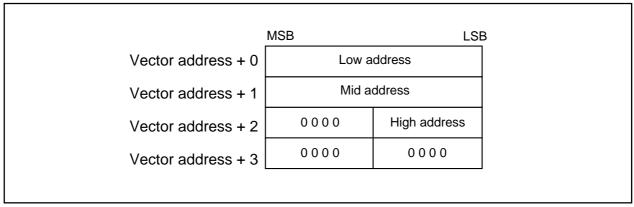


Figure 1.11.2. Format for specifying interrupt vector addresses

Fixed vector tables

The fixed vector table is a table in which addresses are fixed. The vector tables are located in an area extending from FFFDC16 to FFFFF16. One vector table comprises four bytes. Set the first address of interrupt routine in each vector table. Table 1.11.1 shows the interrupts assigned to the fixed vector tables and addresses of vector tables.

Table 1.11.1. Interrupts assigned to the fixed vector tables and addresses of vector tables

Interrupt source	Vector table addresses	Remarks
	Address (L) to address (H)	
Undefined instruction	FFFDC16 to FFFDF16	Interrupt on UND instruction
Overflow	FFFE016 to FFFE316	Interrupt on INTO instruction
BRK instruction	FFFE416 to FFFE716	If the vector contains FF16, program execution starts from
		the address shown by the vector in the variable vector table
Address match	FFFE816 to FFFEB16	There is an address-matching interrupt enable bit
Single step (Note)	FFFEC16 to FFFEF16	Do not use
Watchdog timer	FFFF016 to FFFF316	
DBC (Note)	FFFF416 to FFFF716	Do not use
NMI	FFFF816 to FFFFB16	External interrupt by input to NMI pin
Reset	FFFFC16 to FFFFF16	

Note: Interrupts used for debugging purposes only.



Variable vector tables

The addresses in the variable vector table can be modified, according to the user's settings. Indicate the first address using the interrupt table register (INTB). The 256-byte area subsequent to the address the INTB indicates becomes the area for the variable vector tables. One vector table comprises four bytes. Set the first address of the interrupt routine in each vector table. Table 1.11.2 shows the interrupts assigned to the variable vector tables and addresses of vector tables.

Table 1.11.2. Interrupts assigned to the variable vector tables and addresses of vector tables

Software interrupt number	Vector table address Address (L) to address (H)		Remarks
Software interrupt number 0	+0 to +3 (Note 1)	BRK instruction	Cannot be masked I flag
Software interrupt number 4	+16 to +19 (Note 1)	ĪNT3	
Software interrupt number 5	+20 to +23 (Note 1)	Timer B5	
Software interrupt number 6	+24 to +27 (Note 1)	Timer B4	
Software interrupt number 7	+28 to +31 (Note 1)	Timer B3	
Software interrupt number 8	+32 to +35 (Note 1)	SI/O4/INT5 (Note 2)	
Software interrupt number 9	+36 to +39 (Note 1)	SI/O3/INT4 (Note 2)	
Software interrupt number 10	+40 to +43 (Note 1)	Bus collision detection	
Software interrupt number 11	+44 to +47 (Note 1)	DMA0	
Software interrupt number 12	+48 to +51 (Note 1)	DMA1	
Software interrupt number 13	+52 to +55 (Note 1)	Key input interrupt	
Software interrupt number 14	+56 to +59 (Note 1)	A-D	
Software interrupt number 15	+60 to +63 (Note 1)	UART2 transmit/NACK (Note 3)	
Software interrupt number 16	+64 to +67 (Note 1)	UART2 receive/ACK (Note 3)	
Software interrupt number 17	+68 to +71 (Note 1)	UART0 transmit	
Software interrupt number 18	+72 to +75 (Note 1)	UART0 receive	
Software interrupt number 19	+76 to +79 (Note 1)	UART1 transmit	
Software interrupt number 20	+80 to +83 (Note 1)	UART1 receive	
Software interrupt number 21	+84 to +87 (Note 1)	Timer A0	
Software interrupt number 22	+88 to +91 (Note 1)	Timer A1	
Software interrupt number 23	+92 to +95 (Note 1)	Timer A2	
Software interrupt number 24	+96 to +99 (Note 1)	Timer A3	
Software interrupt number 25	+100 to +103 (Note 1)	Timer A4	
Software interrupt number 26	+104 to +107 (Note 1)	Timer B0	
Software interrupt number 27	+108 to +111 (Note 1)	Timer B1	
Software interrupt number 28	+112 to +115 (Note 1)	Timer B2	
Software interrupt number 29	+116 to +119 (Note 1)	ĪNT0	
Software interrupt number 30	+120 to +123 (Note 1)	INT1	
Software interrupt number 31	+124 to +127 (Note 1)	INT2	
Software interrupt number 32	+128 to +131 (Note 1)		Connot be marked ! !!-
to Software interrupt number 63	to +252 to +255 (Note 1)	Software interrupt	Cannot be masked I fla

Note 1: Address relative to address in interrupt table register (INTB).

Note 2: It is selected by interrupt request cause bit (bit 6, 7 in address 035F16).

Note 3: When IIC mode is selected, NACK and ACK interrupts are selected.



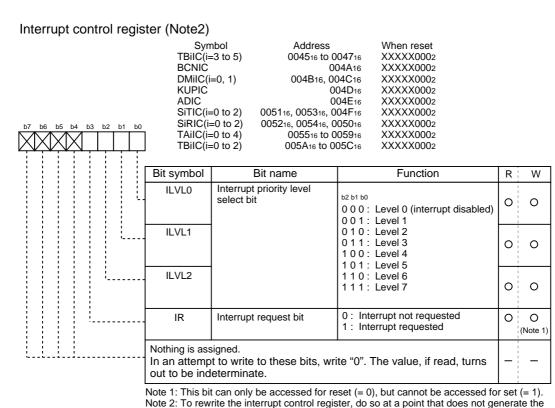
Interrupt Control

Descriptions are given here regarding how to enable or disable maskable interrupts and how to set the priority to be accepted. What is described here does not apply to non-maskable interrupts.

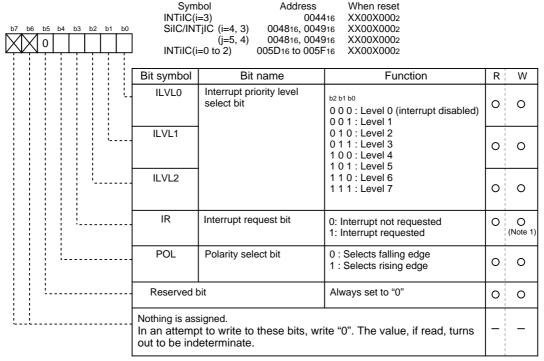
Enable or disable a maskable interrupt using the interrupt enable flag (I flag), interrupt priority level selection bit, or processor interrupt priority level (IPL). Whether an interrupt request is present or absent is indicated by the interrupt request bit. The interrupt request bit and the interrupt priority level selection bit are located in the interrupt control register of each interrupt. Also, the interrupt enable flag (I flag) and the IPL are located in the flag register (FLG).

Figure 1.11.3 shows the memory map of the interrupt control registers.





Note 2: To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, see the precautions for interrupts.



Note 1: This bit can only be accessed for reset (= 0), but cannot be accessed for set (= 1). Note 2: To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, see the precautions for interrupts.

Figure 1.11.3. Interrupt control registers



Interrupt Enable Flag (I flag)

The interrupt enable flag (I flag) controls the enabling and disabling of maskable interrupts. Setting this flag to "1" enables all maskable interrupts; setting it to "0" disables all maskable interrupts. This flag is set to "0" after reset.

Interrupt Request Bit

The interrupt request bit is set to "1" by hardware when an interrupt is requested. After the interrupt is accepted and jumps to the corresponding interrupt vector, the request bit is set to "0" by hardware. The interrupt request bit can also be set to "0" by software. (Do not set this bit to "1").

Interrupt Priority Level Select Bit and Processor Interrupt Priority Level (IPL)

Set the interrupt priority level using the interrupt priority level select bit, which is one of the component bits of the interrupt control register. When an interrupt request occurs, the interrupt priority level is compared with the IPL. The interrupt is enabled only when the priority level of the interrupt is higher than the IPL. Therefore, setting the interrupt priority level to "0" disables the interrupt.

Table 1.11.3 shows the settings of interrupt priority levels and Table 1.11.4 shows the interrupt levels enabled, according to the contents of the IPL.

The following are conditions under which an interrupt is accepted:

- · interrupt enable flag (I flag) = "1"
- · interrupt request bit = "1"
- · interrupt priority level > IPL

The interrupt enable flag (I flag), the interrupt request bit, the interrupt priority select bit, and the IPL are independent, and they are not affected by one another.

Table 1.11.3. Settings of interrupt priority levels

Interrupt place		Interrupt priority level	Priority order		
b2 b1	b0				
0 0	0	Level 0 (interrupt disabled)			
0 0	1	Level 1	Low		
0 1	0	Level 2			
0 1	1	Level 3			
1 0	0	Level 4			
1 0	1	Level 5			
1 1	0	Level 6			
1 1	1	Level 7	High		

Table 1.11.4. Interrupt levels enabled according to the contents of the IPL

IPL		Enabled interrupt priority levels
IPL2 IPL1 I	IPL ₀	
0 0	0	Interrupt levels 1 and above are enabled
0 0	1	Interrupt levels 2 and above are enabled
0 1	0	Interrupt levels 3 and above are enabled
0 1	1	Interrupt levels 4 and above are enabled
1 0	0	Interrupt levels 5 and above are enabled
1 0	1	Interrupt levels 6 and above are enabled
1 1	0	Interrupt levels 7 and above are enabled
1 1	1	All maskable interrupts are disabled



Rewrite the interrupt control register

To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

Example 1:

INT_SWITCH1:

FCLR I ; Disable interrupts.

AND.B #00h, 0055h; Clear TAOIC int. priority level and int. request bit.

NOP ; Four NOP instructions are required when using HOLD function.

NOP ; Enable interrupts.

Example 2:

INT_SWITCH2:

FCLR I ; Disable interrupts.

AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.

MOV.W MEM, R0 ; Dummy read. FSET I ; Enable interrupts.

Example 3:

INT_SWITCH3:

PUSHC FLG ; Push Flag register onto stack

FCLR I ; Disable interrupts.

AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.

POPC FLG ; Enable interrupts.

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change the register.

Instructions: AND, OR, BCLR, BSET



Interrupt Sequence

An interrupt sequence — what are performed over a period from the instant an interrupt is accepted to the instant the interrupt routine is executed — is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

In the interrupt sequence, the processor carries out the following in sequence given:

- (1) CPU gets the interrupt information (the interrupt number and interrupt request level) by reading address 0000016. After this, the corresponding interrupt request bit becomes "0".
- (2) Saves the content of the flag register (FLG) as it was immediately before the start of interrupt sequence in the temporary register (Note) within the CPU.
- (3) Sets the interrupt enable flag (I flag), the debug flag (D flag), and the stack pointer select flag (U flag) to "0" (the U flag, however does not change if the INT instruction, in software interrupt numbers 32 through 63, is executed)
- (4) Saves the content of the temporary register (Note) within the CPU in the stack area.
- (5) Saves the content of the program counter (PC) in the stack area.
- (6) Sets the interrupt priority level of the accepted instruction in the IPL.

After the interrupt sequence is completed, the processor resumes executing instructions from the first address of the interrupt routine.

Note: This register cannot be utilized by the user.

Interrupt Response Time

'Interrupt response time' is the period between the instant an interrupt occurs and the instant the first instruction within the interrupt routine has been executed. This time comprises the period from the occurrence of an interrupt to the completion of the instruction under execution at that moment (a) and the time required for executing the interrupt sequence (b). Figure 1.11.4 shows the interrupt response time.

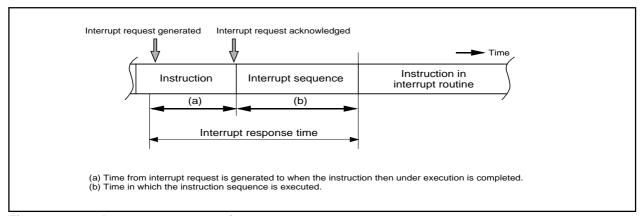


Figure 1.11.4. Interrupt response time



Time (a) is dependent on the instruction under execution. Thirty cycles is the maximum required for the DIVX instruction (without wait).

Time (b) is as shown in Table 1.11.5.

Table 1.11.5. Time required for executing the interrupt sequence

Interrupt vector address	Stack pointer (SP) value	16-Bit bus, without wait	8-Bit bus, without wait
Even	Even	18 cycles (Note 1)	20 cycles (Note 1)
Even	Odd	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Even	19 cycles (Note 1)	20 cycles (Note 1)
Odd (Note 2)	Odd	20 cycles (Note 1)	20 cycles (Note 1)

Note 1: Add 2 cycles in the case of a \overline{DBC} interrupt; add 1 cycle in the case either of an address match interrupt or of a single-step interrupt.

Note 2: Locate an interrupt vector address in an even address, if possible.

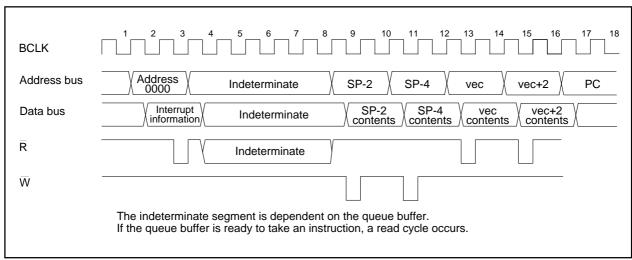


Figure 1.11.5. Time required for executing the interrupt sequence

Variation of IPL when Interrupt Request is Accepted

If an interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL. If an interrupt request, that does not have an interrupt priority level, is accepted, one of the values shown in Table 1.11.6 is set in the IPL.

Table 1.11.6. Relationship between interrupts without interrupt priority levels and IPL

Interrupt sources without priority levels	Value set in the IPL
Watchdog timer, NMI	7
Reset	0
Other	Not changed



Saving Registers

In the interrupt sequence, only the contents of the flag register (FLG) and that of the program counter (PC) are saved in the stack area.

First, the processor saves the four higher-order bits of the program counter, and 4 upper-order bits and 8 lower-order bits of the FLG register, 16 bits in total, in the stack area, then saves 16 lower-order bits of the program counter. Figure 1.11.6 shows the state of the stack as it was before the acceptance of the interrupt request, and the state the stack after the acceptance of the interrupt request.

Save other necessary registers at the beginning of the interrupt routine using software. Using the PUSHM instruction alone can save all the registers except the stack pointer (SP).

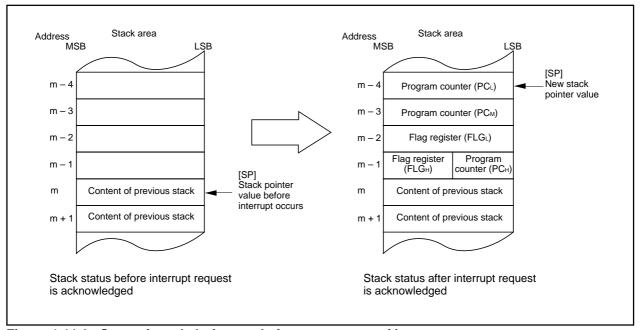


Figure 1.11.6. State of stack before and after acceptance of interrupt request



The operation of saving registers carried out in the interrupt sequence is dependent on whether the content of the stack pointer (Note), at the time of acceptance of an interrupt request, is even or odd. If the content of the stack pointer (Note) is even, the content of the flag register (FLG) and the content of the program counter (PC) are saved, 16 bits at a time. If odd, their contents are saved in two steps, 8 bits at a time. Figure 1.11.7 shows the operation of the saving registers.

Note: When any INT instruction in software numbers 32 to 63 has been executed, this is the stack pointer indicated by the U flag. Otherwise, it is the interrupt stack pointer (ISP).

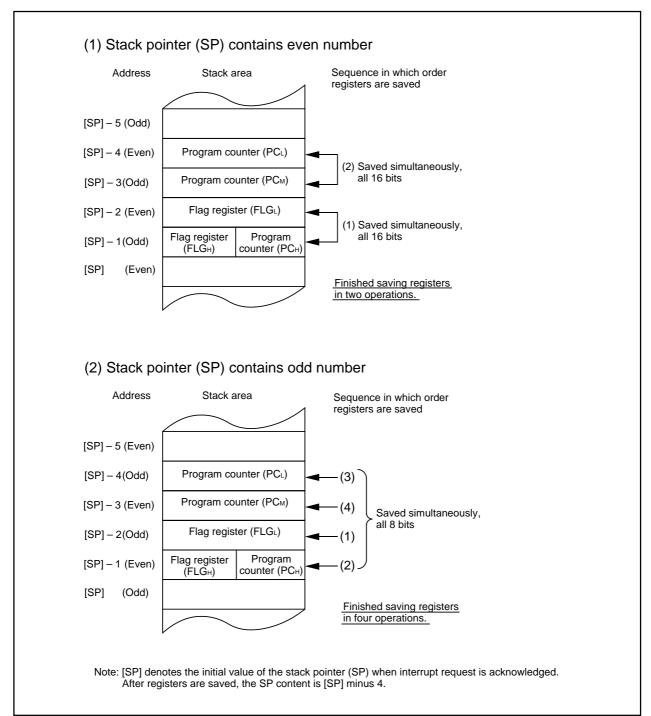


Figure 1.11.7. Operation of saving registers

Returning from an Interrupt Routine

Executing the REIT instruction at the end of an interrupt routine returns the contents of the flag register (FLG) as it was immediately before the start of interrupt sequence and the contents of the program counter (PC), both of which have been saved in the stack area. Then control returns to the program that was being executed before the acceptance of the interrupt request, so that the suspended process resumes.

Return the other registers saved by software within the interrupt routine using the POPM or similar instruction before executing the REIT instruction.

Interrupt Priority

If there are two or more interrupt requests occurring at a point in time within a single sampling (checking whether interrupt requests are made), the interrupt assigned a higher priority is accepted.

Assign an arbitrary priority to maskable interrupts (peripheral I/O interrupts) using the interrupt priority level select bit. If the same interrupt priority level is assigned, however, the interrupt assigned a higher hardware priority is accepted.

Priorities of the special interrupts, such as Reset (dealt with as an interrupt assigned the highest priority), watchdog timer interrupt, etc. are regulated by hardware.

Figure 1.11.8 shows the priorities of hardware interrupts.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, control branches invariably to the interrupt routine.

Reset > NMI > DBC > Watchdog timer > Peripheral I/O > Single step > Address match

Figure 1.11.8. Hardware interrupts priorities

Interrupt resolution circuit

When two or more interrupts are generated simultaneously, this circuit selects the interrupt with the highest priority level. Figure 1.11.9 shows the circuit that judges the interrupt priority level.



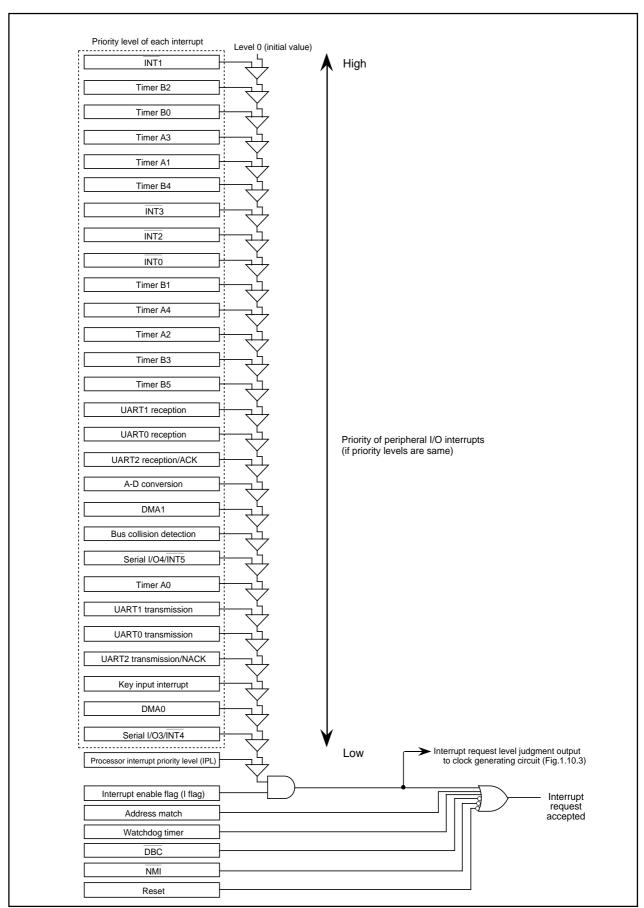


Figure 1.11.9. Maskable interrupts priorities (peripheral I/O interrupts)



INT Interrupt

INTO to INT5 are triggered by the edges of external inputs. The edge polarity is selected using the polarity select bit.

Of interrupt control registers, 004816 is used both as serial I/O4 and external interrupt INT5 input control register, and 004916 is used both as serial I/O3 and as external interrupt INT4 input control register. Use the interrupt request cause select bits - bits 6 and 7 of the interrupt request cause select register (035F16) - to specify which interrupt request cause to select. After having set an interrupt request cause, be sure to clear the corresponding interrupt request bit before enabling an interrupt.

Either of the interrupt control registers - 004816, 004916 - has the polarity-switching bit. Be sure to set this bit to "0" to select an serial I/O as the interrupt request cause.

As for external interrupt input, an interrupt can be generated both at the rising edge and at the falling edge by setting "1" in the INTi interrupt polarity switching bit of the interrupt request cause select register (035F₁₆). To select both edges, set the polarity switching bit of the corresponding interrupt control register to 'falling edge' ("0").

Figure 1.11.10 shows the Interrupt request cause select register.

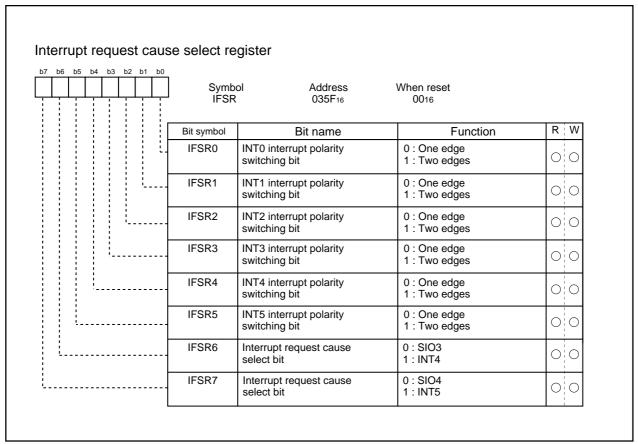


Figure 1.11.10. Interrupt request cause select register

NMI Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when the input to the P85/ $\overline{\text{NMI}}$ pin changes from "H" to "L". The $\overline{\text{NMI}}$ interrupt is a non-maskable external interrupt. The pin level can be checked in the port P85 register (bit 5 at address 03F016).

This pin cannot be used as a normal port input.

Key Input Interrupt

If the direction register of any of P104 to P107 is set for input and a falling edge is input to that port, a key input interrupt is generated. A key input interrupt can also be used as a key-on wakeup function for cancelling the wait mode or stop mode. However, if you intend to use the key input interrupt, do not use P104 to P107 as A-D input ports. Figure 1.11.11 shows the block diagram of the key input interrupt. Note that if an "L" level is input to any pin that has not been disabled for input, inputs to the other pins are not detected as an interrupt.

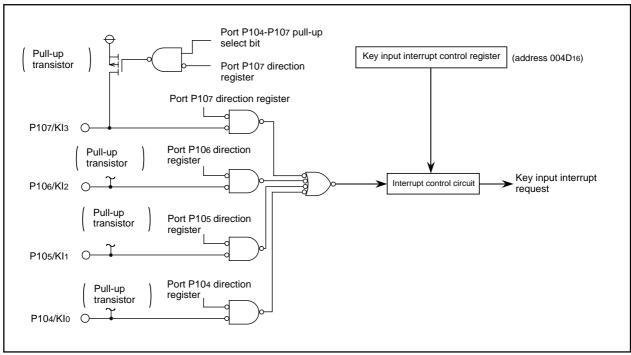


Figure 1.11.11. Block diagram of key input interrupt

Address Match Interrupt

An address match interrupt is generated when the address match interrupt address register contents match the program counter value. Two address match interrupts can be set, each of which can be enabled and disabled by an address match interrupt enable bit. Address match interrupts are not affected by the interrupt enable flag (I flag) and processor interrupt priority level (IPL). For an address match interrupt, the value of the program counter (PC) that is saved to the stack area varies depending on the instruction being executed. Note that when using the external data bus in width of 8 bits, the address match interrupt cannot be used for external area.

Figure 1.11.12 shows the address match interrupt-related registers.

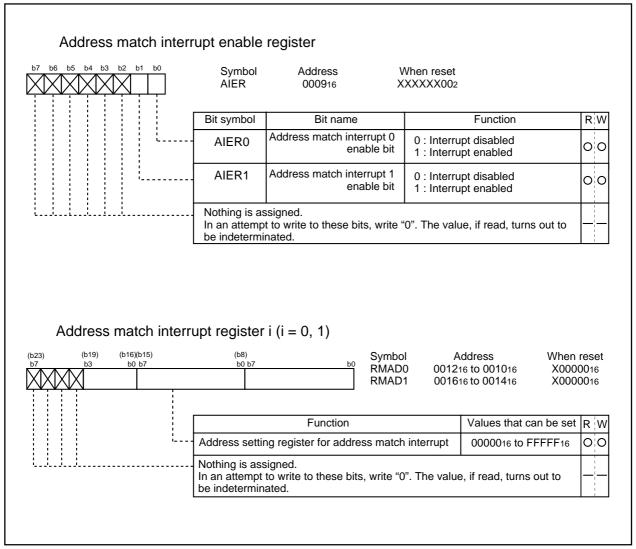


Figure 1.11.12. Address match interrupt-related registers

Precautions for Interrupts

(1) Reading address 0000016

• When maskable interrupt is occurred, CPU reads the interrupt information (the interrupt number and interrupt request level) in the interrupt sequence.

The interrupt request bit of the certain interrupt written in address 0000016 will then be set to "0". Even if the address 0000016 is read out by software, "0" is set to the enabled highest priority interrupt source request bit. Therefore interrupt can be canceled and unexpected interrupt can occur. Do not read address 0000016 by software.

(2) Setting the stack pointer

• The value of the stack pointer immediately after reset is initialized to 000016. Accepting an interrupt before setting a value in the stack pointer may become a factor of runaway. Be sure to set a value in the stack pointer before accepting an interrupt. When using the NMI interrupt, initialize the stack pointer at the beginning of a program. Concerning the first instruction immediately after reset, generating any interrupts including the NMI interrupt is prohibited.

(3) The NMI interrupt

- •The NMI interrupt can not be disabled. Be sure to connect NMI pin to Vcc via a pull-up resistor if unused. Be sure to work on it.
- The NMI pin also serves as P85, which is exclusively input. Reading the contents of the P8 register allows reading the pin value. Use the reading of this pin only for establishing the pin level at the time when the NMI interrupt is input.
- Do not reset the CPU with the input to the NMI pin being in the "L" state.
- Do not attempt to go into stop mode with the input to the \overline{NMI} pin being in the "L" state. With the input to the \overline{NMI} being in the "L" state, the CM10 is fixed to "0", so attempting to go into stop mode is turned down.
- Do not attempt to go into wait mode with the input to the \overline{NMI} pin being in the "L" state. With the input to the \overline{NMI} pin being in the "L" state, the CPU stops but the oscillation does not stop, so no power is saved. In this instance, the CPU is returned to the normal state by a later interrupt.
- Signals input to the NMI pin require an "L" level of 1 clock or more, from the operation clock of the CPU.

(4) External interrupt

- Either an "L" level or an "H" level of at least 250 ns width is necessary for the signal input to pins INTo through INT5 regardless of the CPU operation clock.
- When the polarity of the INTo to INTo pins is changed, the interrupt request bit is sometimes set to "1". After changing the polarity, set the interrupt request bit to "0". Figure 1.11.13 shows the procedure for changing the INT interrupt generate factor.



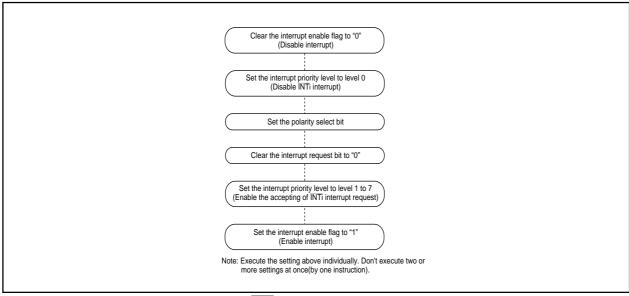


Figure 1.11.13. Switching condition of INT interrupt request

(5) Rewrite the interrupt control register

• To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. If there is possibility of the interrupt request occur, rewrite the interrupt control register after the interrupt is disabled. The program examples are described as follow:

```
Example 1:
   INT_SWITCH1:
       FCLR
                              ; Disable interrupts.
       AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
       NOP
                              ; Four NOP instructions are required when using HOLD function.
       NOP
       FSET
                              ; Enable interrupts.
Example 2:
   INT_SWITCH2:
       FCLR
                              ; Disable interrupts.
       AND.B #00h, 0055h ; Clear TA0IC int. priority level and int. request bit.
       MOV.W MEM, R0
                              ; Dummy read.
       FSET
                              ; Enable interrupts.
Example 3:
   INT_SWITCH3:
       PUSHC FLG
                              ; Push Flag register onto stack
       FCI R
                              ; Disable interrupts.
       AND.B
                #00h, 0055h
                             ; Clear TAOIC int. priority level and int. request bit.
                              ; Enable interrupts.
       POPC
                FLG
```

The reason why two NOP instructions (four when using the HOLD function) or dummy read are inserted before FSET I in Examples 1 and 2 is to prevent the interrupt enable flag I from being set before the interrupt control register is rewritten due to effects of the instruction queue.

When a instruction to rewrite the interrupt control register is executed but the interrupt is disabled, the
interrupt request bit is not set sometimes even if the interrupt request for that register has been generated. This will depend on the instruction. If this creates problems, use the below instructions to change
the register.

Instructions: AND, OR, BCLR, BSET



Watchdog Timer

The watchdog timer has the function of detecting when the program is out of control. Therefore, we recommend using the watchdog timer to improve reliability of a system. The watchdog timer is a 15-bit counter which down-counts the clock derived by dividing the BCLK using the prescaler. A watchdog timer interrupt is generated when an underflow occurs in the watchdog timer. When XIN is selected for the BCLK, bit 7 of the watchdog timer control register (address 000F16) selects the prescaler division ratio (by 16 or by 128). When XCIN is selected as the BCLK, the prescaler is set for division by 2 regardless of bit 7 of the watchdog timer control register (address 000F16). Thus the watchdog timer's period can be calculated as given below. The watchdog timer's period is, however, subject to an error due to the prescaler.

With XIN chosen for BCLK

Watchdog timer period =

prescaler dividing ratio (16 or 128) X watchdog timer count (32768)

BCLK

With XCIN chosen for BCLK

Watchdog timer period =

prescaler dividing ratio (2) X watchdog timer count (32768)

BCLK

For example, suppose that BCLK runs at 16 MHz and that 16 has been chosen for the dividing ratio of the prescaler, then the watchdog timer's period becomes approximately 32.8 ms.

The watchdog timer is initialized by writing to the watchdog timer start register (address 000E16) and when a watchdog timer interrupt request is generated. The prescaler is initialized only when the microcomputer is reset. After a reset is cancelled, the watchdog timer and prescaler are both stopped. The count is started by writing to the watchdog timer start register (address 000E16). In stop mode, wait mode and hold state, the watchdog timer and prescaler are stopped. Counting is resumed from the held value when the modes or state are released.

Figure 1.12.1 shows the block diagram of the watchdog timer. Figure 1.12.2 shows the watchdog timer-related registers.

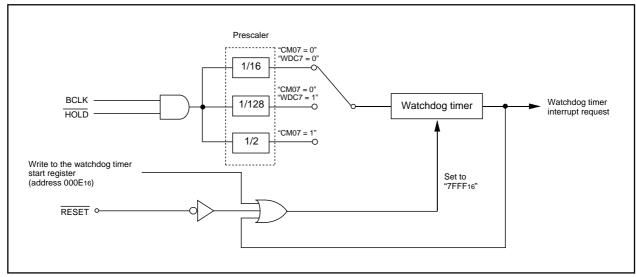


Figure 1.12.1. Block diagram of watchdog timer



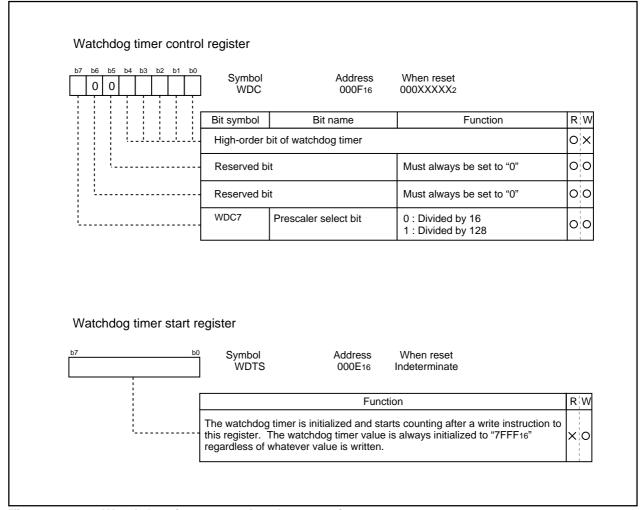


Figure 1.12.2. Watchdog timer control and start registers

DMAC

This microcomputer has two DMAC (direct memory access controller) channels that allow data to be sent to memory without using the CPU. DMAC shares the same data bus with the CPU. The DMAC is given a higher right of using the bus than the CPU, which leads to working the cycle stealing method. On this account, the operation from the occurrence of DMA transfer request signal to the completion of 1-word (16-bit) or 1-byte (8-bit) data transfer can be performed at high speed. Figure 1.13.1 shows the block diagram of the DMAC. Table 1.13.1 shows the DMAC specifications. Figures 1.13.2 to 1.13.4 show the registers used by the DMAC.

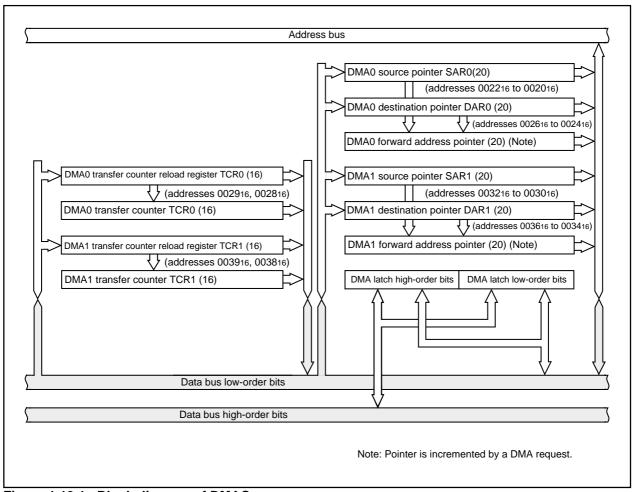


Figure 1.13.1. Block diagram of DMAC

Either a write signal to the software DMA request bit or an interrupt request signal is used as a DMA transfer request signal. But the DMA transfer is affected neither by the interrupt enable flag (I flag) nor by the interrupt priority level. The DMA transfer doesn't affect any interrupts either.

If the DMAC is active (the DMA enable bit is set to 1), data transfer starts every time a DMA transfer request signal occurs. If the cycle of the occurrences of DMA transfer request signals is higher than the DMA transfer cycle, there can be instances in which the number of transfer requests doesn't agree with the number of transfers. For details, see the description of the DMA request bit.



Table 1.13.1. DMAC specifications

Item	Specification
No. of channels	2 (cycle steal method)
Transfer memory space	• From any address in the 1M bytes space to a fixed address
	• From a fixed address to any address in the 1M bytes space
	• From a fixed address to a fixed address
	(Note that DMA-related registers [002016 to 003F16] cannot be accessed)
Maximum No. of bytes transferred	128K bytes (with 16-bit transfers) or 64K bytes (with 8-bit transfers)
DMA request factors (Note)	Falling edge of INT0 or INT1 or both edge
	Timer A0 to timer A4 interrupt requests
	Timer B0 to timer B5 interrupt requests
	UART0 transfer and reception interrupt requests
	UART1 transfer and reception interrupt requests
	UART2 transfer and reception interrupt requests
	Serial I/O3, 4 interrpt requests
	A-D conversion interrupt requests
	Software triggers
Channel priority	DMA0 takes precedence if DMA0 and DMA1 requests are generated simultaneously
Transfer unit	8 bits or 16 bits
Transfer address direction	forward/fixed (forward direction cannot be specified for both source and
	destination simultaneously)
Transfer mode	Single transfer mode
	After the transfer counter underflows, the DMA enable bit turns to
	"0", and the DMAC turns inactive
	Repeat transfer mode
	After the transfer counter underflows, the value of the transfer counter
	reload register is reloaded to the transfer counter.
	The DMAC remains active unless a "0" is written to the DMA enable bit.
DMA interrupt request generation timing	When an underflow occurs in the transfer counter
Active	When the DMA enable bit is set to "1", the DMAC is active.
	When the DMAC is active, data transfer starts every time a DMA
	transfer request signal occurs.
Inactive	When the DMA enable bit is set to "0", the DMAC is inactive.
	After the transfer counter underflows in single transfer mode
Reload timing for forward ad	· ·
dress pointer and transfer	value of one of source pointer and destination pointer - the one specified for the
counter	forward direction - is reloaded to the forward direction address pointer, and the value
	of the transfer counter reload register is reloaded to the transfer counter.
Writing to register	Registers specified for forward direction transfer are always write enabled.
	Registers specified for fixed address transfer are write-enabled when
	the DMA enable bit is "0".
Reading the register	Can be read at any time.
·	However, when the DMA enable bit is "1", reading the register set up as the
	forward register is the same as reading the value of the forward address pointer.

Note: DMA transfer is not effective to any interrupt. DMA transfer is affected neither by the interrupt enable flag (I flag) nor by the interrupt priority level.



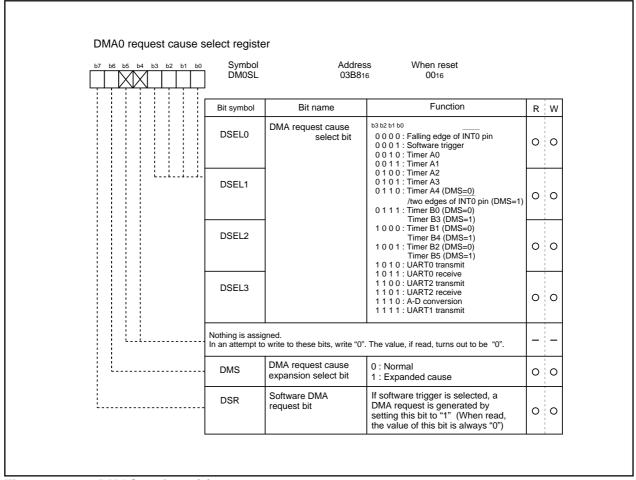


Figure 1.13.2. DMAC register (1)

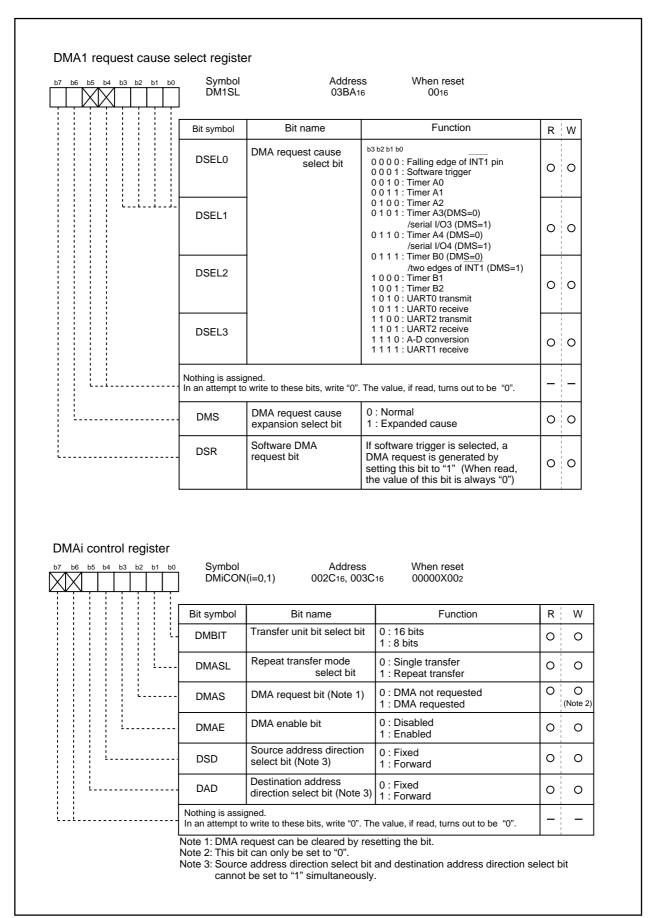


Figure 1.13.3. DMAC register (2)



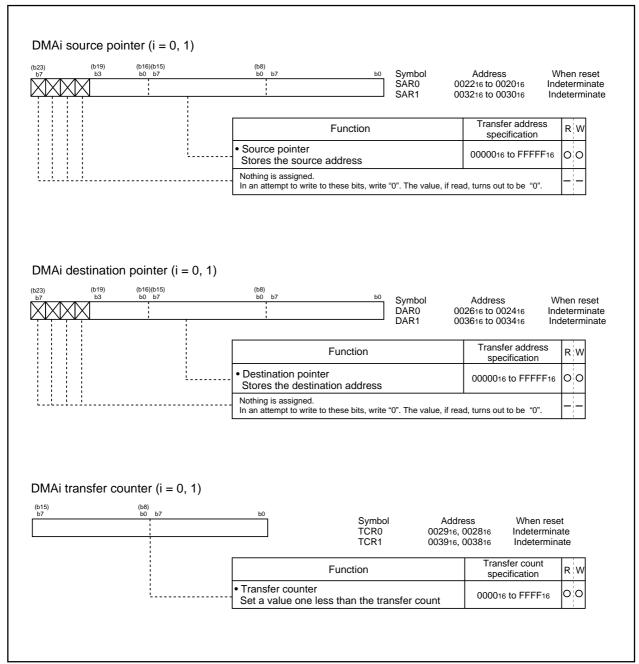


Figure 1.13.4. DMAC register (3)

(1) Transfer cycle

The transfer cycle consists of the bus cycle in which data is read from memory or from the SFR area (source read) and the bus cycle in which the data is written to memory or to the SFR area (destination write). The number of read and write bus cycles depends on the source and destination addresses. In memory expansion mode and microprocessor mode, the number of read and write bus cycles also depends on the level of the BYTE pin. Also, the bus cycle itself is longer when software waits are inserted.

(a) Effect of source and destination addresses

When 16-bit data is transferred on a 16-bit data bus, and the source and destination both start at odd addresses, there are one more source read cycle and destination write cycle than when the source and destination both start at even addresses.

(b) Effect of BYTE pin level

When transferring 16-bit data over an 8-bit data bus (BYTE pin = "H") in memory expansion mode and microprocessor mode, the 16 bits of data are sent in two 8-bit blocks. Therefore, two bus cycles are required for reading the data and two are required for writing the data. Also, in contrast to when the CPU accesses internal memory, when the DMAC accesses internal memory (internal ROM, internal RAM, and SFR), these areas are accessed using the data size selected by the BYTE pin.

(c) Effect of software wait

When the SFR area or a memory area with a software wait is accessed, the number of cycles is increased for the wait by 1 bus cycle. The length of the cycle is determined by BCLK.

Figure 1.13.5 shows the example of the transfer cycles for a source read. For convenience, the destination write cycle is shown as one cycle and the source read cycles for the different conditions are shown. In reality, the destination write cycle is subject to the same conditions as the source read cycle, with the transfer cycle changing accordingly. When calculating the transfer cycle, remember to apply the respective conditions to both the destination write cycle and the source read cycle. For example (2) in Figure 1.13.5, if data is being transferred in 16-bit units on an 8-bit bus, two bus cycles are required for both the source read cycle and the destination write cycle.



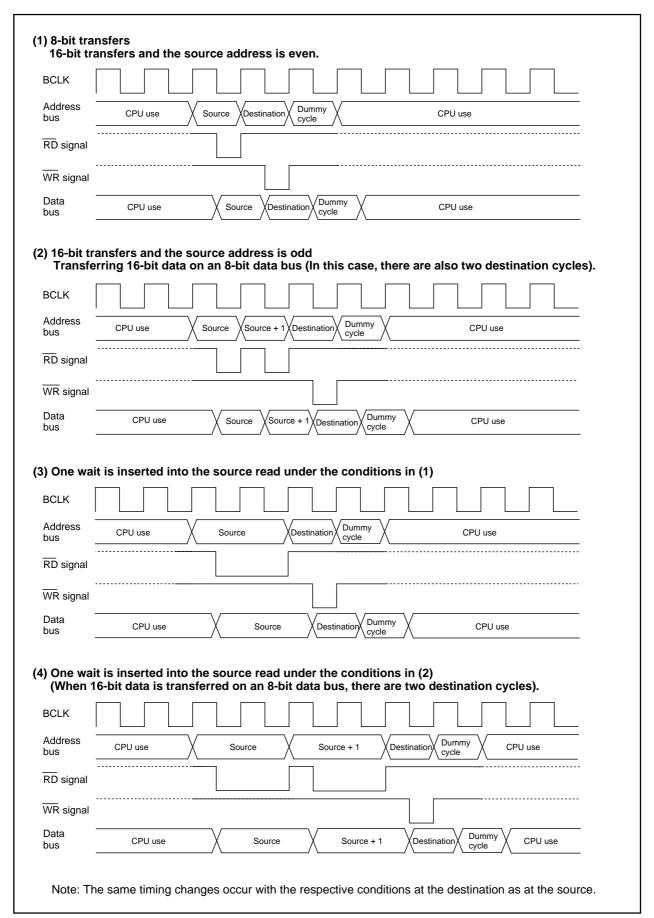


Figure 1.13.5. Example of the transfer cycles for a source read



(2) DMAC transfer cycles

Any combination of even or odd transfer read and write addresses is possible. Table 1.13.2 shows the number of DMAC transfer cycles.

The number of DMAC transfer cycles can be calculated as follows:

No. of transfer cycles per transfer unit = No. of read cycles x j + No. of write cycles x k

Table 1.13.2. No. of DMAC transfer cycles

			Single-ch	nip mode	Memory expa	ansion mode
Transfer unit	Bus width	Access address			Microproce	ssor mode
			No. of read	No. of write	No. of read	No. of write
			cycles	cycles	cycles	cycles
	16-bit	Even	1	1	1	1
8-bit transfers	(BYTE= "L")	Odd	1	1	1	1
(DMBIT= "1")	8-bit	Even	_	_	1	1
	(BYTE = "H")	Odd	_	_	1	1
	16-bit	Even	1	1	1	1
16-bit transfers	(BYTE = "L")	Odd	2	2	2	2
(DMBIT= "0")	8-bit	Even	_	_	2	2
	(BYTE = "H")	Odd	_	_	2	2

Coefficient j, k

Internal memory			Ex	ternal memory	
Internal ROM/RAM	Internal ROM/RAM	SFR area	Separate bus	Separate bus	Multiplex
No wait	With wait		No wait	With wait	bus
1	2	2	1	2	3



DMA enable bit

Setting the DMA enable bit to "1" makes the DMAC active. The DMAC carries out the following operations at the time data transfer starts immediately after DMAC is turned active.

- (1) Reloads the value of one of the source pointer and the destination pointer the one specified for the forward direction to the forward direction address pointer.
- (2) Reloads the value of the transfer counter reload register to the transfer counter.

Thus overwriting "1" to the DMA enable bit with the DMAC being active carries out the operations given above, so the DMAC operates again from the initial state at the instant "1" is overwritten to the DMA enable bit.

DMA request bit

The DMAC can generate a DMA transfer request signal triggered by a factor chosen in advance out of DMA request factors for each channel.

DMA request factors include the following.

- * Factors effected by using the interrupt request signals from the built-in peripheral functions and software DMA factors (internal factors) effected by a program.
- * External factors effected by utilizing the input from external interrupt signals.

For the selection of DMA request factors, see the descriptions of the DMAi factor selection register.

The DMA request bit turns to "1" if the DMA transfer request signal occurs regardless of the DMAC's state (regardless of whether the DMA enable bit is set to "1" or "0"). It turns to "0" immediately before data transfer starts.

In addition, it can be set to "0" by use of a program, but cannot be set to "1".

There can be instances in which a change in DMA request factor selection bit causes the DMA request bit to turn to "1". So be sure to set the DMA request bit to "0" after the DMA request factor selection bit is changed.

The DMA request bit turns to "1" if a DMA transfer request signal occurs, and turns to "0" immediately before data transfer starts. If the DMAC is active, data transfer starts immediately, so the value of the DMA request bit, if read by use of a program, turns out to be "0" in most cases. To examine whether the DMAC is active, read the DMA enable bit.

Here follows the timing of changes in the DMA request bit.

(1) Internal factors

Except the DMA request factors triggered by software, the timing for the DMA request bit to turn to "1" due to an internal factor is the same as the timing for the interrupt request bit of the interrupt control register to turn to "1" due to several factors.

Turning the DMA request bit to "0" due to an internal factor is timed to be effected immediately before the transfer starts.

(2) External factors

An external factor is a factor caused to occur by the leading edge of input from the INTi pin (i depends on which DMAC channel is used).

Selecting the INTi pins as external factors using the DMA request factor selection bit causes input from these pins to become the DMA transfer request signals.

The timing for the DMA request bit to turn to "1" when an external factor is selected synchronizes with the signal's edge applicable to the function specified by the DMA request factor selection bit (synchronizes with the trailing edge of the input signal to each INTi pin, for example).

With an external factor selected, the DMA request bit is timed to turn to "0" immediately before data transfer starts similarly to the state in which an internal factor is selected.



(3) The priorities of channels and DMA transfer timing

If a DMA transfer request signal falls on a single sampling cycle (a sampling cycle means one period from the leading edge to the trailing edge of BCLK), the DMA request bits of applicable channels concurrently turn to "1". If the channels are active at that moment, DMA0 is given a high priority to start data transfer. When DMA0 finishes data transfer, it gives the bus right to the CPU. When the CPU finishes single bus access, then DMA1 starts data transfer and gives the bus right to the CPU.

An example in which DMA transfer is carried out in minimum cycles at the time when DMA transfer request signals due to external factors concurrently occur.

Figure 1.13.6 An example of DMA transfer effected by external factors.

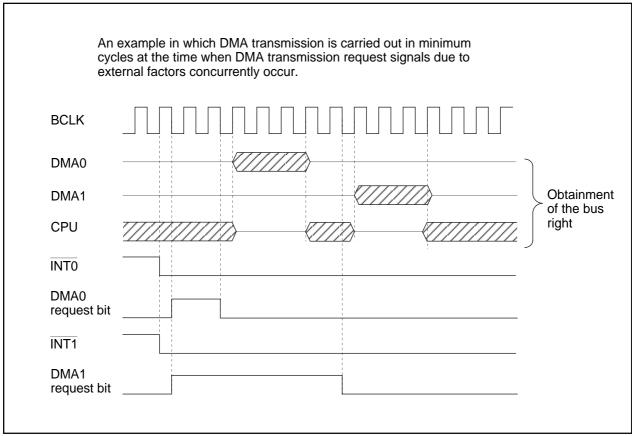


Figure 1.13.6. An example of DMA transfer effected by external factors

Timer

There are eleven 16-bit timers. These timers can be classified by function into timers A (five) and timers B (six). All these timers function independently. Figures 1.14.1 and 1.14.2 show the block diagram of timers.

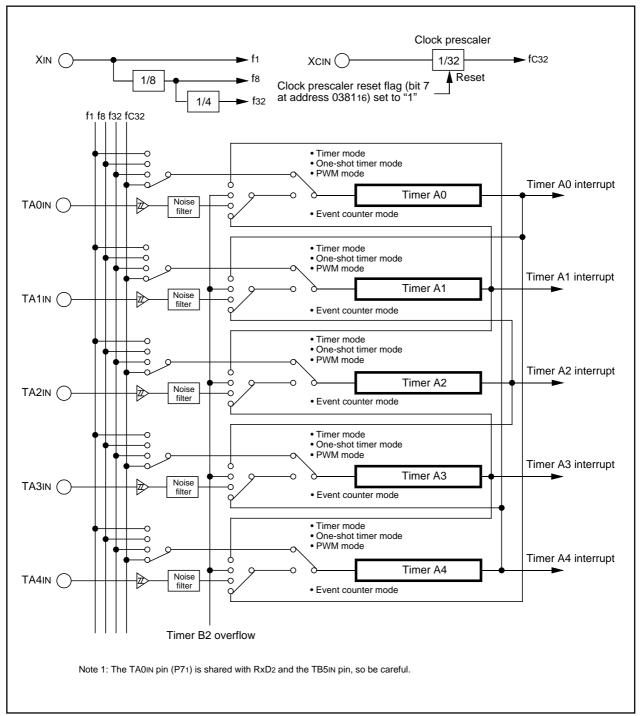


Figure 1.14.1. Timer A block diagram

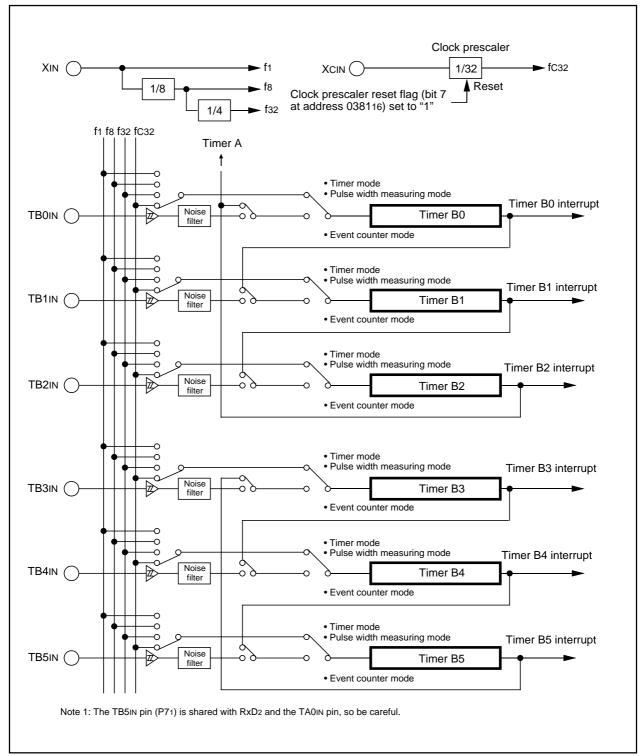


Figure 1.14.2. Timer B block diagram

Timer A

Figure 1.14.3 shows the block diagram of timer A. Figures 1.14.4 to 1.14.6 show the timer A-related registers.

Except in event counter mode, timers A0 through A4 all have the same function. Use the timer Ai mode register (i = 0 to 4) bits 0 and 1 to choose the desired mode.

Timer A has the four operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts pulses from an external source or a timer over flow.
- One-shot timer mode: The timer stops counting when the count reaches "000016".
- Pulse width modulation (PWM) mode: The timer outputs pulses of a given width.

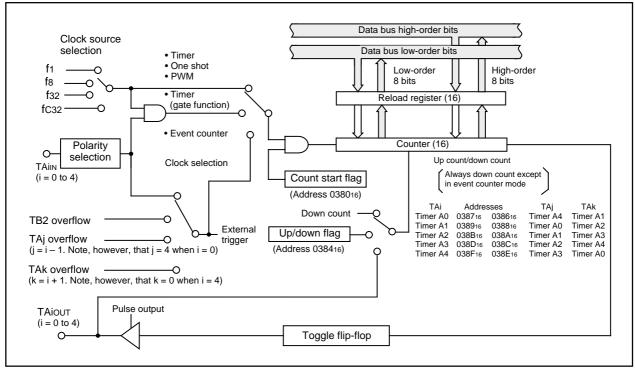


Figure 1.14.3. Block diagram of timer A

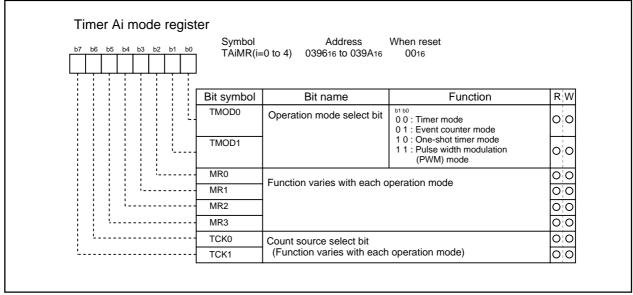


Figure 1.14.4. Timer A-related registers (1)



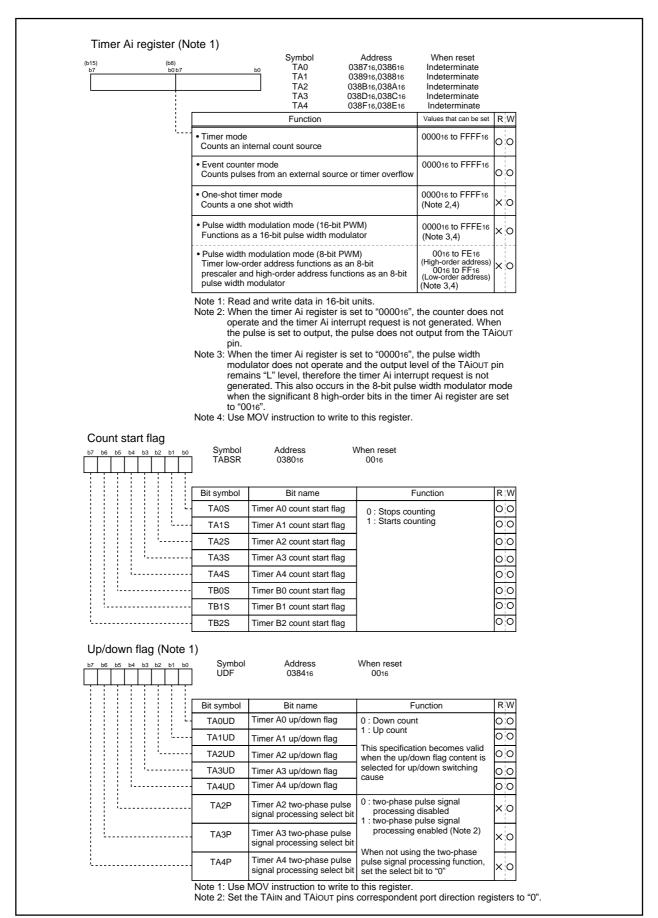


Figure 1.14.5. Timer A-related registers (2)



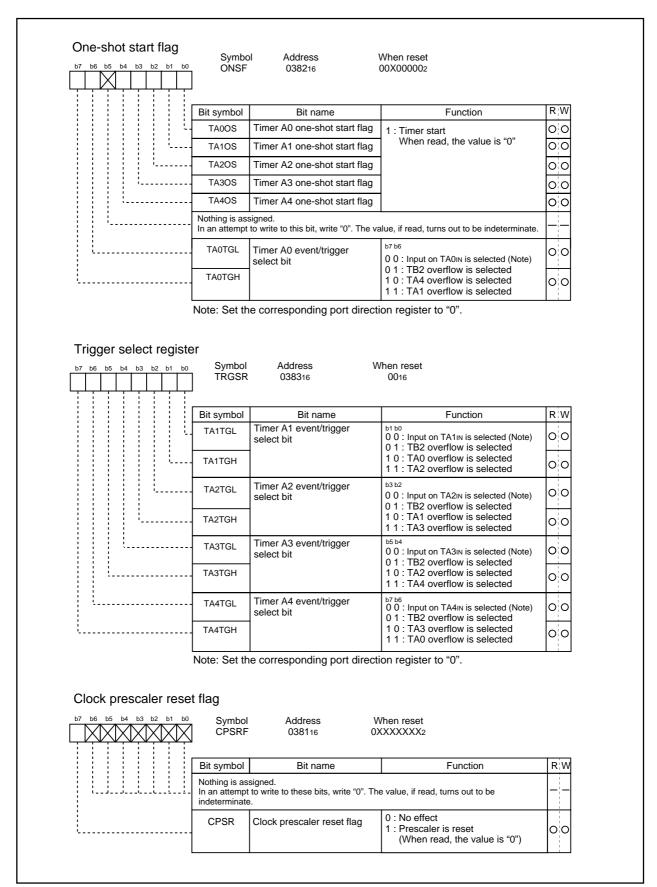


Figure 1.14.6. Timer A-related registers (3)

(1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.14.1.) Figure 1.14.7 shows the timer Ai mode register in timer mode.

Table 1.14.1. Specifications of timer mode

Item	Specification	
Count source	f1, f8, f32, fC32	
Count operation	Down count	
	When the timer underflows, it reloads the reload register contents before continuing counting	
Divide ratio	1/(n+1) n : Set value	
Count start condition	Count start flag is set (= 1)	
Count stop condition	Count start flag is reset (= 0)	
Interrupt request generation timing	When the timer underflows	
TAilN pin function	Programmable I/O port or gate input	
TAiout pin function	Programmable I/O port or pulse output	
Read from timer	Count value can be read out by reading timer Ai register	
Write to timer	When counting stopped	
	When a value is written to timer Ai register, it is written to both reload register and counter	
	When counting in progress	
	When a value is written to timer Ai register, it is written to only reload register	
	(Transferred to counter at next reload time)	
Select function	Gate function	
	Counting can be started and stopped by the TAilN pin's input signal	
	Pulse output function	
	Each time the timer underflows, the TAio∪T pin's polarity is reversed	

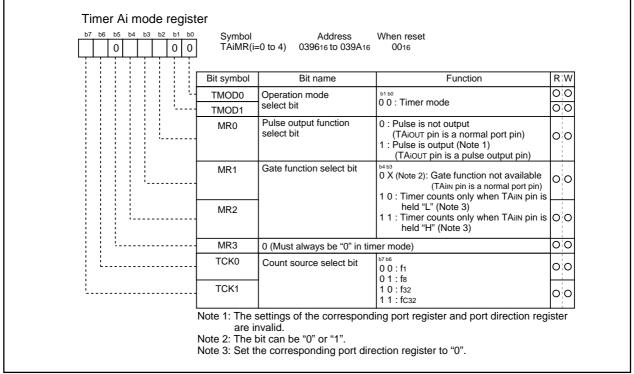


Figure 1.14.7. Timer Ai mode register in timer mode



(2) Event counter mode

In this mode, the timer counts an external signal or an internal timer's overflow. Timers A0 and A1 can count a single-phase external signal. Timers A2, A3, and A4 can count a single-phase and a two-phase external signal. Table 1.14.2 lists timer specifications when counting a single-phase external signal. Figure 1.14.8 shows the timer Ai mode register in event counter mode.

Table 1.14.3 lists timer specifications when counting a two-phase external signal. Figure 1.14.9 shows the timer Ai mode register in event counter mode.

Table 1.14.2. Timer specifications in event counter mode (when not processing two-phase pulse signal)

Item	Specification	
Count source	External signals input to TAilN pin (effective edge can be selected by software)	
	TB2 overflow, TAj overflow	
Count operation	Up count or down count can be selected by external signal or software	
	When the timer overflows or underflows, it reloads the reload register con	
	tents before continuing counting (Note)	
Divide ratio	1/ (FFFF16 - n + 1) for up count	
	1/ (n + 1) for down count n : Set value	
Count start condition	Count start flag is set (= 1)	
Count stop condition	Count start flag is reset (= 0)	
Interrupt request generation timing	The timer overflows or underflows	
TAilN pin function	Programmable I/O port or count source input	
TAiout pin function	Programmable I/O port, pulse output, or up/down count select input	
Read from timer	Count value can be read out by reading timer Ai register	
Write to timer	When counting stopped	
	When a value is written to timer Ai register, it is written to both reload register and counter	
	When counting in progress	
	When a value is written to timer Ai register, it is written to only reload register	
	(Transferred to counter at next reload time)	
Select function	Free-run count function	
	Even when the timer overflows or underflows, the reload register content is not reloaded to it	
	Pulse output function	
	Each time the timer overflows or underflows, the TAiout pin's polarity is reversed	

Note: This does not apply when the free-run function is selected.

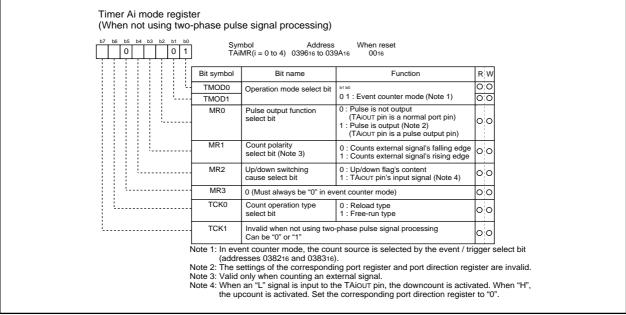


Figure 1.14.8. Timer Ai mode register in event counter mode



Table 1.14.3. Timer specifications in event counter mode (when processing two-phase pulse signal with timers A2, A3, and A4)

Item	Specification		
Count source	Two-phase pulse signals input to TAilN or TAiOUT pin		
Count operation	Up count or down count can be selected by two-phase pulse signal		
Court operation			
	When the timer overflows or underflows, the reload register content is		
Divide retie	reloaded and the timer starts over again (Note 1)		
Divide ratio	1/ (FFFF16 - n + 1) for up count		
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1/ (n + 1) for down count n : Set value		
Count start condition	Count start flag is set (= 1)		
Count stop condition	Count start flag is reset (= 0)		
Interrupt request generation timing	Timer overflows or underflows		
TAilN pin function	Two-phase pulse input (Set the TAilN pin correspondent port direction register to "0".)		
TAiout pin function	Two-phase pulse input (Set the TAiout pin correspondent port direction register to "0".)		
Read from timer	Count value can be read out by reading timer A2, A3, or A4 register		
Write to timer	When counting stopped		
	When a value is written to timer A2, A3, or A4 register, it is written to both		
	reload register and counter		
	When counting in progress		
	When a value is written to timer A2, A3, or A4 register, it is written to only		
	reload register. (Transferred to counter at next reload time.)		
Select function (Note 2)	Normal processing operation (timer A2 and timer A3)		
,	The timer counts up rising edges or counts down falling edges on the TAilN		
	pin when input signal on the TAio∪T pin is "H".		
	First mean input ognition and in the control of the		
	TAIOUT _ L L L		
	TAIN L_ L_ V V		
	(i=2,3) Up Up Down Down Down		
	count count count count count		
	Multiply-by-4 processing operation (timer A3 and timer A4)		
	If the phase relationship is such that the TAilN pin goes "H" when the input		
	signal on the TAiout pin is "H", the timer counts up rising and falling edges		
	on the TAiout and TAil pins. If the phase relationship is such that the		
	TAilN pin goes "L" when the input signal on the TAiOUT pin is "H", the timer		
	counts down rising and falling edges on the TAiout and TAin pins.		
	TAIOUT A VA VA VA		
	Count up all edges Count down all edges		
	TAIN		
	(i=3,4)		
	Count up all edges Count down all edges		

Note 1: This does not apply when the free-run function is selected.

Note 2: Timer A3 alone can be selected. Timer A2 is fixed to normal processing operation, and timer A4 is fixed to multiply-by-4 processing operation.



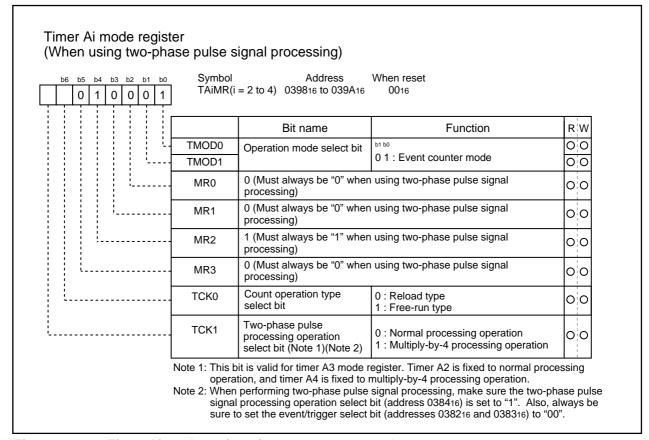


Figure 1.14.9. Timer Ai mode register in event counter mode

(3) One-shot timer mode

In this mode, the timer operates only once. (See Table 1.14.4.) When a trigger occurs, the timer starts up and continues operating for a given period. Figure 1.14.10 shows the timer Ai mode register in one-shot timer mode.

Table 1.14.4. Timer specifications in one-shot timer mode

Item	Specification
Count source	f1, f8, f32, fC32
Count operation	The timer counts down
	When the count reaches 000016, the timer stops counting after reloading a new count
	If a trigger occurs when counting, the timer reloads a new count and restarts counting
Divide ratio	1/n n : Set value
Count start condition	An external trigger is input
	The timer overflows
	• The one-shot start flag is set (= 1)
Count stop condition	A new count is reloaded after the count has reached 000016
	• The count start flag is reset (= 0)
Interrupt request generation timing	The count reaches 000016
TAilN pin function	Programmable I/O port or trigger input
TAiout pin function	Programmable I/O port or pulse output
Read from timer	When timer Ai register is read, it indicates an indeterminate value
Write to timer	When counting stopped
	When a value is written to timer Ai register, it is written to both reload
	register and counter
	When counting in progress
	When a value is written to timer Ai register, it is written to only reload register
	(Transferred to counter at next reload time)

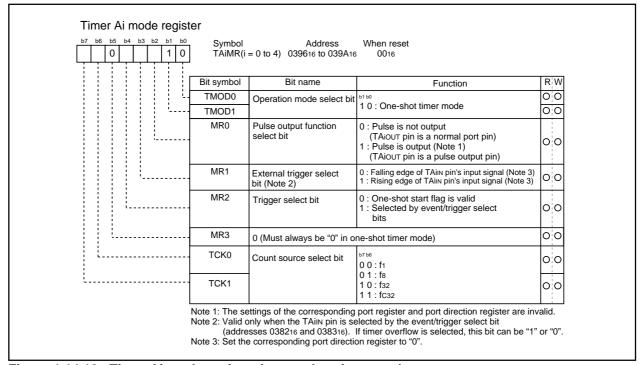


Figure 1.14.10. Timer Ai mode register in one-shot timer mode



(4) Pulse width modulation (PWM) mode

In this mode, the timer outputs pulses of a given width in succession. (See Table 1.14.5.) In this mode, the counter functions as either a 16-bit pulse width modulator or an 8-bit pulse width modulator. Figure 1.14.11 shows the timer Ai mode register in pulse width modulation mode. Figure 1.14.12 shows the example of how a 16-bit pulse width modulator operates. Figure 1.14.13 shows the example of how an 8-bit pulse width modulator operates.

Table 1.14.5. Timer specifications in pulse width modulation mode

Item	Specification	
Count source	f1, f8, f32, fC32	
Count operation	The timer counts down (operating as an 8-bit or a 16-bit pulse width modulator)	
	The timer reloads a new count at a rising edge of PWM pulse and continues counting	
	The timer is not affected by a trigger that occurs when counting	
16-bit PWM	High level width n / fi n : Set value	
	Cycle time (2 ¹⁶ -1) / fi fixed	
8-bit PWM	High level width n×(m+1) / fi n : values set to timer Ai register's high-order address	
	• Cycle time (2 ⁸ -1)×(m+1) / fi m : values set to timer Ai register's low-order address	
Count start condition	External trigger is input	
	The timer overflows	
	The count start flag is set (= 1)	
Count stop condition	The count start flag is reset (= 0)	
Interrupt request generation timing	PWM pulse goes "L"	
TAilN pin function	Programmable I/O port or trigger input	
TAiout pin function	Pulse output	
Read from timer	When timer Ai register is read, it indicates an indeterminate value	
Write to timer	When counting stopped	
	When a value is written to timer Ai register, it is written to both reload	
	register and counter	
	When counting in progress	
	When a value is written to timer Ai register, it is written to only reload register	
	(Transferred to counter at next reload time)	

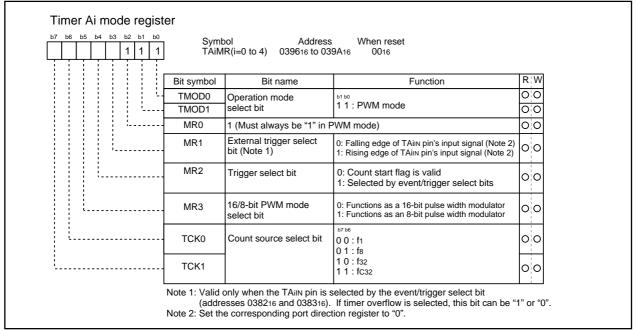


Figure 1.14.11. Timer Ai mode register in pulse width modulation mode



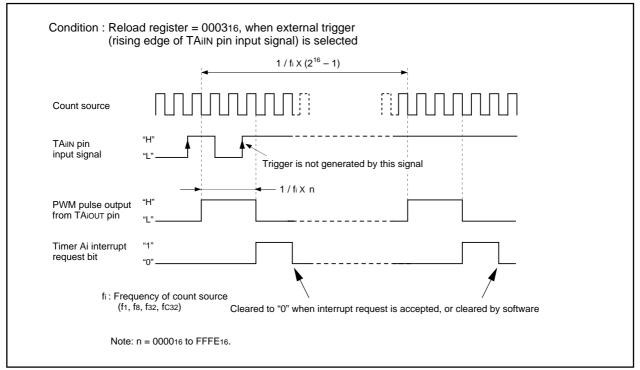


Figure 1.14.12. Example of how a 16-bit pulse width modulator operates

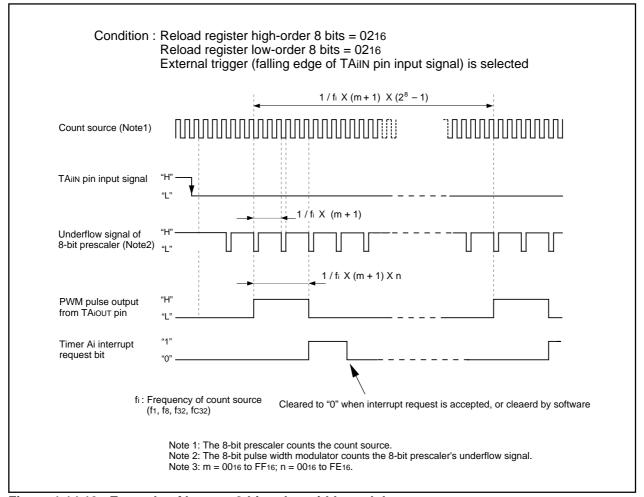


Figure 1.14.13. Example of how an 8-bit pulse width modulator operates



Timer B

Figure 1.14.14 shows the block diagram of timer B. Figures 1.14.15 and 1.14.16 show the timer B-related registers.

Use the timer Bi mode register (i = 0 to 5) bits 0 and 1 to choose the desired mode.

Timer B has three operation modes listed as follows:

- Timer mode: The timer counts an internal count source.
- Event counter mode: The timer counts pulses from an external source or a timer overflow.
- Pulse period/pulse width measuring mode: The timer measures an external signal's pulse period or pulse width.

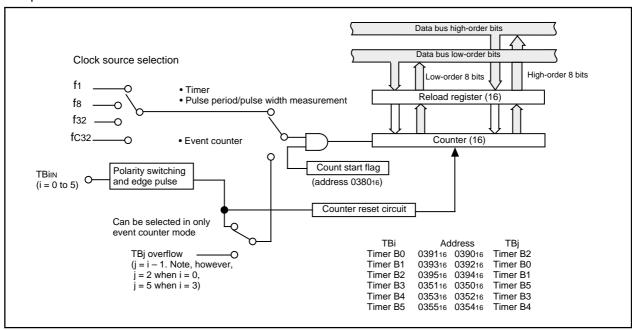


Figure 1.14.14. Block diagram of timer B

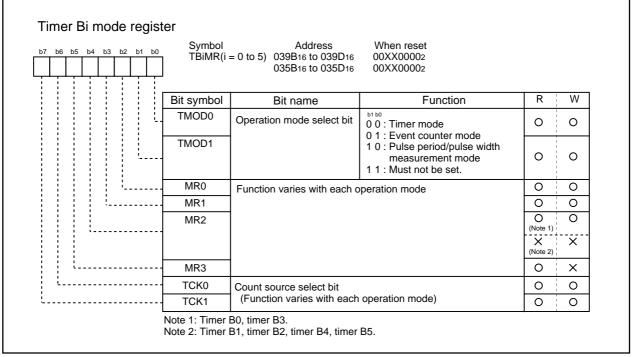


Figure 1.14.15. Timer B-related registers (1)



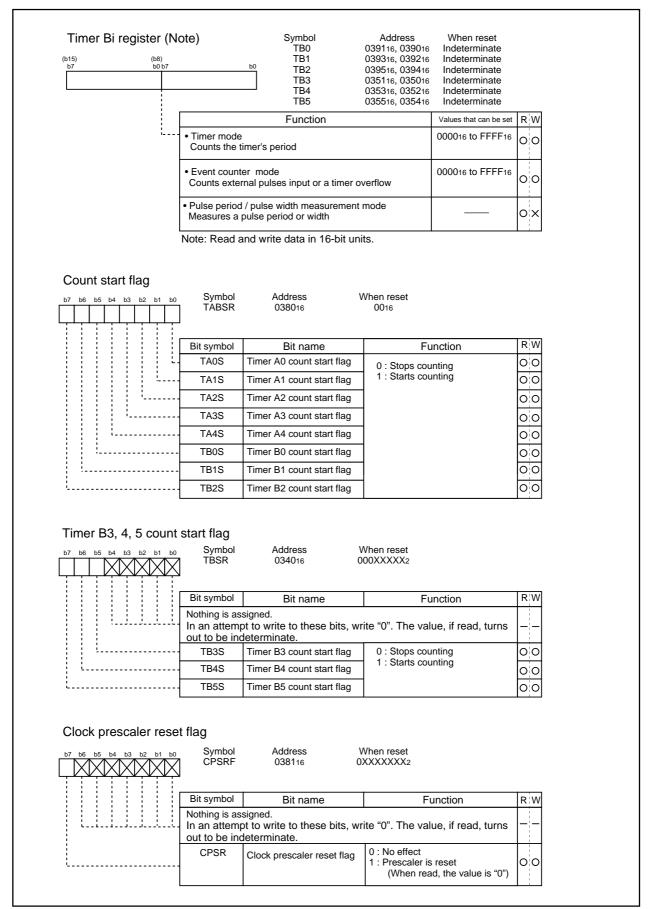


Figure 1.14.16. Timer B-related registers (2)



(1) Timer mode

In this mode, the timer counts an internally generated count source. (See Table 1.14.6.) Figure 1.14.17 shows the timer Bi mode register in timer mode.

Table 1.14.6. Timer specifications in timer mode

Item	Specification	
Count source	f1, f8, f32, fC32	
Count operation	Counts down	
	When the timer underflows, it reloads the reload register contents before	
	continuing counting	
Divide ratio	1/(n+1) n : Set value	
Count start condition	Count start flag is set (= 1)	
Count stop condition	Count start flag is reset (= 0)	
Interrupt request generation timing	The timer underflows	
TBilN pin function	Programmable I/O port	
Read from timer	Count value is read out by reading timer Bi register	
Write to timer	When counting stopped	
	When a value is written to timer Bi register, it is written to both reload register and counter	
	When counting in progress	
	When a value is written to timer Bi register, it is written to only reload register	
	(Transferred to counter at next reload time)	

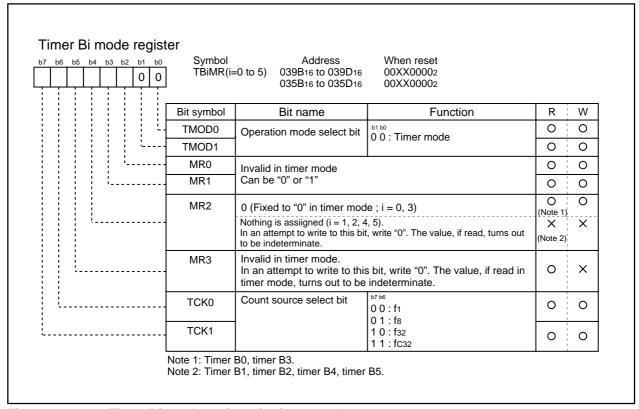


Figure 1.14.17. Timer Bi mode register in timer mode



(2) Event counter mode

In this mode, the timer counts an external signal or an internal timer's overflow. (See Table 1.14.7.) Figure 1.14.18 shows the timer Bi mode register in event counter mode.

Table 1.14.7. Timer specifications in event counter mode

Item	Specification	
Count source	• External signals input to TBilN pin	
	• Effective edge of count source can be a rising edge, a falling edge, or falling	
	and rising edges as selected by software	
Count operation	Counts down	
	When the timer underflows, it reloads the reload register contents before	
	continuing counting	
Divide ratio	1/(n+1) n : Set value	
Count start condition	Count start flag is set (= 1)	
Count stop condition	Count start flag is reset (= 0)	
Interrupt request generation timing	The timer underflows	
TBilN pin function	Count source input	
Read from timer	Count value can be read out by reading timer Bi register	
Write to timer	When counting stopped	
	When a value is written to timer Bi register, it is written to both reload register and counter	
	When counting in progress	
	When a value is written to timer Bi register, it is written to only reload register	
	(Transferred to counter at next reload time)	

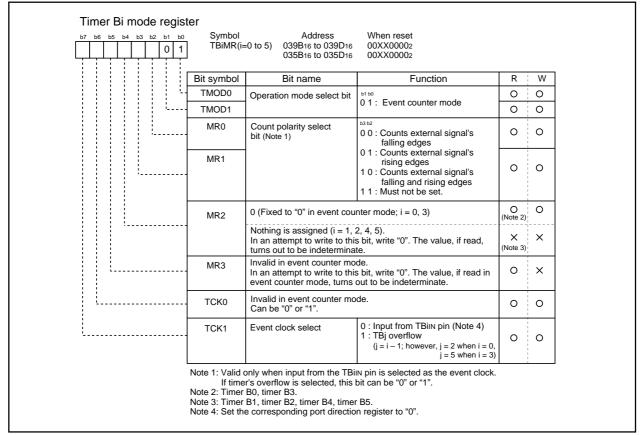


Figure 1.14.18. Timer Bi mode register in event counter mode



(3) Pulse period/pulse width measurement mode

In this mode, the timer measures the pulse period or pulse width of an external signal. (See Table 1.14.8.) Figure 1.14.19 shows the timer Bi mode register in pulse period/pulse width measurement mode. Figure 1.14.20 shows the operation timing when measuring a pulse period. Figure 1.14.21 shows the operation timing when measuring a pulse width.

Table 1.14.8. Timer specifications in pulse period/pulse width measurement mode

Item	Specification	
Count source	f1, f8, f32, fC32	
Count operation	• Up count	
	Counter value "000016" is transferred to reload register at measurement	
	pulse's effective edge and the timer continues counting	
Count start condition	Count start flag is set (= 1)	
Count stop condition	Count start flag is reset (= 0)	
Interrupt request generation timing	When measurement pulse's effective edge is input (Note 1)	
	• When an overflow occurs. (Simultaneously, the timer Bi overflow flag	
	changes to "1". The timer Bi overflow flag changes to "0" when the count	
	start flag is "1" and a value is written to the timer Bi mode register.)	
TBilN pin function	Measurement pulse input	
Read from timer	When timer Bi register is read, it indicates the reload register's content	
	(measurement result) (Note 2)	
Write to timer	Cannot be written to	

Note 1: An interrupt request is not generated when the first effective edge is input after the timer has started counting.

Note 2: The value read out from the timer Bi register is indeterminate until the second effective edge is input after the timer has started counting.

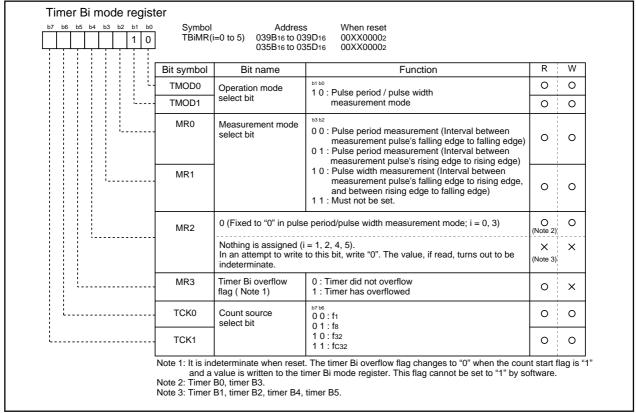


Figure 1.14.19. Timer Bi mode register in pulse period/pulse width measurement mode



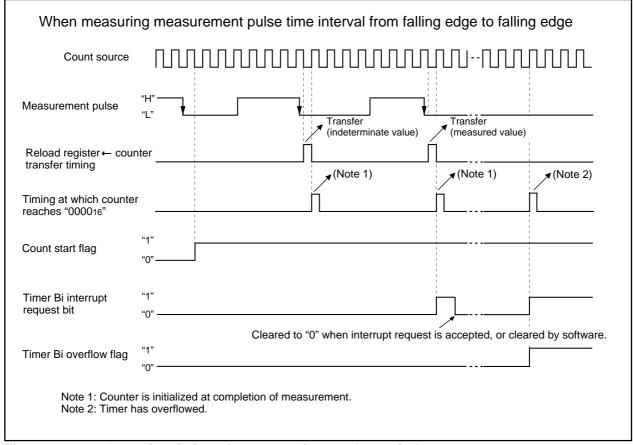


Figure 1.14.20. Operation timing when measuring a pulse period

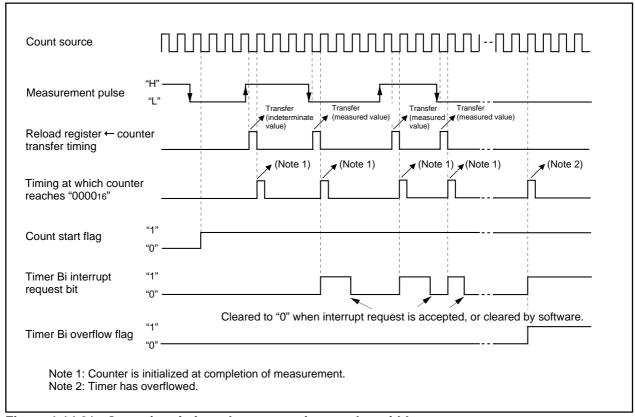


Figure 1.14.21. Operation timing when measuring a pulse width



Timers' functions for three-phase motor control

Use of more than one built-in timer A and timer B provides the means of outputting three-phase motor driving waveforms.

Figures 1.15.1 to 1.15.3 show registers related to timers for three-phase motor control.

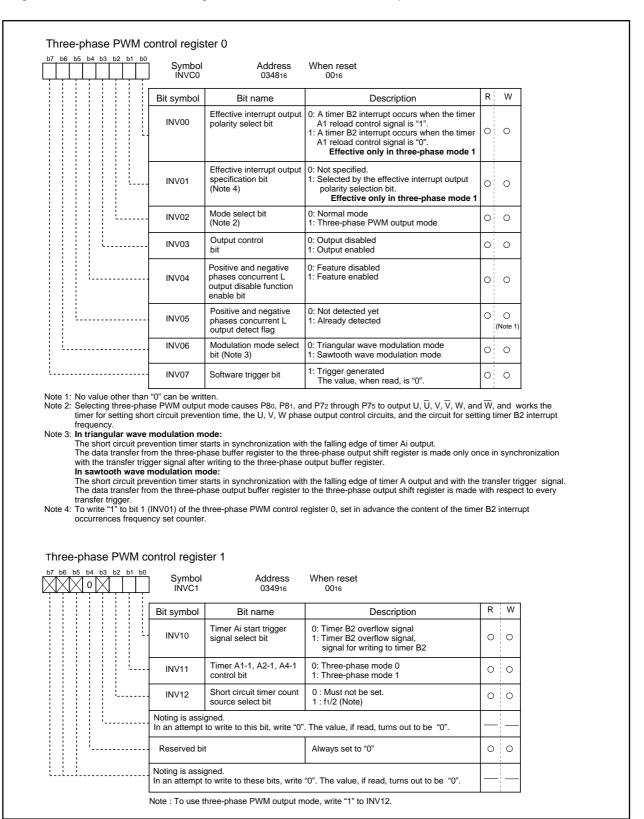


Figure 1.15.1. Registers related to timers for three-phase motor control



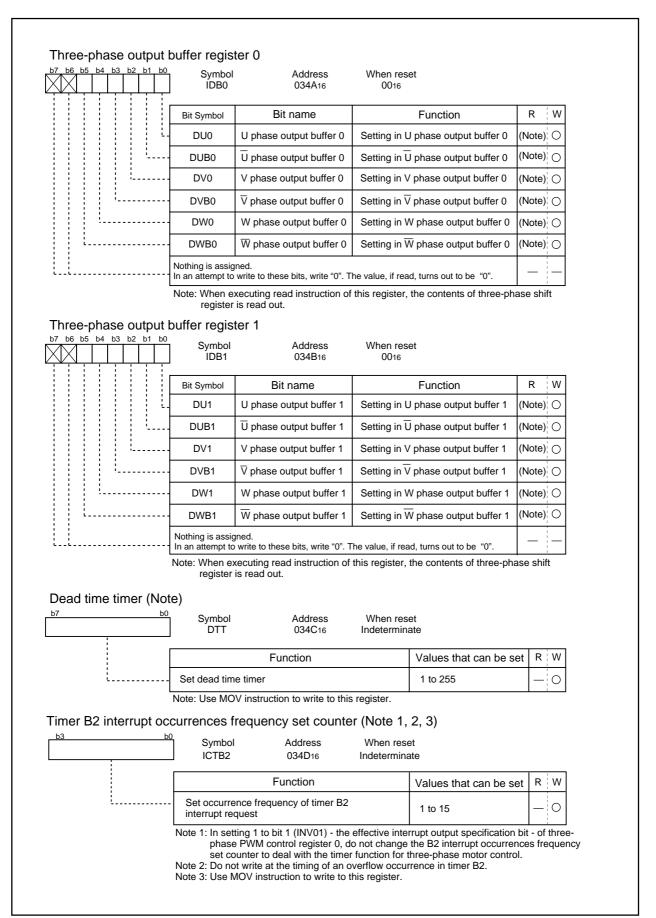


Figure 1.15.2. Registers related to timers for three-phase motor control



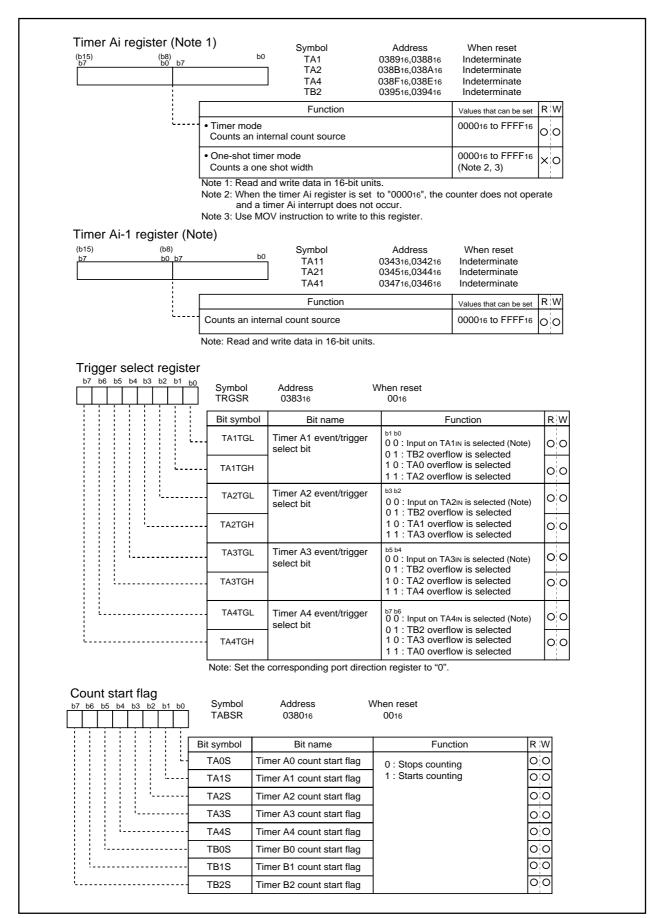


Figure 1.15.3. Registers related to timers for three-phase motor control



Three-phase motor driving waveform output mode (three-phase PWM output mode)

Setting "1" in the mode select bit (bit 2 at 034816) shown in Figure 1.15.1 - causes three-phase PWM output mode that uses four timers A1, A2, A4, and B2 to be selected. As shown in Figure 1.15.4, set timers A1, A2, and A4 in one-shot timer mode, set the trigger in timer B2, and set timer B2 in timer mode using the respective timer mode registers.

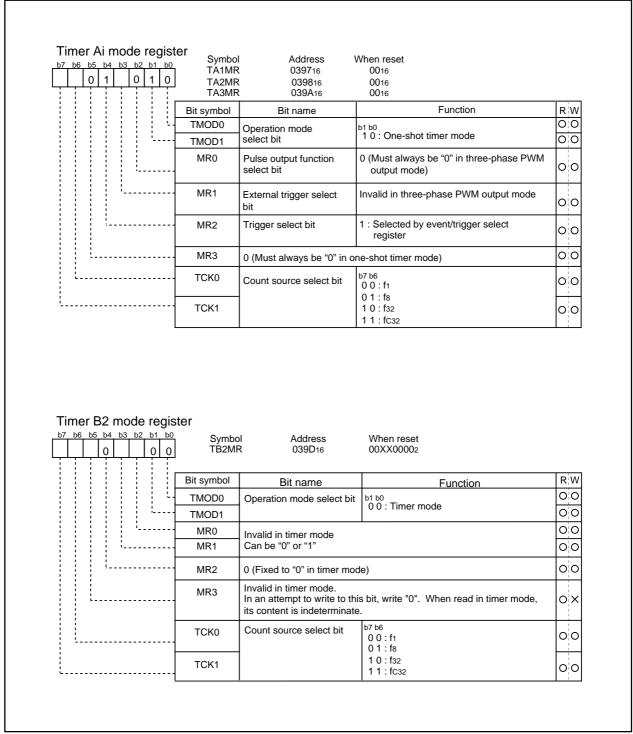


Figure 1.15.4. Timer mode registers in three-phase PWM output mode



Figure 1.15.5 shows the block diagram for three-phase PWM output mode. In three-phase PWM output mode, the positive-phase waveforms (U phase, V phase, and W phase) and negative waveforms (\overline{U} phase, \overline{V} phase, and \overline{W} phase), six waveforms in total, are output from P80, P81, P72, P73, P74, and P75 as active on the "L" level. Of the timers used in this mode, timer A4 controls the U phase and \overline{U} phase, timer A1 controls the V phase and \overline{V} phase, and timer A2 controls the W phase and \overline{W} phase respectively; timer B2 controls the periods of one-shot pulse output from timers A4, A1, and A2.

In outputting a waveform, dead time can be set so as to cause the "L" level of the positive waveform output (U phase, V phase, and W phase) not to lap over the "L" level of the negative waveform output (\overline{U} phase, \overline{V} phase, and \overline{W} phase).

To set short circuit time, use three 8-bit timers sharing the reload register for setting dead time. A value from 1 through 255 can be set as the count of the timer for setting dead time. The timer for setting dead time works as a one-shot timer. If a value is written to the dead time timer (034C16), the value is written to the reload register shared by the three timers for setting dead time.

Any of the timers for setting dead time takes the value of the reload register into its counter, if a start trigger comes from its corresponding timer, and performs a down count in line with the clock source selected by the dead time timer count source select bit (bit 2 at 034916). The timer can receive another trigger again before the workings due to the previous trigger are completed. In this instance, the timer performs a down count from the reload register's content after its transfer, provoked by the trigger, to the timer for setting dead time.

Since the timer for setting dead time works as a one-shot timer, it starts outputting pulses if a trigger comes; it stops outputting pulses as soon as its content becomes 0016, and waits for the next trigger to come.

The positive waveforms (U phase, V phase, and W phase) and the negative waveforms (\overline{U} phase, \overline{V} phase, and \overline{W} phase) in three-phase PWM output mode are output from respective ports by means of setting "1" in the output control bit (bit 3 at 034816). Setting "0" in this bit causes the ports to be the state of set by port direction register. This bit can be set to "0" not only by use of the applicable instruction, but by entering a falling edge in the \overline{NMI} terminal or by resetting. Also, if "1" is set in the positive and negative phases concurrent L output disable function enable bit (bit 4 at 034816) causes one of the pairs of U phase and \overline{U} phase, V phase and \overline{V} phase, and W phase and \overline{W} phase concurrently go to "L", as a result, the port becomes the state of set by port direction register.



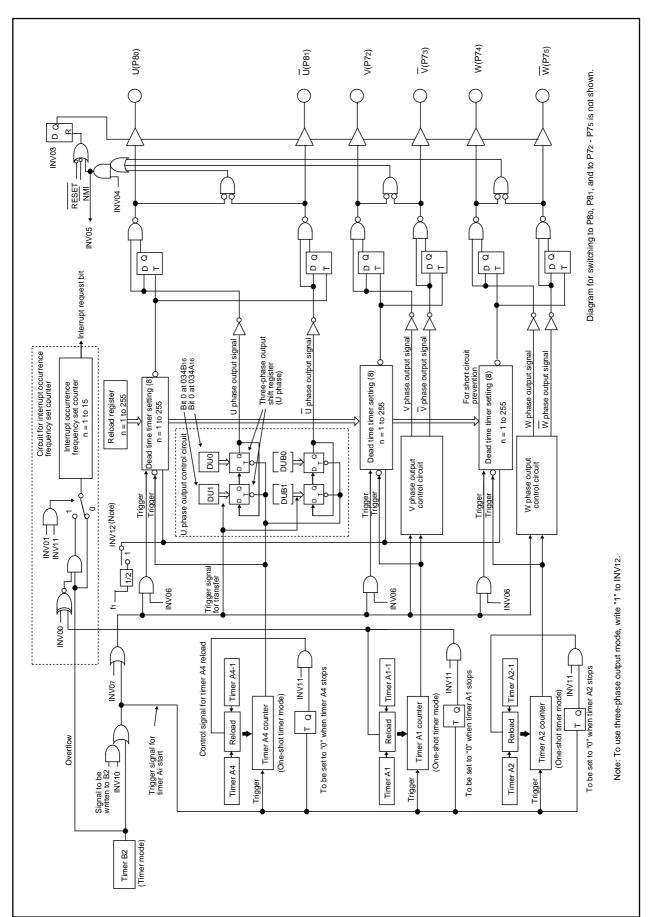


Figure 1.15.5. Block diagram for three-phase PWM output mode



Triangular wave modulation

To generate a PWM waveform of triangular wave modulation, set "0" in the modulation mode select bit (bit 6 at 034816). Also, set "1" in the timers A4-1, A1-1, A2-1 control bit (bit 1 at 034916). In this mode, each of timers A4, A1, and A2 has two timer registers, and alternately reloads the timer register's content to the counter every time timer B2 counter's content becomes 000016. If "0" is set to the effective interrupt output specification bit (bit 1 at 034816), the frequency of interrupt requests that occur every time the timer B2 counter's value becomes 000016 can be set by use of the timer B2 counter (034D16) for setting the frequency of interrupt occurrences. The frequency of occurrences is given by (setting; setting \neq 0). Setting "1" in the effective interrupt output specification bit (bit 1 at 034816) provides the means to choose which value of the timer A1 reload control signal to use, "0" or "1", to cause timer B2's interrupt request to occur. To make this selection, use the effective interrupt output polarity selection bit (bit 0 at 034816). An example of U phase waveform is shown in Figure 1.15.6, and the description of waveform output workings is given below. Set "1" in DU0 (bit 0 at 034A16). And set "0" in DUB0 (bit 1 at 034A16). In addition, set "0" in DU1 (bit 0 at 034B16) and set "1" in DUB1 (bit 1 at 034B16). Also, set "0" in the effective interrupt output specification bit (bit 1 at 034816) to set a value in the timer B2 interrupt occurrence frequency set counter. By this setting, a timer B2 interrupt occurs when the timer B2 counter's content becomes 000016 as many as (setting) times. Furthermore, set "1" in the effective interrupt output specification bit (bit 1 at 034816), set "0" in the effective interrupt output polarity select bit (bit 0 at 034816) and set "1" in the interrupt occurrence frequency set counter (034D16). These settings cause a timer B2 interrupt to occur every other interval when the U phase output goes to "H".

When the timer B2 counter's content becomes 000016, timer A4 starts outputting one-shot pulses. In this instance, the content of DU1 (bit 0 at 034B16) and that of DU0 (bit 0 at 034A16) are set in the three-phase output shift register (U phase), the content of DUB1 (bit 1 at 034B16) and that of DUB0 (bit 1 at 034A16) are set in the three-phase output shift register (\overline{U} phase). After triangular wave modulation mode is selected, however, no setting is made in the shift register even though the timer B2 counter's content becomes 000016.

The value of DU0 and that of DUB0 are output to the U terminal (P80) and to the U terminal (P81) respectively. When the timer A4 counter counts the value written to timer A4 (038F16, 038E16) and when timer A4 finishes outputting one-shot pulses, the three-phase shift register's content is shifted one position, and the value of DU1 and that of DUB1 are output to the U phase output signal and to U phase output signal respectively. At this time, one-shot pulses are output from the timer for setting dead time used for setting the time over which the "L" level of the U phase waveform does not lap over the "L" level of the U phase waveform, which has the opposite phase of the former. The U phase waveform output that started from the "H" level keeps its level until the timer for setting dead time finishes outputting one-shot pulses even though the three-phase output shift register's content changes from "1" to "0" by the effect of the one-shot pulses. When the timer for setting dead time finishes outputting one-shot pulses, "0" already shifted in the three-phase shift register goes effective, and the U phase waveform changes to the "L" level. When the timer B2 counter's content becomes 000016, the timer A4 counter starts counting the value written to timer A4-1 (034716, 034616), and starts outputting one-shot pulses. When timer A4 finishes outputting one-shot pulses, the three-phase shift register's content is shifted one position, but if the three-phase output shift register's content changes from "0" to "1" as a result of the shift, the output level changes from "L" to "H" without waiting for the timer for setting dead time to finish outputting one-shot pulses. A U phase waveform is generated by these workings repeatedly. With the exception that the three-phase output shift register on the U phase side is used, the workings in generating a U phase waveform, which has the opposite phase of the U phase waveform, are the same as in generating a U



phase waveform. In this way, a waveform can be picked up from the applicable terminal in a manner in which the "L" level of the U phase waveform doesn't lap over that of the \overline{U} phase waveform, which has the opposite phase of the U phase waveform. The width of the "L" level too can be adjusted by varying the values of timer B2, timer A4, and timer A4-1. In dealing with the V and W phases, and \overline{V} and \overline{W} phases, the latter are of opposite phase of the former, have the corresponding timers work similarly to dealing with the U and \overline{U} phases to generate an intended waveform.

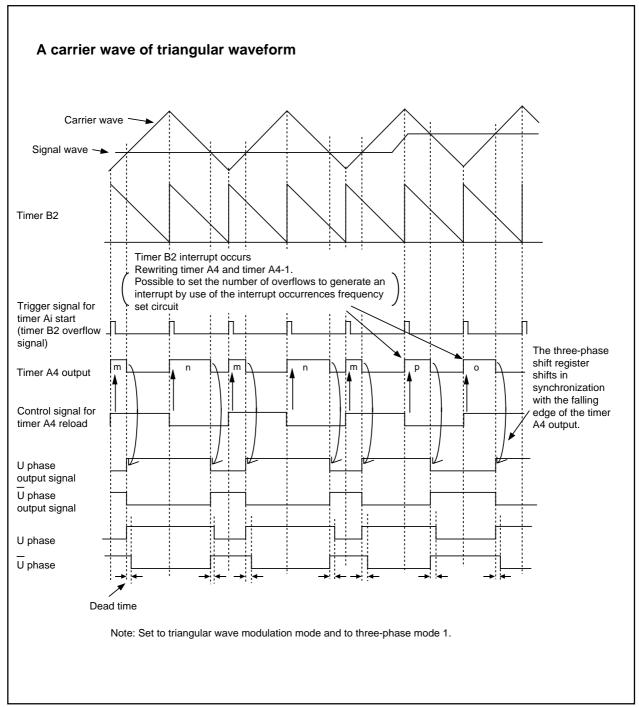


Figure 1.15.6. Timing chart of operation (1)



Assigning certain values to DU0 (bit 0 at 034A16) and DUB0 (bit 1 at 034A16), and to DU1 (bit 0 at 034B16) and DUB1 (bit 1 at 034B16) allows the user to output the waveforms as shown in Figure 1.15.7, that is, to output the U phase alone, to fix \overline{U} phase to "H", to fix the U phase to "H," or to output the \overline{U} phase alone.

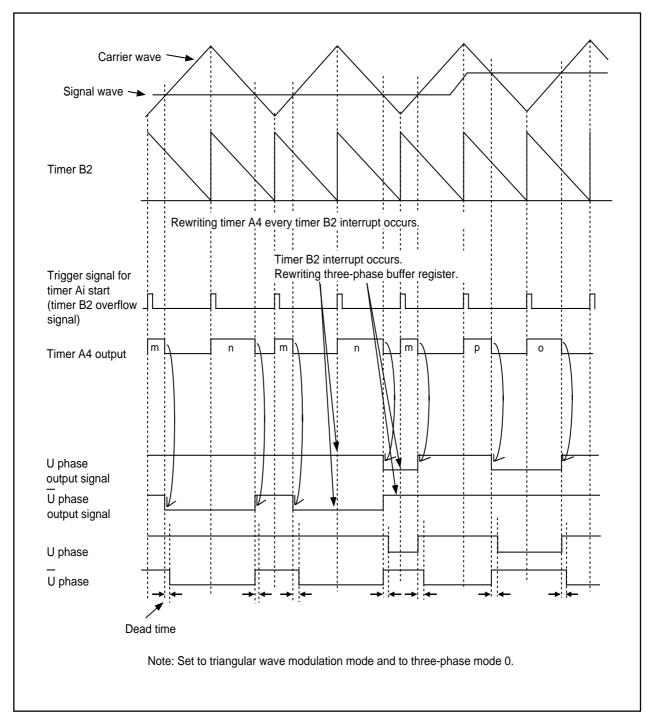


Figure 1.15.7. Timing chart of operation (2)

Sawtooth modulation

To generate a PWM waveform of sawtooth wave modulation, set "1" in the modulation mode select bit (bit 6 at 034816). Also, set "0" in the timers A4-1, A1-1, and A2-1 control bit (bit 1 at 034916). In this mode, the timer registers of timers A4, A1, and A2 comprise conventional timers A4, A1, and A2 alone, and reload the corresponding timer register's content to the counter every time the timer B2 counter's content becomes 000016. The effective interrupt output specification bit (bit 1 at 034816) and the effective interrupt output polarity select bit (bit 0 at 034816) go nullified.

An example of U phase waveform is shown in Figure 1.15.8, and the description of waveform output workings is given below. Set "1" in DU0 (bit 0 at 034A16), and set "0" in DUB0 (bit 1 at 034A16). In addition, set "0" in DU1 (bit 0 at 034A16) and set "1" in DUB1 (bit 1 at 034A16).

When the timber B2 counter's content becomes 000016, timer B2 generates an interrupt, and timer A4 starts outputting one-shot pulses at the same time. In this instance, the contents of the three-phase buffer registers DU1 and DU0 are set in the three-phase output shift register (U phase), and the contents of DUB1 and DUB0 are set in the three-phase output shift register (\overline{U} phase). After this, the three-phase buffer register's content is set in the three-phase shift register every time the timer B2 counter's content becomes 000016.

The value of DU0 and that of DUB0 are output to the U terminal (P80) and to the \overline{U} terminal (P81) respectively. When the timer A4 counter counts the value written to timer A4 (038F16, 038E16) and when timer A4 finishes outputting one-shot pulses, the three-phase output shift register's content is shifted one position, and the value of DU1 and that of DUB1 are output to the U phase output signal and to the \overline{U} output signal respectively. At this time, one-shot pulses are output from the timer for setting dead time used for setting the time over which the "L" level of the U phase waveform doesn't lap over the "L" level of the \overline{U} phase waveform, which has the opposite phase of the former. The U phase waveform output that started from the "H" level keeps its level until the timer for setting dead time finishes outputting one-shot pulses even though the three-phase output shift register's content changes from "1" to "0 "by the effect of the one-shot pulses. When the timer for setting dead time finishes outputting one-shot pulses, 0 already shifted in the three-phase shift register goes effective, and the U phase waveform changes to the "L" level. When the timer B2 counter's content becomes 000016, the contents of the three-phase buffer registers DU1 and DU0 are set in the three-phase output shift register (\overline{U} phase), and the contents of DUB1 and DUB0 are set in the three-phase output shift register (\overline{U} phase) again.

A U phase waveform is generated by these workings repeatedly. With the exception that the three-phase output shift register on the \overline{U} phase side is used, the workings in generating a \overline{U} phase waveform, which has the opposite phase of the U phase waveform, are the same as in generating a U phase waveform. In this way, a waveform can be picked up from the applicable terminal in a manner in which the "L" level of the U phase waveform doesn't lap over that of the \overline{U} phase waveform, which has the opposite phase of the U phase waveform. The width of the "L" level too can be adjusted by varying the values of timer B2 and timer A4. In dealing with the V and W phases, and \overline{V} and \overline{W} phases, the latter are of opposite phase of the former, have the corresponding timers work similarly to dealing with the U and \overline{U} phases to generate an intended waveform.

Setting "1" both in DUB0 and in DUB1 provides a means to output the U phase alone and to fix the $\overline{\text{U}}$ phase output to "H" as shown in Figure 1.15.9.



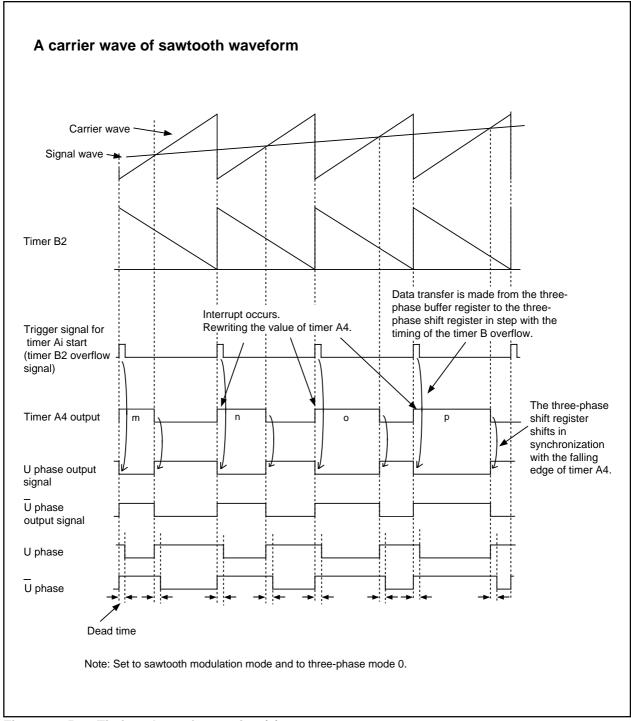


Figure 1.15.8. Timing chart of operation (3)

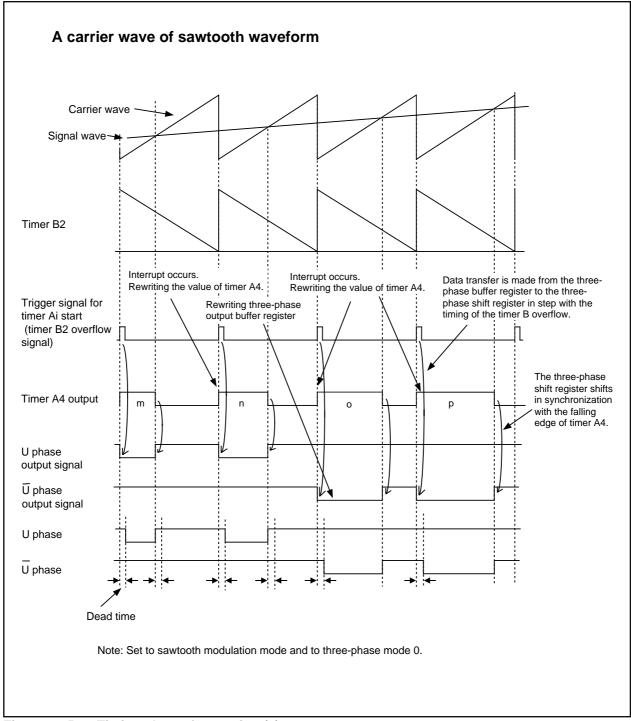


Figure 1.15.9. Timing chart of operation (4)

Serial I/O

Serial I/O is configured as five channels: UART0, UART1, UART2, S I/O3 and S I/O4.

UART0 to 2

UART0, UART1 and UART2 each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 1.16.1 shows the block diagram of UART0, UART1 and UART2. Figures 1.16.2 and 1.16.3 show the block diagram of the transmit/receive unit.

UARTi (i = 0 to 2) has two operation modes: a clock synchronous serial I/O mode and a clock asynchronous serial I/O mode (UART mode). The contents of the serial I/O mode select bits (bits 0 to 2 at addresses 03A016, 03A816 and 037816) determine whether UARTi is used as a clock synchronous serial I/O or as a UART. Although a few functions are different, UART0, UART1 and UART2 have almost the same functions. UART2, in particular, is used for the SIM interface with some extra settings added in clock-asynchronous serial I/O mode (Note). It also has the bus collision detection function that generates an interrupt request if the TxD pin and the RxD pin are different in level.

Table 1.16.1 shows the comparison of functions of UART0 through UART2, and Figures 1.16.4 to 1.16.9 show the registers related to UARTi.

Note: SIM: Subscriber Identity Module

Table 1.16.1. Comparison of functions of UART0 through UART2

Function	UART0	UART1	UART2	
CLK polarity selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 1)	
LSB first / MSB first selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 2)	
Continuous receive mode selection	Possible (Note 1)	Possible (Note 1)	Possible (Note 1)	
Transfer clock output from multiple pins selection	Impossible	Possible (Note 1)	Impossible	
Serial data logic switch	Impossible	Impossible	Possible (Note 4)	
Sleep mode selection	Possible (Note 3)	Possible (Note 3)	Impossible	
TxD, RxD I/O polarity switch	Impossible	Impossible Possible		
TxD, RxD port output format	CMOS output	CMOS output	N-channel open-drain output	
Parity error signal output	Impossible	Impossible	Possible (Note 4)	
Bus collision detection	Impossible Impossible Possible		Possible	

Note 1: Only when clock synchronous serial I/O mode.

Note 2: Only when clock synchronous serial I/O mode and 8-bit UART mode.

Note 3: Only when UART mode.

Note 4: Using for SIM interface.



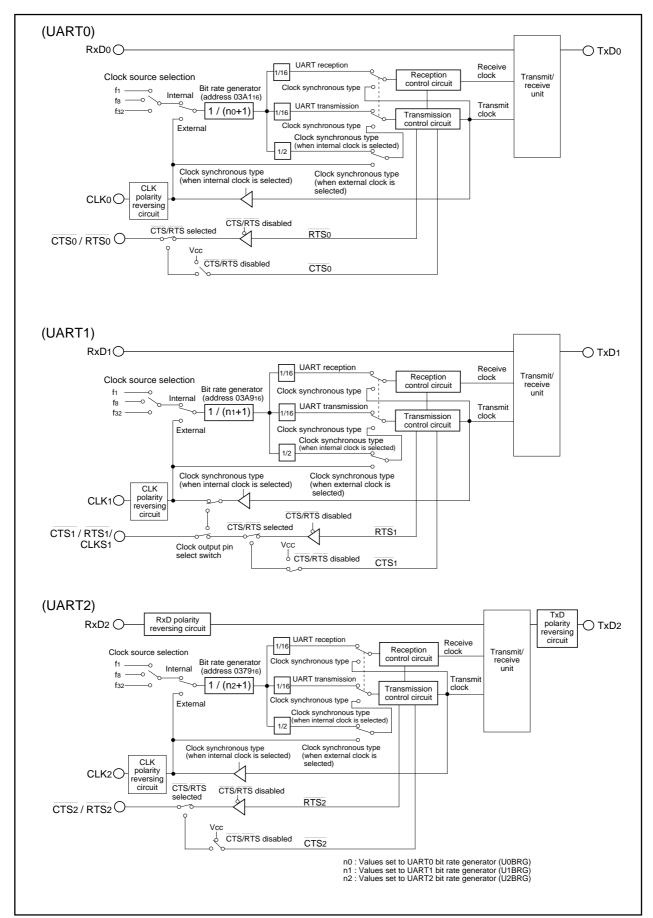


Figure 1.16.1. Block diagram of UARTi (i = 0 to 2)



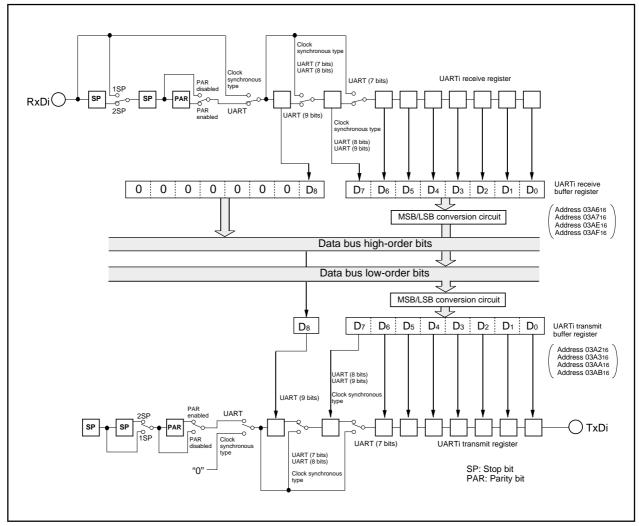


Figure 1.16.2. Block diagram of UARTi (i = 0, 1) transmit/receive unit

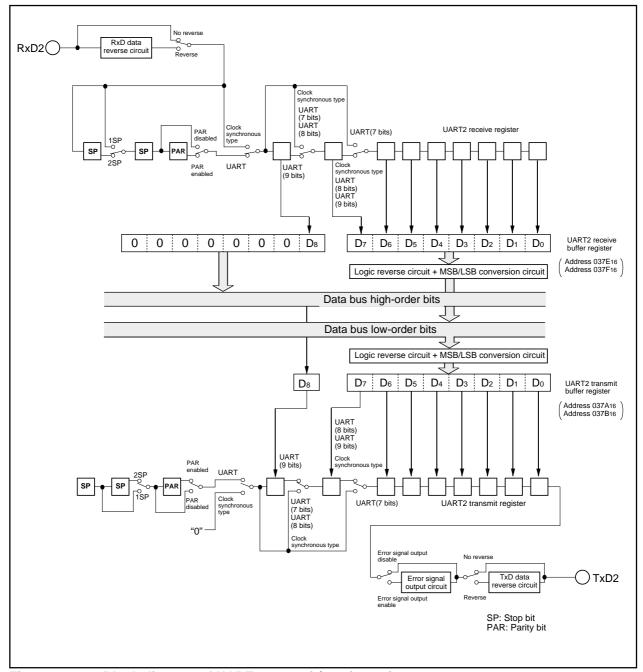


Figure 1.16.3. Block diagram of UART2 transmit/receive unit

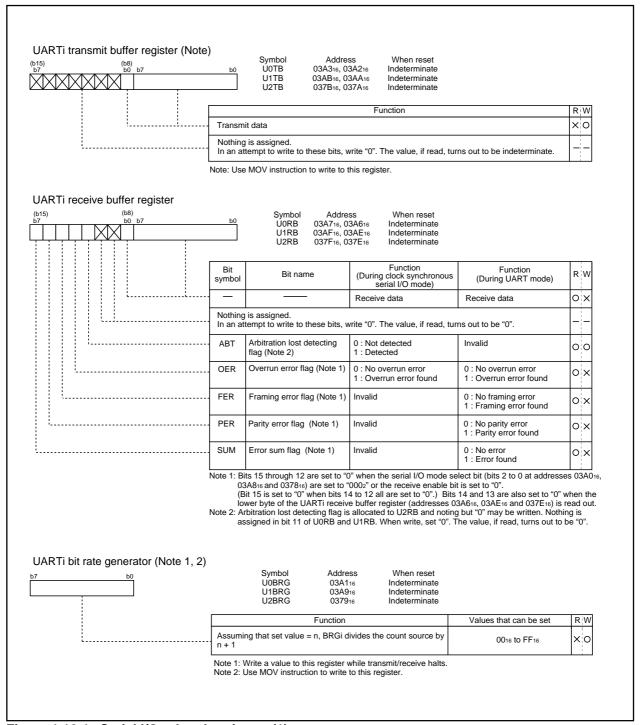


Figure 1.16.4. Serial I/O-related registers (1)

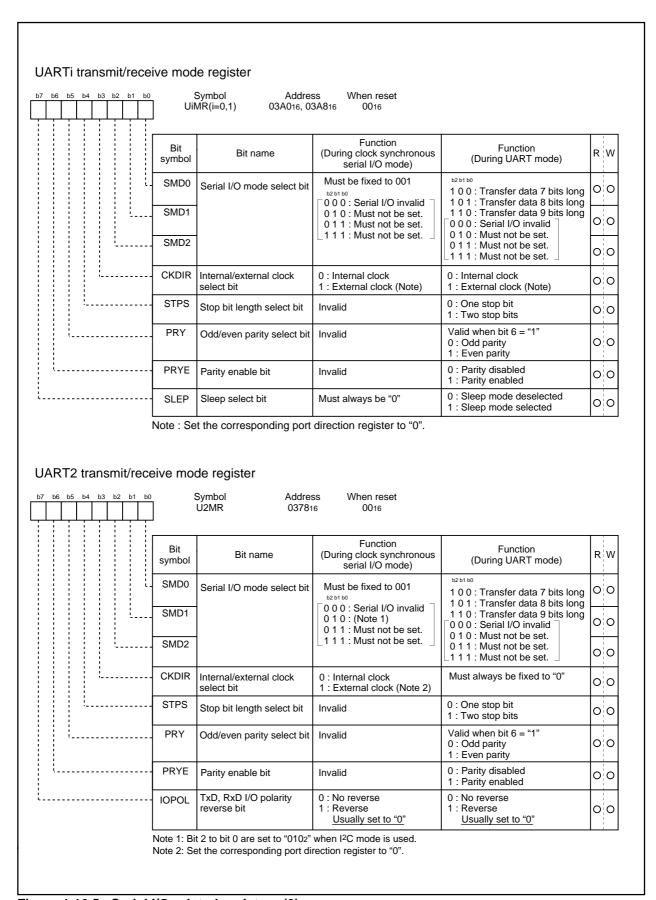


Figure 1.16.5. Serial I/O-related registers (2)



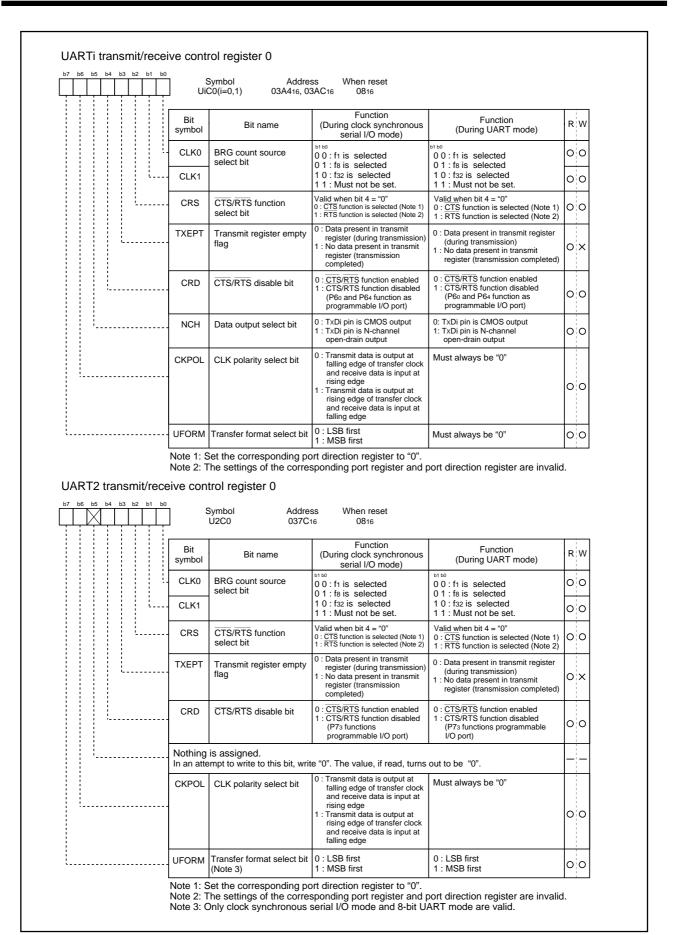


Figure 1.16.6. Serial I/O-related registers (3)

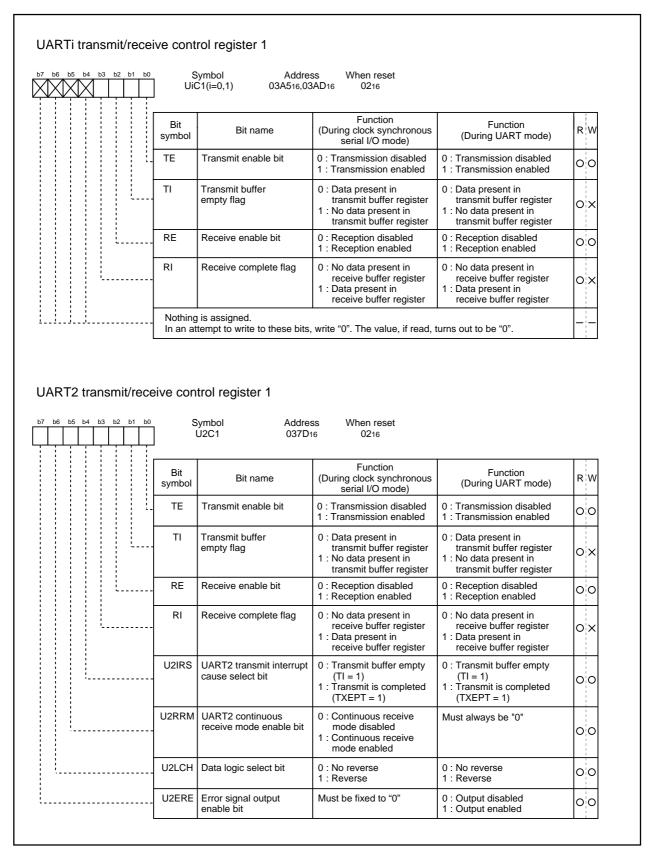


Figure 1.16.7. Serial I/O-related registers (4)



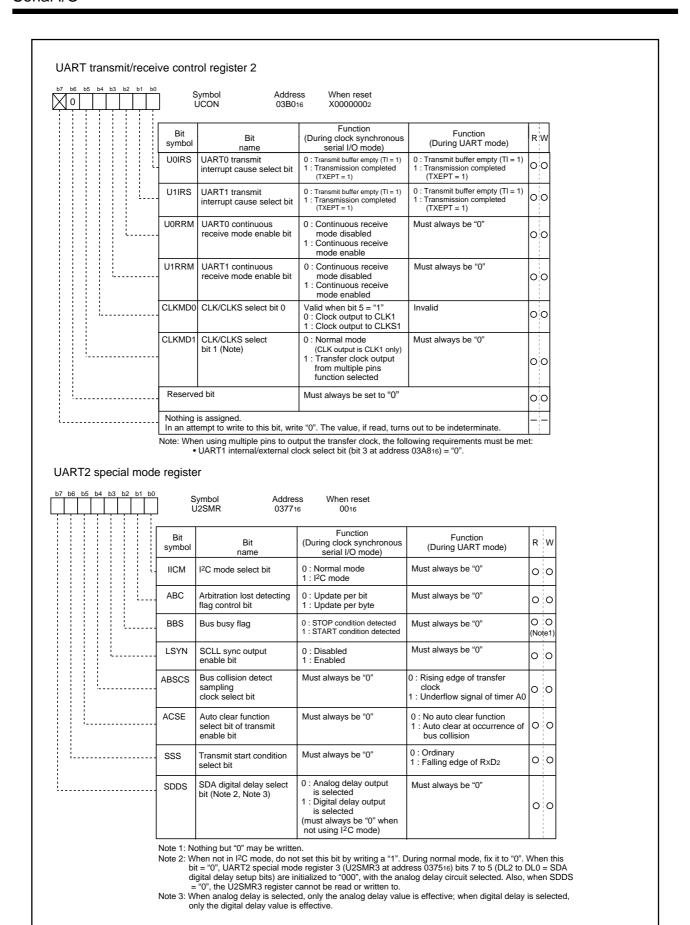
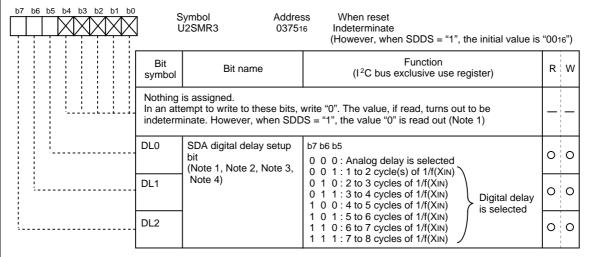


Figure 1.16.8. Serial I/O-related registers (5)

UART2 special mode register 2 (I ² C bus exclusive use register)					
b7 b6 b5 b4 b3 b2 b1 b0	٦ ٥	Symbol Addre J2SMR2 03761			
	Bit symbol	Bit name	Function (I ² C bus exclusive use)	R W	
	IICM2	I ² C mode select bit 2	Refer to Table 1.16.11	0 0	
	CSC	Clock-synchronous bit	0 : Disabled 1 : Enabled	0 0	
	SWC	SCL wait output bit	0 : Disabled 1 : Enabled	0 0	
	ALS	SDA output stop bit	0 : Disabled 1 : Enabled	0 0	
	STAC	UART2 initialization bit	0 : Disabled 1 : Enabled	0 0	
!	SWC2	SCL wait output bit 2	0: UART2 clock 1: 0 output	0 0	
	SDHI	SDA output disable bit	0: Enabled 1: Disabled (high impedance)	0 0	
	SHTC	Start/stop condition control bit	Set this bit to "1" in I ² C mode (refer to Table 1.16.12)	0 0	

UART2 special mode register 3 (I²C bus exclusive use register)



- Note 1: This bit can be read or written to when UART2 special mode register (U2SMR at address 037716) bit 7 (SDDS: SDA digital delay select bit) = "1". When the initial value of UART2 special mode register 3 (U2SMR3) is read after setting SDDS = "1", the value is "0016". When writing to UART2 special mode register 3 (U2SMR3) after setting SDDS = "1", be sure to write 0's to bits 0–4. When SDDS = "0", this register cannot be written to; when read, the value is indeterminate.
- Note 2: These bits are initialized to "000" when SDDS = "0", with the analog delay circuit selected. After a reset, these bits are set to "000", with the analog delay circuit selected. However, because these bits can be read only when SDDS = "1", the value read from these bits when SDDS = "0" is indeterminate.
- Note 3: When analog delay is selected, only the analog delay value is effective; when digital delay is selected, only the digital delay value is effective.
- Note 4: The amount of delay varies with the load on SCL and SDA pins. Also, when using an external clock, the amount of delay increases by about 100 ns, so be sure to take this into account when using the device.

Figure 1.16.9. Serial I/O-related registers (6)



(1) Clock synchronous serial I/O mode

The clock synchronous serial I/O mode uses a transfer clock to transmit and receive data. Tables 1.16.2 and 1.16.3 list the specifications of the clock synchronous serial I/O mode. Figure 1.16.10 shows the UARTi transmit/receive mode register.

Table 1.16.2. Specifications of clock synchronous serial I/O mode (1)

Item	Specification		
Transfer data format	Transfer data length: 8 bits		
Transfer clock	When internal clock is selected (bit 3 at addresses 03A016, 03A816, 037816)		
	= "0") : fi/ 2(n+1) (Note 1) fi = f1, f8, f32		
	When external clock is selected (bit 3 at addresses 03A016, 03A816, 037816)		
	= "1") : Input from CLKi pin		
Transmission/reception control	• CTS function, RTS function, CTS and RTS function invalid: selectable		
Transmission start condition	To start transmission, the following requirements must be met:		
	- Transmit enable bit (bit 0 at addresses 03A516, 03AD16, 037D16) = "1"		
	- Transmit buffer empty flag (bit 1 at addresses 03A516, 03AD16, 037D16) = "0"		
	– When CTS function selected, CTS input level = "L"		
	Furthermore, if external clock is selected, the following requirements must also be met:		
	- CLKi polarity select bit (bit 6 at addresses 03A416, 03AC16, 037C16) = "0":		
	CLKi input level = "H"		
	- CLKi polarity select bit (bit 6 at addresses 03A416, 03AC16, 037C16) = "1":		
	CLKi input level = "L"		
Reception start condition	To start reception, the following requirements must be met:		
	- Receive enable bit (bit 2 at addresses 03A516, 03AD16, 037D16) = "1"		
	- Transmit enable bit (bit 0 at addresses 03A516, 03AD16, 037D16) = "1"		
	- Transmit buffer empty flag (bit 1 at addresses 03A516, 03AD16, 037D16) = "0"		
	Furthermore, if external clock is selected, the following requirements must		
	also be met:		
	CLKi polarity select bit (bit 6 at addresses 03A416, 03AC16, 037C16) = "0":CLKi input level = "H"		
	•		
	CLKi polarity select bit (bit 6 at addresses 03A416, 03AC16, 037C16) = "1":CLKi input level = "L"		
Interrupt request	When transmitting		
Interrupt request generation timing	- Transmit interrupt cause select bit (bits 0, 1 at address 03B016, bit 4 at		
generation timing	address 037D16) = "0": Interrupts requested when data transfer from UARTi		
	transfer buffer register to UARTi transmit register is completed		
	- Transmit interrupt cause select bit (bits 0, 1 at address 03B016, bit 4 at		
	address 037D16) = "1": Interrupts requested when data transmission from		
	UARTi transfer register is completed		
	When receiving		
	Interrupts requested when data transfer from UARTi receive register to		
	UARTi receive buffer register is completed		
Error detection	Overrun error (Note 2)		
	This error occurs when the next data is ready before contents of UARTi		
	receive buffer register are read out		
	1000110 ballot regioter are read out		

Note 1: "n" denotes the value 0016 to FF16 that is set to the UART bit rate generator.

Note 2: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit does not change.



Table 1.16.3. Specifications of clock synchronous serial I/O mode (2)

Item	Specification
Select function	CLK polarity selection
	Whether transmit data is output/input timing at the rising edge or falling edge
	of the transfer clock can be selected
	LSB first/MSB first selection
	Whether transmission/reception begins with bit 0 or bit 7 can be selected
	Continuous receive mode selection
	Reception is enabled simultaneously by a read from the receive buffer register
	Transfer clock output from multiple pins selection (UART1)
	UART1 transfer clock can be chosen by software to be output from one of
	the two pins set
	Switching serial data logic (UART2)
	Whether to reverse data in writing to the transmission buffer register or
	reading the reception buffer register can be selected.
	TxD, RxD I/O polarity reverse (UART2)
	This function is reversing TxD port output and RxD port input. All I/O data
	level is reversed.



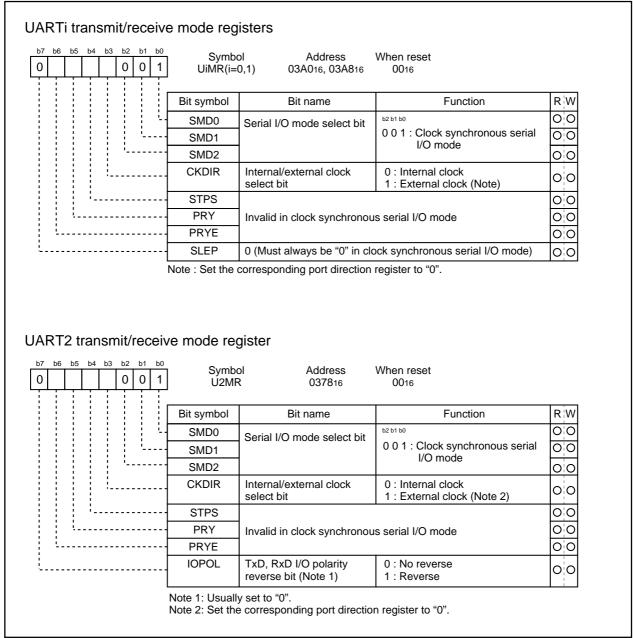


Figure 1.16.10. UARTi transmit/receive mode register in clock synchronous serial I/O mode

Table 1.16.4 lists the functions of the input/output pins during clock synchronous serial I/O mode. This table shows the pin functions when the transfer clock output from multiple pins function is <u>not selected</u>. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.16.4. Input/output pin functions in clock synchronous serial I/O mode (when transfer clock output from multiple pins is <u>not selected</u>)

Pin name	Function	Method of selection
TxDi (P63, P67, P70)	Serial data output	(Outputs dummy data when performing reception only)
RxDi (P62, P66, P71)	Serial data input	Port P62, P66 and P71 direction register (bits 2 and 6 at address 03EE16, bit 1 at address 03EF16)= "0" (Can be used as an input port when performing transmission only)
CLKi	Transfer clock output	Internal/external clock select bit (bit 3 at address 03A016, 03A816, 037816) = "0"
(P61, P65, P72)	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A016, 03A816, 037816) = "1" Port P61, P65 and P72 direction register (bits 1 and 5 at address 03EE16, bit 2 at address 03EF16) = "0"
CTSi/RTSi (P60, P64, P73)	CTS input	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) ="0" CTS/RTS function select bit (bit 2 at address 03A416, 03AC16, 037C16) = "0" Port P60, P64 and P73 direction register (bits 0 and 4 at address 03EE16, bit 3 at address 03EF16) = "0"
	RTS output	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) = "0" CTS/RTS function select bit (bit 2 at address 03A416, 03AC16, 037C16) = "1"
	Programmable I/O port	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) = "1"



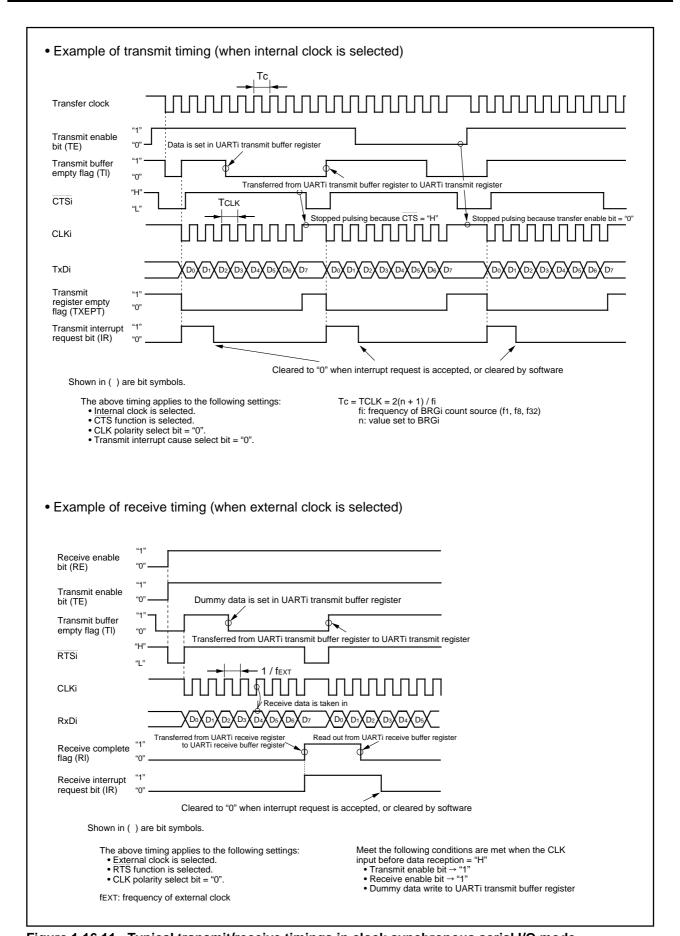


Figure 1.16.11. Typical transmit/receive timings in clock synchronous serial I/O mode



(a) Polarity select function

As shown in Figure 1.16.12, the CLK polarity select bit (bit 6 at addresses 03A416, 03AC16, 037C16) allows selection of the polarity of the transfer clock.

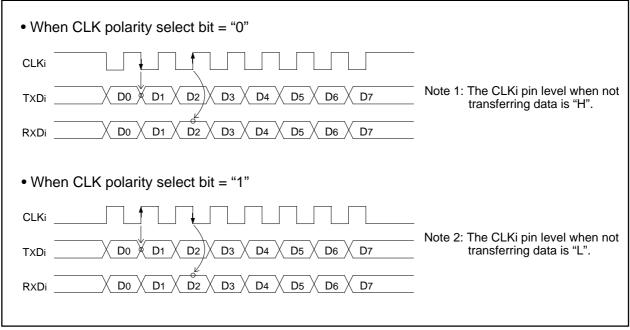


Figure 1.16.12. Polarity of transfer clock

(b) LSB first/MSB first select function

As shown in Figure 1.16.13, when the transfer format select bit (bit 7 at addresses 03A416, 03AC16, 037C16) = "0", the transfer format is "LSB first"; when the bit = "1", the transfer format is "MSB first".

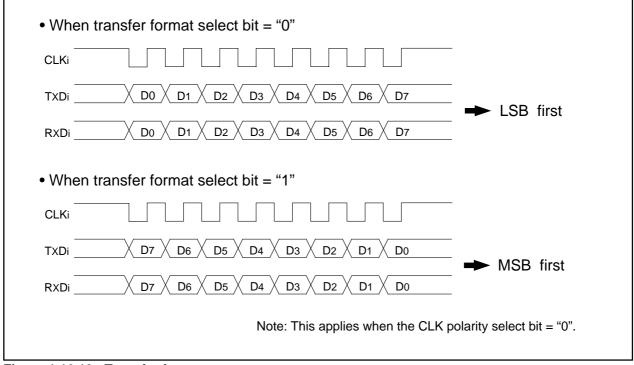


Figure 1.16.13. Transfer format



(c) Transfer clock output from multiple pins function (UART1)

This function allows the setting two transfer clock output pins and choosing one of the two to output a clock by using the CLK and CLKS select bit (bits 4 and 5 at address 03B016). (See Figure 1.16.14.) The multiple pins function is valid only when the internal clock is selected for UART1.

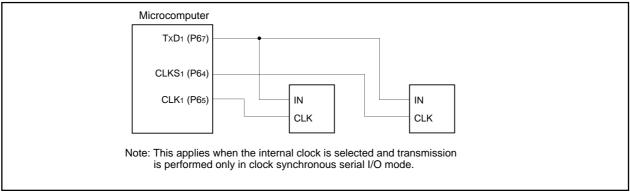


Figure 1.16.14. The transfer clock output from the multiple pins function usage

(d) Continuous receive mode

If the continuous receive mode enable bit (bits 2 and 3 at address 03B016, bit 5 at address 037D16) is set to "1", the unit is placed in continuous receive mode. In this mode, when the receive buffer register is read out, the unit simultaneously goes to a receive enable state without having to set dummy data to the transmit buffer register back again.

(e) Serial data logic switch function (UART2)

When the data logic select bit (bit6 at address 037D16) = "1", and writing to transmit buffer register or reading from receive buffer register, data is reversed. Figure 1.16.15 shows the example of serial data logic switch timing.

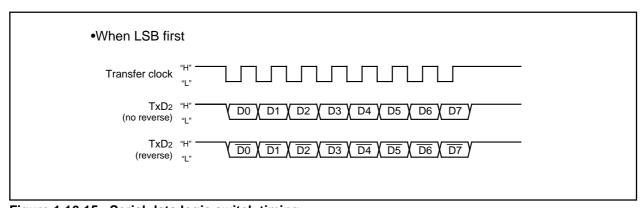


Figure 1.16.15. Serial data logic switch timing

(2) Clock asynchronous serial I/O (UART) mode

The UART mode allows transmitting and receiving data after setting the desired transfer rate and transfer data format. Tables 1.16.5 and 1.16.6 list the specifications of the UART mode. Figure 1.16.16 shows the UARTi transmit/receive mode register.

Table 1.16.5. Specifications of UART Mode (1)

Item	Specification
Transfer data format	Character bit (transfer data): 7 bits, 8 bits, or 9 bits as selected
	Start bit: 1 bit
	Parity bit: Odd, even, or nothing as selected
	Stop bit: 1 bit or 2 bits as selected
Transfer clock	• When internal clock is selected (bit 3 at addresses 03A016, 03A816, 037816 = "0"):
	fi/16(n+1) (Note 1) $fi = f1, f8, f32$
	• When external clock is selected (bit 3 at addresses 03A016, 03A816 ="1"):
	fEXT/16(n+1) (Note 1) (Note 2) (Do not set external clock for UART2)
Transmission/reception control	TTS function, RTS function, CTS and RTS function invalid: selectable
Transmission start condition	To start transmission, the following requirements must be met:
	- Transmit enable bit (bit 0 at addresses 03A516, 03AD16, 037D16) = "1"
	- Transmit buffer empty flag (bit 1 at addresses 03A516, 03AD16, 037D16) = "0"
	- When $\overline{\text{CTS}}$ function selected, $\overline{\text{CTS}}$ input level = "L"
Reception start condition	To start reception, the following requirements must be met:
	- Receive enable bit (bit 2 at addresses 03A516, 03AD16, 037D16) = "1"
	- Start bit detection
Interrupt request	When transmitting
generation timing	- Transmit interrupt cause select bits (bits 0,1 at address 03B016, bit4 at
	address 037D16) = "0": Interrupts requested when data transfer from UARTi
	transfer buffer register to UARTi transmit register is completed
	- Transmit interrupt cause select bits (bits 0, 1 at address 03B016, bit4 at
	address 037D16) = "1": Interrupts requested when data transmission from
	UARTi transfer register is completed
	When receiving
	- Interrupts requested when data transfer from UARTi receive register to
	UARTi receive buffer register is completed
Error detection	Overrun error (Note 3)
	This error occurs when the next data is ready before contents of UARTi
	receive buffer register are read out
	Framing error
	This error occurs when the number of stop bits set is not detected
	Parity error
	This error occurs when if parity is enabled, the number of 1's in parity and
	character bits does not match the number of 1's set
	Error sum flag
	This flag is set (= 1) when any of the overrun, framing, and parity errors is
	encountered

Note 1: 'n' denotes the value 0016 to FF16 that is set to the UARTi bit rate generator.

Note 2: fext is input from the CLKi pin.

Note 3: If an overrun error occurs, the UARTi receive buffer will have the next data written in. Note also that the UARTi receive interrupt request bit is not set to "1".



Table 1.16.6. Specifications of UART Mode (2)

Item	Specification		
Select function	Sleep mode selection (UART0, UART1)		
	This mode is used to transfer data to and from one of multiple slave micro- computers		
	Serial data logic switch (UART2)		
	This function is reversing logic value of transferring data. Start bit, parity bit and stop bit are not reversed.		
	• TxD, RxD I/O polarity switch (UART2)		
	This function is reversing TxD port output and RxD port input. All I/O data		
	level is reversed.		



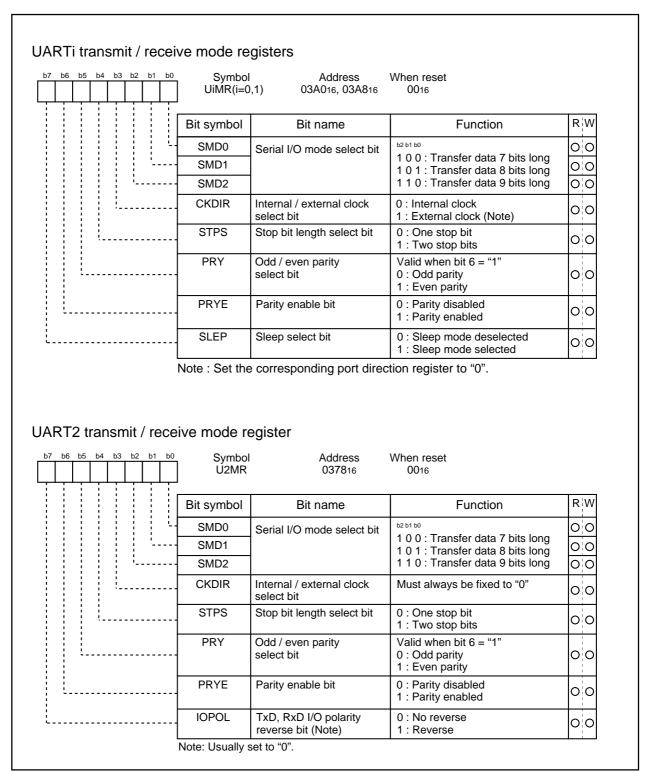


Figure 1.16.16. UARTi transmit/receive mode register in UART mode

Table 1.16.7 lists the functions of the input/output pins during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an "H". (If the N-channel open-drain is selected, this pin is in floating state.)

Table 1.16.7. Input/output pin functions in UART mode

Pin name	Function	Method of selection
TxDi (P63, P67, P70)	Serial data output	
RxDi (P62, P66, P71)	Serial data input	Port P62, P66 and P71 direction register (bits 2 and 6 at address 03EE16, bit 1 at address 03EF16)= "0" (Can be used as an input port when performing transmission only)
CLKi	Programmable I/O port	Internal/external clock select bit (bit 3 at address 03A016, 03A816, 037816) = "0"
(P61, P65, P72)	Transfer clock input	Internal/external clock select bit (bit 3 at address 03A016, 03A816) = "1" Port P61, P65 direction register (bits 1 and 5 at address 03EE16) = "0" (Do not set external clock for UART2)
CTSi/RTSi (P60, P64, P73)	CTS input	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) ="0" CTS/RTS function select bit (bit 2 at address 03A416, 03AC16, 037C16) = "0" Port P60, P64 and P73 direction register (bits 0 and 4 at address 03EE16, bit 3 at address 03EF16) = "0"
	RTS output	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) = "0" CTS/RTS function select bit (bit 2 at address 03A416, 03AC16, 037C16) = "1"
	Programmable I/O port	CTS/RTS disable bit (bit 4 at address 03A416, 03AC16, 037C16) = "1"



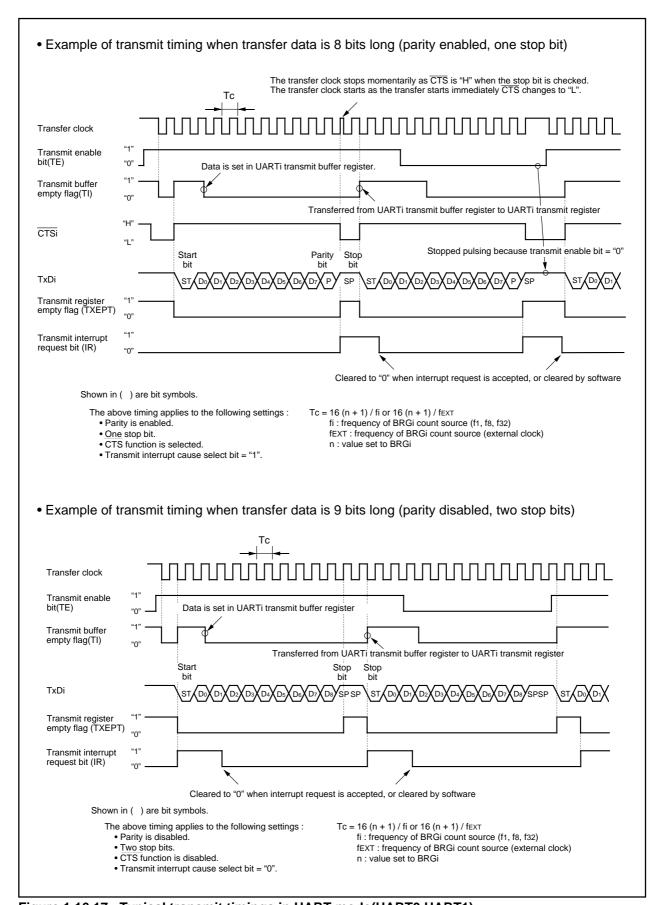


Figure 1.16.17. Typical transmit timings in UART mode(UART0,UART1)



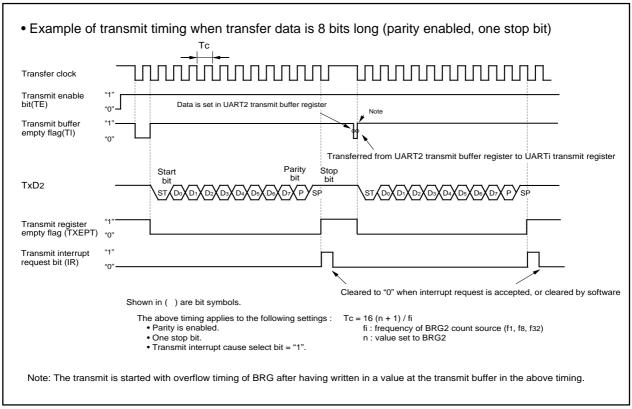


Figure 1.16.18. Typical transmit timings in UART mode(UART2)

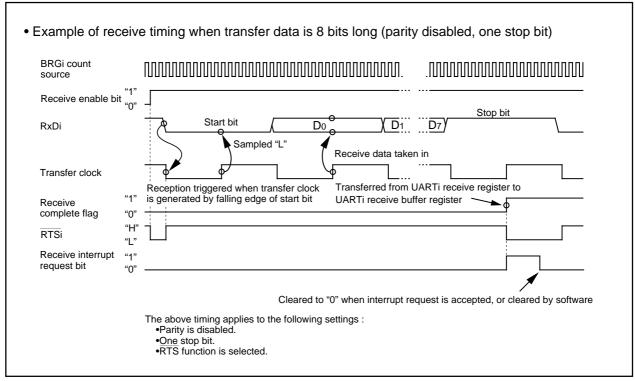


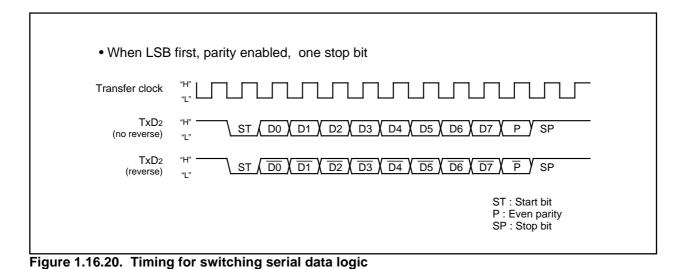
Figure 1.16.19. Typical receive timing in UART mode

(a) Sleep mode (UART0, UART1)

This mode is used to transfer data between specific microcomputers among multiple microcomputers connected using UARTi. The sleep mode is selected when the sleep select bit (bit 7 at addresses 03A016, 03A816) is set to "1" during reception. In this mode, the unit performs receive operation when the MSB of the received data = "1" and does not perform receive operation when the MSB = "0".

(b) Function for switching serial data logic (UART2)

When the data logic select bit (bit 6 of address 037D16) is assigned 1, data is inverted in writing to the transmission buffer register or reading the reception buffer register. Figure 1.16.20 shows the example of timing for switching serial data logic.



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(c) TxD, RxD I/O polarity reverse function (UART2)

This function is to reverse TxD pin output and RxD pin input. The level of any data to be input or output (including the start bit, stop bit(s), and parity bit) is reversed. Set this function to "0" (not to reverse) for usual use.

(d) Bus collision detection function (UART2)

This function is to sample the output level of the TxD pin and the input level of the RxD pin at the rising edge of the transfer clock; if their values are different, then an interrupt request occurs. Figure 1.16.21 shows the example of detection timing of a bus collision (in UART mode).

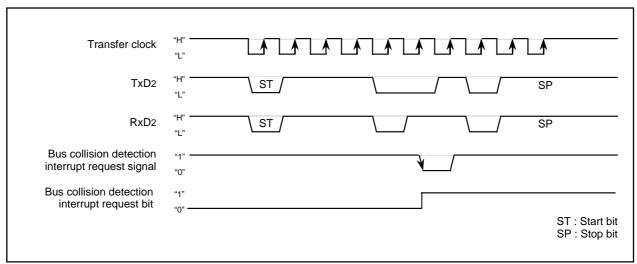


Figure 1.16.21. Detection timing of a bus collision (in UART mode)

(3) Clock-asynchronous serial I/O mode (used for the SIM interface)

The SIM interface is used for connecting the microcomputer with a memory card or the like; adding some extra settings in UART2 clock-asynchronous serial I/O mode allows the user to effect this function. Table 1.16.8 shows the specifications of clock-asynchronous serial I/O mode (used for the SIM interface).

Table 1.16.8. Specifications of clock-asynchronous serial I/O mode (used for the SIM interface)

Item	Specification
Transfer data format	• Transfer data 8-bit UART mode (bit 2 through bit 0 of address 037816 = "1012")
	• One stop bit (bit 4 of address 037816 = "0")
	With the direct format chosen
	Set parity to "even" (bit 5 and bit 6 of address 037816 = "1" and "1" respectively)
	Set data logic to "direct" (bit 6 of address 037D16 = "0").
	Set transfer format to LSB (bit 7 of address 037C16 = "0").
	With the inverse format chosen
	Set parity to "odd" (bit 5 and bit 6 of address 037816 = "0" and "1" respectively)
	Set data logic to "inverse" (bit 6 of address 037D16 = "1")
	Set transfer format to MSB (bit 7 of address 037C16 = "1")
Transfer clock	• With the internal clock chosen (bit 3 of address 037816 = "0"): fi / 16 (n + 1) (Note 1): fi=f1, f8, f32
	(Do not set external clock)
Transmission / reception control	• Disable the CTS and RTS function (bit 4 of address 037C16 = "1")
Other settings	The sleep mode select function is not available for UART2
	• Set transmission interrupt factor to "transmission completed" (bit 4 of address 037D16 = "1")
Transmission start condition	To start transmission, the following requirements must be met:
	- Transmit enable bit (bit 0 of address 037D16) = "1"
	- Transmit buffer empty flag (bit 1 of address 037D16) = "0"
Reception start condition	To start reception, the following requirements must be met:
	- Reception enable bit (bit 2 of address 037D16) = "1"
	- Detection of a start bit
Interrupt request	When transmitting
generation timing	When data transmission from the UART2 transmit register is completed
	(bit 4 of address 037D16 = "1")
	When receiving
	When data transfer from the UART2 receive register to the UART2 receive
	buffer register is completed
Error detection	Overrun error (see the specifications of clock-asynchronous serial I/O) (Note 2)
	• Framing error (see the specifications of clock-asynchronous serial I/O)
	Parity error (see the specifications of clock-asynchronous serial I/O)
	- On the reception side, an "L" level is output from the TxD2 pin by use of the parity error
	signal output function (bit 7 of address 037D16 = "1") when a parity error is detected
	- On the transmission side, a parity error is detected by the level of input to
	the RxD2 pin when a transmission interrupt occurs
	• The error sum flag (see the specifications of clock-asynchronous serial I/O)

Note 1: 'n' denotes the value 0016 to FF16 that is set to the UART2 bit rate generator.

Note 2: If an overrun error occurs, the UART2 receive buffer will have the next data written in. Note also that the UART2 receive interrupt request bit is not set to "1".



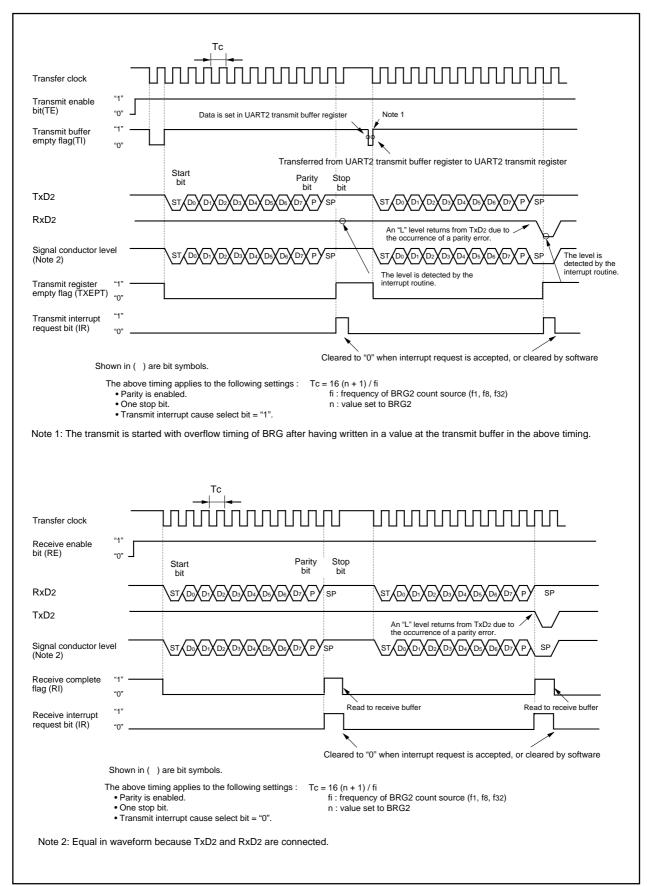


Figure 1.16.22. Typical transmit/receive timing in UART mode (used for the SIM interface)



(a) Function for outputting a parity error signal

During reception, with the error signal output enable bit (bit 7 of address 037D16) assigned "1", you can output an "L" level from the TxD2 pin when a parity error is detected. And during transmission, comparing with the case in which the error signal output enable bit (bit 7 of address 037D16) is assigned "0", the transmission completion interrupt occurs in the half cycle later of the transfer clock. Therefore parity error signals can be detected by a transmission completion interrupt program. Figure 1.16.23 shows the output timing of the parity error signal.

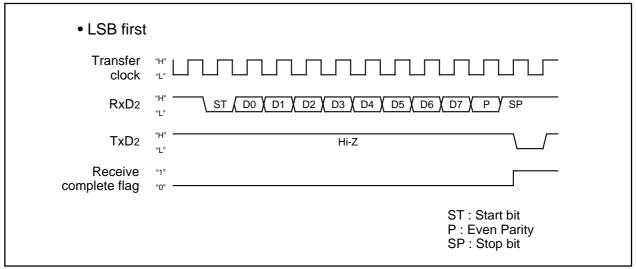


Figure 1.16.23. Output timing of the parity error signal

(b) Direct format/inverse format

Connecting the SIM card allows you to switch between direct format and inverse format. If you choose the direct format, D₀ data is output from TxD₂. If you choose the inverse format, D₇ data is inverted and output from TxD₂.

Figure 1.16.24 shows the SIM interface format.

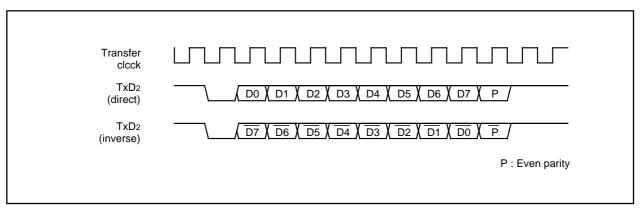


Figure 1.16.24. SIM interface format



Figure 1.16.25 shows the example of connecting the SIM interface. Connect TxD2 and RxD2 and apply pull-up.

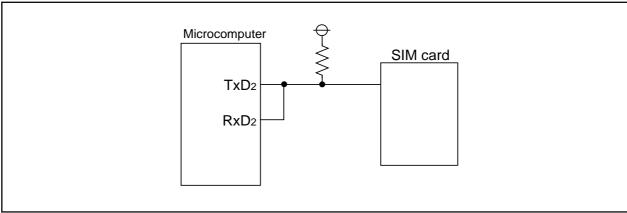


Figure 1.16.25. Connecting the SIM interface

UART2 Special Mode Register

The UART2 special mode register (address 037716) is used to control UART2 in various ways.

Figure 1.16.26 shows the UART2 special mode register.

Bit 0 of the UART2 special mode register (037716) is used as the I²C mode select bit.

Setting "1" in the I²C mode select bit (bit 0) goes the circuit to achieve the I²C bus (simplified I²C bus) interface effective.

Table 1.16.9 shows the relation between the I^2C mode select bit and respective control workings.

Since this function uses clock-synchronous serial I/O mode, set this bit to "0" in UART mode.

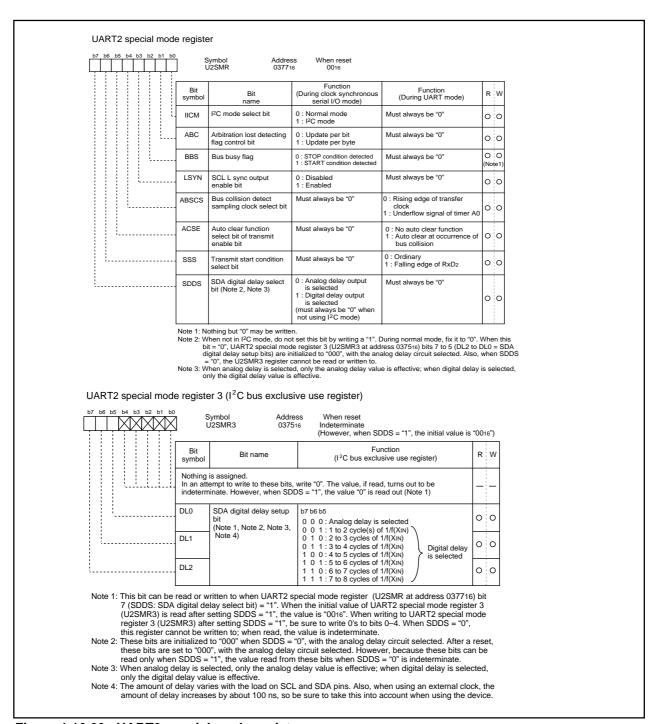


Figure 1.16.26. UART2 special mode register



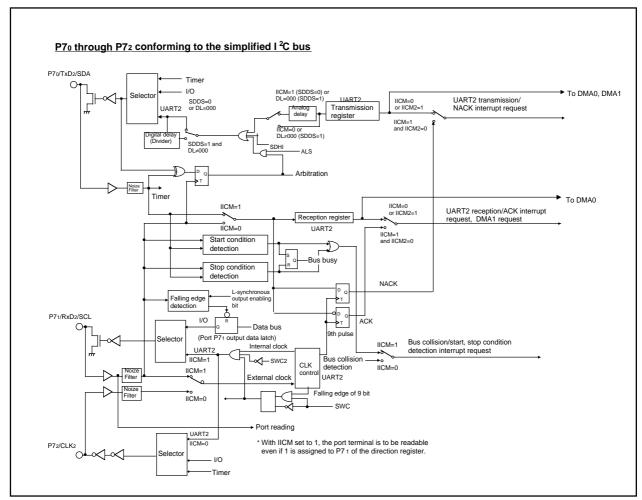


Figure 1.16.27. Functional block diagram for I²C mode

Table 1.16.9. Features in I²C mode

	Function	Normal mode	I ² C mode (Note 1)	
1	Factor of interrupt number 10 (Note 2)	Bus collision detection	Start condition detection or stop condition detection	
2	Factor of interrupt number 15 (Note 2)	UART2 transmission	No acknowledgment detection (NACK)	
3	Factor of interrupt number 16 (Note 2)	UART2 reception	Acknowledgment detection (ACK)	
4	UART2 transmission output delay	Not delayed	Delayed	
5	P70 at the time when UART2 is in use	TxD2 (output)	SDA (input/output) (Note 3)	
6	P71 at the time when UART2 is in use	RxD2 (input)	SCL (input/output)	
7	P72 at the time when UART2 is in use	CLK2	P72	
8	DMA1 factor at the time when 1 1 0 1 is assigned to the DMA request factor selection bits	UART2 reception	Acknowledgment detection (ACK)	
9	Noise filter width	15ns	50ns	
10	Reading P71	Reading the terminal when 0 is assigned to the direction register	Reading the terminal regardless of the value of the direction register	
11	Initial value of UART2 output	H level (when 0 is assigned to the CLK polarity select bit)	The value set in latch P70 when the port is selected	

Note 1: Make the settings given below when I^2C mode is in use.

Set 0 1 0 in bits 2, 1, 0 of the UART2 transmission/reception mode register.

Disable the RTS/CTS function. Choose the MSB First function. Note 2: Follow the steps given below to switch from a factor to another.

- 1. Disable the interrupt of the corresponding number.
- 2. Switch from a factor to another.
- Reset the interrupt request flag of the corresponding number.
- 4. Set an interrupt level of the corresponding number.
- Note 3: Set an initial value of SDA transmission output when serial I/O is invalid.



Figure 1.16.27 shows the functional block diagram for I²C mode. Setting "1" in the I²C mode select bit (IICM) causes ports P70, P71, and P72 to work as data transmission-reception terminal SDA, clock input-output terminal SCL, and port P72 respectively. A delay circuit is added to the SDA transmission output, so the SDA output changes after SCL fully goes to "L". The SDA digital delay select bit (bit 7 at address 037716) can be used to select between analog delay and digital delay. When digital delay is selected, the amount of delay can be selected in the range of 2 cycles to 8 cycles of f1 using UART2 special mode register 3 (at address 037516). Delay circuit select conditions are shown in Table 1.16.10.

Table 1.16.10. Dela	ay circuit	select	cona	itions

	Re	egister va	alue	Comtonto	
	IICM	SDDS	DL	Contents	
Digital delay is selected	1	1	001 to 111	When digital delay is selected, no analog delay is added. Only digital delay is effective.	
Analog delay is selected	1	1	000	When DL is set to "000", analog delay is selected no matter what value is set in SDDS.	
	'	0	(000)	When SDDS is set to "0", DL is initialized, so that DL ="000".	
No delay	0	0	(000)	When IICM = "0", no delay circuit is selected. When IICM = "0", however, always make sure SDDS = "0".	

An attempt to read Port P71 (SCL) results in getting the terminal's level regardless of the content of the port direction register. The initial value of SDA transmission output in this mode goes to the value set in port P70. The interrupt factors of the bus collision detection interrupt, UART2 transmission interrupt, and of UART2 reception interrupt turn to the start/stop condition detection interrupt, acknowledgment non-detection interrupt, and acknowledgment detection interrupt respectively.

The start condition detection interrupt refers to the interrupt that occurs when the falling edge of the SDA terminal (P70) is detected with the SCL terminal (P71) staying "H". The stop condition detection interrupt refers to the interrupt that occurs when the rising edge of the SDA terminal (P70) is detected with the SCL terminal (P71) staying "H". The bus busy flag (bit 2 of the UART2 special mode register) is set to "1" by the start condition detection, and set to "0" by the stop condition detection.

The acknowledgment non-detection interrupt refers to the interrupt that occurs when the SDA terminal level is detected still staying "H" at the rising edge of the 9th transmission clock. The acknowledgment detection interrupt refers to the interrupt that occurs when SDA terminal's level is detected already went to "L" at the 9th transmission clock. Also, assigning 1 1 0 1 (UART2 reception) to the DMA1 request factor select bits provides the means to start up the DMA transfer by the effect of acknowledgment detection. Bit 1 of the UART2 special mode register (037716) is used as the arbitration lost detecting flag control bit. Arbitration means the act of detecting the nonconformity between transmission data and SDA terminal data at the timing of the SCL rising edge. This detecting flag is located at bit 11 of the UART2 reception buffer register (037F16, 037E16), and "1" is set in this flag when nonconformity is detected. Use the arbitration lost detecting flag control bit to choose which way to use to update the flag, bit by bit or byte by byte. When setting this bit to "1" and updated the flag byte by byte if nonconformity is detected, the arbitration lost detecting flag is set to "1" at the falling edge of the 9th transmission clock.

If update the flag byte by byte, must judge and clear ("0") the arbitration lost detecting flag after completing the first byte acknowledge detect and before starting the next one byte transmission.

Bit 3 of the UART2 special mode register is used as SCL- and L-synchronous output enable bit. Setting this bit to "1" goes the P71 data register to "0" in synchronization with the SCL terminal level going to "L".



Some other functions added are explained here. Figure 1.16.28 shows their workings.

Bit 4 of the UART2 special mode register is used as the bus collision detect sampling clock select bit. The bus collision detect interrupt occurs when the RxD2 level and TxD2 level do not match, but the nonconformity is detected in synchronization with the rising edge of the transfer clock signal if the bit is set to "0". If this bit is set to "1", the nonconformity is detected at the timing of the overflow of timer A0 rather than at the rising edge of the transfer clock.

Bit 5 of the UART2 special mode register is used as the auto clear function select bit of transmit enable bit. Setting this bit to "1" automatically resets the transmit enable bit to "0" when "1" is set in the bus collision detect interrupt request bit (nonconformity).

Bit 6 of the UART2 special mode register is used as the transmit start condition select bit. Setting this bit to "1" starts the TxD transmission in synchronization with the falling edge of the RxD terminal.

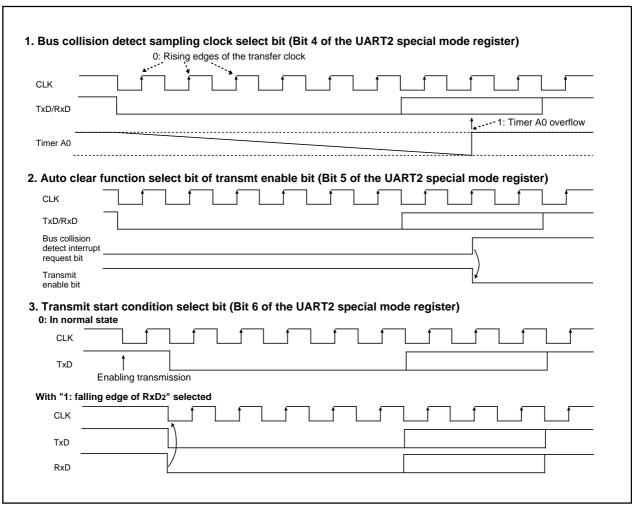


Figure 1.16.28. Some other functions added

UART2 Special Mode Register 2

UART2 special mode register 2 (address 037616) is used to further control UART2 in I²C mode. Figure 1.16.29 shows the UART2 special mode register 2.

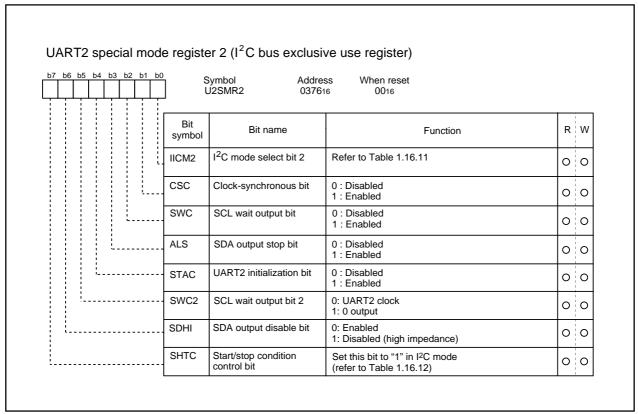


Figure 1.16.29. UART2 special mode register 2

Bit 0 of the UART2 special mode register 2 (address 037616) is used as the I²C mode select bit 2. Table 1.16.11 shows the types of control to be changed by I²C mode select bit 2 when the I²C mode select bit is set to "1". Table 1.16.12 shows the timing characteristics of detecting the start condition and the stop condition. Set the start/stop condition control bit (bit 7 of UART2 special mode register 2) to "1" in I²C mode.

Table 1.16.11. Functions changed by I²C mode select bit 2

	Function	IICM2 = 0	IICM2 = 1
1	Factor of interrupt number 15	No acknowledgment detection (NACK)	UART2 transmission (the rising edge of the final bit of the clock)
2	Factor of interrupt number 16	Acknowledgment detection (ACK)	UART2 reception (the falling edge of the final bit of the clock)
3	DMA1 factor at the time when 1 1 0 1 is assigned to the DMA request factor selection bits	Acknowledgment detection (ACK)	UART2 reception (the falling edge of the final bit of the clock)
4	Timing for transferring data from the UART2 reception shift register to the reception buffer.	The rising edge of the final bit of the reception clock	The falling edge of the final bit of the reception clock
5	Timing for generating a UART2 reception/ACK interrupt request	The rising edge of the final bit of the reception clock	The falling edge of the final bit of the reception clock

Table 1.16.12. Timing characteristics of detecting the start condition and the stop condition (Note1)

3 to 6 cycles < duration for setting-up (Note2)
3 to 6 cycles < duration for holding (Note2)

Note 1: When the start/stop condition control bit SHTC is "1".

Note 2: "Cycles" is in terms of the input oscillation frequency f(XIN) of the main clock.

	Duration for setting up	Duration for holding	1 1 1 1
SCL			
SDA (Start condition)			1 1 1 1 1
SDA (Stop condition)			1

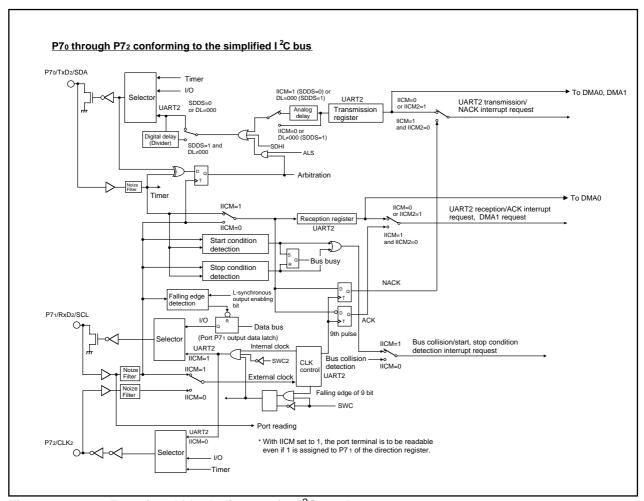


Figure 1.16.30. Functional block diagram for I²C mode

Functions available in I²C mode are shown in Figure 1.16.30 — a functional block diagram.

Bit 3 of the UART2 special mode register 2 (address 037616) is used as the SDA output stop bit. Setting this bit to "1" causes an arbitration loss to occur, and the SDA pin turns to high-impedance state at the instant when the arbitration lost detecting flag is set to "1".

Bit 1 of the UART2 special mode register 2 (address 037616) is used as the clock synchronization bit. With this bit set to "1" at the time when the internal SCL is set to "H", the internal SCL turns to "L" if the falling edge is found in the SCL pin; and the baud rate generator reloads the set value, and start counting within the "L" interval. When the internal SCL changes from "L" to "H" with the SCL pin set to "L", stops counting the baud rate generator, and starts counting it again when the SCL pin turns to "H". Due to this function, the UART2 transmission-reception clock becomes the logical product of the signal flowing through the internal SCL and that flowing through the SCL pin. This function operates over the period from the moment earlier by a half cycle than falling edge of the UART2 first clock to the rising edge of the ninth bit. To use this function, choose the internal clock for the transfer clock.

Bit 2 of the UART2 special mode register 2 (037616) is used as the SCL wait output bit. Setting this bit to "1" causes the SCL pin to be fixed to "L" at the falling edge of the ninth bit of the clock. Setting this bit to "0" frees the output fixed to "L".



Bit 4 of the UART2 special mode register 2 (address 037616) is used as the UART2 initialization bit. Setting this bit to "1", and when the start condition is detected, the microcomputer operates as follows.

- (1) The transmission shift register is initialized, and the content of the transmission register is transferred to the transmission shift register. This starts transmission by dealing with the clock entered next as the first bit. The UART2 output value, however, doesn't change until the first bit data is output after the entrance of the clock, and remains unchanged from the value at the moment when the microcomputer detected the start condition.
- (2) The reception shift register is initialized, and the microcomputer starts reception by dealing with the clock entered next as the first bit.
- (3) The SCL wait output bit turns to "1". This turns the SCL pin to "L" at the falling edge of the ninth bit of the clock.

Starting to transmit/receive signals to/from UART2 using this function doesn't change the value of the transmission buffer empty flag. To use this function, choose the external clock for the transfer clock. Bit 5 of the UART2 special mode register 2 (037616) is used as the SCL pin wait output bit 2. Setting this bit to "1" with the serial I/O specified allows the user to forcibly output an "1" from the SCL pin even if UART2 is in operation. Setting this bit to "0" frees the "L" output from the SCL pin, and the UART2 clock is input/output.

Bit 6 of the UART2 special mode register 2 (037616) is used as the SDA output disable bit. Setting this bit to "1" forces the SDA pin to turn to the high-impedance state. Refrain from changing the value of this bit at the rising edge of the UART2 transfer clock. There can be instances in which arbitration lost detecting flag is turned on.



S I/O3, 4

S I/O3 and S I/O4 are exclusive clock-synchronous serial I/Os.

Figure 1.16.31 shows the S I/O3, 4 block diagram, and Figure 1.16.32 shows the S I/O3, 4 related register. Table 1.16.13 shows the specifications of S I/O3, 4.

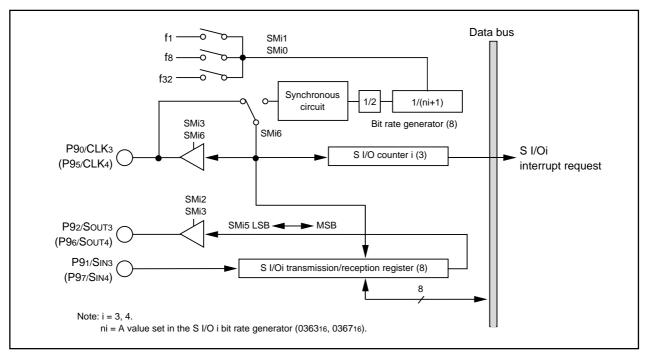


Figure 1.16.31. S I/O3, 4 block diagram

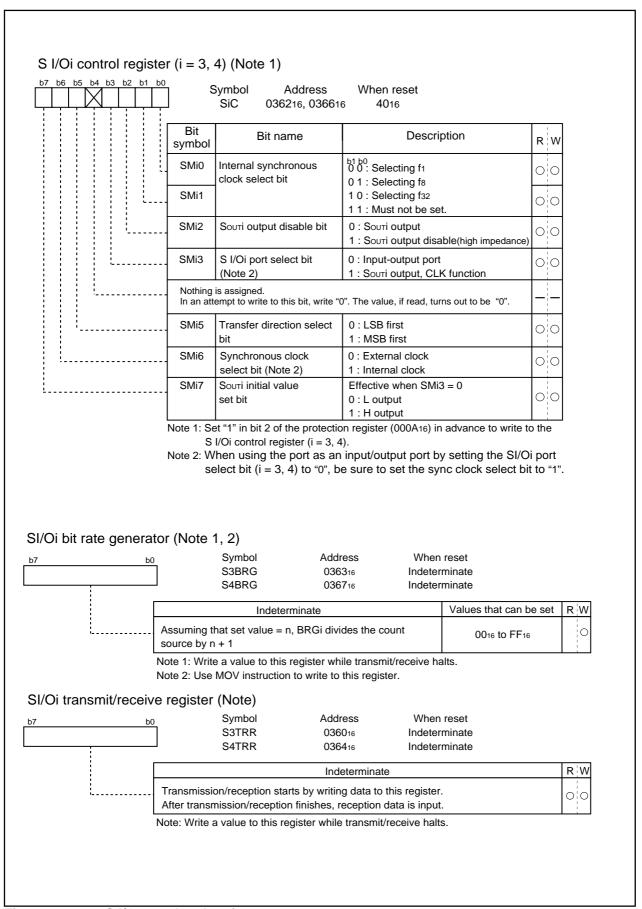


Figure 1.16.32. S I/O3, 4 related register

Table 1.16.13. Specifications of S I/O3, 4

Item	Specifications
Transfer data format	Transfer data length: 8 bits
Transfer clock	• With the internal clock selected (bit 6 of 036216, 036616 = "1"): f1/2(ni+1),
	f8/2(ni+1), f32/2(ni+1) (Note 1)
	• With the external clock selected (bit 6 of 036216, 036616 = 0):Input from the CLKi terminal (Note 2)
Conditions for	To start transmit/reception, the following requirements must be met:
transmission/	- Select the synchronous clock (use bit 6 of 036216, 036616).
reception start	Select a frequency dividing ratio if the internal clock has been selected (use bits
	0 and 1 of 036216, 036616).
	- So∪Ti initial value set bit (use bit 7 of 036216, 036616)= 1.
	- S I/Oi port select bit (bit 3 of 036216, 036616) = 1.
	- Select the transfer direction (use bit 5 of 036216, 036616)
	-Write transfer data to SI/Oi transmit/receive register (036016, 036416)
	To use S I/Oi interrupts, the following requirements must be met:
	- Clear the SI/Oi interrupt request bit before writing transfer data to the SI/Oi
	transmit/receive register (bit 3 of 004916 , 004816) = 0.
Interrupt request	Rising edge of the last transfer clock. (Note 3)
generation timing	
Select function	LSB first or MSB first selection
	Whether transmission/reception begins with bit 0 (LSB) or bit 7 (MSB) can be selected.
	Function for setting an So∪Ti initial value selection
	When using an external clock for the transfer clock, the user can choose the
	SOUTI pin output level during a non-transfer time. For details on how to set, see Figure 1.16.33.
Precaution	• Unlike UART0–2, SI/Oi (i = 3, 4) is not divided for transfer register and buffer.
	Therefore, do not write the next transfer data to the SI/Oi transmit/receive register
	(addresses 036016, 036416) during a transfer.
	• When the internal clock is selected for the transfer clock, Souti holds the last data
	for a 1/2 transfer clock period after it finished transferring and then goes to a high-
	impedance state. However, if the transfer data is written to the SI/Oi transmit/
	receive register (addresses 036016, 036416) during this time, Souti is placed in
	the high-impedance state immediately upon writing and the data hold time is
	thereby reduced.
	ĺ

Note 1: n is a value from 0016 through FF16 set in the S I/Oi bit rate generator (i = 3, 4).

Note 2: With the external clock selected:

- Before data can be written to the SI/Oi transmit/receive register (addresses 036016, 036416), the CLKi pin input must be in the high state. Also, before rewriting the SI/Oi Control Register (addresses 036216, 036616)'s bit 7 (SOUTi initial value set bit), make sure the CLKi pin input is held high.
- The S I/Oi circuit keeps on with the shift operation as long as the synchronous clock is entered in it, so stop the synchronous clock at the instant when it counts to eight. The internal clock, if selected, automatically stops.

Note 3: If the internal clock is used for the synchronous clock, the transfer clock signal stops at the "H" state.



■ Functions for setting an Souti initial value

When using an external clock for the transfer clock, the SOUTi pin output level during a non-transfer time can be set to the high or the low state. Figure 1.16.33 shows the timing chart for setting an SOUTi initial value and how to set it.

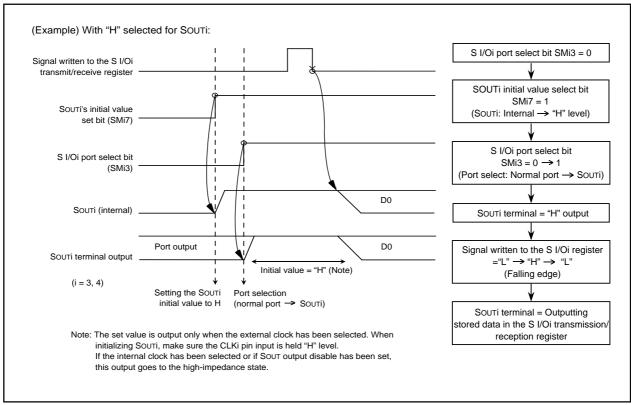


Figure 1.16.33. Timing chart for setting Souti's initial value and how to set it

■ S I/Oi operation timing

Figure 1.16.34 shows the S I/Oi operation timing

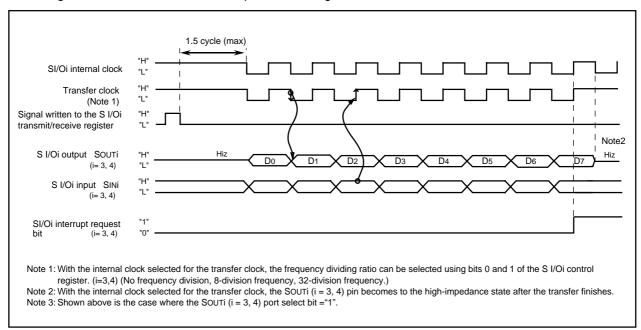


Figure 1.16.34. S I/Oi operation timing chart



A-D Converter

The A-D converter consists of one 10-bit successive approximation A-D converter circuit with a capacitive coupling amplifier. Pins P100 to P107, P95, and P96 also function as the analog signal input pins. The direction registers of these pins for A-D conversion must therefore be set to input. The Vref connect bit (bit 5 at address 03D716) can be used to isolate the resistance ladder of the A-D converter from the reference voltage input pin (VREF) when the A-D converter is not used. Doing so stops any current flowing into the resistance ladder from VREF, reducing the power dissipation. When using the A-D converter, start A-D conversion only after setting bit 5 of 03D716 to connect VREF. The result of A-D conversion is stored in the A-D registers of the selected pins. When set to 10-bit precision, the low 8 bits are stored in the even addresses and the high 2 bits in the odd addresses. When set to 8-bit precision, the low 8 bits are stored in the even addresses.

Table 1.17.1 shows the performance of the A-D converter. Figure 1.17.1 shows the block diagram of the A-D converter, and Figures 1.17.2 and 1.17.3 show the A-D converter-related registers.

Table 1.17.1. Performance of A-D converter

Item	Performance				
Method of A-D conversion	Successive approximation (capacitive coupling amplifier)				
Analog input voltage (Note 1)	0V to AVcc (Vcc)				
Operating clock \$\phiAD\$ (Note 2)	VCC = 5V fAD/divide-by-2 of fAD/divide-by-4 of fAD, fAD=f(XIN)				
	VCC = 3V divide-by-2 of fAD/divide-by-4 of fAD, fAD=f(XIN)				
Resolution	-bit or 10-bit (selectable)				
Absolute precision	Vcc = 5V • Without sample and hold function				
	±3LSB				
	 With sample and hold function (8-bit resolution) 				
	±2LSB				
	 With sample and hold function (10-bit resolution) 				
	ANo to AN7 input: ±3LSB				
	ANEX0 and ANEX1 input (including mode in which external				
	operation amp is connected): ±7LSB				
	Vcc = 3V • Without sample and hold function (8-bit resolution)				
	±2LSB				
Operating modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0,				
	and repeat sweep mode 1				
Analog input pins	8pins (ANo to AN7) + 2pins (ANEXO and ANEX1)				
A-D conversion start condition	Software trigger				
	A-D conversion starts when the A-D conversion start flag changes to "1"				
	External trigger (can be retriggered)				
	A-D conversion starts when the A-D conversion start flag is "1" and the				
	ADTRG/P97 input changes from "H" to "L"				
Conversion speed per pin	Without sample and hold function				
	8-bit resolution: 49 φAD cycles, 10-bit resolution: 59 φAD cycles				
	With sample and hold function				
	8-bit resolution: 28 \$\phiAD\$ cycles, 10-bit resolution: 33 \$\phiAD\$ cycles				

Note 1: Does not depend on use of sample and hold function.

Note 2: Divide the frequency if f(XIN) exceeds 10MHz, and make φAD frequency equal to or less than 10MHz. Without sample and hold function, set the φAD frequency to 250kHz min.

With the sample and hold function, set the φAD frequency to 1MHz min.



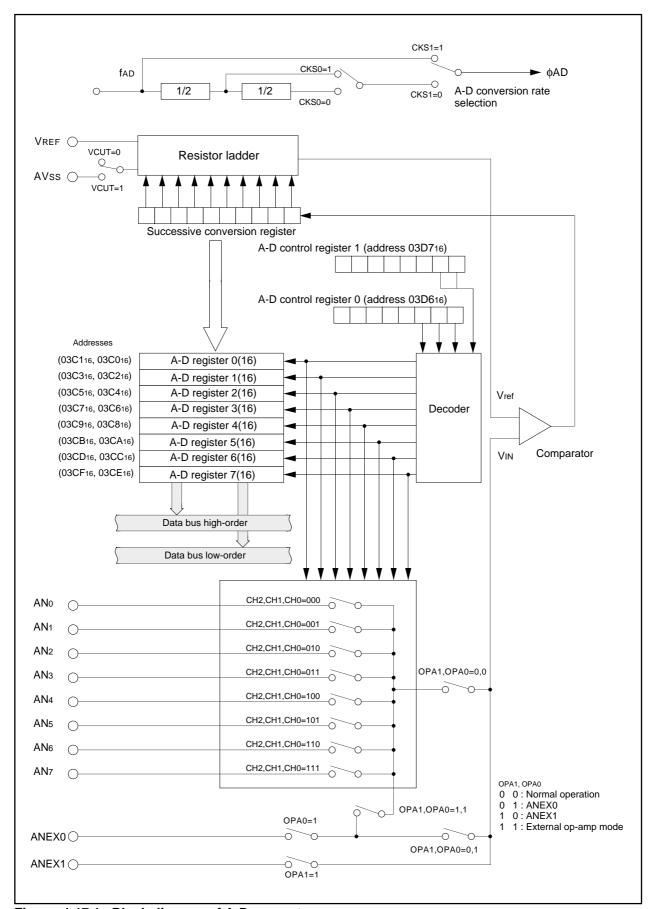


Figure 1.17.1. Block diagram of A-D converter

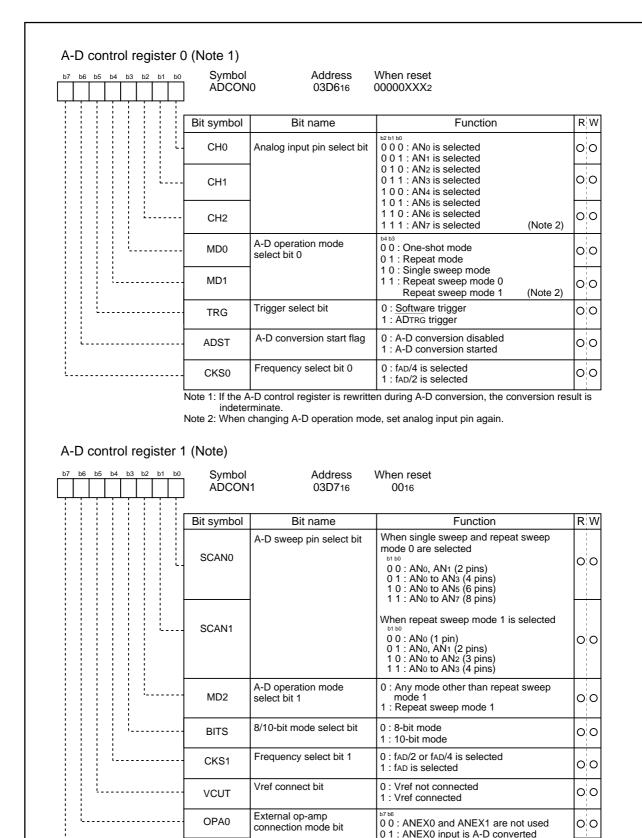


Figure 1.17.2. A-D converter-related registers (1)



Note: If the A-D control register is rewritten during A-D conversion, the conversion result is

1 0 : ANEX1 input is A-D converted

1 1: External op-amp connection mode

00

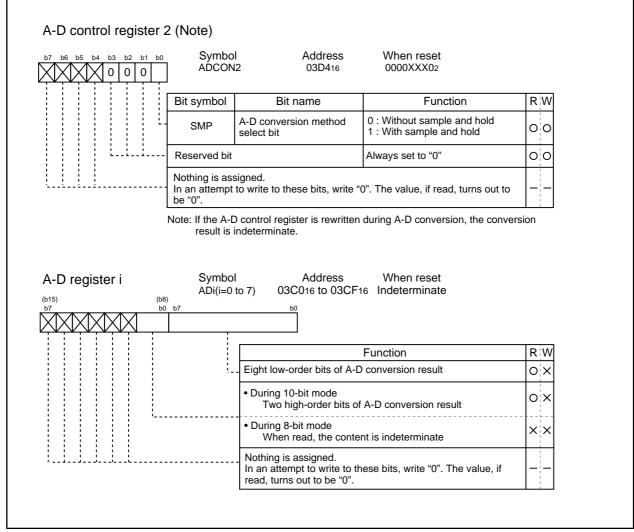


Figure 1.17.3. A-D converter-related registers (2)

(1) One-shot mode

In one-shot mode, the pin selected using the analog input pin select bit is used for one-shot A-D conversion. Table 1.17.2 shows the specifications of one-shot mode. Figure 1.17.4 shows the A-D control register in one-shot mode.

Table 1.17.2. One-shot mode specifications

	•	
Item	Specification	
Function	The pin selected by the analog input pin select bit is used for one A-D conversion	
Start condition	Writing "1" to A-D conversion start flag	
Stop condition	• End of A-D conversion (A-D conversion start flag changes to "0", except	
	when external trigger is selected)	
	Writing "0" to A-D conversion start flag	
Interrupt request generation timing	End of A-D conversion	
Input pin	One of ANo to AN7, as selected	
Reading of result of A-D converter	Read A-D register corresponding to selected pin	

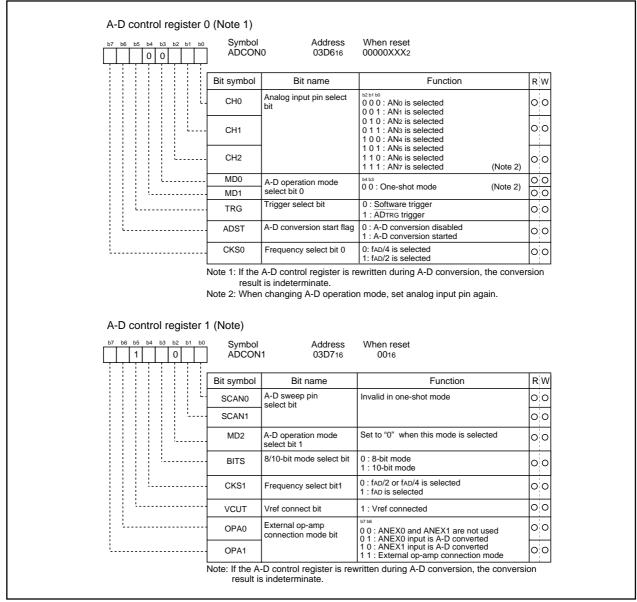


Figure 1.17.4. A-D conversion register in one-shot mode



(2) Repeat mode

In repeat mode, the pin selected using the analog input pin select bit is used for repeated A-D conversion. Table 1.17.3 shows the specifications of repeat mode. Figure 1.17.5 shows the A-D control register in repeat mode.

Table 1.17.3. Repeat mode specifications

Item	Specification
Function	The pin selected by the analog input pin select bit is used for repeated A-D conversion
Star condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	One of ANo to AN7, as selected
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

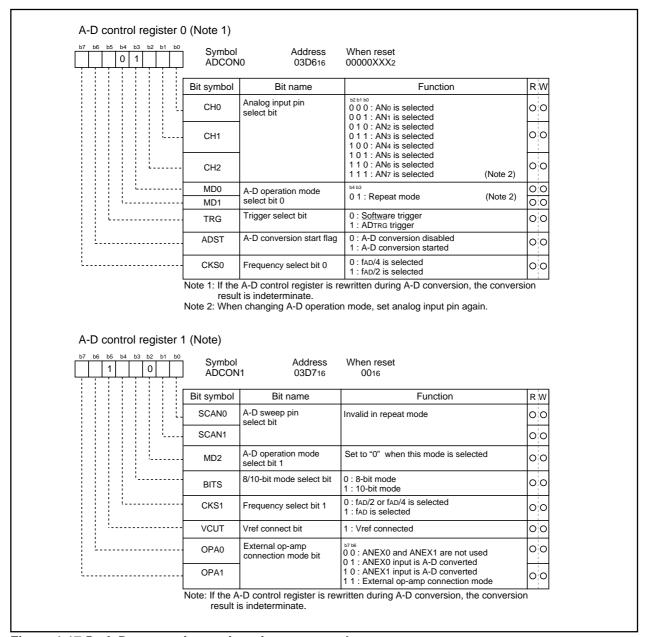


Figure 1.17.5. A-D conversion register in repeat mode

(3) Single sweep mode

In single sweep mode, the pins selected using the A-D sweep pin select bit are used for one-by-one A-D conversion. Table 1.17.4 shows the specifications of single sweep mode. Figure 1.17.6 shows the A-D control register in single sweep mode.

Table 1.17.4. Single sweep mode specifications

Item	Specification	
Function	The pins selected by the A-D sweep pin select bit are used for one-by-one A-D conversion	
Start condition	Writing "1" to A-D converter start flag	
Stop condition	End of A-D conversion (A-D conversion start flag changes to "0", except	
	when external trigger is selected)	
	Writing "0" to A-D conversion start flag	
Interrupt request generation timing	End of A-D conversion	
Input pin	ANo and AN1 (2 pins), ANo to AN3 (4 pins), ANo to AN5 (6 pins), or ANo to AN7 (8 pins)	
Reading of result of A-D converter	Read A-D register corresponding to selected pin	

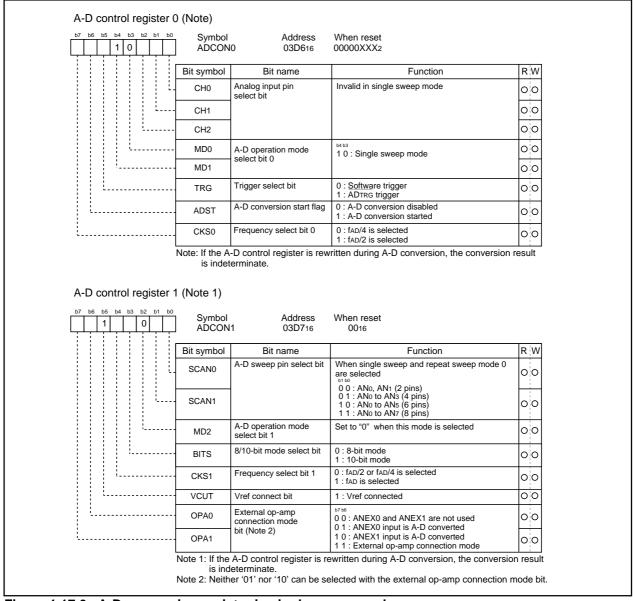


Figure 1.17.6. A-D conversion register in single sweep mode



(4) Repeat sweep mode 0

In repeat sweep mode 0, the pins selected using the A-D sweep pin select bit are used for repeat sweep A-D conversion. Table 1.17.5 shows the specifications of repeat sweep mode 0. Figure 1.17.7 shows the A-D control register in repeat sweep mode 0.

Table 1.17.5. Repeat sweep mode 0 specifications

Item	Specification
Function	The pins selected by the A-D sweep pin select bit are used for repeat A-D conversion
Start condition	Writing "1" to A-D conversion start flag
Stop condition	Writing "0" to A-D conversion start flag
Interrupt request generation timing	None generated
Input pin	ANo and AN1 (2 pins), ANo to AN3 (4 pins), ANo to AN5 (6 pins), or ANo to AN7 (8 pins)
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)

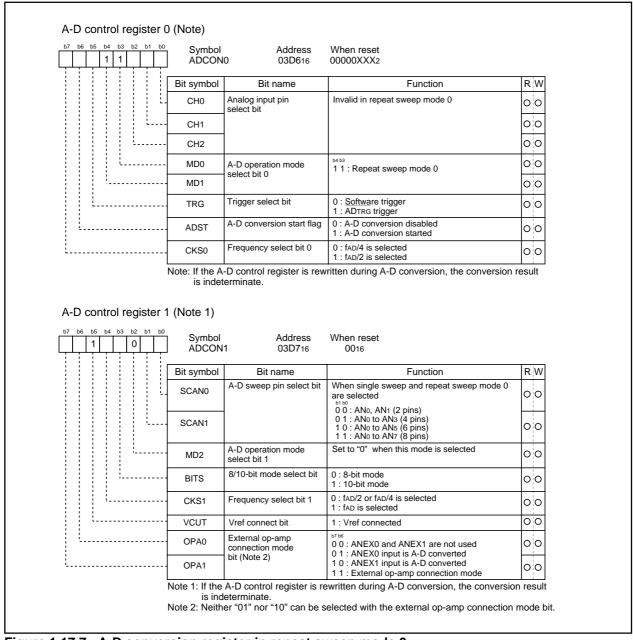


Figure 1.17.7. A-D conversion register in repeat sweep mode 0

(5) Repeat sweep mode 1

In repeat sweep mode 1, all pins are used for A-D conversion with emphasis on the pin or pins selected using the A-D sweep pin select bit. Table 1.17.6 shows the specifications of repeat sweep mode 1. Figure 1.17.8 shows the A-D control register in repeat sweep mode 1.

Table 1.17.6. Repeat sweep mode 1 specifications

Item	Specification							
Function	All pins perform repeat A-D conversion, with emphasis on the pin or pins							
	selected by the A-D sweep pin select bit							
	ample : AN₀ selected AN₀ → AN₁ → AN₀ → AN₂ → AN₀ → AN₃, etc							
Start condition	Vriting "1" to A-D conversion start flag							
Stop condition	Writing "0" to A-D conversion start flag							
Interrupt request generation timing	None generated							
Input pin	With emphasis on these pins; ANo (1 pin), ANo and AN1 (2 pins),							
	ANo to AN2 (3 pins), ANo to AN3 (4 pins)							
Reading of result of A-D converter	Read A-D register corresponding to selected pin (at any time)							

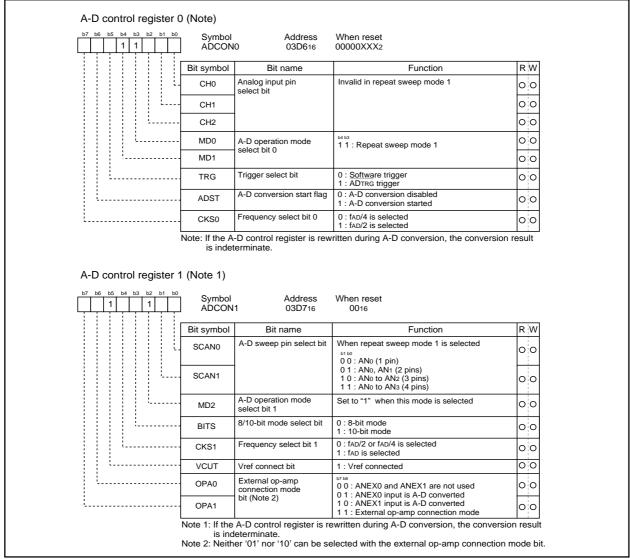


Figure 1.17.8. A-D conversion register in repeat sweep mode 1



(a) Sample and hold

Sample and hold is selected by setting bit 0 of the A-D control register 2 (address 03D416) to "1". When sample and hold is selected, the rate of conversion of each pin increases. As a result, a 28 \$\phiAD\$ cycle is achieved with 8-bit resolution and 33 \$\phiAD\$ with 10-bit resolution. Sample and hold can be selected in all modes. However, in all modes, be sure to specify before starting A-D conversion whether sample and hold is to be used.

(b) Extended analog input pins

In one-shot mode and repeat mode, the input via the extended analog input pins ANEX0 and ANEX1 can also be converted from analog to digital.

When bit 6 of the A-D control register 1 (address 03D716) is "1" and bit 7 is "0", input via ANEX0 is converted from analog to digital. The result of conversion is stored in A-D register 0.

When bit 6 of the A-D control register 1 (address 03D716) is "0" and bit 7 is "1", input via ANEX1 is converted from analog to digital. The result of conversion is stored in A-D register 1.

(c) External operation amp connection mode

In this mode, multiple external analog inputs via the extended analog input pins, ANEX0 and ANEX1, can be amplified together by just one operation amp and used as the input for A-D conversion.

When bit 6 of the A-D control register 1 (address 03D716) is "1" and bit 7 is "1", input via ANo to AN7 is output from ANEX0. The input from ANEX1 is converted from analog to digital and the result stored in the corresponding A-D register. The speed of A-D conversion depends on the response of the external operation amp. Do not connect the ANEX0 and ANEX1 pins directly. Figure 1.17.9 is an example of how to connect the pins in external operation amp mode.

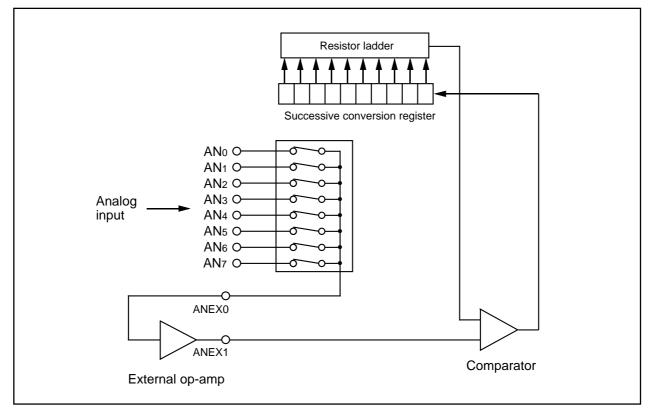


Figure 1.17.9. Example of external op-amp connection mode



D-A Converter

This is an 8-bit, R-2R type D-A converter. The microcomputer contains two independent D-A converters of this type.

D-A conversion is performed when a value is written to the corresponding D-A register. Bits 0 and 1 (D-A output enable bits) of the D-A control register decide if the result of conversion is to be output. Do not set the target port to output mode if D-A conversion is to be performed. When the D-A output is enabled, the pull-up function of the corresponding port is automatically disabled.

Output analog voltage (V) is determined by a set value (n : decimal) in the D-A register.

V = VREF X n / 256 (n = 0 to 255)

VREF: reference voltage

Table 1.18.1 lists the performance of the D-A converter. Figure 1.18.1 shows the block diagram of the D-A converter. Figure 1.18.2 shows the D-A converter equivalent circuit.

Table 1.18.1. Performance of D-A converter

Item	Performance
Conversion method	R-2R method
Resolution	8 bits
Analog output pin	2 channels

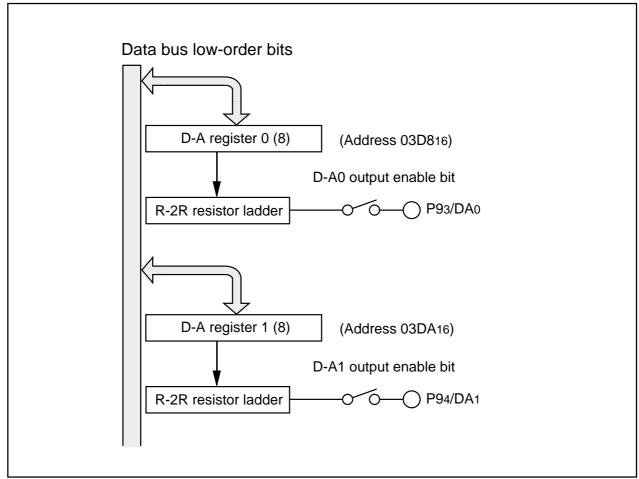


Figure 1.18.1. Block diagram of D-A converter



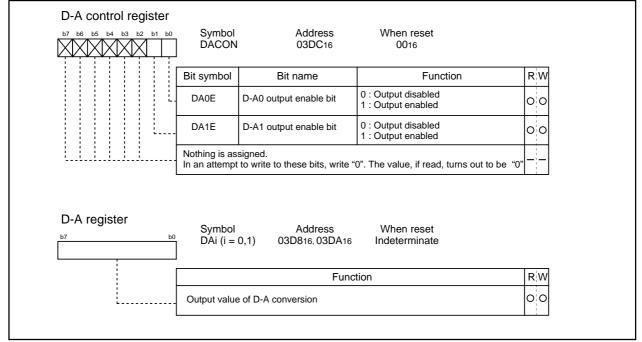


Figure 1.18.2. D-A control register

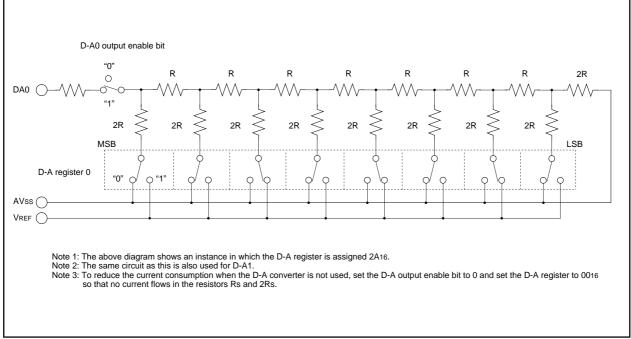


Figure 1.18.3. D-A converter equivalent circuit

CRC Calculation Circuit

The Cyclic Redundancy Check (CRC) calculation circuit detects an error in data blocks. The microcomputer uses a generator polynomial of CRC_CCITT ($X^{16} + X^{12} + X^5 + 1$) to generate CRC code.

The CRC code is a 16-bit code generated for a block of a given data length in multiples of 8 bits. The CRC code is set in a CRC data register each time one byte of data is transferred to a CRC input register after writing an initial value into the CRC data register. Generation of CRC code for one byte of data is completed in two machine cycles.

Figure 1.19.1 shows the block diagram of the CRC circuit. Figure 1.19.2 shows the CRC-related registers. Figure 1.19.3 shows the calculation example using the CRC calculation circuit.

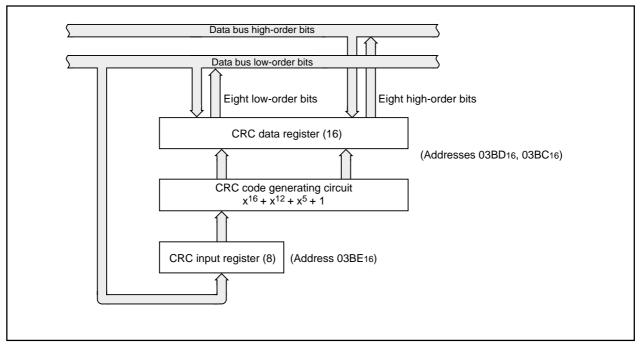


Figure 1.19.1. Block diagram of CRC circuit

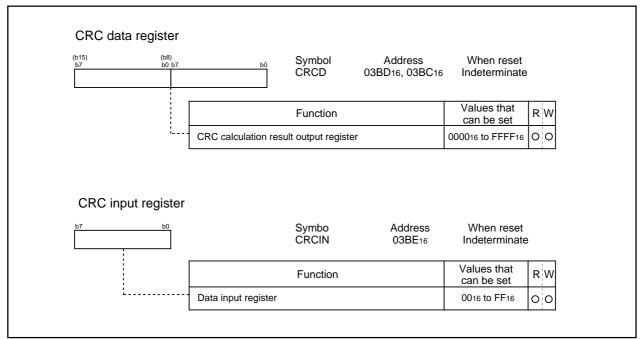


Figure 1.19.2. CRC-related registers



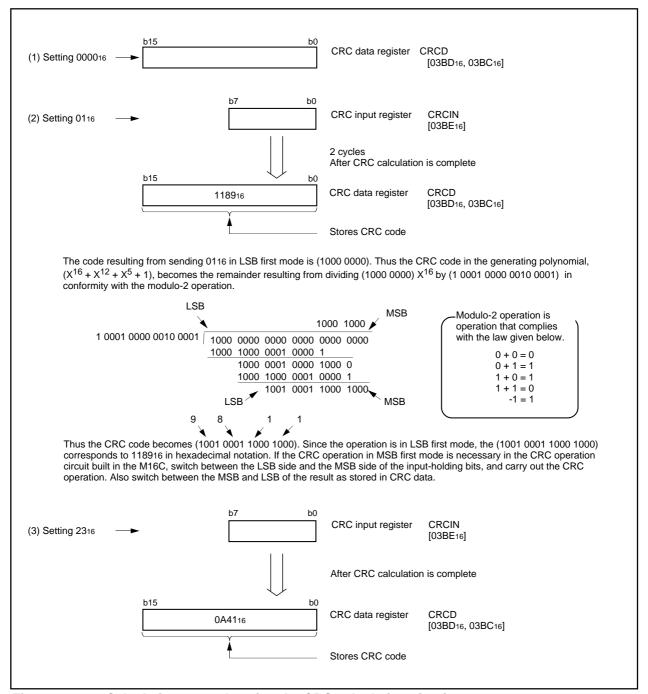


Figure 1.19.3. Calculation example using the CRC calculation circuit

Programmable I/O Ports

There are 87 programmable I/O ports: P0 to P10 (excluding P85). Each port can be set independently for input or output using the direction register. A pull-up resistance for each block of 4 ports can be set. P85 is an input-only port and has no built-in pull-up resistance.

Figures 1.20.1 to 1.20.4 show the programmable I/O ports. Figure 1.20.5 shows the I/O pins.

Each pin functions as a programmable I/O port and as the I/O for the built-in peripheral devices.

To use the pins as the inputs for the built-in peripheral devices, set the direction register of each pin to input mode. When the pins are used as the outputs for the built-in peripheral devices (other than the D-A converter), they function as outputs regardless of the contents of the direction registers. When pins are to be used as the outputs for the D-A converter, do not set the direction registers to output mode. See the descriptions of the respective functions for how to set up the built-in peripheral devices.

(1) Direction registers

Figure 1.20.6 shows the direction registers.

These registers are used to choose the direction of the programmable I/O ports. Each bit in these registers corresponds one for one to each I/O pin.

In memory expansion and microprocessor mode, the contents of corresponding direction register of pins A₀ to A₁₉, D₀ to D₁₅, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{RD}}$, $\overline{\text{WRL/WR}}$, $\overline{\text{WRH/BHE}}$, ALE, $\overline{\text{RDY}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and BCLK cannot be modified.

Note: There is no direction register bit for P85.

(2) Port registers

Figure 1.20.7 shows the port registers.

These registers are used to write and read data for input and output to and from an external device. A port register consists of a port latch to hold output data and a circuit to read the status of a pin. Each bit in port registers corresponds one for one to each I/O pin.

In memory expansion and microprocessor mode, the contents of corresponding port register of pins A₀ to A₁₉, D₀ to D₁₅, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{RD}}$, $\overline{\text{WRL/WR}}$, $\overline{\text{WRH/BHE}}$, ALE, $\overline{\text{RDY}}$, $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and BCLK cannot be modified.

(3) Pull-up control registers

Figure 1.20.8 shows the pull-up control registers.

The pull-up control register can be set to apply a pull-up resistance to each block of 4 ports. When ports are set to have a pull-up resistance, the pull-up resistance is connected only when the direction register is set for input.

However, in memory expansion mode and microprocessor mode, the pull-up control register of P0 to P3, P40 to P43, and P5 is invalid. The contents of register can be changed, but the pull-up resistance is not connected.

(4) Port control register

Figure 1.20.9 shows the port control register.

The bit 0 of port control register is used to read port P1 as follows:

- 0 : When port P1 is input port, port input level is read.When port P1 is output port , the contents of port P1 register is read.
- 1: The contents of port P1 register is read always.

This register is valid in the following:

- External bus width is 8 bits in microprocessor mode or memory expansion mode.
- Port P1 can be used as a port in multiplexed bus for the entire space.



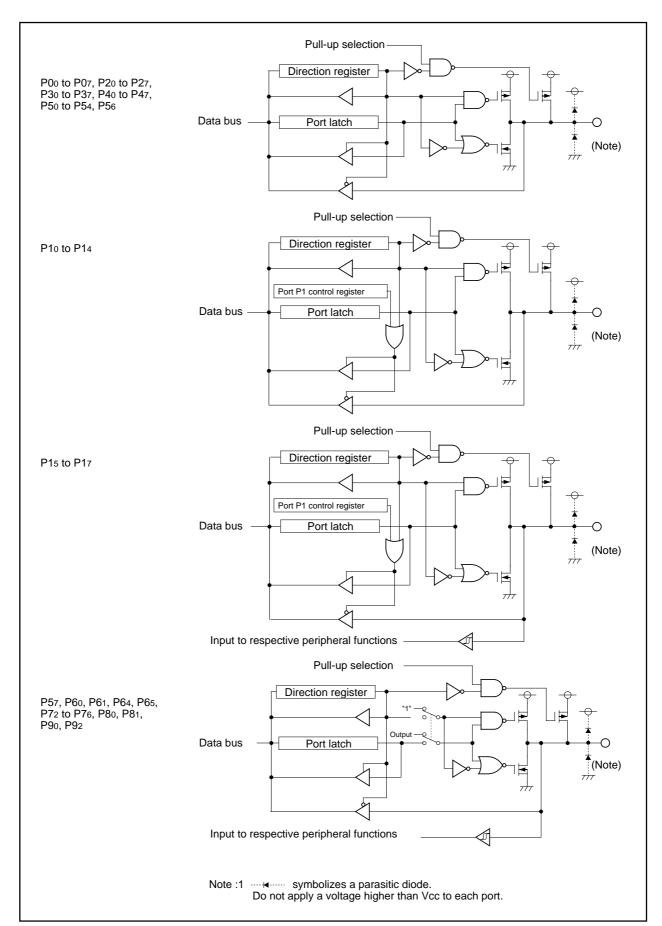


Figure 1.20.1. Programmable I/O ports (1)

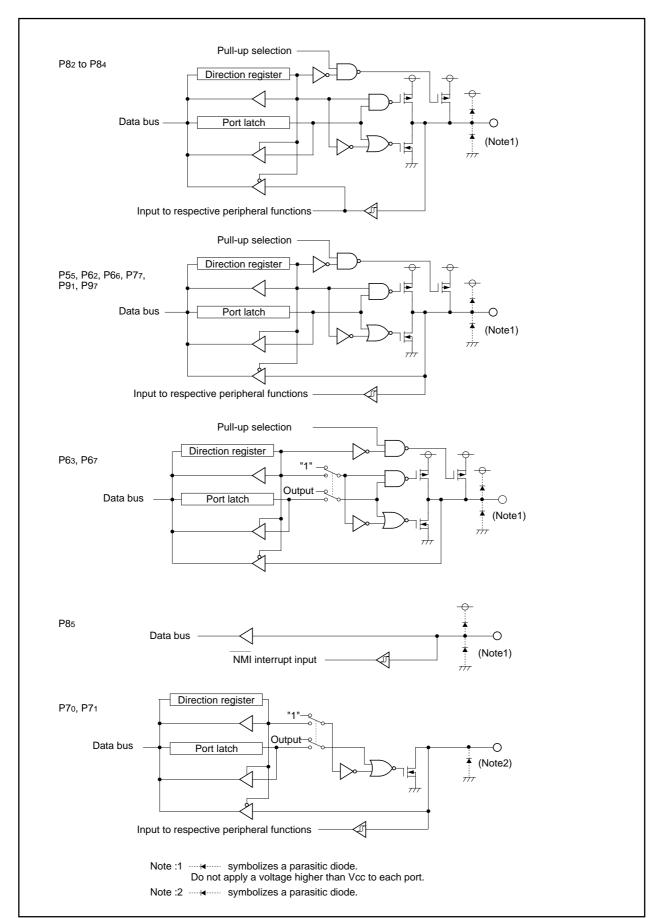


Figure 1.20.2. Programmable I/O ports (2)



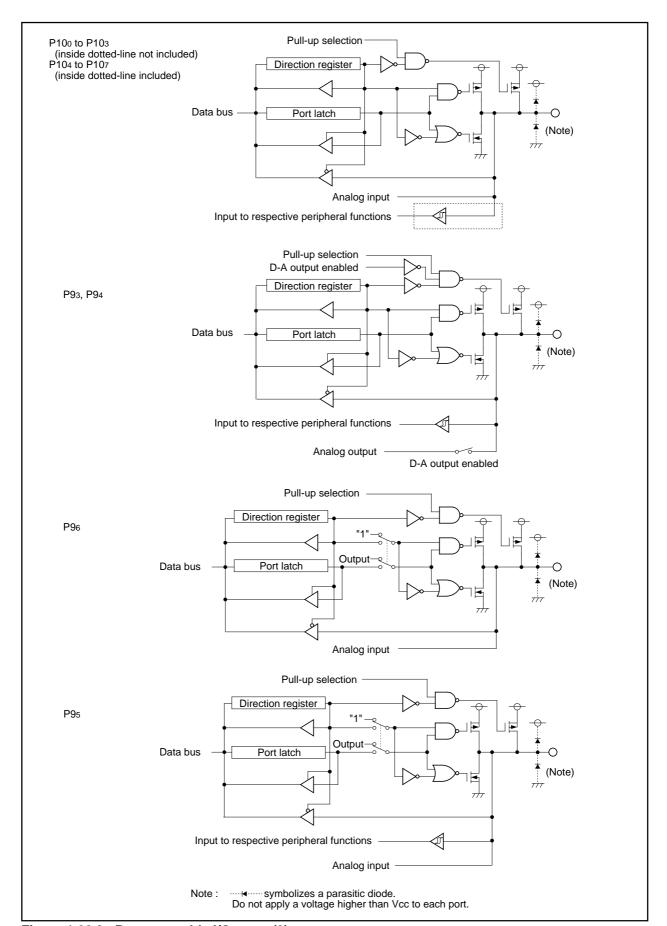


Figure 1.20.3. Programmable I/O ports (3)

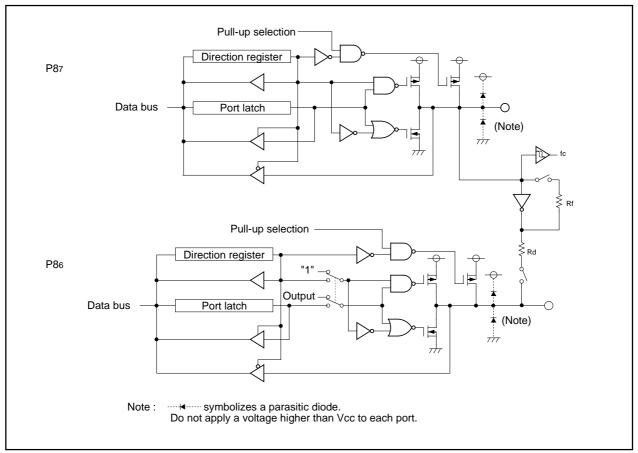


Figure 1.20.4. Programmable I/O ports (4)

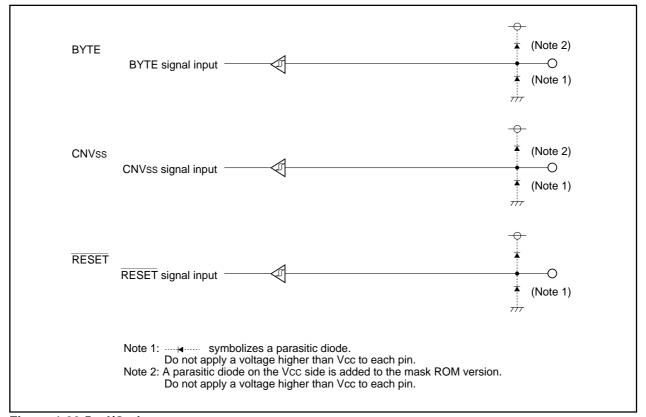


Figure 1.20.5. I/O pins



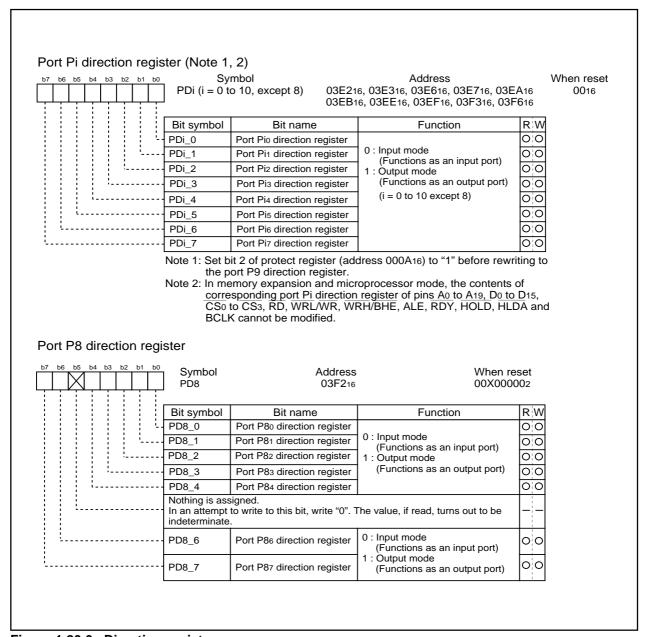


Figure 1.20.6. Direction register

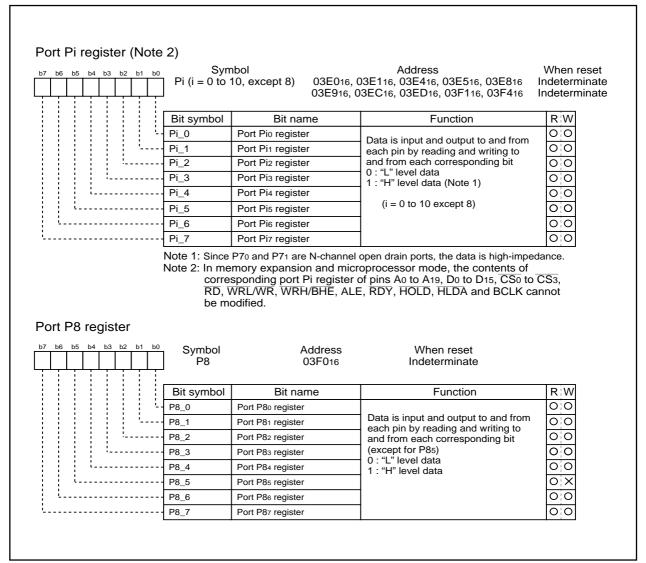


Figure 1.20.7. Port register

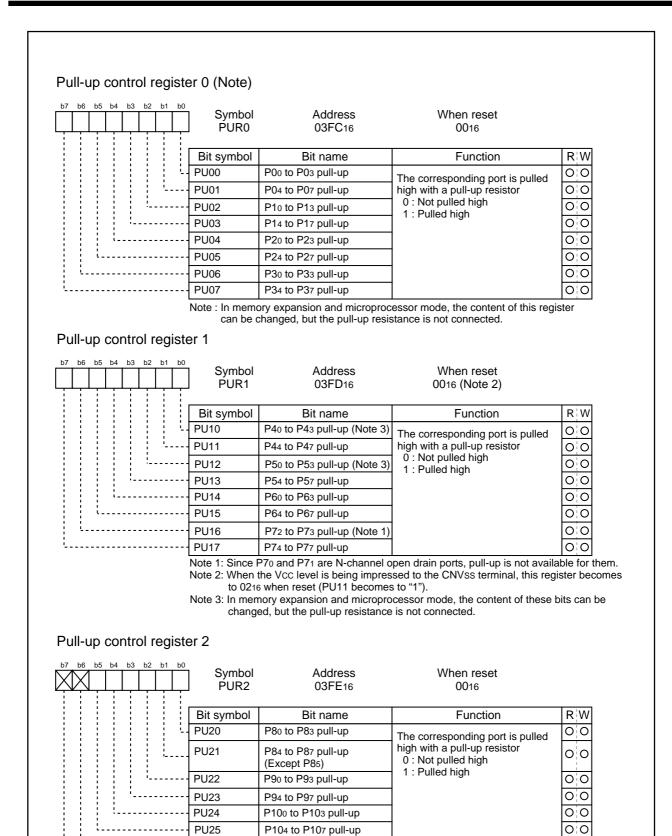


Figure 1.20.8. Pull-up control register

In an attempt to write to these bits, write "0". The value, if read, turns out to be "0".

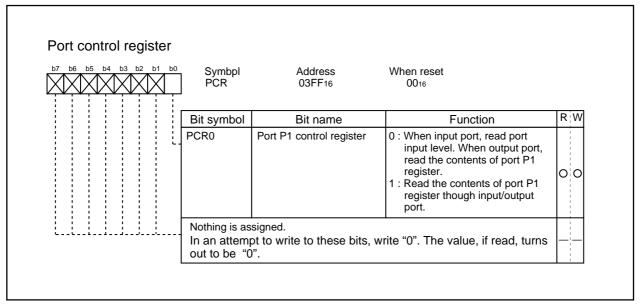


Figure 1.20.9. Port control register

Table 1.20.1. Example connection of unused pins in single-chip mode

Pin name	Connection			
Ports P0 to P10 (excluding P85)	After setting for input mode, connect every pin to Vss via a resistor (pull-down); or after setting for output mode, leave these pins open.			
XOUT (Note)	Open			
NMI	Connect via resistor to Vcc (pull-up)			
AVcc	Connect to Vcc			
AVSS, VREF, BYTE	Connect to VSS			

Note: With external clock input to XIN pin.

Table 1.20.2. Example connection of unused pins in memory expansion mode and microprocessor mode

Pin name	Connection
Ports P6 to P10 (excluding P85)	After setting for input mode, connect every pin to Vss via a resistor (pull-down); or after setting for output mode, leave these pins open.
P45 / CS1 to P47 / CS3	Set ports to input mode, set output enable bits of $\overline{\text{CS1}}$ through $\overline{\text{CS3}}$ to 0, and connect to Vcc via resistors (pull-up).
BHE, ALE, HLDA, XOUT (Note 1), BCLK (Note 2)	Open
HOLD, RDY, NMI	Connect via resistor to Vcc (pull-up)
AVCC	Connect to Vcc
AVSS, VREF	Connect to Vss

Note 1: With external clock input to XIN pin.

Note 2: When the BCLK output disable bit (bit 7 at address 000416) is set to "1", connect to Vcc via a resistor (pull-up).

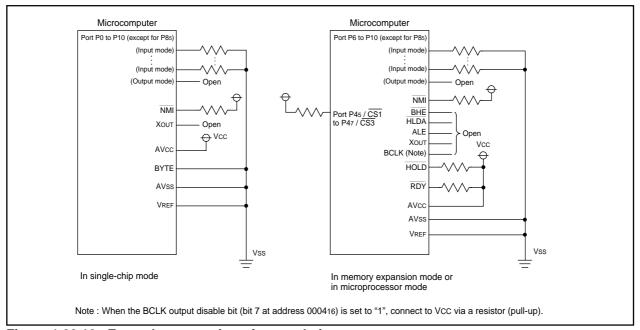


Figure 1.20.10. Example connection of unused pins



Items to be submitted when ordering masked ROM version

Please submit the following when ordering masked ROM products:

- (1) Mask ROM confirmation form
- (2) Mark specification sheet
- (3) ROM data: Floppy disks *



^{*: 3.5-}inch double-sided high-density disk (IBM format) is required per pattern.

Table 1.23.1. Absolute maximum ratings

Symbol		Parameter	Condition	Rated value	Unit
Vcc	Supply volta	age	Vcc=AVcc	-0.3 to 6.5	V
AVcc	Analog supp	oly voltage	Vcc=AVcc	-0.3 to 6.5	V
Vı	Input voltage	RESET, CNVss, BYTE, P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P87, P90 to P97, P100 to P107, VREF, XIN		-0.3 to Vcc+0.3	V
		P70, P71		-0.3 to 6.5	V
Vo	Output voltage	P00 to P07, P10 to P17, P20 to P27, P30 to P37,P40 to P47, P50 to P57, P60 to P67,P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107, XOUT		-0.3 to Vcc+0.3	V
		P70, P71		-0.3 to 6.5	V
Pd	Power dissi	Power dissipation		300	mW
Topr	Operating a	Operating ambient temperature		-20 to 85 / -40 to 85 (Note)	O _°
Tstg	Storage tem	Storage temperature		-65 to 150	°C

Note: Specify a product of -40°C to 85°C to use it.

Table 1.23.2. Recommended operating conditions (referenced to VCC = 2.7V to 5.5V at Topr = -20° C to 85° C (Note 3) unless otherwise specified)

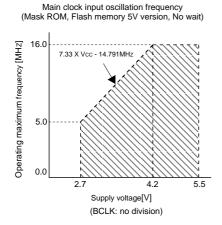
0					Standard				
Symbol	Parameter					Min	Typ.	Max.	Unit
Vcc	Supply volt	tage				2.7	5.0	5.5	V
AVcc	Analog sur	nalog supply voltage					Vcc		V
Vss		Supply voltage					0		V
AVss	Analog sup	g supply voltage					0		V
Vih	HIGH input voltage	P72 to P77.	P31 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P72, P80 to P87, P90 to P97, P100 to P107, XIN, RESET, CNVss, BYTE			0.8Vcc		Vcc	٧
		P70,P71				0.8Vcc		6.5	V
		P00 to P07,	P10 to P17, P	20 to P27, P30 (during	single-chip mode)	0.8Vcc		Vcc	V
				220 to P27, P30 emory expansion and m	croprocessor modes)	0.5Vcc		Vcc	V
VIL	LOW input voltage	P70 to P77.		P50 to P57, P60 to P67, P90 to P97, P100 to P1 TE		0		0.2Vcc	V
		P00 to P07, P10 to P17, P20 to P27, P30 (during single-chip mode)				0		0.2Vcc	V
		P0 ₀ to P0 ₇ , P1 ₀ to P1 ₇ , P2 ₀ to P2 ₇ , P3 ₀ (data input function during memory expansion and microprocessor modes)			0		0.16Vcc	V	
I _{OH (peak)}	HIGH peak current	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P72 to P77, P80 to P84, P86, P87, P90 to P97, P100 to P107				-10.0	mA		
I _{OH (avg)}	HIGH average output current		P40 to P47,	o to P07, P10 to P17, P20 to P27, P30 to P37, o to P47, P50 to P57, P60 to P67, P72 to P77, o to P84, P86, P87, P90 to P97, P100 to P107				-5.0	mA
I _{OL (peak)}	LOW peak output current		P40 to P47,	P10 to P17, P20 to P27 P50 to P57, P60 to P67 P86, P87, P90 to P97,	, P70 to P77,			10.0	mA
I _{OL (avg)}	LOW average P00 to P07, P10 to P17, P20 to P27, P30 output current P40 to P47, P50 to P57, P60 to P67, P70 P80 to P84, P86, P87, P90 to P97, P100		7, P70 to P77,			5.0	mA		
	Main clock input oscillation frequency		No wait Flash	Mask ROM version,	Vcc=4.2V to 5.5V	0		16	MHz
				Flash memory 5V version (Note 5)	Vcc=2.7V to 4.2V	0		7.33 X Vcc -14.791	MHz
f (XIN)			With wait Mask ROM version, Flash memory 5V version (Note 5)	Mask ROM version,	Vcc=4.2V to 5.5V	0		16	MHz
				Vcc=2.7V to 4.2V	0		4 X Vcc -0.8	MHz	
f (Xcin)	Subclock oscillation frequency						32.768	50	kHz

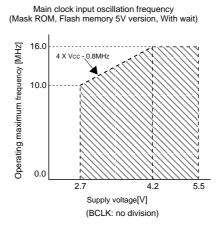
Note 1: The mean output current is the mean value within 100ms.

Note 2: The total IoL (peak) for ports P0, P1, P2, P86, P87, P9, and P10 must be 80mA max. The total IoH (peak) for ports P0, P1, P2, P86, P87, P9, and P10 must be 80mA max. The total IoL (peak) for ports P3, P4, P5, P6, P7, and P80 to P84 must be 80mA max. The total IOH (peak) for ports P3, P4, P5, P6, P72 to P77, and P80 to P84 must be 80mA max.

Note 3: Specify a product of -40°C to 85°C to use it.

Note 4: Relationship between main clock oscillation frequency and supply voltage.





Note 5: Execute case without wait, program / erase of flash memory by Vcc=4.2V to 5.5V and f(BCLK) ≤ 6.25 MHz. Execute case with wait, program / erase of flash memory by Vcc=4.2V to 5.5V and f(BCLK) ≤ 12.5 MHz.



Vcc = 5V

Table 1.23.3. A-D conversion characteristics (referenced to VCC = AVCC = VREF = 2.7V to 5.5V, Vss = AVSS = 0V at Topr = -20° C to 85° C (-40° C to 85° C (Note 4) unless otherwise specified)

	Parameter		Measuring condition		Standard			
Symbol					Min.	Тур.	Max.	Unit
-	Resolution		VREF = VCC				10	Bits
_	Absolute	Sample & hold function not available	VREF = VCC = 5V				±3	LSB
	accuracy	Sample & hold function available(10bit)	VREF =VCC = 5V	ANo to AN7 input			±3	LSB
				ANEX0, ANEX1 input, External op-amp connection mode			±7	LSB
		Sample & hold function available(8bit)	VREF = VC	c = 5V			±2	LSB
		Sample & hold function not available(8bit)	VREF = VC	$C = 3V$, $\emptyset AD = fAD/2$			±2	LSB
RLADDER	Ladder resistance		VREF = VCC		10		40	kΩ
tconv	Conversion time(10bit), Sample & hold function available		VREF = VCC = 5V, ØAD =10MHz		3.3			μs
tconv	Conversion time(8bit), Sample & hold function available		VREF = VCC = 5V, ØAD =10MHz		2.8			μs
tconv	Conversion time(8bit), Sample & hold function not available		VREF = VCC = 3V, ØAD = fAD/2 = 5MHz		9.8			μs
t SAMP	Sampling time				0.3			μs
VREF	Reference voltage				2.7		Vcc	V
VIA	Analog input voltage				0		VREF	V

- Note 1: Do f(XIN) in range of main clock input oscillation frequency prescribed with recommended operating conditions of table 1.23.2. Divide the f AD if f(XIN) exceeds 10MHz, and make AD operation clock frequency (ØAD) equal to or lower than 10MHz. And divide the f AD if VCC is less than 4.2V, and make AD operation clock frequency (ØAD) equal to or lower than f AD/2.
- Note 2: A case without sample & hold function turn AD operation clock frequency (ØAD) into 250 kHz or more in addition to a limit of Note 1.

 A case with sample & hold function turn AD operation clock frequency (ØAD) into 1MHz or more in addition to a limit of Note 1.
- Note 3: Connect AVCC pin to VCC pin and apply the same electric potential.
- Note 4: Specify a product of -40°C to 85°C to use it.

Table 1.23.4. D-A conversion characteristics (referenced to VCC = VREF = 2.7V to 5.5V, VSS = AVSS = 0V, at Topr = -20° C to 85° C (-40° C to 85° C (Note 2) unless otherwise specified)

0	D	Manager de la completa de	5	11.2		
Symbol	Parameter	Measuring condition	Min.	Тур.	Max.	Unit
-	Resolution				8	Bits
_	Absolute accuracy				1.0	%
t su	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note 1)			1.5	mA

Note 1: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "0016".

The A-D converter's ladder resistance is not included.

Also, when D-A register contents are not "00 16", the current IVREF always flows even though Vref may have been set to be unconnected by the A-D control register.

Note 2: Specify a product of -40°C to 85°C to use it.

Table 1.23.5. Flash memory version electrical characteristics

(referenced to Vcc = 4.2V to 5.5V, at Topr =0 to 60°C unless otherwise specified)

		Standard			
Parameter	Min.	Typ.	Max	Unit	
Page program time		6	120	ms	
Block erase time		50	600	ms	
Erase all unlocked blocks time		50 X n (Note)	600 X n (Note)	ms	
Lock bit program time		6	120	ms	

Note: n denotes the number of block erases.



Vcc = 5V

Table 1.23.6. Electrical characteristics (referenced to VCC = 4.2V to 5.5V, VSS = 0V at Topr = -20°C to 85°C / - 40°C to 85°C (Note 2), f(XIN) = 16MHz unless otherwise specified)

C				GOC (Note 2), f(XIN) = 16MHz un			Standard		
Symbol		Parameter		Measu	Min	Тур.	Max.	Unit	
Vон	HIGH output voltage	P60 to P67, P72	to P17, P20 to P27, to P47, P50 to P57, to P77, P80 to P84, P97, P100 to P107	Іон = -5mA	3.0			V	
Vон	HIGH output voltage	P60 to P67, P72	to P17, P20 to P27, to P47, P50 to P57, to P77, P80 to P84, P97, P100 to P107	Іон = -200μΑ	4.7			٧	
	HIGH output XOUT HIGHPOWER			IOH = -1mA		3.0			V
Vон	HIGH output XCOUT HIGHPOWE			Ioн = -0.5mA With no load app	lied	3.0	3.0		.,
	voltage	ACOUT	LOWPOWER	With no load app		1.6		V	
VoL	LOW output voltage	P00 to P07, P10 to P30 to P37, P40 to P60 to P67, P70 to P86, P87, P90 to P	P47, P50 to P57, P77, P80 to P84,	IoL = 5mA			2.0	V	
VoL	LOW output voltage	P00 to P07, P10 to P30 to P37, P40 to P60 to P67, P70 to P86, P87, P90 to F	P47, P50 to P57, P77, P80 to P84,	IoL = 200μA			0.45	V	
VoL	LOW output XOUT		HIGHPOWER	IoL = 1mA				2.0	V
	LOW output		LOWPOWER	IoL = 0.5mA With no load app	lied		0	2.0	
	voltage	Хсоит	LOWPOWER	With no load app			0		V
VT+-VT-	Hysteresis	HOLD, RDY, TAC TB0IN to TB5IN, II ADTRG, CTS0 to C CLK0 to CLK4, TA KI0 to KI3, RxD0 t	NTo to INT5, NMI, CTS2, SCL, SDA,		0.2		1.0	V	
VT+-VT-	Hysteresis	RESET			0.2		1.8	V	
Іін	HIGH input current P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, XIN, RESET, CNVss, BYTE			VI = 5V				5.0	μА
I _{IL}	LOW input current	P30 to P37, P40 to		VI = 0V			-5.0	μА	
R _{PULLUP}	Pull-up resistance	P30 to P37, P40 to P60 to P67, P72 to	P17, P20 to P27, p P47, P50 to P57, p P77, P80 to P84, P97, P100 to P107	Vi = 0V		30.0	50.0	167.0	kΩ
R _{fXIN}	Feedback re	esistance XIN					1.0		MΩ
R _{fXCIN}	Feedback re	esistance XcIN					6.0		МΩ
V _{RAM}	RAM retenti	on voltage			When clock is stopped				V
	mode, the output pins at			Mask ROM version	f(XIN) = 16MHz Square wave, no division		30.0	50.0	mA
			open and other	Flash memory 5V version	f(XIN) = 16MHz Square wave, no division		32.5	50.0	mA
				Mask ROM version	f(Xcin) = 32kHz Square wave		90.0		μA
				Flash memory 5V version	f(Xcin) = 32kHz Square wave, in RAM		90.0		μA
Icc				Flash memory 5V version	f(XCIN) = 32kHz Square wave, in flash memory		2.2		mA
				Flash memory 5V version, Program	f(XIN) = 16MHz Square wave, Division by 4		25		mA
				Flash memory 5V version, Erase	f(XIN) = 16MHz Square wave, Division by 4		28		mA
					f(XCIN) = 32kHz When a WAIT instruction is executed (Note 1)		4.0	10 (Topr = 25°C)	μA
					Topr = 25°C when clock is stopped			1.0	μA
					Topr = 85°C when clock is stopped			20.0	

Note 1: With one timer operated using fc32.

Note 2: Specify a product of -40°C to 85°C to use it.



Vcc = 5V

Timing requirements (referenced to VCC = 5V, VSS = 0V at Topr = $-20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.7. External clock input

Symbol	Doromotor	Stan	Unit	
Symbol	Parameter			Max.
tc	External clock input cycle time	62.5		ns
tw(H)	External clock input HIGH pulse width	25		ns
tw(L)	External clock input LOW pulse width	25		ns
tr	External clock rise time		15	ns
t f	External clock fall time		15	ns

Table 1.23.8. Memory expansion and microprocessor modes

Symbol	Parameter		Standard		
			Max.	Unit	
tac1(RD-DB)	Data input access time (no wait)		(Note)	ns	
tac2(RD-DB)	Data input access time (with wait)		(Note)	ns	
tac3(RD-DB)	Data input access time (when accessing multiplex bus area)		(Note)	ns	
tsu(DB-RD)	Data input setup time	40		ns	
tsu(RDY-BCLK)	RDY input setup time	30		ns	
tsu(HOLD-BCLK)	HOLD input setup time	40		ns	
th(RD-DB)	Data input hold time	0		ns	
th(BCLK -RDY)	RDY input hold time	0		ns	
th(BCLK-HOLD)	HOLD input hold time	0		ns	
td(BCLK-HLDA)	HLDA output delay time		40	ns	

Note: Calculated according to the BCLK frequency as follows:

$$tac1(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 45$$
 [ns]

$$tac2(RD - DB) = \frac{3 \times 10^9}{f(BCLK) \times 2} - 45$$
 [ns]

$$tac3(RD - DB) = \frac{3 \times 10^9}{f(BCLK) \times 2} - 45$$
 [ns]

Timing requirements (referenced to VCC = 5V, VSS = 0V at Topr = $-20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.9. Timer A input (counter input in event counter mode)

Symbol	Devented	Standard Min. Max.	Unit	
	Parameter			
tc(TA)	TAin input cycle time	100		ns
tw(TAH)	TAin input HIGH pulse width	40		ns
tw(TAL)	TAin input LOW pulse width	40		ns

Table 1.23.10. Timer A input (gating input in timer mode)

Symbol	5	Standard Min. Max.		
	Parameter		Max.	Unit
tc(TA)	TAin input cycle time	400		ns
tw(TAH)	TAin input HIGH pulse width	200		ns
tw(TAL)	TAin input LOW pulse width	200		ns

Table 1.23.11. Timer A input (external trigger input in one-shot timer mode)

Cymphol	Parameter	Standard Min. Max.	Unit	
Symbol	Farameter			
tc(TA)	TAil input cycle time	200		ns
tw(TAH)	TAin input HIGH pulse width	100		ns
tw(TAL)	TAin input LOW pulse width	100		ns

Table 1.23.12. Timer A input (external trigger input in pulse width modulation mode)

Coursells al	Daramatar	Standard	Lloit	
Symbol	Parameter	Min.	Max.	Unit
tw(TAH)	TAiın input HIGH pulse width	100		ns
tw(TAL)	TAin input LOW pulse width	100		ns

Table 1.23.13. Timer A input (up/down input in event counter mode)

Symbol Parameter	Description	Star	ndard	1.1
	Parameter	Min.	Max.	Unit
tc(UP)	TAiout input cycle time	2000		ns
tw(UPH)	TAiout input HIGH pulse width	1000		ns
tw(UPL)	TAiout input LOW pulse width	1000		ns
tsu(UP-TIN)	TAiout input setup time	400		ns
th(TIN-UP)	TAio∪⊤ input hold time	400		ns



Timing requirements (referenced to VCC = 5V, VSS = 0V at Topr = $-20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.14. Timer B input (counter input in event counter mode)

Symbol	Description	Star	Standard	Unit
	Parameter	Min.	Max.	
tc(TB)	TBiin input cycle time (counted on one edge)	100		ns
tw(TBH)	TBil input HIGH pulse width (counted on one edge)	40		ns
tw(TBL)	TBiin input LOW pulse width (counted on one edge)	40		ns
tc(TB)	TBiin input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiln input HIGH pulse width (counted on both edges)	80		ns
tw(TBL)	TBin input LOW pulse width (counted on both edges)	80		ns

Table 1.23.15. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard Min. Max.	Unit	
	Farameter		Offic	
tc(TB)	TBiin input cycle time	400		ns
tw(TBH)	TBiin input HIGH pulse width	200		ns
tw(TBL)	TBiin input LOW pulse width	200		ns

Table 1.23.16. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standa	dard	Unit
	i didiffeter	Min.	Max.	Oill
tc(TB)	TBiln input cycle time	400		ns
tw(TBH)	TBiin input HIGH pulse width	200		ns
tw(TBL)	TBiin input LOW pulse width	200		ns

Table 1.23.17. A-D trigger input

Symbol	Parameter	Standar	dard	Unit
Symbol	i didilielei	Min.	Max.	Offic
tc(AD)	ADTRG input cycle time (trigger able minimum)	1000		ns
tw(ADL)	ADTRG input LOW pulse width	125		ns

Table 1.23.18. Serial I/O

Symbol	Dozomator	Standa	dard	Unit
	Parameter	Min.	Max.	
tc(CK)	CLKi input cycle time	200		ns
tw(CKH)	CLKi input HIGH pulse width	100		ns
tw(CKL)	CLKi input LOW pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	30		ns
th(C-D)	RxDi input hold time	90		ns

Table 1.23.19. External interrupt INTi inputs

Symbol	Parameter	Standard Min. Max.	Unit	
Cymbol	i arameter		Max.	Offic
tw(INH)	INTi input HIGH pulse width	250		ns
tw(INL)	INTi input LOW pulse width	250		ns



Switching characteristics (referenced to Vcc = 5V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (Note 3), CM15 = "1" unless otherwise specified)

Table 1.23.20. Memory expansion mode and microprocessor mode (no wait)

Symbol	Parameter	Measuring condition	Stan	dard	Unit
Symbol	Farameter	gg	Min.	Max.	Offic
td(BCLK-AD)	Address output delay time			25	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		0		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns
td(BCLK-ALE)	ALE signal output delay time			25	ns
th(BCLK-ALE)	ALE signal output hold time	Figure 1.23.1	- 4		ns
td(BCLK-RD)	RD signal output delay time	1 19410 1.20.1		25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
td(BCLK-WR)	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (BCLK standard)			40	ns
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns
th(WR-DB)	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$td(DB - WR) = \frac{10^{9}}{f(BCLK) \times 2} - 40$$
 [ns]

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.

Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times In (1 - VoL / Vcc)$$

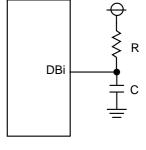
by a circuit of the right figure.

For example, when Vol = 0.2VCC, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30 pF X 1k\Omega X ln (1 - 0.2 Vcc / Vcc)$$

= 6.7ns.

Note 3: Specify a product of -40°C to 85°C to use it.



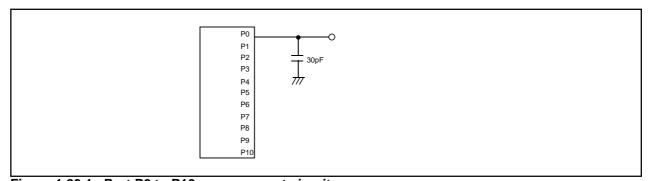


Figure 1.23.1. Port P0 to P10 measurement circuit



$$Vcc = 5V$$

Switching characteristics (referenced to Vcc = 5V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ (Note 3), CM15 = "1" unless otherwise specified)

Table 1.23.21. Memory expansion mode and microprocessor mode (with wait, accessing external memory)

Ol	Dawa wa ata u	Measuring condition	Stan	dard	l lade
Symbol	Parameter	Weasuring condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time			25	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		0		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns
td(BCLK-ALE)	ALE signal output delay time			25	ns
th(BCLK-ALE)	ALE signal output hold time	Figure 1.23.1	- 4		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time		0		ns
td(BCLK-WR)	WR signal output delay time			25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (BCLK standard)			40	ns
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns
th(WR-DB)	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$td(DB - WR) = \frac{10^{9}}{f(BCLK)} - 40$$
 [ns]

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.

Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times In (1 - VoL / Vcc)$$

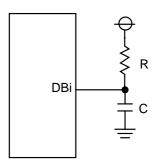
by a circuit of the right figure.

For example, when Vol = 0.2Vcc, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k\Omega X In (1 - 0.2Vcc / Vcc)$$

= 6.7ns.

Note 3: Specify a product of -40°C to 85°C to use it.



Switching characteristics (referenced to Vcc = 5V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (Note 2), CM15 = "1" unless otherwise specified)

Table 1.23.22. Memory expansion mode and microprocessor mode (with wait, accessing external memory, multiplex bus area selected)

0	December	Manager and dition	Standard		
Symbol	Parameter	Measuring condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time			25	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns
th(RD-AD)	Address output hold time (RD standard)		(Note1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note1)		ns
td(BCLK-CS)	Chip select output delay time			25	ns
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns
th(RD-CS)	Chip select output hold time (RD standard)		(Note1)		ns
th(WR-CS)	Chip select output hold time (WR standard)		(Note1)		ns
td(BCLK-RD)	RD signal output delay time			25	ns
th(BCLK-RD)	RD signal output hold time	Figure 1.23.1	0		ns
td(BCLK-WR)	WR signal output delay time	1 iguie 1.23.1		25	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (BCLK standard)			40	ns
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			25	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		- 4		ns
td(AD-ALE)	ALE signal output delay time (Address standard)		(Note1)		ns
th(ALE-AD)	ALE signal output hold time (Adderss standard)		30		ns
td(AD-RD)	Post-address RD signal output delay time		0		ns
td(AD-WR)	Post-address WR signal output delay time		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]
$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]
$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]
$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]
$$td(DB - WR) = \frac{10^9 \times 3}{f(BCLK) \times 2} - 40$$
 [ns]
$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]
$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 25$$
 [ns]

Note 2: Specify a product of -40°C to 85°C to use it.



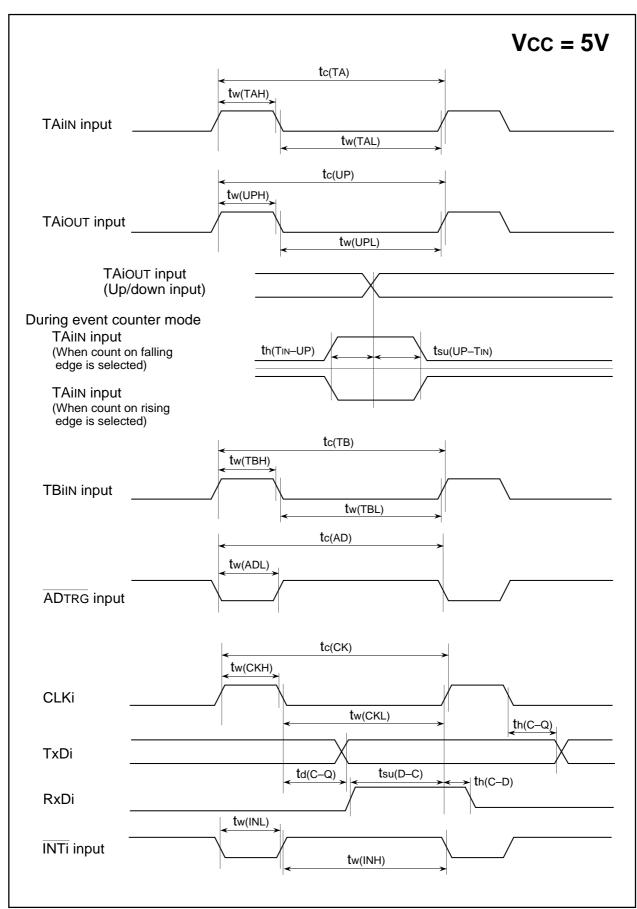


Figure 1.23.2. Vcc = 5V timing diagram (1)

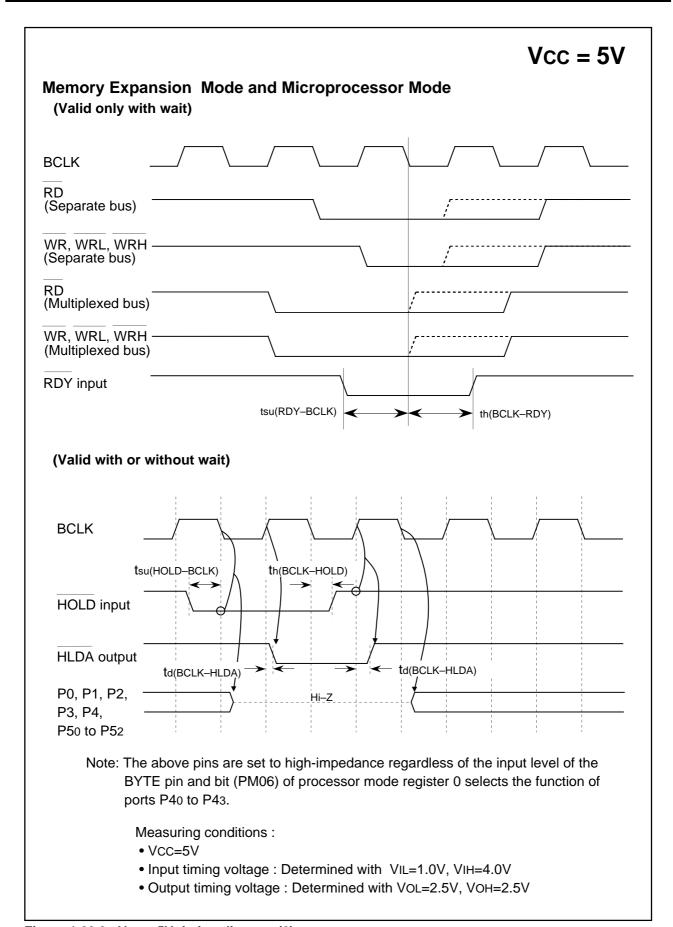


Figure 1.23.3. Vcc = 5V timing diagram (2)



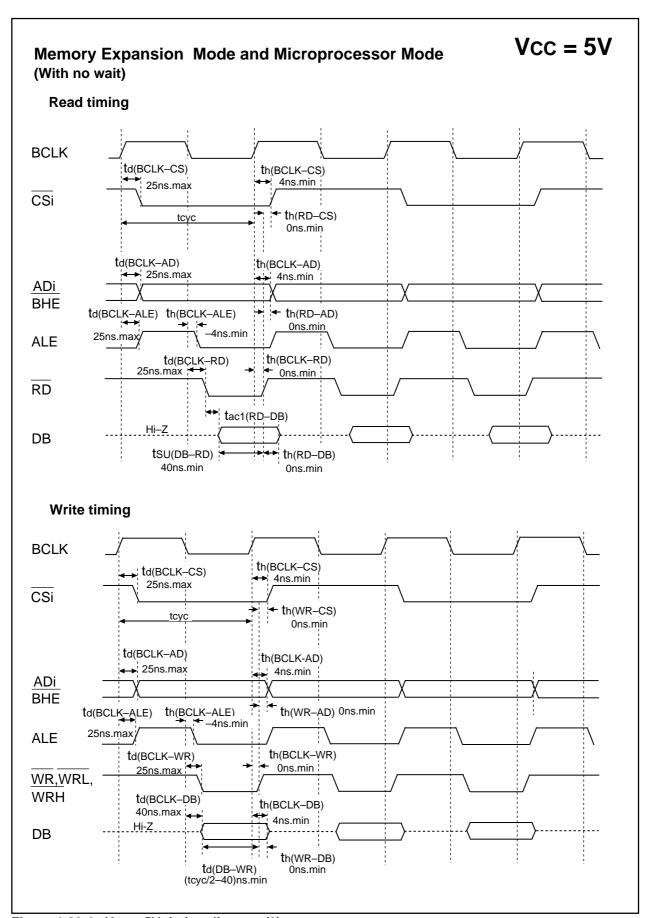


Figure 1.23.4. Vcc = 5V timing diagram (3)



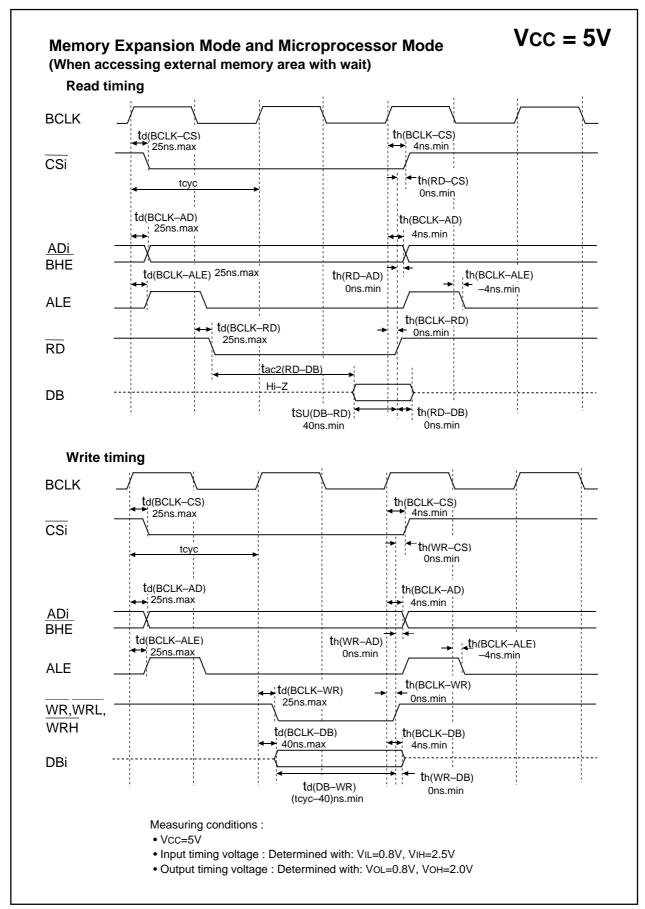


Figure 1.23.5. Vcc = 5V timing diagram (4)



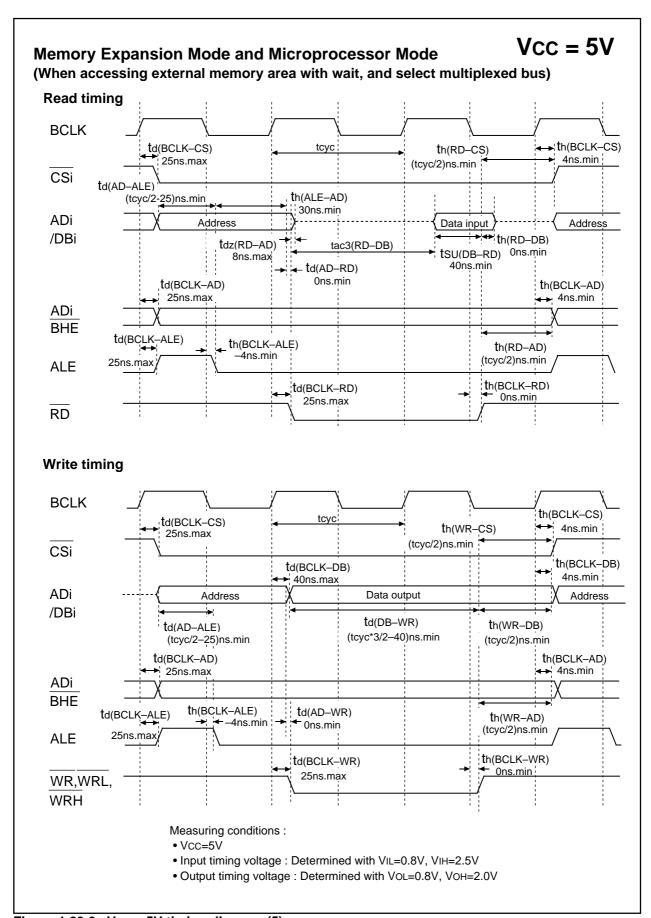


Figure 1.23.6. Vcc = 5V timing diagram (5)

Table 1.23.23. Electrical characteristics (referenced to VCC = 2.7 to 3.3V, VSS = 0V at Topr = -20°C to 85° C / -40° C to 85° C (Note 1), f(XIN) = 10MHz (Note 2) with wait unless otherwise specified)

Cumbal		Doromote		Meacu	uring condition	S	tandard	t	ا ما ا
Symbol		Parameter		ivieasu	ıring condition	Min	Тур.	Max.	Unit
Vон	HIGH output voltage	P00 to P07, P10 to F P30 to P37, P40 to F P60 to P67, P72 to F P86, P87, P90 to P9	P47, P50 to P57, P77, P80 to P84,	Iон = -1mA		2.5			V
	HIGH output	voltage XouT	HIGHPOWER	Iон = -0.1mA		2.5			
Vон	Thorrouput	vollage 7001	LOWPOWER	Іон = -50µА		2.5			V
	HIGH output	voltage Хсоит	HIGHPOWER	With no load appl	lied		3.0		V
		· ·	LOWPOWER	With no load appl	lied		1.6		
VoL	LOW output voltage	P00 to P07, P10 to F P30 to P37, P40 to F P60 to P67, P70 to F P86, P87, P90 to P9	P47, P50 to P57, P77, P80 to P84,	IoL = 1mA				0.5	V
			HIGHPOWER	IoL = 0.1mA				0.5	
Vol	LOW output	voltage Xout	LOWPOWER	IoL = 50μA				0.5	V
			HIGHPOWER	With no load appl	ied		0	0.5	
	LOW output	voltage Хсоит	LOWPOWER	With no load appl			0		V
VT+-VT-	Hysteresis	HOLD, RDY, TAOIN TBOIN to TB5IN, INT ADTRG, CTS0 to CT CLK0 to CLK4,TA20 Klo to Kl3, RxD0 to	to TA4IN, to TNT5, NMI, S2, SCL, SDA out to TA4out,	with the load appr		0.2	U	0.8	V
VT+-VT-	Hysteresis	RESET				0.2		1.8	V
lin	HIGH input current		P47 ,P50 to P57, P77, P80 to P87, P107,	Vı = 3V		0.2		4.0	μA
I _{IL}	LOW input current	P00 to P07, P10 to F P30 to P37, P40 to F P60 to P67, P70 to F P90 to P97, P100 to XIN, RESET, CNVs:	P47, P50 to P57, P77, P80 to P87, P107,	Vı = 0V				-4.0	μА
R PULLUP	Pull-up resistance	P00 to P07, P10 to F P30 to P37, P40 to F P60 to P67, P72 to F P86, P87, P90 to P9	P47, P50 to P57, P77, P80 to P84,	VI = 0V		66.0	120.0	500.0	kΩ
R _{fXIN}	Feedback re	esistance XIN					3.0		МΩ
R fXCIN	Feedback re	esistance Xcin					10.0		МΩ
V _{RAM}	RAM retenti			When clock is sto	nned	2.0			V
- IXAIVI	10 avi reteriti	- ronago	In single-chip	Mask ROM	f(Xin) = 10MHz	2.0			-
			mode, the	version	Square wave, no division		8.5	21.25	mA
			output pins are open and other pins are Vss	Flash memory 5V version	f(XIN) = 10MHz Square wave, no division		12.0	21.25	mA
				Mask ROM version	f(Xcin) = 32kHz Square wave		40.0		μA
				Flash memory 5V version	f(Xcin) = 32kHz Square wave, in RAM		40.0		μA
Icc	Power suppl	lv current		Flash memory 5V version	f(XCIN) = 32kHz Square wave, in flash memory		800		μA
					f(XCIN) = 32kHz When a WAITinstruction is executed. Oscillation capacity High (Note 3)		2.8	10 (Topr = 25°C)	μА
					f(XCIN) = 32kHz When a WAIT instruction is executed. Oscillation capacity Low (Note 3)		0.9	10 (Topr = 25°C)	μА
					Topr = 25°C when clock is stopped			1.0	μA
					Topr = 85°C when clock is stopped			20.0	

Note 1: Specify a product of -40°C to 85°C to use it.

Note 2: 10 MHz for the mask ROM version and flash memory 5V version.

Note 3: With one timer operated using fc32.



$$Vcc = 3V$$

Timing requirements (referenced to VCC = 3V, VSS = 0V at Topr = - 20°C to 85°C / - 40°C to 85°C (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.24. External clock input

Cymphal	Parameter		Standard		Unit
Symbol			Min.	Max.	Offic
tc	External clock input cycle time	Mask ROM, Flash memory 5V version	100		ns
tw(H)	External clock input HIGH pulse width	Mask ROM, Flash memory 5V version	40		ns
tw(L)	External clock input LOW pulse width	Mask ROM, Flash memory 5V version	40		ns
tr	External clock rise time			18	ns
tf	External clock fall time			18	ns

Table 1.23.25. Memory expansion and microprocessor modes

Cymahal	Description	Stan	Standard	
Symbol	Parameter	Min.	Max.	Unit
tac1(RD-DB)	Data input access time (no wait)		(Note)	ns
tac2(RD-DB)	Data input access time (with wait)		(Note)	ns
tac3(RD-DB)	Data input access time (when accessing multiplex bus area)		(Note)	ns
tsu(DB-RD)	Data input setup time	80		ns
tsu(RDY-BCLK)	RDY input setup time	60		ns
tsu(HOLD-BCLK)	HOLD input setup time	80		ns
th(RD-DB)	Data input hold time	0		ns
th(BCLK -RDY)	RDY input hold time	0		ns
th(BCLK-HOLD)	HOLD input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		100	ns

Note: Calculated according to the BCLK frequency as follows:

$$tac1(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 90$$
 [ns]

$$tac2(RD - DB) = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90$$
 [ns]

$$tac3(RD - DB) = \frac{3 \times 10^9}{f(BCLK) \times 2} - 90$$
 [ns]

Timing requirements (referenced to VCC = 3V, VSS = 0V at Topr = - 20°C to 85°C / - 40°C to 85°C (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.26. Timer A input (counter input in event counter mode)

Symbol	Parameter	Standard		Unit
	i alametei	Min.	Max.	Offic
tc(TA)	TAin input cycle time	150		ns
tw(TAH)	TAin input HIGH pulse width	60		ns
tw(TAL)	TAin input LOW pulse width	60		ns

Table 1.23.27. Timer A input (gating input in timer mode)

Symbol	Parameter -	Standard		l lmi4
		Min.	Max.	Unit
tc(TA)	TAin input cycle time	600		ns
tw(TAH)	TAin input HIGH pulse width	300		ns
tw(TAL)	TAin input LOW pulse width	300		ns

Table 1.23.28. Timer A input (external trigger input in one-shot timer mode)

Symbol	Description	Standard		l lait
	Parameter	Min.	Max.	Unit
tc(TA)	TAil input cycle time	300		ns
tw(TAH)	TAil input HIGH pulse width	150		ns
tw(TAL)	TAin input LOW pulse width	150		ns

Table 1.23.29. Timer A input (external trigger input in pulse width modulation mode)

Symbol	Parameter	Standard		11.7
		Min.	Max.	Unit
tw(TAH)	TAin input HIGH pulse width	150		ns
tw(TAL)	TAin input LOW pulse width	150		ns

Table 1.23.30. Timer A input (up/down input in event counter mode)

Symbol	Parameter	Standard		I India
		Min.	Max.	Unit
tc(UP)	TAiout input cycle time	3000		ns
tw(UPH)	TAiout input HIGH pulse width	1500		ns
tw(UPL)	TAiout input LOW pulse width	1500		ns
tsu(UP-TIN)	TAiouT input setup time	600		ns
th(TIN-UP)	TAiout input hold time	600		ns



Timing requirements (referenced to VCC = 3V, VSS = 0V at Topr = $-20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (*) unless otherwise specified)

*: Specify a product of -40°C to 85°C to use it.

Table 1.23.31. Timer B input (counter input in event counter mode)

Symbol Parameter		Standard		11.3
	Parameter	Min.	Max.	Unit
tc(TB)	TBiin input cycle time (counted on one edge)	150		ns
tw(TBH)	TBiin input HIGH pulse width (counted on one edge)	60		ns
tw(TBL)	TBin input LOW pulse width (counted on one edge)	60		ns
tc(TB)	TBiin input cycle time (counted on both edges)	300		ns
tw(TBH)	TBilN input HIGH pulse width (counted on both edges)	160		ns
tw(TBL)	TBiin input LOW pulse width (counted on both edges)	160		ns

Table 1.23.32. Timer B input (pulse period measurement mode)

Symbol	Parameter	Standard		Unit
	i didilictei	Min.	Max.	Offic
tc(TB)	TBin input cycle time	600		ns
tw(TBH)	TBiin input HIGH pulse width	300		ns
tw(TBL)	TBin input LOW pulse width	300		ns

Table 1.23.33. Timer B input (pulse width measurement mode)

Symbol	Parameter	Standard		Unit
	i arameter	Min.	Max.	01111
tc(TB)	TBin input cycle time	600		ns
tw(TBH)	TBilN input HIGH pulse width	300		ns
tw(TBL)	TBilN input LOW pulse width	300		ns

Table 1.23.34. A-D trigger input

Symbol	Parameter	Standard		Unit
Cymbol	i diamotoi	Min.	Max.	J
tc(AD)	ADTRG input cycle time (trigger able minimum)	1500		ns
tw(ADL)	ADTRG input LOW pulse width	200		ns

Table 1.23.35. Serial I/O

Symbol	Parameter	Stan	Standard	
	i alametei	Min.	Max.	Unit
tc(CK)	CLKi input cycle time	300		ns
tw(CKH)	CLKi input HIGH pulse width	150		ns
tw(CKL)	CLKi input LOW pulse width	150		ns
td(C-Q)	TxDi output delay time		160	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input setup time	50		ns
th(C-D)	RxDi input hold time	90		ns

Table 1.23.36. External interrupt INTi inputs

Symbol	Parameter	Standard		Unit
Symbol	i didilielei	Min.	Min. Max.	Offic
tw(INH)	INTi input HIGH pulse width	380		ns
tw(INL)	INTi input LOW pulse width	380		ns



Switching characteristics (referenced to Vcc = 3V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ (Note 3), CM15="1" unless otherwise specified)

Table 1.23.37. Memory expansion and microprocessor modes (with no wait)

Courada a l	Development	Measuring condition	Stand	dard	1.1:4
Symbol	Parameter	weasuring condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time			60	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		0		ns
td(BCLK-CS)	Chip select output delay time			60	ns
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns
td(BCLK-ALE)	ALE signal output delay time			60	ns
th(BCLK-ALE)	ALE signal output hold time		-4		ns
td(BCLK-RD)	RD signal output delay time	Figure 1.23.7		60	ns
th(BCLK-RD)	RD signal output hold time	1 19010 1.20.7	0		ns
td(BCLK-WR)	WR signal output delay time			60	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (BCLK standard)			80	ns
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns
th(WR-DB)	Data output hold time (WR standard)(Note2)		0		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$td(DB - WR) = \frac{10^9}{f(BCLK) \times 2} - 80$$
 [ns]

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.

Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR X In (1 - VoL / Vcc)$$

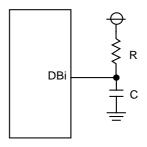
by a circuit of the right figure.

For example, when Vol = 0.2VCC, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k\Omega X In (1 - 0.2Vcc / Vcc)$$

= 6.7ns.

Note 3: Specify a product of -40°C to 85°C to use it.



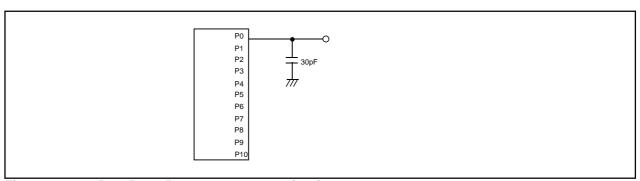


Figure 1.23.7. Port P0 to P10 measurement circuit



$$Vcc = 3V$$

Switching characteristics (referenced to Vcc = 3V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ (Note 3), CM15="1" unless otherwise specified)

Table 1.23.38. Memory expansion and microprocessor modes (when accessing external memory area with wait)

0	Damana I.a.	Magazzing condition	Stan	dard	1.111	
Symbol	Parameter	Measuring condition	Min.	Max.	Unit	
td(BCLK-AD)	Address output delay time			60	ns	
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns	
th(RD-AD)	Address output hold time (RD standard)		0		ns	
t h(WR-AD)	Address output hold time (WR standard)		0		ns	
td(BCLK-CS)	Chip select output delay time			60	ns	
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns	
td(BCLK-ALE)	ALE signal output delay time	Figure 1.23.7		60	ns	
th(BCLK-ALE)	ALE signal output hold time		- 4		ns	
td(BCLK-RD)	RD signal output delay time			60	ns	
th(BCLK-RD)	RD signal output hold time		0		ns	
td(BCLK-WR)	WR signal output delay time			60	ns	
th(BCLK-WR)	WR signal output hold time		0		ns	
td(BCLK-DB)	Data output delay time (BCLK standard)			80	ns	
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns	
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns	
th(WR-DB)	Data output hold time (WR standard)(Note2)		0		ns	

Note 1: Calculated according to the BCLK frequency as follows:

$$td(DB - WR) = \frac{10^9}{f(BCLK)} - 80$$
 [ns]

Note 2: This is standard value shows the timing when the output is off, and doesn't show hold time of data bus.

Hold time of data bus is different by capacitor volume and pull-up (pull-down) resistance value.

Hold time of data bus is expressed in

$$t = -CR \times In (1 - VoL / VCC)$$

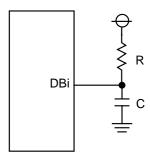
by a circuit of the right figure.

For example, when Vol = 0.2VCC, C = 30pF, R = 1k Ω , hold time of output "L" level is

$$t = -30pF X 1k\Omega X In (1 - 0.2Vcc / Vcc)$$

= 6.7ns.

Note 3: Specify a product of -40°C to 85°C to use it.



Switching characteristics (referenced to Vcc = 3V, Vss = 0V at $Topr = -20^{\circ}C$ to $85^{\circ}C$ / $-40^{\circ}C$ to $85^{\circ}C$ (Note 2), CM15="1" unless otherwise specified)

Table 1.23.39. Memory expansion and microprocessor modes
(when accessing external memory area with wait, and select multiplexed bus)

0 1 1		Manageria a condition	Stan	dard	11.
Symbol	Parameter	Measuring condition	Min.	Max.	Unit
td(BCLK-AD)	Address output delay time			60	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		4		ns
th(RD-AD)	Address output hold time (RD standard)		(Note1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note1)		ns
td(BCLK-CS)	Chip select output delay time			60	ns
th(BCLK-CS)	Chip select output hold time (BCLK standard)		4		ns
th(RD-CS)	Chip select output hold time (RD standard)		(Note1)		ns
th(WR-CS)	Chip select output hold time (WR standard)		(Note1)		ns
td(BCLK-RD)	RD signal output delay time			60	ns
th(BCLK-RD)	RD signal output hold time	Figure 1.23.7	0		ns
td(BCLK-WR)	WR signal output delay time			60	ns
th(BCLK-WR)	WR signal output hold time		0		ns
td(BCLK-DB)	Data output delay time (BCLK standard)			80	ns
th(BCLK-DB)	Data output hold time (BCLK standard)		4		ns
td(DB-WR)	Data output delay time (WR standard)		(Note1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			60	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		- 4		ns
td(AD-ALE)	ALE signal output delay time (Address standard)		(Note1)		ns
th(ALE-AD)	ALE signal output hold time(Address standard)		50		ns
td(AD-RD)	Post-address RD signal output delay time		0		ns
td(AD-WR)	Post-address WR signal output delay time		0		ns
tdZ(RD-AD)	Address output floating start time			8	ns

Note: Calculated according to the BCLK frequency as follows:

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2}$$
 [ns]

th(WR - AD) =
$$\frac{10^{9}}{\text{f(BCLK) X 2}}$$
 [ns]

th(RD - CS) =
$$\frac{10^9}{\text{f(BCLK) X 2}}$$
 [ns]

th(WR - CS) =
$$\frac{10^{9}}{\text{f(BCLK) X 2}}$$
 [ns]

$$td(DB - WR) = \frac{10^9 X 3}{f(BCLK) X 2} - 80$$
 [ns]

th(WR – DB) =
$$\frac{10^{9}}{\text{f(BCLK) X 2}}$$
 [ns]

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 45$$
 [ns]

Note 2: Specify a product of -40°C to 85°C to use it.



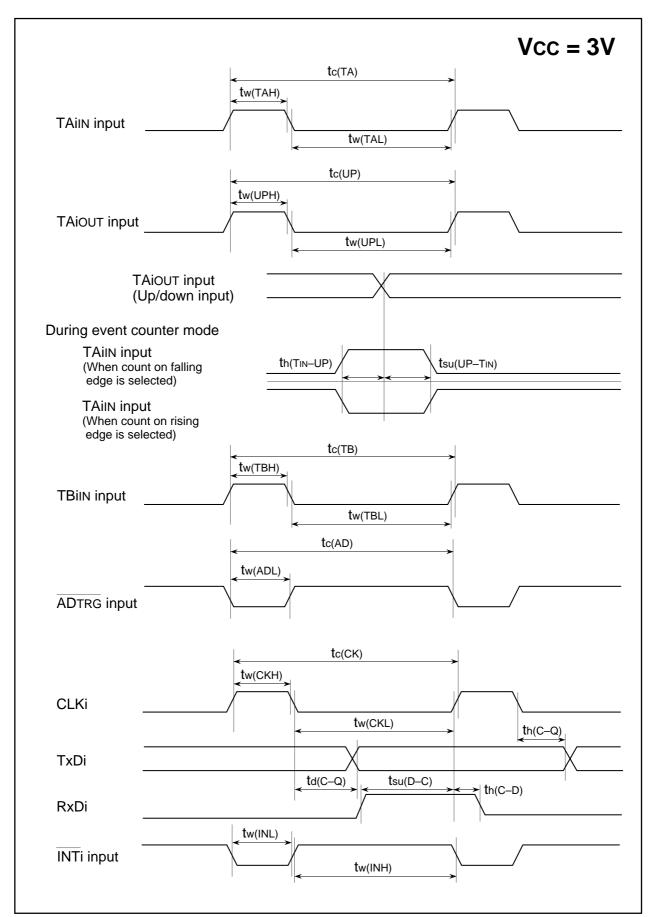
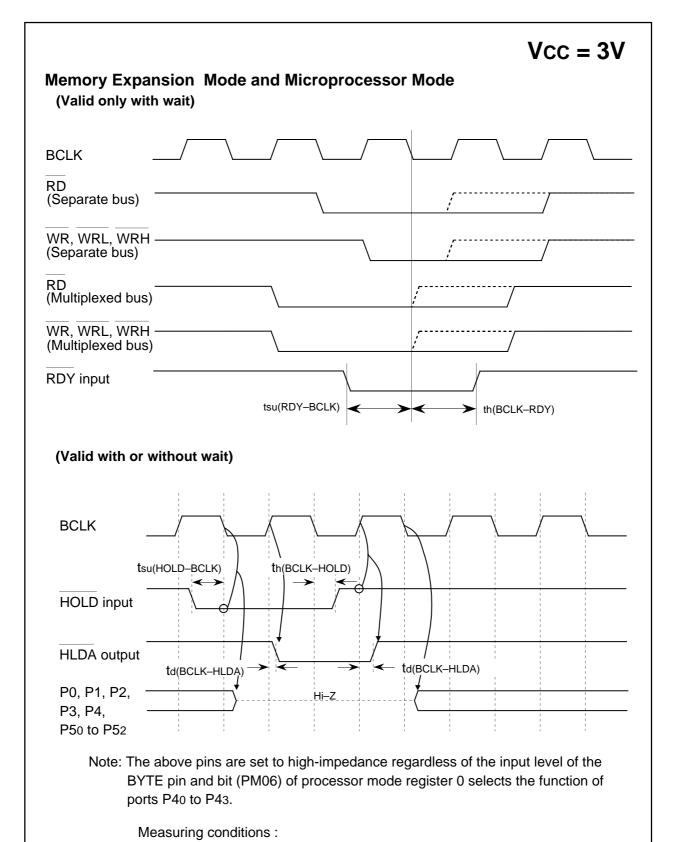


Figure 1.23.8. Vcc = 3V timing diagram (1)



VCC=3V

- Input timing voltage: Determined with VIL=0.6V, VIH=2.4V
- Output timing voltage: Determined with VoL=1.5V, VoH=1.5V

Figure 1.23.9. Vcc = 3V timing diagram (2)



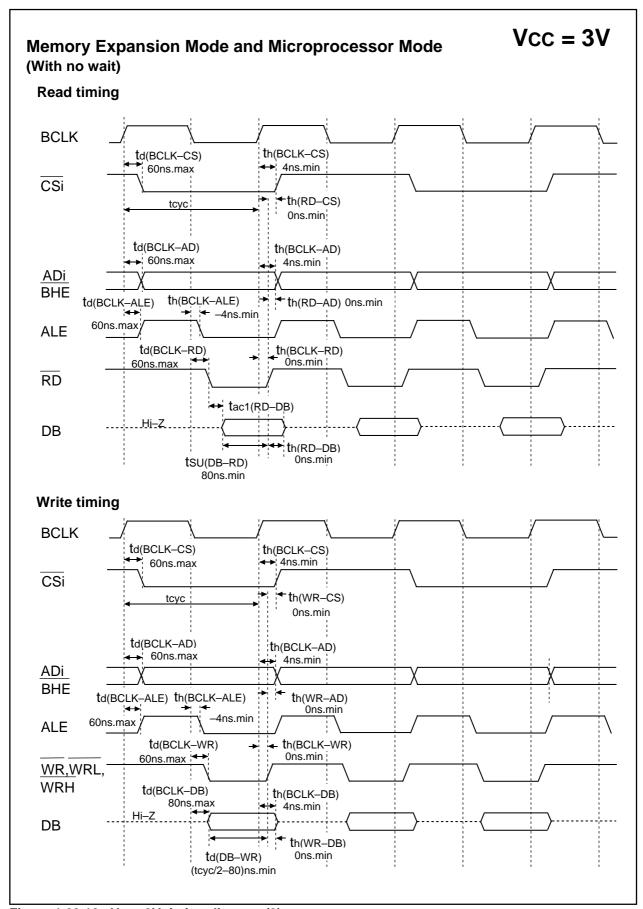


Figure 1.23.10. Vcc = 3V timing diagram (3)

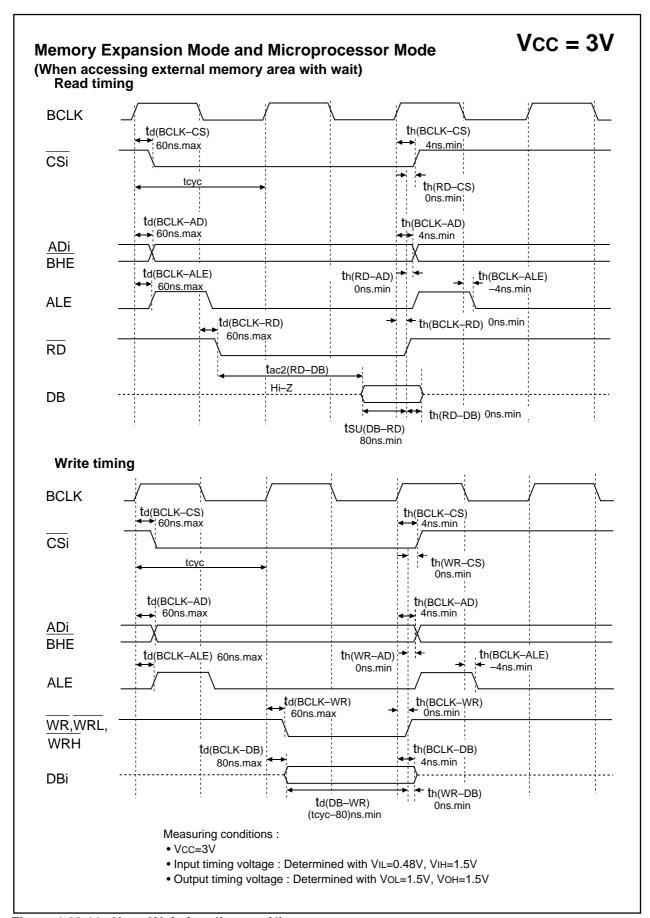


Figure 1.23.11. Vcc = 3V timing diagram (4)

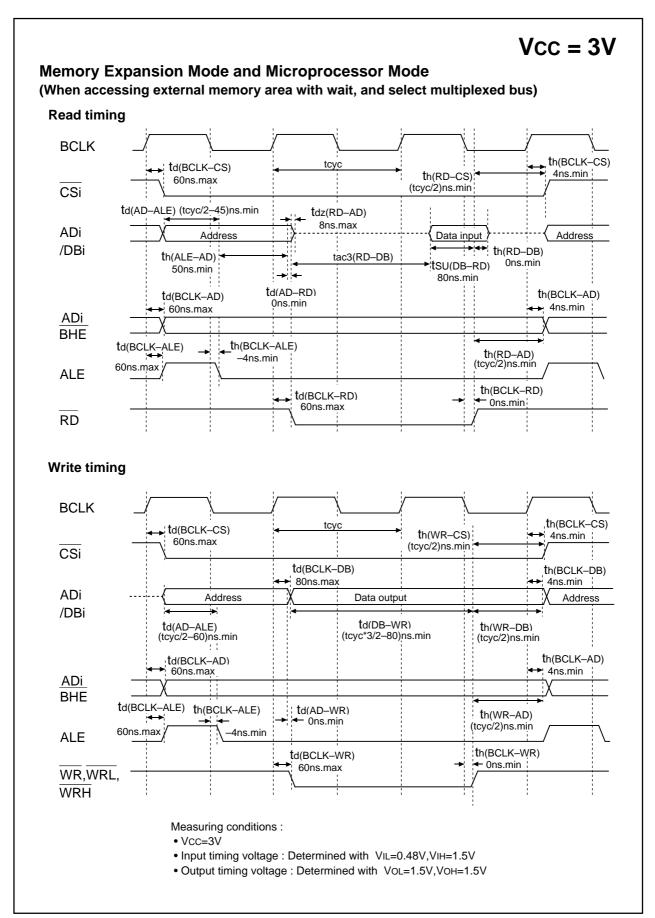


Figure 1.23.12. Vcc = 3V timing diagram (5)

GZZ-SH13-36B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620M8A-XXXFP/GP MASK ROM CONFIRMATION FORM

Mask ROM number	
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	Date :	
÷	Section head signature	Supervisor signature
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Note: Please complete all items marked * .

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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	☐M30620M8A-XXXFP	☐M30620M8A-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30620M8A-XXXFP, submit the 100P6S mark specification sheet. For the M30620M8A-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT osci	llation	circuit is used?	
Ceramic resonator		Quartz-crystal oscill	ator
External clock input		Other ()
What frequency do not use?	•		
f(XIN) =	MHz		



GZZ-SH13-36B<96A0>

Mask ROM numbe

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620M8A-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which	kind of XCIN-X	COUT oscilla	ition circuit i	s used?					
	Ceramic reson	ator	Quar	tz-crysta	al oscillato	r			
	External clock	input	Othe	r ()				
What fr	equency do n	ot use?							
f	(XCIN) =	kHz	<u>z</u>						
(3) Which	peration mod	e do you us	e?						
	Single-chip mo	ode	☐ Mem	ory expa	ansion mo	de			
r	/licroprocesso	r mode							
(4) Which	operating supp	oly voltage o	lo you use?						
(Circle	the operating	voltage ranç	ge of use)						
2.4 2.	7 3.0 3.3	3.5 3.8	4.0 4.2	4.5 4	5.0	5.3	5.5	5.7 — (V)	
(5) Which	operating amb	ient temper	ature do vou	ı use?					
	the operating	•	-						
,	0 -30 -20	-10 0	10 20	30 4	40 50	60	70	80	90 (°C)
(6) Do you	use I ² C (Inter	IC) bus fun	ction?						
. , _	Not use	,	Use						
(7) Do you	use IE (Inter I	Equipment)	bus function	ı?					
	Not use		Use						
Thank you co	ooperation.								
*4. Special item	(Indicate nor	e if there is	not specifie	d item)					



GZZ-SH13-37B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MAA-XXXFP/GP MASK ROM CONFIRMATION FORM

Mask ROM number	
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	Date :	
	Section head	Supervisor
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Receipt	Signature	Signature

Note: Please complete all items marked * .

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*	Customer	name		()	ance	atur		
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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No.:	☐M30620MAA-XXXFP	☐M30620MAA-XXXGP			
File code :		(hex)			
Mask file name :		.MSK (alpha-numeric 8-digit)			

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30620MAA-XXXFP, submit the 100P6S mark specification sheet. For the M30620MAA-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT oscillation	circuit is used?	
Ceramic resonator	Quartz-crystal oscillato	r
External clock input	Other (
What frequency do not use?		
f(XIN) = MHz		



GZZ-SH13-37B<96A0>

Mask ROM numbe

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MAA-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of ACIN-ACOUT oscillation	n circuit is used?
Ceramic resonator	Quartz-crystal oscillator
External clock input	Other ()
What frequency do not use?	
f(XCIN) = kHz	
(3) Which operation mode do you use?	
☐ Single-chip mode	Memory expansion mode
☐ Microprocessor mode	
(4) Which operating supply voltage do y	ou use?
(Circle the operating voltage range of	of use)
2.4 2.7 3.0 3.3 3.5 3.8 4	1.0 4.2 4.5 4.7 5.0 5.3 5.5 5.7
(5) Which operating ambient temperatu	re do you use?
(Circle the operating temperature ra	nge of use)
	10 20 30 40 50 60 70 80 90
(6) Do you use I ² C (Inter IC) bus function	on?
☐ Not use	Use
(7) Do you use IE (Inter Equipment) bus	s function?
☐ Not use	Use
Thank you cooperation.	
*4. Special item (Indicate none if there is no	t specified item)



GZZ-SH13-28B<95A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MCA-XXXFP/GP MASK ROM CONFIRMATION FORM

Mask ROM number	
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Date :	
Section head	Supervisor
signature	signature

Note: Please complete all items marked * .

		Company		TEL		a)	е	Submitted by	Supervisor
*	Customer	name		()	ance	atur		
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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	∐M30620MCA-XXXFP	☐M30620MCA-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30620MCA-XXXFP, submit the 100P6S mark specification sheet. For the M30620MCA-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT oscillation	on circuit is used?	
Ceramic resonator	Quartz-crystal oscilla	tor
External clock input	Other ()
What frequency do not use?		
f(XIN) = MH	IZ	



GZZ-SH13-28B<95A0>

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MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30620MCA-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?
Ceramic resonator Quartz-crystal oscillator
External clock input Other ()
What frequency do not use?
f(XCIN) = kHz
(3) Which operation mode do you use?
☐ Single-chip mode ☐ Memory expansion mode
☐ Microprocessor mode
(4) Which operating supply voltage do you use?
(Circle the operating voltage range of use)
2.4 2.7 3.0 3.3 3.5 3.8 4.0 4.2 4.5 4.7 5.0 5.3 5.5 5.7
(5) Which operating ambient temperature do you use?
(Circle the operating temperature range of use)
-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90
(6) Do you use I ² C (Inter IC) bus function?
☐ Not use ☐ Use
(7) Do you use IE (Inter Equipment) bus function?
☐ Not use ☐ Use
Thank you cooperation.
Special item (Indicate none if there is not specified item)



GZZ-SH13-40B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622M4A-XXXFP/GP MASK ROM CONFIRMATION FORM

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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	∐M30622M4A-XXXFP	∐M30622M4A-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30622M4A-XXXFP, submit the 100P6S mark specification sheet. For the M30622M4A-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT oscillation	circuit is used?
Ceramic resonator	Quartz-crystal oscillator
External clock input	Other ()
What frequency do not use?	
f(XIN) = MHz	



GZZ-SH13-40B<96A0>

Mask ROM number	
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MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622M4A-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circuit is used?
Ceramic resonator Quartz-crystal oscillator
External clock input Other ()
What frequency do not use?
f(XCIN) = kHz
(2) Which operation made do you use?
(3) Which operation mode do you use?
☐ Single-chip mode ☐ Memory expansion mode
Microprocessor mode
(4) Which operating supply voltage do you use?
(Circle the operating voltage range of use)
2.4 2.7 3.0 3.3 3.5 3.8 4.0 4.2 4.5 4.7 5.0 5.3 5.5 5.7
(5) Which operating ambient temperature do you use?
(Circle the operating temperature range of use)
-50 -40 -30 -20 -10 0 10 20 30 40 50 60 70 80 90
-30 -40 -30 -20 -10 0 10 20 30 40 30 00 70 00 30 (°C)
(6) Do you use I ² C (Inter IC) bus function?
☐ Not use ☐ Use
(7) Do you use IE (Inter Equipment) bus function?
□ Not use □ Use
Thank you cooperation.
mank you occoporation.
*4. Special item (Indicate none if there is not specified item)



GZZ-SH13-38B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622M8A-XXXFP/GP MASK ROM CONFIRMATION FORM

Mask ROM number	
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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	∐M30622M8A-XXXFP	∐M30622M8A-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30622M8A-XXXFP, submit the 100P6S mark specification sheet. For the M30622M8A-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT o	scillation	circuit is used?	
Ceramic resonator		Quartz-cryst	tal oscillator
External clock inpu	ıt	Other ()
What frequency do not us	se?		
f(XIN) =	MHz		



GZZ-SH13-38B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622M8A-XXXFP/GP MASK ROM CONFIRMATION FORM

(2	2) Which k	kind of X	CIN-X	COUT O	scillat	tion ci	rcuit is	usec	1?					
		Ceramic	reson	ator			Quart	z-crys	stal os	cillato	or			
		External	clock	input			Other	. ()				
	What from	equency	do no	ot use?										
	f	(XCIN) =			kHz	<u> </u>								
13	3) Which o	poration	mode	o do ve) I II I I I I	2								
(3	<i>'</i>	Single-ch		•	Ju use		Memo	ory ov	nanci	on mo	do			
		/licropro				Ш	MEIII	лу ех	parisi		ue			
	ШΝ	лсторго	Cessoi	mode	;									
(4	4) Which c	perating	g supp	ly volta	age d	o you	use?							
	(Circle t	the oper	ating \	/oltage	rang	e of u	se)							
	2.4 2.7	7 3.0	3.3	3.5	3.8	4.0	4.2	4.5	4.7	5.0	5.3	5.5	5.7	
													(V)
(5	5) Which c	perating	ambi	ent ter	mpera	ature c	lo vou	use?						
(-	•	he oper			•		•							
	-50 -40	•	-20	-10	0	10	20	30	40	50	60	70	80	90
			_					-				+	_	(°C)
,,	· · ·	.20			,			·	·	,	·	·	·	'
(6	6) Do you		(Inter	IC) bu	s tund	ction?								
	Пи	lot use					Use							
(7	7) Do you	use IE (Inter E	quipm	nent) k	ous fu	nction	?						
		lot use					Use							
Tha	ank you co	operatio	n.											
*4 C-	ooial itaa	(Indicat		a if the	ro io	not co	ooific	d :to:	١					
※4. ⊃ β	ecial item	(maicat	e non	e ii trie	HE IS	not sp	ecille	a item)					



GZZ-SH13-34B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622MAA-XXXFP/GP MASK ROM CONFIRMATION FORM

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*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	□M30622MAA-XXXFP	□M30622MAA-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30622MAA-XXXFP, submit the 100P6S mark specification sheet. For the M30622MAA-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT oscillation circuit is used?							
Ceramic resonator	Quartz-crystal oscillator						
External clock input	Other ()						
What frequency do not use?							
f(XIN) = MHz							



GZZ-SH13-34B<96A0>

Mask ROM number	
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MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622MAA-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation	circuit is used?
Ceramic resonator	Quartz-crystal oscillator
External clock input	Other()
What frequency do not use?	
f(XCIN) = kHz	
(3) Which operation mode do you use?	¬
Single-chip mode	Memory expansion mode
Microprocessor mode	
(4) Which operating supply voltage do yo	u use?
(Circle the operating voltage range of	use)
2.4 2.7 3.0 3.3 3.5 3.8 4.0	
	(V)
(5) Which operating ambient temperature	o do vou uso?
(Circle the operating temperature range)	
-50 -40 -30 -20 -10 0 10	•
	(°C)
(6) Do you use I ² C (Inter IC) bus function	?
☐ Not use	Use
(7) Do you use IE (Inter Equipment) bus t	function?
□ Not use	Use
	_
Thank you cooperation.	
main you ocoporation.	
*4. Special item (Indicate none if there is not s	specified item)



GZZ-SH13-39B<96A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622MCA-XXXFP/GP MASK ROM CONFIRMATION FORM

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	Section head	Supervisor
pt	signature	signature
Receipt		
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Note: Please complete all items marked * .

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*	Customer	name	()	ance	atur		
	Customer	Date issued	Date :	nssı	sign		

*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	☐M30622MCA-XXXFP	M30622MCA-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

*2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30622MCA-XXXFP, submit the 100P6S mark specification sheet. For the M30622MCA-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

(1) Which kind of XIN-XOUT oscillation	circuit is used?	
Ceramic resonator	Quartz-crystal oscilla	ator
External clock input	Other ()
What frequency do not use?		
f(XIN) = MHz		



GZZ-SH13-39B<96A0>

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Mask ROM number	
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MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30622MCA-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillati	ion circuit is used?
Ceramic resonator	Quartz-crystal oscillator
External clock input	Other ()
What frequency do not use?	
f(XCIN) = kHz	
(2) \\(\text{\tinc{\text{\tin}\text{\tin\tinit}\\ \text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\ticl{\text{\ti}\}\tint{\text{\text{\text{\text{\text{\text{\text{\text{\text{\ticl{\text{\text{\texi}\tint{\text{\tintett{\text{\texit{\text{\ti}\tinttitt{\texi}\tint{\text{\texi}\text{\texit{\text{\	2
(3) Which operation mode do you use	<u></u>
☐ Single-chip mode	Memory expansion mode
Microprocessor mode	
(4) Which operating supply voltage do	you use?
(Circle the operating voltage range	e of use)
2.4 2.7 3.0 3.3 3.5 3.8	4.0 4.2 4.5 4.7 5.0 5.3 5.5 5.7
	(*)
(5) Which operating ambient temperat	ture do you use?
(Circle the operating temperature	range of use)
-50 -40 -30 -20 -10 0	10 20 30 40 50 60 70 80 90
(2) 7	
(6) Do you use I ² C (Inter IC) bus func	
☐ Not use	Use
(7) Do you use IE (Inter Equipment) b	us function?
☐ Not use	Use
Thank you cooperation.	
On a sight items (In disease a see 17.1)	
. Special item (Indicate none if there is n	ioi specinea item)



GZZ-SH13-30B<95A0>

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30624MGA-XXXFP/GP MASK ROM CONFIRMATION FORM

	Date :	
	Section head	Supervisor
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*	Customer	name		()	ance	atur		
311.	Odstorrier	Date issued	Date :			Issn	sign		

*1. Check sheet

Mitsubishi processes the mask files generated by the mask file generation utilities out of those held on the floppy disks you give in to us, and forms them into masks. Hence, we assume liability provided that there is any discrepancy between the contents of these mask files and the ROM data to be burned into products we produce. Check thoroughly the contents of the mask files you give in.

Prepare 3.5 inches 2HD (IBM format) floppy disks. And store only one mask file in a floppy disk.

Microcomputer type No. :	□M30624MGA-XXXFP	∐M30624MGA-XXXGP
File code :		(hex)
Mask file name :		.MSK (alpha-numeric 8-digit)

**2. Mark specification

The mark specification differs according to the type of package. After entering the mark specification on the separate mark specification sheet (for each package), attach that sheet to this masking check sheet for submission to Mitsubishi.

For the M30624MGA-XXXFP, submit the 100P6S mark specification sheet. For the M30624MGA-XXXGP, submit the 100P6Q mark specification sheet.

***3.** Usage Conditions

For our reference when of testing our products, please reply to the following questions about the usage of the products you ordered.

(1) Which kind of XIN-XOUT oscillation	n circuit is used?
Ceramic resonator	Quartz-crystal oscillator
External clock input	Other (
What frequency do not use?	
f(XIN) = MHz	



GZZ-SH13-30B<95A0>

Mask ROM numbe	er
----------------	----

MITSUBISHI ELECTRIC-CHIP 16-BIT MICROCOMPUTER M30624MGA-XXXFP/GP MASK ROM CONFIRMATION FORM

(2) Which kind of XCIN-XCOUT oscillation circ	uit is used?
☐ Ceramic resonator ☐ C	Quartz-crystal oscillator
External clock input	Other (
What frequency do not use?	
f(Xcin) = kHz	
(0) \\	
(3) Which operation mode do you use?	
<u> </u>	Memory expansion mode
Microprocessor mode	
(4) Which operating supply voltage do you u	se?
(Circle the operating voltage range of use	e)
	4.2 4.5 4.7 5.0 5.3 5.5 5.7
(5) Which operating ambient temperature do	2001 11592
(Circle the operating temperature range of	
	20 30 40 50 60 70 80 90
-30 -40 -30 -20 -10 0 10	
(6) Do you use I ² C (Inter IC) bus function?	
☐ Not use ☐ L	Jse
(7) Do you use IE (Inter Equipment) bus fund	ction?
	Jse
Thank you cooperation.	
manik you ocoporation.	
*4. Special item (Indicate none if there is not spe-	cified item)



Outline Performance

Table 1.25.1 shows the outline performance of the M16C/62A (flash memory version).

Table 1.25.1. Outline performance of the M16C/62A (flash memory version)

Item		Performance		
Flash memory operation mode		Three modes (parallel I/O, standard serial I/O, CPU rewrite)		
Erase block	User ROM area	See Figure 1.25.1		
division	Boot ROM area	One division (8 Kbytes) (Note)		
Program meth	iod	In units of pages (in units of 256 bytes)		
Erase method		Collective erase/block erase		
Program/erase	e control method	Program/erase control by software command		
Protect metho	d	Protected for each block by lock bit		
Number of cor	mmands	8 commands		
Program/erase count		100 times		
Data retantion		10 years		
ROM code protect		Parallel I/O and standard serial I/O modes are supported.		

Note: The boot ROM area contains a standard serial I/O mode control program which is stored in it when shipped from the factory. This area can be erased and programmed in only parallel I/O mode.



Flash Memory

The M16C/62A (flash memory version) contains the flash memory that can be rewritten with a single voltage. For this flash memory, three flash memory modes are available in which to read, program, and erase: parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and a CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). Each mode is detailed in the pages to follow.

The flash memory is divided into several blocks as shown in Figure 1.25.1, so that memory can be erased one block at a time. Each block has a lock bit to enable or disable execution of an erase or program operation, allowing for data in each block to be protected.

In addition to the ordinary user ROM area to store a microcomputer operation control program, the flash memory has a boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This boot ROM area can be rewritten in only parallel I/O mode.

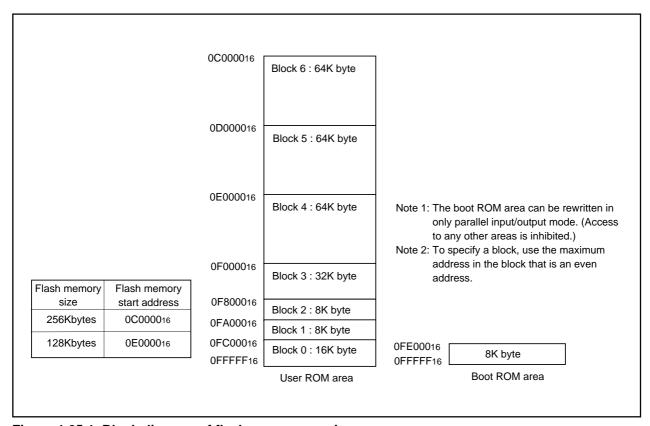


Figure 1.25.1. Block diagram of flash memory version

CPU Rewrite Mode

In CPU rewrite mode, the on-chip flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).

In CPU rewrite mode, only the user ROM area shown in Figure 1.25.1 can be rewritten; the boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the user ROM area and each block area.

The control program for CPU rewrite mode can be stored in either user ROM or boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to any area other than the internal flash memory before it can be executed.

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the user ROM or boot ROM area in parallel I/O mode beforehand. (If the control program is written into the boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 1.25.1 for details about the boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVss pin low. In this case, the CPU starts operating using the control program in the user ROM area.

When the microcomputer is reset by pulling the P55 pin low, the CNVss pin high, and the P50 pin high, the CPU starts operating using the control program in the boot ROM area. This mode is called the "boot" mode. The control program in the boot ROM area can also be used to rewrite the user ROM area.

Block Address

Block addresses refer to the maximum even address of each block. These addresses are used in the block erase command, lock bit program command, and read lock status command.



Outline Performance (CPU Rewrite Mode)

In the CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. Operations must be executed from a memory other than the internal flash memory, such as the internal RAM.

When the CPU rewrite mode select bit (bit 1 at address 03B716) is set to "1", transition to CPU rewrite mode occurs and software commands can be accepted.

In the CPU rewrite mode, write to and read from software commands and data into even-numbered address ("0" for byte address A0) in 16-bit units. Always write 8-bit software commands into even-numbered address. Commands are ignored with odd-numbered addresses.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 1.26.1 shows the flash memory control register 0 and the flash memory control register 1.

Bit 0 of the flash memory control register 0 is the RY/BY status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0". Otherwise, it is "1".

Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. The CPU rewrite mode is entered by setting this bit to "1", so that software commands become acceptable. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, write bit 1 in an area other than the internal flash memory. Also only when $\overline{\text{NMI}}$ pin is "H" level. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. The bit can be set to "0" by only writing a "0".

Bit 2 of the flash memory control register 0 is a lock bit disable select bit. By setting this bit to "1", it is possible to disable erase and write protect (block lock) effectuated by the lock bit data. The lock bit disable select bit only disables the lock bit function; it does not change the lock data bit value. However, if an erase operation is performed when this bit ="1", the lock bit data that is "0" (locked) is set to "1" (unlocked) after erasure. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. This bit can be manipulated only when the CPU rewrite mode select bit = "1".

Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of the internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU rewrite mode select bit is "1", writing "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".

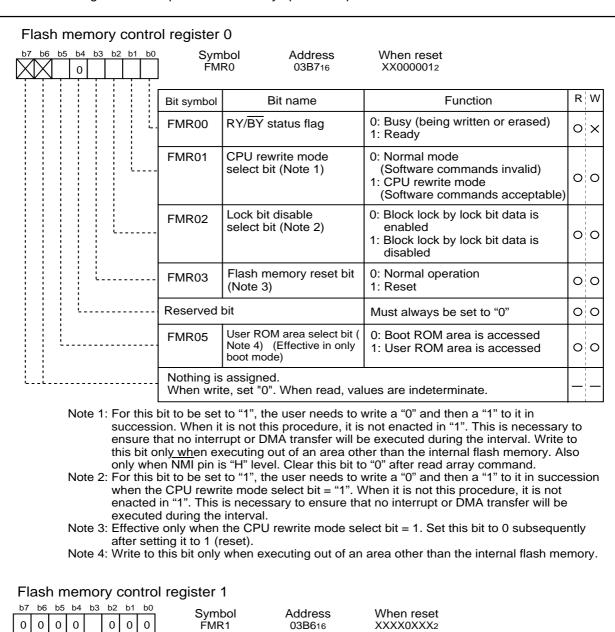
Bit 5 of the flash memory control register 0 is a user ROM area select bit which is effective in only boot mode. If this bit is set to "1" in boot mode, the area to be accessed is switched from the boot ROM area to the user ROM area. When the CPU rewrite mode needs to be used in boot mode, set this bit to "1". Note that if the microcomputer is booted from the user ROM area, it is always the user ROM area that can be accessed and this bit has no effect. When in boot mode, the function of this bit is effective regardless of whether the CPU rewrite mode is on or off. Write to this bit only when executing out of an area other than the internal flash memory.

Bit 3 of the flash memory control register 1 turns power supply to the internal flash memory on/off. When this bit is set to "1", power is not supplied to the internal flash memory, thus power consumption can be reduced. However, in this state, the internal flash memory cannot be accessed. To set this bit to "1", it is necessary to write "0" and then write "1" in succession. Use this bit mainly in the low speed mode (when XCIN is the count source of BCLK).

When the CPU is shifted to the stop or wait modes, power to the internal flash memory is automatically shut off. It is reconnected automatically when CPU operation is restored. Therefore, it is not particularly necessary to set flash memory control register 1.



Figure 1.26.2 shows a flowchart for setting/releasing the CPU rewrite mode. Figure 1.26.3 shows a flow-chart for shifting to the low speed mode. Always perform operation as indicated in these flowcharts.



R W Bit symbol Bit name **Function** Reserved bit Must always be set to "0" 0 FMR13 Flash memory power Flash memory power supply is 0:0 supply-OFF bit (Note) connected 1: Flash memory power supply-off Reserved bit Must always be set to "0" 0

Note: For this bit to be set to "1", the user needs to write a "0" and then a "1" to it in succession. When it is not this procedure, it is not enacted in "1". This is necessary to ensure that no interrupt or DMA transfer will be executed during the interval. During parallel I/O mode,programming,erase or read of flash memory is not controlled by this bit,only by external pins. Write to this bit only when executing out of an area other than the internal flash memory.

Figure 1.26.1. Flash memory control registers



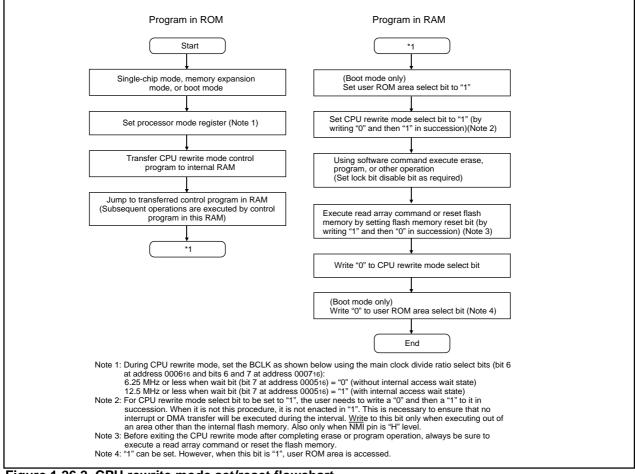


Figure 1.26.2. CPU rewrite mode set/reset flowchart

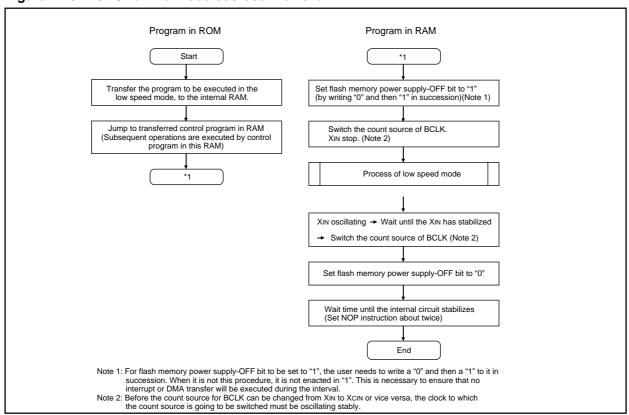


Figure 1.26.3. Shifting to the low speed mode flowchart

Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During CPU rewrite mode, set the BCLK as shown below using the main clock divide ratio select bit (bit 6 at address 000616 and bits 6 and 7 at address 000716):

6.25 MHz or less when wait bit (bit 7 at address 000516) = 0 (without internal access wait state)

12.5 MHz or less when wait bit (bit 7 at address 000516) = 1 (with internal access wait state)

(2) Instructions inhibited against use

The instructions listed below cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory:

UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction

(3) Interrupts inhibited against use

The address match interrupt cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory. If interrupts have their vector in the variable vector table, they can be used by transferring the vector into the RAM area. The $\overline{\text{NMI}}$ and watchdog timer interrupts can be used because the flash memory conterol register 0 and 1 is forcibly initialized and return to normal mode when each interrupt occurs. But it is needed that the jump addresses for each interrupt are set in the fixed vector table and there is an interrupt program. Since the rewrite operation is halted when the $\overline{\text{NMI}}$ and watchdog timer interrupts occur, it is needed that CPU rewriting mode select bit is set to "1" and the erase/program operation is performed over again.

(4) Internal reserved area expansion bit (Bit 3 at address 000516)

The reserved area of the internal memory can be changed by using the internal reserved area expansion bit (bit 3 at address 000516). However, if the CPU rewrite mode select bit (bit 1 at address 03B716) is set to 1, the internal reserved area expansion bit (bit 3 at address 000516) also is set to 1 automatically. Similarly, if the CPU rewrite mode select bit (bit 1 at address 03B716) is set to 0, the internal reserved area expansion bit (bit 3 at address 000516) also is set to 0 automatically.

The precautions above apply to the products which RAM size is over 15 Kbytes or flash memory size is over 192 Kbytes.

(5) Reset

Reset input is always accepted. After a reset, the addresses 0C000016 through 0CFFF16 are made a reserved area and cannot be accessed. Therefore, if your product has this area in the user ROM area, do not write any address of this area to the reset vector. This area is made accessible by changing the internal reserved area expansion bit (bit 3 at address 000516) in a program.

(6) Access disable

Write CPU rewrite mode select bit, flash memory power supply-OFF bit and user ROM area select bit only when executing out of an area other than the internal flash memory.

(7) How to access

For CPU rewrite mode select bit, lock bit disable select bit, and flash memory power supply-OFF bit to be set to "1", the user needs to write a "0" and then a "1" to it in succession. When it is not this procedure, it is not enacted in "1". This is necessary to ensure that no interrupt or DMA transfer will be executed during the interval.

Write CPU rewrite mode select bit only when executing out of an area other than the internal flash memory. Also only when $\overline{\text{NMI}}$ pin is "H" level.



(8) Writing in the user ROM area

If power is lost while rewriting blocks that contain the flash rewrite program with the CPU rewrite mode, those blocks may not be correctly rewritten and it is possible that the flash memory can no longer be rewritten after that. Therefore, it is recommended to use the standard serial I/O mode or parallel I/O mode to rewrite these blocks.

(9) Using the lock bit

To use the CPU rewrite mode, use a boot program that can set and cancel the lock command.



Software Commands

Table 1.26.1 lists the software commands available with the M16C/62A (flash memory version). After setting the CPU rewrite mode select bit to 1, write a software command to specify an erase or program operation. Note that when entering a software command, the upper byte (D8 to D15) is ignored. The content of each software command is explained below.

Table 1.26.1. List of software commands (CPU rewrite mode)

	First bus cycle		Second bus cycle			Third bus cycle			
Command	Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)	Mode	Address	Data (D ₀ to D ₇)
Read array	Write	X (Note 6)	FF16						
Read status register	Write	X	7016	Read	X	SRD (Note 2)			
Clear status register	Write	Х	5016						
Page program (Note 3)	Write	Х	41 16	Write	WA0(Note 3)	WD0 (Note 3)	Write	WA1	WD1
Block erase	Write	Х	2016	Write	BA (Note 4)	D016			
Erase all unlock block	Write	Х	A716	Write	Х	D016			
Lock bit program	Write	Х	7716	Write	ВА	D016			
Read lock bit status	Write	Х	7116	Read	ВА	D ₆ (Note 5)			

- Note 1: When a software command is input, the high-order byte of data (D8 to D15) is ignored.
- Note 2: SRD = Status Register Data
- Note 3: WA = Write Address, WD = Write Data
 - WA and WD must be set sequentially from 0016 to FE16 (byte address; however, an even address). The page size is 256 bytes.
- Note 4: BA = Block Address (Enter the maximum address of each block that is an even address.)
- Note 5: D6 corresponds to the block lock status. Block not locked when D6 = 1, block locked when D6 = 0.
- Note 6: X denotes a given address in the user ROM area (that is an even address).

Read Array Command (FF16)

The read array mode is entered by writing the command code "FF16" in the first bus cycle. When an even address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data bus (D0–D15), 16 bits at a time.

The read array mode is retained intact until another command is written.

Read Status Register Command (7016)

When the command code "7016" is written in the first bus cycle, the content of the status register is read out at the data bus (D0–D7) by a read in the second bus cycle.

The status register is explained in the next section.

Clear Status Register Command (5016)

This command is used to clear the bits SR3 to 5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "5016" in the first bus cycle.



Page Program Command (4116)

Page program allows for high-speed programming in units of 256 bytes. Page program operation starts when the command code "4116" is written in the first bus cycle. In the second bus cycle through the 129th bus cycle, the write data is sequentially written 16 bits at a time. At this time, the addresses A0-A7 need to be incremented by 2 from "0016" to "FE16." When the system finishes loading the data, it starts an auto write operation (data program and verify operation).

Whether the auto write operation is completed can be confirmed by reading the status register or the flash memory control register 0. At the same time the auto write operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to 0 at the same time the auto write operation starts and is returned to 1 upon completion of the auto write operation. In this case, the read status register mode remains active until the Read Array command (FF16) or Read Lock Bit Status command (7116) is written or the flash memory is reset using its reset bit.

The RY/BY status flag of the flash memory control register 0 is 0 during auto write operation and 1 when the auto write operation is completed as is the status register bit 7.

After the auto write operation is completed, the status register can be read out to know the result of the auto write operation. For details, refer to the section where the status register is detailed.

Figure 1.26.4 shows an example of a page program flowchart.

Each block of the flash memory can be write protected by using a lock bit. For details, refer to the section where the data protect function is detailed.

Additional writes to the already programmed pages are prohibited.

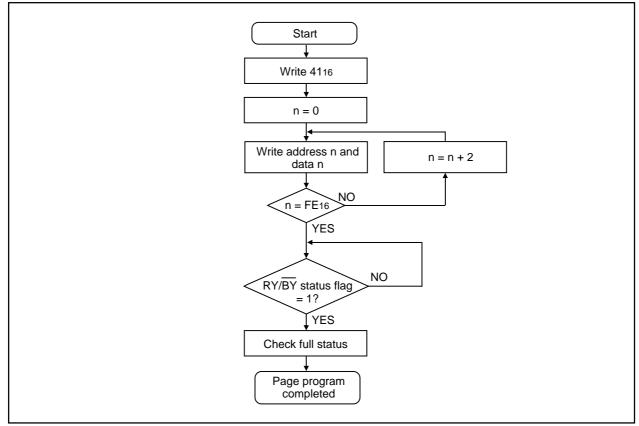


Figure 1.26.4. Page program flowchart



Block Erase Command (2016/D016)

By writing the command code "2016" in the first bus cycle and the confirmation command code "D016" in the second bus cycle that follows to the block address of a flash memory block, the system initiates an auto erase (erase and erase verify) operation.

Whether the auto erase operation is completed can be confirmed by reading the status register or the flash memory control register 0. At the same time the auto erase operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to 0 at the same time the auto erase operation starts and is returned to 1 upon completion of the auto erase operation. In this case, the read status register mode remains active until the Read Array command (FF16) or Read Lock Bit Status command (7116) is written or the flash memory is reset using its reset bit.

The RY/BY status flag of the flash memory control register 0 is 0 during auto erase operation and 1 when the auto erase operation is completed as is the status register bit 7.

After the auto erase operation is completed, the status register can be read out to know the result of the auto erase operation. For details, refer to the section where the status register is detailed.

Figure 1.26.5 shows an example of a block erase flowchart.

Each block of the flash memory can be protected against erasure by using a lock bit. For details, refer to the section where the data protect function is detailed.

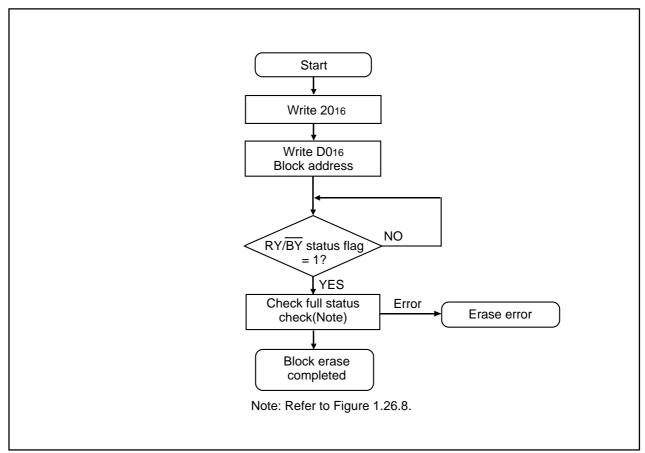


Figure 1.26.5. Block erase flowchart



Erase All Unlock Blocks Command (A716/D016)

By writing the command code "A716" in the first bus cycle and the confirmation command code "D016" in the second bus cycle that follows, the system starts erasing blocks successively.

Whether the erase all unlock blocks command is terminated can be confirmed by reading the status register or the flash memory control register 0, in the same way as for block erase. Also, the status register can be read out to know the result of the auto erase operation.

When the lock bit disable select bit of the flash memory control register 0 = 1, all blocks are erased no matter how the lock bit is set. On the other hand, when the lock bit disable select bit = 0, the function of the lock bit is effective and only nonlocked blocks (where lock bit data = 1) are erased.

Lock Bit Program Command (7716/D016)

By writing the command code "7716" in the first bus cycle and the confirmation command code "D016" in the second bus cycle that follows to the block address of a flash memory block, the system sets the lock bit for the specified block to 0 (locked).

Figure 1.26.6 shows an example of a lock bit program flowchart. The status of the lock bit (lock bit data) can be read out by a read lock bit status command.

Whether the lock bit program command is terminated can be confirmed by reading the status register or the flash memory control register 0, in the same way as for page program.

For details about the function of the lock bit and how to reset the lock bit, refer to the section where the data protect function is detailed.

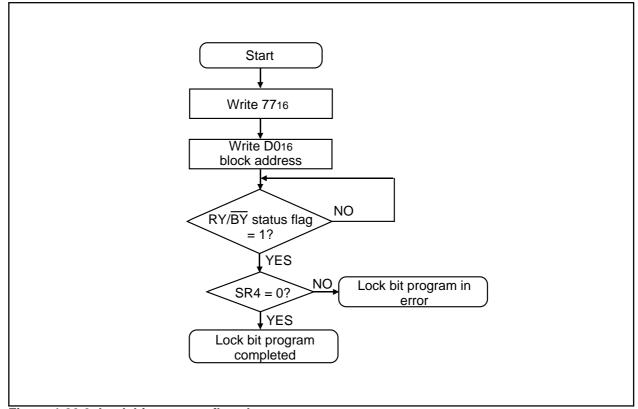


Figure 1.26.6. Lock bit program flowchart



Read Lock Bit Status Command (7116)

By writing the command code "7116" in the first bus cycle and then the block address of a flash memory block in the second bus cycle that follows, the system reads out the status of the lock bit of the specified block on to the data bus(D6).

Figure 1.26.7 shows an example of a read lock bit program flowchart.

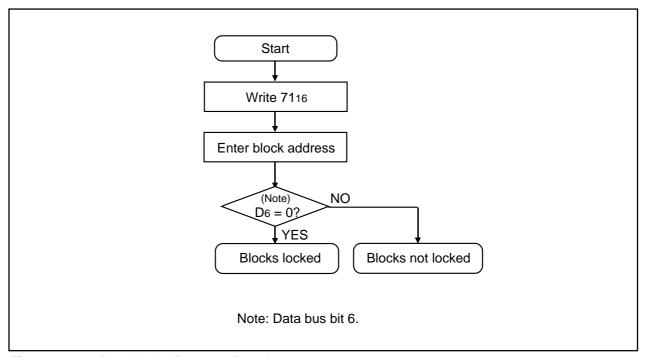


Figure 1.26.7. Read lock bit status flowchart

Data Protect Function (Block Lock)

Each block in Figure 1.25.1 has a nonvolatile lock bit to specify that the block be protected (locked) against erase/write. The lock bit program command is used to set the lock bit to 0 (locked). The lock bit of each block can be read out using the read lock bit status command.

Whether block lock is enabled or disabled is determined by the status of the lock bit and how the flash memory control register 0's lock bit disable select bit is set.

- (1) When the lock bit disable select bit = "0", a specified block can be locked or unlocked by the lock bit status (lock bit data). Blocks whose lock bit data = "0" are locked, so they are disabled against erase/write. On the other hand, the blocks whose lock bit data = "1" are not locked, so they are enabled for erase/write.
- (2) When the lock bit disable select bit = "1", all blocks are nonlocked regardless of the lock bit data, so they are enabled for erase/write. In this case, the lock bit data that is "0" (locked) is set to "1" (nonlocked) after erasure, so that the lock bit-actuated lock is removed.

Status Register

The status register indicates the operating status of the flash memory and whether an erase or program operation has terminated normally or in an error. The content of this register can be read out by only writing the read status register command (7016). Table 1.26.2 details the status register.

The status register is cleared by writing the Clear Status Register command (5016).

After a reset, the status register is set to "8016."

Each bit in this register is explained below.

Write state machine (WSM) status (SR7)

After power-on, the write state machine (WSM) status is set to "1".

The write state machine (WSM) status indicates the operating status of the device, as for output on the RY/BY pin. This status bit is set to "0" during auto write or auto erase operation and is set to "1" upon completion of these operations.

Erase status (SR5)

The erase status informs the operating status of auto erase operation to the CPU. When an erase error occurs, it is set to "1".

The erase status is reset to "0" when cleared.



Program status (SR4)

The program status informs the operating status of auto write operation to the CPU. When a write error occurs, it is set to "1".

The program status is reset to "0" when cleared.

When an erase command is in error (which occurs if the command entered after the block erase command (2016) is not the confirmation command (D016), both the program status and erase status (SR5) are set to "1".

When the program status or erase status = "1", only the following flash commands will be accepted: Read Array, Read Status Register, and Clear Status Register.

Also, in one of the following cases, both SR4 and SR5 are set to "1" (command sequence error):

- (1) When the valid command is not entered correctly
- (2) When the data entered in the second bus cycle of lock bit program (7716/D016), block erase (2016/D016), or erase all unlock blocks (A716/D016) is not the D016 or FF16. However, if FF16 is entered, read array is assumed and the command that has been set up in the first bus cycle is canceled.

Block status after program (SR3)

If excessive data is written (phenomenon whereby the memory cell becomes depressed which results in data not being read correctly), "1" is set for the program status after-program at the end of the page write operation. In other words, when writing ends successfully, "8016" is output; when writing fails, "9016" is output; and when excessive data is written, "8816" is output.

Table 1.26.2. Definition of each bit in status register

Each bit of	_	Definition		
SRD	SRD Status name		"0"	
SR7 (bit7)	Write state machine (WSM) status	Ready	Busy	
SR6 (bit6)	Reserved	-	-	
SR5 (bit5)	Erase status	Terminated in error	Terminated normally	
SR4 (bit4)	Program status	Terminated in error	Terminated normally	
SR3 (bit3)	Block status after program	Terminated in error	Terminated normally	
SR2 (bit2)	Reserved	-	-	
SR1 (bit1)	Reserved	-	-	
SR0 (bit0)	Reserved	-	-	



Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 1.26.8 shows a full status check flowchart and the action to be taken when each error occurs.

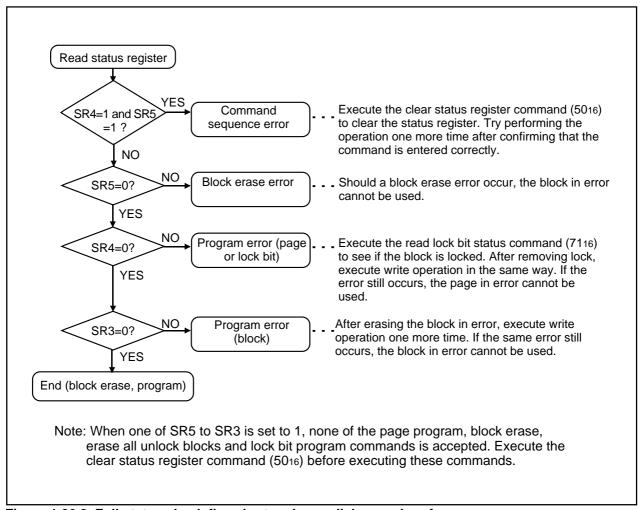


Figure 1.26.8. Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

To prevent the contents of the flash memory version from being read out or rewritten easily, the device incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

ROM code protect function

The ROM code protect function is used to prohibit reading out or modifying the contents of the flash memory during parallel I/O mode and is set by using the ROM code protect control address register (0FFFFF16). Figure 1.27.1 shows the ROM code protect control address (0FFFFF16). (This address exists in the user ROM area.)

If one of the pair of ROM code protect bits is set to 0, ROM code protect is turned on, so that the contents of the flash memory version are protected against readout and modification. ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to "00," ROM code protect is turned off, so that the contents of the flash memory version can be read out or modified. Once ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or some other mode to rewrite the contents of the ROM code protect reset bits.

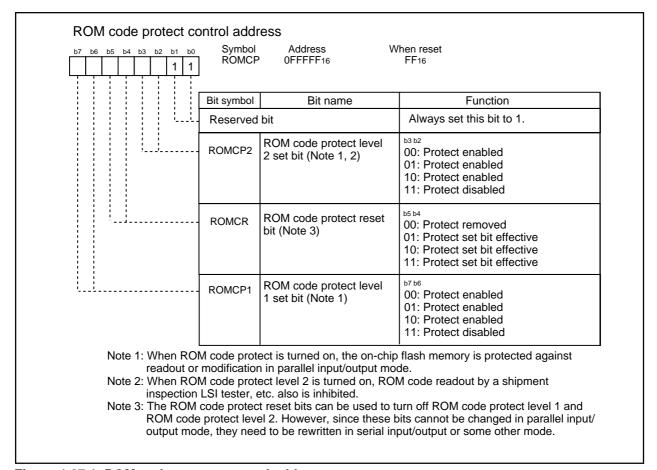


Figure 1.27.1. ROM code protect control address



ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the peripheral unit is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the peripheral unit are not accepted. The ID code consists of 8-bit data, the areas of which, beginning with the first byte, are 0FFFDF16, 0FFFE316, 0FFFE316, 0FFFEB16, 0FFFEB16. Write a program which has had the ID code preset at these addresses to the flash memory.

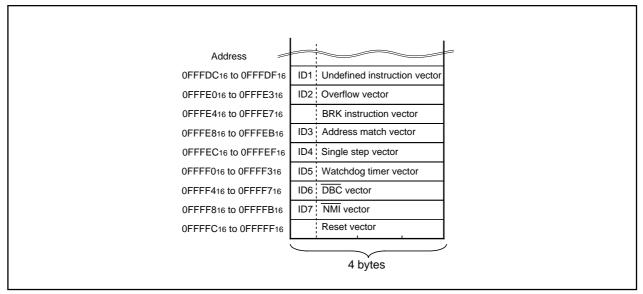


Figure 1.27.2. ID code store addresses

Parallel I/O Mode

The parallel I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is parallel.

Use an exclusive programer supporting M16C/62A (flash memory version).

Refer to the instruction manual of each programer maker for the details of use.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 1.25.1 can be rewritten. Both areas of flash memory can be operated on in the same way.

Program and block erase operations can be performed in the user ROM area. The user ROM area and its blocks are shown in Figure 1.25.1.

The boot ROM area is 8 Kbytes in size. In parallel I/O mode, it is located at addresses 0FE00016 through 0FFFF16. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the boot ROM area, an erase block operation is applied to only one 8 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Mitsubishi factory. Therefore, using the device in standard serial input/output mode, you do not need to write to the boot ROM area.



Pin functions (Flash memory standard serial I/O mode)

Pin	Name	I/O	Description
Vcc,Vss	Power input		Apply program/erase protection voltage to Vcc pin and 0 V to Vss pin.
CNVss	CNVss	ı	Connect to Vcc pin.
RESET	Reset input	I	Reset input pin. While reset is "L" level, a 20 cycle or longer clock must be input to XIN pin.
XIN	Clock input	ı	Connect a ceramic resonator or crystal oscillator between XIN and XOUT pins. To input an externally generated clock, input it to XIN pin
Хоит	Clock output	0	and open Xout pin.
BYTE	BYTE	ı	Connect this pin to Vss or Vcc.
AVcc, AVss	Analog power supply input		Connect AVss to Vss and AVcc to Vcc, respectively.
VREF	Reference voltage input	I	Enter the reference voltage for AD from this pin.
P00 to P07	Input port P0	ı	Input "H" or "L" level signal or open.
P10 to P17	Input port P1	ı	Input "H" or "L" level signal or open.
P20 to P27	Input port P2	I	Input "H" or "L" level signal or open.
P30 to P37	Input port P3	ı	Input "H" or "L" level signal or open.
P40 to P47	Input port P4	ı	Input "H" or "L" level signal or open.
P51 to P54, P56, P57	Input port P5	I	Input "H" or "L" level signal or open.
P50	CE input	ı	Input "H" level signal.
P55	EPM input	ı	Input "L" level signal.
P60 to P63	Input port P6	I	Input "H" or "L" level signal or open.
P64	BUSY output	0	Standard serial I/O mode 1: BUSY signal output pin Standard serial I/O mode 2: Monitors the boot program operation check signal output pin.
P65	SCLK input	I	Standard serial I/O mode 1: Serial clock input pin Standard serial I/O mode 2: Input "L".
P66	RxD input	ı	Serial data input pin
P67	TxD output	0	Serial data output pin
P70 to P77	Input port P7	ı	Input "H" or "L" level signal or open.
P80 to P84, P86, P87	Input port P8	I	Input "H" or "L" level signal or open.
P85	NMI input	ı	Connect this pin to Vcc.
P90 to P97	Input port P9	ı	Input "H" or "L" level signal or open.
P100 to P107	Input port P10	ı	Input "H" or "L" level signal or open.



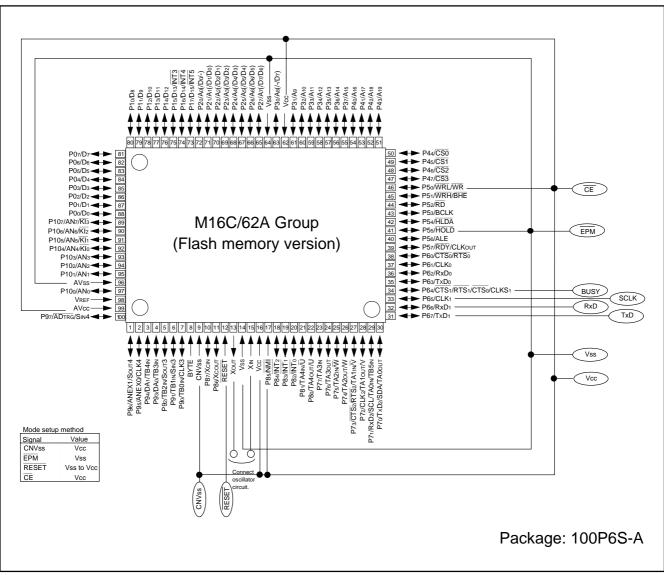


Figure 1.29.1. Pin connections for serial I/O mode (1)

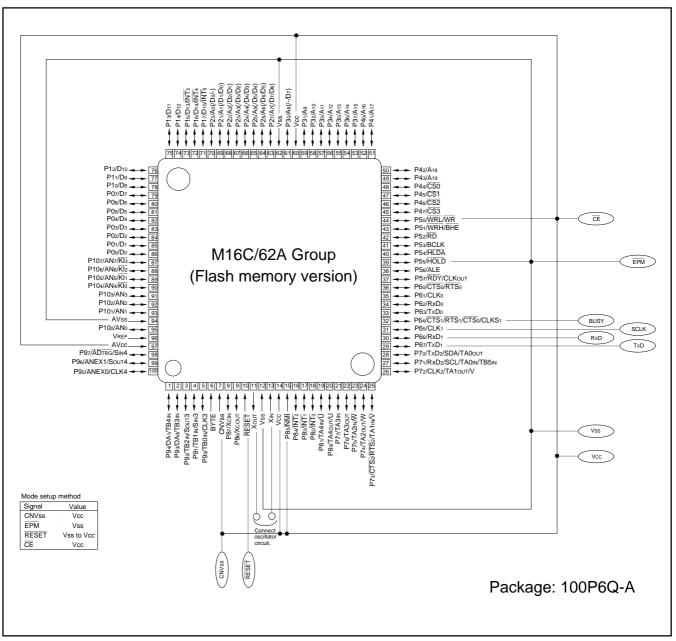


Figure 1.29.2. Pin connections for serial I/O mode (2)

Standard serial I/O mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is serial. There are actually two standard serial I/O modes: mode 1, which is clock synchronized, and mode 2, which is asynchronized. Both modes require a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU's rewrite mode), rewrite data input and so forth. It is started when the reset is released, which is done when the P50 ($\overline{\text{CE}}$) pin is "H" level, the P55 ($\overline{\text{EPM}}$) pin "L" level and the CNVss pin "H" level. (In the ordinary command mode, set CNVss pin to "L" level.)

This control program is written in the boot ROM area when the product is shipped from Mitsubishi. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the boot ROM area is rewritten in the parallel I/O mode. Figures 1.29.1 and 1.29.2 show the pin connections for the standard serial I/O mode. Serial data I/O uses UART1 and transfers the data serially in 8-bit units. Standard serial I/O switches between mode 1 (clock synchronized) and mode 2 (clock asynchronized) according to the level of CLK1 pin when the reset is released.

To use standard serial I/O mode 1 (clock synchronized), set the CLK1 pin to "H" level and release the reset. The operation uses the four UART1 pins CLK1, RxD1, TxD1 and RTS1 (BUSY). The CLK1 pin is the transfer clock input pin through which an external transfer clock is input. The TxD1 pin is for CMOS output. The RTS1 (BUSY) pin outputs an "L" level when ready for reception and an "H" level when reception starts.

To use standard serial I/O mode 2 (clock asynchronized), set the CLK1 pin to "L" level and release the reset. The operation uses the two UART1 pins RxD1 and TxD1.

In the standard serial I/O mode, only the user ROM area indicated in Figure 1.29.19 can be rewritten. The boot ROM cannot.

In the standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit are not accepted unless the ID code matches.



Overview of standard serial I/O mode 1 (clock synchronized)

In standard serial I/O mode 1, software commands, addresses and data are input and output between the MCU and peripheral units (serial programer, etc.) using 4-wire clock-synchronized serial I/O (UART1). Standard serial I/O mode 1 is engaged by releasing the reset with the P65 (CLK1) pin "H" level.

In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the CLK1 pin, and are then input to the MCU via the RxD1 pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD1 pin.

The TxD1 pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the RTS1 (BUSY) pin is "H" level. Accordingly, always start the next transfer after the RTS1 (BUSY) pin is "L" level.

Also, data and status registers in memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained software commands, status registers, etc.



Software Commands

Table 1.29.1 lists software commands. In the standard serial I/O mode 1, erase operations, programs and reading are controlled by transferring software commands via the RxD1 pin. Software commands are explained here below.

Table 1.29.1. Software commands (Standard serial I/O mode 1)

	Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte		When ID is not verified
1	Page read	FF ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41 ₁₆	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Block erase	2016	Address (middle)	Address (high)	D0 ₁₆				Not acceptable
4	Erase all unlocked blocks	A7 ₁₆	D0 ₁₆						Not acceptable
5	Read status register	7016	SRD output	SRD1 output					Acceptable
6	Clear status register	5016							Not acceptable
7	Read lock bit status	71 ₁₆	Address (middle)	Address (high)	Lock bit data output				Not acceptable
8	Lock bit program	7716	Address (middle)	Address (high)	D0 ₁₆				Not acceptable
9	Lock bit enable	7A ₁₆							Not acceptable
10	Lock bit disable	7516							Not acceptable
11	ID check function	F5 ₁₆	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
12	Download function	FA ₁₆	Size (low)	Size (high)	Check- sum	Data input	To required number of times		Not acceptable
13	Version data output function	FB ₁₆	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable
14	Boot ROM area output function	FC ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
15	Read check data	FD ₁₆	Check data (low)	Check data (high)					Not acceptable

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.



Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.

Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first in sync with the fall of the clock.

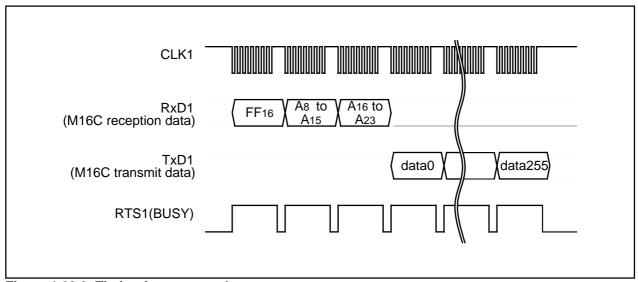


Figure 1.29.3. Timing for page read

Read Status Register Command

This command reads status information. When the "7016" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

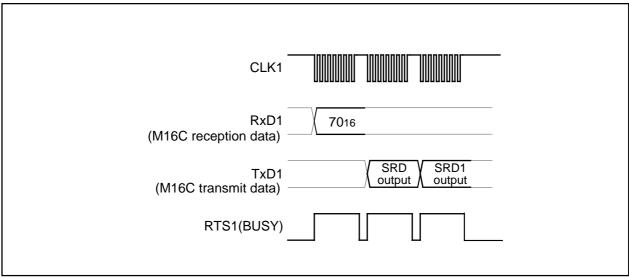


Figure 1.29.4. Timing for reading the status register



Clear Status Register Command

This command clears the bits (SR3–SR5) which are set when the status register operation ends in error. When the "5016" command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the RTS1 (BUSY) signal changes from the "H" to the "L" level.

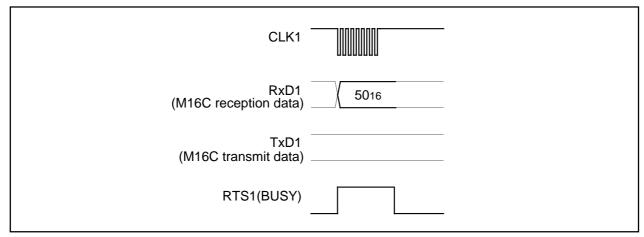


Figure 1.29.5. Timing for clearing the status register

Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the "4116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the RTS1 (BUSY) signal changes from the "H" to the "L" level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

Each block can be write-protected with the lock bit. For more information, see the section on the data protection function. Additional writing is not allowed with already programmed pages.

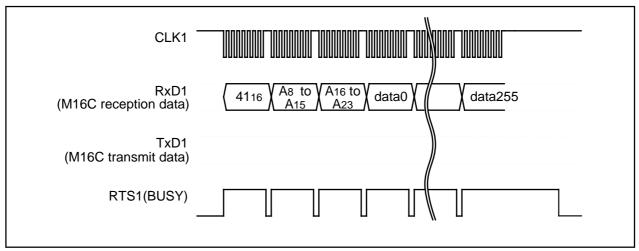


Figure 1.29.6. Timing for the page program



Block Erase Command

This command erases the data in the specified block. Execute the block erase command as explained here following.

- (1) Transfer the "2016" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) Transfer the verify command code "D016" with the 4th byte. With the verify command code, the erase operation will start for the specified block in the flash memory. Write the highest address of the specified block for addresses A8 to A23.

When block erasing ends, the RTS1 (BUSY) signal changes from the "H" to the "L" level. After block erase ends, the result of the block erase operation can be known by reading the status register. For more information, see the section on the status register.

Each block can be erase-protected with the lock bit. For more information, see the section on the data protection function.

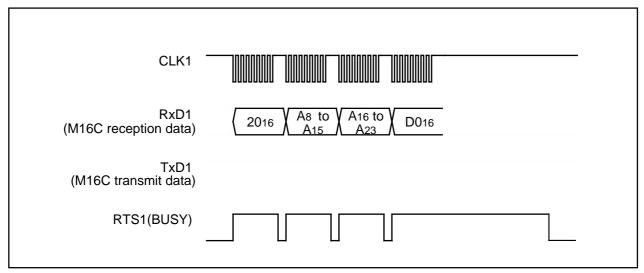


Figure 1.29.7. Timing for block erasing



Erase All Unlocked Blocks Command

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A716" command code with the 1st byte.
- (2) Transfer the verify command code "D016" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When block erasing ends, the RTS1 (BUSY) signal changes from the "H" to the "L" level. The result of the erase operation can be known by reading the status register. Each block can be erase-protected with the lock bit. For more information, see the section on the data protection function.

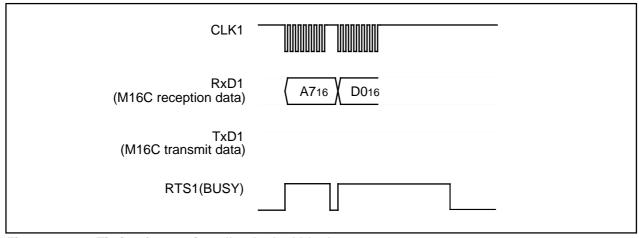


Figure 1.29.8. Timing for erasing all unlocked blocks

Lock Bit Program Command

This command writes "0" (lock) for the lock bit of the specified block. Execute the lock bit program command as explained here following.

- (1) Transfer the "7716" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) Transfer the verify command code "D016" with the 4th byte. With the verify command code, "0" is written for the lock bit of the specified block. Write the highest address of the specified block for addresses A8 to A23.

When writing ends, the RTS1 (BUSY) signal changes from the "H" to the "L" level. Lock bit status can be read with the read lock bit status command. For information on the lock bit function, reset procedure and so on, see the section on the data protection function.

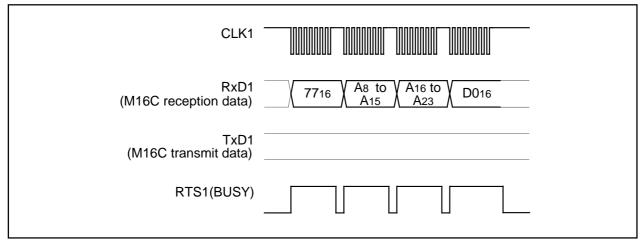


Figure 1.29.9. Timing for the lock bit program



Read Lock Bit Status Command

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "7116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. The lock bit data is the 6th bit(D6) of the output data. Write the highest address of the specified block for addresses A8 to A23.

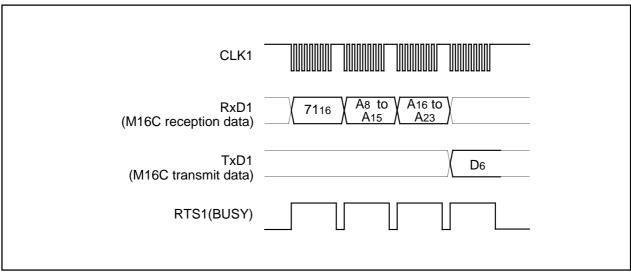


Figure 1.29.10. Timing for reading lock bit status

Lock Bit Enable Command

This command enables the lock bit in blocks whose bit was disabled with the lock bit disable command. The command code "7A16" is sent with the 1st byte of the serial transmission. This command only enables the lock bit function; it does not set the lock bit itself.

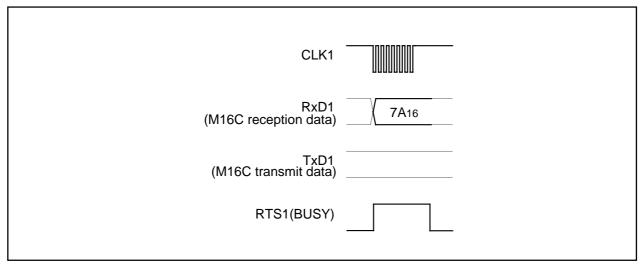


Figure 1.29.11. Timing for enabling the lock bit



Lock Bit Disable Command

This command disables the lock bit. The command code "7516" is sent with the 1st byte of the serial transmission. This command only disables the lock bit function; it does not set the lock bit itself. However, if an erase command is executed after executing the lock bit disable command, "0" (locked) lock bit data is set to "1" (unlocked) after the erase operation ends. In any case, after the reset is cancelled, the lock bit is enabled.

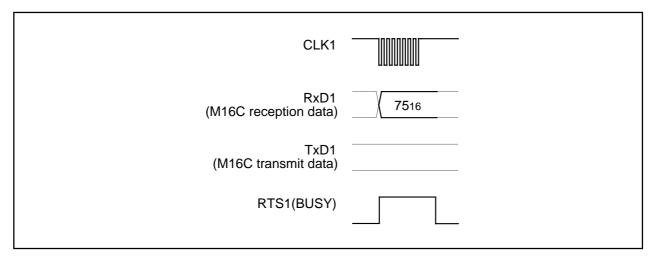


Figure 1.29.12. Timing for disabling the lock bit

Download Command

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

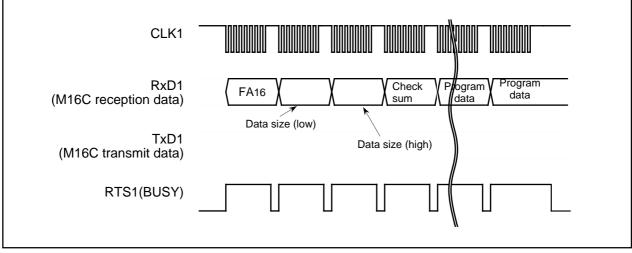


Figure 1.29.13. Timing for download



Version Information Output Command

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

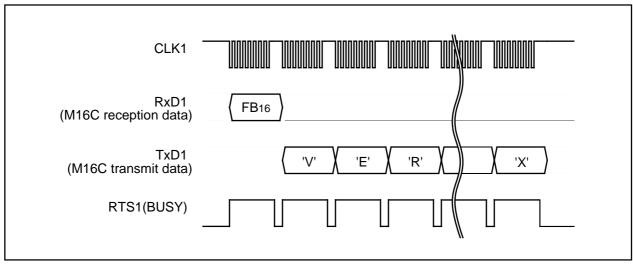


Figure 1.29.14. Timing for version information output

Boot ROM Area Output Command

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first, in sync with the fall of the clock.

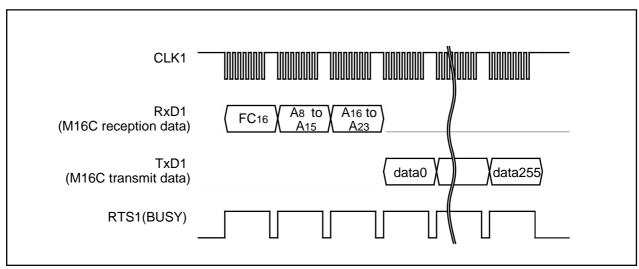


Figure 1.29.15. Timing for boot ROM area output



ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the "F516" command code with the 1st byte.
- (2) Transfer addresses A₀ to A₇, A₈ to A₁₅ and A₁₆ to A₂₃ of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

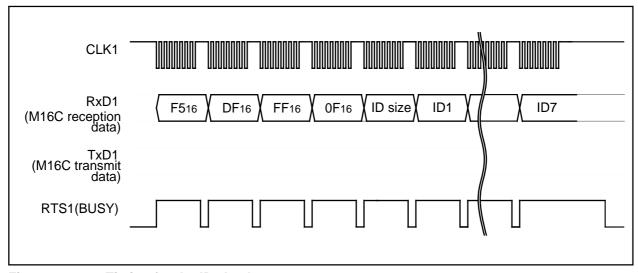


Figure 1.29.16. Timing for the ID check

ID Code

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFDF16, 0FFFE316, 0FFFEB16, 0FFFEF16, 0FFFF316, 0FFFF716 and 0FFFFB16. Write a program into the flash memory, which already has the ID code set for these addresses.

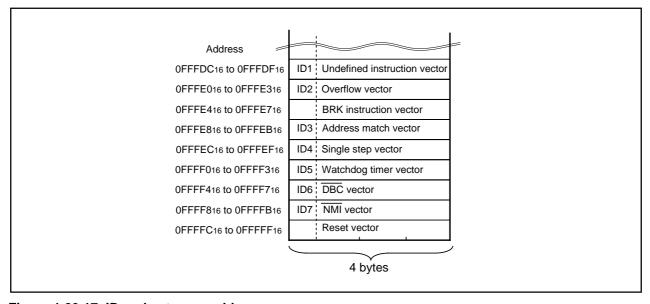


Figure 1.29.17. ID code storage addresses



Read Check Data

This command reads the check data that confirms that the write data, which was sent with the page program command, was successfully received.

- (1) Transfer the "FD16" command code with the 1st byte.
- (2) The check data (low) is received with the 2nd byte and the check data (high) with the 3rd.

To use this read check data command, first execute the command and then initialize the check data. Next, execute the page program command the required number of times. After that, when the read check command is executed again, the check data for all of the read data that was sent with the page program command during this time is read. The check data is the result of CRC operation of write data.

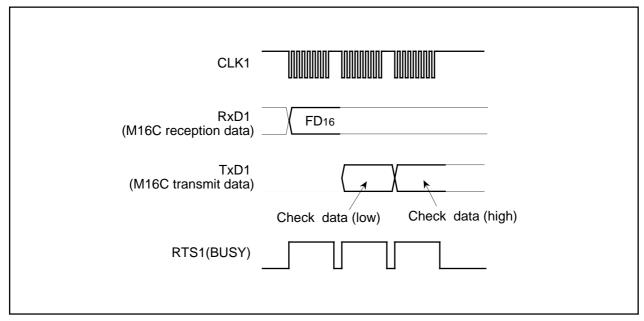


Figure 1.29.18. Timing for the read check data

Data Protection (Block Lock)

Each of the blocks in Figure 1.29.19 have a nonvolatile lock bit that specifies protection (block lock) against erasing/writing. A block is locked (writing "0" for the lock bit) with the lock bit program command. Also, the lock bit of any block can be read with the read lock bit status command.

Block lock disable/enable is determined by the status of the lock bit itself and execution status of the lock bit disable and lock enable bit commands.

- (1) After the reset has been cancelled and the lock bit enable command executed, the specified block can be locked/unlocked using the lock bit (lock bit data). Blocks with a "0" lock bit data are locked and cannot be erased or written in. On the other hand, blocks with a "1" lock bit data are unlocked and can be erased or written in.
- (2) After the lock bit disable command has been executed, all blocks are unlocked regardless of lock bit data status and can be erased or written in. In this case, lock bit data that was "0" (locked) before the block was erased is set to "1" (unlocked) after erasing, therefore the block is actually unlocked with the lock bit.

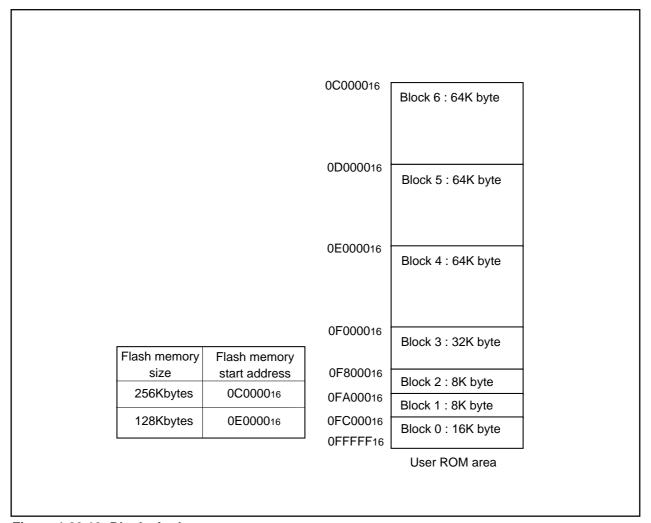


Figure 1.29.19. Blocks in the user area



Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (7016). Also, the status register is cleared by writing the clear status register command (5016). Table 1.29.2 gives the definition of each status register bit. After clearing the reset, the status register outputs "8016".

Table 1.29.2. Status register (SRD)

000011	0	Definition		
SRD0 bits	Status name	"1"	"0"	
SR7 (bit7)	Write state machine (WSM) status	Ready	Busy	
SR6 (bit6)	Reserved	-	-	
SR5 (bit5)	Erase status	Terminated in error	Terminated normally	
SR4 (bit4)	Program status	Terminated in error	Terminated normally	
SR3 (bit3)	Block status after program	Terminated in error	Terminated normally	
SR2 (bit2)	Reserved	-	-	
SR1 (bit1)	Reserved	-	-	
SR0 (bit0)	Reserved	-	-	

Write State Machine (WSM) Status (SR7)

The write state machine (WSM) status indicates the operating status of the flash memory. When power is turned on, "1" (ready) is set for it. The bit is set to "0" (busy) during an auto write or auto erase operation, but it is set back to "1" when the operation ends.

Erase Status (SR5)

The erase status reports the operating status of the auto erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

Program Status (SR4)

The program status reports the operating status of the auto write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

Block Status After Program (SR3)

If excessive data is written (phenomenon whereby the memory cell becomes depressed which results in data not being read correctly), "1" is set for the block status after-program at the end of the page write operation. In other words, when writing ends successfully, "8016" is output; when writing fails, "9016" is output; and when excessive data is written, "8816" is output.

If "1" is written for any of the SR5, SR4 or SR3 bits, the page program, block erase, erase all unlocked blocks and lock bit program commands are not accepted. Before executing these commands, execute the clear status register command (5016) and clear the status register.



Status Register 1 (SRD1)

Status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the SRD by writing the read status register command (7016). Also, status register 1 is cleared by writing the clear status register command (5016).

Table 1.29.3 gives the definition of each status register 1 bit. "0016" is output when power is turned ON and the flag status is maintained even after the reset.

Table 1.29.3. Status register 1 (SRD1)

SRD1 bits	Otatus name	Definition	
SKUT DIIS	Status name	"1"	"0"
SR15 (bit7)	Boot update completed bit	Update completed	Not update
SR14 (bit6)	Reserved	-	-
SR13 (bit5)	Reserved	-	-
SR12 (bit4)	Check sum match bit	Match	Mismatch
SR11 (bit3)	ID check completed bits		verified
SR10 (bit2)		1	ication mismatch
		10 Reserved 11 Verified	
		1	
SR9 (bit1)	Data receive time out	Time out	Normal operation
SR8 (bit0)	Reserved	-	-

Boot Update Completed Bit (SR15)

This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

Check Sum Match Bit (SR12)

This flag indicates whether the check sum matches or not when a program, is downloaded for execution using the download function.

ID Check Completed Bits (SR11 and SR10)

These flags indicate the result of ID checks. Some commands cannot be accepted without an ID check.

Data Receive Time Out (SR9)

This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the microcomputer returns to the command wait state.



Full Status Check

Results from executed erase and program operations can be known by running a full status check. Figure 1.29.20 shows a flowchart of the full status check and explains how to remedy errors which occur.

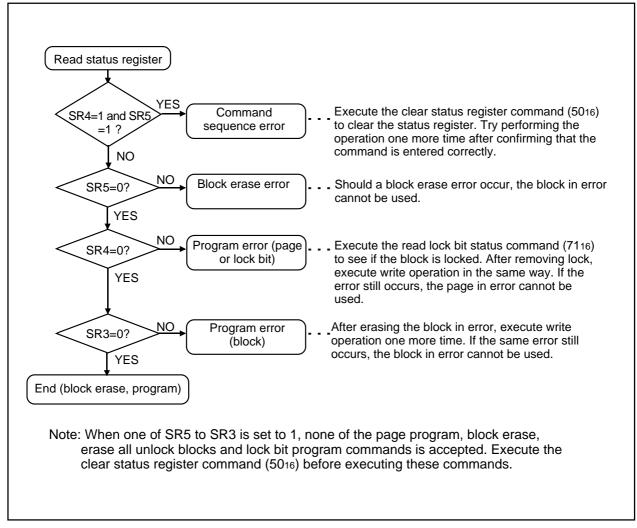


Figure 1.29.20. Full status check flowchart and remedial procedure for errors



Example Circuit Application for The Standard Serial I/O Mode 1

The below figure shows a circuit application for the standard serial I/O mode 1. Control pins will vary according to programmer, therefore see the peripheral unit manual for more information.

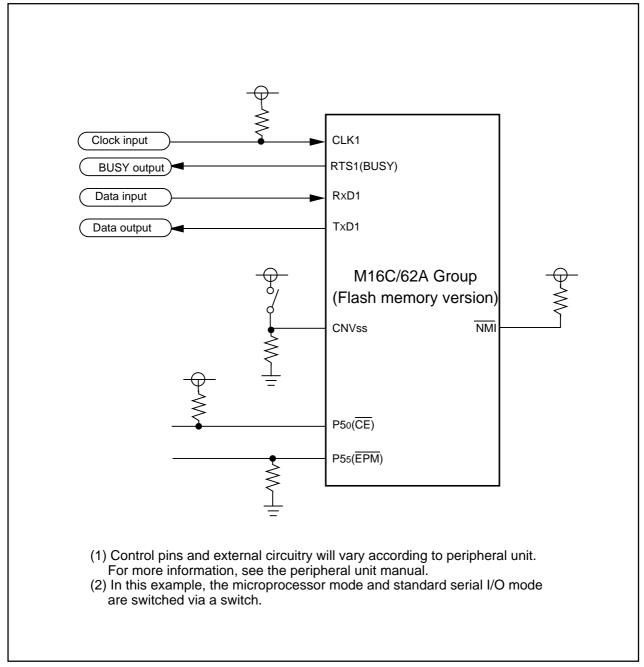


Figure 1.29.21. Example circuit application for the standard serial I/O mode 1



Overview of standard serial I/O mode 2 (clock asynchronized)

In standard serial I/O mode 2, software commands, addresses and data are input and output between the MCU and peripheral units (serial programer, etc.) using 2-wire clock-asynchronized serial I/O (UART1). Standard serial I/O mode 2 is engaged by releasing the reset with the P6s (CLK1) pin "L" level.

The TxD1 pin is for CMOS output. Data transfer is in 8-bit units with LSB first, 1 stop bit and parity OFF. After the reset is released, connections can be established at 9,600 bps when initial communications (Figure 1.29.22) are made with a peripheral unit. However, this requires a main clock with a minimum 2 MHz input oscillation frequency. Baud rate can also be changed from 9,600 bps to 19,200, 38,400 or 57,600 bps by executing software commands. However, communication errors may occur because of the oscillation frequency of the main clock. If errors occur, change the main clock's oscillation frequency and the baud rate.

After executing commands from a peripheral unit that requires time to erase and write data, as with erase and program commands, allow a sufficient time interval or execute the read status command and check how processing ended, before executing the next command.

Data and status registers in memory can be read after transmitting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained initial communications with peripheral units, how frequency is identified and software commands.

Initial communications with peripheral units

After the reset is released, the bit rate generator is adjusted to 9,600 bps to match the oscillation frequency of the main clock, by sending the code as prescribed by the protocol for initial communications with peripheral units (Figure 1.29.22).

- (1) Transmit "B016" from a peripheral unit. If the oscillation frequency input by the main clock is 10 or 16 MHz, the MCU with internal flash memory outputs the "B016" check code. If the oscillation frequency is anything other than 10 or 16 MHz, the MCU does not output anything.
- (2) Transmit "0016" from a peripheral unit 16 times. (The MCU with internal flash memory sets the bit rate generator so that "0016" can be successfully received.)
- (3) The MCU with internal flash memory outputs the "B016" check code and initial communications end successfully *1. Initial communications must be transmitted at a speed of 9,600 bps and a transfer interval of a minimum 15 ms. Also, the baud rate at the end of initial communications is 9,600 bps.
- *1. If the peripheral unit cannot receive "B016" successfully, change the oscillation frequency of the main clock.

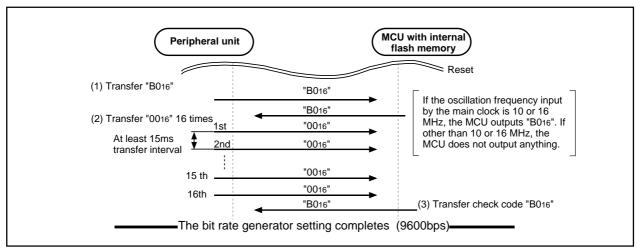


Figure 1.29.22. Peripheral unit and initial communication



How frequency is identified

When "0016" data is received 16 times from a peripheral unit at a baud rate of 9,600 bps, the value of the bit rate generator is set to match the operating frequency (2 - 16 MHz). The highest speed is taken from the first 8 transmissions and the lowest from the last 8. These values are then used to calculate the bit rate generator value for a baud rate of 9,600 bps.

Baud rate cannot be attained with some operating frequencies. Table 1.29.4 gives the operation frequency and the baud rate that can be attained for.

Table 1.29.4 Operation frequency and the baud rate

Operation frequency (MHz)	Baud rate 9,600bps	Baud rate 19,200bps	Baud rate 38,400bps	Baud rate 57,600bps
16MHz	√	√	V	√
12MHz	$\sqrt{}$	V	V	_
11MHz	√	V	V	_
10MHz	√	V	_	√
8MHz	√	V	_	√
7.3728MHz	√	V	V	√
6MHz	√	V	√	_
5MHz	√	V	_	_
4.5MHz	√	V	_	√
4.194304MHz	√	V	√	_
4MHz	√	V	_	_
3.58MHz	√	√ V	√	
3MHz	√	√	√	_
2MHz	V	_	_	_

 $\sqrt{}$: Communications possible

-: Communications not possible



Software Commands

Table 1.29.5 lists software commands. In the standard serial I/O mode 2, erase operations, programs and reading are controlled by transferring software commands via the RxD1 pin. Standard serial I/O mode 2 adds four transmission speed commands - 9,600, 19,200, 38,400 and 57,600 bps - to the software commands of standard serial I/O mode 1. Software commands are explained here below.

Table 1.29.5. Software commands (Standard serial I/O mode 2)

	Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte		When ID is not verified
1	Page read	FF ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41 ₁₆	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Block erase	20 ₁₆	Address (middle)	Address (high)	D016				Not acceptable
4	Erase all unlocked blocks	A7 ₁₆	D0 ₁₆						Not acceptable
5	Read status register	7016	SRD output	SRD1 output					Acceptable
6	Clear status register	5016							Not acceptable
7	Read lock bit status	71 ₁₆	Address (middle)	Address (high)	Lock bit data output				Not acceptable
8	Lock bit program	77 ₁₆	Address (middle)	Address (high)	D0 ₁₆				Not acceptable
9	Lock bit enable	7A ₁₆							Not acceptable
10	Lock bit disable	75 ₁₆							Not acceptable
11	ID check function	F5 ₁₆	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
12	Download function	FA ₁₆	Size (low)	Size (high)	Check- sum	Data input	To required number of times		Not acceptable
13	Version data output function	FB ₁₆	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable
14	Boot ROM area output function	FC ₁₆	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
15	Read check data	FD ₁₆	Check data (low)	Check data (high)					Not acceptable
16	Baud rate 9600	B0 ₁₆	B0 ₁₆						Acceptable
17	Baud rate 19200	B1 ₁₆	B1 ₁₆						Acceptable
18	Baud rate 38400	B2 ₁₆	B2 ₁₆						Acceptable
19	Baud rate 57600	B3 ₁₆	B3 ₁₆						Acceptable

Note 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.

Note 2: SRD refers to status register data. SRD1 refers to status register 1 data.

Note 3: All commands can be accepted when the flash memory is totally blank.



Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

- (1) Transfer the "FF16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first.

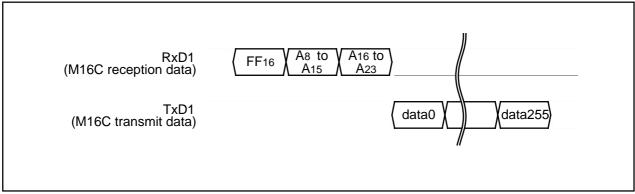


Figure 1.29.23. Timing for page read

Read Status Register Command

This command reads status information. When the "7016" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

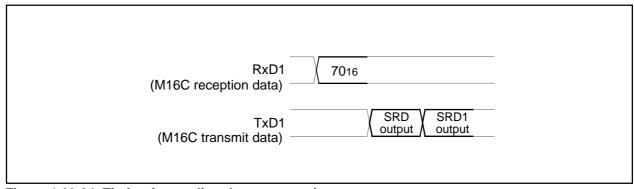


Figure 1.29.24. Timing for reading the status register



Clear Status Register Command

This command clears the bits (SR3–SR5) which are set when the status register operation ends in error. When the "5016" command code is sent with the 1st byte, the aforementioned bits are cleared.



Figure 1.29.25. Timing for clearing the status register

Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

- (1) Transfer the "4116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, as write data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 is input sequentially from the smallest address first, that page is automatically written.

The result of the page program can be known by reading the status register. For more information, see the section on the status register.

Each block can be write-protected with the lock bit. For more information, see the section on the data protection function. Additional writing is not allowed with already programmed pages.

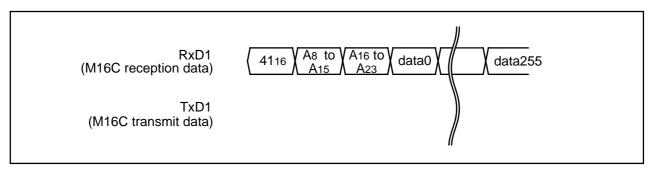


Figure 1.29.26. Timing for the page program



Block Erase Command

This command erases the data in the specified block. Execute the block erase command as explained here following.

- (1) Transfer the "2016" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) Transfer the verify command code "D016" with the 4th byte. With the verify command code, the erase operation will start for the specified block in the flash memory. Write the highest address of the specified block for addresses A8 to A23.

After block erase ends, the result of the block erase operation can be known by reading the status register. For more information, see the section on the status register.

Each block can be erase-protected with the lock bit. For more information, see the section on the data protection function.

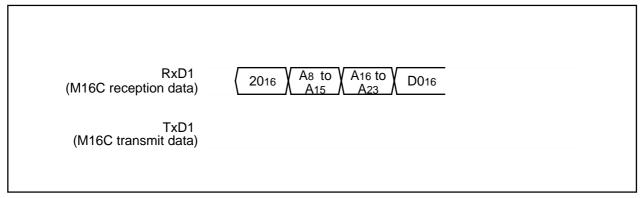


Figure 1.29.7. Timing for block erasing



Erase All Unlocked Blocks Command

This command erases the content of all blocks. Execute the erase all unlocked blocks command as explained here following.

- (1) Transfer the "A716" command code with the 1st byte.
- (2) Transfer the verify command code "D016" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

The result of the erase operation can be known by reading the status register. Each block can be erase-protected with the lock bit. For more information, see the section on the data protection function.



Figure 1.29.28. Timing for erasing all unlocked blocks

Lock Bit Program Command

This command writes "0" (lock) for the lock bit of the specified block. Execute the lock bit program command as explained here following.

- (1) Transfer the "7716" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) Transfer the verify command code "D016" with the 4th byte. With the verify command code, "0" is written for the lock bit of the specified block. Write the highest address of the specified block for addresses A8 to A23.

Lock bit status can be read with the read lock bit status command. For information on the lock bit function, reset procedure and so on, see the section on the data protection function.

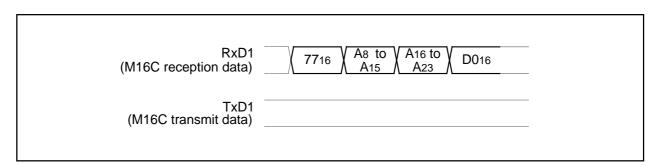


Figure 1.29.29. Timing for the lock bit program



Read Lock Bit Status Command

This command reads the lock bit status of the specified block. Execute the read lock bit status command as explained here following.

- (1) Transfer the "7116" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) The lock bit data of the specified block is output with the 4th byte. The lock bit data is the 6th bit(D6) of the output data. Write the highest address of the specified block for addresses A8 to A23.

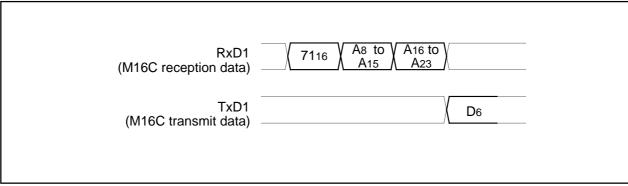


Figure 1.29.30. Timing for reading lock bit status

Lock Bit Enable Command

This command enables the lock bit in blocks whose bit was disabled with the lock bit disable command. The command code "7A16" is sent with the 1st byte of the serial transmission. This command only enables the lock bit function; it does not set the lock bit itself.

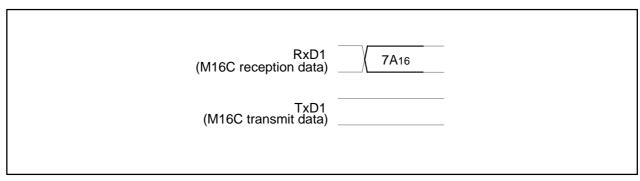


Figure 1.29.31. Timing for enabling the lock bit



Lock Bit Disable Command

This command disables the lock bit. The command code "7516" is sent with the 1st byte of the serial transmission. This command only disables the lock bit function; it does not set the lock bit itself. However, if an erase command is executed after executing the lock bit disable command, "0" (locked) lock bit data is set to "1" (unlocked) after the erase operation ends. In any case, after the reset is cancelled, the lock bit is enabled.

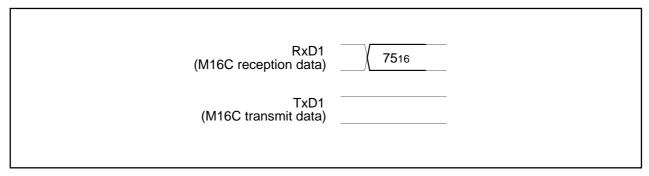


Figure 1.29.32. Timing for disabling the lock bit

Download Command

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

- (1) Transfer the "FA16" command code with the 1st byte.
- (2) Transfer the program size with the 2nd and 3rd bytes.
- (3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
- (4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

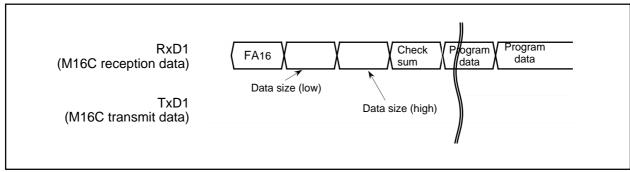


Figure 1.29.33. Timing for download



Version Information Output Command

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

- (1) Transfer the "FB16" command code with the 1st byte.
- (2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

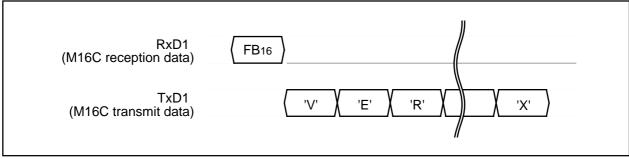


Figure 1.29.34. Timing for version information output

Boot ROM Area Output Command

This command outputs the control program stored in the boot ROM area in one page blocks (256 bytes). Execute the boot ROM area output command as explained here following.

- (1) Transfer the "FC16" command code with the 1st byte.
- (2) Transfer addresses A8 to A15 and A16 to A23 with the 2nd and 3rd bytes respectively.
- (3) From the 4th byte onward, data (D0–D7) for the page (256 bytes) specified with addresses A8 to A23 will be output sequentially from the smallest address first.

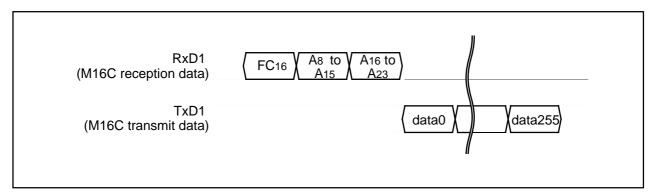


Figure 1.29.35. Timing for boot ROM area output



ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

- (1) Transfer the "F516" command code with the 1st byte.
- (2) Transfer addresses A₀ to A₇, A₈ to A₁₅ and A₁₆ to A₂₃ of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.
- (3) Transfer the number of data sets of the ID code with the 5th byte.
- (4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

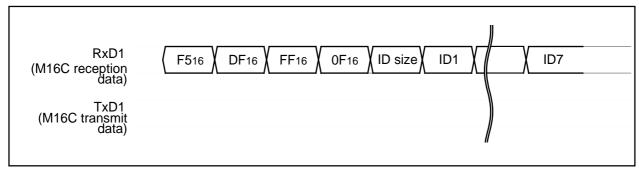


Figure 1.29.36. Timing for the ID check

ID Code

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses 0FFFDF16, 0FFFE316, 0FFFEB16, 0FFFEB16, 0FFFF316, 0FFFF716 and 0FFFFB16. Write a program into the flash memory, which already has the ID code set for these addresses.

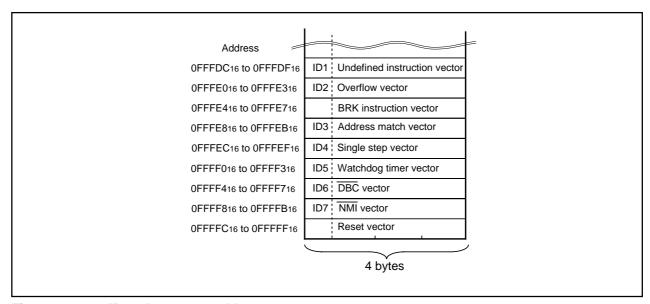


Figure 1.29.37. ID code storage addresses



Read Check Data

This command reads the check data that confirms that the write data, which was sent with the page program command, was successfully received.

- (1) Transfer the "FD16" command code with the 1st byte.
- (2) The check data (low) is received with the 2nd byte and the check data (high) with the 3rd.

To use this read check data command, first execute the command and then initialize the check data. Next, execute the page program command the required number of times. After that, when the read check command is executed again, the check data for all of the read data that was sent with the page program command during this time is read. The check data is the result of CRC operation of write data.

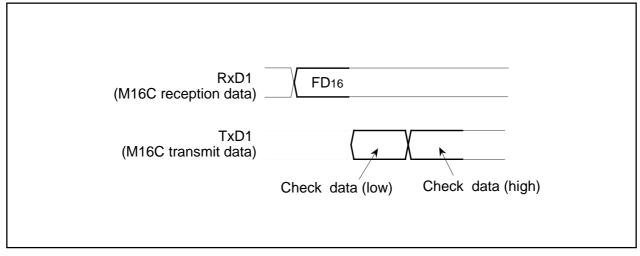


Figure 1.29.38. Timing for the read check data

Baud Rate 9600

This command changes baud rate to 9,600 bps. Execute it as follows.

- (1) Transfer the "B016" command code with the 1st byte.
- (2) After the "B016" check code is output with the 2nd byte, change the baud rate to 9,600 bps.

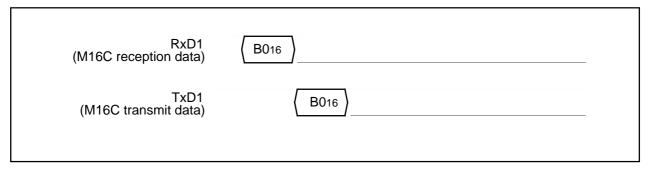


Figure 1.29.39. Timing of baud rate 9600



Baud Rate 19200

This command changes baud rate to 19,200 bps. Execute it as follows.

- (1) Transfer the "B116" command code with the 1st byte.
- (2) After the "B116" check code is output with the 2nd byte, change the baud rate to 19,200 bps.

RxD1 (M16C reception data)	(B116)	
TxD1 (M16C transmit data)	(B116)	

Figure 1.29.40. Timing of baud rate 19200

Baud Rate 38400

This command changes baud rate to 38,400 bps. Execute it as follows.

- (1) Transfer the "B216" command code with the 1st byte.
- (2) After the "B216" check code is output with the 2nd byte, change the baud rate to 38,400 bps.

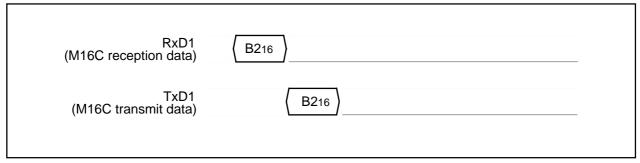


Figure 1.29.41. Timing of baud rate 38400

Baud Rate 57600

This command changes baud rate to 57,600 bps. Execute it as follows.

- (1) Transfer the "B316" command code with the 1st byte.
- (2) After the "B316" check code is output with the 2nd byte, change the baud rate to 57,600 bps.

RxD1 (M16C reception data)	B316
TxD1 (M16C transmit data)	B316

Figure 1.29.42. Timing of baud rate 57600



Example Circuit Application for The Standard Serial I/O Mode 2

The below figure shows a circuit application for the standard serial I/O mode 2.

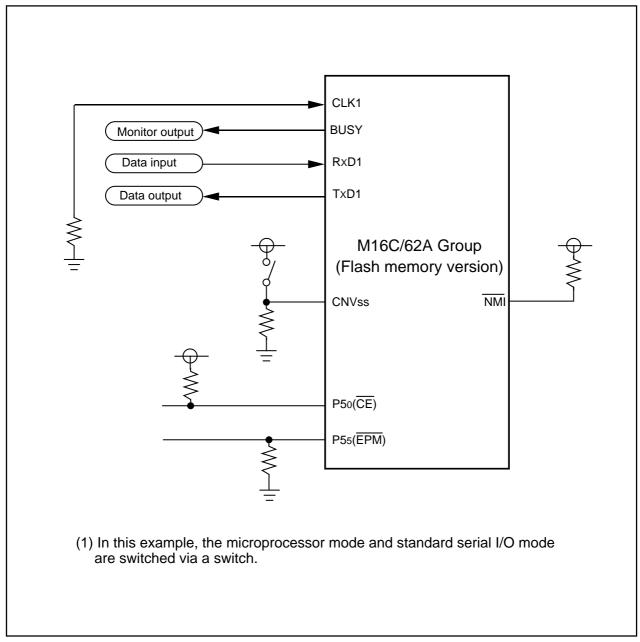


Figure 1.29.43. Example circuit application for the standard serial I/O mode 2



Differences between M16C/62A and M16C/62

Item	M16C/62A	M16C/62
Memory area	1 Mbyte fixed	Memory expansion 1.2 Mbytes mode 4 Mbytes mode
Serial I/O	No CTS/RTS separate function	CTS/RTS separate function
IIC bus mode	Analog or digital delay is selected as SDA delay	Only analog delay is selected as SDA delay
EPROM / one time PROM version	None	Have
Flash memory version	Standard serial I/O mode (clock asynchronized) is supported	Clock synchronized only

Differences in SFR between M16C/62A and M16C/62

Address	Register name	M16C/62A	M16C/62
000516	Processor mode register 1 (PM1)	b5,b4 Reserved bits	b5,b4 Memory area expansion bits
000B16	Data bank register (DBR)	Reserved register	Have
03B016	UART transmit/receive register 2 (UCON)	b6 Reserved bit	b6 CTS/RTS separation bit
037516	UART2 special mode register 3 (U2SMR3)	Have	None
037716	UART2 special mode register (U2SMR)	b7 SDA digital delay select bit	b7 Reserved bit



Revision History

Version		Contents for change		Revision date
REV.A1	036016, 036416), the SI/Oi Control F set bit), make sure to the SI/Oi transm input must be in th	De written to the SI/Oi transmit/receive register the CLKi pin input must be in the low state. Also register (addresses 036216, 036616)'s bit 7 (Souther CLKi pin input is held low> • Before contivered register (addresses 036016, 036416) in high state. Also, before rewriting the SI/Oi (souther continued on the state) in the side of the state. Also, before rewriting the SI/Oi (souther continued on the side of the side of the side of the state. Also, before rewriting the SI/Oi (souther continued on the side of the	so, before rewriting south initial value lata can be written s), the CLKi pin Control Register	99.12.21
REV. A2	"0" . Other b be reset by	lue to an address after "1" is written to this bit bits do not automatically return to "0" and they the program.		00.7.3
	Page 144, Figure 1.16.3 When using the post 3, 4) to "1", be sur	ort as an input/output port by setting the SI/Oi e to set the sync clock select bit to "1". ort as an input/output port by setting the SI/Oi		
		e to set the sync clock select bit to "1". ne UART2 special mode register 2 (bit symbo	1)	00.7.10
REV. B	Page 10 Figure 1.3.1 is page 22 Figure 1.7.1 is page 23 Figure 1.7.2 is page 23 "Internal Reservage 24 Figure 1.7.3 is page 25 Explanation of Page 28 Explanation of Page 29 Figure 1.9.2 is a Page 37 Explanation of Page 38 Figure 1.10.4 is page 39 Explanation of Page 39 Table 1.10.2 is page 40 Explanation of Page 40 Table 1.10.3 is page 42 Explanation of Page 44 Explanation of Page 45 Explanation of Page 46 Explanation of Page 47 Explanation of Page 48 Explanation of Page 48 Explanation of Page 49 Exp	Figure 1.1.2. 'Memory" is partly revised. partly revised. partly revised. partly revised. partly revised. partly revised. (2) Selecting separate/multiplex bus" is partly (2) Chip select signal" is partly added. (2) Sub-clock" is partly revised. partly revised. (5) Sub-clock" is partly revised. partly revised. (5) Sub-Mode" is partly revised. partly revised.	revised.	01.3.27
Re	vision history	M16C/62A Group data sheet		



Version		Contents for change	Revision date
REV. B	Page 63 Explanation of "	Precautions for Interrupts" is partly revised.	01.3.27
	Page 64 Note is added in	n Figure 1.11.13.	
	Page 65 Explanation of "	Watchdog Timer" is partly revised.	
	Page 73 Table 1.13.5 is	partly revised.	
	Page 75 Explanation of "	DMA request bit" is partly revised.	
	Page 80 Figure 1.14.5 is	partly revised.	
	Page 84 Table 1.14.3 is	partly revised.	
	Page 93 Table 1.14.8 is	partly revised.	
	Page 93 Figure 1.14.19 i	s partly revised.	
	Page 95 Figure 1.15.1 is		
	Page 96 Figure 1.15.2 is		
	Page 97 Figure 1.15.3 is		
		of "Three-phase motor driving waveform output mode" is partly	
	Page 98 Figure 1.15.4 is	partly revised.	
	Page 100 Figure 1.15.5 i		
		"Triangular wave modulation" is partly revised.	
	Page 103 Figure 1.15.7 i		
	1 -	"Satooth modulation" is partly revised.	
	Page 106 Figure 1.15.9 i		
	Page 111 Figure 1.16.4 i		
	Page 114 Figure 1.16.7 i		
	Page 115 Figure 1.16.8 i		
	Page 116 Figure 1.16.9 i		
	1 -	"(d) Bus collision detection function (UART2)" is partly revised.	
	· ·	"(a) Function for outputting a parity error signal" is revised.	
	Page 136 Figure 1.16.26		
	Page 141 Table 1.16.12		
	Page 145 Figure 1.16.32	•	
	Page 146 Table 1.16.13	• •	
	1 -		
	Page 148 Note 2 in Table		
	Page 153 Table 1.17.3 is		
		"(a) Sample and hold" is partly revised.	
		"Programmable I/O Ports" is partly revised.	
	Page 167 Note 2 is adde	-	
	Page 168 Note 2 is adde	-	
	Page 169 Figure 1.20.8 i		
		nd Table 1.20.2 are partly revised.	
		cluded (which have described on pages 171-174 of Rev. A2).	
		f "Items to be submitted when ordering masked ROM version" is	
	revised.		
	1 *	ls of Ta are revised to Topr.	
	Page 188 Table 1.23.23		
	Page 216 Table 1.25.1 is Page 219 Explanation of	s partly revised. "Outline Performance (CPU Rewrite Mode)" is partly revised.	
Re	vision history	M16C/62A Group data sheet	<u> </u>



Version	Contents for change	Revision date				
REV. B	Page 220 Figure 1.26.1 is partly revised.	01.3.27				
	Page 221 Figure 1.26.2 is partly revised.					
	Page 222 Explanation of "(1) Operation speed" is partly revised.					
	Page 222 Explanation of "(3) Interrupts inhibited against use" is revised.					
	Page 222 Explanation of "(6) Access disable" is partly revised.					
	Page 222 Explanation of "(7) How to access" is partly revised.					
	Page 223 "(8) Writing in the user ROM area" and "(9) Using the lock bit" are added.					
	Page 226 Figure 1.26.5 is partly revised.					
	Page 230 Explanation of "Program status (SR4)" is partly revised.					
	Page 232 Explanation of "ROM code protect function" is partly revised.					
	Page 234 Explanation of "Parallel I/O Mode" is partly revised.					
	Page 239 Explanation of "Overview of standard serial I/O mode 1 (clock synchronized)" is partly revised.					
	Page 241 Explanation of "Page Read Command" is partly revised.					
	Page 243 Explanation of "Block Erase Command" is partly revised.					
	Page 245 Figure 1.29.10 and explanation of "Read Lock Bit Status Command" are partly revised.					
	Page 247 Explanation of "Boot ROM area Output Command" is partly revised.					
	Page 250 Explanation of "Data Protection (Block Lock)" is partly revised.					
	Page 251 Explanation of "Block Status After Program (SR3)" is partly revised.					
	Page 252 Table 1.29.3 is partly revised.					
	Page 258 Explanation of "Page Read Command" is partly revised.					
	Page 259 Explanation of "Clear Status Register Command" is partly revised.					
	Page 259 Explanation of "Page Program Command" is partly revised.					
	Page 260 Explanation of "Block Erase Command" is partly revised.					
	Page 261 Explanation of "Erase All Unlocked Blocks Command" is partly revised. Page 261 Explanation of "Lock Bit Program Command" is partly revised.					
	Page 262 Figure 1.29.30 and explanation of "Read Lock Bit Status Command" is partly					
	revised.					
	Page 264 Explanation of "Boot ROM Area Output Command" is partly revised. Page 269 Table of "Differences in SFR between M16C/62A and M16C/62" is added.					
	Page 21 Explanation of "Processor Mode" is partly revised.	01.4.6				
	Page 65 Explanation of "Watchdog Timer" is partly revised.					
	Page 158 Explanation of "D-A Converter" is partly revised.	01.4.23				
	Page 83 Figure 1.14.8 is partly revised. Page 176 Table 1.23.6 is partly revised.					
REV. B1	Page 65 Explanation of "Watchdog Timer" is partly added.	01.5.10				



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