

# MC74HC4066A

## Quad Analog Switch/ Multiplexer/Demultiplexer

### High-Performance Silicon-Gate CMOS

The MC74HC4066A utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from  $V_{CC}$  to GND).

The HC4066A is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so the ON resistances ( $R_{ON}$ ) are more linear over input voltage than  $R_{ON}$  of metal-gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316A.

#### Features

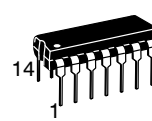
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 V
- Analog Input Voltage Range ( $V_{CC} - GND$ ) = 2.0 to 12.0 V
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



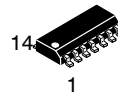
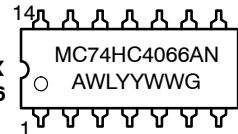
ON Semiconductor®

<http://onsemi.com>

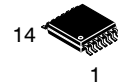
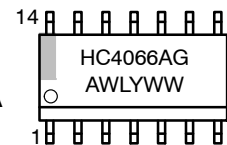
#### MARKING DIAGRAMS



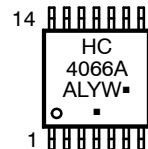
PDIP-14  
N SUFFIX  
CASE 646



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

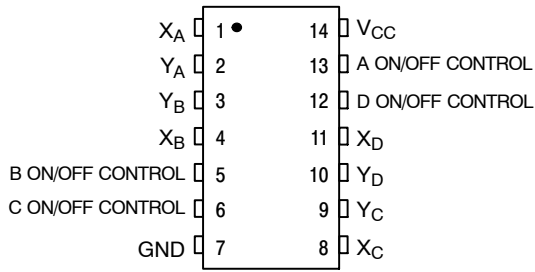
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HC4066A

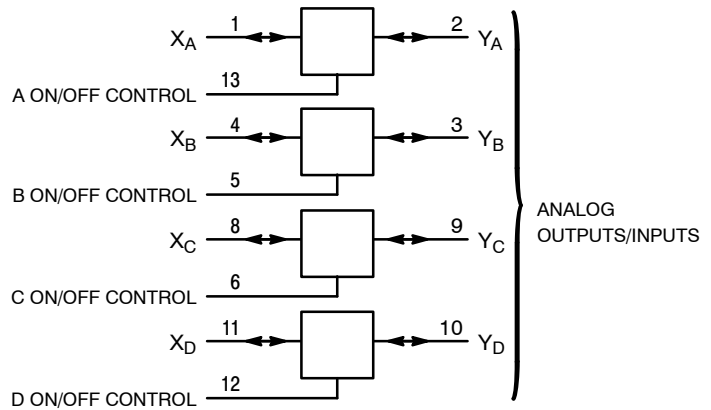
## PIN ASSIGNMENT



## FUNCTION TABLE

| On/Off Control Input | State of Analog Switch |
|----------------------|------------------------|
| L                    | Off                    |
| H                    | On                     |

## LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X<sub>A</sub>, X<sub>B</sub>, X<sub>C</sub>, X<sub>D</sub>  
 PIN 14 = V<sub>CC</sub>  
 PIN 7 = GND

## ORDERING INFORMATION

| Device           | Package               | Shipping <sup>†</sup> |
|------------------|-----------------------|-----------------------|
| MC74HC4066ANG    | PDIP-14<br>(Pb-Free)  | 25 Units / Rail       |
| MC74HC4066ADG    | SOIC-14<br>(Pb-Free)  | 55 Units / Rail       |
| MC74HC4066ADR2G  | SOIC-14<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC74HC4066ADTR2G | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel    |
| NLVHC4066ADTR2G  | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC74HC4066A

## MAXIMUM RATINGS

| Symbol           | Parameter   | Value                          | Unit |
|------------------|---|--------------------------------|------|
| V <sub>CC</sub>  | Positive DC Supply Voltage (Referenced to GND)  | - 0.5 to + 14.0                | V    |
| V <sub>IS</sub>  | Analog Input Voltage (Referenced to GND)  | - 0.5 to V <sub>CC</sub> + 0.5 | V    |
| V <sub>in</sub>  | Digital Input Voltage (Referenced to GND)   | - 0.5 to V <sub>CC</sub> + 0.5 | V    |
| I                | DC Current Into or Out of Any Pin   | ± 25                           | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air,<br>Plastic DIP†<br>EIAJ/SOIC Package†<br>TSSOP Package† | 750                            | mW   |
|                  |   | 500                            |      |
|                  |   | 450                            |      |
| T <sub>stg</sub> | Storage Temperature   | - 65 to + 150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package) | 260                            | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

† Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
EIAJ/SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol                          | Parameter   | Min                      | Max             | Unit |    |
|---------------------------------|---|--------------------------|-----------------|------|----|
| V <sub>CC</sub>                 | Positive DC Supply Voltage (Referenced to GND)              | 2.0                      | 12.0            | V    |    |
| V <sub>IS</sub>                 | Analog Input Voltage (Referenced to GND)                    | GND                      | V <sub>CC</sub> | V    |    |
| V <sub>in</sub>                 | Digital Input Voltage (Referenced to GND)                   | GND                      | V <sub>CC</sub> | V    |    |
| V <sub>IO*</sub>                | Static or Dynamic Voltage Across Switch                     | -                        | 1.2             | V    |    |
| T <sub>A</sub>                  | Operating Temperature, All Package Types                    | -55                      | + 125           | °C   |    |
| t <sub>r</sub> , t <sub>f</sub> | Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10) | V <sub>CC</sub> = 2.0 V  | 0               | 1000 | ns |
|                                 |   | V <sub>CC</sub> = 3.0 V  | 0               | 600  |    |
|                                 |   | V <sub>CC</sub> = 4.5 V  | 0               | 500  |    |
|                                 |   | V <sub>CC</sub> = 9.0 V  | 0               | 400  |    |
|                                 |   | V <sub>CC</sub> = 12.0 V | 0               | 250  |    |

\*For voltage drops across the switch greater than 1.2 V (switch on), excessive V<sub>CC</sub> current may be drawn; i.e., the current out of the switch may contain both V<sub>CC</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

## DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

| Symbol          | Parameter  | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
|                 |  |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Voltage<br>ON/OFF Control Inputs    | R <sub>on</sub> = Per Spec  | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |  |   | 3.0                  | 2.1              | 2.1    | 2.1     |      |
|                 |  |   | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |  |   | 9.0                  | 6.3              | 6.3    | 6.3     |      |
|                 |  |   | 12.0                 | 8.4              | 8.4    | 8.4     |      |
| V <sub>IL</sub> | Maximum Low-Level Voltage<br>ON/OFF Control Inputs     | R <sub>on</sub> = Per Spec  | 2.0                  | 0.5              | 0.5    | 0.5     | V    |
|                 |  |   | 3.0                  | 0.9              | 0.9    | 0.9     |      |
|                 |  |   | 4.5                  | 1.35             | 1.35   | 1.35    |      |
|                 |  |   | 9.0                  | 2.7              | 2.7    | 2.7     |      |
|                 |  |   | 12.0                 | 3.6              | 3.6    | 3.6     |      |
| I <sub>in</sub> | Maximum Input Leakage Current<br>ON/OFF Control Inputs | V <sub>in</sub> = V <sub>CC</sub> or GND                          | 12.0                 | ± 0.1            | ± 1.0  | ± 1.0   | µA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current<br>(per Package)      | V <sub>in</sub> = V <sub>CC</sub> or GND<br>V <sub>IO</sub> = 0 V | 6.0                  | 2                | 20     | 40      | µA   |
|                 |  |   | 12.0                 | 4                | 40     | 160     |      |

# MC74HC4066A

## DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

| Symbol           | Parameter  | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|------------------|--|--|----------------------|------------------|--------|---------|------|
|                  |  |  |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| R <sub>on</sub>  | Maximum "ON" Resistance  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> to GND<br>I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2)                | 2.0†                 | -                | -      | -       | Ω    |
|                  |  |  | 3.0†                 | -                | -      | -       |      |
|                  |  |  | 4.5                  | 120              | 160    | 200     |      |
|                  |  |  | 9.0                  | 70               | 85     | 100     |      |
|                  |  |  | 12.0                 | 70               | 85     | 100     |      |
|                  |  | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND<br>(Endpoints)<br>I <sub>S</sub> ≤ 2.0 mA (Figures 1, 2) | 2.0                  | -                | -      | -       |      |
|                  |  |  | 3.0                  | -                | -      | -       |      |
|                  |  |  | 4.5                  | 70               | 85     | 120     |      |
|                  |  |  | 9.0                  | 50               | 60     | 80      |      |
|                  |  |  | 12.0                 | 50               | 60     | 80      |      |
| ΔR <sub>on</sub> | Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = 1/2 (V <sub>CC</sub> - GND)<br>I <sub>S</sub> ≤ 2.0 mA                          | 2.0                  | -                | -      | -       | Ω    |
|                  |  |  | 4.5                  | 20               | 25     | 30      |      |
|                  |  |  | 9.0                  | 15               | 20     | 25      |      |
|                  |  |  | 12.0                 | 15               | 20     | 25      |      |
| I <sub>off</sub> | Maximum Off-Channel Leakage Current, Any One Channel                               | V <sub>in</sub> = V <sub>IL</sub><br>V <sub>IO</sub> = V <sub>CC</sub> or GND<br>Switch Off (Figure 3)                                 | 12.0                 | 0.1              | 0.5    | 1.0     | μA   |
| I <sub>on</sub>  | Maximum On-Channel Leakage Current, Any One Channel                                | V <sub>in</sub> = V <sub>IH</sub><br>V <sub>IS</sub> = V <sub>CC</sub> or GND<br>(Figure 4)  | 12.0                 | 0.1              | 0.5    | 1.0     | μA   |

†At supply voltage (V<sub>CC</sub>) approaching 3 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, ON/OFF Control Inputs: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |         | Unit |    |
|--|---|---|------------------|--------|---------|------|----|
|  |   |   | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |    |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Analog Input to Analog Output<br>(Figures 8 and 9)     | 2.0                                     | 40               | 50     | 60      | ns   |    |
|  |   | 3.0                                     | 30               | 40     | 50      |      |    |
|  |   | 4.5                                     | 10               | 13     | 15      |      |    |
|  |   | 9.0                                     | 10               | 13     | 15      |      |    |
|  |   | 12.0                                    | 10               | 13     | 15      |      |    |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 10 and 11) | 2.0                                     | 80               | 90     | 110     | ns   |    |
|  |   | 3.0                                     | 60               | 70     | 80      |      |    |
|  |   | 4.5                                     | 30               | 38     | 45      |      |    |
|  |   | 9.0                                     | 25               | 28     | 30      |      |    |
|  |   | 12.0                                    | 25               | 28     | 30      |      |    |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, ON/OFF Control to Analog Output<br>(Figures 10 and 11) | 2.0                                     | 80               | 90     | 100     | ns   |    |
|  |   | 3.0                                     | 45               | 50     | 60      |      |    |
|  |   | 4.5                                     | 25               | 32     | 37      |      |    |
|  |   | 9.0                                     | 25               | 32     | 37      |      |    |
|  |   | 12.0                                    | 25               | 32     | 37      |      |    |
| C                                      | Maximum Capacitance   | ON/OFF Control Input                    | -                | 10     | 10      | 10   | pF |
|  |   | Control Input = GND                     | -                | 35     | 35      | 35   |    |
|  |   | Analog I/O<br>Feedthrough               | -                | 1.0    | 1.0     | 1.0  |    |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Switch) (Figure 13)*                           | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        |         | pF   |    |
|  |   |   |                  | 15     |         |      |    |

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC4066A

## ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter   | Test Conditions  | V <sub>CC</sub><br>V                     | Limit*<br>25°C<br>54/74HC                    | Unit             |
|--------|---|--|--|--|------------------|
| BW     | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5) | f <sub>in</sub> = 1 MHz Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>OS</sub><br>Increase f <sub>in</sub> Frequency Until dB Meter Reads - 3 dB<br>R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF  | 4.5<br>9.0<br>12.0                       | 150<br>160<br>160                            | MHz              |
| -      | Off-Channel Feedthrough Isolation (Figure 6)                          | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br>f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF                                   | 4.5<br>9.0<br>12.0<br>4.5<br>9.0<br>12.0 | - 50<br>- 50<br>- 50<br>- 40<br>- 40<br>- 40 | dB               |
| -      | Feedthrough Noise, Control to Switch (Figure 7)                       | V <sub>in</sub> ≤ 1 MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6 ns)<br>Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0 A<br>R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br>R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF  | 4.5<br>9.0<br>12.0<br>4.5<br>9.0<br>12.0 | 60<br>130<br>200<br>30<br>65<br>100          | mV <sub>PP</sub> |
| -      | Crosstalk Between Any Two Switches (Figure 12)                        | f <sub>in</sub> ≡ Sine Wave<br>Adjust f <sub>in</sub> Voltage to Obtain 0 dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10 kHz, R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 50 pF<br>f <sub>in</sub> = 1.0 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 10 pF                                   | 4.5<br>9.0<br>12.0<br>4.5<br>9.0<br>12.0 | - 70<br>- 70<br>- 70<br>- 80<br>- 80<br>- 80 | dB               |
| THD    | Total Harmonic Distortion (Figure 14)                                 | f <sub>in</sub> = 1 kHz, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF<br>THD = THD <sub>Measured</sub> - THD <sub>Source</sub><br>V <sub>IS</sub> = 4.0 V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 8.0 V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 11.0 V <sub>PP</sub> sine wave | 4.5<br>9.0<br>12.0                       | 0.10<br>0.06<br>0.04                         | %                |

\*Guaranteed limits not tested. Determined by design and verified by qualification.

# MC74HC4066A

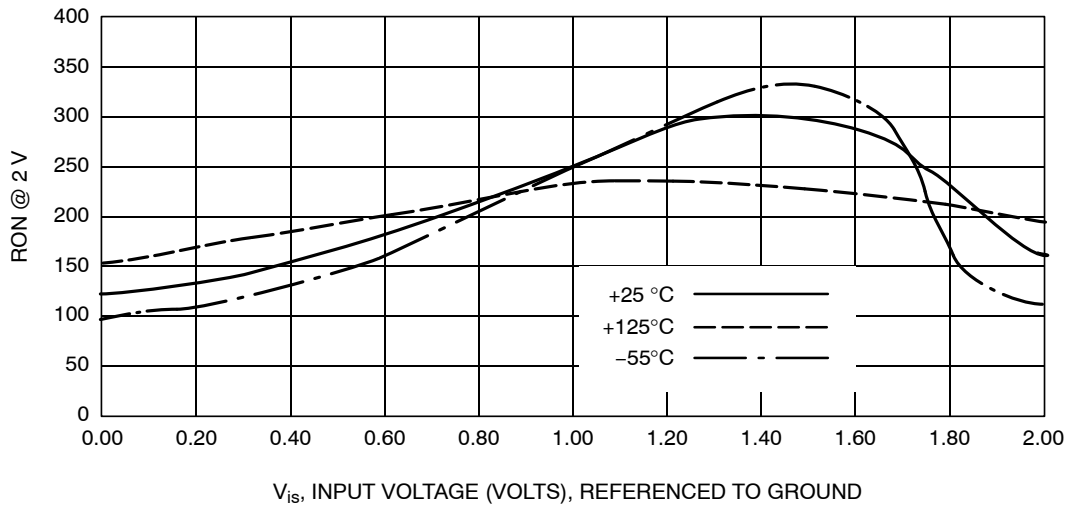


Figure 1a. Typical On Resistance, V<sub>CC</sub> = 2.0 V

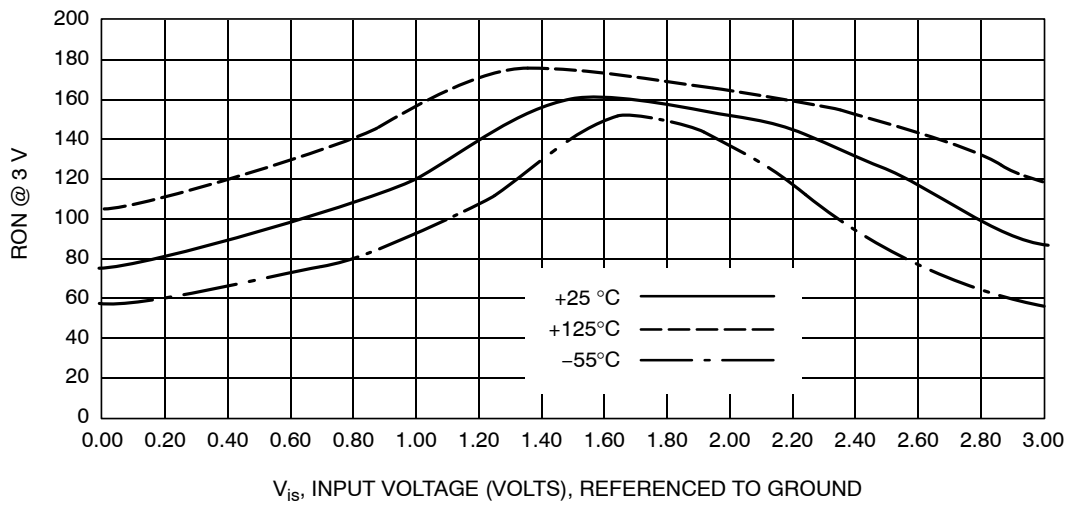


Figure 1b. Typical On Resistance, V<sub>CC</sub> = 3.0 V

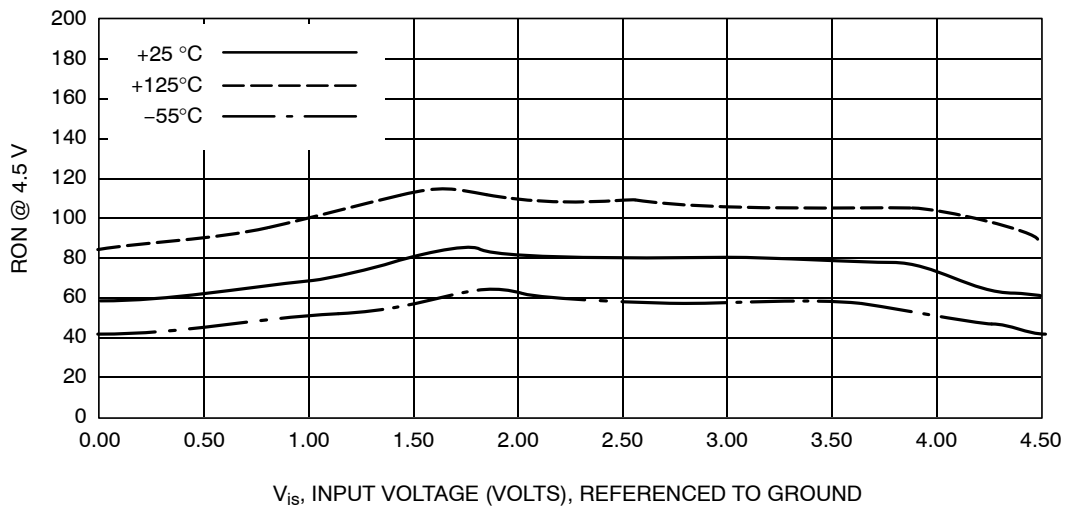
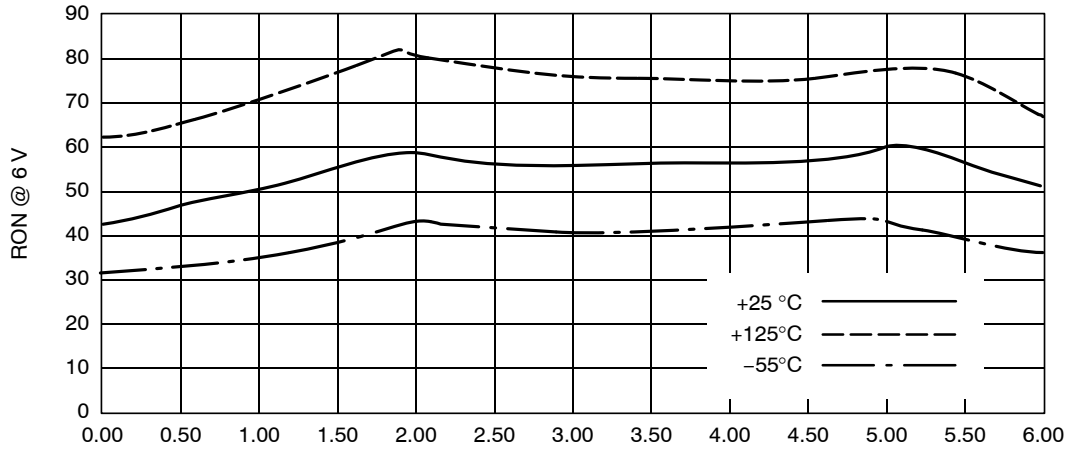


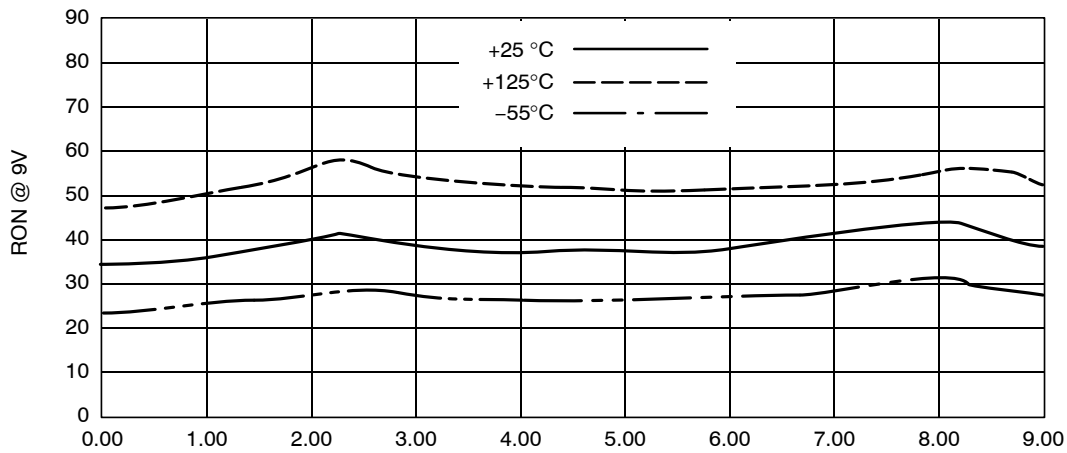
Figure 1c. Typical On Resistance, V<sub>CC</sub> = 4.5 V

# MC74HC4066A



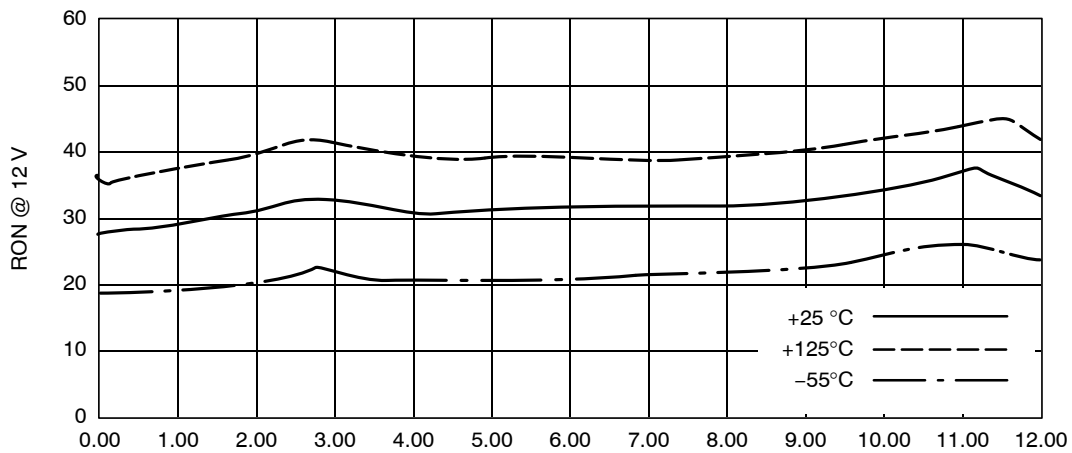
V<sub>IS</sub>, INPUT VOLTAGE (VOLTS), REFERENCED TO GROUND

**Figure 1d. Typical On Resistance, V<sub>CC</sub> = 6.0 V**



V<sub>IS</sub>, INPUT VOLTAGE (VOLTS), REFERENCED TO GROUND

**Figure 1e. Typical On Resistance, V<sub>CC</sub> = 9.0 V**



V<sub>IS</sub>, INPUT VOLTAGE (VOLTS), REFERENCED TO GROUND

**Figure 1f. Typical On Resistance, V<sub>CC</sub> = 12.0 V**

# MC74HC4066A

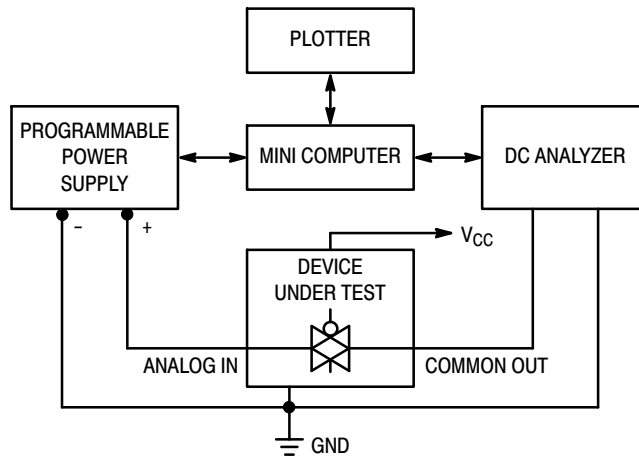


Figure 2. On Resistance Test Set-Up

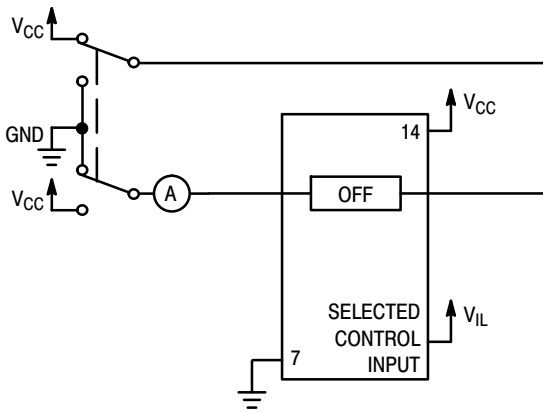


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

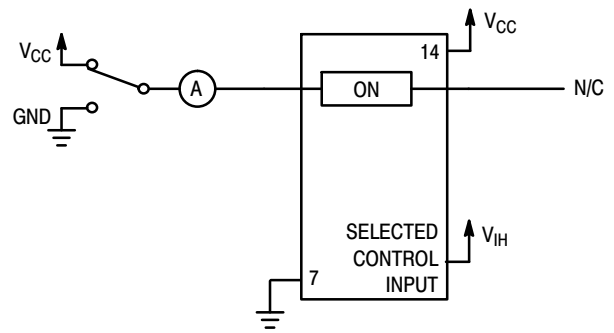
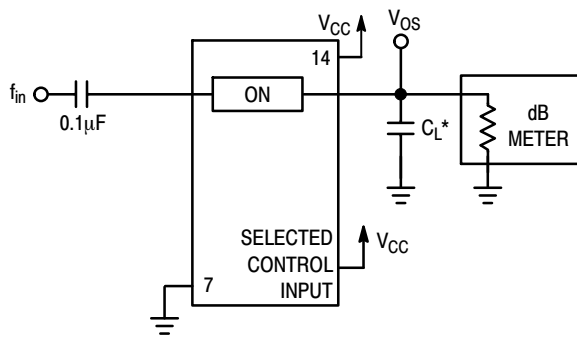


Figure 4. Maximum On Channel Leakage Current, Test Set-Up

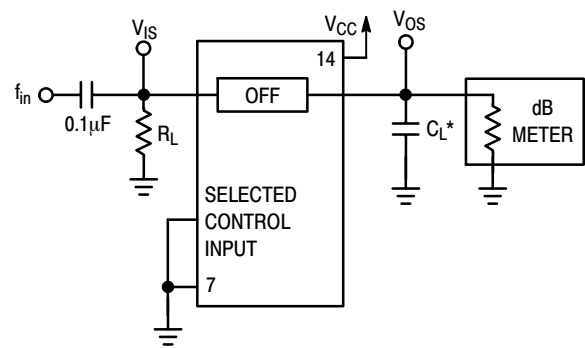


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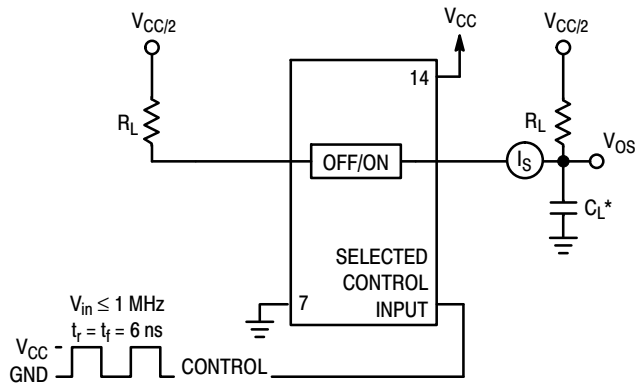
\*Includes all probe and jig capacitance.

**Figure 5. Maximum On-Channel Bandwidth Test Set-Up**



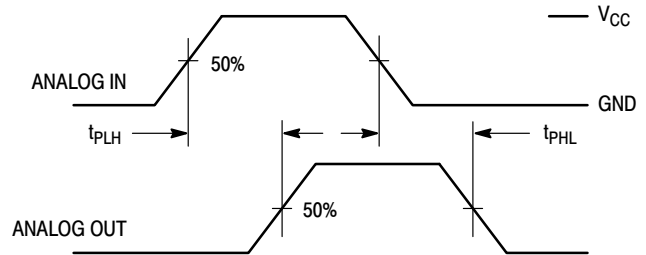
\*Includes all probe and jig capacitance.

**Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up**



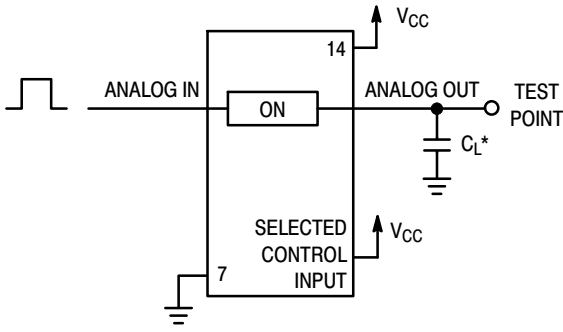
\*Includes all probe and jig capacitance.

**Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up**



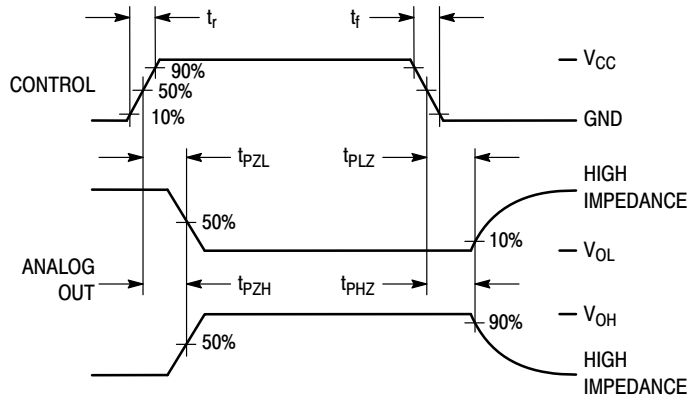
**Figure 8. Propagation Delays, Analog In to Analog Out**

# MC74HC4066A

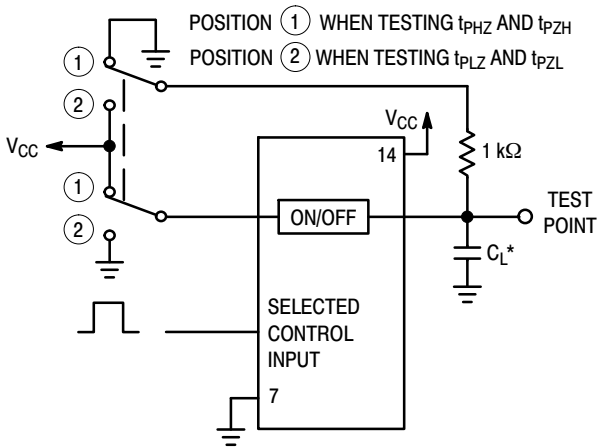


\*Includes all probe and jig capacitance.

**Figure 9. Propagation Delay Test Set-Up**

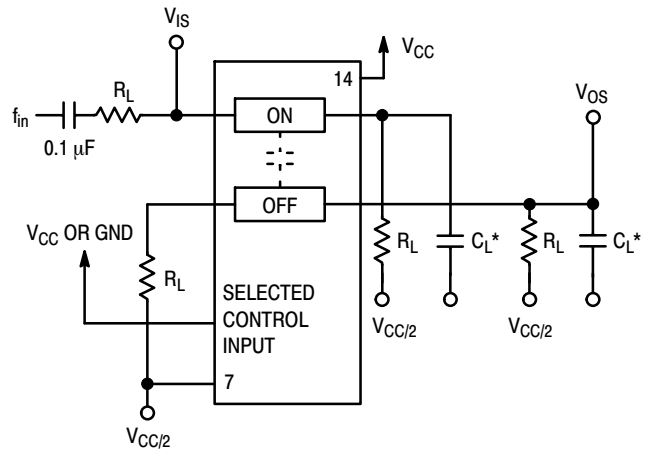


**Figure 10. Propagation Delay, ON/OFF Control to Analog Out**



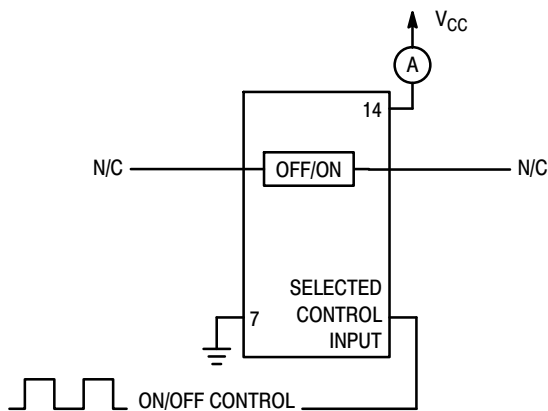
\*Includes all probe and jig capacitance.

**Figure 11. Propagation Delay Test Set-Up**

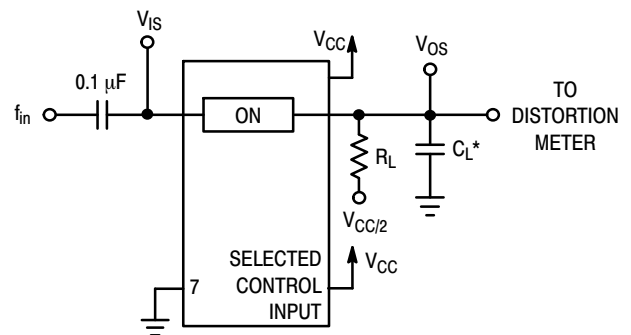


\*Includes all probe and jig capacitance.

**Figure 12. Crosstalk Between Any Two Switches, Test Set-Up**



**Figure 13. Power Dissipation Capacitance Test Set-Up**



\*Includes all probe and jig capacitance.

**Figure 14. Total Harmonic Distortion, Test Set-Up**

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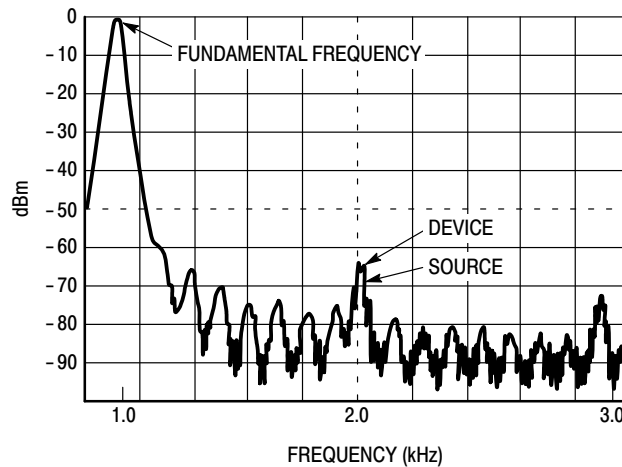


Figure 15. Plot, Harmonic Distortion

## APPLICATION INFORMATION

The ON/OFF Control pins should be at  $V_{CC}$  or GND logic levels,  $V_{CC}$  being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to  $V_{CC}$  or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and GND. The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below GND. In the example

below, the difference between  $V_{CC}$  and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above  $V_{CC}$  and/or below GND are anticipated on the analog channels, external diodes ( $D_x$ ) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the  $D_x$  diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

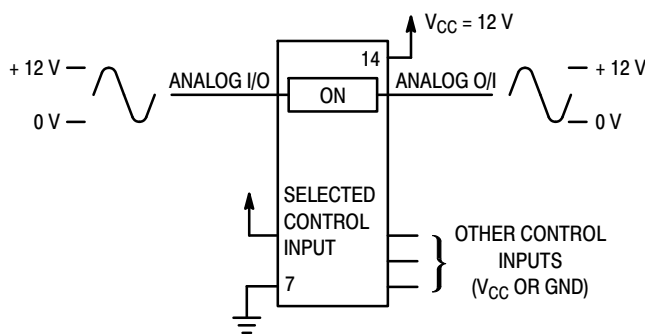


Figure 16. 12 V Application

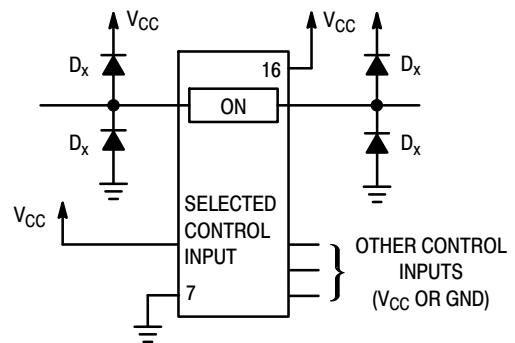


Figure 17. Transient Suppressor Application

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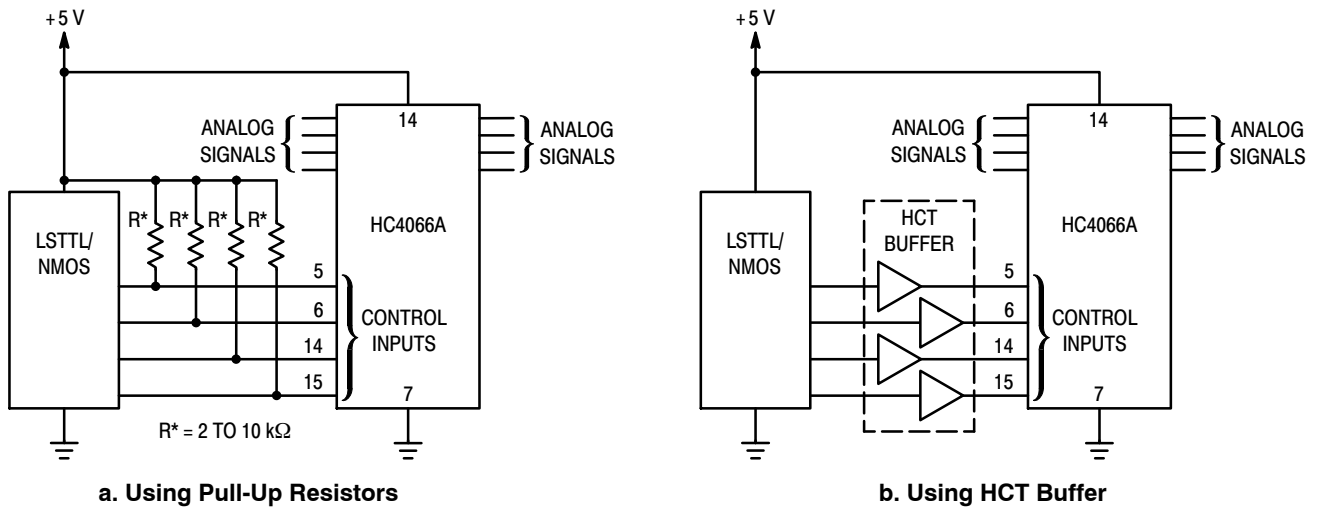


Figure 18. LSTTL/NMOS to HCMOS Interface

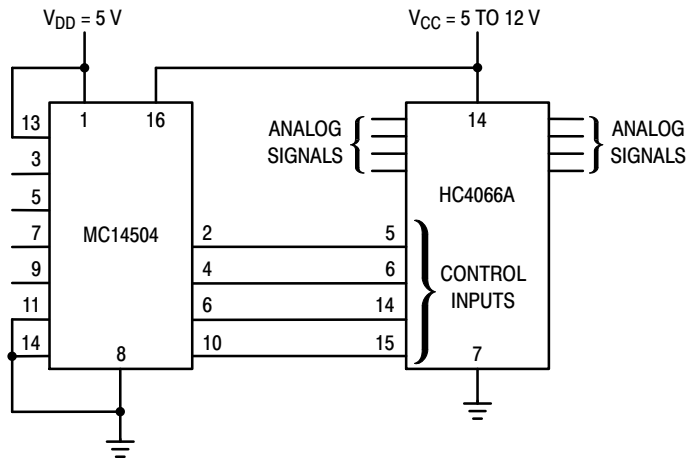


Figure 19. TTL/NMOS-to-CMOS Level Converter  
Analog Signal Peak-to-Peak Greater than 5 V  
(Also see HC4316A)

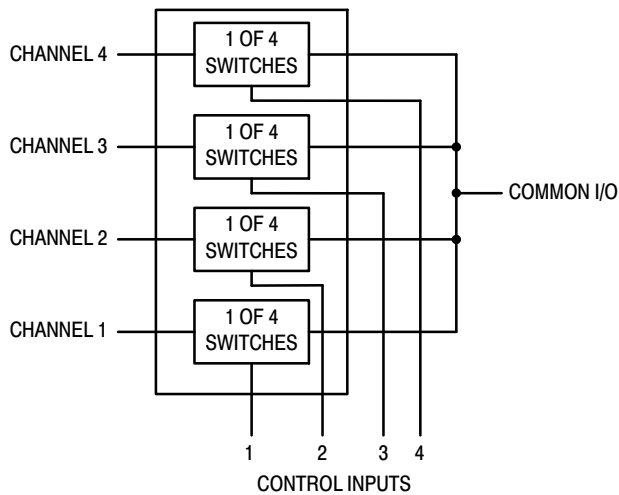


Figure 20. 4-Input Multiplexer

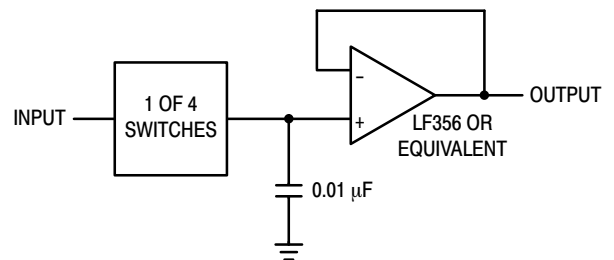
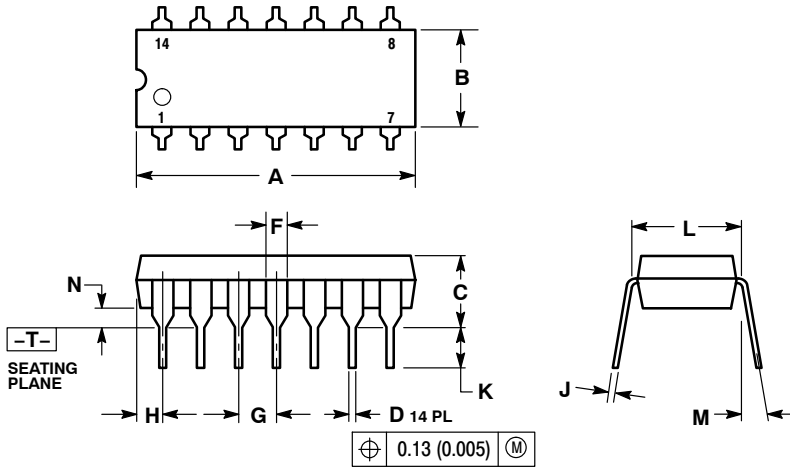


Figure 21. Sample/Hold Amplifier

# MC74HC4066A

## PACKAGE DIMENSIONS

PDIP-14  
N SUFFIX  
CASE 646-06  
ISSUE P



### NOTES:

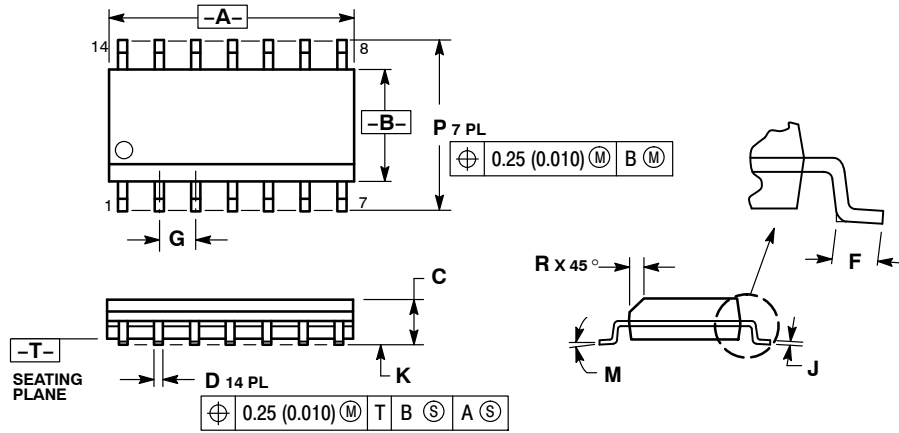
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.715     | 0.770 | 18.16       | 19.56 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.145     | 0.185 | 3.69        | 4.69  |
| D   | 0.015     | 0.021 | 0.38        | 0.53  |
| F   | 0.040     | 0.070 | 1.02        | 1.78  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.052     | 0.095 | 1.32        | 2.41  |
| J   | 0.008     | 0.015 | 0.20        | 0.38  |
| K   | 0.115     | 0.135 | 2.92        | 3.43  |
| L   | 0.290     | 0.310 | 7.37        | 7.87  |
| M   | ---       | 10°   | ---         | 10°   |
| N   | 0.015     | 0.039 | 0.38        | 1.01  |

# MC74HC4066A

## PACKAGE DIMENSIONS

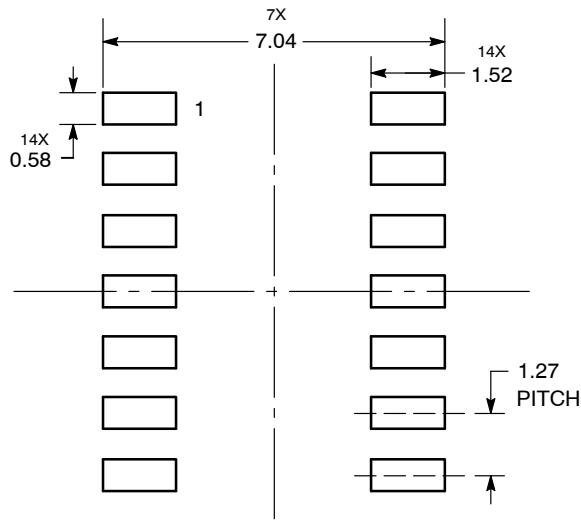
SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE J



- NOTES:
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  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

### SOLDERING FOOTPRINT

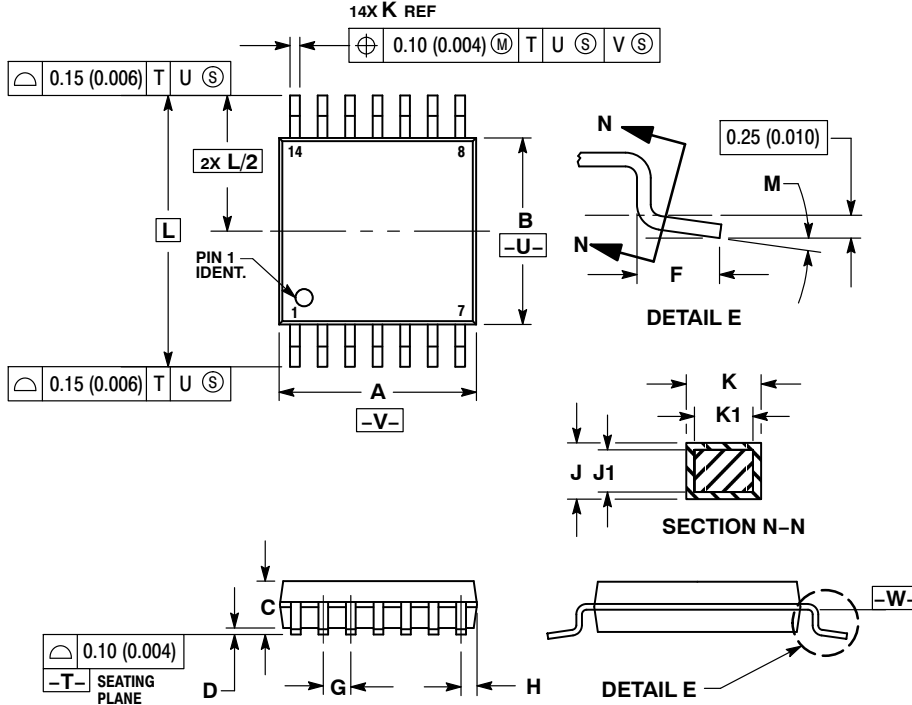


DIMENSIONS: MILLIMETERS

# MC74HC4066A

## PACKAGE DIMENSIONS

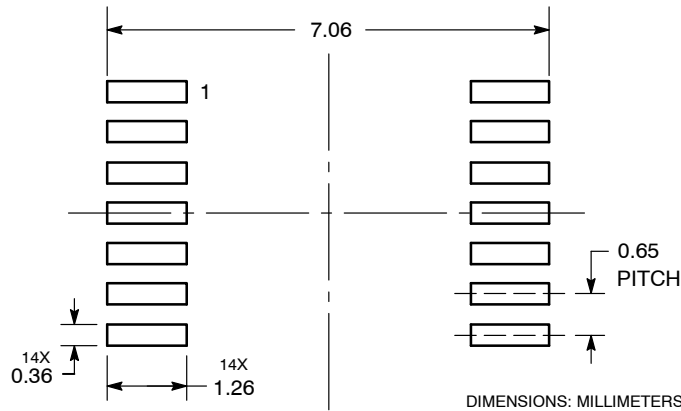
TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE B



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