XC866 8-Bit Single-Chip Microcontroller

Microcontrollers



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XC866

8-Bit Single-Chip Microcontroller

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XC866 Data Sheet

Revision History: 2007-10 V1.2

Previous Version: V 0.1, 2005-01

V1.0, 2006-02 V1.1, 2006-12

Page	Subjects (major changes since last revision)
3	Device summary table is updated for Flash 4-Kb and ROM variants.
13	Footnote is added to MBC pin; description of $V_{\rm DDP}$ pin is updated.
25	Section on bit protection scheme and access type of register bit field PASSWD.PASS are updated.
26	Access type of PAGE bits of all module page registers are corrected to rwh.
29	Access type of Px_DIR register bits are corrected to rwh
38	New bullet point on Flash delivery state is added to the feature list.
88	Digital power supply voltage are differentiated for 5V and 3.3V variants.
89	New parameters on XTAL1 hysteresis and Voltage on GPIO pins during $V_{\rm DDP}$ power-off condition are added.
104	Figure on Power-on reset timing is updated.

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8-Bit Single-Chip Microcontroller XC800 Family

XC866

1 Summary of Features

- · High-performance XC800 Core
 - compatible with standard 8051 processor
 - two clocks per machine cycle architecture (for memory access without wait state)
 - two data pointers
- · On-chip memory
 - 8 Kbytes of Boot ROM
 - 256 bytes of RAM
 - 512 bytes of XRAM
 - 4/8/16 Kbytes of Flash; or
 8/16 Kbytes of ROM, with additional 4 Kbytes of Flash (includes memory protection strategy)
- I/O port supply at 3.3 V/5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(further features are on next page)

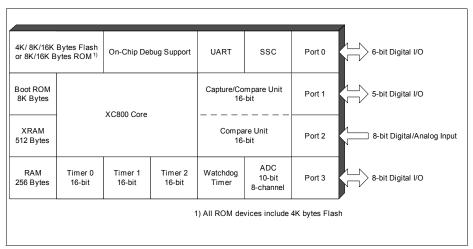


Figure 1 XC866 Functional Units



Features (continued):

- · Reset generation
 - Power-On reset
 - Hardware reset
 - Brownout reset for core logic supply
 - Watchdog timer reset
 - Power-Down Wake-up reset
- On-chip OSC and PLL for clock generation
 - PLL loss-of-lock detection
- · Power saving modes
 - slow-down mode
 - idle mode
 - power-down mode with wake-up capability via RXD or EXINT0
 - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Four ports
 - 19 pins as digital I/O
 - 8 pins as digital/analog input
- · 8-channel, 10-bit ADC
- Three 16-bit timers
 - Timer 0 and Timer 1 (T0 and T1)
 - Timer 2
- Capture/compare unit for PWM signal generation (CCU6)
- Full-duplex serial interface (UART)
- Synchronous serial channel (SSC)
- On-chip debug support
 - 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
 - 64 bytes of monitor RAM
- · PG-TSSOP-38 pin package
- Temperature range T_△:
 - SAF (-40 to 85 °C)
 - SAK (-40 to 125 °C)



XC866 Variant Devices

The XC866 product family features devices with different configurations and program memory sizes, temperature and quality profiles (Automotive or Industrial), offering cost-effective solution for different application requirements.

The configuration of LIN BSL for XC866 devices are summarized in Table 1.

Table 1 Device Configuration for LIN BSL

Device Name	LIN BSL Support
XC866	No
XC866L	Yes

The list of XC866 devices and their differences are summarized in Table 2.

Table 2 Device Summary

Table 2	Device Summary					
Device Type	Device Name	Power Supply (V)		D-Flash Size (Kbytes)	ROM Size (Kbytes)	Quality Profile ¹⁾
Flash ²⁾	SAK-XC866*-4FRA	5.0	12	4	_	Automotive
	SAK-XC866*-4FRI	5.0	12	4	_	Industrial
	SAK-XC866*-2FRA	5.0	4	4	_	Automotive
	SAK-XC866*-2FRI	5.0	4	4	_	Industrial
	SAK-XC866*-1FRA	5.0	_	4	_	Automotive
	SAK-XC866*-1FRI	5.0	_	4	_	Industrial
	SAF-XC866*-4FRA	5.0	12	4	_	Automotive
	SAF-XC866*-4FRI	5.0	12	4	_	Industrial
	SAF-XC866*-2FRA	5.0	4	4	_	Automotive
	SAF-XC866*-2FRI	5.0	4	4	_	Industrial
	SAF-XC866*-1FRA	5.0	_	4	_	Automotive
	SAF-XC866*-1FRI	5.0	_	4	_	Industrial
	SAK-XC866*-4FRA 3V	3.3	12	4	_	Automotive
	SAK-XC866*-4FRI 3V	3.3	12	4	_	Industrial
	SAK-XC866*-2FRA 3V	3.3	4	4	_	Automotive
	SAK-XC866*-2FRI 3V	3.3	4	4	_	Industrial
	SAK-XC866*-1FRA 3V	3.3	_	4	_	Automotive



Table 2	Device Summary					
	SAK-XC866*-1FRI 3V	3.3	_	4	_	Industrial
	SAF-XC866*-4FRA 3V	3.3	12	4	_	Automotive
	SAF-XC866*-4FRI 3V	3.3	12	4	_	Industrial
	SAF-XC866*-2FRA 3V	3.3	4	4	_	Automotive
	SAF-XC866*-2FRI 3V	3.3	4	4	_	Industrial
	SAF-XC866*-1FRA 3V	3.3	_	4	_	Automotive
	SAF-XC866*-1FRI 3V	3.3	_	4	_	Industrial
ROM	SAK-XC866*-4RRA	5.0	_	4	16	Automotive
	SAK-XC866*-4RRI	5.0	_	4	16	Industrial
	SAK-XC866*-2RRA	5.0	_	4	8	Automotive
	SAK-XC866*-2RRI	5.0	_	4	8	Industrial
	SAF-XC866*-4RRA	5.0	_	4	16	Automotive
	SAF-XC866*-4RRI	5.0	_	4	16	Industrial
	SAF-XC866*-2RRA	5.0	_	4	8	Automotive
	SAF-XC866*-2RRI	5.0	_	4	8	Industrial
	SAK-XC866*-4RRA 3V	3.3	_	4	16	Automotive
	SAK-XC866*-4RRI 3V	3.3	_	4	16	Industrial
	SAK-XC866*-2RRA 3V	3.3	_	4	8	Automotive
	SAK-XC866*-2RRI 3V	3.3	_	4	8	Industrial
	SAF-XC866*-4RRA 3V	3.3	_	4	16	Automotive
	SAF-XC866*-4RRI 3V	3.3	_	4	16	Industrial
	SAF-XC866*-2RRA 3V	3.3	_	4	8	Automotive
	SAF-XC866*-2RRI 3V	3.3	_	4	8	Industrial

¹⁾ Industrial is not for Automotive usage

Note: The asterisk (*) above denotes the device configuration letters from Table 1.

²⁾ The flash memory (P-Flash and D-Flash) can be used for code or data.



Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- · the package and the type of delivery

For the available ordering codes for the XC866, please refer to your responsible sales representative or your local distributor.

As this document refers to all the derivatives, some descriptions may not apply to a specific product. For simplicity all versions are referred to by the term XC866 throughout this document.



2 General Device Information

2.1 Block Diagram

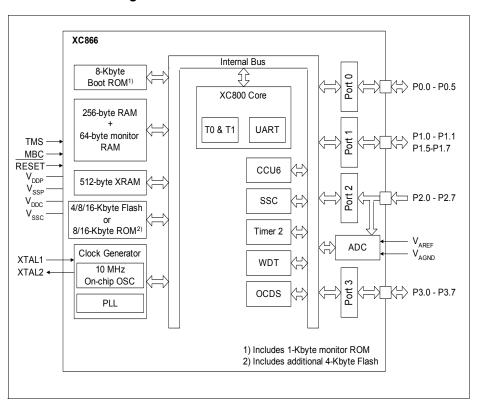


Figure 2 XC866 Block Diagram



2.2 Logic Symbol

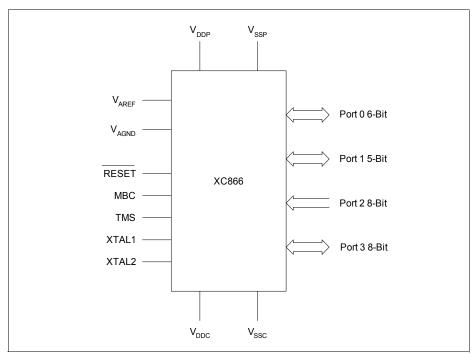


Figure 3 XC866 Logic Symbol



2.3 Pin Configuration

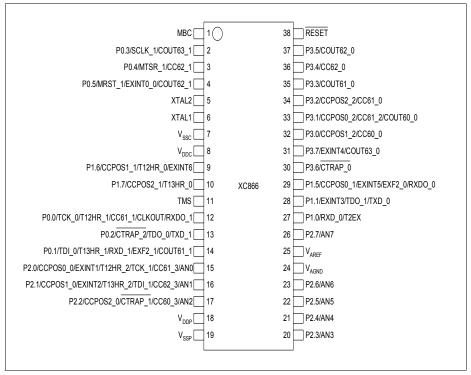


Figure 4 XC866 Pin Configuration, PG-TSSOP-38 Package (top view)



2.4 Pin Definitions and Functions

Table 3 Pin Definitions and Functions

Symbol	Pin Number	Туре	Reset State	Function	
P0		I/O		port. It can b	-bit bidirectional general purpose I/O e used as alternate functions for the 5, UART, and the SSC.
P0.0	12		Hi-Z	TCK_0 T12HR_1	JTAG Clock Input CCU6 Timer 12 Hardware Run Input
				CC61_1 CLKOUT RXDO_1	Input/Output of Capture/Compare channel 1 Clock Output UART Transmit Data Output
P0.1	14		Hi-Z	TDI_0 T13HR_1	JTAG Serial Data Input CCU6 Timer 13 Hardware Run Input
				RXD_1 COUT61_1	UART Receive Data Input
P0.2	13		PU	EXF2_1 CTRAP_2 TDO_0 TXD_1	Timer 2 External Flag Output CCU6 Trap Input JTAG Serial Data Output UART Transmit Data Output/ Clock Output
P0.3	2		Hi-Z	SCK_1 COUT63_1	SSC Clock Input/Output Output of Capture/Compare channel 3
P0.4	3		Hi-Z	MTSR_1 CC62_1	SSC Master Transmit Output/ Slave Receive Input Input/Output of Capture/Compare channel 2
P0.5	4		Hi-Z	MRST_1 EXINT0_0 COUT62_1	SSC Master Receive Input/ Slave Transmit Output External Interrupt Input 0 Output of Capture/Compare channel 2



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Туре	Reset State	Function	
P1		I/O		port. It can b	bit bidirectional general purpose I/O e used as alternate functions for the 5, UART, and the SSC.
P1.0	27		PU	RXD_0 T2EX	UART Receive Data Input Timer 2 External Trigger Input
P1.1	28		PU	EXINT3 TDO_1 TXD_0	External Interrupt Input 3 JTAG Serial Data Output UART Transmit Data Output/ Clock Output
P1.5	29		PU	CCPOS0_1 EXINT5 EXF2_0 RXDO_0	CCU6 Hall Input 0 External Interrupt Input 5 TImer 2 External Flag Output UART Transmit Data Output
P1.6	9		PU	CCPOS1_1 T12HR_0 EXINT6	CCU6 Hall Input 1 CCU6 Timer 12 Hardware Run Input External Interrupt Input 6
P1.7	10		PU	CCPOS2_1 T13HR_0	CCU6 Hall Input 2 CCU6 Timer 13 Hardware Run Input
					.6 can be used as a software chip t for the SSC.



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Туре	Reset State	Function	
P2		I		can be used inputs of the	a-bit general purpose input-only port. It as alternate functions for the digital JTAG and CCU6. It is also used as the s for the ADC.
P2.0	15		Hi-Z	CCPOS0_0 EXINT1 T12HR_2	CCU6 Hall Input 0 External Interrupt Input 1 CCU6 Timer 12 Hardware Run Input
				TCK_1 CC61_3 AN0	JTAG Clock Input Input of Capture/Compare channel 1 Analog Input 0
P2.1	16		Hi-Z	CCPOS1_0 EXINT2 T13HR_2	CCU6 Hall Input 1 External Interrupt Input 2 CCU6 Timer 13 Hardware Run Input
				TDI_1 CC62_3 AN1	JTAG Serial Data Input Input of Capture/Compare channel 2 Analog Input 1
P2.2	17		Hi-Z	CCPOS2_0 CTRAP_1 CC60_3 AN2	CCU6 Hall Input 2 CCU6 Trap Input Input of Capture/Compare channel 0 Analog Input 2
P2.3	20		Hi-Z	AN3	Analog Input 3
P2.4	21		Hi-Z	AN4	Analog Input 4
P2.5	22		Hi-Z	AN5	Analog Input 5
P2.6	23		Hi-Z	AN6	Analog Input 6
P2.7	26		Hi-Z	AN7	Analog Input 7



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Туре	Reset State	Function	
P3		I		Port 3 Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for the CCU6.	
P3.0	32		Hi-Z	CCPOS1_2 CC60_0	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0
P3.1	33		Hi-Z	CCPOS0_2 CC61_2	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1
				COUT60_0	Output of Capture/Compare channel 0
P3.2	34		Hi-Z	CCPOS2_2 CC61_0	CCU6 Hall Input 2 Input/Output of Capture/Compare channel 1
P3.3	35		Hi-Z	COUT61_0	Output of Capture/Compare channel 1
P3.4	36		Hi-Z	CC62_0	Input/Output of Capture/Compare channel 2
P3.5	37		Hi-Z	COUT62_0	Output of Capture/Compare channel 2
P3.6	30		PD	CTRAP_0	CCU6 Trap Input
P3.7	31		Hi-Z	EXINT4 COUT63_0	External Interrupt Input 4 Output of Capture/Compare channel 3



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Туре	Reset State	Function
V_{DDP}	18	-	_	I/O Port Supply (3.3 V/5.0 V) Also used by EVR and analog modules.
V _{SSP}	19	_	-	I/O Port Ground
V _{DDC}	8	_	_	Core Supply Monitor (2.5 V)
V _{SSC}	7	_	_	Core Supply Ground
V _{AREF}	25	_	_	ADC Reference Voltage
V _{AGND}	24	_	_	ADC Reference Ground
XTAL1	6	I	Hi-Z	External Oscillator Input (NC if not needed)
XTAL2	5	0	Hi-Z	External Oscillator Output (NC if not needed)
TMS	11	I	PD	Test Mode Select
RESET	38	I	PU	Reset Input
MBC ¹⁾	1	I	PU	Monitor & BootStrap Loader Control

¹⁾ An external pull-up device in the range of 4.7 kΩ to 100 kΩ is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.



3 Functional Description

3.1 Processor Architecture

The XC866 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC866 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. Access to the Flash memory, however, requires an additional wait state (one machine cycle). The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC866 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and SFRs.

Figure 5 shows the CPU functional blocks.

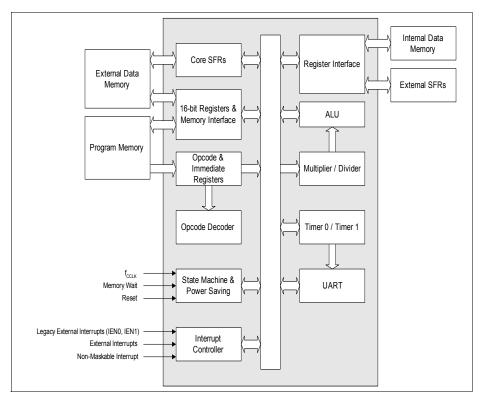


Figure 5 CPU Block Diagram



3.2 Memory Organization

The XC866 CPU operates in the following five address spaces:

- 8 Kbytes of Boot ROM program memory
- · 256 bytes of internal RAM data memory
- 512 bytes of XRAM memory (XRAM can be read/written as program memory or external data memory)
- · a 128-byte Special Function Register area
- 4/8/16 Kbytes of Flash program memory (Flash devices); or 8/16 Kbytes of ROM program memory, with additional 4 Kbytes of Flash (ROM devices)

Figure 6 illustrates the memory address spaces of the XC866-4FR device.

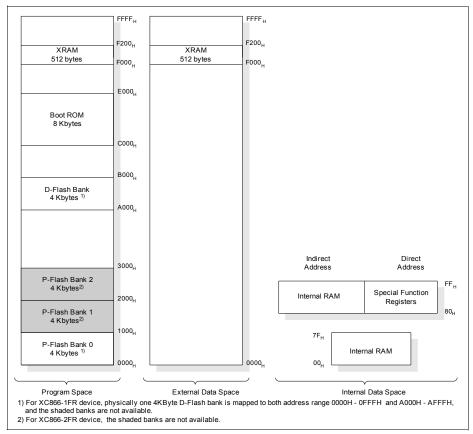


Figure 6 Memory Map of XC866 Flash Devices



Figure 7 illustrates the memory address spaces of the XC866-4RR device.

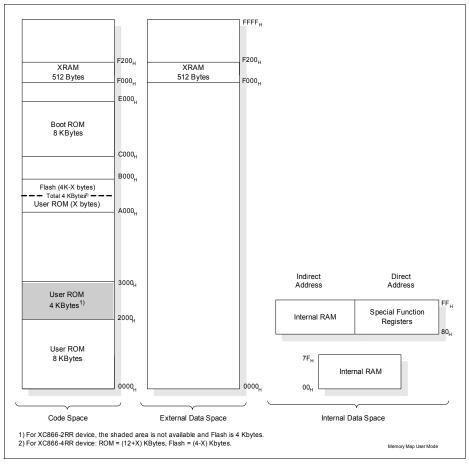


Figure 7 Memory Map of XC866 ROM Devices



3.2.1 Memory Protection Strategy

The XC866 memory protection strategy includes:

- Read-out protection: The Flash Memory can be enabled for read-out protection and ROM memory is always protected.
- Program and erase protection: The Flash memory in all devices can be enabled for program and erase protection.

Flash memory protection is available in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- · Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

Table 4 Flash Protection Modes

Mode	0	1				
Activation	Program a valid password via BSL m	node 6				
Selection	MSB of password = 0 MSB of password = 1					
P-Flash contents can be read by	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash				
P-Flash program and erase	Not possible	Not possible				
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash				
D-Flash program	Possible	Not possible				
D-Flash erase	Possible, on the condition that bit DFLASHEN in register MISC_CON is set to 1 prior to each erase operation	Not possible				

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. A password match triggers an automatic erase of the read-protected Flash contents, see **Table 5** and **Table 6**, and the programmed password is erased. The Flash protection is then disabled upon the next reset.

For XC866-2FR and XC866-4FR devices:

The selection of protection type is summarized in **Table 5**.



Table 5 Flash Protection Type for XC866-2FR and XC866-4FR devices

PASSWORD	71	Flash Banks to Erase when Unprotected
1XXXXXXX _B	Flash Protection Mode 1	All Banks
0XXXXXXX _B	Flash Protection Mode 0	P-Flash Bank

For XC866-1FR device and ROM devices:

The selection of protection type is summarized in **Table 6**.

Table 6 Flash Protection Type for XC866-1FR device and ROM devices

PASSWORD	Type of Protection (Applicable to the whole Flash)	Sectors to Erase when Unprotected	Comments
1XXXXXXX _B	Read/Program/Erase	All Sectors	Compatible to Protection mode 1
00001XXX _B	Erase	Sector 0	
00010XXX _B	Erase	Sector 0 and 1	
00011XXX _B	Erase	Sector 0 to 2	
00100XXX _B	Erase	Sector 0 to 3	
00101XXX _B	Erase	Sector 0 to 4	
00110XXX _B	Erase	Sector 0 to 5	
00111XXX _B	Erase	Sector 0 to 6	
01000XXX _B	Erase	Sector 0 to 7	
01001XXX _B	Erase	Sector 0 to 8	
01010XXX _B	Erase	All Sectors	
Others	Erase	None	

Although no protection scheme can be considered infallible, the XC866 memory protection strategy provides a very high level of protection for a general purpose microcontroller.



Reset Value: 00_H

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range $80_{\rm H}$ to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range $80_{\rm H}$ to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_{\rm H}$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

SYSCON0 System Control Register 0

7	6	5	4	3	2	1	0
		0	I	I	1	0	RMAP
		r	1	I	rw	r	rw

Field	Bits	Type	Description
RMAP	0	rw	Special Function Register Map Control The access to the standard SFR area is enabled. The access to the mapped SFR area is enabled.
1	2	rw	Reserved Returns the last value if read; should be written with 1.
0	1,[7:3]	r	Reserved Returns 0 if read; should be written with 0.



Note: The RMAP bit must be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

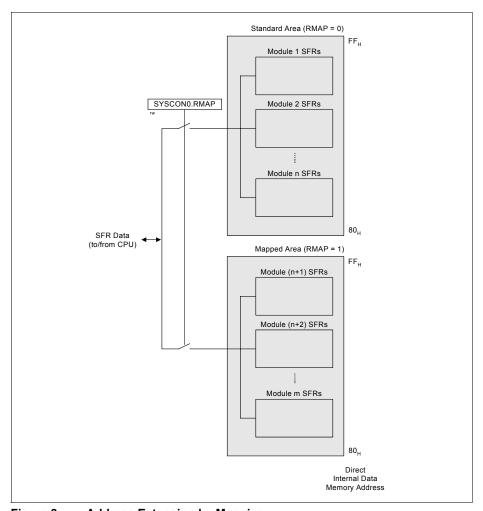


Figure 8 Address Extension by Mapping



3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC866 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in Figure 9.

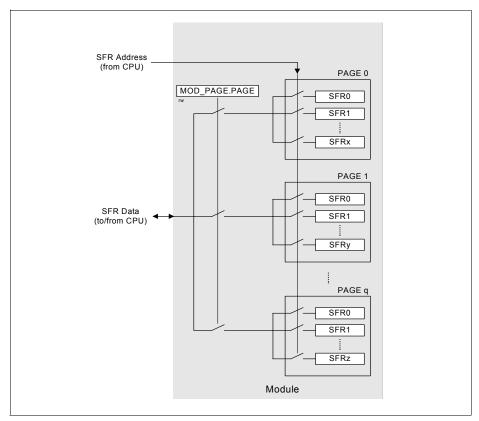


Figure 9 Address Extension by Paging



In order to access a register located in a page different from the actual one, the current page must be left. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and finally, the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or
- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

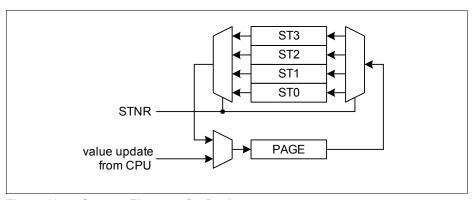


Figure 10 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC866 supports local address extension for:

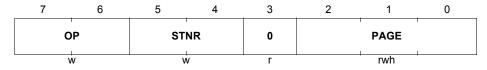
- · Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers



The page register has the following definition:

MOD_PAGE Page Register for module MOD

Reset Value: 00_H



Field	Bits	Туре	Description
PAGE	[2:0]	rwh	Page Bits When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	Storage Number This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10 _B , the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11 _B , the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. O ST0 is selected. O ST1 is selected. TS1 is selected. TS1 is selected. TS3 is selected.



Field	Bits	Type	Description
OP	[7:6]	W	 Operation Manual page mode. The value of STNR is ignored and PAGE is directly written. New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR. Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.
0	3	r	Reserved Returns 0 if read; should be written with 0.



Reset Value: 07_H

3.2.3 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected bits (i.e., protected bits) using the PASSWD register. When the bit field MODE is 11_B , writing 10011_B to the bit field PASS opens access to writing of all protected bits, and writing 10101_B to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with 98_H or 48_H . It can only be changed when bit field PASS is written with 11000_B , for example, writing 100_H to PASSWD register disables the bit protection scheme.

The access is opened for maximum 32 CCLKs if the "close access" password is not written. If "open access" password is written again before the end of 32 CCLK cycles, there will be a recount of 32 CCLK cycles. The protected bits include NDIV, WDTEN, PD, and SD.

PASSWD Password Register

7	6	5	4	3	2	1	0
	1	PASS	1	1	PROTECT _S	МОІ	DE
		W			rh	rw	1

Field	Bits	Туре	Description
MODE	[1:0]	rw	Bit Protection Scheme Control bits 00 Scheme Disabled 11 Scheme Enabled (default) Others: Scheme Enabled These two bits cannot be written directly. To change the value between 11 _B and 00 _B , the bit field PASS must be written with 11000 _B ; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	Bit Protection Signal Status bit This bit shows the status of the protection. O Software is able to write to all protected bits. Software is unable to write to any protected bits.
PASS	[7:3]	W	Password bits The Bit Protection Scheme only recognizes three patterns. 11000 _B Enables writing of the bit field MODE. 10011 _B Opens access to writing of all protected bits. 10101 _B Closes access to writing of all protected bits.



3.2.4 XC866 Register Overview

The SFRs of the XC866 are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in **Table 7** to **Table 15**, with the addresses of the bitaddressable SFRs appearing in bold typeface.

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Table 7 CPU Register Overview

Addr	Register Name		Bit	7	6	5	4	3	2	1	0	
RMAP =	0 or 1		I.	1	I		I	I	I	I	ı	
81 _H	SP	Reset: 07 _H	Bit Field				S	P				
	Stack Pointer Register		Туре				r	w				
82 _H	DPL	Reset: 00 _H	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0	
	Data Pointer Register Lo	ow	Туре	rw	rw	rw	rw	rw	rw	rw	rw	
83 _H	DPH	Reset: 00 _H	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0	
	Data Pointer Register H	igh	Туре	rw	rw	rw	rw	rw	rw	rw	rw	
87 _H	PCON	Reset: 00 _H	Bit Field	SMOD		0		GF1	GF0	0	IDLE	
	Power Control Register		Туре	rw		r		rw	rw	r	rw	
88 _H	TCON	Reset: 00 _H	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
	Timer Control Register		Туре	rwh	rw	rwh	rw	rwh	rw	rwh	rw	
89 _H	TMOD	Reset: 00 _H	Bit Field	GATE1	0	T1	IM	GATE0	0	TO	M	
	Timer Mode Register		Туре	rw	r	r	W	rw	r	r	w	
8A _H	TL0	Reset: 00 _H	Bit Field				V	AL				
	Timer 0 Register Low		Туре				rv	vh				
8B _H	TL1	Reset: 00 _H	Bit Field				V	AL				
	Timer 1 Register Low		Туре	rwh								
8C _H	TH0	Reset: 00 _H	Bit Field				V	AL				
	Timer 0 Register High		Туре				rv	vh				
8D _H	TH1	Reset: 00 _H	Bit Field				V	AL				
	Timer 1 Register High		Туре				rv	vh				
98 _H	SCON	Reset: 00 _H	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
	Serial Channel Control F	Register	Туре	rw	rw	rw	rw	rw	rwh	rwh	rwh	
99 _H	SBUF	Reset: 00 _H	Bit Field				V	AL				
	Serial Data Buffer Regis	ter	Туре				rv	vh				
A2 _H	EO Extended Operation Reg	Reset: 00 _H	Bit Field		0		TRAP_ EN		0		DPSEL 0	
	Exterided Operation Res	gistei	Туре		r		rw		r		rw	
A8 _H	IEN0	Reset: 00 _H	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0	
Аон	Interrupt Enable Registe		Туре	rw	r	rw	rw	rw	rw	rw	rw	
B8 _H	IP.	Reset: 00 _H	Bit Field)	PT2	PS	PT1	PX1	PT0	PX0	
Бон	Interrupt Priority Registe		Туре		r	rw	rw	rw	rw	rw	rw	
B9 _H	IPH	Reset: 00 _H	Bit Field)	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	
БЭН	Interrupt Priority Registe		Туре		r	rw	rw	rw	rw	rw	rw	
D0 _H	PSW	Reset: 00 _H	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P	
- •н	Program Status Word R		Туре	rw	rwh	rwh	rw	rw	rwh	rwh	rh	
E0 _H	ACC	Reset: 00 _H	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0	
-11	Accumulator Register		Туре	rw	rw	rw	rw	rw	rw	rw	rw	
E8 _H	IEN1	Reset: 00 _H	Bit Field	ECCIP	ECCIP	ECCIP	ECCIP	EXM	EX2	ESSC	EADC	
-11	Interrupt Enable Registe			3	2	1	0					
			Type	rw	rw	rw	rw	rw	rw	rw	rw	



Table 7 CPU Register Overview (cont'd)

Addr	Register Name		Bit	7	6	5	4	3	2	1	0
F0 _H		eset: 00 _H	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
	B Register		Туре	rw	rw	rw	rw	rw	rw	rw	rw
F8 _H	IP1 R Interrupt Priority Register 1	eset: 00 _H	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
			Туре	rw	rw	rw	rw	rw	rw	rw	rw
F9 _H	IPH1 R Interrupt Priority Register 1	eset: 00 _H High	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSCH	PADC H
			Туре	rw	rw	rw	rw	rw	rw	rw	rw

The system control SFRs can be accessed in the standard memory area (RMAP = 0).

Table 8 System Control Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	0 or 1			1			I		I	
8F _H	SYSCON0 Reset: 00 _H	Bit Field				0				RMAP
	System Control Register 0	Туре				r				rw
RMAP =	0									
BF _H	SCU_PAGE Reset: 00 _H	Bit Field	C)P	ST	NR	0		PAGE	
	Page Register for System Control	Туре	,	w	١	N	r		rwh	
RMAP =	0, Page 0	•								
B3 _H	MODPISEL Reset: 00 _H Peripheral Input Select Register	Bit Field			JTAG TDIS	JTAG TCKS	(0	EXINT 0IS	URRIS
		Туре		r	rw	rw		r	rw	rw
B4 _H	IRCON0 Reset: 00 _H Interrupt Request Register 0	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0
		Туре	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B5 _H	IRCON1 Reset: 00 _H Interrupt Request Register 1	Bit Field		0		ADCS RC1	ADCS RC0	RIR	TIR	EIR
		Туре		r		rwh	rwh	rwh	rwh	rwh
B7 _H	EXICON0 Reset: 00 _H	Bit Field	EXINT3		EXINT2		EXI	NT1	EXI	NT0
	External Interrupt Control Register 0	Туре	rw		r	rw		w	r	w
BA _H	EXICON1 Reset: 00 _H	Bit Field	0		EXI	NT6	EXI	NT5	EXI	NT4
	External Interrupt Control Register 1	Туре	r		rw		rw		rw	
BB _H	NMICON Reset: 00 _H NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	NMI VDD	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Туре	r	rw	rw	rw	rw	rw	rw	rw
BC _H	NMISR Reset: 00 _H NMI Status Register	Bit Field	0	FNMI ECC	FNMI VDDP	FNMI VDD	FNMI OCDS	FNMI FLASH	FNMI PLL	FNMI WDT
		Туре	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
BD_H	BCON Reset: 00 _H	Bit Field	BG	SEL	0	BREN		BRPRE		R
	Baud Rate Control Register	Туре	r	w	r	rw		rw		rw
BE _H	BG Reset: 00 _H	Bit Field				BR_V	ALUE			
	Baud Rate Timer/Reload Register	Туре					w			
E9 _H	FDCON Reset: 00 _H Fractional Divider Control Register	Bit Field	BGS	SYNEN	ERRSY N	EOFSY N	BRK	NDOV	FDM	FDEN
		Туре	rw	rw	rwh	rwh	rwh	rwh	rw	rw
EA _H	FDSTEP Reset: 00 _H	Bit Field				ST	EP			
	Fractional Divider Reload Register	Туре	ype rw							
EB _H	FDRES Reset: 00 _H	Bit Field				RES	ULT			
	Fractional Divider Result Register	Туре				r	h			
RMAP =	0, Page 1									



Table 8 System Control Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
B3 _H	ID Reset: 01 _h	Bit Field			PRODID)			VERID	ı	
	Identity Register	Туре			r				r		
B4 _H	PMCON0 Reset: 00 _h Power Mode Control Register 0	Bit Field	0	WDT RST	WKRS	WK SEL	SD	PD	W	/S	
		Туре	r	rwh	rwh	rw	rw	rwh	r	rw	
B5 _H	PMCON1 Reset: 00 _H Power Mode Control Register 1	Bit Field						SSC _DIS	ADC _DIS		
		Type			r		rw	rw	rw	rw	
B6 _H	OSC_CON Reset: 08 _H OSC Control Register	Bit Field		0		OSC PD	XPD	OSC SS	ORD RES	OSCR	
		Type		r		rw	rw	rw	rwh	rh	
B7 _H	PLL_CON Reset: 20 _H PLL Control Register	Bit Field		NI	OIV		VCO BYP	OSC DISC	RESLD	LOCK	
		Туре		r	w		rw	rw	rwh	rh	
BA _H	CMCON Reset: 00 _h Clock Control Register	Bit Field	VCO 0 CLKREL SEL				REL				
		Type	rw		r			r	rw		
BB _H	PASSWD Reset: 07 _H Password Register	Bit Field			PASS			PROTE CT_S	MC	DDE	
		Туре			W			rh	r	W	
BC _H	FEAL Reset: 00 _H	Bit Field			E	CCERR	ADDR[7:	0]			
	Flash Error Address Register Low	Туре					th .				
BD_H	FEAH Reset: 00 _H				E	CCERRA	ADDR[15	:8]			
	Flash Error Address Register High	Type					'h				
BE _H	COCON Reset: 00 _H Clock Output Control Register	Bit Field	()	TLEN	COUT		СО	REL		
		Туре		r	rw	rw		r	w		
E9 _H	MISC_CON Reset: 00 _h Miscellaneous Control Register	Bit Field				0				DFLAS HEN	
		Туре				r				rwh	
	0, Page 3										
B3 _H	XADDRH Reset: F0 _H	' L				ADI	DRH				
	On-Chip XRAM Address Higher Orde	Type				r	W				

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
RMAP =	1	1	!			!	!		!	!		
BB _H	WDTCON Reset: 00 _H Watchdog Timer Control Register	Bit Field	'	0	WINB EN	WDT PR	0	WDT EN	WDT RS	WDT IN		
		Туре		r	rw	rh	r	rw	rwh	rw		
BC _H	WDTREL Reset: 00 _H	Bit Field				WD1	REL					
	Watchdog Timer Reload Register	Туре	rw									
BD _H	WDTWINB Reset: 00 _H Watchdog Window-Boundary Count	Bit Field				WDT	WINB					
	Register	Туре				r	w					
BE _H	WDTL Reset: 00 _H	Bit Field				WDT	Γ[7:0]					
	Watchdog Timer Register Low	Туре				r	h					
BF _H	WDTH Reset: 00 _H	Bit Field				WDT	[15:8]					
	Watchdog Timer Register High	Туре				r	h					



The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	0	ı	I							
B2 _H	PORT_PAGE Reset: 00 _H	Bit Field	C)P	ST	NR	0		PAGE	
	Page Register for PORT	Туре	,	N	,	N	r		rwh	
RMAP =	0, Page 0		1							
80 _H	P0_DATA Reset: 00 _H	Bit Field		0	P5	P4	P3	P2	P1	P0
	P0 Data Register	Туре		r	rwh	rwh	rwh	rwh	rwh	rwh
86 _H	P0_DIR Reset: 00 _H	Bit Field		0	P5	P4	P3	P2	P1	P0
	P0 Direction Register	Туре		r	rw	rw	rw	rw	rw	rw
90 _H	P1_DATA Reset: 00 _H	Bit Field	P7	P6	P5		0	•	P1	P0
	P1 Data Register	Туре	rwh	rwh	rwh		r		rwh	rwh
91 _H	P1_DIR Reset: 00 _H	Bit Field	P7	P6	P5		0		P1	P0
	P1 Direction Register	Type	rw	rw	rw		r		rw	rw
A0 _H	P2_DATA Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P2 Data Register	Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
A1 _H	P2_DIR Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P2 Direction Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_DATA Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Data Register	Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B1 _H	P3_DIR Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Direction Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
	0, Page 1									
80 _H	P0_PUDSEL Reset: FF _H	Bit Field		0	P5	P4	P3	P2	P1	P0
	P0 Pull-Up/Pull-Down Select Register	Туре		r	rw	rw	rw	rw	rw	rw
86 _H	P0_PUDEN Reset: C4 _H	Bit Field		0	P5	P4	P3	P2	P1	P0
	P0 Pull-Up/Pull-Down Enable Register	1 9 P C		r	rw	rw	rw	rw	rw	rw
90 _H	P1_PUDSEL Reset: FF _H	Bit Field	P7	P6	P5		0		P1	P0
	P1 Pull-Up/Pull-Down Select Register	Туре	rw	rw	rw		r		rw	rw
91 _H	P1_PUDEN Reset: FF _H	Bit Field	P7	P6	P5		0		P1	P0
	P1 Pull-Up/Pull-Down Enable Register	1 9 P C	rw	rw	rw		r		rw	rw
A0 _H	P2_PUDSEL Reset: FF _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P2 Pull-Up/Pull-Down Select Register	Type	rw	rw	rw	rw	rw	rw	rw	rw
A1 _H	P2_PUDEN Reset: 00 _H P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		турс	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_PUDSEL Reset: BF _H P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	'	Туре	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_PUDEN Reset: 40 _H P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
DAMAD		Туре	rw	rw	rw	rw	rw	rw	rw	rw
	0, Page 2	Ina reals		^	Dr	D4	_ D0	D0	D4	DO
80 _H	P0_ALTSEL0 Reset: 00 _H P0 Alternate Select 0 Register	Bit Field		0	P5	P4	P3	P2	P1	P0
00	<u> </u>	Type		r	rw	rw P4	rw	rw	rw P1	rw
86 _H	P0_ALTSEL1 Reset: 00 _H P0 Alternate Select 1 Register	Bit Field		0	P5		P3	P2		P0
00	<u> </u>	Type Bit Field	P7	r P6	rw P5	rw	rw 0	rw	rw P1	rw P0
90 _H	P1_ALTSEL0 Reset: 00 _H P1 Alternate Select 0 Register				-					
04	•	Type	rw D7	rw	rw		r		rw D4	rw
91 _H	P1_ALTSEL1 Reset: 00 _H P1 Alternate Select 1 Register	Bit Field	P7	P6	P5		0		P1	P0
B0	<u> </u>	Type Bit Field	IW D7	rw	rw P5	P4	r P3	Do	rw P1	rw P0
B0 _H	P3_ALTSEL0 Reset: 00 _H P3 Alternate Select 0 Register	Bit Field	P7	P6	-			P2		
	. C. Mainate Coloct o Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw



Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
111	P3_ALTSEL1 Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Alternate Select 1 Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
RMAP =	0, Page 3									
80 _H	P0_OD Reset: 00 _H	Bit Field	()	P5	P4 P3 P2			P1	P0
	P0 Open Drain Control Register	Туре		r	rw	rw	rw	rw	rw	rw
90 _H	P1_OD Reset: 00 _H	Bit Field	P7	P6	P5		0	P1	P0	
	P1 Open Drain Control Register	Туре	rw	rw	rw		r	rw	rw	
B0 _H	P3_OD Reset: 00 _H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Open Drain Control Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 11 ADC Register Overview

Addr	Register Name		Bit	7	6	5	4	3	2	1	0	
RMAP =	0		1	-1	1		1	1	1		I	
D1 _H	ADC_PAGE	Reset: 00 _H	Bit Field	C	OP STNR			0	PAGE			
	Page Register for ADC		Туре	w w			r	rwh				
RMAP =	0, Page 0											
CA _H	Global Control Register		Bit Field	ANON	DW	C.	TC		()		
			Туре	rw	rw	r	w			r		
CB _H	Global Status Register		Bit Field	0		CHNR			0	SAM PLE	BUSY	
			Туре		r		rh		r	rh	rh	
CCH	ADC_GLOBCTR Global Control Register ADC_GLOBSTR Global Status Register ADC_PRAR Priority and Arbitration Re ADC_LCBR Limit Check Boundary Re ADC_INPCR0 Input Class Register 0 ADC_ETRCR External Trigger Control I ADC_CHCTR0 Channel Control Register ADC_CHCTR1 Channel Control Register ADC_CHCTR2 Channel Control Register ADC_CHCTR2 Channel Control Register	Reset: 00 _H	Bit Field	ASEN1	ASEN0	0	ARBM	CSM1	PRIO1	CSM0	PRIO	
	Priority and Arbitration R	egister	Туре	rw	rw	r	rw	rw	rw	rw	rw	
					BOL	JND1			BOUND0			
	Limit Check Boundary Ro	egister	Туре		r	w			r	w		
CEH				STC								
	Input Class Register 0		Туре				r	W				
CF _H	External Trigger Control Register		Bit Field	SYNEN 1	SYNEN SYNEN ETRSEL 1 0				1 ETRSEL0			
			Туре	rw	rw		rw		rw			
RMAP =	0, Page 1											
CA _H	ADC_CHCTR0 Reset: 00 _H	Bit Field	0		LCC		0		RES	RSEL		
	· ·	r 0	Туре	r	rw		r			w		
CB _H		Reset: 00 _H	Bit Field	0	LCC		0		RES	RSEL		
	ū		Туре	r		rw			r	rw		
CCH		Reset: 00 _H	Bit Field	0	LCC		0		RESRSEL			
	•		Туре	r		rw		r		rw		
CD _H	ADC_CHCTR3	Reset: 00 _H	Bit Field	0	0 LCC		0		RESRSEL			
	Channel Control Registe	r 3	Туре	r		rw			r	rw		
CE _H	ADC_CHCTR4	Reset: 00 _H	Bit Field	0	LCC			0		RESRSEL		
	Channel Control Registe		Туре	r		rw		r		rw		
CF _H	ADC_CHCTR5	Reset: 00 _H	Bit Field	0	LCC			0		RESRSEL		
	Channel Control Registe		Type Bit Field	r		rw		r		rw		
D2 _H		ADC_CHCTR6 Reset: 00 _H		0	0 LCC			0		RES	RSEL	
	Channel Control Registe		Туре	r			r		rw			
D3 _H	ADC_CHCTR7	Reset: 00 _H	Bit Field	0		LCC		0		RES	RSEL	
Channel Control Register 7		r /	Type	r	r rw				r rw			



Table 11 ADC Register Overview (cont'd)

Register Name		Bit	7	6	5	4	3	2	1	0				
ADC_RESR0L	Reset: 00 _H	Bit Field	RESUI	LT[1:0]	0	VF	DRC		CHNR					
Result Register 0 Low		Туре	r	h	r	rh	rh							
ADC_RESR0H	Reset: 00 _H	Bit Field	RESULT[9:2]											
Result Register 0 High		Туре	rh											
ADC_RESR1L	Reset: 00 _H	Bit Field	RESUI	LT[1:0]	0	VF	DRC	CHNR						
Result Register 1 Low		Туре	rl	h	r	rh	rh rh							
ADC_RESR1H	Reset: 00 _H	Bit Field				RESU	LT[9:2]							
Result Register 1 High		Туре				r	h							
ADC_RESR2L	esuit Register 0 Low DC_RESR0H esuit Register 1 High DC_RESR1L esuit Register 1 High DC_RESR1H esuit Register 1 High DC_RESR2L esuit Register 2 Low DC_RESR2H esuit Register 2 High DC_RESR2H esuit Register 3 Low DC_RESR3H esuit Register 3 Low DC_RESR3H esuit Register 3 Low DC_RESR3H esuit Register 3 High Page 3 DC_RESR3H esuit Register 0, View A Low DC_RESRA0H esuit Register 0, View A High DC_RESRA1H esuit Register 1, View A High DC_RESRA1H esuit Register 1, View A High DC_RESRA2H esuit Register 1, View A Low DC_RESRA1H esuit Register 1, View A High DC_RESRA2H esuit Register 2, View A Low DC_RESRA2H esuit Register 2, View A Low DC_RESRA3H esuit Register 2, View A High DC_RESRA3H esuit Register 3, View A High DC_RESRA3H esuit Register 3	Bit Field	RESUI	LT[1:0]	0	VF	DRC		CHNR					
Result Register 2 Low		Туре	rl	h	r	rh	rh		rh					
Result Register 0 Low ADC_RESR0H Reset: 00H	Bit Field				RESU	LT[9:2]								
		Туре				r	h							
ADC_RESR3L	Reset: 00 _H	Bit Field	RESUI	LT[1:0]	0	VF	DRC		CHNR					
Result Register 3 Low		Туре	ri	h	r	rh	rh		rh					
ADC_RESR3H	Reset: 00 _H	Bit Field				RESU	LT[9:2]							
Result Register 3 High		Туре				r	h		CHNR rh CHNR rh					
0, Page 3														
ADC_RESRA0L		Bit Field	RE	SULT[2	:0]	VF	DRC		CHNR					
•		Туре	rh			rh	rh	h rh						
ADC_RESRA0H				RESULT[10:3]										
Result Register 0, View A	Туре	rh												
		Bit Field	RE	ESULT[2	:0]	VF								
•				rh		rh	rh		rh					
ADC_RESRA1H			RESULT[10:3]											
Result Register 1, View A	N High	Туре	rh											
		Bit Field	RESULT[2:0]			VF	DRC	CHNR						
	lesult Register 2, View A Low		rh			rh	***							
			RESULT[10:3]											
•	High					r	h							
		Bit Field	RE	ESULT[2	:0]	VF			CHNR					
•	Low	Туре		rh		rh	rh		rh					
	High	Type				r	h							
		Bit Field	VFCTR	WFR	0	IEN		0		DRCT R				
		Туре	rw	rw	r	rw		r		rw				
ADC_RCR1 Result Control Register 1		Bit Field	VFCTR	WFR	0	IEN	0			DRCT R				
		Туре	rw	rw	r	rw		r		rw				
ADC_RCR2 Result Control Register 2	Reset: 00 _H	Bit Field	VFCTR	WFR	0	IEN		0		DRCT R				
		Туре	rw	rw	r	rw		r		rw				
ADC_RCR3 Result Control Register 3		Bit Field	VFCTR	WFR	0	IEN		0		DRCT R				
<u> </u>		Туре	rw	rw	r	rw		r		rw				
ADC VECD	Reset: 00 _H	Bit Field			VFC3	VFC2	VFC1	VFC0						
ADC_VFCR Valid Flag Clear Register		Туре	r											
	Result Register 0 Low ADC_RESR0H Result Register 0 High ADC_RESR1H Result Register 1 Low ADC_RESR1H Result Register 2 Low ADC_RESR2L Result Register 2 High ADC_RESR2H Result Register 3 Low ADC_RESR3H Result Register 3 Low ADC_RESR3H Result Register 3 High 0, Page 3 ADC_RESR3H Result Register 0, View A ADC_RESRA0L Result Register 0, View A ADC_RESRA1H Result Register 1, View A ADC_RESRA1H Result Register 1, View A ADC_RESRA1H Result Register 1, View A ADC_RESRA1H Result Register 2, View A ADC_RESRA2H Result Register 2, View A ADC_RESRA3H Result Register 3, View A ADC_RESRA3H Result Register 3	Result Register 0 Low ADC_RESR0H Result Register 0 High ADC_RESR1L Result Register 1 Low ADC_RESR1H Result Register 1 High ADC_RESR1H Result Register 2 Low ADC_RESR2L Reset: 00 _H Result Register 2 Low ADC_RESR3H Result Register 2 High ADC_RESR3H Result Register 3 Low ADC_RESR3H Result Register 3 Low ADC_RESR3H Result Register 3 High 0, Page 3 ADC_RESR3H Result Register 0, View A Low ADC_RESRA0H Result Register 0, View A Low ADC_RESRA1H Result Register 0, View A High ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 2, View A Low ADC_RESRA2L Reset: 00 _H Result Register 2, View A Low ADC_RESRA2L Reset: 00 _H Result Register 2, View A Low ADC_RESRA2L Reset: 00 _H Result Register 3, View A High ADC_RESRA3H Reset: 00 _H Result Register 3, View A High ADC_RESRA3H Reset: 00 _H Result Register 3, View A High ADC_RESRA3H Reset: 00 _H Result Control Register 0 ADC_RESR 4 ADC_RCR0 Reset: 00 _H Result Control Register 1 ADC_RCR1 Reset: 00 _H Reset: 00 _H Result Control Register 2	Result Register 0 Low ADC_RESR0H Result Register 0 High ADC_RESR1L Result Register 1 Low ADC_RESR1H Result Register 1 High ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 2 High ADC_RESR2H Reset: 00H Result Register 2 High ADC_RESR2H Reset: 00H Result Register 3 High ADC_RESR3H Reset: 00H Result Register 3 High 0, Page 3 ADC_RESR3H Reset: 00H Result Register 3 High 0, Page 3 ADC_RESRA0L Reset: 00H Result Register 0, View A Low ADC_RESRA0H Reset: 00H Result Register 0, View A High ADC_RESRA1H Result Register 1, View A High ADC_RESRA1H Result Register 1, View A High ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Reset: 00H Result Register 1, View A High ADC_RESRA2L Reset: 00H Result Register 2, View A Low ADC_RESRA2H Reset: 00H Result Register 2, View A High ADC_RESRA3H Reset: 00H Result Register 2, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Control Register 0 ADC_RESRA3H Reset: 00H Result Control Register 0 ADC_RESRA3H Reset: 00H Reset: 00H Result Control Register 0 ADC_RESRA3H Reset: 00H Reset: 00H Result Control Register 0 ADC_RESRA3H Reset: 00H Reset:	Result Register 0 Low ADC_RESR0H Result Register 0 High ADC_RESR1L Reset: 00H Result Register 1 Low ADC_RESR1H Result Register 1 High ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 2 High ADC_RESR3H Reset: 00H Result Register 2 High ADC_RESR3H Reset: 00H Result Register 3 Low ADC_RESR3H Reset: 00H Result Register 3 Low ADC_RESR3H Reset: 00H Result Register 3 High 0, Page 3 ADC_RESR3H Reset: 00H Result Register 0, View A Low ADC_RESR3H Reset: 00H Result Register 0, View A Low ADC_RESR3H Reset: 00H Result Register 1, View A Low ADC_RESR3H Reset: 00H Result Register 1, View A Low ADC_RESR3H Reset: 00H Result Register 1, View A Low ADC_RESR3H Reset: 00H Result Register 2, View A Low ADC_RESR3H Reset: 00H Result Register 2, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A Low ADC_RESR3H Reset: 00H Result Register 3, View A High Type ADC_RESR3H Reset: 00H Reset: 00H Result Register 3, View A High ADC_RESR3H Reset: 00H Reset: 00H Result Register 3, View A High ADC_RESR3H Reset: 00H Reset: 00H Result Register 3, View A High ADC_RESR3H Reset: 00H Reset: 00H Result Control Register 0 ADC_RESR Reset: 00H Reset: 00H Result Control Register 1 ADC_RCR2 Reset: 00H Reset: 00H Reset: 00H Rit Field RETERION Reset: 00H Reset	Result Register 0 Low ADC_RESR0H Result Register 0 High ADC_RESR1L Result Register 1 Low ADC_RESR1H Result Register 1 High ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 2 High ADC_RESR2L Reset: 00H Result Register 2 High ADC_RESR3L Reset: 00H Result Register 2 High ADC_RESR3L Reset: 00H Result Register 3 Low ADC_RESR3H Result Register 3 High 0, Page 3 ADC_RESR3H Reset: 00H Result Register 0, View A Low ADC_RESRA0L Reset: 00H Result Register 0, View A High ADC_RESRA1L Reset: 00H Result Register 1, View A Low ADC_RESRA1L Reset: 00H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 2, View A Low ADC_RESRA1H Result Register 2, View A Low ADC_RESRA1L Reset: 00H Result Register 2, View A Low ADC_RESRA1L Reset: 00H Result Register 3, View A Low ADC_RESRA1L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3H Result Register 3, View A High Type ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A Low ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Register 3, View A High ADC_RESRA3H Reset: 00H Result Control Register 1 Type Reset: 00H Result Control Register 2 Reset: 00H Reset: 00H Result Control Register 3 Reset: 00H Reset: 00H Result Control Register 3 Reset: 00H Reset: 00H Result Control Register 3 Reset: 00H Reset:	Result Register 0 Low ADC_RESR0H Result Register 1 Low ADC_RESR1L Result Register 1 High ADC_RESR1H Result Register 1 High ADC_RESR2L Result Register 2 Low ADC_RESR2L Result Register 2 Low ADC_RESR2L Result Register 2 High ADC_RESR3H Result Register 3 Low ADC_RESR3L Result Register 3 Low ADC_RESR3L Result Register 3 Low ADC_RESR3H Result Register 0, View A Low ADC_RESR4DL Result Register 1, View A Low ADC_RESR4H Result Register 1, View A Low ADC_RESR4H Result Register 1, View A Low ADC_RESR4H Result Register 1, View A Low ADC_RESRA1L Result Register 1, View A Low ADC_RESRA1L Result Register 1, View A Low ADC_RESRA1L Result Register 2, View A High ADC_RESRA2L Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 4, View A Low ADC_RESRA3L Reset: 00H Result Register 5, View A Low ADC_RESRA3L Reset: 00H Result Register 6, View A Low ADC_RESRA3L Reset: 00H Result Register 6, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Result Register 7, View A Low ADC_RESRA3L Reset: 00H Resu	Result Register 0 Low ADC_RESR0H Result Register 1 Low ADC_RESR1L Reset: 00H Result Register 1 High ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 2 Low ADC_RESR2L Reset: 00H Result Register 3 High ADC_RESR3H Result Register 3 Low ADC_RESR3H Result Register 3 Low ADC_RESR3H Reset: 00H Result Register 3 High ADC_RESR3H Reset: 00H Result Register 0, View A Low ADC_RESRA0L Reset: 00H Result Register 0, View A Low ADC_RESRA1L Reset: 00H Result Register 0, View A Low ADC_RESRA1H Result Register 0, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA1H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA1L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 1, View A Low ADC_RESRA2L Reset: 00H Result Register 2, View A Low ADC_RESRA2L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low ADC_RESRA3L Reset: 00H Result Register 3, View A Low Bit Field RESULT[2:0] VF Type rh rh rh ADC_RESRA3L Reset: 00H Result Register 3, View A Low Bit Field RESULT[2:0] VF Type rh rh rh rh ADC_RESRA3L Reset: 00H Result Register 3, View A Low Bit Field RESULT[2:0] VF Type rh rh rh rh rh rh rh rh rh r	Result Register 0 Low	Result Register 0 Low	Result Register 0 Low ADC_RESR0H Reset: 00H Bit Field RESULT[1:0] O VF DRC CHNR CHNR				



Table 11 ADC Register Overview (cont'd)

CA _H				6	5	4	3	2	1	0
	ADC_CHINFR Reset: 00 _H	Bit Field	CHINF	CHINF	CHINF	CHINF	CHINF	CHINF	CHINF	CHINF
	Channel Interrupt Flag Register		7	6	5	4	3	2	1	0
		Туре	rh	rh	rh	rh	rh	rh	rh	rh
CB _H	ADC_CHINCR Reset: 00 _H	Bit Field	CHINC	CHINC	CHINC	CHINC	CHINC	CHINC	CHINC	CHINC
	Channel Interrupt Clear Register		7	6	5	4	3	2	1	0
		Type	w	W	W	W	w	w	w	w
CCH	ADC_CHINSR Reset: 00 _H	Bit Field	CHINS	CHINS	CHINS	CHINS	CHINS	CHINS	CHINS	CHINS
	Channel Interrupt Set Register		7	6	5	4	3	2	1	0
		Туре	w	W	W	W	w	w	w	w
CD _H	ADC_CHINPR Reset: 00 _H	Bit Field	CHINP	CHINP	CHINP	CHINP	CHINP	CHINP	CHINP	CHINP
	Channel Interrupt Node Pointer Register	_	7	6	5	4	3	2	1	0
	· ·	Туре	rw	rw	rw	rw	rw	rw	rw	rw
CEH	ADC_EVINFR Reset: 00 _H	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	(ט	EVINF 1	EVINF 0
	Event Interrupt Flag Register	Tuna	rh	rh	rh	rh	_		rh	rh
05	ADO EVINOR Deserti 00	Type					r 0			
CF _H	ADC_EVINCR Reset: 00 _H Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	U		EVINC 1	EVINC 0
	Event interrupt oreal ring register	Туре	w	W	w	W		r	w	w
D2 _H	ADC_EVINSR Reset: 00 _H	Bit Field	EVINS	EVINS	EVINS	EVINS)	EVINS	EVINS
DZH	Event Interrupt Set Flag Register	DIL FIEIU	7	6	5	4	,	,	1	0
		Туре	w	w	w	w		r	w	w
D3 _H	ADC EVINPR Reset: 00 _H	Bit Field	EVINP	EVINP	EVINP	EVINP)	EVINP	EVINP
DJH	Event Interrupt Node Pointer Register	Dit i icia	7	6	5	4	`	,	1	0
		Туре	rw	rw	rw	rw		r	rw	rw
RMAP =	0, Page 6		1							
CA _H	ADC_CRCR1 Reset: 00 _H	Bit Field	CH7	CH6	CH5	CH4				
- 11	Conversion Request Control Register 1									
		Туре	rwh	rwh	rwh	rwh				
СВн	ADC_CRPR1 Reset: 00 _H	Bit Field	CHP7	CHP6	CHP5	CHP4	r 0			
	Conversion Request Pending									
	Register 1	Туре	rwh	rwh	rwh	rwh			r	
CCH	ADC_CRMR1 Reset: 00 _H	Bit Field	Rsv	LDEV	CLR	SCAN	ENSI	ENTR	EN	GT
	Conversion Request Mode Register 1				PND					
		Type	r	W	W	rw	rw	rw		W
CD _H	ADC_QMR0 Reset: 00 _H	Bit Field	CEV	TREV	FLUSH	CLRV	TRMD	ENTR	EN	GT
	Queue Mode Register 0	Туре	W	W	W	W	rw	rw	r	W
CE _H	ADC_QSR0 Reset: 20 _H	Bit Field	Rsv	0	EMPTY	EV		()	
	Queue Status Register 0	Туре	r	r	rh	rh		r		
CF _H	ADC_Q0R0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHN	R
	Queue 0 Register 0	Туре	rh	rh	rh	rh	r		rh	
D2 _H	ADC_QBUR0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHN	R
••	Queue Backup Register 0	Туре	rh	rh	rh	rh	r		rh	
D2 _H	ADC_QINR0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF)	REQCHNR		
	Queue Input Register 0	Туре	w	w	W		r		w	

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 Timer 2 Register Overview

Addr	Register Name		Bit	7	6	5	4	3	2	1	0
C0H	T2_T2CON Timer 2 Control Register	Reset: 00 _H	Bit Field	TF2	EXF2	(0	EXEN2	TR2	0	CP/ RL2
			Туре	rwh	rwh		r	rw	rwh	r	rw



Table 12 Timer 2 Register Overview (cont'd)

C1 _H	T2_T2MOD Timer 2 Mode Register	Reset: 00 _H	Bit Field	T2 REGS	T2 RHEN	EDGE SEL	PREN	T2PRE	DCEN			
			Туре	rw	rw	rw	rw	rw	rw			
C2 _H	T2_RC2L	Reset: 00 _H	Bit Field	RC2[7:0]								
	Timer 2 Reload/Capture	Туре	rwh									
C3 _H	T2_RC2H Reset: 00 _H		Bit Field	RC2[15:8]								
	Timer 2 Reload/Capture	Register High	Туре				rv	/h				
C4 _H	T2_T2L	Reset: 00 _H	Bit Field				THL	2[7:0]				
	Timer 2 Register Low		Туре				rv	/h				
C5 _H	T2_T2H	Reset: 00 _H	Bit Field				THL2	[15:8]				
	Timer 2 Register High		Туре	rwh								

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 13 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP =	0				I	I			I	I	
A3 _H	CCU6_PAGE Reset: 00 _H	Bit Field	C)P	ST	NR	0		PAGE		
	Page Register for CCU6	Туре	١	N	١	v	r		rwh		
RMAP =	0, Page 0	•									
9A _H	CCU6_CC63SRL Reset: 00 _H Capture/Compare Shadow Register for Channel CC63 Low						3SL				
		Туре	rw								
9B _H	CCU6_CC63SRH Reset: 00 _H Capture/Compare Shadow Register for Channel CC63 High		CC63SH								
	· ·	Туре					w				
9C _H	CCU6_TCTR4L Reset: 00 _H Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	()	DTRES	T12 RES	T12RS	T12RR	
		Туре	W	W		r	W	W	W	W	
9D _H	CCU6_TCTR4H Reset: 00 _H Timer Control Register 4 High	Bit Field	T13 STD	T13 STR	0			T13 RES	T13RS	T13RR	
		Type	w	w	r			w	w	w	
9E _H	CCU6_MCMOUTSL Reset: 00 _H Multi-Channel Mode Output Shadow	Bit Field	STRM CM	0	MCMPS						
	Register Low	Туре	W	r	rw						
9F _H	CCU6_MCMOUTSH Reset: 00 _H	Bit Field	STRHP	0	CURHS				EXPHS		
	Multi-Channel Mode Output Shadow Register High	Туре	w	r	rw rw			rw			
A4 _H	CCU6_ISRL Reset: 00 _H Capture/Compare Interrupt Status	Bit Field	RT12P M	RT12O M	RCC62 F	RCC62 R	RCC61 F	RCC61 R	RCC60 F	RCC60 R	
	Reset Register Low	Туре	w	w	w	w	w	w	w	w	
A5 _H	CCU6_ISRH Reset: 00 _H Capture/Compare Interrupt Status	Bit Field	RSTR	RIDLE	RWHE	RCHE	0	RTRPF	RT13 PM	RT13 CM	
	Reset Register High	Туре	w	w	w	w	r	w	w	w	
A6 _H	CCU6_CMPMODIFL Reset: 00 _H Compare State Modification Register	Bit Field	0	MCC63 S		0		MCC62 S	MCC61 S	MCC60 S	
	Low	Type	r	w		r		w	w	w	
A7 _H	CCU6_CMPMODIFH Reset: 00 _H Compare State Modification Register	Bit Field	0	MCC63 R		0		MCC62 R	MCC61 R	MCC60 R	
	High	Туре	r	w	r w w				w		
FA _H	Capture/Compare Shadow Register for					CC	60SL				
	Channel CC60 Low	Туре				rv	vh				



Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0						
FB _H	CCU6_CC60SRH Reset: 00 _H Capture/Compare Shadow Register for	Bit Field				CC6	iosh									
	Channel CC60 High	Туре				rv	vh									
FC _H	CCU6_CC61SRL Reset: 00 _H Capture/Compare Shadow Register for Channel CC61 Low	Bit Field					S1SL vh									
		Туре					• • • • • • • • • • • • • • • • • • • •									
FD _H	CCU6_CC61SRH Reset: 00 _H Capture/Compare Shadow Register for Channel CC61 High	Bit Field					i1SH									
	· ·	Туре					vh									
FE _H	CCU6_CC62SRL Reset: 00 _H Capture/Compare Shadow Register for Channel CC62 Low	Bit Field					S2SL									
		Type					vh									
FF _H	CCU6_CC62SRH Reset: 00 _H Capture/Compare Shadow Register for Channel CC62 High	Bit Field					i2SH									
DMAAD	· ·	Туре				rv	vh									
	0, Page 1	Dit Field				000	3VL									
9A _H	CCU6_CC63RL Reset: 00 _H Capture/Compare Register for Channel CC63 Low	Bit Field														
00		Type					h									
9B _H	CCU6_CC63RH Reset: 00 _H Capture/Compare Register for Channel CC63 High	Bit Field CC63VH														
	-	Туре					h -: "									
9C _H	CCU6_T12PRL Reset: 00 _H Timer T12 Period Register Low	Bit Field T12PVL Type rwh														
	•	Туре														
9D _H	CCU6_T12PRH Reset: 00 _H Timer T12 Period Register High	Bit Field					PVH									
	0 0	Type rwh														
9E _H	CCU6_T13PRL Reset: 00 _H Timer T13 Period Register Low	Bit Field T13PVL														
	· ·	Type rwh														
9F _H	CCU6_T13PRH Reset: 00 _H Timer T13 Period Register High	Bit Field T13PVH														
	o o	Туре					vh									
A4 _H	CCU6_T12DTCL Reset: 00 _H Dead-Time Control Register for Timer	Bit Field					ГМ									
	T12 Low	Туре	_				w									
A5 _H	CCU6_T12DTCH Reset: 00 _H Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0						
	<u> </u>	Туре	r	rh	rh	rh	r	rw	rw	rw						
A6 _H	CCU6_TCTR0L Reset: 00 _H Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE12	T12R	T12 PRE		T12CLK							
		Туре	rw	rh	rh	rh	rw		rw							
A7 _H	CCU6_TCTR0H Reset: 00 _H Timer Control Register 0 High	Bit Field	()	STE13	T13R	T13 PRE		T13CLK							
		Туре		r	rh	rh	rw		rw							
FA _H	CCU6_CC60RL Reset: 00 _H Capture/Compare Register for Channel	Bit Field					60VL									
	CC60 Low	Туре					h									
FB _H	CCU6_CC60RH Reset: 00 _H Capture/Compare Register for Channel	Bit Field					60VH									
	CC60 High	Туре					h									
FC _H	CCU6_CC61RL Reset: 00 _H Capture/Compare Register for Channel	Bit Field				CC6	S1VL									
	CC61 Low	Туре				r	h		Type rh							



Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	6 5 4 3 2 1 0				0	
FD _H	CCU6_CC61RH Reset: 00 _H	Bit Field	-				1VH			
, DH	Capture/Compare Register for Channel CC61 High									
		Туре					h			
FE _H	CCU6_CC62RL Reset: 00 _H Capture/Compare Register for Channel CC62 Low						S2VL			
		Type					h			
FF _H	CCU6_CC62RH Reset: 00 _H Capture/Compare Register for Channel CC62 High	Bit Field Type					i2VH			
PMAP =	: 0, Page 2	Туре	rh							
9A _H	CCU6_T12MSELL Reset: 00 _H	Bit Field		MSF	EL61			MSF	EL60	
57 tH	T12 Capture/Compare Mode Select Register Low	Туре	rw						w	
OR.	CCU6_T12MSELH Reset: 00 _H	Bit Field	DBYP	1	W HSYNC				EL62	
9B _H	T12 Capture/Compare Mode Select Register High									
00	* *	Туре	rw	ENT 10	rw	FNOO	FNICO		W	FNOO
9C _H	CCU6_IENL Reset: 00 _H Capture/Compare Interrupt Enable Register Low	Bit Field	ENT12 PM	ENT12 OM	ENCC 62F	ENCC 62R	ENCC 61F	ENCC 61R	ENCC 60F	ENCC 60R
	•	Туре	rw	rw	rw	rw	rw	rw	rw	rw
9D _H	CCU6_IENH Reset: 00 _H Capture/Compare Interrupt Enable Register High	Bit Field	ENSTR	EN IDLE	EN WHE	EN CHE	0	EN TRPF	ENT13 PM	ENT13 CM
	, , , , , , , , , , , , , , , , , , ,	Туре	rw	rw	rw rw INPCC62		r	r rw INPCC61		rw
9E _H	CCU6_INPL Reset: 40 _H Capture/Compare Interrupt Node	Bit Field						CC60		
	Pointer Register Low	Туре		w		w		w	r	
9F _H	CCU6_INPH Reset: 39 _H Capture/Compare Interrupt Node Pointer Register High	Bit Field		0 INPT13			PT12		ERR	
		Туре		r		w		W		W
A4 _H	CCU6_ISSL Reset: 00 _H Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12P M	ST12O M	F	R	F	SCC61 R	F	R
	•	Туре	W	w	W	w	W	W	W	W
A5 _H	CCU6_ISSH Reset: 00 _H Capture/Compare Interrupt Status Set	Bit Field	SSTR	SIDLE	SWHE			STRPF	ST13 PM	ST13 CM
	Register High	Туре	W	w	w	w	W	W	w	W
A6 _H	CCU6_PSLR Reset: 00 _H Passive State Level Register	Bit Field	PSL63	0				SL		
	-	Туре	rwh	r				vh		
A7 _H	CCU6_MCMCTR Reset: 00 _H Multi-Channel Mode Control Register	Bit Field		0		SYN	0		SWSEL	
Ε.Δ.	•	Type		r T10		W	r	<u> </u>	T42	T40
FA _H	CCU6_TCTR2L Reset: 00 _H Timer Control Register 2 Low	Bit Field	0		TED		T13TEC		T13 SSC	T12 SSC
		Туре	r		W		rw		rw	rw
FB _H	CCU6_TCTR2H Reset: 00 _H Timer Control Register 2 High	Bit Field) r			RSEL		RSEL
EC	CCU6_MODCTRL Reset: 00 _H	Type Bit Field	MC	0	r			W ODEN	r	w
FC _H	Modulation Control Register Low		MEN			T12MODEN				
ED.	COULD MODOTDI	Type	TW FOT40	r						
FD _H	CCU6_MODCTRH Reset: 00 _H Modulation Control Register High	Bit Field	ECT13 O	0						
		Туре	rw	rw r rw						
FE _H	CCU6_TRPCTRL Reset: 00 _H Trap Control Register Low	Bit Field					TRPM0 rw			
	Trap Contion Register Low	Type	<u> </u>		r		r rw rw			



Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
FF _H	CCU6_TRPCTRH Reset: 00 _H Trap Control Register High	Bit Field	TRPPE N	TRPEN 13			TRI	PEN				
		Туре	rw	rw	rw							
RMAP =	0, Page 3											
9A _H	CCU6_MCMOUTL Reset: 00 _H Multi-Channel Mode Output Register	Bit Field	0	R	MCMP							
	Low	Туре	r rh rh					h				
9B _H	CCU6_MCMOUTH Reset: 00 _H Multi-Channel Mode Output Register	Bit Field		0 C					EXPH			
	High	Type		r		rh			rh			
9C _H	CCU6_ISL Reset: 00 _H Capture/Compare Interrupt Status	Bit Field	T12PM	T12OM	ICC62F	ICC62 R	ICC61F	ICC61 R	ICC60F	ICC60 R		
	Register Low	Туре	rh	rh	rh	rh	rh	rh	rh	rh		
9D _H	CCU6_ISH Reset: 00 _H Capture/Compare Interrupt Status	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM		
	Register High	Туре	rh	rh	rh	rh	rh	rh	rh	rh		
9E _H	CCU6_PISEL0L Reset: 00 _H	Bit Field	ISTRP		ISCC62 ISC		C61	ISC	C60			
	Port Input Select Register 0 Low	Туре	r	w				N	n	N		
9F _H	CCU6_PISEL0H Reset: 00 _H Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2 ISP			OS1	ISP	OS0		
		Туре	rw rw rw					N	n	N		
A4 _H	CCU6_PISEL2 Reset: 00 _H	Bit Field			()			IST1	3HR		
	Port Input Select Register 2	Туре	r rw									
FA _H	CCU6_T12L Reset: 00 _H	Bit Field				T12	CVL					
	Timer T12 Counter Register Low	Туре				rv	vh					
FB _H	CCU6_T12H Reset: 00 _H	Bit Field				T12	CVH					
	Timer T12 Counter Register High	Туре				rv	vh					
FC _H	CCU6_T13L Reset: 00 _H	Bit Field				T13	CVL					
	Timer T13 Counter Register Low	Туре				rv	vh					
FD_H	CCU6_T13H Reset: 00 _H	Bit Field				T13	CVH					
	Timer T13 Counter Register High	Туре				rv	vh					
FE _H	CCU6_CMPSTATL Reset: 00 _H Compare State Register Low	Bit Field	0	CC63 ST	CCPO S2	CCPO S1	CCPO S0	CC62 ST	CC61 ST	CC60 ST		
		Туре	r	rh	rh	rh	rh	rh	rh	rh		
FF _H	CCU6_CMPSTATH Reset: 00 _H Compare State Register High	Bit Field	T13IM	COUT 63PS	COUT 62PS	CC62 PS	COUT 61PS	CC61 PS	COUT 60PS	CC60 PS		
		Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh		

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 SSC Register Overview

Addr	Register Name		Bit	7	6	5	4	3	2	1	0
RMAP =	0		•	,		,	,	,			,
A9 _H			Bit Field			0		CIS	SIS	MIS	
	Port Input Select Register	Туре			r		rw	rw	rw		
AA_H	SSC_CONL	Reset: 00 _H	Bit Field	LB	PO	PH	HB	BM			
	Control Register Low Programming Mode	Туре	rw	rw	rw	rw	rw				
	Operating Mode		Bit Field	0					BC		
			Туре			r			r	h	



Table 14 SSC Register Overview

AB _H	SSC_CONH Reset: 00 _H Control Register High	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN	
	Programming Mode	Туре	rw	rw	r	rw	rw	rw	rw	rw	
	Operating Mode	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE	
		Туре	rw	rw	r	rh	rwh	rwh	rwh	rwh	
AC _H	SSC_TBL Reset: 00 _H	Bit Field				TB_V	ALUE				
	Transmitter Buffer Register Low	Туре	rw								
AD_H	SSC_RBL Reset: 00 _H	Bit Field	RB_VALUE								
	Receiver Buffer Register Low	Туре				r	h				
AE _H	SSC_BRL Reset: 00 _H	Bit Field				BR_VAI	_UE[7:0]				
	Baudrate Timer Reload Register Low	Туре				n	W				
AF _H	SSC_BRH Reset: 00 _H	Bit Field				BR_VAL	UE[15:8]				
	Baudrate Timer Reload Register High	Туре				n	N				

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	1	I	1							
E9 _H	MMCR2 Reset: 0U _H Monitor Mode Control Register 2	Bit Field	EXBC_ P	EXBC	MBCO N_P	MBCO N	MMEP _P	MMEP	MMOD E	JENA
		Туре	W	rw	w	rwh	W	rwh	rh	rh
F1 _H	MMCR Reset: 00 _H Monitor Mode Control Register	Bit Field	MEXIT _P	MEXIT	MSTEP _P	MSTEP	MRAM S_P	MRAM S	TRF	RRF
		Туре	w	rwh	w	rw	W	rwh	rh	rh
F2 _H	MMSR Reset: 00 _H Monitor Mode Status Register	Bit Field	MBCA M	MBCIN	EXBF	SWBF	HWB3 F	HWB2 F	HWB1 F	HWB0 F
		Туре	rw	rh	rwh	rwh	rwh	rwh	rwh	rwh
F3 _H	MMBPCR Reset: 00 _H BreakPoints Control Register	Bit Field	SWBC	HW	B3C	HW	HWB2C		HWB0C	
		Туре	rw	r	rw n		W	rw	n	N
F4 _H	MMICR Reset: 00 _H Monitor Mode Interrupt Control Register	Bit Field	DVECT	DRETR	(Ö	MMUIE _P		RRIE_ P	RRIE
		Туре	rwh	rwh		r	W	rw	w	rw
F5 _H	MMDR Reset: 00 _H Monitor Mode Data Register	Bit Field				MN	IRR			
	Receive	Туре				r	h			
	Transmit	Bit Field				MN	ITR			
		Туре				١	v			
F6 _H	HWBPSR Reset: 00 _H Hardware Breakpoints Select Register	Bit Field		0		BPSEL _P				
		Туре		r		w		r	w	
F7 _H	HWBPDR Reset: 00 _H	Bit Field				HW	3Pxx			
	Hardware Breakpoints Data Register	Туре				r	N			



3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width¹⁾ of 32-byte for D-Flash and 32-byte for P-Flash
- · 1-sector minimum erase width
- · 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: 3 × t_{CCLK} = 112.5 ns²⁾
- Program time: 209440 / f_{SYS} = 2.6 ms³⁾
- Erase time: $8175360 / f_{SYS} = 102 \text{ ms}^{3)}$

Data Sheet 38 V1.2. 2007-10

P-Flash: 32-byte wordline can only be programmed once, i.e., one gate disturb allowed. D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

 $f_{\rm sys}$ = 80 MHz ± 7.5% ($f_{\rm CCLK}$ = 26.7 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

³⁾ $f_{\rm sys}$ = 80 MHz ± 7.5% is the only frequency range for Flash programming and erasing. $f_{\rm sysmin}$ is used for obtaining the worst case timing.



Table 16 shows the Flash data retention and endurance targets.

Table 16 Flash Data Retention and Endurance (Operating Conditions apply)

-	40	· · ·	,
Retention	Endurance ¹⁾	Size	Remarks
Program Flash			
20 years	1,000 cycles	up to 16 Kbytes ²⁾	for 16-Kbyte Variant
20 years	1,000 cycles	up to 8 Kbytes ²⁾	for 8-Kbyte Variant
20 years	1,000 cycles	up to 4 Kbytes ²⁾	for 4-Kbyte Variant
Data Flash			
20 years	1,000 cycles	4 Kbytes	
5 years	10,000 cycles	1 Kbyte	
2 years	70,000 cycles	512 bytes	
2 years	100,000 cycles	128 bytes	

One cycle refers to the programming of all wordlines in a sector and erasing of sector. The Flash endurance data specified in Table 16 is valid only if the following conditions are fulfilled:

3.3.1 Flash Bank Sectorization

The XC866 product family offers four Flash devices with either 8 Kbytes or 16 Kbytes of embedded Flash memory. These Flash memory sizes are made up of two or four 4-Kbyte Flash banks, respectively. Each Flash device consists of Program Flash (P-Flash) bank(s) and a single Data Flash (D-Flash) bank with different sectorization shown in **Figure 11**. Both types can be used for code and data storage. The label "Data" neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different Flash bank sectorizations. The XC866 ROM devices offer a single 4-Kbyte D-Flash bank.

⁻ the maximum number of erase cycles per Flash sector must not exceed 100,000 cycles.

⁻ the maximum number of erase cycles per Flash bank must not exceed 300,000 cycles.

⁻ the maximum number of program cycles per Flash bank must not exceed 2,500,000 cycles.

²⁾ If no Flash is used for data, the Program Flash size can be up to the maximum Flash size available in the device variant. Having more Data Flash will mean less Flash is available for Program Flash.



Sector 2: 128-byte	Sector 9: 128-byte
Sector 1: 128-byte	Sector 8: 128-byte
	Sector 7: 128-byte
	Sector 6: 128-byte
	Sector 5: 256-byte
	Sector 4: 256-byte
	Sector 3: 512-byte
Sector 0: 3.75-Kbyte	Sector 2: 512-byte
	Sector 1: 1-Kbyte
	Sector 0: 1-Kbyte
P-Flash	D-Flash

Figure 11 Flash Bank Sectorization

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.



3.3.2 Flash Programming Width

For the P-Flash banks, a programmed wordline (WL) must be erased before it can be reprogrammed as the Flash cells can only withstand one gate disturb. This means that the entire sector containing the WL must be erased since it is impossible to erase a single WL.

For the D-Flash bank, the same WL can be programmed twice before erasing is required as the Flash cells are able to withstand two gate disturbs. Hence, it is possible to program the same WL, for example, with 16 bytes of data in two times (see Figure 12).

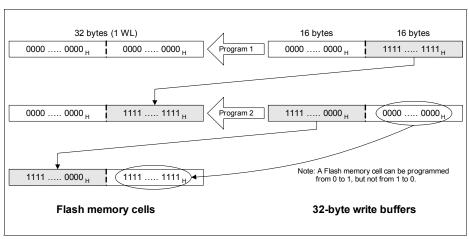


Figure 12 D-Flash Programming

Note: When programming a D-Flash WL the second time, the previously programmed Flash memory cells (whether 0s or 1s) should be reprogrammed with 0s to retain its original contents and to prevent "over-programming".



3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC866 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to Figure 17 give a general overview of the interrupt sources and illustrates the request and control flags.

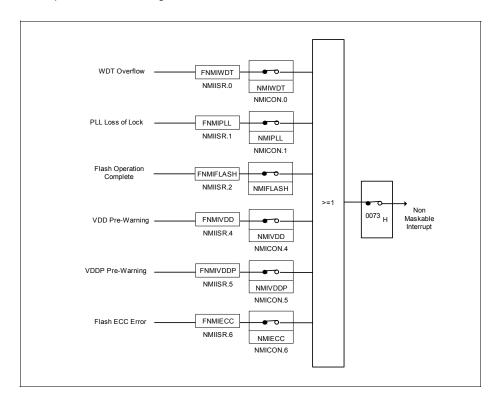


Figure 13 Non-Maskable Interrupt Request Sources



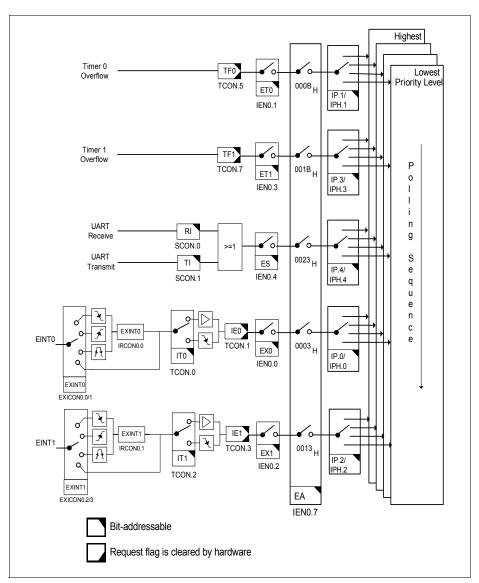


Figure 14 Interrupt Request Sources (Part 1)



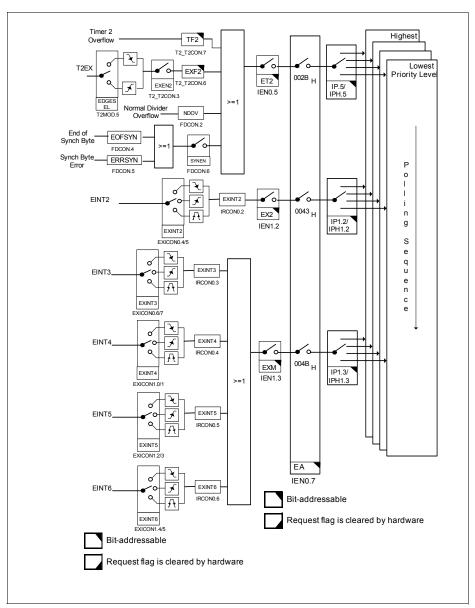


Figure 15 Interrupt Request Sources (Part 2)



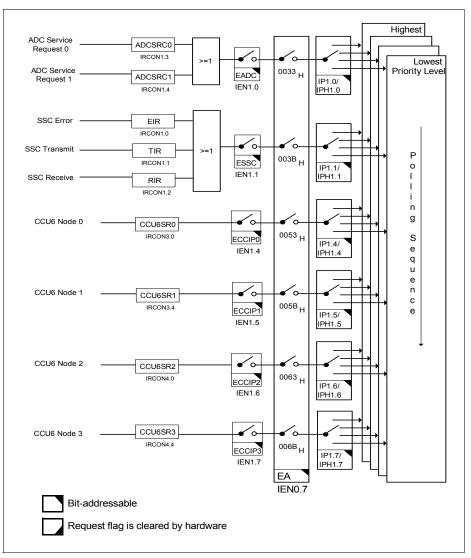


Figure 16 Interrupt Request Sources (Part 3)



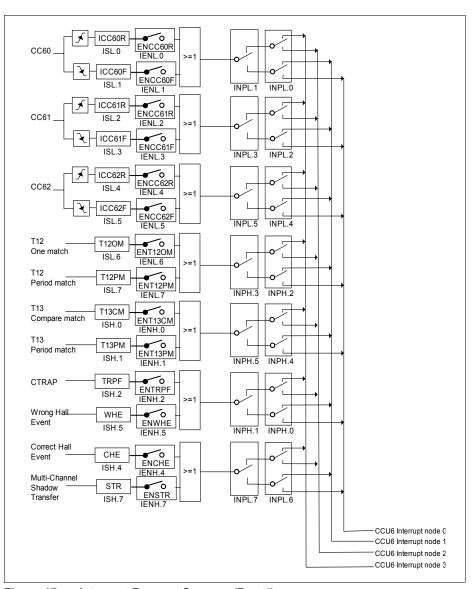


Figure 17 Interrupt Request Sources (Part 4)



3.4.2 Interrupt Source and Vector

Each interrupt source has an associated interrupt vector address. This vector is accessed to service the corresponding interrupt source request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC866 interrupt sources to the interrupt vector addresses and the corresponding interrupt source enable bits are summarized in **Table 17**.

Table 17 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC866	Enable Bit	SFR
NMI	0073 _H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 _H	External Interrupt 0	EX0	IEN0
XINTR1	000B _H	Timer 0	ET0	
XINTR2	0013 _H	External Interrupt 1	EX1	
XINTR3	001B _H	Timer 1	ET1	
XINTR4	0023 _H	UART	ES	
XINTR5	002B _H	T2	ET2	
		Fractional Divider (Normal Divider Overflow)		
		LIN		



Table 17 Interrupt Vector Addresses (cont'd)

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					
XINTR8	XINTR6	0033 _H	ADC	EADC	IEN1
XINTR9	XINTR7	003B _H	SSC	ESSC	
External Interrupt 4 External Interrupt 5 External Interrupt 6 XINTR10 0053 _H CCU6 INP0 ECCIP0 XINTR11 005B _H CCU6 INP1 ECCIP1 XINTR12 0063 _H CCU6 INP2 ECCIP2	XINTR8	0043 _H	External Interrupt 2	EX2	
External Interrupt 5 External Interrupt 6 XINTR10 0053 _H CCU6 INP0 ECCIP0 XINTR11 005B _H CCU6 INP1 ECCIP1 XINTR12 0063 _H CCU6 INP2 ECCIP2	XINTR9	004B _H	External Interrupt 3	EXM	
External Interrupt 6			External Interrupt 4		
XINTR10 0053 _H CCU6 INP0 ECCIP0 XINTR11 005B _H CCU6 INP1 ECCIP1 XINTR12 0063 _H CCU6 INP2 ECCIP2			External Interrupt 5		
XINTR11 005B _H CCU6 INP1 ECCIP1 XINTR12 0063 _H CCU6 INP2 ECCIP2			External Interrupt 6		
XINTR12 0063 _H CCU6 INP2 ECCIP2	XINTR10	0053 _H	CCU6 INP0	ECCIP0	
The state of the s	XINTR11	005B _H	CCU6 INP1	ECCIP1	
XINTR13 006B _H CCU6 INP3 ECCIP3	XINTR12	0063 _H	CCU6 INP2	ECCIP2	
	XINTR13	006B _H	CCU6 INP3	ECCIP3	



3.4.3 Interrupt Priority

Each interrupt source, except for NMI, can be individually programmed to one of the four possible priority levels. The NMI has the highest priority and supersedes all other interrupts. Two pairs of interrupt priority registers (IP and IPH, IP1 and IPH1) are available to program the priority level of each non-NMI interrupt vector.

A low-priority interrupt can be interrupted by a high-priority interrupt, but not by another interrupt of the same or lower priority. Further, an interrupt of the highest priority cannot be interrupted by any other interrupt source.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 18**.

Table 18 Priority Structure within Interrupt Level

,				
Level				
(highest)				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				



3.5 Parallel Ports

The XC866 has 27 port pins organized into four parallel ports, Port 0 (P0) to Port 3 (P3). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. Ports P0, P1 and P3 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. Port P2 is an input-only port, providing general purpose input functions, alternate input functions for the on-chip peripherals, and also analog inputs for the Analog-to-Digital Converter (ADC).

Bidirectional Port Features:

- · Configurable pin direction
- · Configurable pull-up/pull-down devices
- · Configurable open drain mode
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Input Port Features:

- · Configurable input driver
- Configurable pull-up/pull-down devices
- Receive of data through digital input (general purpose input)
- Alternate input for on-chip peripherals
- · Analog input for ADC module



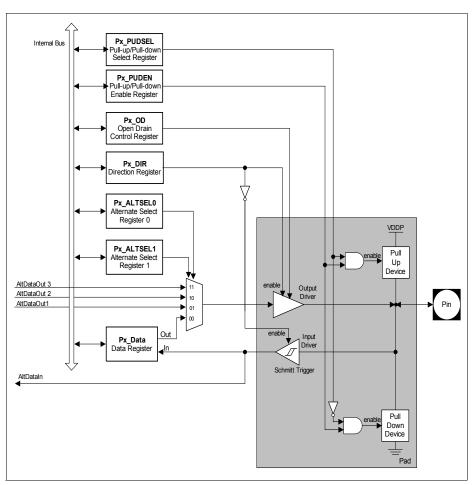


Figure 18 General Structure of Bidirectional Port



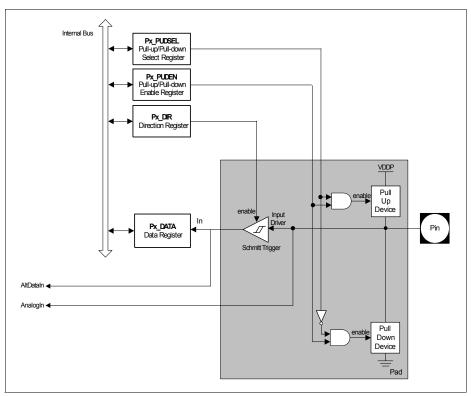


Figure 19 General Structure of Input Port



3.6 Power Supply System with Embedded Voltage Regulator

The XC866 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- · 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 20 shows the XC866 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

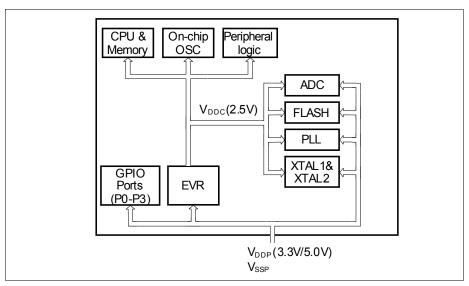


Figure 20 XC866 Power Supply System

EVR Features:

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage ($V_{\rm DDC}$): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection



3.7 Reset Control

The XC866 has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC866 is first powered up, the status of certain pins (see **Table 20**) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

In order to power up the system properly, the external reset pin RESET must be asserted until $V_{\rm DDC}$ reaches $0.9^*V_{\rm DDC}$. The delay of external reset can be realized by an external capacitor at $\overline{\rm RESET}$ pin. This capacitor value must be selected so that $V_{\rm RESET}$ reaches 0.4 V, but not before $V_{\rm DDC}$ reaches 0.9* $V_{\rm DDC}$

A typical application example is shown in Figure 21. V_{DDP} capacitor value is 300 nF. V_{DDC} capacitor value is 220 nF. The capacitor connected to \overline{RESET} pin is 100 nF.

Typically, the time taken for $V_{\rm DDC}$ to reach $0.9^*V_{\rm DDC}$ is less than 50 μs once $V_{\rm DDP}$ reaches 2.3V. Hence, based on the condition that 10% to 90% $V_{\rm DDP}$ (slew rate) is less than 500 μs , the RESET pin should be held low for 500 μs typically. See Figure 22.

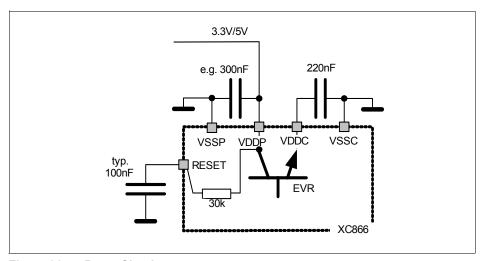


Figure 21 Reset Circuitry



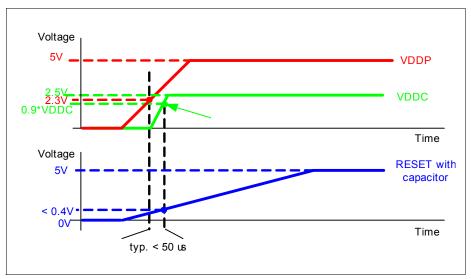


Figure 22 V_{DDP} , V_{DDC} and V_{RESET} during Power-on Reset

The second type of reset in XC866 is the hardware reset. This reset function can be used <u>during</u> normal operation or when the chip is in power-down mode. A reset input pin RESET is <u>provided</u> for the hardware reset. To ensure the recognition of the hardware reset, pin RESET must be held low for at least 100 ns.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.



3.7.1 Module Reset Behavior

Table 19 shows how the functions of the XC866 are affected by the various reset types. A "

" means that this function is reset to its default state.

Table 19 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core					
Peripherals	-				
On-Chip Static RAM	Not affected, reliable	Not affected, reliable	Not affected, reliable	Affected, un- reliable	Affected, un- reliable
Oscillator, PLL	-	Not affected			
Port Pins					
EVR	The voltage regulator is switched on	Not affected	•		
FLASH					
NMI	Disabled	Disabled			

3.7.2 Booting Scheme

When the XC866 is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. **Table 20** shows the available boot options in the XC866.

Table 20 XC866 Boot Selection

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	х	User Mode; on-chip OSC/PLL non-bypassed	0000 _H
0	0	х	BSL Mode; on-chip OSC/PLL non-bypassed	0000 _H
0	1	0	OCDS Mode ¹⁾ ; on-chip OSC/PLL non- bypassed	0000 _H
1	1	0	Standalone User (JTAG) Mode ²⁾ ; on-chip OSC/PLL non-bypassed (normal)	0000 _H

¹⁾ The OCDS mode is not accessible if Flash is protected.

²⁾ Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.



3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC866. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features:

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL.In the XC866, the oscillator can be from either of these two sources: the on-chip oscillator (10 MHz) or the external oscillator (4 MHz to 12 MHz). The term "oscillator" is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default. The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

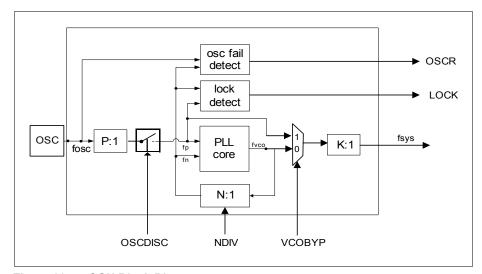


Figure 23 CGU Block Diagram



The clock system provides three ways to generate the system clock:

PLL Base Mode

The system clock is derived from the VCO base (free running) frequency clock divided by the K factor.

$$f_{SYS} = f_{VCObase} \times \frac{1}{K}$$

Prescaler Mode (VCO Bypass Operation)

In VCO bypass operation, the system clock is derived from the oscillator clock, divided by the P and K factors.

$$f_{SYS} = f_{OSC} \times \frac{1}{P \times K}$$

PLL Mode

The system clock is derived from the oscillator clock, multiplied by the N factor, and divided by the P and K factors. Both VCO bypass and PLL bypass must be inactive for this PLL mode. The PLL mode is used during normal system operation.

$$f_{SYS} = f_{OSC} \times \frac{N}{P \times K}$$

Table 3-1 shows the settings of bits OSCDISC and VCOBYP for different clock mode selection.

Table 3-1 Clock Mode Selection

OSCDISC	VCOBYP	Clock Working Modes
0	0	PLL Mode
0	1	Prescaler Mode
1	0	PLL Base Mode
1	1	PLL Base Mode

Note: When oscillator clock is disconnected from PLL, the clock mode is PLL Base mode regardless of the setting of VCOBYP bit.

System Frequency Selection

For the XC866, the values of P and K are fixed to "1" and "2", respectively. In order to obtain the required system frequency, f_{sys} , the value of N can be selected by bit NDIV for different oscillator inputs. Table 21 provides examples on how f_{sys} = 80 MHz can be obtained for the different oscillator sources.



Table 21 System frequency (f_{svs} = 80 MHz)

Oscillator	fosc	N	Р	K	fsys
On-chip	10 MHz	16	1	2	80 MHz
External	10 MHz	16	1	2	80 MHz
	8 MHz	20	1	2	80 MHz
	5 MHz	32	1	2	80 MHz

Table 22 shows the VCO range for the XC866.

Table 22 VCO Range

f _{VCOmin}	f _{VCOmax}	f _{VCOFREEmin}	f _{VCOFREEmax}	Unit
150	200	20	80	MHz
100	150	10	80	MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 12 MHz. Additionally, it is necessary to have two load capacitances $C_{\rm X1}$ and $C_{\rm X2}$, and depending on the crystal type, a series resistor $R_{\rm X2}$, to limit the current. A test resistor $R_{\rm Q}$ may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. $R_{\rm Q}$ values are typically specified by the crystal vendor. The $C_{\rm X1}$ and $C_{\rm X2}$ values shown in **Figure 24** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor.

Figure 24 shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.



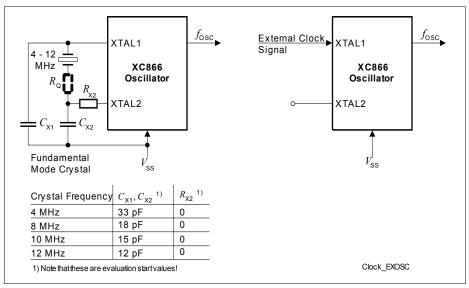


Figure 24 External Oscillator Circuitries

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.



3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 26.7 MHz
- CCU6 clock: FCLK = 26.7 MHz
- Other peripherals: PCLK = 26.7 MHz
- Flash Interface clock: CCLK3 = 80 MHz and CCLK = 26.7 MHz

In addition, different clock frequency can output to pin CLKOUT(P0.0). The clock output frequency can further be divided by 2 using toggle latch (bit TLEN is set to 1), the resulting output frequency has 50% duty cycle. **Figure 25** shows the clock distribution of the XC866.

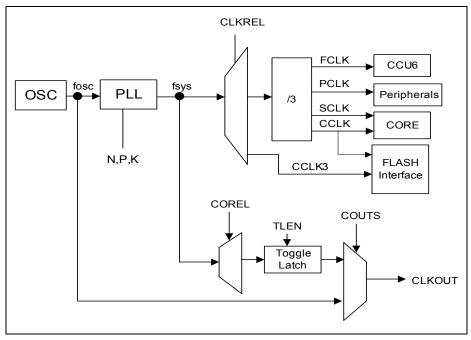


Figure 25 Clock Generation from f_{sys}



For power saving purposes, the clocks may be disabled or slowed down according to **Table 23**.

Table 23 System frequency (f_{sys} = 80 MHz)

Power Saving Mode	Action
Idle	Clock to the CPU is disabled.
Slow-down	Clocks to the CPU and all the peripherals, including CCU6, are divided by a common programmable factor defined by bit field CMCON.CLKREL.
Power-down	Oscillator and PLL are switched off.



3.9 Power Saving Modes

The power saving modes of the XC866 provide flexible power consumption through a combination of techniques, including:

- · Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see Figure 26) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- · Idle mode
- · Slow-down mode
- · Power-down mode

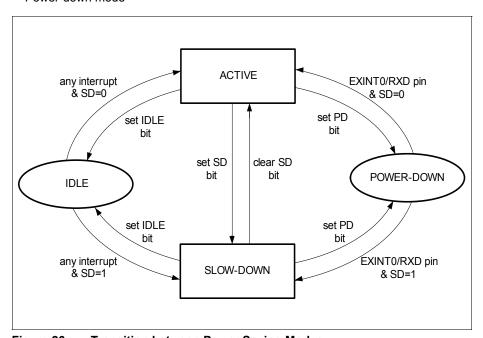


Figure 26 Transition between Power Saving Modes



3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC866 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC866 will be aborted in a user-specified time period. In debug mode, the WDT is suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features:

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of f_{PCLK}/2 or f_{PCLK}/128
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 27** shows the block diagram of the WDT unit.

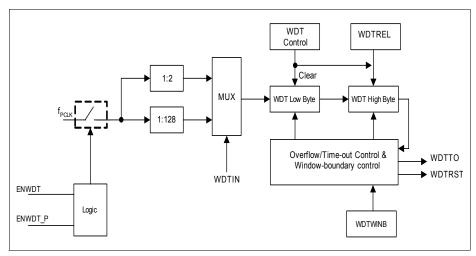


Figure 27 WDT Block Diagram



If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for $30_{\rm H}$ count, after which the system is reset (assert WDTRST).

The WDT has a "programmable window boundary" which disallows any refresh during the WDT's count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_{\rm H}$ to the value obtained from the concatenation of WDTWINB and $00_{\rm H}$.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2⁸). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either f_{PCLK}/2 or f_{PCLK}/128
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT} , between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1+WDTIN\times6)} \times (2^{16} - WDTREL \times 2^{8})}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 28**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

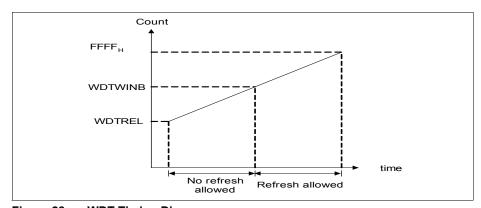


Figure 28 WDT Timing Diagram



Table 24 lists the possible watchdog time range that can be achieved for different module clock frequencies . Some numbers are rounded to 3 significant digits.

Table 24 Watchdog Time Ranges

Reload value	Prescaler for f _{PCLK}			
in WDTREL	2 (WDTIN = 0)	128 (WDTIN = 1)		
	26.7 MHz	26.7 MHz		
FF _H	19.2 μs	1.23 ms		
7F _H	2.48 ms	159 ms		
00 _H	4.92 ms	315 ms		



3.11 Universal Asynchronous Receiver/Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features:

- · Full-duplex asynchronous modes
 - 8-bit or 9-bit data frames, LSB first
 - fixed or variable baud rate
- · Receive buffered
- · Multiprocessor communication
- · Interrupt generation on the completion of a data transmission or reception

The UART can operate in the four modes as shown in **Table 25**. Data is transmitted on TXD and received on RXD.

Table 25 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	f _{PCLK} /2
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	f _{PCLK} /32 or f _{PCLK} /64
Mode 3: 9-bit shift UART	Variable

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. The variable baud rate is set by either the underflow rate on the dedicated baud-rate generator, or by the overflow rate on Timer 1.



3.11.1 Baud-Rate Generator

The baud-rate generator is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 29**.

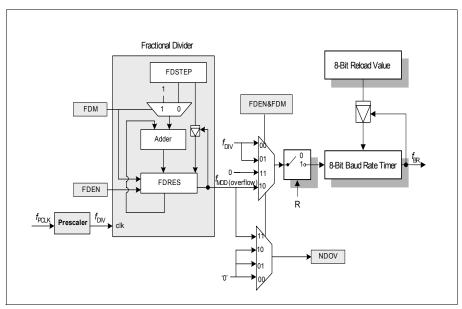


Figure 29 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.12**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP (to be considered only if fractional divider is enabled and operating in fractional divider mode)



• 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG The following formulas calculate the final baud rate without and with the fractional divider respectively:

baud rate =
$$\frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR \ VALUE + 1)}$$
 where $2^{BRPRE} \times (BR \ VALUE + 1) > 1$

$$\text{baud rate } = \frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR_VALUE + 1)} \times \frac{STEP}{256}$$

The maximum baud rate that can be generated is limited to f_{PCLK}/32. Hence, for a module clock of 26.7 MHz, the maximum achievable baud rate is 0.83 MBaud.

Standard LIN protocal can support a maximum baud rate of 20kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20kHz to 115.2kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

Table 26 lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 26.7 MHz is used.

Table 26 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2 ^{BRPRE})	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000 _B)	87 (57 _H)	-0.22 %
9600 Baud	1 (BRPRE=000 _B)	174 (AE _H)	-0.22 %
4800 Baud	2 (BRPRE=001 _B)	174 (AE _H)	-0.22 %
2400 Baud	4 (BRPRE=010 _B)	174 (AE _H)	-0.22 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. Table 27 lists the resulting deviation errors from generating a baud rate of



115.2 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

Table 27 Deviation Error for UART with Fractional Divider enabled

f _{PCLK}	Prescaling Factor (2 ^{BRPRE})	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
26.67 MHz	1	10 (A _H)	177 (B1 _H)	+0.03 %
13.33 MHz	1	7 (7 _H)	248 (F8 _H)	+0.11 %
6.67 MHz	1	3 (3 _H)	212 (D4 _H)	-0.16 %



3.11.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 band rate=
$$\frac{2^{\text{SMOD}} \times f_{\text{PCLK}}}{32 \times 2 \times (256 - \text{TH1})}$$
 [3.1]

3.12 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 29**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV} , where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

$$f_{\text{MOD}} = f_{\text{DIV}} \times \frac{1}{256 - \text{STEP}}$$
 [3.2]



3.13 LIN Protocol

The UART can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in Figure 30. The frame consists of the:

- header, which comprises a Break (13-bit time low), Synch Byte (55_H), and ID field
- · response time
- data bytes (according to UART protocol)
- · checksum

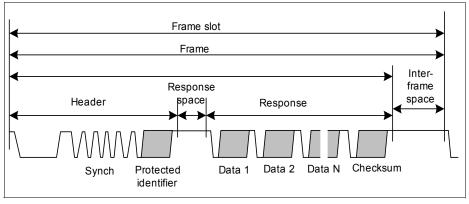


Figure 30 Structure of LIN Frame

3.13.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data.



The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

STEP 4: Enter for Master Request Frame or for Slave Response Frame

Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.



3.14 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features:

- · Master and slave mode operation
 - Full-duplex or half-duplex operation
- Transmit and receive buffered
- · Flexible data format
 - Programmable number of data bits: 2 to 8 bits
 - Programmable shift direction: LSB or MSB shift first
 - Programmable clock polarity: idle low or high state for the shift clock
 - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- · Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- · Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)



Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 31 shows the block diagram of the SSC.

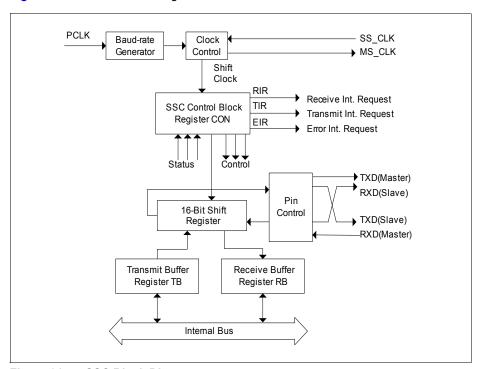


Figure 31 SSC Block Diagram



3.15 Timer 0 and Timer 1

Timers 0 and 1 are count-up timers which are incremented every machine cycle, or in terms of the input clock, every 2 PCLK cycles. They are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 28**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 28 Timer 0 and Timer 1 Modes

Mode	Operation
0	13-bit timer The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	16-bit timer The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	8-bit timer with auto-reload The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	Timer 0 operates as two 8-bit timers The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.



3.16 Timer 2

Timer 2 is a 16-bit general purpose timer (THL2) that has two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode. If the prescalar is disabled, Timer 2 counts with an input clock of PCLK/12. Timer 2 continues counting as long as it is enabled.

Table 29	Timer 2 Modes
Mode	Description
Auto-reload	Up/Down Count Disabled Count up only Start counting from 16-bit reload value, overflow at FFFFH Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well Programmble reload value in register RC2 Interrupt is generated with reload event
	 Up/Down Count Enabled Count up or down, direction determined by level at input pin T2EX No interrupt is generated Count up Start counting from 16-bit reload value, overflow at FFFFH Reload event triggered by overflow condition Programmble reload value in register RC2 Count down Start counting from FFFFH, underflow at value defined in register RC2 Reload event triggered by underflow condition Reload value fixed at FFFFH
Channel capture	 Count up only Start counting from 0000_H, overflow at FFFF_H Reload event triggered by overflow condition Reload value fixed at 0000_H Capture event triggered by falling/rising edge at pin T2EX Captured timer value stored in register RC2 Interrupt is generated with reload or capture event



3.17 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Timer T12 Features:

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- · Generation of center-aligned and edge-aligned PWM
- · Supports single-shot mode
- · Supports many interrupt request sources
- Hysteresis-like control mode

Timer T13 Features:

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- · Supports single-shot mode

Additional Features:

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- · Control modes for multi-channel AC-drives
- · Output levels can be selected and adapted to the power stage



The block diagram of the CCU6 module is shown in Figure 32.

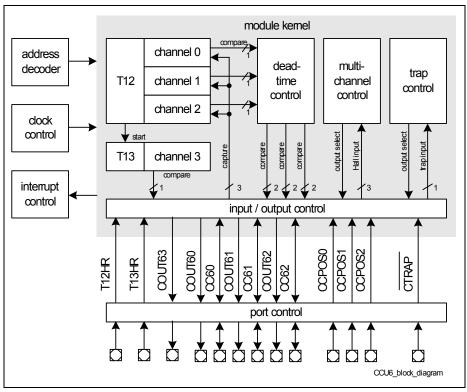


Figure 32 CCU6 Block Diagram



3.18 Analog-to-Digital Converter

The XC866 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features:

- Successive approximation
- 8-bit or 10-bit resolution (TUE of ± 1 LSB and ± 2 LSB, respectively)
- · Eight analog channels
- · Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- · Single conversion mode
- · Autoscan functionality
- · Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- · Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- · Flexible interrupt generation with configurable service nodes
- · Programmable sample time
- · Programmable clock divider
- · Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes



3.18.1 ADC Clocking Scheme

A common module clock $f_{\mbox{\scriptsize ADC}}$ generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length
 and the sample time). This clock is generated internally in the analog part, based on
 the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- · f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

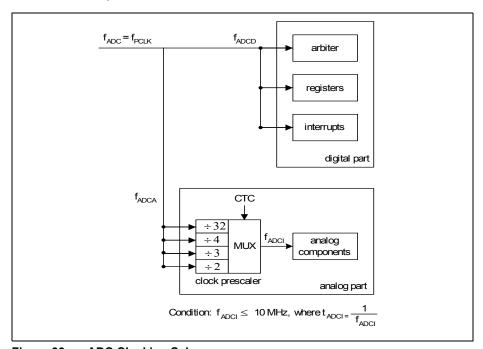


Figure 33 ADC Clocking Scheme



For module clock f_{ADC} = 26.7 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 30**.

Table 30 f_{ADCI} Frequency Selection

Module Clock f _{ADC}	СТС	Prescaling Ratio	Analog Clock f _{ADCI}
26.7 MHz	00 _B	÷ 2	13.3 MHz (N.A)
	01 _B	÷ 3	8.9 MHz
	10 _B	÷ 4	6.7 MHz
	11 _B (default)	÷ 32	833.3 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 26.7 MHz. During slow-down mode where f_{ADC} may be reduced to 13.3 MHz, 6.7 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.18.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- · Conversion phase
- Write result phase (t_{WR})

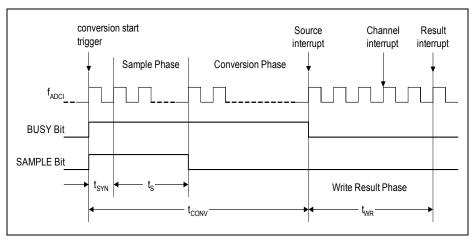


Figure 34 ADC Conversion Timing



3.19 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- use the built-in debug functionality of the XC800 Core
- · add a minimum of hardware overhead
- provide support for most of the operations by a Monitor Program
- use standard interfaces to communicate with the Host (a Debugger)

Features:

- · Set breakpoints on instruction address and within a specified address range
- · Set breakpoints on internal RAM address
- Support unlimited software breakpoints in Flash/RAM code region
- · Process external breaks
- · Step through the program code

The OCDS functional blocks are shown in **Figure 35**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals. After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack). The OCDS system is accessed through the JTAG¹⁾, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC866 has been started in OCDS mode.

¹⁾ The pins of the JTAG port can be assigned to either Port 0 (primary) or Ports 1 and 2 (secondary). User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.



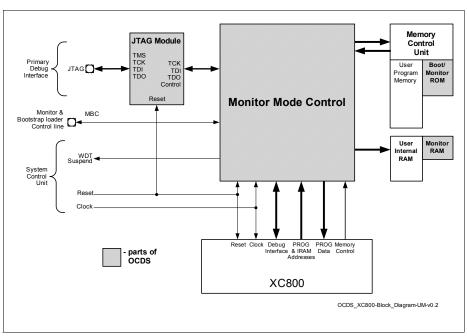


Figure 35 OCDS Block Diagram

3.19.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode $04_{\rm H}$), and the same is also true immediately after reset.

The JTAG ID register contents for the XC866 devices are given in Table 31.

Table 31 JTAG ID Summary

Device Type	Device Name	JTAG ID	
Flash	XC866L-4FR	1010 0083 _H	
	XC866-4FR	100F 5083 _H	
	XC866L-2FR	1010 2083 _H	
	XC866-2FR	1010 1083 _H	
	XC866L-1FR	1013 8083 _H	
	XC866-1FR	1013 8083 _H	



Table 31	JTAG ID Summary
----------	-----------------

	•	
ROM	XC866L-4RR	1013 9083 _H
	XC866-4RR	1013 9083 _H
	XC866L-2RR	1013 9083 _H
	XC866-2RR	1013 9083 _H

3.20 **Identification Register**

The XC866 identity register is located at Page 1 of address B3_H.

ID **Identity Register**

Reset Value: 0000 0010_B

1	б	5	4	3	2	1	U
	T	PRODID	П	П		VERID	
	Ì	I.	i.	i.		İ	İ
		r				r	

Field	Bits	Type	Description
VERID	[2:0]	r	Version ID 010 _B
PRODID	[7:3]	r	Product ID 00000 _B



4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC866.

Note: The electrical parameters are valid for the XC866-4FR and XC866-2FR. The electrical parameters for the ROM variants and XC866-1FR are preliminary, differences from XC866-4FR and XC866-2FR are stated explicitly.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC866 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

· cc

These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC866 and must be regarded for a system design.

• SR

These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC866 is designed in.



4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC866 can be subjected to without permanent damage.

Table 32 Absolute Maximum Rating Parameters

Parameter	Symbol	Lim	Limit Values		Notes
		min.	max.		
Ambient temperature	T_{A}	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	
Junction temperature	T_{J}	-40	150	°C	under bias
$\begin{tabular}{ll} \hline \begin{tabular}{ll} Voltage on power supply pin with respect to $V_{\rm SS}$ \\ \hline \end{tabular}$	V_{DDP}	-0.5	6	V	
Voltage on core supply pin with respect to $V_{\rm SS}$	V_{DDC}	-0.5	3.25	V	
Voltage on any pin with respect to $V_{\rm SS}$	V_{IN}	-0.5	V _{DDP} + 0.5 or max. 6	V	Whatever is lower
Input current on any pin during overload condition	I_{IN}	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	_	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions $(V_{IN} > V_{DDP})$ or $V_{IN} < V_{SS}$ the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.



4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC866. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 33 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/	
	min.		in. max.		Conditions	
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device	
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device	
Digital ground voltage	V_{SS}		0	V		
Digital core supply voltage	V_{DDC}	2.3	2.7	V		
System Clock Frequency ¹⁾	$f_{\sf SYS}$	74	86	MHz		
Ambient temperature	T_{A}	-40	85	°C	SAF-XC866	
		-40	125	°C	SAK-XC866	

¹⁾ $f_{\rm SYS}$ is the PLL output clock. During normal operating mode, CPU clock is $f_{\rm SYS}$ / 3. Please refer to Figure 25 for detailed description.



4.2 DC Parameters

4.2.1 Input/Output Characteristics

Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit	Values	Unit	Test Conditions
		min.	max.		Remarks
V_{DDP} = 5V Range					
Output low voltage	V_{OL} CC	_	1.0	V	I _{OL} = 15 mA
		_	0.4	V	$I_{\rm OL}$ = 5 mA
Output high voltage	V _{OH} CC	V _{DDP} - 1.0	_	٧	I _{OH} = -15 mA
		V _{DDP} - 0.4	_	V	I _{OH} = -5 mA
Input low voltage on port pins (all except P0.0 & P0.1)	V_{ILP} SR	_	$0.3 \times V_{\text{DDP}}$	V	CMOS Mode
Input low voltage on P0.0 & P0.1	V_{ILP0} SR	-0.2	$0.3 \times V_{DDP}$	V	CMOS Mode
Input low voltage on RESET pin	V_{ILR} SR	_	$0.3 \times V_{DDP}$	٧	CMOS Mode
Input low voltage on TMS pin	V_{ILT} SR	_	$0.3 \times V_{DDP}$	V	CMOS Mode
Input high voltage on port pins (all except P0.0 & P0.1)	V _{IHP} SR	V_{DDP}	-	V	CMOS Mode
Input high voltage on P0.0 & P0.1	$V_{IHP0}SR$	$0.7 \times V_{DDP}$	V_{DDP}	V	CMOS Mode
Input high voltage on RESET pin	V_{IHR} SR	$0.7 \times V_{DDP}$	_	V	CMOS Mode
Input high voltage on TMS pin	V_{IHT} SR	$0.75 \times V_{DDP}$	_	V	CMOS Mode
Input Hysteresis ¹⁾ on Port pins	HYS CC	$0.08 \times V_{\mathrm{DDP}}$	_	V	CMOS Mode
Input Hysteresis ¹⁾ on XTAL1	HYSXCC	$V_{ m DDC}$	_	V	



Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Syml	ool	Limit	Values	Unit	Test Conditions
			min.	max.		Remarks
Input low voltage at XTAL1	V_{ILX}	SR	V _{SS} - 0.5	$0.3 \times V_{ m DDC}$	V	
Input high voltage at XTAL1	V_{IHX}	SR	$V_{ m DDC}$	V _{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	_	-10	μΑ	$V_{IH,min}$
			-150	_	μΑ	$V_{IL,max}$
Pull-down current	I_{PD}	SR	_	10	μΑ	$V_{IL,max}$
			150	_	μΑ	$V_{IH,min}$
Input leakage current ²⁾	I _{OZ1}	CC	-1	1	μA	0 < $V_{\rm IN}$ < $V_{\rm DDP}$, $T_{\rm A} \le$ 125°C , XC866-4FR and XC866-2FR
			-2.5	1	μΑ	0 < $V_{\rm IN}$ < $V_{\rm DDP}$, $T_{\rm A} \le$ 125°C, XC866-1FR and ROM device
Input current at XTAL1	I_{ILX}	CC	-10	10	μΑ	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	ΣI_{OV}	 SR	_	25	mA	3)
Voltage on any pin during $V_{\rm DDP}$ power off	V_{PO}	SR	_	0.3	V	4)
$\label{eq:maximum} $	I_{M}	SR	_	15	mA	
$\label{eq:maximum} \begin{array}{l} \mbox{Maximum current for all} \\ \mbox{pins (excluding } V_{\mbox{DDP}} \\ \mbox{and } V_{\mbox{SS}}) \end{array}$	$\Sigma I_{M} $	SR	_	60	mA	
$\begin{array}{c} {\rm Maximum~current~into} \\ V_{\rm DDP} \end{array}$	I_{MVDI}	OP SR	_	80	mA	
$\begin{tabular}{ll} \hline \textbf{Maximum current out of} \\ V_{\rm SS} \\ \hline \end{tabular}$	I _{MVS}	SR	_	80	mA	



Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit	Values	Unit	Test Conditions
		min.	max.		Remarks
V _{DDP} = 3.3V Range					
Output low voltage	V_{OL} CC	_	1.0	V	I _{OL} = 8 mA
		_	0.4	V	$I_{\rm OL}$ = 2.5 mA
Output high voltage	V _{OH} CC	V _{DDP} - 1.0	_	V	I_{OH} = -8 mA
		V _{DDP} - 0.4	_	V	I _{OH} = -2.5 mA
Input low voltage on port pins (all except P0.0 & P0.1)	V_{ILP} SR	_	$0.3 \times V_{\mathrm{DDP}}$	V	CMOS Mode
Input low voltage on P0.0 & P0.1	V_{ILP0} SR	-0.2	$0.3 \times V_{DDP}$	V	CMOS Mode
Input low voltage on RESET pin	V_{ILR} SR	_	$0.3 \times V_{DDP}$	V	CMOS Mode
Input low voltage on TMS pin	V_{ILT} SR	_	$0.3 \times V_{DDP}$	V	CMOS Mode
Input high voltage on port pins (all except P0.0 & P0.1)	V_{IHP} SR	V_{DDP}	_	V	CMOS Mode
Input high voltage on P0.0 & P0.1	$V_{IHP0}SR$	V_{DDP}	V_{DDP}	V	CMOS Mode
Input high voltage on RESET pin	V_{IHR} SR	V_{DDP}	_	V	CMOS Mode
Input high voltage on TMS pin	V_{IHT} SR	$0.75 \times V_{\mathrm{DDP}}$	_	V	CMOS Mode
Input Hysteresis ¹⁾ on Port pins	HYS CC	$V_{\rm DDP}$	_	V	CMOS Mode
Input Hysteresis ¹⁾ on XTAL1	HYSXCC	$V_{ m DDC}$	_	V	
Input low voltage at XTAL1	V_{ILX} SR	V _{SS} - 0.5	$V_{ m DDC}$	V	
Input high voltage at XTAL1	V_{IHX} SR	V_{DDC}	<i>V</i> _{DDC} + 0.5	V	



Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Syml	ool	Limit	Values	Unit		
			min.	max.		Remarks	
Pull-up current	I_{PU}	SR	_	-5	μΑ	$V_{IH,min}$	
			-50	_	μΑ	$V_{IL,max}$	
Pull-down current	I_{PD}	SR	_	5	μΑ	$V_{IL,max}$	
			50	_	μΑ	$V_{IH,min}$	
Input leakage current ²⁾	I _{OZ1}	CC	-1	1	μA	0 < $V_{\rm IN}$ < $V_{\rm DDP}$, $T_{\rm A} \le$ 125°C , XC866-4FR and XC866-2FR	
			-2.5	1	μA	0 < $V_{\rm IN}$ < $V_{\rm DDP}$, $T_{\rm A} \le$ 125°C, XC866-1FR and ROM device	
Input current at XTAL1	I_{ILX}	CC	- 10	10	μΑ		
Overload current on any pin	I_{OV}	SR	-5	5	mA		
Absolute sum of overload currents	$\Sigma I_{\sf OV}$	 SR	_	25	mA	3)	
Voltage on any pin during $V_{\rm DDP}$ power off	V_{PO}	SR	_	0.3	V	4)	
	I_{M}	SR	_	15	mA		
$\begin{array}{l} \text{Maximum current for all} \\ \text{pins (excluding } V_{\text{DDP}} \\ \text{and } V_{\text{SS}}) \end{array}$	$\Sigma I_{M} $	SR	_	60	mA		
	I_{MVDI}	OP SR	_	80	mA		
$\overline{ \begin{array}{c} \text{Maximum current out of} \\ V_{\text{SS}} \end{array} }$	I _{MVS}	SR	_	80	mA		

Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

²⁾ An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and RESET pin have internal pull devices and are not included in the input leakage current characteristic.

³⁾ Not subjected to production test, verified by design/characterization.



4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when VDDP is powered off.



4.2.2 Supply Threshold Characteristics

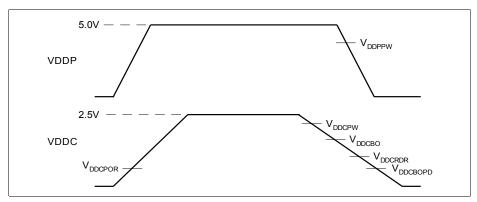


Figure 36 Supply Threshold Parameters

Table 35 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol	Symbol		nit Val	ues	Unit	Remarks
			min.	typ.	max.		
$V_{\rm DDC}$ prewarning voltage ¹⁾	$V_{\rm DDCPW}$	CC	2.2	2.3	2.4	V	
$V_{\rm DDC}$ brownout voltage in active mode ¹⁾	$V_{\rm DDCBO}$	CC	2.0	2.1	2.2	V	XC866-4FR, XC866-2FR
			2.0	2.1	2.3	V	XC866-1FR, ROM device
RAM data retention voltage	$V_{\rm DDCRDR}$	CC	0.9	1.0	1.1	V	
$V_{\rm DDC}$ brownout voltage in power-down mode ²⁾	V _{DDCBOPD}	CC	1.3	1.5	1.7	V	
V _{DDP} prewarning voltage ³⁾	$V_{\rm DDPPW}$	CC	3.4	4.0	4.6	V	
Power-on reset voltage ²⁾⁴⁾	$V_{\rm DDCPOR}$	CC	1.3	1.5	1.7	V	

¹⁾ Detection is disabled in power-down mode.

²⁾ Detection is enabled in both active and power-down mode.

³⁾ Detection is enabled for external power supply of 5.0V. Detection must be disabled for external power supply of 3.3V.

⁴⁾ The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.



4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins ($V_{\rm SS}$) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 36 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol	Li	mit Valu	es	Unit	Test Conditions/
		min.	typ .	max.		Remarks
Analog reference voltage	V_{AREF} SR	V _{AGND} + 1	V_{DDP}	V _{DDP} + 0.05	V	
Analog reference ground	V_{AGND} SR	V _{SS} - 0.05	V_{SS}	V _{AREF} - 1	V	
Analog input voltage range	V _{AIN} SR	V_{AGND}	_	V_{AREF}	V	
ADC clocks	f _{ADC}	_	20	40	MHz	module clock
	f _{ADCI}	_	_	10	MHz	internal analog clock See Figure 33
Sample time	t _S CC	(2 + INF t _{ADCI}	,		μs	
Conversion time	t _C CC	See Se	ction 4.	2.3.1	μs	
Total unadjusted	TUE ¹⁾ CC	_	_	±1	LSB	8-bit conversion. ²⁾
error		_	_	±2	LSB	10-bit conversion.
Differential Nonlinearity	DNL CC	_	±1	-	LSB	10-bit conversion ²⁾
Integral Nonlinearity	INL CC	_	±1	_	LSB	10-bit conversion ²⁾
Offset	OFF CC	_	±1	_	LSB	10-bit conversion ²⁾
Gain	GAIN CC	_	±1	_	LSB	10-bit conversion ²⁾
Switched capacitance at the reference voltage input	C _{AREFSW} CC	_	10	20	pF	2)3)



Table 36 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

		• •		•	•	
Parameter	Symbol	Limit Values			Unit	Test Conditions/
		min.	typ.	max.		Remarks
Switched capacitance at the analog voltage inputs	C _{AINSW} CC	_	5	7	pF	2)4)
Input resistance of the reference input	R _{AREF} CC	_	1	2	kΩ	2)
Input resistance of the selected analog channel	R _{AIN} CC	_	1	1.5	kΩ	2)

¹⁾ TUE is tested at $V_{\rm AREF}$ = 5.0 V, $V_{\rm AGND}$ = 0 V , $V_{\rm DDP}$ = 5.0 V.

²⁾ Not subject to production test, verified by design/characterization.

³⁾ This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

⁴⁾ The sampling capacity of the conversion C-Network is pre-charged to V_{AREF}/2 before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than V_{AREF}/2.



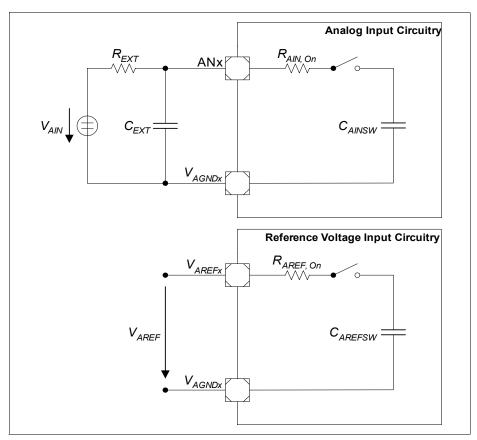


Figure 37 ADC Input Circuits

4.2.3.1 ADC Conversion Timing

```
Conversion time, t_C = t_{ADC} \times ( 1 + r \times (3 + n + STC) ), where r = CTC + 2 for CTC = 00_B, 01_B or 10_B, r = 32 for CTC = 11_B, CTC = Conversion Time Control (GLOBCTR.CTC), STC = Sample Time Control (INPCR0.STC), n = 8 or 10 (for 8-bit and 10-bit conversion respectively), t_{ADC} = 1 / t_{ADC}
```



4.2.4 Power Supply Current

Table 37 Power Supply Current Parameters (Operating Conditions apply; $V_{\text{DDP}} = 5V \text{ range}$)

Parameter	Symbol	Limit	Values	Unit	Test Condition	
		typ. ¹⁾	max. ²⁾		Remarks	
$V_{\rm DDP}$ = 5V Range		1			<u>, </u>	
Active Mode	I_{DDP}	22.6	24.5	mA	3)	
Idle Mode	I_{DDP}	17.2	19.7	mA	XC866-4FR, XC866-2FR ⁴⁾	
		12.5	14	mA	XC866-1FR, ROM device ⁴⁾	
Active Mode with slow-down enabled	I_{DDP}	7.2	8.2	mA	XC866-4FR, XC866-2FR ⁵⁾	
		5.6	7.5	mA	XC866-1FR, ROM device ⁵⁾	
Idle Mode with slow-down enabled	I_{DDP}	7.1	8	mA	XC866-4FR, XC866-2FR ⁶⁾	
		5.1	7.2	mA	XC866-1FR, ROM device ⁶⁾	

¹⁾ The typical $I_{\rm DDP}$ values are periodically measured at $T_{\rm A}$ = + 25 °C and $V_{\rm DDP}$ = 5.0 V.

The maximum $I_{\rm DDP}$ values are measured under worst case conditions ($T_{\rm A}$ = + 125 °C and $V_{\rm DDP}$ = 5.5 V).

³⁾ I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to 0010_B), RESET = V_{DDP}, no load on ports.

⁴⁾ I_{DDP} (idle mode) is measured with: <u>CPU clock</u> disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, <u>RESET</u> = V_{DDP}, no load on ports.

⁵⁾ I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to 0101_B, RESET = V_{DDP}, no load on ports.

⁶⁾ I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 833 KHz by setting CLKREL in CMCON to 0101_B, RESET = V_{DDP}, no load on ports.



Table 38 Power Down Current (Operating Conditions apply; $V_{\rm DDP}$ = 5V range)

Parameter	Symbol	Limit	Values	Unit	Test Condition Remarks
		typ. ¹⁾	max. ²⁾		
$V_{\rm DDP}$ = 5V Range	<u> </u>				
Power-Down Mode ³⁾	I_{PDP}	1	10	μΑ	$T_{A} = + 25 {}^{\circ}\text{C.}^{4)}$
		-	30	μΑ	$T_A = +85 ^{\circ}\text{C}, \text{ XC866-}$ 4FR, XC866-2FR ⁴⁾⁵⁾
		-	35	μΑ	T_{A} = + 85 °C, XC866- 1FR, ROM device ⁴⁾⁵⁾

¹⁾ The typical $I_{\rm PDP}$ values are measured at $V_{\rm DDP}$ = 5.0 V.

²⁾ The maximum $I_{\rm PDP}$ values are measured at $V_{\rm DDP}$ = 5.5 V.

³⁾ I_{PDP} (power-down mode) has a maximum value of 200 μ A at T_A = + 125 °C.

⁴⁾ I_{PDP} (power-down mode) is measured with: RESET = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0 = V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

⁵⁾ Not subject to production test, verified by design/characterization.



Table 39 Power Supply Current Parameters (Operating Conditions apply; $V_{\text{DDP}} = 3.3 \text{V range}$)

Parameter	Symbol	Limit	Values	Unit	Test Condition	
		typ. ¹⁾	max. ²⁾		Remarks	
V _{DDP} = 3.3V Range		1				
Active Mode	I_{DDP}	21.5	23.3	mA	3)	
Idle Mode	I_{DDP}	16.4	18.9	mA	XC866-4FR, XC866-2FR ⁴⁾	
		11.2	13.5	mA	XC866-1FR, ROM device ⁴⁾	
Active Mode with slow-down enabled	I_{DDP}	6.8	8	mA	XC866-4FR, XC866-2FR ⁵⁾	
		5.4	7.3	mA	XC866-1FR, ROM device ⁵⁾	
Idle Mode with slow-down enabled	I_{DDP}	6.8	7.8	mA	XC866-4FR, XC866-2FR ⁶⁾	
		4.9	6.9	mA	XC866-1FR, ROM device ⁶⁾	

¹⁾ The typical $I_{\rm DDP}$ values are periodically measured at $T_{\rm A}$ = + 25 °C and $V_{\rm DDP}$ = 3.3 V.

The maximum $I_{\rm DDP}$ values are measured under worst case conditions ($T_{\rm A}$ = + 125 °C and $V_{\rm DDP}$ = 3.6 V).

³⁾ I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to 0010_B), RESET = V_{DDP}, no load on ports.

⁴⁾ I_{DDP} (idle mode) is measured with: <u>CPU clock</u> disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, <u>RESET</u> = V_{DDP}, no load on ports.

⁵⁾ I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to 0101_B, RESET = V_{DDP}, no load on ports.

 $^{^{6)}}$ I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enable and running at 833 KHz by setting CLKREL in CMCON to 0101_B,, RESET = $V_{\rm DDP}$, no load on ports.



Table 40 Power Down Current (Operating Conditions apply; $V_{\rm DDP}$ = 3.3V range)

Parameter	Symbol	Limit	Values	Unit	Test Condition Remarks
		typ. ¹⁾	max. ²⁾		
V_{DDP} = 3.3V Range	"				
Power-Down Mode ³⁾	I_{PDP}	1	10	μΑ	$T_{A} = + 25 {}^{\circ}\text{C.}^{4)}$
		-	30	μΑ	T_A = + 85 °C, XC866- 4FR, XC866-2FR ⁴⁾⁵⁾
		-	35	μΑ	T_{A} = + 85 °C, XC866- 1FR, ROM device ⁴⁾⁵⁾

¹⁾ The typical $I_{\rm PDP}$ values are measured at $V_{\rm DDP}$ = 3.3 V.

 $^{^{2)}~}$ The maximum $I_{\rm PDP}$ values are measured at $V_{\rm DDP}$ = 3.6 V.

 $^{^{3)}}$ I_{PDP} (power-down mode) has a maximum value of 200 μA at $T_{\rm A}$ = + 125 °C.

⁴⁾ I_{PDP} (power-down mode) is measured with: RESET = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0= V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

⁵⁾ Not subject to production test, verified by design/characterization.



4.3 AC Parameters

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in Figure 38, Figure 39 and Figure 40.

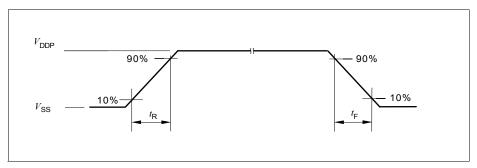


Figure 38 Rise/Fall Time Parameters

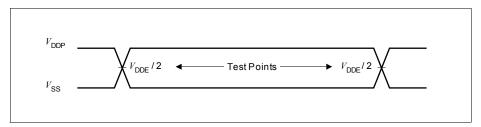


Figure 39 Testing Waveform, Output Delay

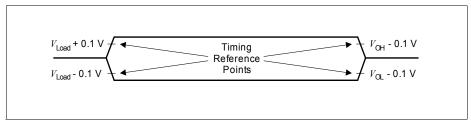


Figure 40 Testing Waveform, Output High Impedance



4.3.2 Output Rise/Fall Times

Table 41 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	_	Limit Values		Test Conditions	
		min. max.				
$V_{\rm DDP}$ = 5V Range	"	'		'		
Rise/fall times 1) 2)	t _R , t _F	_	10	ns	20 pF. ³⁾	
$V_{\rm DDP}$ = 3.3V Range	"	'		'		
Rise/fall times 1) 2)	t _R , t _F	_	10	ns	20 pF. ⁴⁾	

¹⁾ Rise/Fall time measurements are taken with 10% - 90% of the pad supply.

 $^{^{\}rm 4)}$ Additional rise/fall time valid for C $_{\rm L}$ = 20pF - 100pF @ 0.225 ns/pF.

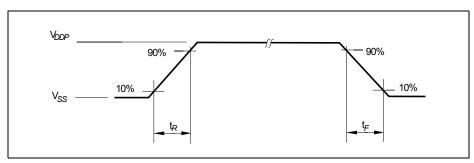


Figure 41 Rise/Fall Times Parameters

²⁾ Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

 $^{^{3)}}$ Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.125 ns/pF.



4.3.3 Power-on Reset and PLL Timing

Table 42 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Conditions	
		min.	typ.	max.			
Pad operating voltage	V_{PAD} CC	2.3	_	_	V		
On-Chip Oscillator start-up time	t _{OSCST} CC	_	-	500	ns		
Flash initialization time	$t_{\sf FINIT}$ CC	_	160	_	μs		
RESET hold time ¹⁾	t _{RST} SR	_	500	_	μs	V_{DDP} rise time (10% – 90%) \leq 500 μ s	
PLL lock-in in time	$t_{LOCK}CC$	_	_	200	μs		
PLL accumulated jitter	D_{P}	_	_	0.7	ns	2)	

 $[\]overline{\text{RESET}}$ signal has to be active (low) until V_{DDC} has reached 90% of its maximum value (typ. 2.5V).

²⁾ PLL lock at 80 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 40 and P = 1.

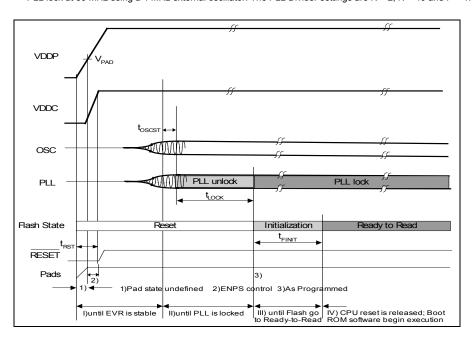


Figure 42 Power-on Reset Timing



4.3.4 On-Chip Oscillator Characteristics

Table 43 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Lin	Limit Values			Test Conditions	
			min.	typ.	max.			
Nominal frequency	f _{NOM}	CC	9.75	10	10.25	MHz	under nominal conditions ¹⁾ after IFX-backend trimming	
Long term frequency deviation ²⁾	Δf_{LT}	CC	-5.0	_	5.0	%	with respect to f_{NOM} , over lifetime and temperature (– 10°C to 125°C), for one device after trimming	
			-6.0	_	0	%	with respect to f_{NOM} , over lifetime and temperature (– 40°C to -10°C), for one device after trimming	
Short term frequency deviation	Δf_{ST}	CC	-1.0	_	1.0	%	with respect to f_{NOM} , within one LIN message (<10 ms 100 ms)	

¹⁾ Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

²⁾ Not all parameters are 100% tested, but are verified by design/characterization and test correlation.



4.3.5 JTAG Timing

Table 44 TCK Clock Timing (Operating Conditions apply; $C_L = 50 \text{ pF}$)

Parameter	Symbol	Limits		Unit
		min	max	
TCK clock period	$t_{TCK}SR$	50	_	ns
TCK high time	t ₁ SR	20	_	ns
TCK low time	t_2 SR	20	_	ns
TCK clock rise time	t ₃ SR	_	4	ns
TCK clock fall time	t_4 SR	_	4	ns

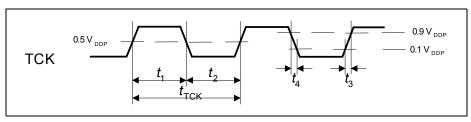


Figure 43 TCK Clock Timing



Table 45 JTAG Timing (Operating Conditions apply; $C_L = 50 \text{ pF}$)

Parameter		nbol	Lir	Unit	
			min	max	
TMS setup to TCK _r	t_1	SR	8.0	-	ns
TMS hold to TCK _r	t_2	SR	5.0	-	ns
TDI setup to TCK _r	t_1	SR	11.0	_	ns
TDI hold to TCK _/	t_2	SR	6.0	-	ns
TDO valid output from TCK ¬_	t_3	CC	_	23	ns
TDO high impedance to valid output from TCK ٦	t_4	CC	_	26	ns
TDO valid output to high impedance from TCK ٦_	t_5	CC	_	18	ns

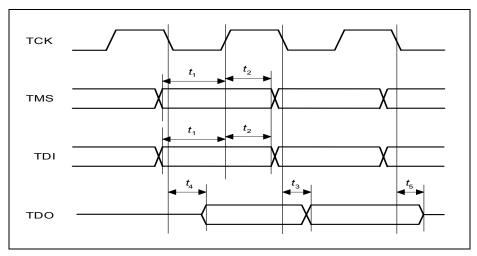


Figure 44 JTAG Timing



4.3.6 SSC Master Mode Timing

Table 46 SSC Master Mode Timing (Operating Conditions apply; $C_L = 50 \text{ pF}$)

Parameter	Symbol	Limit	Unit	
		min.	max.	
SCLK clock period	t_0 CC	2*T _{SSC} 1)	_	ns
MTSR delay from SCLK _/	t ₁ CC	0	8	ns
MRST setup to SCLK ٦_	t_2 SR	22	_	ns
MRST hold from SCLK ٦_	t_3 SR	0	_	ns

¹⁾ $T_{\rm SSCmin}$ = $T_{\rm CPU}$ = 1/ $f_{\rm CPU}$. When $f_{\rm CPU}$ = 26.7MHz, $t_{\rm 0}$ = 74.9ns. $T_{\rm CPU}$ is the CPU clock period.

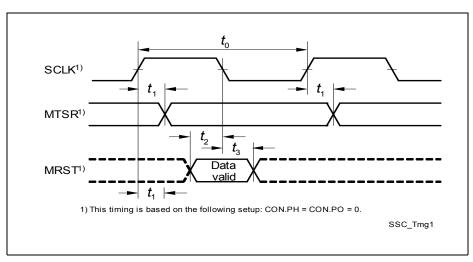


Figure 45 SSC Master Mode Timing



Package and Reliability

5 Package and Reliability

5.1 Package Parameters (PG-TSSOP-38)

Table 47 provides the thermal characteristics of the package.

Table 47 Thermal Characteristics of the Package

Parameter	Symbol		Limi	t Values	Unit	Notes			
			Min.	Max.					
Thermal resistance junction case ¹⁾	R_{TJC}	CC	-	15.7	K/W	-			
Thermal resistance junction lead ¹⁾	R_{TJL}	СС	-	39.2	K/W	-			

The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by

a) simply adding only the two thermal resistances (junction lead and lead ambient), or

b) by taking all four resistances into account, depending on the precision needed.



Package and Reliability

5.2 Package Outline

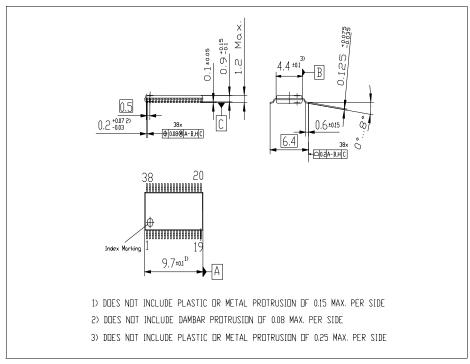


Figure 46 PG-TSSOP-38-4 Package Outline



Package and Reliability

5.3 Quality Declaration

Table 48 shows the characteristics of the quality parameters in the XC866.

Table 48 Quality Parameters

Parameter	Symbol	Limit	Values	Unit	Notes	
		Min.	Max.			
ESD susceptibility according to Human Body Model (HBM)	V _{HBM}	-	2000	V	Conforming to EIA/JESD22- A114-B	
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C	





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