



MIC3002

FOM Management IC with Internal Calibration

General Description

The MIC3002 is a fiber optic module controller which enables the implementation of sophisticated, hot-pluggable fiber optic transceivers with intelligent laser control and an internally calibrated Digital Diagnostic Monitoring Interface per SFF-8472. It essentially integrates all non-datapath functions of an SFP transceiver into a tiny (4mm x 4mm) QFN package. It also works well as a microcontroller peripheral in transponders or 10Gbps transceivers.

A highly configurable automatic power control (APC) circuit controls laser bias. Bias and modulation are temperature compensated using dual DACs, an on-chip temperature sensor, and NVRAM look-up tables. A programmable internal feedback resistor provides a wide dynamic range for the APC. Controlled laser turn-on facilitates hot plugging.

An analog-to-digital converter converts the measured temperature, voltage, bias current, transmit power, and received power from analog to digital. An EEPROM provides front-end adjustment of RX power. Each parameter is compared against user-programmed warning and alarm thresholds. Analog comparators and DACs provide high-speed monitoring of received power and critical laser operating parameters. Data can be reported as either internally calibrated or externally calibrated.

An interrupt output, power-on hour meter, and data-ready bits add user friendliness beyond SFF-8472. The interrupt output and data-ready bits reduce overhead in the host system. The power-on hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM.

In addition to the features listed above which are already implemented in the previous controller MIC3001, the MIC3002 features an extensive temperature range, options to mask alarms and warnings interrupt and TXFAULT, and ability to support up to four chips with the same address on the serial interface.

Communication with the MIC3002 is via an industry standard 2-wire serial interface. Nonvolatile memory is provided for serial ID, configuration, and separate OEM and user scratchpad spaces. Two-level password protection guards against data corruption.

Features

- Extensive temperature range
- Alarms and Warnings interrupt and TXFAULT masks
- Capability to support up to four chips on the serial interface
- LUT to compensate for chip-FOM case temperature difference
- APC or constant-current laser bias
- Turbo mode for APC loop start-up and shorter laser turn on time
- Supports multiple laser types and bias circuit topologies
- Integrated digital temperature sensor
- Temperature compensation of modulation, bias, and fault levels via NVRAM look-up tables
- NVRAM to support GBIC/SFP serial ID function
- User writable EEPROM scratchpad
- Diagnostic monitoring interface per SFF-8472
 - Monitors and reports critical parameters: temperature, bias current, TX and RX optical power, and supply voltage
 - S/W control and monitoring of TXFAULT, RXLOS, RATESELECT, and TXDISABLE
 - Internal or external calibration
 - EEPROM for adjusting RX power measurement
- Power-on hour meter
- Interrupt capability
- Extensive test and calibration features
- 2-wire SMBus-compatible serial interface
- SFP/SFP+ MSA and SFF-8472 compliant
- 3.0V to 3.6V power supply range
- 5V-tolerant I/O
- Available in (4mm x 4mm) 24-pin QFN package

Applications

- SFP/SFP+ optical transceivers
- SONET/SDH transceivers and transponders
- Fibre Channel transceivers
- 10Gbps transceivers
- Free space optical communications
- Proprietary optical links

Ordering Information

| Part Number | Package Type | Junction Temp. Range | Package Marking | Lead Finish |
|-----------------------------|--------------|----------------------|---|-------------------|
| MIC3002BML | 24-pin QFN | -45°C to +105°C | 3002 | Sn-Pb |
| MIC3002BMLTR ⁽¹⁾ | 24-pin QFN | -45°C to +105°C | 3002 | Sn-Pb |
| MIC3002GML | 24-pin QFN | -45°C to +105°C | 3002 with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| MIC3002GMLTR ⁽¹⁾ | 24-pin QFN | -45°C to +105°C | 3002 with Pb-Free bar-line indicator | Pb-Free NiPdAu |

1. **Note:**
2. Tape and Reel.

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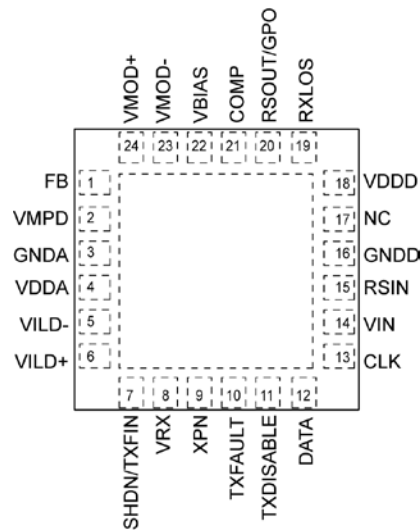
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Pin Configuration



24-Pin QFN

Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|------------|--|
| 1 | FB | Analog Input. Feedback voltage for the APC loop op-amp. Polarity and scale are programmable via the APC configuration bits. Connect to V_{BIAS} if APC is not used. |
| 2 | VMPD | Analog Input. Multiplexed A/D converter input for monitoring transmitted optical power via a monitor photodiode. In most applications, VMPD will be connected directly to FB. The input range is $0 - V_{REF}$ or $0 - V_{REF}/4$ depending on the setting of the APC configuration bits |
| 3 | GND A | Ground return for analog functions. |
| 4 | VDD A | Power supply input for analog functions. |
| 5 | VILD- | Analog Input. Reference terminal for the multiplexed pseudo-differential A/D converter inputs for monitoring laser bias current via a sense resistor (VILD+ is the sensing input). Tie to V_{DD} or GND to reference the voltage sensed on VILD+ to V_{DD} or GND, respectively. Limited common-mode voltage range, see "Applications Information" section for more details. |
| 6 | VILD+ | Analog Input. Multiplexed A/D input for monitoring laser bias current via a sense resistor (signal input); accommodates inputs referenced to V_{DD} or GND (see pin 5 description). Limited common-mode voltage range, see "Applications Information" section for more details. |
| 7 | SHDN/TXFIN | Digital output/Input; programmable polarity. When used as shutdown output (SHDN), OEMCFG3-2 set to 0, SHDN is asserted at the detection of a fault condition if OEMCFG4-7 is set to 0. If the latter bit is set to 1, a fault condition will not assert SHDN. When programmed as TXFIN, it is an input for external fault signals to be ORed with the internal fault sources to drive TXFAULT. |
| 8 | VRX | Analog Input. Multiplexed A/D converter input for monitoring received optical power. The input range is 0 to V_{REF} . A 5-bit programmable EEPROM on this pin provides for coarse calibration and ranging of the RX power measurement. |
| 9 | XPN | Analog Input/Output. Optional connection to an external PN junction for sensing temperature at a remote location. The Zone bit in OEMCFG1 determines whether temperature is measured using the on-chip sensor or the remote PN junction. |
| 10 | TXFAULT | Digital Output; Open-Drain, programmable polarity. If OEMCFG5-4 is set to 0, a high level indicates a hardware fault impeding transmitter operation. The state of this pin is always reflected in the TXFLT bit. |

Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|-----------|--|
| 11 | TXDISABLE | Digital Input; Active High. The transmitter is disabled when this line is high or the STXDIS bit is set. The state of this input is always reflected in the TXDIS bit. |
| 12 | DATA | Digital I/O; Open-drain. Bi-directional serial data input/output. |
| 13 | CLK | Digital Input; Serial clock input. |
| 14 | VIN/INT | If bit 4 (IE) in USRCTL register is set to 0 (default), this pin is configured as analog input. If IE bit is set to 1, this pin is configured as open-drain output. Analog Input: Multiplexed A/D input for monitoring supply voltage. 0V to 5.5V input range. Open-drain output: outputs the internally generated interrupt signal /INT. |
| 15 | RSIN | Digital Input; Rate Select Input; ORed with rate select bit to determine the state of the RSOUT pin. The state of this pin is always reflected in the RSEL bit. |
| 16 | GNDD | Ground return for digital functions. |
| 17 | NC | No connection. This pin is used for test purposes and must be left unconnected. |
| 18 | VDDD | Power supply input for digital functions. |
| 19 | RXLOS | Digital Output; programmable polarity Open-Drain. Indicates the loss of the received signal as indicated by a level of received optical power below the programmed RXLOS comparator threshold; may be wire-ORed with external signals. Normal operation is indicated by a Low level when OEMCFG6-3 is set to 0 and a high level when OEMCFG6-3 is set to 1. RXLOS is de-asserted when $VRX > LOSFLn$. The LOS bit reflects the state of RXLOS whether driven by the MIC3002 or an external circuit. |
| 20 | RS0/GPO | Digital Output. Open-Drain or push-pull. When used as rate select output, it represents the receiver rate select as per SFF. This output is controlled by the SRSEL bit ORed with RSIN input and is open drain only. When used as a general-purpose, non-volatile output, it is controlled by the GPO configuration bits in OEMCFG3. |
| 21 | COMP | Analog Output, compensation terminal. Connect a capacitor between this pin and GNDA or VDDA with appropriate value to tune the APC loop time constant to a desirable value. |
| 22 | VBIAS | Analog Output. Buffered DAC output capable of sourcing or sinking up to 10mA under control of the APC function to drive an external transistor for laser diode D.C. bias. The output and feedback polarity are programmable to accommodate either a NPN or a PNP transistor to drive a common-anode or common-cathode laser diode. |
| 23 | VMOD- | Analog Input. Inverting terminal of VMOD buffer op-amp. Connect to V_{MOD+} (gain = 1) or feedback resistors network to set a different gain |
| 24 | VMOD+ | Analog Output. Buffered DAC output to set the modulation current on the laser driver IC. Operates with either a $0 - V_{REF}$ or a $(V_{DD} - V_{REF}) - V_{DD}$ output swing so as to generate either a ground-referenced or a V_{DD} referenced programmed voltage. A simple external circuit can be used to generate a programmable current for those drivers that require a current rather than a voltage input. See "Applications Information" section for more details. |

Absolute Maximum Ratings⁽¹⁾

| | |
|--|------------------------|
| Power Supply Voltage, V_{DD} | +3.8V |
| Voltage on CLK, DATA, TXFAULT, VIN, RXLOS, DISABLE, RSIN..... | -0.3V to +6.0V |
| Voltage On Any Other Pin | -0.3V to $V_{DD}+0.3V$ |
| Power Dissipation, $T_A = 85^\circ\text{C}$ | 1.5W |
| Junction Temperature (T_J) | 150°C |
| Storage Temperature (T_S) | -65°C to +150°C |
| ESD Ratings⁽³⁾ | |
| Human Body Model..... | 2kV |
| Machine Model | 300V |
| Soldering (20sec) | 260°C |

Operating Ratings⁽²⁾

| | |
|---|-----------------|
| Power Supply Voltage, V_{DDA}/V_{DDD} | +3.0V to +3.6V |
| Ambient Temperature Range (T_A) ... | -40°C to +105°C |
| Package Thermal Resistance QFN (θ_{JA}) | 43°C/W |

Electrical Characteristics

For typical values, $T_A = 25^\circ\text{C}$, $V_{DDA} = V_{DDD} = +3.3V$, unless otherwise noted. **Bold** values are guaranteed for $+3.0V \leq (V_{DDA} = V_{DDD}) \leq 3.6V$, $T_{(\min)} \leq T_A \leq T_{(\max)}$ ⁽⁸⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------------------|-----------------------------------|--|-------|-------|-------|---------------|
| Power Supply | | | | | | |
| I_{DD} | Supply Current | CLK = DATA = $V_{DDD} = V_{DDA}$; TXDISABLE low; all DACs at full- scale; all A/D inputs at full-scale; all other pins open. | | 2.3 | 3.5 | mA |
| | | CLK = DATA = $V_{DDD} = V_{DDA}$; TXDISABLE high; FLTDAC at full- scale; all A/D inputs at full-scale; all other pins open. | | 2.3 | 3.5 | mA |
| V_{POR} | Power-on Reset Voltage | All registers reset to default values; A/D conversions initiated. | | 2.9 | 2.98 | V |
| V_{UVLO} | Under-Voltage Lockout Threshold | Note 5 | 2.5 | 2.73 | | V |
| V_{HYST} | Power-on Reset Hysteresis Voltage | | | 170 | | mV |
| t_{POR} | Power-on Reset Time | $V_{DD} > V_{POR}$ ⁽⁴⁾ | | 50 | | μs |
| V_{REF} | Reference Voltage | | 1.210 | 1.225 | 1.240 | V |
| $\Delta V_{REF}/\Delta V_{DDA}$ | Voltage Reference Line Regulation | | | 1.7 | | mV/V |

Temperature-to-Digital Converter Characteristics

| | | | | | | |
|--------------|--------------------------------------|---|--|---------|---------|------------------|
| | Local Temperature Measurement Error | $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ ⁽⁶⁾ | | ± 1 | ± 3 | $^\circ\text{C}$ |
| | Remote Temperature Measurement Error | $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ ⁽⁶⁾ | | ± 1 | ± 3 | $^\circ\text{C}$ |
| t_{CONV} | Conversion Time | Note 4 | | | 60 | ms |
| t_{SAMPLE} | Sample Period | | | | 100 | ms |

Remote Temperature Input, XPN

| | | | | | | |
|-------|--|-------------------------------------|---|-----|-----|---------------|
| I_F | Current to External Diode ⁽⁴⁾ | XPN at high level, clamped to 0.6V. | | 192 | 400 | μA |
| | | XPN at low level, clamped to 0.6V. | 7 | 12 | | μA |

Voltage-to-Digital Converter Characteristics (V_{RX} , V_{AUX} , V_{BIAS} , V_{MPD} , $V_{ILD\pm}$)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------------|---------------------------|--|-----|---------|-----------|-------|
| | Voltage Measurement Error | $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}^{(6)}$ | | ± 1 | ± 2.0 | %fs |
| t_{CONV} | Conversion Time | Note 4 | | | 10 | ms |
| t_{SAMPLE} | Sample Period | Note 4 | | | 100 | ms |

Voltage Input, V_{IN} (Pin 14 used as an ADC Input)

| | | | | | | |
|-------------------|---------------------|--|-----|----|-----|---------------|
| V_{IN} | Input Voltage Range | $-0.3 \leq V_{\text{DD}} \leq 3.6\text{V}$ | GND | | 5.5 | V |
| I_{LEAK} | Input Current | $V_{\text{IN}} = V_{\text{DD}}$ or GND; $V_{\text{AUX}} = V_{\text{IN}}$ | | 55 | | μA |
| C_{IN} | Input Capacitance | | | 10 | | pF |

Digital-to-Voltage Converter Characteristics (V_{MOD} , V_{BIAS})

| | | | | | | |
|-------------------|----------------------------------|--|--|-----------|---------|-----|
| | Accuracy | $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}^{(6)}$ | | ± 1 | 2.0 | %fs |
| t_{CONV} | Conversion Time | Note 4 | | | 20 | ms |
| DNL | Differential Non-linearity Error | Note 4 | | ± 0.5 | ± 1 | LSB |

Bias Current Sense Inputs, $V_{\text{ILD}+}$, $V_{\text{ILD}-}$

| | | | | | | |
|------------------|--|--|---|------|--------------------|---------------|
| V_{ILD} | Differential Input Signal Range, $ V_{\text{ILD}+} - V_{\text{ILD}-} $ | | 0 | | $V_{\text{REF}}/4$ | mV |
| $I_{\text{IN}+}$ | $V_{\text{ILD}+}$ input current | | | | ± 1 | μA |
| $I_{\text{IN}-}$ | $V_{\text{ILD}-}$ input current $ V_{\text{ILD}+} - V_{\text{ILD}-} = 0.3\text{V}$ | $V_{\text{ILD}-}$ referred to V_{DDA} | | +150 | | μA |
| | | $V_{\text{ILD}-}$ referred to GND | | -150 | | μA |
| C_{IN} | Input Capacitance | | | 10 | | pF |

APC Op Amp, FB, V_{BIAS} , COMP

| | | | | | | |
|-----------------------------|---|--|-------------------------|----------|------------------|--------------------------------|
| GBW | Gain Bandwidth Product | $C_{\text{COMP}} = 20\text{pF}$; Gain = 1 | | 1 | | MHz |
| TC_{VOS} | Input Offset Voltage Temperature Coefficient ⁽⁴⁾ | | | 1 | | $\mu\text{V}/^{\circ}\text{C}$ |
| V_{OUT} | Output Voltage Swing | $I_{\text{OUT}} = 10\text{mA}$, SRCE bit = 1 | GND | | 1.25 | V |
| | | $I_{\text{OUT}} = -10\text{mA}$, SRCE bit = 0 | $V_{\text{DDA}} - 1.25$ | | V_{DDA} | V |
| I_{SC} | Output Short-Circuit Current | | | 55 | | mA |
| t_{SC} | Short Circuit Withstand Time | $T_J \leq 150^{\circ}\text{C}^{(4)}$ | | | | sec |
| PSRR | Power Supply Rejection Ratio | $C_{\text{COMP}} = 20\text{pF}$; Gain = 1, to GND | | 55 | | dB |
| | | $C_{\text{COMP}} = 20\text{pF}$; Gain = 1, to V_{DD} | | 40 | | |
| A_{MIN} | Minimum Stable Gain | $C_{\text{COMP}} = 20\text{pF}$, Note 4 | | | 1 | V/V |
| $\Delta V/\Delta t$ | Slew Rate | $C_{\text{COMP}} = 20\text{pF}$; Gain = 1 | | 3 | | V/ μs |
| ΔRFB | Internal Feedback Resistor Tolerance | | | ± 20 | | % |
| $\Delta\text{RFB}/\Delta t$ | Internal Feedback Resistor Temperature Coefficient | | | 25 | | ppm/C |
| I_{START} | Laser Start-up Current Magnitude | START = 01 _h | | 0.375 | | mA |
| | | START = 02 _h | | 0.750 | | mA |
| | | START = 04 _h | | 1.500 | | mA |
| | | START = 08 _h | | 3.000 | | mA |
| C_{IN} | Pin Capacitance | | | 10 | | pF |

Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------|-----------|-----------|-----|-----|-----|-------|
|--------|-----------|-----------|-----|-----|-----|-------|

V_{MOD} Buffer Op-Amp, V_{MOD+}, V_{MOD-}

| | | | | | | |
|-------------------|--|--|--------|------|----------------------|-------|
| GBW | Gain Bandwidth | C _{COMP} = 20pF; Gain = 1 | | 1 | | MHz |
| TC _{VOS} | Input Offset Voltage Temperature Coefficient | | | 1 | | μV/°C |
| I _{BIAS} | V _{MOD-} Input Current | | | ±0.1 | ±1 | μA |
| V _{OUT} | Output Voltage Swing | I _{OUT} = ±1mA | GND+75 | | V _{DDA} -75 | mV |
| I _{SC} | Output Short-Circuit Current | | | 35 | | mA |
| t _{SC} | Short Circuit Withstand Time | T _J ≤ 150°C ⁽⁴⁾ | | | | sec |
| PSRR | Power Supply Rejection Ratio | C _{COMP} = 20pF; Gain = 1, to GND | | 65 | | dB |
| | | C _{COMP} = 20pF; Gain = 1, to V _{DD} | | 44 | | dB |
| A _{MIN} | Minimum Stable Gain | C _{COMP} = 20pF | | | 1 | V/V |
| ΔV/ΔT | Slew Rate | C _{COMP} = 20pF; Gain = 1 | | 1 | | V/μs |
| C _{IN} | Pin Capacitance | | | 10 | | pF |

Control and Status I/O, TXDISABLE, TXFAULT, RSIN, RSOUT(GPO), SHDN(TXFIN), RXLOS, /INT

| | | | | | | |
|-------------------|--|-----------------------|-----|----|-----------------------|----|
| V _{IL} | Low Input Voltage | | | | 0.8 | V |
| V _{IH} | High Input Voltage | | 2.0 | | | V |
| V _{OL} | Low Output Voltage | I _{OL} ≤ 3mA | | | 0.3 | V |
| V _{OH} | High Output Voltage (applies to SHDN only) | I _{OH} ≤ 3mA | | | V _{DDD} -0.3 | V |
| I _{LEAK} | Input Current | | | | ±1 | μA |
| C _{IN} | Input Capacitance | | | 10 | | pF |

Transmit Optical Power Input, V_{MPD}

| | | | | | | |
|-------------------|---------------------|-----------|------------------------------------|----|------------------|----|
| V _{IN} | Input Voltage Range | Note 4 | GND | | V _{DDA} | V |
| V _{RX} | Input Signal Range | BIASREF=0 | | | V _{REF} | V |
| | | BIASREF=1 | V _{DDA} -V _{REF} | | V _{DDA} | V |
| C _{IN} | Input Capacitance | Note 4 | | 10 | | pF |
| I _{LEAK} | Input Current | | | | ±1 | μA |

Received Optical Power Input, VRX, RXPOT

| | | | | | | |
|--------------------------------------|--|------------------------------|-----|-----|------------------|-------|
| | Input Voltage Range | Note 4 | GND | | V _{DDA} | V |
| V _{RX} | Valid Input Signal Range (ADC Input Range) | | 0 | | V _{REF} | V |
| R _{RXPOT(32)} | End-to-End Resistance | RXPOT = 1F _h | | 32 | | KΩ |
| ΔRXPOT | Resistor Tolerance | | | ±20 | | % |
| ΔRXPOT/ΔT | Resistor Temperature Coefficient | | | 25 | | ppm/C |
| ΔV _{RX} /V _{RXPOT} | Divider Ratio Accuracy | 00 ≤ RXPOT ≤ 1F _h | -5 | | +5 | % |
| I _{LEAK} | Input Current | RXPOT = 0 (disconnected) | | | ±1 | μA |
| C _{IN} | Input Capacitance | Note 4 | | 10 | | pF |
| I _{LEAK} | Input Current | | | | ±1 | μA |

Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--|--|---|-----------|-----|------------|---------|
| Control and Status I/O Timing, TXFAULT, TXDISABLE, RSIN, RSOUT, and RXLOS | | | | | | |
| t_{OFF} | TXDISABLE Assert Time | From input asserted to optical output at 10% of nominal, $C_{COMP} = 10nF$. | | | 10 | μs |
| t_{ON} | TXDISABLE De-assert Time | From input de-asserted to optical output at 90% of nominal, $C_{COMP} = 10nF$. | | | 1 | ms |
| t_{INIT} | Initialization Time | From power on or transmitter enabled to optical output at 90% of nominal and TX_FAULT de-asserted. ⁽⁴⁾ | | | 300 | ms |
| t_{INIT2} | Power-on Initialization Time | From power on to APC loop-enabled. | | | 200 | ms |
| t_{FAULT} | TXFAULT Assert Time | From fault condition to TXFAULT assertion. ⁽⁴⁾ | | | 95 | μs |
| t_{RESET} | Fault Reset Time | Length of time TXDISABLE must be asserted to reset fault condition. | 10 | | | μs |
| t_{LOSS_ON} | RXLOS Assert Time | From loss of signal to RXLOS asserted. | | | 95 | μs |
| t_{LOSS_OFF} | RXLOS De-assert Time | From signal acquisition to LOS de-asserted. | | | 100 | μs |
| t_{DATA} | Analog Parameter Data Ready | From power on to valid analog parameter data available. ⁽⁴⁾ | | | 400 | ms |
| t_{PROP_IN} | TXFAULT, TXDISABLE, RXLOS, RSIN Input Propagation Time | Time from input change to corresponding internal register bit set or cleared. ⁽⁴⁾ | | | 1 | μs |
| t_{PROP_OUT} | TXFAULT, RSOUT, /INT Output Propagation Time | From an internal register bit set or cleared to corresponding output change. ⁽⁴⁾ | | | 1 | μs |

Fault Comparators

| | | | | | | |
|----------------|--------------------------------------|---|--------------|-----|--------------|---------|
| ϕ_{FLTMR} | Fault Suppression Timer Clock Period | Note 4 | 0.475 | 0.5 | 0.525 | ms |
| | Accuracy | | -3 | | +3 | %/F.S. |
| t_{REJECT} | Glitch Rejection | Maximum length pulse that will not cause output to change state. ⁽⁴⁾ | 4.5 | | | μs |
| V_{SAT} | Saturation Detection Threshold | High level | | 95 | | %VDDA |
| | | Low level | | 5 | | %VDDA |

Power-On Hour Meter

| | | | | | | |
|--|-------------------|--|------------|----|------------|-------|
| | Timebase Accuracy | $0^{\circ}C \leq T_A \leq +70^{\circ}C$ ⁽⁴⁾ | +5 | | -5 | % |
| | | $-40^{\circ}C \leq T_A \leq +105^{\circ}C$ | +10 | | -10 | % |
| | Resolution | Note 4 | | 10 | | hours |

Non-Volatile (FLASH) Memory

| | | | | | | |
|-----------|---------------------------------------|---|---------------|--|-----------|--------|
| t_{WR} | Write Cycle Time(7) | From STOP of a one to four-byte write transaction. ⁽⁴⁾ | | | 13 | ms |
| | Data Retention | | 100 | | | years |
| Endurance | Minimum Permitted Number Write Cycles | | 10,000 | | | cycles |

Serial Data I/O Pin, Data

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------------|--------------------|-----------------------|------------|-----|------------|-------|
| V _{OL} | Low Output Voltage | I _{OL} = 3mA | | | 0.4 | V |
| | | I _{OL} = 6mA | | | 0.6 | V |
| V _{IL} | Low Input Voltage | | | | 0.8 | V |
| V _{IH} | High Input Voltage | | 2.1 | | | V |
| I _{LEAK} | Input Current | | | | ±1 | μA |
| C _{IN} | Input Capacitance | Note 4 | | 10 | | pF |

Serial Clock Input, CLK

| | | | | | | |
|-------------------|--------------------|-------------------------------|------------|----|------------|----|
| V _{IL} | Low Input Voltage | 2.7V ≤ V _{DD} ≤ 3.6V | | | 0.8 | V |
| V _{IH} | High Input Voltage | 2.7V ≤ V _{DD} ≤ 3.6V | 2.1 | | | V |
| I _{LEAK} | Input Current | | | | ±1 | μA |
| C _{IN} | Input Capacitance | Note 4 | | 10 | | pF |

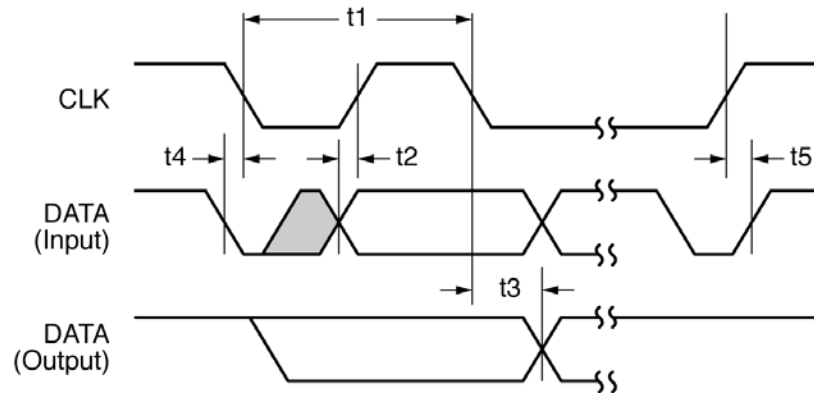
Serial Interface Timing⁽⁴⁾

| | | | | | | |
|-------------------|------------------------------------|--|------------|--|------------|----|
| t ₁ | CLK (clock) Period | | 2.5 | | | μs |
| t ₂ | Data In Setup Time to CLK High | | 100 | | | ns |
| t ₃ | Data Out Stable After CLK Low | | 300 | | | ns |
| t ₄ | Data Low Setup Time to CLK Low | Start Condition | 100 | | | ns |
| t ₅ | Data High Hold Time After CLK High | Stop Condition | 100 | | | ns |
| t _{DATA} | Data Ready Time | From power on to completion of one set of ADC conversions; analog data available via serial interface. | | | 400 | ms |

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended.
4. Guaranteed by designing and/or testing of related parameters. Not 100% tested in production.
5. The MIC3000 will attempt to enter its shutdown state when V_{DD} falls below V_{JVLO}. This operation requires time to complete. If the supply voltage falls too rapidly, the operation may not be completed.
6. Does not include quantization error.
7. The MIC3002 will not respond to serial bus transactions during an EEPROM write-cycle. The host will receive a NACK during t_{WR}.
8. Final test on outgoing product is performed at T_A = +25°C.

Timing Diagram



Serial Interface Timing

Address Map

| Address(s) | Field Size (Bytes) | Name | Description |
|------------|--------------------|------------------------------|---|
| 0 – 95 | 96 | Serial ID defined by SEP MSA | G-P NVRAM; R/W under valid OEM password. |
| 96 – 127 | 32 | Vendor Specific | Vendor specific EEPROM |
| 128 – 255 | 128 | Reserved | Reserved for future use. G-P NVRAM; R/W under valid OEM password. |

Table 1. MIC3002 Address Map, Serial Address = A0_h

| Address(s) | | Field Size (Bytes) | Name | Description |
|------------|---------|--------------------|-----------------------------|--|
| HEX | DEC | | | |
| 00-27 | 0-39 | 40 | Alarm and Warning Threshold | High/low limits for warning and alarms; writeable using OEM p/w; read-only otherwise. |
| 28-37 | 40-55 | 16 | Reserved | Reserved – do not write; reads undefined. |
| 38-5B | 56-91 | 36 | Calibration Constants | Numerical constants for external calibration; writeable using OEM p/w; read-only otherwise. |
| 5C-5E | 92-94 | 3 | Reserved | Reserved – do not write; reads undefined. |
| 5F | 95 | 1 | Checksum | G-P NVRAM; writeable using OEM p/w; ready only otherwise. |
| 60-69 | 96-105 | 10 | Analog Data | Real time analog parameter data. |
| 6A-6D | 106-109 | 4 | Reserved | Reserved – do not write; reads undefined. |
| 6E | 110 | 1 | Control/Status Bits | Control and status bits. |
| 6F | 111 | 1 | Reserved | Reserved – do not write; reads undefined. |
| 70-71 | 112-113 | 2 | Alarm Flags | Alarm status bits; read only. |
| 72-73 | 114-115 | 2 | Reserved | Reserved – do not write; reads undefined. |
| 74-75 | 116-117 | 2 | Warning Flags | Warning status bits; read only. |
| 76-77 | 118-119 | 2 | Reserved | Reserved – do not write; reads undefined. |
| 78-7E | 120-126 | 7 | OEMPW | OEM password entry field. The OEM password location can be selected to be 78-7B (120-123) or 7B-7E (123-126) by setting the bit OEMCFG5 bit 2 to 0 (default) or 1. |
| 7F | 127 | 1 | Vendor Specific | Vendor specific. Reserved – do not write; reads undefined. |
| 80-DD | 128-221 | 94 | User Scratchpad | User writeable EEPROM. G-P NVRAM; R/W using any valid password. |
| DE | 222 | 1 | ALT_USRCTL | Alternate location for USRCTL register. Set bit OEMCFG6-2 to 1 to select this location. Can be used as a scratch pad if not selected. |
| DF-F5 | 223-245 | 23 | User Scratchpad | User writeable EEPROM. G-P NVRAM; R/W using any valid password. |
| F6 | 246 | 1 | USRPWSET | User password setting; read/write using any p/w; returns zero otherwise. |
| F7 | 247 | 1 | USRPW | User password register |
| F8-F9 | 248-249 | 2 | Alarms Masks | Bit =1: corresponding alarm not masked Bit = 0: corresponding alarm masked |
| FA-FB | 250-251 | 2 | Warnings Masks | Bit =1: corresponding warning not masked Bit = 0: corresponding warning masked |
| FC-FE | 252-254 | 3 | Reserved | Reserved – do not write; reads undefined. |
| FF | 255 | 1 | USRCTL | End-user control and status bits If ALT-USRCTL is not selected. Can be used as a scratch pad if not selected. |

Table 2. MIC3002 Address Map, Serial Address = A2_h

| Address(s) | | Field Size (Bytes) | Name | Description |
|------------|---------|--------------------|----------|---|
| HEX | DEC | | | |
| 00-3F | 0-63 | 64 | BIASLUT1 | Bias temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: 90-9B. |
| 40-7F | 64-127 | 64 | MODLUT1 | Modulation temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: A0-AB. |
| 80-BF | 128-191 | 64 | IFTLUT1 | Bias current fault threshold temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: B0-BB. |
| C0-FF | 192-255 | 64 | HATLUT1 | Bias current high alarm threshold temperature compensation L.U.T. first 64 entries. Additional 12 entries are located in A6: C0-CB. |

Table 3. Temperature Compensation Tables, Serial Address = A4_n

| Address(s) | | Field Size (Bytes) | Name | Description |
|------------|-------|--------------------|----------|---|
| HEX | DEC | | | |
| 00 | 0 | 1 | OEMCFG0 | OEM configuration register 0 |
| 01 | 1 | 1 | OEMCFG1 | OEM configuration register 1 |
| 02 | 2 | 1 | OEMCFG2 | OEM configuration register 2 |
| 03 | 3 | 1 | APCSET0 | APC setpoint register 0 |
| 04 | 4 | 1 | APCSET1 | APC setpoint register 1 |
| 05 | 5 | 1 | APCSET2 | APC setpoint register 2 |
| 06 | 6 | 1 | MODSET0 | Modulation setpoint register 0 |
| 07 | 7 | 1 | IBFLT | Bias current fault-comparator threshold. This register is temperature compensated |
| 08 | 8 | 1 | TXPFLT | TX power fault threshold |
| 09 | 9 | 1 | LOSFLT | RX LOS fault-comparator threshold |
| 0A | 10 | 1 | FLTTMR | Fault comparator timer setting |
| 0B | 11 | 1 | FLTMSK | Fault source mask bits |
| 0C-0F | 12-15 | 4 | OEMPWSET | Password for access to OEM areas |
| 10 | 16 | 1 | OEMCAL0 | OEM calibration register 0 |
| 11 | 17 | 1 | OEMCAL1 | OEM calibration register 1 |
| 12 | 18 | 1 | LUTINDX | Look-up table index read-back |
| 13 | 19 | 1 | OEMCFG3 | OEM configuration register 3 |
| 14 | 20 | 1 | APCDAC | Reads back current APC DAC value (setpoint+offset) |
| 15 | 21 | 1 | MODDAC | Reads back current modulation DAC value (setpoint+offset) |
| 16 | 22 | 1 | OEMREAD | Reads back OEM calibration data |
| 17 | 23 | 1 | LOSFLTn | LOS De-assert threshold |
| 18 | 24 | 1 | RXPOT | RXPOT tap selection |
| 19 | 25 | 1 | OEMCFG4 | OEM configuration register 4 |
| 1A | 26 | 1 | OEMCFG5 | OEM configuration register 5 |
| 1B | 27 | 1 | OEMCFG6 | OEM configuration register 6 |
| 1C-1D | 28-29 | 2 | SCRATCH | Reserved – do not write; reads undefined. |
| 1E | 30 | 1 | MODSET 1 | Modulation setpoint register 1 |
| 1F | 31 | 1 | MODSET 2 | Modulation setpoint register 2 |

| | | | | |
|-------|---------|-----|------------------|---|
| 20-27 | 32-39 | 8 | POHDATA | Power-on hour meter scratchpad |
| 28-47 | 40-71 | 32 | RXLUT | RX power calibration look-up table. Eight sets of slope and offset |
| 48-57 | 72-87 | 16 | CALCOEF | Slope and offset coefficients used for Temperature, Voltage, Bias, and TXPOWER internal calibration |
| 58-5F | 88-95 | 8 | SCRATCH | OEM scratchpad area |
| 60-86 | 96-134 | 39 | TCTRLUT | LUT to temperature-compensate temperature results and/or temperature to be used by parameters compensation LUT. |
| 87-8F | 135-143 | 9 | SCRATCH | OEM scratchpad area. |
| 90-9B | 144-155 | 12 | BIASLUT2 | Bias temperature compensation L.U.T. additional 12 entries. |
| 9C-9F | 156-159 | 4 | SCRATCH | OEM scratchpad area |
| A0-AB | 160-171 | 12 | MODLUT2 | Modulation temperature compensation L.U.T. additional 12 entries. |
| AC-AF | 172-175 | 14 | SCRATCH | OEM scratchpad area. |
| B0-BB | 176-187 | 12 | IFTLUT2 | Bias current fault threshold temperature compensation L.U.T. additional 12 entries. |
| BC-BF | 188-191 | 4 | SCRATCH | OEM scratchpad area |
| C0-CB | 192-203 | 12 | HATLUT2 | Bias current high alarm threshold temperature compensation L.U.T. additional 12 entries. |
| CC-CF | 204-207 | 4 | SCRATCH | OEM scratchpad area |
| D0-DD | 208-221 | 14 | RXLUTSEG | RXPWR calibration segments delimiters. Each of the eight segments can have its own slope and offset. |
| DE-FA | 222-250 | 128 | SCRATCH | OEM scratchpad area |
| FB-FC | 251-252 | 2 | POH | Power on hour meter result; read only |
| FD | 253 | 1 | Data Ready Flags | Data ready bits for each measured parameter; read only |
| FE | 254 | 1 | MFG_ID | Manufacturer identification (Micrel = 42 = 2Ah) |
| FF | 255 | 1 | DEV_ID | Device and die revision |

Table 4. OEM Configuration Registers, Serial Address = A6_n

Block Diagram

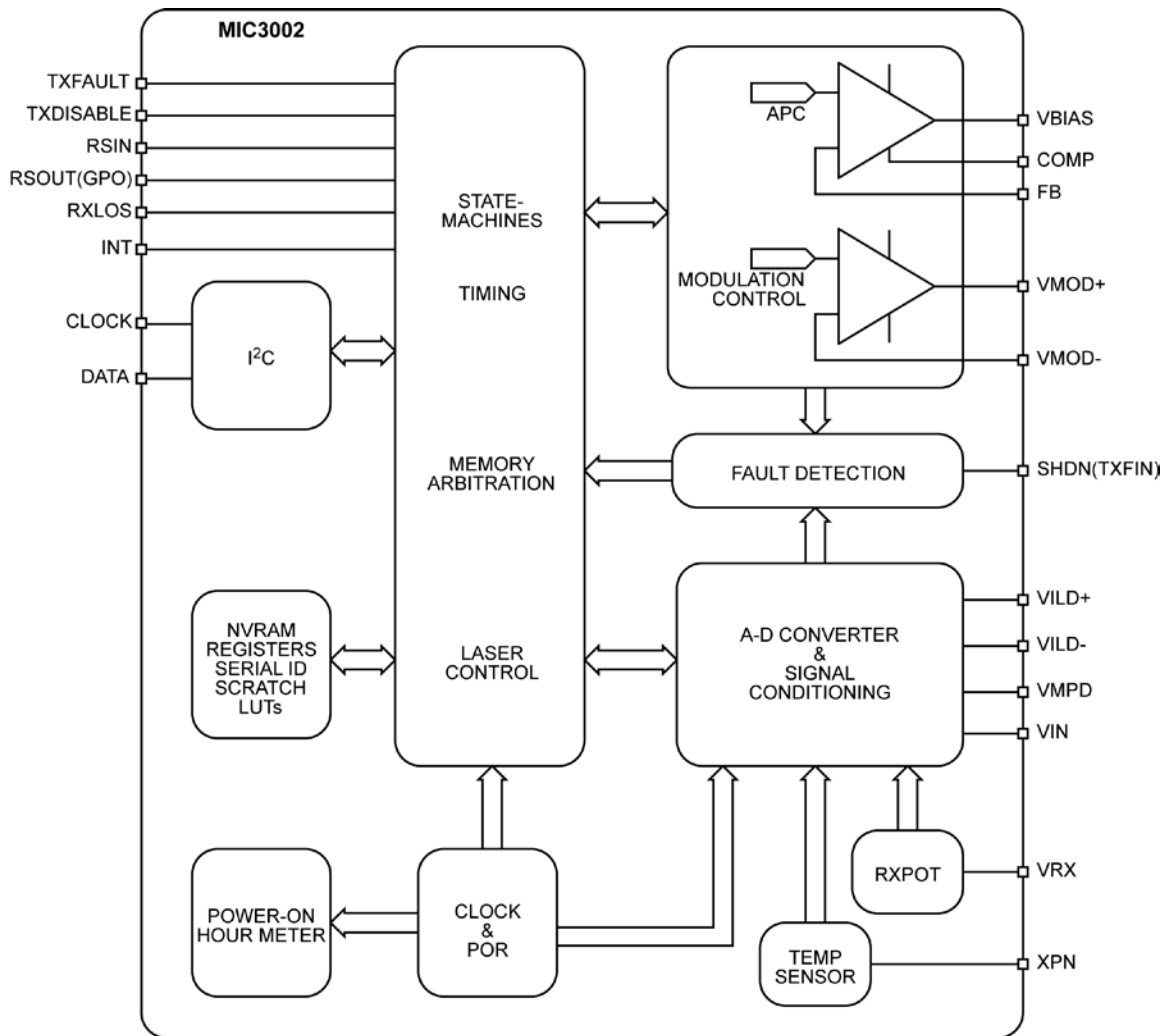


Figure 1. MIC3002 Block Diagram

Analog-to-Digital Converter/Signal Monitoring

A block diagram of the monitoring circuit is shown below. Each of the five analog parameters monitored by the MIC3002 are sampled in sequence. All five parameters are sampled and the results updated within the t_{CONV} internal given in the “Electrical Characteristics” section. In OEM_r Mode, the channel that is normally used to measure V_{IN} may be assigned to measure the level of the V_{DDA} pin or one of five other nodes. This provides a kind of analog loopback for debug and test purposes. The V_{AUX} bits in OEMCFG0 control which voltage source is being sampled. The various V_{AUX} channels are level-shifted differently depending on the signal source, resulting in different LSB values and signal ranges. See Table 5.

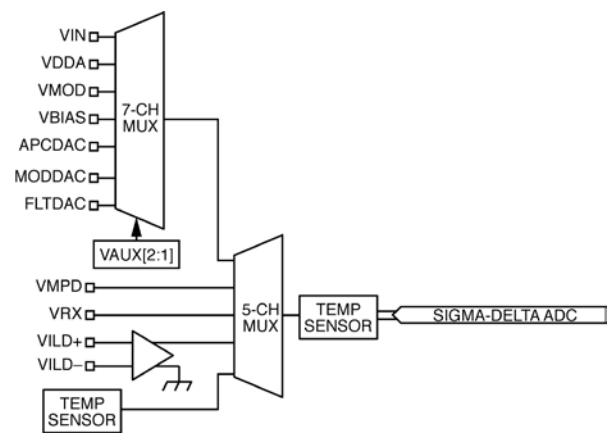


Figure 2. Analog-to-Digital Converter Block Diagram

| Channel | ADC Resolution (bits) | Conditions | Input Range (V) | LSB ⁽¹⁾ |
|---------|-----------------------|-----------------------|-----------------------------------|--------------------|
| TEMP | 8 or 9 | | N/A | 1°C or 0.5°C |
| VAUX | 8 | See Table 6 | | |
| VMPD | 8 | GAIN = 0; BIASREF = 0 | $G_{NDA} - V_{REF}$ | 4.77mV |
| | | GAIN = 0; BIASREF = 1 | $V_{DDA} - (V_{DDA} - V_{REF})$ | |
| | | GAIN = 1; BIASREF = 0 | $G_{NDA} - V_{REF}/4$ | 1.17mV |
| | | GAIN = 1; BIASREF = 1 | $V_{DDA} - (V_{DDA} - V_{REF})/4$ | |
| VILD | 8 | VILD- = VDDA | $V_{DDA} - (V_{DDA} - V_{REF})$ | 4.77mV |
| | | VILD- = GNDA | $G_{NDA} - V_{REF}$ | |
| VRX | 12 | RXPOT = 00 | 0 - V_{REF} | 0.298mV |

Table 5. A/D Input Signal Ranges and Resolutions

Note:

- Assumes typical VREF value of 1.22V.

| Channel | VAUX [2:0] | Input Range (V) | LSB ⁽¹⁾ (mV) |
|-------------------|------------------------|------------------------|-------------------------|
| V _{IN} | 000 = 00 _h | 0.5V to 5.5V | 25.6mV |
| V _{DDA} | 0001 = 01 _h | 0.5V to 5.5V | 25.6mV |
| V _{BIAS} | 010 = 02 _h | 0.5V to 5.5V | 25.6mV |
| V _{MOD} | 011 = 03 _h | 0.5V to 5.5V | 25.6mV |
| APCDAC | 100 = 04 _h | 0V to V _{REF} | 4.77mV |
| MODDAC | 101 = 05 _h | 0V to V _{REF} | 4.77mV |
| FLTDAC | 110 = 06 _h | 0V to V _{REF} | 4.77mV |

Table 6. V_{AUX} Input Signal Ranges and Resolutions**Note:**

- Assumes typical V_{REF} value of 1.22V.

Temperature Reading Compensation

The sensed temperature by the MIC3002 can be temperature compensated and converted to the optical module case temperature to be monitored or used for modulation and other parameters (L.U.T.s). There are 39 entries (bytes) at address A6: 96-134 (60-86h) where the OEM can enter the temperature difference between the chip (sensed) temperature and the measured module case temperature over the operating temperature range. Table 7 shows the correspondence between the entries and temperature intervals.

The resolution of this table is 0.5°C/bit. The number entered should be twice the temperature difference. For example if the chip-case temperature difference is 5°C, the value to be entered should be 2x5=10.

| Entry | Address | Temperature Range |
|-------|---------------|---|
| 0 | A6: 96 (60h) | $t \leq -45\text{ }^{\circ}\text{C}$ |
| 1 | A6: 97 (61h) | $-44\text{ }^{\circ}\text{C} \leq t \leq -41\text{ }^{\circ}\text{C}$ |
| 2 | A6: 98 (62h) | $-40\text{ }^{\circ}\text{C} \leq t \leq -37\text{ }^{\circ}\text{C}$ |
| | | |
| 36 | A6: 97 (61h) | $96\text{ }^{\circ}\text{C} \leq t \leq 99\text{ }^{\circ}\text{C}$ |
| 37 | A6: 97 (61h) | $100 \leq t \leq 103\text{ }^{\circ}\text{C}$ |
| 38 | A6: 134 (86h) | $t \geq 104\text{ }^{\circ}\text{C}$ |

Table 7. L.U.T. for Temperature Reading Compensation

Alarms and Warnings Interrupt Source Masking

Alarms and warnings set the flags and Interrupt when they are asserted if they are not masked (default). If an alarm or warning is masked, it will not set the Interrupt.

Table 8 shows the locations of the masking bits. The warning or alarm is masked if the corresponding bit is set to 1.

| Serial Address A2h | | Default Value | Description |
|--------------------|-----|---------------|--|
| Byte | Bit | | |
| 248 | 7 | 0 | Masking bit for Temp High Alarm interrupt source |
| | 6 | 0 | Masking bit for Temp Low Alarm interrupt source |
| | 5 | 0 | Masking bit for Voltage High Alarm interrupt source |
| | 4 | 0 | Masking bit for Voltage Low Alarm interrupt source |
| | 3 | 0 | Masking bit for Bias High Alarm interrupt source |
| | 2 | 0 | Masking bit for Bias Low Alarm interrupt source |
| | 1 | 0 | Masking bit for TX Power High Alarm interrupt source |
| | 0 | 0 | Masking bit for TX Power Low Alarm interrupt source |
| 249 | 7 | 0 | Masking bit for RX Power High Alarm interrupt source |
| | 6 | 1 | Masking bit for RX Power Low Alarm interrupt source |
| | 5 | Reserved | |
| | 4 | Reserved | |
| | 3 | Reserved | |
| | 2 | Reserved | |
| | 1 | Reserved | |
| | 0 | Reserved | |

Table 8. Alarms Interrupt Sources Masking Bits

| Serial Address A2h | | Default Value | Description |
|--------------------|-----|---------------|--|
| Byte | Bit | | |
| 250 | 7 | 0 | Masking bit for Temp High Warning interrupt source |
| | 6 | 0 | Masking bit for Temp Low Warning interrupt source |
| | 5 | 0 | Masking bit for Voltage High Warning interrupt source |
| | 4 | 0 | Masking bit for Voltage Low Warning interrupt source |
| | 3 | 0 | Masking bit for Bias High Warning interrupt source |
| | 2 | 0 | Masking bit for Bias Low Warning interrupt source |
| | 1 | 0 | Masking bit for TX Power High Warning interrupt source |
| | 0 | 0 | Masking bit for TX Power Low Warning interrupt source |
| 251 | 7 | 0 | Masking bit for RX Power High Warning interrupt source |
| | 6 | 1 | Masking bit for RX Power Low Warning interrupt source |
| | 5 | Reserved | |
| | 4 | Reserved | |
| | 3 | Reserved | |
| | 2 | Reserved | |
| | 1 | Reserved | |
| | 0 | Reserved | |

Table 9. Warnings Interrupt Sources Masking Bits

Alarms and Warnings as TXFAULT Source

Alarms and warnings are not sources for TXFAULT with the default setting. To set alarms as a TXFAULT source set OEMCFG4 bit 6 to 1. To set warnings as a TXFAULT, source set OEMCFG4 bit 7 to 1. The alarms and warnings TXFAULT sources can be masked individually in the same way shown in Tables 7 and 8.

Alarms and Warnings Latch

Alarms and warnings are latched with the default setting, i.e., the flags once asserted remain ON until the register is read or TXDSABLE is toggled. If OEMCFG4 bit 5 is set to 1, the warnings are not latched and will be set and reset with the warning condition. Reading the register or toggling TXDISABLE will clear the flag. If OEMCFG4 bit 4 is set to 1, the alarms are not latched and will be set and reset with the alarm condition. Reading the register or toggling TXDISABLE will clear the flag.

SMBus Multipart Support

If more than one MIC3002 device shares the same serial interface and multipart mode is selected on them (OEMCFG5 bit 3 = 1), then pin 7 and pin 20 become SMBus address bits 3 and 4 respectively. Therefore, the parts should have a different setting on those pins to create four address combinations based upon pin 7 and pin 20 state, (00, 01, 10, 11) where 0 is a pull down to GND and 1 is a pull up to VCC. The parts come from the factory with the same address (A0) and multipart mode OFF (OEMCFG5 bit 3 = 0). After power up, write 1 to OEMCFG5 bit 3 to turn ON multipart mode, which is done to all parts at the same time since they all respond to serial address A0 at this point. With multipart mode ON, the parts have different addresses based on the states of pins 7 and 20. Another option is to access each part individually, set their single mode address in OEMCFG2 bits [4-7] to different values and then turn OFF multipart mode to return to normal mode where the parts have new different address.

Calibration Modes

The default mode of calibration in the MIC3002 is external calibration, for which INTCAL bit (bit 0 in OEMCF3 register) is set to 0. The internal calibration mode is selected by setting INTCAL bit to 1.

A/ External Calibration

The voltage and temperature values returned by the MIC3002's A/D converter are internally calibrated. The binary values of TEMP_{Ph}:TEMP_I and VOL_{Th}:VOL_I are in the format called for by SFF-8472 under Internal Calibration.

SFF-8472 calls for a set of calibration constants to be stored by the transceiver OEM at specific non-volatile memory locations; refer to SFF-8472 specifications for memory map of calibration coefficient. The MIC3002 provides the non-volatile memory required for the storage of these constants. The Digital Diagnostic Monitoring Interface specification should be consulted for full details. Slopes and offsets are stored for use with voltage, temperature, bias current, and transmitted power measurements. Coefficients for a fourth-order polynomial are provided for use with received power measurements. The host system can retrieve these constants and use them to process the measured data.

Voltage

The voltage values returned by the MIC3002's A/D converter are internally calibrated. The binary values of VOL_{Th}:VOL_I are in the format called for by SFF-8472 under Internal Calibration. Since VIN_h:VIN_I requires no processing, the corresponding slope should be set to one and the offset to zero.

Temperature

The temperature values returned by the MIC3002's A/D converter are internally calibrated. The binary values of TEMP_{Ph}:TEMP_I are in the format called for by SFF-8472 under Internal Calibration.

Bias Current

Bias current is sensed via an external sense resistor as a voltage appearing between VILD+ and VILD-. The value returned by the A/D is therefore a voltage analogous to bias current. Bias current, IBIAS, is simply V_{VILD}/R_{SENSE} . The binary value in IBIAS_h (IBIAS_I is always zero) is related to bias current by:

$$I_{BIAS} = \frac{(0.300V) \left(\frac{IBIAS_h}{256} \right)}{R_{SENSE}} \quad (1)$$

The value of the least significant bit (LSB) of IBIAS_h is given by:

$$LSB(IBIAS_h) = \frac{0.300V}{256 \times R_{SENSE}} \text{ Amps} = \frac{300mV}{256 \times R_{SENSE}} \text{ mA} = \frac{1171.9}{R_{SENSE}} \mu\text{A} \quad (2)$$

Per SFF-8472, the value of the bias current LSB is 2 μ A. The conversion factor, "slope", needed is therefore:

$$\text{Slope} = \frac{1171.9\mu\text{A}}{512\mu\text{A} \times R_{SENSE}} = 2.289 + R_{SENSE}$$

The tolerance of the sense resistor directly impacts the accuracy of the bias current measurement. It is recommended that the sense resistor chosen be 1% accurate or better. The offset correction, if needed, can be determined by shutting down the laser, i.e., asserting TXDISABLE, and measuring the bias current. Any non-zero result gives the offset required. The offset will be equal and opposite to the result of the "zero current" measurement.

TX Power

Transmit power is sensed via a resistor carrying the monitor photodiode current. In most applications, the signal at VMPD will be feedback voltage on FB. The VMPD voltage may be measured relative to GND or V_{DDA} depending on the setting of the BIASREF bit in OEMCFG1. The value returned by the A/D is therefore a voltage analogous to transmit power. The binary value in TXOP_h (TXOP_I is always zero) is related to transmit power by:

$$P_{TX}(\text{mW}) = \frac{K \times V_{REF} \left(\frac{TXOP_h}{256} \right)}{R_{SENSE}} = \frac{K \times (1220\text{mV}) \left(\frac{TXOP_h}{256} \right)}{R_{SENSE}} \\ = \frac{K \times 4.7656 \times TXOP_h}{R_{SENSE}} \text{ mW} \quad (3)$$

For a given implementation, the value of R_{SENSE} is known. It is either the value of the external resistor or the chosen value of RFB used in the application. The constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends on the monitoring photodiode responsivity and coupling efficiency.

It should be noted that the APC circuit acts to hold the transmitted power constant. The value of transmit power reported by the circuit should only vary by a small amount as long as APC is functioning correctly.

RX Power

Received power is sensed as a voltage appearing at VRX. It is assumed that this voltage is generated by a sense resistor carrying the receiver photodiode current or by the RSSI circuit of the receiver. The value returned by the A/D is therefore a voltage analogous to received power. The binary values in RXOPh and RXOPI are related to receive power by:

$$RX(mW) = K \times VREF \times (256 \times RXOPh + RXOPI/16) / 65536 \tag{4}$$

For a given implementation, the constant, K, will likely have to be determined through experimentation or closed-loop calibration, as it depends upon the gain and efficiencies of the receiver. In SFF-8472 implementations, the external calibration constants can describe up to a fourth-order polynomial in case K is nonlinear.

B/ Internal Calibration

If the INTCAL bit in OEMCFG3 is set to 1 (internal calibration selected), the MIC3002 will process each piece of data coming out of the A/D converter before storing the result in memory. Linear slope/offset correction will be applied on a per-channel basis to the measured values for voltage, bias current, TX power, and RX power. Only compensation is applied to temperature.

The user must store the appropriate slope/offset parameters in memory at the time of transceiver calibration. In the case of RX power, a look-up table is provided that implements eight-segment piecewise-linear correction. This correction may be performed as a compensation of the receiver non-linearity over receive power level. If static slope/offset correction for RX power is desired, the eight coefficient sets can simply be made the same. The memory maps for these coefficients are shown in Tables 11 and 12. The user must enter the seven delimiters of the intervals that fit better the receiver response. The diagram in Figure 3 shows the link between the delimiters and the sets of slopes/offsets.

The slopes allow for the correction of gain errors. Each slope coefficient is an unsigned, sixteen-bit, fixed-point binary number in the format:

[mmmmmmmm.IIIIIII], where m is a data bit (5) in the most-significant byte and I is a data bit in the least significant byte

Slopes are always positive. The binary point is in between the two bytes, i.e., between bits 7 and 8. This provides a numerical range of 1/256 (0.00391) to 255.997 in steps of 1/256. The most significant byte is always stored in memory at the lower numerical address.

The offsets correct for constant errors in the measured data. Each offset is a signed, sixteen-bit, fixed-point binary number. The bit-weights of the offsets are the same as that of the final results. The sixteen-bit offsets provide a numerical range of -32768 to +32767 for voltage, bias current, transmit power, and receive power. The numerical range for the temperature offset is -32513 (-128°) to +32512 (+127°) in increments of 256 (1°). The format for offsets is:

[SmmmmmmmlIIIIII], where S is the sign bit (6) (0 = positive, 1 = negative), m is a data bit in the most-significant byte and l is a data bit in the least significant byte

The most significant byte is always stored in memory at the lower numerical address.

Calibration of voltage, bias current, and TX power are performed using the following calculation:

$$RESULTn = ADC_RESULTn \times SLOPEn + OFFSETn \tag{7}$$

Calibration of RX power is performed using the following calculation:

$$RESULT = ADC_RESULT \times SLOPE(m) + OFFSET(m) \tag{9}$$

where m represents one of the eight linearization intervals corresponding to the RX power level.

The results of these calculations are rounded to sixteen bits in length. If the seventeenth most significant bit is a one, the result is rounded up to the next higher value. If the seventeenth most significant bit is zero, the upper sixteen bits remain unchanged. The bit-weights of the offsets are the same as that of the final results. For SFF-8472 compatible applications, these bit-weights are given in Table 10.

| Parameter | Magnitude of LSB |
|--------------|------------------|
| Voltage | 100µV |
| Bias Current | 2µA |
| TX Power | 0.1µW |
| RX Power | 0.1µW |

Table 10. LSB Values of Offset Coefficients

| Address(s) | | Field Size | Name | Description |
|------------|-------|------------|-------------------|--|
| HEX | DEC | | | |
| 48-49 | 72-73 | 2 | RESERVED | Reserved. (There is no slope for temperature.) Do not write; reads undefined. |
| 4A-4B | 74-75 | 2 | RESERVED | Reserved. (There is no offset for temperature.) Do not write; reads undefined. |
| 4C-4D | 76-77 | 2 | VSLPh:VSLPI | Voltage slope; unsigned fixed-point; MSB is at lower physical address. |
| 4E-4F | 78-79 | 2 | VOFFh:VOFFI | Voltage offset; signed fixed point; MSB is at lower physical address. |
| 50-51 | 80-81 | 2 | ISLPh:ISLPI | Bias current slope; unsigned fixed-point; MSB is at lower physical address. |
| 52-53 | 82-83 | 2 | IOFFh:IOFFI | Bias current offset; signed fixed point; MSB is at lower physical address. |
| 54-55 | 84-85 | 2 | TXSLPh: TXSLPI | TX power slope; unsigned fixed-point; MSB is at lower physical address. |
| 56-57 | 86-87 | 2 | TXOFFh: TXOFFI | TX power offset; signed fixed point; MSB is at lower physical address. |

Table 11. Internal Calibration Coefficient Memory Map – Part I

| Address(s) | | Field Size | Name | Description |
|------------|-------|------------|---------------------|--|
| HEX | DEC | | | |
| 28-29 | 40-41 | 2 | RXSLP0h: RXSLP0I | RX power slope 0; unsigned fixed-point; MSB is at lower physical address. |
| 2A-2B | 42-43 | 2 | RXOFF0h: RXOFF0I | RX power offset 0; signed twos-complement; MSB is at lower physical address. |
| 2C-2D | 44-45 | 2 | RXSLP1h: RXSLP1I | RX power slope 1; unsigned fixed-point; MSB is at lower physical address. |
| 2E-2F | 46-47 | 2 | RXOFF1h: RXOFF1I | RX power offset 1; signed twos-complement; MSB is at lower physical address. |
| 30-31 | 48-49 | 2 | RXSLP2h: RXSLP2I | RX power slope 2; unsigned fixed-point; MSB is at lower physical address. |
| 32-33 | 50-51 | 2 | RXOFF2h: RXOFF2I | RX power offset 2; signed twos-complement; MSB is at lower physical address. |
| 34-35 | 52-53 | 2 | RXSLP3h: RXSLP3I | RX power slope 3; unsigned fixed-point; MSB is at lower physical address. |
| 36-37 | 54-55 | 2 | RXOFF3h: RXOFF3I | RX power offset 3; signed twos-complement; MSB is at lower physical address. |
| 38-39 | 56-57 | 2 | RXSLP4h: RXSLP4I | RX power slope 4; unsigned fixed-point; MSB is at lower physical address. |
| 3A-3B | 58-59 | 2 | RXOFF4h: RXOFF4I | RX power offset 4; signed twos-complement; MSB is at lower physical address. |
| 3C-3D | 60-61 | 2 | RXSLP5h: RXSLP5I | RX power slope 5; unsigned fixed-point; MSB is at lower physical address. |
| 3E-3F | 62-63 | 2 | RXOFF5h: RXOFF5I | RX power offset 5; signed twos-complement; MSB is at lower physical address. |
| 40-41 | 64-65 | 2 | RXSLP6h: RXSLP6I | RX power slope 6; unsigned fixed-point; MSB is at lower physical address. |
| 42-43 | 66-67 | 2 | RXOFF6h: RXOFF6I | RX power offset 6; signed twos-complement; MSB is at lower physical address. |
| 44-45 | 68-69 | 2 | RXSLP7h: RXSLP7I | RX power slope 7; signed twos-complement; MSB is at lower physical address. |
| 46-47 | 70-71 | 2 | RXOFF7h: RXOFF7I | RX power offset 7; signed fixed-point; MSB is at lower physical address. |

Table 12. Internal Calibration Coefficient Memory Map – Part II

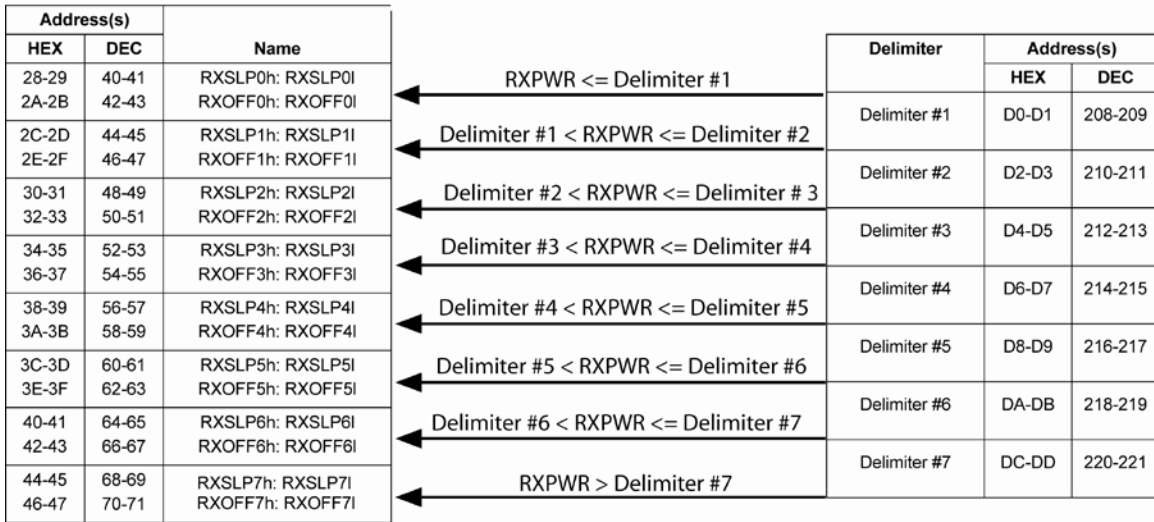


Figure 3. Internal Calibration RX Power Linear Approximation

Temperature Offset

In both internal and external calibration, the temperature offset is set in the temperature reading compensation LUT (see subsection above). Bit 5 in OMCFG5 (A6:1Ah) must be set to 1 in order to enable temperature reading compensation. Since the resolution of that L.U.T. is 0.5°C, the entered value should be twice the real value. For example, if the content of the L.U.T. is 0 for all the entries and the offset is 5°C, then the offset value to be added to the entries content is 10. The new content of the L.U.T. entries will be 0+10=10.

C/ ADC Result Registers Reading

The ADC result registers should be read as 16-bit registers under internal calibration while under external calibration they should be read as 8-bit or 16-bit registers at the MSB address. For example, TX power should be read under internal calibration as 16 bits at address A2_h: 66–67 and under external calibration as 8 bits at address A2_h: 66_h. 9-bit temperature results and 12-bit receive power results should always be read as 16-bit quantities.

RXPOT

A programmable, non-volatile digitally controlled potentiometer is provided for adjusting the gain of the receive power measurement signal chain in the analog domain. Five bits in the RXPOT register are used to set and adjust the position of potentiometer. RXPOT functions as a programmable divider or attenuator. It is adjustable in steps from 1:1 (no divider action) down to 1/32 in steps of 1/32. If RXPOT is set to zero, then the divider is bypassed completely. There will be no scaling of the input signal, and the resistor network will be disconnected from the VRX pin.

At all other settings of RXPOT, there will be a 32kΩ (typical) load seen on VRX.

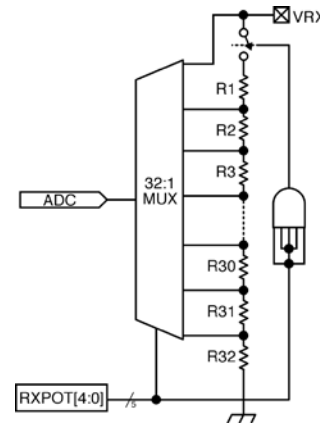


Figure 4. RXPOT Block Diagram

Laser Diode Bias Control

The MIC3002 can be configured to generate a constant bias current using electrical feedback, or regulate average transmitted optical power using a feedback signal from a monitor photodiode, refer to Figure 5. An operational amplifier is used to control laser bias current via the V_{BIAS} output. The V_{BIAS} pin can drive a maximum of ±10mA. An external bipolar transistor provides current gain. The polarity of the op amp’s output is programmable BIASREF in OMCFG1 in order to accommodate either NPN or PNP transistors that drive common anode and common cathode laser, respectively. Additionally, the polarity of the feedback signal is programmable for use with either common-emitter or emitter-follower transistor circuits.

Furthermore, the reference level for the APC circuit is selectable to accommodate electrical, i.e., current feedback, or optical feedback via a monitor photodiode. Finally, any one of seven different internal feedback resistors can be selected. This internal resistor can be used alone or in parallel with an external resistor. This wide range of adjustability (50:1) accommodates a wide range of photodiode current, i.e., wide range of transmitter output power. The APC operating point can be kept near the mid-scale value of the APC DAC, insuring maximum SNR, maximum effective resolution for digital diagnostics, and the widest possible DAC adjustment range for temperature compensation, etc. See Figure 6.

The APCCAL bit in OEMCAL0 is used to turn the APC function on and off. It will be turned off in the MIC3002's default state as shipped from the factory. When APC is on, the value in the selected APCSETx register is added to the signed value taken from the APC look-up table and loaded into the V_{BIAS} DAC. When APC is off, the V_{BIAS} DAC may be written directly via the V_{BIAS} register, bypassing the look-up table entirely. This provides direct control of the laser diode bias during setup and calibration. In either case, the V_{BIAS} DAC setting is reported in the APCDAC register. The APCCFG bits determine the DACs response to higher or lower numeric values.

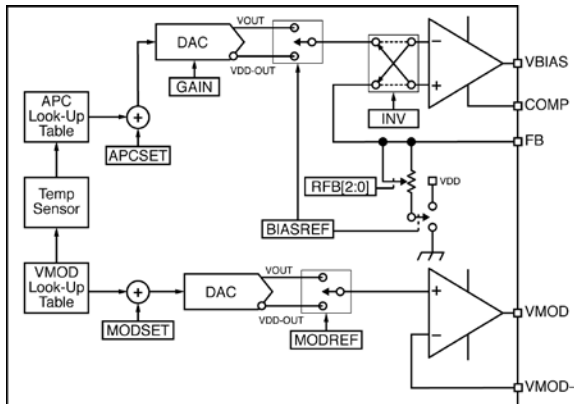


Figure 5. MIC3002 APC and Modulation Control Block Diagram

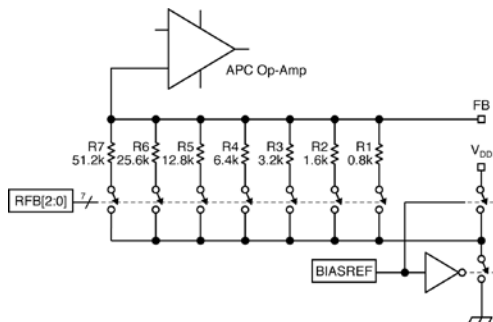


Figure 6. Programmable Feedback Resistor

Laser Modulation Control

As shown in Figure 5, a temperature-compensated DAC is provided to set and control the laser modulation current via an external laser driver circuit. MODREF in OEMCFG0 selects whether the V_{MOD} DAC output swings up from ground or down from V_{DD}. If the laser driver requires a voltage input to set the modulation current, the MIC3002's V_{MOD} output can drive it directly. If a current input is required, a fixed resistor can be used between the driver and the V_{MOD} output. Several different configurations are possible as shown in Figure 8.

When APC is on, i.e., the APCCAL bit in OEMCAL0 is set to 0, the value corresponding to the current temperature is taken from the MODLUT look-up table, added to MODSET, and loaded into the V_{MOD} DAC. When APC is off, the value in V_{MOD} is loaded directly into the V_{MOD} DAC, bypassing the look-up table entirely. This provides for direct modulation control for setup and calibration. The MODREF bit determines the DACs response to higher or lower numeric values.

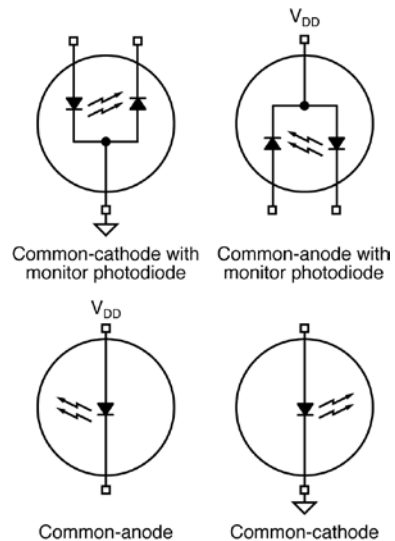


Figure 7. Transmitter Configurations Supported by MIC3002

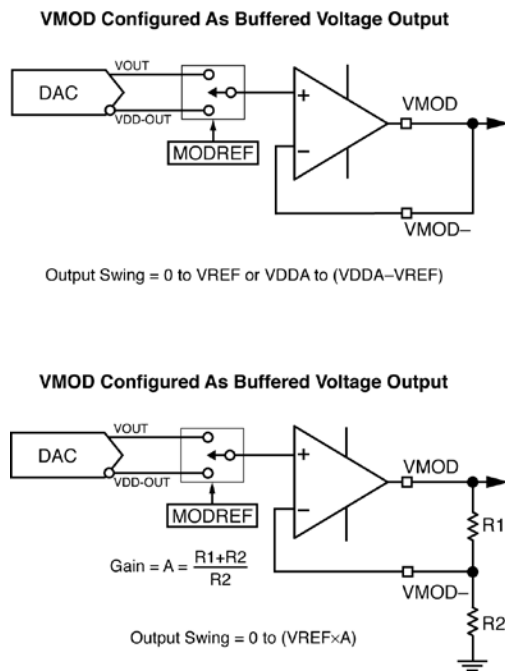


Figure 8. V_{MOD} Configured as Voltage Output with Gain

Power ON and Laser Start-Up

When power is applied, then the MIC3002 initializes its internal registers and state machine. This process takes t_{POR} , about 50ms. Following t_{POR} , analog-to-digital conversions begin, serial communication is possible, and the POR bit and data ready bits may be polled. The first set of analog data will be available t_{CONV} after t_{POR} . MIC3002s are shipped from the factory with the output enable bit, OE, set to zero, off. The MIC3002’s power-up default state, therefore, is APC off, V_{BIAS} , V_{MOD} , and SHDN outputs disabled. V_{BIAS} , V_{MOD} , and SHDN will be floating (high impedance) and the laser diode, if connected, will be off. Once the device is incorporated into a transceiver and properly configured, then the shutdown states of SHDN, V_{BIAS} and V_{MOD} will be determined by the state of the APC configuration and OE bits. Tables 13, 14, and 15 illustrate the shutdown states of the various laser control outputs versus the control bits.

| Configuration Bits | | Shutdown State |
|--------------------|------------|---------------------------|
| OE | SPOL | SHDN |
| 0 | Don't Care | Hi-Z |
| 1 | 0 | \approx GND |
| 1 | 1 | \approx V _{DD} |

Table 13. Shutdown State of SHDN vs. Configuration Bits

| Configuration Bits | | | V_{BIAS} Shutdown State |
|--------------------|------------|------------|---------------------------|
| OE | INV | BIASREF | V_{BIAS} |
| 0 | Don't Care | Don't Care | Hi-Z |
| 1 | Don't Care | 0 | \approx GND |
| 1 | Don't Care | 1 | \approx V _{DD} |

Table 14. Shutdown State of V_{BIAS} vs. Configuration Bits

| Configuration Bits | | V_{MOD} Shutdown State |
|--------------------|------------|---------------------------|
| OE | MODREF | V_{MOD} |
| 0 | Don't Care | Hi-Z |
| 1 | 0 | \approx GND |
| 1 | 1 | \approx V _{DD} |

Table 15. Shutdown State of V_{MOD} vs. Configuration Bits

In order to facilitate hot-plugging, the laser diode is not turned on until t_{INIT2} after Power-On. Following t_{INIT2} , and assuming TXDISABLE is not asserted, the DACs will be loaded with their initial values. Since t_{CONV} is much less than t_{INIT2} , the first set of analog data, including temperature, is available at t_{INIT2} . Temperature compensation will be applied to the DAC values if enabled. APC will begin if OE is asserted. (If the output enable bit, OE, is not set, the V_{MOD} , V_{BIAS} , and SHDN outputs will float indefinitely.) Figure 9 shows the power-up timing of the MIC3002. If TXDISABLE is asserted at power-up, the V_{MOD} and V_{BIAS} outputs will stay in their shutdown states following MIC3002 initialization. A/D conversions will begin, but the laser will remain off.

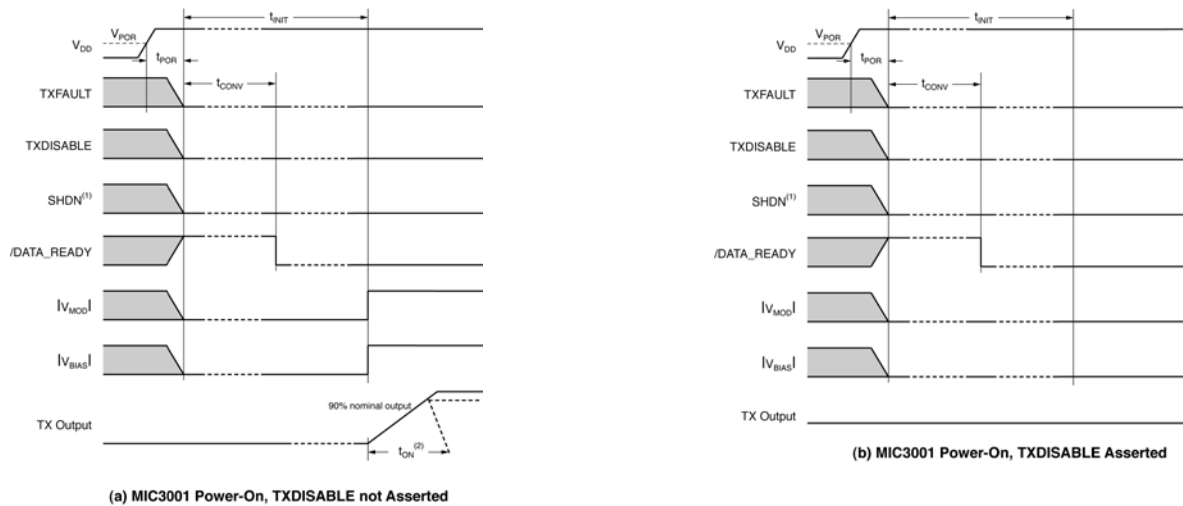


Figure 9. MIC3002 Power-On Timing (OE = 1)

Fault Comparators

In addition to detecting and reporting the events specified in SFF-8472, the MIC3002 also monitors five fault conditions: inadequate supply voltage, thermal diode faults, excessive bias current, excessive transmit power, and APC op-amp saturation. Comparators monitor these parameters in order to respond quickly to fault conditions that could indicate link failure or safety issues, see Figure 10. When a fault is detected, the laser is shut down and TXFAULT is asserted. Each fault source may be independently disabled using the FLTMSK register. FLTMSK is non-volatile, allowing faults to be masked only during calibration and testing or permanently.

Thermal diode faults are detected within the temperature measurement subsystem when an out-of-range signal is detected. A window comparator circuit monitors the voltage on the compensation capacitor to detect APC op-amp saturation (Figure 11). Op-amp saturation indicates that some fault has occurred in the control loop such as loss of feedback. The saturation detector is blanked for a time, tFLTMR, following laser turn-on since the compensation voltage will essentially be zero at turn-on. The FLTMR interval is programmable from 0.5ms to 127ms (typical) in increments of 0.5ms (tFLTMR). Note that a saturation comparator cannot be relied upon to meet certain eye-safety standards that require 100ms response times. This is because the operation of a saturation detector is limited by the loop bandwidth, i.e., the choice of CCOMP. Even if the comparator itself was very fast, it would be subject to the limited slew-rate of the APC op-amp. Only the other fault comparator channels will meet <100ms timing requirements.

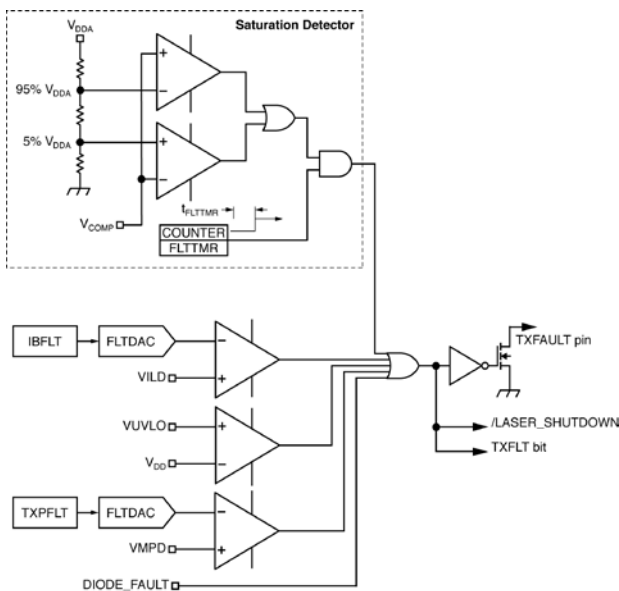


Figure 10. Fault Comparator Logic

The MIC3002 can also except and respond to fault inputs from external devices. See “SHDN and TXFIN” section.

A similar comparator circuit monitors received signal strength and asserts RXLOS when loss-of-signal is detected (Figure 12). RXLOS will be asserted when and if VRX drops below the level programmed in LOSFLT. Hysteresis is implemented such that RXLOS will be de-asserted when VRX subsequently rises above the level programmed in LOSFLTn. The loss-of-signal comparator may be disabled completely by setting the LOSDIS bit in OEMCFG3. Once the LOS comparator is disabled, an external device may drive RXLOS. The state of the RXLOS pin is reported in the CNTRL register regardless of whether it is driven by the internal comparator or by an external device. A programmable digital-to-analog converter provides the comparator reference voltages for monitoring

received signal strength, transmit power, and bias current. Glitches less than 10ms (typical) in length are rejected by the fault comparators. Since laser bias current varies greatly with temperature, there is a temperature compensation look-up table for the bias current fault DAC value.

When a fault condition is detected, the laser will be shutdown immediately and TXFAULT will be asserted. The V_{MOD} , V_{BIAS} , and SHDN if enabled, OEMCFG5-7 is set to 1, outputs will be driven to their shutdown state according to the state of the configuration bits. The shutdown states of V_{MOD} , V_{BIAS} , and SHDN versus the configuration bit settings are shown in Table 13, Table 14, and Table 15.

SHDN and TXFIN

SHDN and TXFIN are optional functions of pin 7. SHDN is an output function and is designed to drive a redundant safety switch in the laser current path. TXFIN is an input function and serves as an input for fault signals from external devices that must be reported to the host via TXFAULT. The SHDN function is designed for applications in which the MIC3002 is performing all APC and laser management tasks. The TXFIN function is for situations in which an external device such as a laser diode driver IC is performing laser management tasks, including fault detection.

If the TXFIN bit in OEMCFG3 is zero (the default mode), SHDN will be activated anytime the laser is off. Thus, it will be active if 1) TXDISABLE is asserted, 2) STXDIS in CNTRL, is set, or 3) a fault is detected. SHDN is a push-pull logic output. Its polarity is programmable via the SPOL bit in OEMCFG1.

If TXFIN is set to one, pin 7 serves as an input that accepts fault signals from external devices such as laser diode driver ICs. Multiple TXFAULT signals cannot simply be wire-ORed together as they are open-drain and active high. The input polarity is programmable via the TXFPOL bit in OEMCFG3. TXFIN is logically ORed with the MIC3002's internal fault sources to produce TXFAULT and determine the value of the transmit fault bit in CNTRL. See Figure 10.

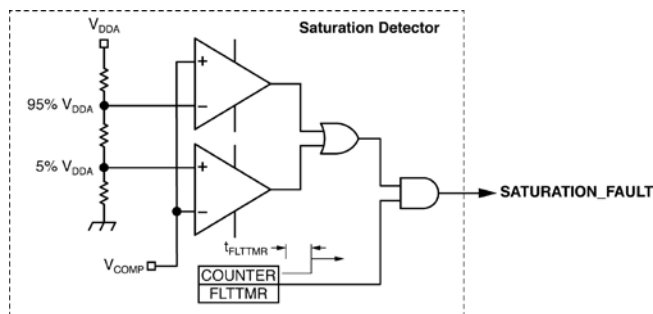


Figure 11. Saturation Detector

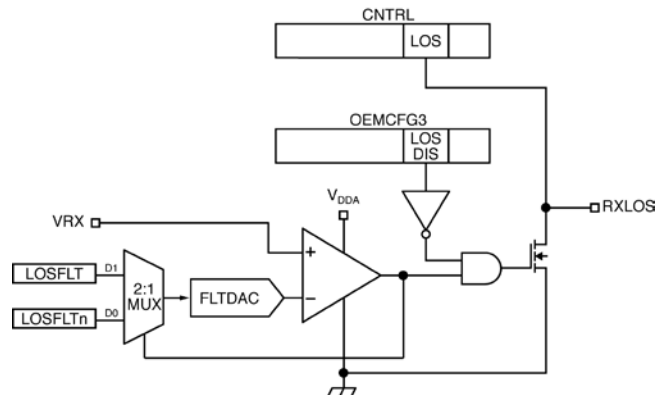


Figure 12. RXLOS Comparator Logic

Temperature Measurement

The temperature-to-digital converter for both internal and external temperature data is built around a switched current source and an eight-bit/nine-bit analog-to-digital converter. The temperature is calculated by measuring the forward voltage of a diode junction at two different bias current levels. An internal multiplexer directs the current source's output to either an internal or external diode junction. The value of the ZONE bit in OEMCFG1 determines whether readings are taken from the on-chip sensor or from the XPN input. The external PN junction may be embedded in an integrated circuit, or it may be a diode-connected discrete transistor. This data is also used as the input to the temperature compensation look-up tables. Each time temperature is sampled and an updated value acquired, new corrective values for IMOD and the APC setpoint are read from the corresponding tables, added to the set values, and transferred to the DACs.

Diode Faults

The MIC3002 is designed to respond in a failsafe manner to hardware faults in the temperature sensing circuitry. If the connection to the sensing diode is lost or the sense line is shorted to V_{DD} or ground, the temperature data reported by the A/D converter will be forced to its full-scale value (+127°C). The diode fault flag, DFLT, will be set in OEMCFG1, TXFAULT will be asserted, and the high temperature alarm and warning flags will be set. The reported temperature will remain +127°C until the fault condition is cleared. Diode faults may be reset by toggling TXDISABLE, as with any other fault. Diode faults will not be detected at power up until the first A/D conversion cycle is completed. Diode faults are not reported while TXDISABLE is asserted.

Temperature Compensation

Since the performance characteristics of laser diodes and photodiodes change with operating temperature, the

MIC3002 provides a facility for temperature compensation of the A.P.C. loop set-point, laser modulation current, bias current fault comparator threshold, and bias current high alarm flag threshold. Temperature compensation is performed using a look-up table (LUT) that stores values corresponding to each measured temperature over a 150°C span. Four identical tables reside at serial address A4h and A6h as summarized in Table 16. Each table entry is a signed twos complement number that is used as an offset to the parameter being compensated. The default value of all table entries is zero, giving a flat response.

The A/D converter reports a new temperature sample each t_{CONV} . This occurs at roughly 10Hz. To prevent temperature oscillation due to thermal or electrical noise, sixteen successive temperature samples are averaged together and used to index the L.U.T.s. Temperature compensation results are therefore updated at $16xt_{CONV}$ intervals, or about 1.6 seconds. This can be expressed as shown in Equation 10:

$$T_{COMPm} = \frac{T_n + T_{n+1} + T_{n+2} + \dots + T_{n+15}}{16} \tag{10}$$

Each time an updated average value is acquired, a new offset value for the APC setpoint is read from the corresponding look-up table (see Table 17) and transferred to the APC circuitry. This is illustrated in Equation 11. In a same way, new offset values are taken from similar look-up tables (see Table 18 and Table 19), added to the nominal values and transferred into the modulation and fault comparator DACs. The bias current high alarm threshold is compensated using a fourth look-up table (see Table 20). This compensation happens internally and does not affect any host-accessible registers.

$$\begin{aligned} APCSET_m &= APCSETx + APCLUT(T_{COMPm}) && Table_min \leq T_{COMPm} \leq Table_max \\ APCSET_m &= APCSETx + APCLUT(max) && T_{COMP} > Table_max \\ APCSET_m &= APCSETx + APCLUT(min) && T_{COMP} < Table_min \end{aligned} \tag{11}$$

If the measured temperature is greater than the maximum table value, the highest value in each table is used. If the measured temperature is less than the minimum, the minimum value is used. Hysteresis is employed to further enhance noise immunity and prevent oscillation about a table threshold. Each table entry spans two degrees C. The table index will not change unless the new temperature average results in a table index beyond the midpoint of the next entry in either direction. There is therefore 2 to 3°C of hysteresis on temperature compensation changes. The table index will never oscillate due to quantization noise as the hysteresis is much larger than $\pm 1/2$ LSB.

| Serial Address | Byte Addresses | Function |
|----------------|----------------|--|
| I2CADR+4h | 00h–3Fh | APC Look-up Table |
| | 40h–7Fh | I _{MOD} Look-up Table |
| | 80h–BFh | IFLT Look-up Table |
| | C0h–FFh | Bias High Alarm Look-up Table |
| I2CADR+6h | 90h–9Bh | APC Look-up Table (cont.) |
| | A0h–ABh | I _{MOD} Look-up Table (cont.) |
| | B0h–BBh | IFLT Look-up Table (cont.) |
| | C0h–CBh | Bias High Alarm Look-up Table (cont.) |

Table 16. Temperature Compensation Look-up Tables

| Serial Address | Register Address | Table Offset | Temperature Offset (°C) |
|----------------|------------------|--------------|-------------------------|
| I2CADR+4h | 00h | 0 | ≤ -45 |
| | 01h | 1 | -44 |
| | | | -43 |
| | | | |
| | • | • | • |
| | • | • | • |
| | • | • | • |
| | | | |
| I2CADR+6h | 3Fh | 63 | 80 81 |
| | 90h | 64 | 82 83 |
| | • | • | • |
| | • | • | • |
| I2CADR+6h | 9A | 74 | 102 103 |
| | 9B | 75 | ≥ 104 |

Table 17. APC Temperature Compensation Look-Up Table

| Serial Address | Register Address | Table Offset | Temperature Offset (°C) |
|----------------|------------------|--------------|-------------------------|
| I2CADR+4h | 80h | | ≤ -45 |
| | 81h | | -44 |
| | | | -43 |
| | 82h | | |
| | • | | |
| | • | | |
| | • | | |
| | | | |
| I2CADR+6h | 8Eh | | |
| | 8Fh | 63 | 80 81 |
| | B0 | 64 | 82 83 |
| | • | • | • |
| I2CADR+6h | • | • | • |
| | BA | 74 | 102 103 |
| | BB | 75 | ≥ 104 |

Table 19. I_{BIAS} Comparator Temperature Compensation Look-Up Table

| Serial Address | Register Address | Table Offset | Temperature Offset (°C) |
|----------------|------------------|--------------|-------------------------|
| I2CADR+4h | 40h | 0 | ≤ -45 |
| | 41h | 1 | -44 |
| | | | -43 |
| | | | |
| | • | • | • |
| | • | • | • |
| | • | • | • |
| | | | |
| I2CADR+6h | 7Fh | 63 | 80 81 |
| | A0 | 64 | 82 83 |
| | • | • | • |
| | • | • | • |
| I2CADR+6h | AA | 74 | 102 103 |
| | AB | 75 | ≥ 104 |

Table 18. V_{MOD} Temperature Compensation Look-Up Table

| Serial Address | Register Address | Table Offset | Temperature Offset (°C) |
|----------------|------------------|--------------|-------------------------|
| I2CADR+4h | C0h | | ≤ -45 |
| | C1h | | -44 |
| | | | -43 |
| | C2h | | |
| | • | | |
| | • | | |
| | • | | |
| | | | |
| I2CADR+6h | FEh | | |
| | FFh | 63 | 80 81 |
| | C0 | 64 | 82 83 |
| | • | • | • |
| I2CADR+6h | • | • | • |
| | CA | 74 | 102 103 |
| | | | 103 |

Table 20. BIAS Current High Alarm Temperature Compensation Table

The internal state machine calculates a new table index each time a new average temperature value becomes available. This table index is derived from the average temperature value. The table index is then converted into a table address for each of the four look-up tables. These operations can be expressed as:

$$\text{INDEX} = \left\lfloor \frac{T_{\text{AVG}(n)}}{2} \right\rfloor \quad (12)$$

where $T_{\text{AVG}(n)}$ is the current average temperature; and

$$\text{TABLE_ADDRESS} = \text{INDEX} + \text{BASE_ADDRESS}$$

where BASE_ADDRESS is the physical base address of each table, i.e., 00_{h} , 40_{h} , 80_{h} , or $C0_{\text{h}}$ (tables reside in the $\text{I2CADR}+4_{\text{h}}$ and $\text{I2CADR}+6_{\text{h}}$ pages of memory).

At any given time, the current table index can be read in the LUTINDX register.

Alarms and Warning Flags

There are 20 different conditions that will cause the MIC3002 to set one of the bits in the WARNx or ALARMx registers. These conditions are listed in Table 22. The less critical of these events generate warning flags by setting a bit in WARN0 or WARN1 . The more critical events cause bits to be set in ALARM0 or ALARM1 .

An event occurs when any alarm or warning condition becomes true. Each event causes its corresponding status bit in ALARM0 , ALARM1 , WARN0 , or WARN1 to be set. This action cannot be masked by the host. The status bit will remain set until the host reads that particular status register, a power on-off cycle occurs, or the host toggles TXDISABLE .

If TXDISABLE is asserted at any time during normal operation, A/D conversions continue. The A/D results for all parameters will continue to be reported. All events will be reported in the normal way. If they have not already been individually cleared by read operations, when TXDISABLE is de-asserted, all status registers will be cleared.

Control and Status I/O

The logic for the transceiver control and status I/O is shown schematically in Figure 13. Note that the internal drivers on RXLOS , RATE_SELECT , and TXFAULT are all open-drain. These signals may be driven either by the internal logic or external drivers connected to the corresponding MIC3002 pins. In any case, the signal level appearing at the pins of the MIC3002 will be reported in the control register status bits.

Note that the control bits for TX_DISABLE and RATE_SELECT and the status bits for TXFAULT and RXLOS do not meet the timing requirements as specified in the SFP MSA or the GBIC Specification, revision 5.5 (SFF-8053) for the hardware signals. The speed of the serial interface limits the rate at which these functions can be manipulated and/or reported. The response time for the control and status bits is given in the "Electrical Characteristics" subsection.

| Event | Condition | MIC3002 Response |
|--------------------------|----------------|------------------|
| Temperature high alarm | TEMP > TMAX | Set ALARM0[7] |
| Temperature low alarm | TEMP < TMIN | Set ALARM0[6] |
| Voltage high alarm | VIN > VMAX | Set ALARM0[5] |
| Voltage low alarm | VIN < VMIN | Set ALARM0[4] |
| TX bias high alarm | IBIAS > IBMAX | Set ALARM0[3] |
| TX bias low alarm | IBIAS < IBMIN | Set ALARM0[2] |
| TX power high alarm | TXOP > TXMAX | Set ALARM0[1] |
| TX power low alarm | TXOP < TXMIN | Set ALARM0[0] |
| RX power high alarm | RXOP > RXMAX | Set ALARM1[7] |
| RX power low alarm | RXOP < RXMIN | Set ALARM1[6] |
| Temperature high warning | TEMP > THIGH | Set WARN0[7] |
| Temperature low warning | TEMP < TLOW | Set WARN0[6] |
| Voltage high warning | VIN > VHIGH | Set WARN0[5] |
| Voltage low warning | VIN < VLOW | Set WARN0[4] |
| TX bias high warning | IBIAS > IBHIGH | Set WARN0[3] |
| TX bias low warning | IBIAS < IBLOW | Set WARN0[2] |
| TX power high warning | TXOP > TXHIGH | Set WARN0[1] |
| TX power low warning | TXOP < TXLOW | Set WARN0[0] |
| RX power high warning | RXOP > RXHIGH | Set WARN1[7] |
| RX power low warning | RXOP < RXLOW | Set WARN1[6] |

Table 22. MIC3002 Events

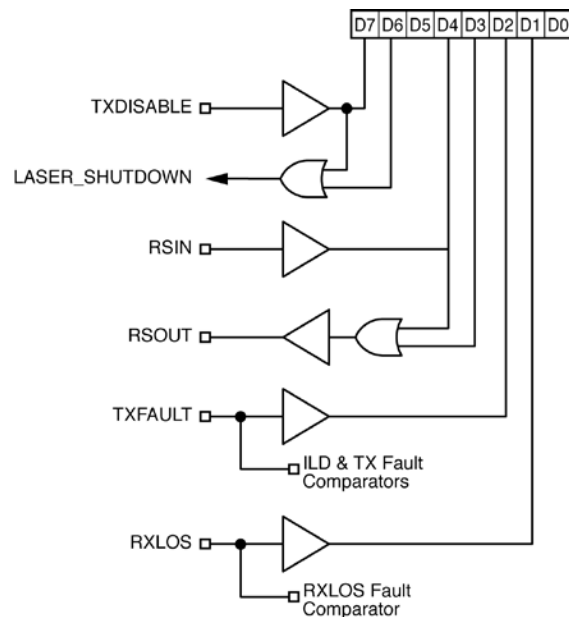


Figure 13. Control and Status I/O Logic

System Timing

The timing specifications for MIC3002 control and status

I/O are given in the “Electrical Characteristics” subsection.

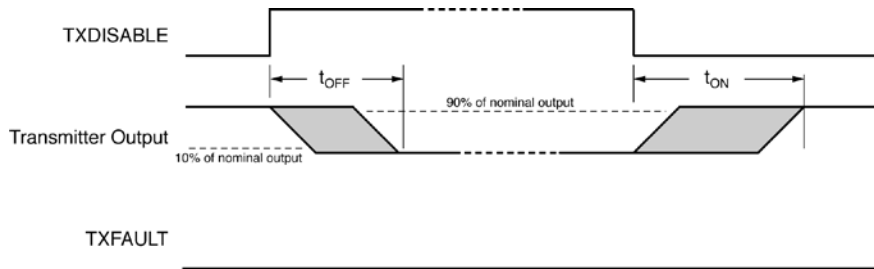


Figure 14. Transmitter ON-OFF Timing

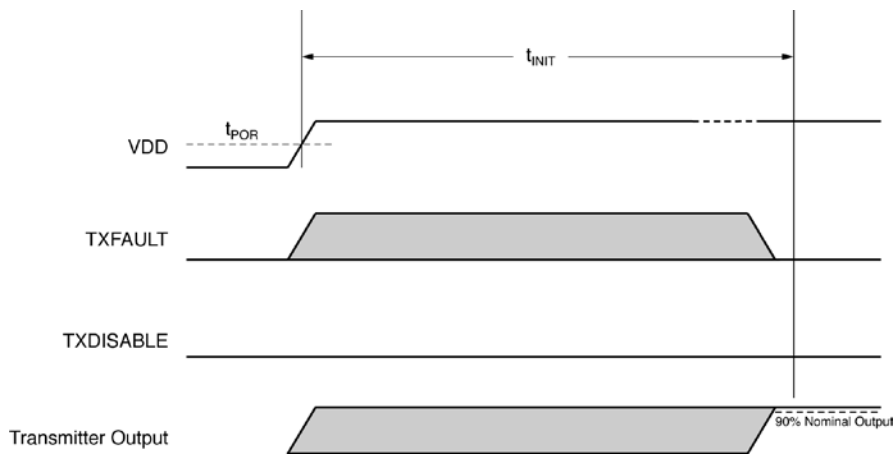


Figure 15. Initialization Timing with TXDISABLE Asserted

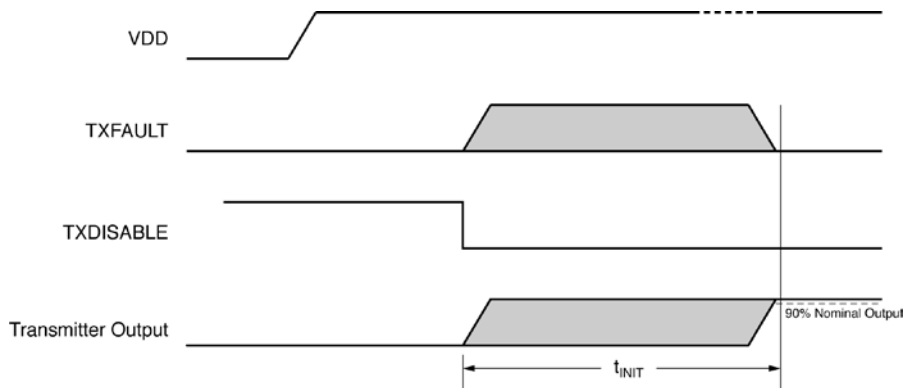


Figure 16. Initialization Timing with TXDISABLE Not Asserted

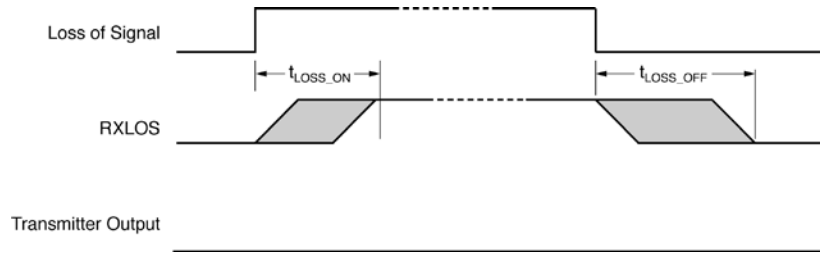


Figure 17. Loss-of-Signal (LOS) Timing

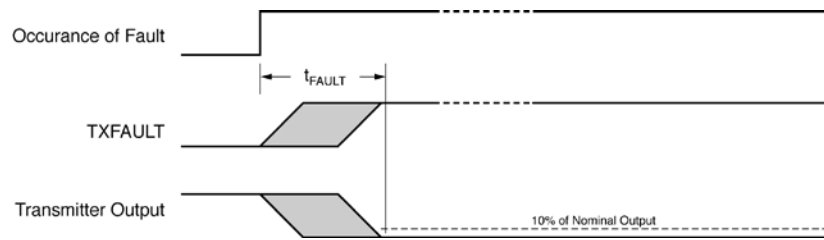


Figure 18. Transmit Fault Timing

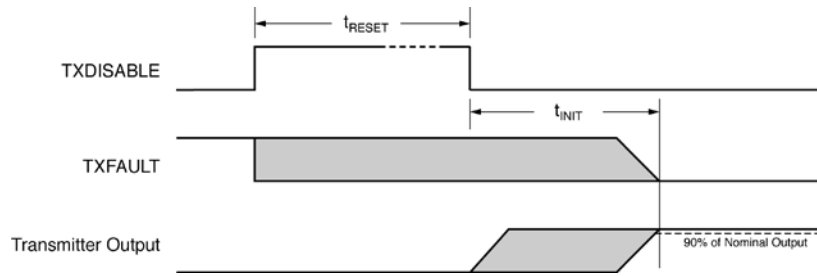


Figure 19. Successfully Clearing a Fault Condition

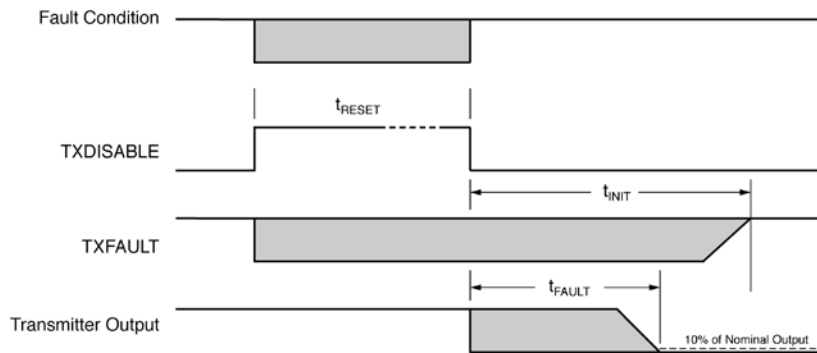


Figure 20. Unsuccessful Attempt to Clear a Fault

Warm Resets

The MIC3002 can be reset to its power-on default state during operation by setting the reset bit in OEMCFG0. When this bit is set, TXFAULT and RXLOS will be de-asserted, all registers will be restored to their normal power-on default values, and any A/D conversion in progress will be halted and the results discarded. The state of the MIC3002 following this operation is indistinguishable from a power-on reset.

Power-On Hour Meter

The Power-On Hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM. The hour count is incremented at ten-hour intervals in the middle of each interval. The first increment therefore takes place five hours after power-on. Time is accumulated whenever the MIC3002 is powered. The hour meter's time base is accurate to 5% over all MIC3002 operating conditions. The counter is capable of storing counts of more than thirty years, but is ultimately limited by the write-cycle endurance of the non-volatile

memory. This implies a range of at least twenty years. Actual results will depend upon the operating conditions and write-cycle endurance of the part in question.

Two registers, POHH and POHI, contain a 15-bit power-on hour measurement and an error flag, POHFLT. Great care has been taken to make the MIC3002's hour meter immune to data corruption and to insure that valid data is maintained across power cycles. The hour meter employs multiple data copies and error correction codes to maintain data validity. This data is stored in the POHDATA registers. If POHFLT is set, however, the power-on hour meter data has been corrupted and should be ignored.

It is recommended that a two-byte (or more) sequential read operation be performed on POHH and POHI to insure coherency between the two registers. These registers are accessible by the OEM using a valid OEM password. The only operation that should be performed on these registers is to clear the hour meters initial value, if necessary, at the time of product shipment. The hour meter result may be cleared by setting all eight POHDATA bytes to 00_h.

| Power-On Hour Result Format | | |
|-----------------------------|-------------------------------|-------------------------------|
| High Byte, POHH | | Low Byte, POHI |
| Error Flag | Elapsed Time / 10 Hours, MSBs | Elapsed Time / 10 Hours, LSBs |
| MSB | | LSB |

Table 23. Power-On Hour Meter Result Format

Test and Calibration Features

Numerous features are included in the MIC3002 to facilitate development, testing, and diagnostics. These

features are available via registers in the OEM area. As shown in Table 24, these features include:

| Function | Description | Control Register(s) |
|---------------------------------------|---|---------------------|
| Analog loop-back | Provides analog visibility of op-amp and DAC outputs via the ADC | OEMCFG0 |
| Fault comparator disable control | Disables the fault comparator | OEMCAL0 |
| Fault comparator spin-on-channel mode | Selects a single fault comparator channel | OEMCAL0 |
| Fault comparator output read-back | Allows host to read individual fault comparator outputs | OEMRD |
| RSOUT, /INT read-back | Allows host to read the state of these pins | OEMRD |
| Inhibit EEPROM write cycles | Speeds repetitive writes to registers backed up by NVRAM | OEMCAL0 |
| APC calibration mode | Allows direct writes to MODDAC and APCDAC (temperature compensation not used) | OEMCAL0 |
| Continuity checking | Forcing of RXLOS, TXFAULT, /INT | OEMCAL0 |
| Halt A/D | Stops A/D conversions; ADC in one-shot mode | OEMCAL1 |
| ADC idle flag | Indicates ADC status | OEMCAL1 |
| A/D one-shot mode | Performs a single A/D conversion on the selected input channel | OEMCAL1 |
| A/D spin-on-channel mode | Selects a single input channel | OEMCAL1 |
| Channel selection | Selects ADC or fault comparator channel for spin-on-channel modes | OEMCAL1 |
| LUT index read-back | Permits visibility of the LUT index calculated by the state-machine | LUTINDX |
| Manufacturer and device ID registers | Facilitates presence detection and version control | MFG_ID, DEV_ID |

Table 24. Test and Diagnostic Features

Serial Port Operation

The MIC3002 uses standard Write_Byte, Read_Byte, and Read_Word operations for communication with its host. It also supports Page_Write and Sequential_Read transactions. The Write_Byte operation involves sending the device's slave address (with the R/W bit low to signal a write operation), followed by the address of the register to be operated upon and the data byte. The Read_Byte operation is a composite write and read operation: the host first sends the device's slave address followed by the register address, as in a write operation. A new start bit must then be sent to the MIC3002, followed by a repeat of the slave address with the R/W bit (LSB) set to the high (read) state. The data to be read from the part may then be clocked out. A Read_Word is similar, but two successive data bytes are clocked out rather than one. These protocols are shown in Figures 21 to 24.

The MIC3002 will respond to up to four sequential slave addresses depending upon whether it is in OEM or User mode. A match between one of the MIC3002's addresses and the address specified in the serial bit stream must be made to initiate communication. The MIC3002 responds to slave addresses A0_h and A2_h in User Mode; it also responds to A4_h and A6_h in OEM Mode (assuming I2CADR = Ax_h).

Page Writes

To increase the speed of multi-byte writes, the MIC3002 allows up to four consecutive bytes (one page) to be written before the internal write cycle begins. The entire non-volatile memory array is organized into four-byte pages. Each page begins on a register address boundary where the last two bits of the address are 00_b. Thus, the page is composed of any four consecutive bytes having the addresses xxxxxx00_b, xxxxxx01_b, xxxxxx10_b, and xxxxxx11_b.

The page write sequence begins just like a Write_Byte operation with the host sending the slave address, R/W bit low, register address, etc. After the first byte is sent the host should receive an acknowledge. Up to three more bytes can be sent in sequence. The MIC3002 will acknowledge each one and increment its internal address register in anticipation of the next byte. After the last byte is sent, the host issues a STOP. The MIC3002's internal write process then begins. If more than four bytes are sent, the MIC3002's internal address counter wraps around to the beginning of the four-byte page.

To accelerate calibration and testing, NVRAM write cycles can be disabled completely by setting the WRINH bit in OEMCAL0. Writes to registers that do not have NVRAM backup, will not incur write-cycle delays when writes are inhibited. Write operations on registers that exist only in NVRAM will still incur write cycle delays.

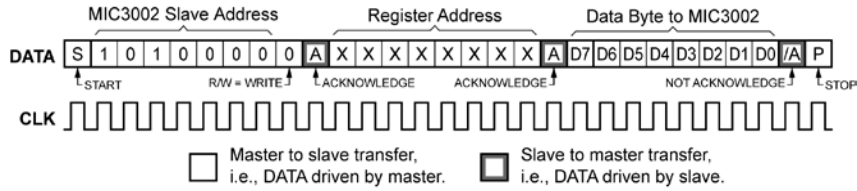


Figure 21. Write Byte Protocol

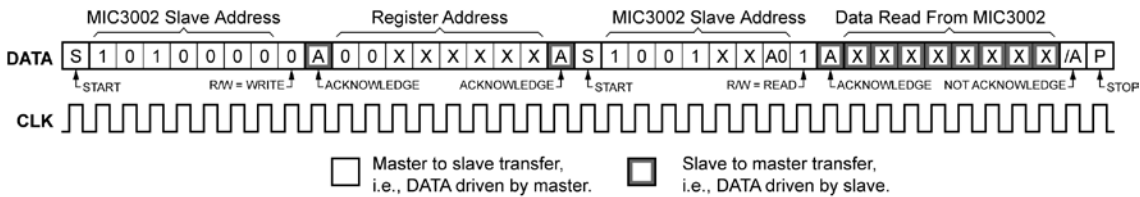


Figure 22. Read Byte Protocol

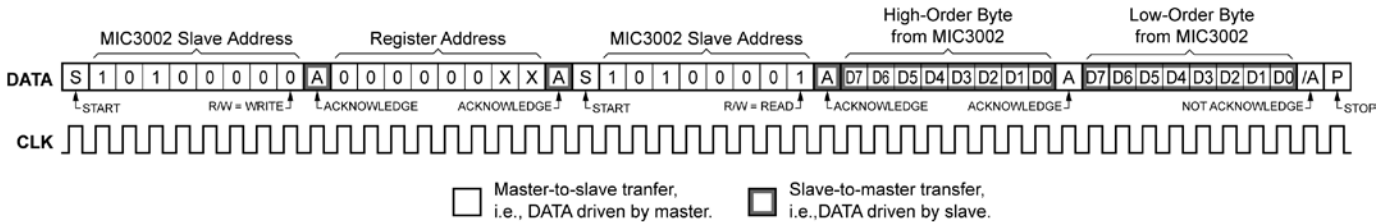


Figure 23. Read_Word Protocol

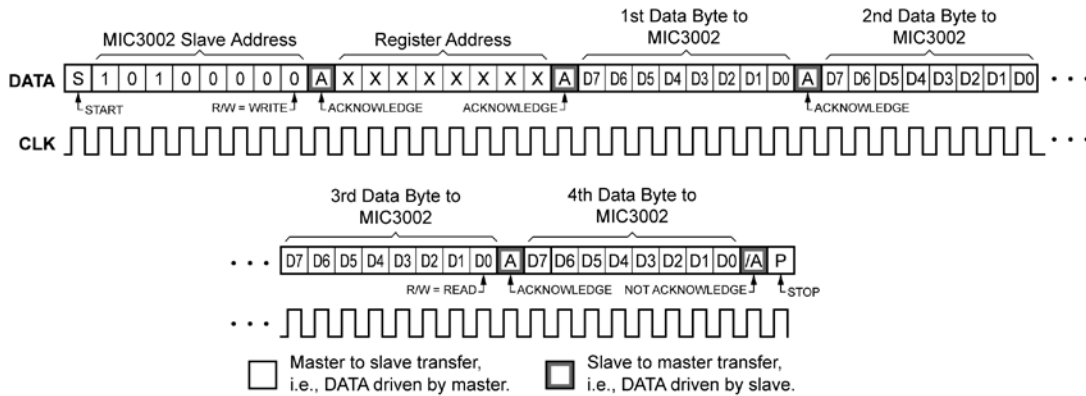


Figure 24. Four-Byte Page White Protocol

Acknowledge Polling

The MIC3002’s non-volatile memory cannot be accessed during the internal write process. To allow for maximum speed bulk writes, the MIC3002 supports acknowledge polling. The MIC3002 will not acknowledge serial bus transactions while internal writes are in progress. The host may therefore monitor for the end of the write process by periodically checking for an acknowledgement.

Write Protection and Data Security

OEM Password

A password is required to access the OEM areas of the MIC3002, specifically the non-volatile memory, look-up tables, and registers at serial addresses A4_h and A6_h. A four-byte field, OEMPWSET, at serial address A6_h is used for setting the OEM password. The OEM password is set by writing OEMPWSET with the new value. The password comparison is performed following the write to the MSB of the OEMPW, address 7B_h (or 7E_h) at serial address A2_h. Therefore, this byte must be written last. A four-byte burst-write sequence to address 78_h (or 7B_h) may be used as this will result in the MSB being written last. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect.

The corresponding four-byte field for password entry, OEMPW, is located at serial address A2_h. This field is therefore always visible to the host system. OEMPW is compared to the four-byte OEMPWSET field at serial address A6_h. If the two fields match, access is allowed to the OEM areas of the MIC3002 non-volatile memory at serial addresses A4_h and A6_h. If OEMPWSET is all zeroes, no password security will exist. The value in OEMPW will be ignored. This helps prevent a deliberately unsecured MIC3002 from being inadvertently locked. Once a valid

password is entered, the MIC3002 OEM areas will be accessible. The OEM areas may be re-secured by writing an incorrect password value at OEMPW, e.g., all zeroes. In all cases, OEMPW must be written LSB first through MSB last. The OEM areas will be inaccessible following the final write operation to OEMPW’s LSB. The OEMPW field is reset to all zeros at power on. Any values written to these locations will be readable by the host regardless of the locked/unlocked status of the device. If OEMPWSET is set to zero (00000000_h), the MIC3002 will remain unlocked regardless of the contents of the OEMPW field. This is the factory default security setting.

Note that a valid OEM password allows access to the OEM and user areas of the chip, i.e., the entire memory map, regardless of any user password that may be in place. Once the OEM areas are locked, the user password can provide access and write protection for the user areas.

User Password

A password is required to access the USER areas of the MIC3002, specifically, the non-volatile memory at serial addresses A0_h and A2_h. A one-byte field, USRPWSET at serial address A2_h is used for setting the USER password. USRPWSET is compared to the USRPW field at serial address A2_h. If the two fields match, access is allowed to the USER areas of the MIC3002 non-volatile memory at serial addresses A0_h and A2_h. The USER password is set by writing USRPWSET with the new value. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect.

Note also that a valid OEM password allows access to the OEM and user areas of the chip, i.e., the entire memory map, regardless of any user password that may be in place. Once the OEM areas are locked, the user password can then provide access and write protection for the user areas. If a valid OEM password is in place, the user password will have no effect.

Detailed Register Descriptions

Note: Serial bus addresses shown assume that I2CADR = Ax_h.

Alarm Threshold Registers

| Temperature High Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TXMAHh): 00 = 00 _h LSB (TXMAHl): 00 = 01 _h | | | | |
| <p>Each LSB of TMAXh represents one degree centigrade. This register is to be used in conjunction with TMAXl to yield a sixteen-bit temperature value.</p> <p>The value in this register is uncalibrated. The nine MSbits of threshold value (TMAXh;TMAXl) are compared bit to bit to the nine MSbits value of the temperature reading (TEMPH;TEMPI).. Alarm bit Ax is set if Reading > Threshold.</p> | | | | | | | |

| Temperature Low Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TMINh): 02 = 02 _h LSB (TMINl): 02 = 02 _h | | | | |
| <p>Each LSB of TMINh represents one degree centigrade. TMINh is to be used in conjunction with TMINl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The nine MSbits of threshold value (TMINh;TMINl) are compared, bit to bit, to The nine MSbits value of the temperature reading (TEMPH;TEMPI). Alarm bit Ax is set if Reading < Threshold.</p> | | | | | | | |

| Voltage High Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0V) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (VMAXh): 08 = 08 _h LSB (VMAXl): 09 = 09 _h | | | | |
| <p>Each LSB of VMAXh represents 25.6mV and each LSB of VMAXl represents 0.1mV. The sixteen bits threshold value (VMAXh;VMAXl) is compared bit to bit to the sixteen bits value of the voltage reading (VINh;VINl). Alarm bit Ax is set if Reading > Threshold.</p> | | | | | | | |

| Voltage Low Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0V) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (VMINh): 10 = 0A _h LSB (VMINI): 11 = 0B _h | | | | |
| Each LSB of VMINh represents 25.6mV and each LSB of VMINI represents 0.1mV. The sixteen bits threshold value (VMINh;VMINI) is compared bit to bit to the sixteen bits value of the voltage reading (VINh;VINI). Alarm bit Ax is set if Reading < Threshold. | | | | | | | |

| Bias Current High Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mA) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (IMAXh): 16 = 10 _h LSB (IMAXI): 17 = 11 _h | | | | |
| Each LSB of IMAXh represents 512μA and each LSB of IMAXI represents 2μA. The sixteen bits threshold value (IMAXh;IMAXI) is compared, bit to bit, to the sixteen bits value of the bias current reading (ILDh:ILDl). Alarm bit Ax is set if Reading > Threshold. | | | | | | | |

| Bias Current Low Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mA) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (IMINh): 18 = 12 _h LSB (IMINI): 19 = 13 _h | | | | |
| Each LSB of IMINh represents 512μA and each LSB of IMINI represents 2μA. The sixteen bits threshold value (IMINh;IMINI) is compared, bit to bit, to the sixteen bits value of the bias current reading (ILDh:ILDl). Alarm bit Ax is set if Reading < Threshold. | | | | | | | |

| TX Optical Power High Alarm | | | | | | | |
|---|--------------------|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TXMAXh): 24 = 18 _h LSB (TXMAXI): 25 = 19 _h 24 = 18 _h | | | | |
| Each LSB of TXMAXh represents 25.6μW. This register is to be used in conjunction with TXMAXI to yield a sixteen-bit value. The values in TXMAXh:TXMAXI are in an unsigned binary format. The value in this register is uncalibrated. The sixteen bits threshold value (TXMAXh;TXMAXI) is compared, bit to bit, to the sixteen bits value of the TX power reading (TXOPh:TXOPl). Alarm bit Ax is set if Reading > Threshold. | | | | | | | |

| TX Optical Power Low Alarm | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TXMAXh): 24 = 18 _h LSB (TXMAXl): 25 = 19 _h | | | | |
| <p>Each LSB of TXMINh represents 25.6μW. This register is to be used in conjunction with TXMINl to yield a sixteen-bit value. The values in TXMINh:TXMINl are in an unsigned binary format. The value in this register is uncalibrated. The sixteen bits threshold value (TXMINh;TXMINl) is compared, bit to bit, to the sixteen bits value of the RTX power reading (TXOPh:TXOPl). Alarm bit Ax is set if Reading < Threshold.</p> | | | | | | | |

| RX Optical Power High Alarm Threshold MSB (RXMAXh) | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (RXMAXh): 32 = 20 _h LSB (RXMAXl): 33 = 21 _h | | | | |
| <p>Each LSB of RXMAXh represents 25.6μW. This register is to be used in conjunction with RXMAXl to yield a sixteen-bit value. The value in this register is uncalibrated. The sixteen bits threshold value (RXMAXh;RXMAXl) is compared, bit to bit, to the sixteen bits value of the RX power reading (RXOPh:RXOPl). Alarm bit Ax is set if Reading > Threshold.</p> | | | | | | | |

| RX Optical Power Low Alarm Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (RXMINh): 34 = 22 _h LSB (RXMINl): 35 = 23 _h | | | | |
| <p>Each LSB of RXMINh represents 25.6μW. This register is to be used in conjunction with RXMINl to yield a sixteen-bit value. The value in this register is uncalibrated. The sixteen bits threshold value (RXMINh;RXMINl) is compared, bit to bit, to the sixteen bits value of the RX power reading (RXOPh:RXOPl). Alarm bit Ax is set if Reading < Threshold.</p> | | | | | | | |

Warning Threshold Registers

| Temperature High Warning Threshold | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (THIGHh): 04 = 04 _h LSB (THIGHl): 05 = 05 _h | | | | |
| Each LSB of THIGHh represents one degree centigrade. This register is to be used in conjunction with THIGHl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The nine MSbits of threshold value (THIGHh;THIGHl) are compared, bit to bit, to the nine MSbits value of the temperature reading (TEMPH;TEMPI).. Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| Temperature Low Warning Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (TLOWh): 06 = 06 _h LSB (TLOWl): 06 = 06 _h | | | | |
| Each LSB of TLOWh represents one degree centigrade. This register is to be used in conjunction with TLOWl to yield a sixteen-bit temperature value. The value in this register is uncalibrated. The threshold value (THIGHh;THIGHl) is compared, bit to bit, to the value of the temperature reading (TEMPH;TEMPI). Warning bit Wx is set if Reading < Threshold, | | | | | | | |

| Voltage High Warning Threshold | | | | | | | |
|--|--------------------|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0V) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (VHIGHh): 12 = 0C _h LSB (VHIGHl): 13 = 0D _h 12 = 0C _h | | | | |
| Each LSB of VHIGHh represents 25.6mV. This register is to be used in conjunction with VHIGHl to yield a sixteen-bit value. The value in this register is uncalibrated. The threshold value (VHIGHh;VHIGHl) is compared. bit to bit, to the value of the voltage reading (VINh;VINl). Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| Voltage Low Warning Threshold | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0V) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (VLOWh): 14 = 0E _h LSB (VLOWl): 15 = 0F _h | | | | |
| Each LSB of VLOWh represents 25.6mV. This register is to be used in conjunction with VLOWl to yield a sixteen-bit value. The value in this register is uncalibrated. The threshold value (VLOWh;VLOWl) is compared. bit to bit, to the value of the voltage reading (VINh;VINl). Warning bit Wx is set if Reading < Threshold. | | | | | | | |

| Bias Current High Warning Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mA) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (IHIGHh): 20 = 14 _h LSB (IHIGHl): 21 = 15 _h | | | | |
| Each LSB of IHIGHh represents 512μA and each LSB of IHIGHl represents 2μA. The sixteen bits threshold value (IHIGHh;IHIGHl) is compared, bit to bit, to the sixteen bits value of the bias current reading (ILDh:ILDl). Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| Bias Current Low Warning Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mA) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (ILOWh): 22 = 16 _h LSB (ILOWl): 23 = 17 _h | | | | |
| Each LSB of ILOWh represents 512μA and each LSB of ILOWl represents 2μA. The sixteen bits threshold value (ILOWh;ILOWl) is compared, bit to bit, to the sixteen bits value of the bias current reading (ILDh:ILDl). Warning bit Wx is set if Reading < Threshold. | | | | | | | |

| TX Optical Power High Warning MSB (TXHIGHh) | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Bytes Address | | | MSB (TXHIGHh): 28 = 1C _h LSB (TXHIGHl): 29 = 1D _h | | | | |
| Each LSB of TXHIGHh represents 25.6μW. This register is to be used in conjunction with TXHIGHl to yield a sixteen-bit value. The values in TXHIGHh:TXHIGHl are in an unsigned binary format. The value in this register is uncalibrated. The sixteen bits threshold value (TXHIGHh;TXHIGHl) is compared, bit to bit, to the sixteen bits value of the TX power reading (TXOPh:TXOPl). Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| TX Optical Power Low Warning | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TXLOWh): 30 = 1E _h LSB (TXLOWl): 31 = 1F _h | | | | |
| Each LSB of TXLOWh represents 25.6μW. This register is to be used in conjunction with TXLOWl to yield a sixteen-bit value. The values in TXLOWh:TXLOWl are in an unsigned binary format. The value in this register is uncalibrated. The sixteen bits threshold value (TXLOWh;TXLOWl) is compared, bit to bit, to the sixteen bits value of the TX power reading (TXOPh:TXOPl). Warning bit Wx is set if Reading < Threshold. | | | | | | | |

| RX Optical Power High Warning Threshold | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (RXHIGHh): 36 = 24 _h LSB (RXHIGHl): 37 = 25 _h | | | | |
| Each LSB of RXHIGHh represents 25.6μW and each ach LSB of RXHIGHl represents 0.1μW.. The value in this register is uncalibrated. The sixteen bits threshold value (RXHIGHh;RXHIGHl) is compared, bit to bit, to the sixteen bits value of the RX power reading (RXOPh:RXOPl). Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| RX Optical Power Low Warning Threshold | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | 38 = 26 _h | | | | |
| Each LSB of RXLOWh represents 25.6μW and each eah LSB of RXLOWl represents 0.1μW. The value in this register is uncalibrated. The sixteen bits threshold value (RXLOWh;RXLOWl) is compared, bit to bit, to the sixteen bits value of the RX power reading (RXOPh:RXOPl). Warning bit Wx is set if Reading > Threshold. | | | | | | | |

| Checksum (CHKSUM) Checksum of bytes 0 - 94 at serial address A2h | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | 95 = 5F _h | | | | |
| This register is provided for compliance with SFF-8472. It is implemented as general-purpose non-volatile memory. Read/write access is possible whenever a valid OEM password has been entered. CHKSUM is read-only in USER mode. | | | | | | | |

ADC Result Registers

| Temperature Result | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read-only | D[6] read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value | | | 0000 0000 _b = 00 _h (0°C) ⁽¹⁾ | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TEMPH): 96 = 60 _h LSB (TEMPI): 97 = 61 _h | | | | |
| Each LSB of TEMPh represents one degree centigrade. The TEMPh register is to be used in conjunction with TEMPI to yield a sixteen-bit temperature value. If OEMCFG6 bit 1 is a zero, temperature is read to 1°C resolution in TEMPh only, and TEMPI is zero. If OEMCFG6 bit 1 is a one, then temperature is read to 0.5°C resolution as a nine-bit value consisting of TEMPh and the MS bit of TEMPI. The lower seven bits of TEMPI are zero. | | | | | | | |

| Voltage | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read-only | D[6] read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value | | | 0000 0000 _b = 00 _h (0V) ⁽²⁾ | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (VINh): 98 = 62 _h LSB (VINl): 99 = 63 _h | | | | |
| Each LSB of VINh represents 25.6mV. VINh register is to be used in conjunction with VINl to yield a sixteen-bit value. The values in VINh:VINl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3002, VINl will always return zero. It is provided for compliance with SFF-8472. | | | | | | | |

Notes:

- TEMPh will contain measured temperature data after the completion of one conversion.
- VINh will contain measured data after one A/D conversion cycle.

| Laser Diode Bias Current | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read-only | D[6] read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value | | | 0000 0000 _b = 00 _h (0mA) ⁽³⁾ | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (ILDh):100 = 64 _h LSB (ILDl):100 = 65 _h | | | | |
| ILDh is to be used in conjunction with ILDI to yield a sixteen-bit value. The values in ILDh:ILDI are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration sections. In the MIC3002, ILDI will always return zero. It is provided for compliance with SFF-8472. | | | | | | | |

| Transmitted Optical Power | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read-only | D[6] read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) ⁽⁵⁾ | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (TXOPh): 102 = 66 _h LSB (TXOPl): 103 = 67 _h | | | | |
| Each LSB of TXOPh represents 25.6μW. THOPh is to be used in conjunction with TXOPl to yield a sixteen-bit value. The values in TXOPh:TXOPl are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. In the MIC3002, this TXOPl will always return zero. It is provided for compliance with SFF-8472. | | | | | | | |

Notes:

- ILDh will contain measured data after one A/D conversion cycle.
- The scale factor corresponding to the sense resistor used must be set in the configuration register.
- TXOPh will contain measured data after one A/D conversion cycle.

| Received Optical Power | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read-only | D[6] read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value | | | 0000 0000 _b = 00 _h (0mW) ⁽⁶⁾ | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | MSB (RXOPh): 104 = 68 _h LSB (RXOPI): 105 = 69 _h | | | | |
| Each LSB of RXOPI represents 25.6μW and each LSB of RXOPh represents 0.1μW. RXOPh is to be used in conjunction with RXOPI to yield a sixteen-bit value. The values in RXOPh:RXOPI are in an unsigned binary format. The value in this register is uncalibrated. The host should process the results using the scale factor and offset provided. See the External Calibration section. | | | | | | | |

| Control and Status (CNTRL) | | | | | | | |
|----------------------------|------------------------------|------------------|----------------------------|-----------------------------|--|--------------------------|--------------------------|
| D[7] TXDIS read-only | D[6] STXDIS read/write | D[5] reserved | D[4] RSEL read/write | D[3] SRSEL read/write | D[2] XFLT read-only | D[1] LOS read-only | D[0] POR read-only |
| Default Value | | | | | 0000 0000 _b = 00 _h | | |
| Serial Address | | | | | A2 _h | | |
| Byte Address | | | | | 110 = 6E _h | | |

| Bit(s) | Function | Operation |
|--------|----------|--|
| D[7] | TXDIS | Reflects the state of the TXDISABLE pin 1 = disabled, 0 = enabled, read only. |
| D[6] | STXDIS | Soft transmit disable 1 = disabled; 0 = enabled. |
| D[5] | D[5] | Reserved Reserved - always write as zero. |
| D[4] | RSEL | Reflects the state of the RSEL pin 1 = high; 0 = low. |
| D[3] | SREL | Soft rate select 1 = high (2Gbps); 0 = low (1Gbps). |
| D[2] | TXFLT | Reflects the state of the TXFAULT pin 1 = high (fault); 0 = low (no fault). |
| D[1] | LOS | Loss of signal. Reflects the state of the LOS pin 1 = high (loss of signal); 0 = low (no loss of signal). |
| D[0] | POR | MIC3002 power-on status 0 = POR complete, analog data ready; 1 = POR in progress. |

Notes:

- 6. RXOPh will contain measured data after one A/D conversion cycle.

Alarm Flags

| Alarm Status Register 0 (ALARM0) | | | | | | | |
|---|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| D[7] A7 read-only | D[6] A6 read-only | D[5] A5 read-only | D[4] A4 read-only | D[3] A3 read-only | D[2] A2 read-only | D[1] A1 read-only | D[0] A1 read-only |
| Default Value 0000 0000 _b = 00 _h (no events pending) | | | | | | | |
| Serial Address A2 _h | | | | | | | |
| Byte Address 112 = 70 _h | | | | | | | |
| The power-up default value is 00 _h . Following the first A/D conversion, however, any of the bits may be set depending upon the results. | | | | | | | |

| Bit(s) | Function | Operation |
|------------|--|--------------------------------------|
| D[7] A7 | High temperature alarm, TEMP > TMAX _h | 1 = condition exists, 0 = normal/OK. |
| D[6] A6 | Low temperature alarm, TEMP _h < TMIN | 1 = condition exists, 0 = normal/OK. |
| D[5] A5 | High voltage alarm, VIN > VMAX | 1 = condition exists, 0 = normal/OK. |
| D[4] A4 | Low voltage alarm, VIN < VMIN | 1 = condition exists, 0 = normal/OK. |
| D[3] A3 | High laser diode bias alarm, IBIAS > IMAX | 1 = condition exists, 0 = normal/OK. |
| D[2] A2 | Low laser diode bias alarm, IBIAS < IMIN | 1 = condition exists, 0 = normal/OK. |
| D[1] A1 | High transmit optical power alarm, TXOP > TXMAX | 1 = condition exists, 0 = normal/OK. |
| D[0] A0 | Low transmit optical power alarm, TXOP < TXMIN | 1 = condition exists, 0 = normal/OK. |

| Alarm Status Register 1 (ALARM1) | | | | | | | |
|---|--------------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D[7] A15 read-only | D[6] A14 read-only | D[5] reserved | D[4] reserved | D[3] reserved | D[2] reserved | D[1] reserved | D[0] reserved |
| Default Value 0000 0000 _b = 00 _h (no events pending) | | | | | | | |
| Serial Address A2 _h | | | | | | | |
| Byte Address 113 = 71 _h | | | | | | | |
| The power-up default value is 00 _h . Following the first A/D conversion, however, any of the bits may be set depending upon the results. | | | | | | | |

| Bit(s) | Function | Operation |
|-------------|--|--------------------------------------|
| D[7] A15 | High received power (overload) alarm, RXOP > RXMAX | 1 = condition exists, 0 = normal/OK. |
| D[6] A14 | Low received power (LOS) alarm, RXOP < RXMIN | 1 = condition exists, 0 = normal/OK. |
| D[5:0] | Reserved | Reserved - always write as zero. |

Warning Flags

| Warning Status Register 0 (WARN0) | | | | | | | |
|---|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| D[7] W7 read-only | D[6] W6 read-only | D[5] W5 read-only | D[4] W4 read-only | D[3] W3 read-only | D[2] W2 read-only | D[1] W1 read-only | D[0] W1 read-only |
| Default Value 0000 0000 _b = 00 _h (no events pending) | | | | | | | |
| Serial Address A2 _h | | | | | | | |
| Byte Address 116 = 74 _h | | | | | | | |
| The power-up default value is 00 _h . Following the first A/D conversion, however, any of the bits may be set depending upon the results. | | | | | | | |

| Bit(s) | Function | Operation |
|------------|--|--------------------------------------|
| D[7] W7 | High temperature warning, TEMP > THIGH | 1 = condition exists, 0 = normal/OK. |
| D[6] W6 | Low temperature warning, TEMP < TLOW | 1 = condition exists, 0 = normal/OK. |
| D[5] W5 | High voltage warning, VIN > VHIGH | 1 = condition exists, 0 = normal/OK. |
| D[4] W4 | Low voltage warning, VIN < VLOW | 1 = condition exists, 0 = normal/OK. |
| D[3] W3 | High laser diode bias warning, IBIAS > IHIGH | 1 = condition exists, 0 = normal/OK. |
| D[2] W2 | Low laser diode bias warning, IBIAS < ILOW | 1 = condition exists, 0 = normal/OK. |
| D[1] W1 | High transmit optical power warning, TXOP > TXHIGH | 1 = condition exists, 0 = normal/OK. |
| D[0] W0 | Low transmit optical power warning, TXOP < TXLOW | 1 = condition exists, 0 = normal/OK. |

| Warning Status Register 1 (WARN1) | | | | | | | |
|---|--------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| D[7] W15 read-only | D[6] W14 read-only | D[5] read-only | D[4] read-only | D[3] read-only | D[2] read-only | D[1] read-only | D[0] read-only |
| Default Value 0000 0000 _b = 00 _h (no events pending) | | | | | | | |
| Serial Address A2 _h | | | | | | | |
| Byte Address 117 = 75 _h | | | | | | | |
| The power-up default value is 00 _h . Following the first A/D conversion, however, any of the bits may be set depending upon the results. | | | | | | | |

| Bit(s) | Function | Operation |
|-------------|--|--------------------------------------|
| D[7] W15 | Received power high warning, RXOP > RXHIGH | 1 = condition exists, 0 = normal/OK. |
| D[6] W14 | Received power low warning, RXOP < RXMIN | 1 = condition exists, 0 = normal/OK. |
| D[5:0] | Reserved | Reserved - always write as zero. |

| OEM Password Entry (OEMPW) | | | | | | | |
|--|--------------------|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h (reset to zero at power-on) | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | If OEMCFG5-2 = 0: 120 – 123 = 78 _h - 7B _h (MSB is 7B _h If OEMCFG5-2 = 1: 123– 126 = 7B _h – 7E _h (MSB is 7E _h) | | | | |
| <p>This four-byte field is for entry of the password required to access the OEM area of the MIC3002's memory and registers. A valid OEM password will also permit access to the user areas of memory. The byte at address 123 (7B_h), 126 (7E_h) if OMFG5 bit2 =1, is the most significant byte. This field is compared to the four-byte OEMPWSET field at serial address A6h, bytes 12 to 15. If the two fields match, access is allowed to the OEM areas of the MIC3002 non-volatile memory at serial addresses A4_h and A6_h. The OEM password is set by writing the new value into OEMPWSET. The password comparison is performed following the write to the MSB, address 7B_h (7E_h if OEMCFG5-2 = 1). This byte must be written last!</p> <p>A four-byte burst-write sequence to address 78_h(7B_h if OEMCFG5-2 = 1) may be used as this will result in the MSB being written last. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. This field is reset to all zeros at power on. Any values written to these locations will be readable by the host regardless of the locked/unlocked status of the device. If OEMPWSET is set to zero (00000000_h), the MIC3002 will remain unlocked regardless of the contents of the OEMPW field. This is the factory default security setting.</p> | | | | | | | |

| Byte | Weight |
|------|--|
| 3 | OEM Password Entry, Most Significant Byte (Address = 7Bh resp. 7Eh) |
| 2 | OEM Password Entry, 2nd Most Significant Byte (Address = 7Ah resp. 7Dh) |
| 1 | OEM Password Entry, 2nd Least Significant Byte (Address = 79h resp. 7Ch) |
| 0 | OEM Password Entry, Least Significant Byte (Address = 78h resp. 7Bh) |

| USER Password Setting (USRPWSET) | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | 246 = F6 _h | | | | |
| <p>This register is for setting the password required to access the USER area of the MIC3002's memory and registers. This field is compared to the USRPW field at serial address A2_h, byte 247(F7h). If the two fields match, access is allowed to the USER areas of the MIC3002 non-volatile memory at serial addresses A0h and A2h. If a valid USER password has not been entered, writes to the serial ID fields, USRCTRL, and the user scratchpad areas of A0_h and A2_h will not be allowed, and USRPWSET will be unreadable (returns all zeroes).</p> <p>A USER password is set by writing the new value into USRPWSET. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. This register is non-volatile and will be maintained through power and reset cycles. A valid USER or OEM password is required for access to this register. Otherwise, this register will read as 00_h. Note: a valid OEM password overrides the USER password setting. If a valid OEM password is currently in place, the user password will have no effect.</p> | | | | | | | |

| USER Password (USRPW) | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | 247 = F7 _h | | | | |
| <p>USER passwords are entered in this field. This field is compared to the USRPWSET field at serial address A2h, byte 246 (F6h). If the two fields match, access is allowed to the USER areas of the MIC3002 non-volatile memory at serial addresses A0h and A2h. If a valid USER password has not been entered, writes to the serial ID fields and user scratchpad areas of A0h and A2h will not be allowed and USRPWSET will be unreadable (returns all zeroes).</p> | | | | | | | |

| Power-On Hours | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Bytes Address | | | MSB (POHh): 251 = FB _h LSB (POHl): 252 = FC _h | | | | |
| <p>The lower seven bits of POHh register contain the most-significant bits of the 15-bit power-on hours measurement. POHFLT is an error flag. The value in POHh should be combined with the Power-on Hours, Low Byte, POHl, to yield the complete result. If POHFLT is set, the power-on hour meter data has been corrupted and should be ignored. It is recommended that a two-byte (or more) sequential read operation be performed on POHh and POHl to insure coherency between the two registers. This register is non-volatile and will be maintained through power and reset cycle.</p> | | | | | | | |

| POHh Bit(s) | Function | Operation |
|-------------|---------------------------|--------------------------|
| D[7] | Power-on hours fault flag | 1 = fault; 0 = no fault. |
| D[6:0] | Power-on hours, high byte | Non-volatile. |

| Data Ready Flags (DATARDY) | | | | | | | |
|---|----------------------------|----------------------------|--|----------------------------|------------------|------------------|------------------|
| D[7] TRDY read/write | D[6] VRDY read/write | D[5] IRDY read/write | D[4] TXRDY read/write | D[3] RXDY read/write | D[2] reserved | D[1] reserved | D[0] reserved |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 253 = FD _h | | | | |
| <p>When the A/D conversion for a given parameter is completed and the results available to the host, the corresponding data ready flag will be set. The flag will be cleared when the host reads the corresponding result register.</p> | | | | | | | |

| Bit(s) | Function | Operation |
|--------|----------|--------------------------------|
| D[7] | TRDY | Temperature data ready flag |
| D[6] | VRDY | Voltage data ready flag |
| D[5] | IRDY | Bias current data ready flag |
| D[4] | TXRDY | Transmit power data ready flag |
| D[3] | RXRDY | Receive power data ready flag |
| D[2:0] | | Reserved |

| USER Control Register (USRCTL) | | | | | | | |
|--|----------------------------|----------------------------|--|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| D[7] read/write | D[6] PORM read/write | D[5] PORS read/write | D[4] IE read/write | D[3] APCSEL[1] read/write | D[2] APCSEL[0] read/write | D[1] MODSEL[1] read/write | D[0] MODSEL[0] read/write |
| Default Value | | | 0010 0000 _b = 20 _h | | | | |
| Serial Address | | | A2 _h | | | | |
| Byte Address | | | 255 = FF _h if OMCFG6 bit 2 = 0 222 = DE _h if OMCFG6 bit 2 = 1 | | | | |
| <p>This register provides for control of the nominal APC setpoint and management of interrupts by the end-user. APCSEL[1:0] select which of the APC setpoint registers, APCSET0, APCSET1, or APCSET2 are used as the nominal automatic power control setpoint.</p> <p>IE must be set for any interrupts to occur. If PORM is set, the power-on event will generate an interrupt and warm resets using RST will not generate a POR interrupt. When a power-on interrupt occurs, assuming PORM=1, PORS will be set. PORS will be cleared and the interrupt output de-asserted when USRCTL is read by the host. If IE is set while /INT is asserted, /INT will be de-asserted. The host must still clear the various status flags by reading them. If PORM is set following the setting of PORS, PORS will remain set, and /INT will not be de-asserted, until USRCTL is read by the host.</p> <p>PORM, IE, and APCSEL are non-volatile and will be maintained through power and reset cycles. A valid USER password is required for access to this register.</p> | | | | | | | |

| Bit | Function | Operation |
|--------|----------|--|
| D[7] | Reserved | Always write as zero; reads undefined. |
| D[6] | PORM | Power-on interrupt mask 1 = POR interrupts enabled; 0 = disabled; read/write; non-volatile. |
| D[5] | PORS | Power-on interrupt flag 1 = POR interrupt occurred; 0 = no POR interrupt; read-only. |
| D[4] | IE | Global interrupt enable 1 = enabled; 0 = disabled; read/write; non-volatile. |
| D[3:2] | APCSEL | Selects APC setpoint register 00 = APCSET0, 01 = APCSET1, 10 = APCSET2; 11 = reserved; read/write; non-volatile. |
| D[1:0] | MODSEL | Selects Modulation setpoint register 00 = MODSET0, 01 = MODSET1, 10 = MODSET2, 11 = reserved; read/write; non volatile. |

| OEM Configuration Register 0 (OEMCFG0) | | | | | | | |
|--|----------------------------|---------------------------|--|----------------------------|-------------------------------|-------------------------------|-------------------------------|
| D[7] RST write only | D[6] ZONE read/write | D[5] DFLT read only | D[4] OE reserved | D[3] MODREF reserved | D[2] VAUX[2] read/write | D[1] VAUX[1] read/write | D[0] VAUX[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 00 = 00 _h | | | | |
| <p>A write to OEMCFG0 will result in any A/D conversion in progress being aborted and the result discarded. The A/D will begin a new conversion sequence once the write operation is complete. All bits in OEMCFG0 are non-volatile except DFLT and RST. A valid OEM password is required for access to this register.</p> | | | | | | | |

| Bit(s) | Function | Operation |
|--------|----------|--|
| D[7] | RST | 0 = no action; 1 = reset; write-only. |
| D[6] | ZONE | Selects temperature zone. 0 = internal; 1 = external; non-volatile. |
| D[5] | DFLT | Diode fault flag. 1 = diode fault; 0 = OK. |
| D[4] | OE | Output enable for SHDN, V _{MOD} . 1 = enabled; 0 = hi-Z; non-volatile. |

| | | | |
|--------|-----------|---|--|
| | | and V_{BIAS} . | |
| D[3] | MODREF | Selects whether V_{MOD} is referenced to ground or V_{DD} . | 1 = V_{DD} ; 0 = GND; non-volatile. |
| D[2:0] | VAUX[2:0] | Selects the voltage reported in $V_{INh}:V_{INI}$. | 000 = V_{IN} ; 001 = V_{DDA} ; 010 = V_{BIAS} ; 011 = V_{MOD} ; 100 = APCDAC; 101 = MODDAC; 110 = FLTDAC; non-volatile |

OEM Configuration Register 1 (OEMCFG1)

| D[7] INV read/write | D[6] GAIN read/write | D[5] BIASREF read/write | D[4] RFB[2] read/write | D[3] RFB[1] read/write | D[2] RFB[0] read/write | D[1] SRCE read/write | D[0] SPOL read/write |
|---------------------------|----------------------------|-------------------------------|--|------------------------------|------------------------------|----------------------------|----------------------------|
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 1 = 01 _h | | | | |

A write to OEMCFG1 will result in any A/D conversion in progress being aborted and the result discarded. The A/D will begin a new conversion sequence once the write operation is complete. All bits in OEMCFG1 are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register.

| Bit(s) | | Function | Operation |
|--------|----------|---|--|
| D[7] | INV | Inverts the APC op-amp inputs. When set to "0" the BIAS DAC output is connected to the "+" input and FB is connected to the "-" input of the op amp. Set to "0" to use the ADC feedback loop. | 0 = emitter follower (no inversion); 1 = common emitter (inverted); read/write; non-volatile. |
| D[6] | GAIN | Sets the feedback voltage range by changing the APCDAC output swing; 0- V_{REF} for optical feedback, 0- $V_{REF}/4$ for electrical feedback. | 1 = $V_{REF}/4$ full scale; 0 = V_{REF} full scale; read/write; non-volatile. |
| D[5] | BIASREF | Selects whether FB and VMPD are referenced to ground or V_{DD} and selects feedback resistor termination voltage (V_{DDA} or GNDA). | 1 = V_{DD} ; 0 = GND; read/write; non-volatile. |
| D[4:2] | RFB[2:0] | Selects internal feedback resistance. (Resistors will be terminated to V_{DDA} or GNDA according to BIASREF.) | 000 = ∞ ; 001 = 800 Ω , 010 = 1.6k Ω , 011 = 3.2k Ω , 100 = 6.4k Ω , 101 = 12.8k Ω , 110 = 25.6k Ω , 111 = 51.2k Ω ; read/write; non-volatile. |
| D[1] | SRCE | V_{BIAS} source vs. sink drive. | 1 = source (NPN), 0 = sink (PNP); read/write; non-volatile. |
| D[0] | SPOL | Polarity of shutdown output, SHDN, when active. | 1 = high; 0 = low; read/write; non-volatile. |

| OEM Configuration Register 2 (OEMCFG2) | | | | | | | |
|---|---------------------------------|---------------------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] I2CADR[3] read/write | D[6] I2CADR[2] read/write | D[5] I2CADR[1] read/write | D[4] I2CADR[0] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 1010 xxxx _b = xx _h (slave address = 1010xxx _b) | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 2 = 02 _h | | | | |
| CAUTION: Changes to I2CADR take effect immediately! Any accesses following a write to I2CADR must be to the newly programmed serial bus address. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. | | | | | | | |

| Bit(s) | Function | Operation |
|--------|---|---------------------------|
| D[7:4] | I2CADR[3:0] Upper four MSBs of the serial bus slave address; writes take effect immediately. | Read/write; non-volatile. |
| D[3:0] | Reserved | Read/write; non-volatile. |

| APC Setpoint x (APCSETx) Automatic power control setpoint (unsigned binary) used when APCSEL[1:0] = 00 | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Bytes Address | | | APCSET0: 3 = 03 _h APCSET1: 4 = 04 _h APCSET2: 5 = 05 _h | | | | |
| When A.P.C. is on, i.e., the APCCAL bit in OEMCAL0 is set, the value in APCSETx is added to the signed value taken from the A.P.C. look-up table and loaded into the VBIAS DAC. When A.P.C. is off, the value in APCSET is loaded directly into the VBIAS DAC, bypassing the look-up table entirely. In either case, the VBIAS DAC setting is reported in the VBIAS register. The APCCFG bits determine the DAC's response to higher or lower numeric values. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. | | | | | | | |

| Modulation Setpoint x (MODSETx) Nominal V _{MOD} setpoint | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | MODSET0: 6 = 06 _h MODSET1: 30 = 1E _h MODSET2: 31 = 1F _h | | | | |
| When A.P.C. is on, the value corresponding to the current temperature is taken from the MODLUT look-up table, added to MODSET and loaded into the V _{MOD} DAC. This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register. | | | | | | | |

| I _{BIAS} Fault Threshold (IBFLT) Bias current fault threshold | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 7 = 07 _h | | | | |
| A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the bias current is higher than IBFLT value set in this register. | | | | | | | |

| Transmit Power Fault Threshold (TXFLT) | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 8 = 08 _h | | | | |
| A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the Transmit power is higher than TXFLT value set in this register. | | | | | | | |

| Loss-Of-Signal Threshold (LOSFLT) | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 9 = 09 _h | | | | |
| A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. A fault is generated if the received power is lower than LOSFLT value set in this register. | | | | | | | |

| Byte | Function | Operation |
|--------|----------------------------------|---------------------------|
| D[7:4] | Receive loss-of-signal threshold | Read/write; non-volatile. |

| Fault Suppression Timer (FLTTMR) Fault suppression interval in increments of 0.5ms | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 10 = 0A _h | | | | |
| Saturation faults are suppressed for a time, t _{FLTTMR} , following laser turn-on. This avoids nuisance tripping while the APC loop starts up. The length of this interval is (FLTTMRx 0.5ms), typical. A value of zero will result in no fault suppression. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. | | | | | | | |

| Fault Mask (FLTMSK) | | | | | | | |
|--|----------------------------|------------------|--|------------------------------|-----------------------------|-----------------------------|-----------------------------|
| D[7] OEMIM read/write | D[6] POHE read/write | D[5] reserved | D[4] reserved | D[3] SATMSK read/write | D[2] TXMSK read/write | D[1] IAMSK read/write | D[0] DFMSK read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 11 = 0B _h | | | | |
| A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. | | | | | | | |

| Bit | Function | Operation |
|--------|----------|--|
| D[7] | OEMIM | OEM interrupt mask bit 1 = masked; 0 = enabled; Read/write; non-volatile. |
| D[6] | POHE | OEM Power-on Hour Meter enable bit 1 = enabled; 0 = disabled; Read/write; non-volatile. |
| D[5:4] | D[5:4] | Reserved Always write as zero; reads undefined. |
| D[3] | SATMSK | APC saturation fault mask bit 1 = masked; 0 = enabled; Read/write; non-volatile. |
| D[2] | TXMSK | High TX optical power fault mask bit 1 = masked; 0 = enabled; Read/write; non-volatile. |
| D[1] | IAMSK | Bias current high alarm mask bit 1 = masked; 0 = enabled; Read/write; non-volatile. |
| D[0] | DFMSK | Diode fault mask bit 1 = masked; 0 = enabled; Read/write; non-volatile. |

| OEM Password Setting (OEMPWSET) | | | | | | | |
|--|--------------------|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 12 - 15 = 0C _h - 0F _h ; 0C _h = MSB | | | | |
| This four-byte field is the password required for access to the OEM area of the MIC3002's memory and registers. The byte at address 12 (0C _h) is the most significant byte. This field is compared to the four-byte OEMPW field at serial address A2 _h , byte 120 to 123 if OMCFG6-2 = 0, or byte 123 to 126 if OMCFG6-2 = 1. If the two fields match, access is allowed to the OEM areas of the MIC3002 non-volatile memory at serial addresses A4 _h and A6 _h . The OEM password may be set by writing the new value into OEMPWSET. The new password will not take effect until after a power-on reset occurs or a warm reset is performed using the RST bit in OEMCFG0. This allows the new password to be verified before it takes effect. These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register. | | | | | | | |

| Byte | Weight |
|------|--|
| 3 | OEM Password, Most Significant Byte |
| 2 | OEM Password, 2nd Most Significant Byte |
| 1 | OEM Password, 2nd Least Significant Byte |
| 0 | OEM Password, Least Significant Byte |

| OEM Calibration 0 (OEMCAL0) | | | | | | | |
|---|----------------------|---------------------|--|----------------------|----------------------|----------------------|----------------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| reserved | FLTDIS read/write | FSPIN read/write | WRINH read/write | APCCAL read/write | FRCINT read/write | FRCTXF read/write | FRCLOS read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 16 = 10 _h | | | | |
| A valid OEM password is required for access to this register. | | | | | | | |

| Bit | Function | Operation |
|------|----------|--|
| D[7] | Reserved | Always write as zero; reads undefined. |
| D[6] | FLTDIS | Fault comparator disable; inhibits output of fault comparators when set. 0 = faults enabled; 1 = disabled; Read/write. |
| D[5] | FSPIN | Fault comparator "spin-on-channel" mode select; do not enable ADC and FC spin-on-channel modes simultaneously. 0 = normal operation; 1 = spin on channel; Read/write. |
| D[4] | WRINH | Inhibit NVRAM write cycles. 0 = normal operation; 1 = inhibit writes; Read/write. |
| D[3] | APCCAL | Selects APC calibration mode - DACs may be controlled directly. 0 = normal mode; 1 = calibration mode; Read/write. |
| D[2] | FRCINT | Forces the assertion of /INT 0 = normal operation; 1 = asserted; Read/write. |
| D[1] | FRCTXF | Forces the assertion of TXFAULT 0 = normal operation; 1 = asserted; Read/write. |
| D[0] | FDCLOS | Forces the assertion of RXLOS 0 = normal operation; 1 = asserted; Read/write. |

| OEM Calibration 1 (OEMCAL1) | | | | | | | |
|---|---------------------|---------------------|--|----------------------|-----------------------|-----------------------|-----------------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| reserved | ADSTP read/write | ADIDL read/write | 1SHOT read/write | ADSPIN read/write | SPIN[2] read/write | SPIN[1] read/write | SPIN[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 17 = 11 _h | | | | |
| A valid OEM password is required for access to this register. | | | | | | | |

| Bit | Function | Operation |
|---------------------|-----------|--|
| D[7] | Reserved | Always write as zero; reads undefined. |
| D[6] | ADSTP | Stop ADC Halts the analog to digital converter 0 = normal operation; 1 = stopped; Read/write. |
| D[5] | ADIDL | ADC idle flag 0 = busy; 1 = idle; Read/write. |
| D[4] | 1SHOT | Triggers one-shot A/D conversion cycle 0 = normal operation; 1 = one-shot; Read/write. |
| D[3] | ADSPIN | Selects ADC spin-on-channel mode; do not enable ADC and FC spin-on-channel modes simultaneously 0 = normal operation; 1 = spin-on-channel; Read/write. |
| D[2], D[1], D[0] | SPIN[2:0] | ADC and fault comparator (FC) channel select for spin-on-channel mode; do not enable ADC and FC spin-on-channel modes simultaneously ADC: 000 = temperature; 001 = voltage; 010 = VILD; 011 = VMPD; 100 = VRX; FC: 001 = VILD; 001 = VMPD; 010 = VRX; Read/write. |

| OEM Calibration 1 (LUT Index) | | | | | | | |
|--|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 18 = 12 _h | | | | |
| The look-up table index is derived from the current temperature measurement as follows: INDEX = TAVG / 2 where T _{AVG} (n) is the current average temperature. This register allows the current table index to be read by the host. The table base address must be added to LUTINDEX to form a complete table index in physical memory. A valid OEM password is required for access to this register. Otherwise, reads are undefined. | | | | | | | |

| OEM Configuration 3 (OEMCFG3) | | | | | | | |
|---|------------------------------|----------------------------|--|----------------------------|-----------------------------|------------------------------|------------------------------|
| D[7] LUTSEL read/write | D[6] TXFPOL read/write | D[5] GPOD read/write | D[4] GPOM read/write | D[3] GPOC read/write | D[2] TXFIN read/write | D[1] LOSDIS read/write | D[0] INTCAL read/write |
| Default Value | | | 0000 1000 _b = 08 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 19 = 13 _h | | | | |
| This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to this register. GPOD and GPOC are ignored when GPOM = 0. TXFPOL is ignored if TXFIN = 0. | | | | | | | |

| Bit | | Function | Operation |
|------|--------|--|---|
| D[7] | LUTSEL | RX power look-up table input selection bit | 1 = RX power; 0 = temperature; read/write; ignored if INTCAL = 0. |
| D[6] | TXFPOL | TXFIN active polarity select; a fault is indicated when TXFIN = TXFPOL | 0 = active-low; 1 = active-high; read/write; ignored if TXFIN = 0. |
| D[5] | GPOD | GPO output drive | 0 = open drain; 1 = push-pull; read/write; ignored if GPOM = 0. |
| D[4] | GPOM | GPO/RSOUT mode select | 0 = RSOUT; 1 = GPO; read/write. |
| D[3] | GPOC | GPO output control | 0 = low; 1 = high; read/write; ignored if GPOM = 0. |
| D[2] | TXFIN | TXFIN mode select | 0 = SHDN; 1 = TXFIN; read/write. |
| D[1] | LOSDIS | RXLOS comparator disable | 0 = enabled; 1 = disabled; read/write. |
| D[0] | INTCAL | Calibration mode select | 0 = external calibration; 1 = internal calibration; read/write. |

| BIAS DAC Setting (APCDAC) Current VBIAS Setting | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read only | D[6] read only | D[5] read only | D[4] read only | D[3] read only | D[2] read only | D[1] read only | D[0] read only |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 20 = 14 _h | | | | |
| This register reflects (reads back) the value set in the APC register (APCSET0, APCSET1, or APCSET2 whichever is selected). A valid OEM password is required for access to this register. | | | | | | | |

| Modulation DAC Setting (MODDAC) Current VMOD Setting | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read only | D[6] read only | D[5] read only | D[4] read only | D[3] read only | D[2] read only | D[1] read only | D[0] read only |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 21 = 15 _h | | | | |
| This register reflects (reads back) the value set in the MODSET register. A valid OEM password is required for access to this register. | | | | | | | |

| OEM Readback Register (OEMRD) | | | | | | | |
|--|------------------|------------------|--|-----------------------------|----------------------------|----------------------------|----------------------------|
| D[7] reserved | D[6] reserved | D[5] reserved | D[4] INT read only | D[3] APCSAT read only | D[2] IBFLT read only | D[1] TXFLT read only | D[0] RSOUT read only |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 22 = 16 _h | | | | |
| This register reflects (reads back) the status of the bits corresponding to the parameters defined below. A valid OEM password is required for access to this register. Otherwise, reads are undefined and writes are ignored. | | | | | | | |

| Bit | Function | Operation |
|--------|----------|---|
| D[7:5] | Reserved | Always write as zero; reads undefined. |
| D[4] | INT | Mirrors state of /INT but active-high; not state of physical pin! |
| D[3] | APCSAT | APC saturation fault comparator output state |
| D[2] | IBFLT | State of IBIAS over-current fault comparator output |
| D[1] | TXFLT | State of transmit power fault comparator output |
| D[0] | RSOUT | State of the rate select output pin, RSOUT |

| Signal Detect Threshold (LOSFLTn) | | | | | | | |
|---|--------------------|--------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 23 = 17 _h | | | | |
| This register works in conjunction with the LOSFLT register to control the operation of the loss of signal comparator. The comparator's output, RXLOS, is asserted when the input on VRX falls below the level in LOSFLT. The output will then be de-asserted when the VRX signal rises above LOSFLTn. The input signal is subject to scaling by the RXPOT. If the LOS comparator is disabled, i.e., LOSDIS = 1, this register is ignored. A valid OEM password is required for access to this register. This register is non-volatile and will be maintained through power and reset cycles. | | | | | | | |

| RX EEPOT Tap Selection (RXPOT) | | | | | | | |
|--|------------------|------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] reserved | D[6] reserved | D[5] reserved | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 24 = 18 _h | | | | |
| This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | | | | | | | |

| Bit(s) | Function | Operation |
|--------|--|--|
| D[7:5] | Reserved | Reserved. Always write as zero; reads undefined. |
| D[4:0] | RXPOT tap selection: 00000 = No divider action; POT disconnected 00001 = 31/32 00010 = 30/32 • • • 11110 = 2/32 11111 = 1/32 | Read/write; non-volatile. |

| OEM Configuration 4 (OEMCFG4) | | | | | | | |
|--|------------------|------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] reserved | D[6] reserved | D[5] reserved | D[4] reserved | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 25 = 19 _h | | | | |
| This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | | | | | | | |

| Bit(s) | Function | Operation |
|--------|-----------------------------------|---|
| D[7] | Allows Warnings to assert TXFAULT | 0: Warnings do not assert TXFAULT 1: Warnings assert TXFAULT The RXPWR low warning flag does not assert TXFAULT |
| D[6] | Allows Alarms to assert TXFAULT | 0: Alarms do not assert TXFAULT 1: Alarms assert TXFAULT The RXPWR low alarm flag does not assert TXFAULT |
| D[5] | Warning Latch | 0: Warnings flags are latched. They are cleared by reading the register or toggling TXDISABLE. 1: Warnings flags are not latched., i.e. they are set and reset with alarm condition. The flags are also cleared by reading the register or toggling TXDISABLE. |
| D[4] | Alarm Latch | 0: Alarms flags are latched. They are cleared by reading the register or toggling TXDISABLE. 1: Alarms flags are not latched., i.e. they are set and reset with alarm condition. The flags are also cleared by reading the register or toggling TXDISABLE. |

| | | |
|--------------------------|---|---------------------------|
| I _{START} [3:0] | <p>I_{START} current level selection: 0000 = No I_{START} current 0001 - 1111 = 0.375mA x I_{START}[3:0] I_{START} is used to speed up the laser start-up after a fault occurs. The charging current of the compensation cap starts from I_{START} instead of ramping up from 0.</p> | Read/write; non-volatile. |
|--------------------------|---|---------------------------|

| OEM Configuration 5 (OEMCFG5) | | | | | | | |
|--|------------------|------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] reserved | D[6] reserved | D[5] reserved | D[4] reserved | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 26 = 1A _h | | | | |
| This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | | | | | | | |

| Bit(s) | Function | Operation |
|--------|---|---|
| D[7] | SHDN output enable / disable | 0: SHDN is enabled. TXFAULT will trigger SHDN output 1: SHDN is disabled. TXFAULT has no effect on SHDN output This applies when pin 7 is set as SHDN output. |
| D[6] | Temperature-compensation of the temperature used to access the L.U.T.s. | 0: The temperature used to index into the LUTs is not compensated (sensed temperature used) 1: The temperature used to index the LUTs is temperature-compensated (module case temperature used) |
| D[5] | Temperature-compensation of the temperature result in the temperature register. | 0: The temperature result in the temperature register is not compensated (sensed temperature used) 1: The temperature result in the temperature register is compensated (module case temperature used) |
| D[4] | Polarity of TXFAULT | 0: TXFAULT is active high 1: TXFAULT is active low |
| D[3] | SMBUS multipart support | 0: Multipart mode off 1: Multipart mode on |
| D[2] | OEM password location | 0: A6h 120-123 (78h-7Bh) 1: A6h 123-126 (7Bh-7Eh) |
| D[1] | SMBUS timeout enable / disable | 0: SMBUS timeout enabled 1: SMBUS timeout disabled |
| D[0] | DACs reset | 0: Clear DACs when the laser is off 1: Do not clear the DACs when laser is off |

| OEM Configuration 6 (OEMCFG6) | | | | | | | |
|--|------------------|------------------|--|--------------------|--------------------|--------------------|--------------------|
| D[7] reserved | D[6] reserved | D[5] reserved | D[4] reserved | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 27 = 1B _h | | | | |
| This register is non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | | | | | | | |

| Bit(s) | Function | Operation |
|--------|-------------------------------------|---|
| D[5-7] | Reserved | |
| D[4] | TXDISABLE debounce enable / disable | 0: TXDISABLE is not debounced 1: TXDISABLE is debounced. Glitches less than 5 ms are rejected. Set the bit to 1 if a mechanical switch is used for TXDISABLE. Set to 0 for normal operation to assure compliance to the SFP MSA. |
| D[3] | RXLOS Polarity | 0: RXLOS low for normal operation and high with a loss of signal condition. 1: RXLOS high for normal operation (signal detected) and low with a loss of signal (no signal detected) condition. |
| D[2] | USRCTRL register location | 0: A2 255 (FF _h) 1: A2 222 (DE _h) |
| D[1] | Temperature resolution | 0: Temperature is measured to a resolution of 1°C 1: Temperature is measured to a resolution of 0.5°C |
| D[0] | TXFAULT clear mode | 0: TXFAULT remains set until TXDISABLE is toggled 1: TXFAULT is in continuous mode and follows the state of the faults. |

| Power-On Hour Meter Data (POHDATA) | | | | | | | |
|---|--------------------|--------------------|---|--------------------|--------------------|--------------------|--------------------|
| D[7] read/write | D[6] read/write | D[5] read/write | D[4] read/write | D[3] read/write | D[2] read/write | D[1] read/write | D[0] read/write |
| Default Value | | | 0000 0000 _b = 00 _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 32-39 = 20 _h - 27 _h | | | | |
| These registers are used for backing up the POH result during power cycles. At power-up, the POH meter selects the larger of the two values as the initial count. Incremental results are stored in alternate register pairs. The power-on hour meter may be reset or preset by writing to these registers. These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | | | | | | | |

| Byte | Weight |
|------|-----------------|
| 3 | POHA, high-byte |
| 2 | POHA, low-byte |
| 1 | POHB, high-byte |
| 0 | POHB, low-byte |

| OEM Scratchpad Registers (SCRATCHn) | |
|--|--|
| Default Value | 0000 0000 _b = 00 _h |
| Serial Address | A6 _h |
| Byte Address | 135-143 (87-8F _h) 156-159 (9C-9F _h) 172-175 (AC-AF _h) 188-191 (BC-BF _h) 204-207 (CC-CF _h) 222-250 (DE-FA _h) |
| The scratchpad registers are general-purpose non-volatile memory locations. They can be freely read from and written to any time the MIC3002 is in OEM mode. | |

| RX Power Look-up Table (RXLUTn) | |
|---|---|
| Default Value | 0000 0000 _b = 00 _h |
| Serial Address | A6 _h |
| Byte Address | 40-71 = 28 _h - 47 _h |
| These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | |

| Bytes | Definition |
|--------------|-------------------------|
| RXSLP0h | RX Slope 0, High Byte. |
| RXSLP0l | RX Slope 0, Low Byte. |
| RXOFF0h | RX Offset 0, High Byte. |
| RXOFF0l | RX Offset 0, Low Byte. |
| RXSLP1h | RX Slope 1, High Byte. |
| RXSLP1l | RX Slope 1, Low Byte. |
| RXOFF1h | RX Offset 1, High Byte. |
| RXOFF1l | RX Offset 1, Low Byte. |
| • | • |
| • | • |
| • | • |
| RXSLP7h | RX Slope 7, High Byte. |
| RXSLP7l | RX Slope 7, Low Byte. |
| RXOFF7h | RX Offset 7, High Byte. |
| RXOFF7l | RX Offset 7, Low Byte. |

| Calibration Constants (CALn) | |
|---|---|
| Default Value | 0000 0000 _b = 00 _h |
| Serial Address | A6 _h |
| Byte Address | 74 - 87 = 4A _h - 57 _h |
| These registers are non-volatile and will be maintained through power and reset cycles. A valid OEM password is required for access to these registers. | |

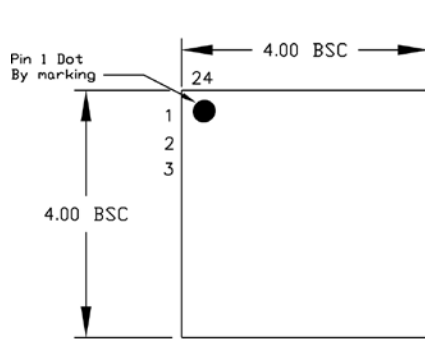
| Bytes | Definition |
|--------|---------------------------------|
| VSLP0h | Voltage Slope, High Byte. |
| VSLP0l | Voltage Slope, Low Byte. |
| VOFFh | Voltage Offset, High Byte. |
| VOFF0l | Voltage Offset, Low Byte. |
| ISLP0h | Bias Current Slope, High Byte. |
| ISLP0l | Bias Current Slope, Low Byte. |
| IOFFh | Bias Current Offset, High Byte. |
| IOFF0l | Bias Current Offset, Low Byte. |
| TXSLPh | TX Power Slope, High Byte. |
| TXSLPl | TX Power Slope, Low Byte. |
| TXOFFh | TX Power Offset, High Byte. |
| TXOFFl | TX Power Offset, Low Byte. |

| Manufacturer ID Register (MFG_ID) | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| Identifies Micrel as the manufacturer of the device. Always returns 2Ah | | | | | | | |
| D[7] read only | D[6] read only | D[5] read only | D[4] read only | D[3] read only | D[2] read only | D[1] read only | D[0] read only |
| Default Value | | | 0010 1010 _b = 2A _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 254 = FE _h | | | | |
| The value in this register, in combination with the DEV_ID register, serve to identify the MIC3002 and its revision number to software. This register is read-only. | | | | | | | |

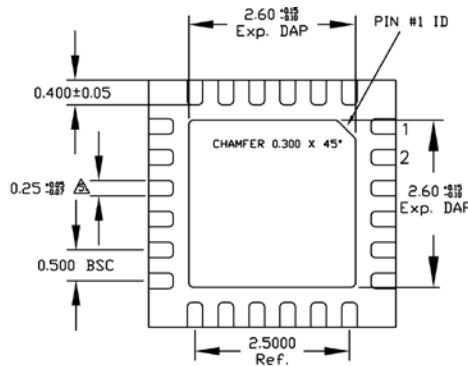
| Bit(s) | Function | Operation |
|--------|---|--|
| D[7:0] | Identifies Micrel as the manufacturer of the device. Always returns 2A _h . | Read only. Always returns A _h |

| Device ID Register (DEV_ID) | | | | | | | |
|---|-------------------|-------------------|--|-------------------|-------------------|-------------------|-------------------|
| D[7] read only | D[6] read only | D[5] read only | D[4] read only | D[3] read only | D[2] read only | D[1] read only | D[0] read only |
| MIC3002 DEVICE ID always reads 0 at D[5-7] and 1 at D[4] | | | | DIE REVISION | | | |
| Default Value | | | 0001 xxxx _b = 1x _h | | | | |
| Serial Address | | | A6 _h | | | | |
| Byte Address | | | 255 = FF _h | | | | |
| The value in this register, in combination with the MFG_ID register, serve to identify the MIC3002 and its revision number to software. This register is read-only. | | | | | | | |

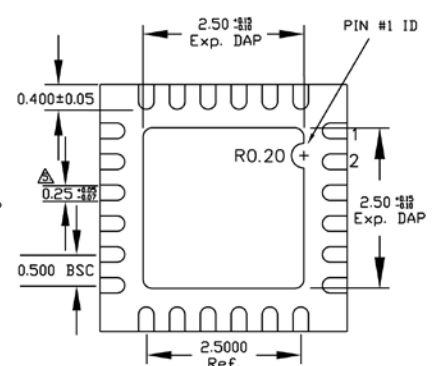
Package Information



TOP VIEW

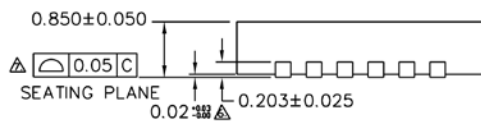


VARIATION A



VARIATION B

BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin QFN

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