

# LC898124EP1XC

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## Optical Image Stabilization (OIS) / Open-Auto Focus (AF) Controller & Driver integrating an on-chip 32-bit DSP



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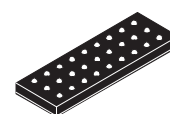
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### Over View

LC898124EP1XC is a system LSI integrating an on-chip 32-bit DSP, a EEPROM and peripherals including analog circuits for Optical Image Stabilization (OIS) / Auto Focus (AF) control and constant current drivers.

### Features

- On-chip 32-bit DSP
  - Built-in software for digital servo filter
  - Built-in software for Gyro filter
- Memory
  - EEPROM
  - ROM
  - SRAM
- Peripherals
  - AD converter : Input 4-ch
  - DA converter : Output 2-ch
  - 2-wire Serial I/F circuit (with clock stretch function)
  - Hall Bias circuit x2-ch
  - Hall Amp x2-ch
  - OSC (Oscillator)
  - LDO (Low Drop-Out regulator)
  - Digital Gyro I/F for various types of gyro (SPI Bus)
  - Interrupt I/F
- Driver
  - OIS
    - Constant current linear driver (x2-ch,  $I_{full} = 160\text{ mA}$ )
  - OP-AF(bidirection)
    - Constant current linear driver (x1-ch,  $I_{full} = 130\text{ mA}$ )
- Package
  - WLCSP27 (3.89 mm x 1.30 mm), thickness Max. 0.33 mm, with back coat
  - Pb-Free and Halogen Free compliance
- Power supply voltage
  - AD / DA / VGA / LDO / OSC : AVDD30 = 2.6 V to 3.3 V
  - Driver : VM = 2.6 V to 3.3 V



WLCSP27, 3.89x1.30, 0.4P

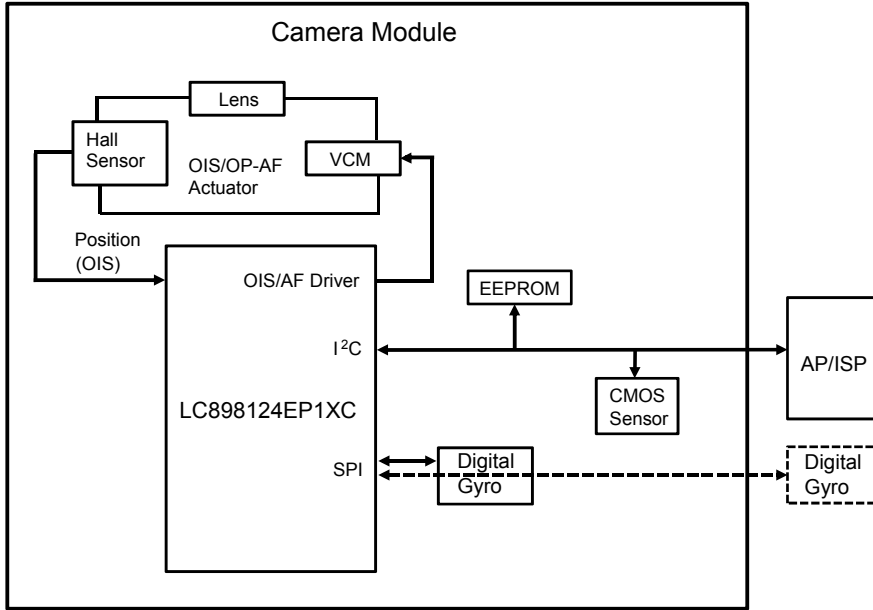
### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.



# LC898124EP1XC

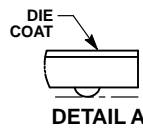
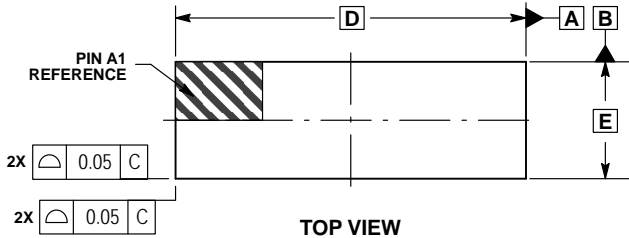
## Application Diagram



## Package Dimensions

unit : mm

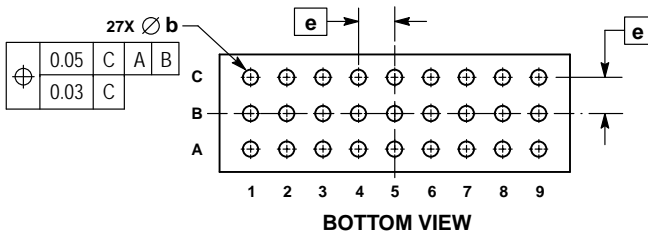
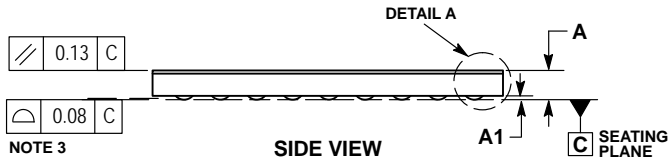
**WLCSP27, 3.89x1.30, 0.4P**  
CASE 567NJ  
ISSUE O



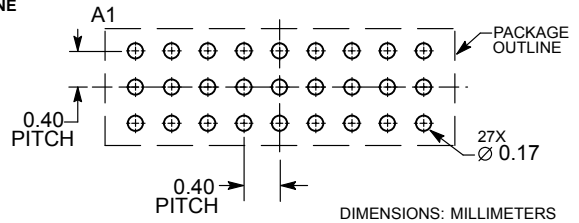
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	—	0.33
A1	0.04 REF	
b	0.12	0.22
D	3.89 BSC	
E	1.30 BSC	
e	0.40 BSC	



### RECOMMENDED SOLDERING FOOTPRINT\*







\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# LC898124EP1XC

## Pin Assign

bottom view

C	OUT4	OUT3	OUT2	OUT1	OPINPX	HLXBO	MON2	EIRQ	DGDATA
B	VM	PGND	OPINPY	OPINMY	OPINMX	HLYBO	SDA2	SDA	DGSCCLK
A	OUT5	OUT6	AVSS	AVDD30	LDPO	MON1	SCL2	SCL	DGSSB
	1	2	3	4	5	6	7	8	9

	Driver
	VDD/VSS
	Internal VDD Output
	1.8 V I/O

# LC898124EP1XC

## Pin Description

No.	Pin	I/O	I/O Spec		Primary Function	Sub Functions	Init
1	MON1	B			Servo Monitor Analog In/Out	2-wire serial Data Interrupt Input	Z
2	MON2	B			Servo Monitor Analog In/Out	2-wire serial Clock	Z
3	SCL	B		OD	2-wire serial HOST I/F Clock Slave		Z
4	SDA	B		OD	2-wire serial HOST I/F Data Slave		Z
5	SDA2	B			NC		Z
6	SCL2	B			NC		Z
7	DGSSB	B			Digital Gyro Data I/F Chip Select Out (3/4-wire Master)	3/4-wire I/F Chip Select In (Read only)	Z
8	DGSCLK	B			Digital Gyro Data I/F Clock Out (3/4-wire Master)	3/4-wire I/F Clock In (Read only)	Z
9	EIRQ	B		OD	Interrupt Input	Digital Gyro Data I/F Data In (4-wire Master)	Z
10	DGDATA	B			Digital Gyro Data I/F Data (3-wire Master)	Digital Gyro Data I/F Data Out (4-wire Master) 3/4-wire I/F Data In (Read only)	Z
11	HLXBO	O			OIS Hall X Bias Output		Z
12	HLYBO	O			OIS Hall Y Bias Output		Z
13	OPINMX	I			OIS Hall X Opamp Input Minus		Z
14	OPINPX	I			OIS Hall X Opamp Input Plus		-
15	OPINMY	I			OIS Hall Y Opamp Input Minus		-
16	OPINPY	I			OIS Hall Y Opamp Input Plus		-
17	OUT1	O			OIS Driver Output		Z
18	OUT2	O			OIS Driver Output		Z
19	OUT3	O			OIS Driver Output		Z
20	OUT4	O			OIS Driver Output		Z
21	OUT5	O			Open-AF Driver Output		Z
22	OUT6	O			Open-AF Driver Output		Z
23	AVDD30	P			Analog Power (2.6 V to 3.3 V)		-
24	AVSS	P			Analog GND		-
25	VM	P			Driver Power (2.6 V to 3.3 V)		-
26	PGND	P			Driver GND		
27	LDPO	P			Internal LDO Power Output		

# LC898124EP1XC

## Electrical Characteristics

**Absolute Maximum Rating** at AVSS = 0 V, PGND = 0 V (Note 1)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V <sub>AD30</sub> max	T <sub>a</sub> ≤ 25°C	-0.3 to +4.6	V
	V <sub>M</sub> max	T <sub>a</sub> ≤ 25°C	-0.3 to +4.6	V
Input / Output voltage	V <sub>AI30</sub> , V <sub>AO30</sub>	T <sub>a</sub> ≤ 25°C	-0.3 to V <sub>AD30</sub> +0.3	V
	V <sub>MI30</sub> , V <sub>MO30</sub>	T <sub>a</sub> ≤ 25°C	-0.3 to V <sub>M30</sub> +0.3	V
Input voltage	V <sub>I8</sub> *1	T <sub>a</sub> ≤ 25°C	-0.3 to +1.98	V
Storage temperature	T <sub>stg</sub>		-55 to +125	°C
Operating temperature	Topr1	Read for EEPROM	-30 to +85	°C
	Topr2	Program & Erase for EEPROM	-30 to +70	°C

\*1 : DGSSB, DGCLK, DGDATA, EIRQ

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Allowable Operating Ratings** at T<sub>a</sub> = -30 to 85°C, AVSS = 0 V, PGND = 0 V (Note 2)

### 3.0 V Power Supply (AVDD30)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V <sub>AD30</sub>	2.6	2.8	3.3	V
Input voltage range	V <sub>INA</sub>	0	-	V <sub>AD30</sub>	V

### 3.0 V Power Supply (VM)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V <sub>M30</sub>	2.6	2.8	3.3	V
Input voltage range	V <sub>INM</sub>	0	-	V <sub>M30</sub>	V

Note 2 : Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**D.C. Characteristics [Input/Output]** at T<sub>a</sub> = -30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.6 to 3.3 V (Note 3)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable pins
High-level input voltage	V <sub>IH</sub>	CMOS schmitt	1.26			V	DGSSB, DGCLK, DGDATA, EIRQ
Low-level input voltage	V <sub>IL</sub>		0.4			V	
High-level input voltage	V <sub>IH</sub>	CMOS schmitt	1.4			V	SCL, SDA
Low-level input voltage	V <sub>IL</sub>		0.4			V	
High-level input voltage	V <sub>IH</sub>	CMOS schmitt	0.75 AVDD30			V	MON1, MON2,
Low-level input voltage	V <sub>IL</sub>		0.25 AVDD30			V	
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	1.51		1.89	V	DGSSB, DGCLK DGDATA
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.2	V	DGSSB, DGCLK DGDATA, EIRQ
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	AVDD30 -0.3			V	MON1, MON2
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA			0.3	V	
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA			0.2	V	SCL, SDA
Analog input voltage	V <sub>AI</sub>		AVSS		AVDD30	V	MON1, MON2
Pull Up resistor	R <sub>up</sub>		50		250	kΩ	DGSSB, DGCLK DGDATA, MON1, MON2
Pull Down resistor	R <sub>dn</sub>		50		220	kΩ	DGSSB, DGCLK, DGDATA, EIRQ, MON1, MON2

Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## LC898124EP1XC

**Driver output** at Ta = 25°C, V<sub>SS</sub> = 0 V, PGND = 0 V, AVDD = VM = 2.8 V

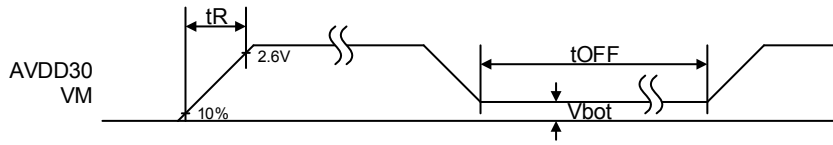
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	I <sub>full</sub>	Full code		160		mA
Output Current OUT5, OUT6		Full Code OP-AF (bidirection)		130		mA

### Non-volatile Memory Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable circuit
Endurance	EN				1000	Cycles	EEPROM
Data retention	RT		10			Years	
Write time	t <sub>WT</sub>				20	ms	

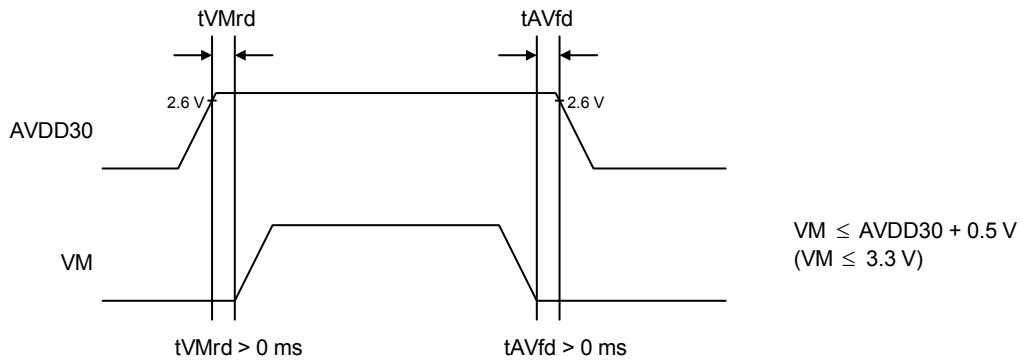
# LC898124EP1XC

## AC Characteristics Power Sequence



Item	Symbol	Min	Typ	Max	Units
Rise time	$t_R$			3	ms
Wait time	$t_W$	100			ms
Bottom Voltage	$V_{bot}$			0.2	V

Injection order between AVDD30 and VM is below.



SDA, SCL tolerate 3 V input at the time of power off.

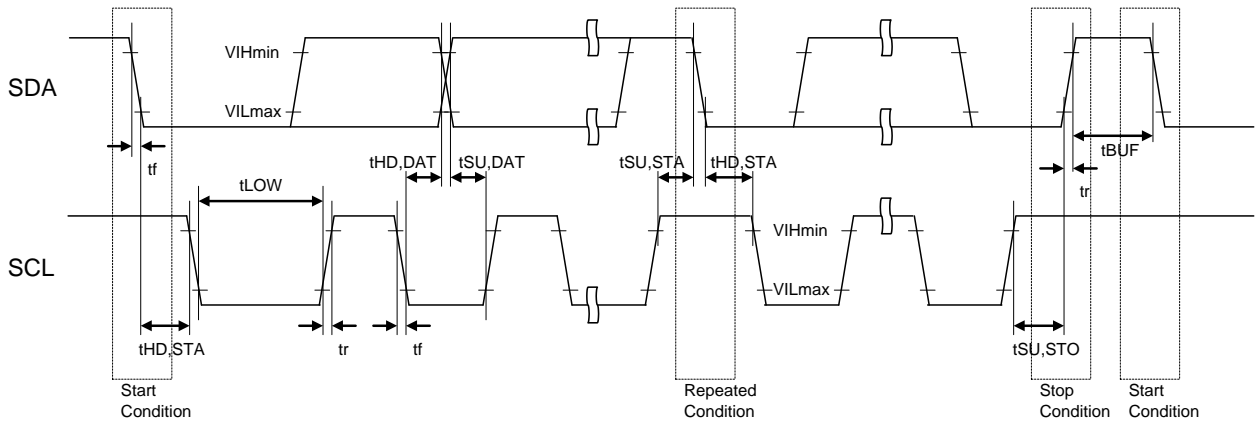
The data in the EEPROM may be rewritten unintentionally if you do not keep specifications. And it is forbidden to power off during EEPROM access. The data in the EEPROM may be rewritten unintentionally.



# LC898124EP1XC

## 2-wire serial Interface Timing

The communication protocol is compatible with I<sup>2</sup>C (Fast mode Plus).  
This circuit has clock stretch function.



Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	SCL			1000	kHz
START condition hold time	tHD,STA	SCL SDA	0.26			μs
SCL clock Low period	tLOW	SCL	0.5			μs
SCL clock High period	tHIGH	SCL	0.26			μs
Setup time for repetition START condition	tSU,STA	SCL SDA	0.26			μs
Data hold time	tHD,DAT	SCL SDA	0 (*1)		0.9	μs
Data setup time	tSU,DAT	SCL SDA	50			ns
SDA, SCL rising time	tr	SCL SDA			120	ns
SDA, SCL falling time	tf	SCL SDA			120	ns
STOP condition setup time	tSU,STO	SCL SDA	0.26			μs
Bus free time between STOP and START	tBUF	SCL SDA	0.5			μs

(\*1) Although the I<sup>2</sup>C specification defines a condition that 300 ns of hold time is required internally, This LSI is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

# LC898124EP1XC

## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898124EP1XC-MH	WLCSP27, 3.89x1.30, 0.4P (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

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