ANALOG DEVICES

3.1 nV/√Hz, 1 mA, 180 MHz, Rail-to-Rail Input/Output Amplifiers

Data Sheet

ADA4807-1/ADA4807-2

FEATURES

- **Low power**
  - **Quiescent current per amplifier: 1.0 mA at ±5 V**
  - **Fully specified at +3 V, +5 V, and ±5 V supplies**
- **High speed and fast settling for ±5 V**
  - **180 MHz, −3 dB bandwidth (G = +1, V_{OUT} = 20 mV p-p)**
  - **28 MHz, −3 dB bandwidth (G = +1, V_{OUT} = 2 V p-p)**
  - **225 V/µs slew rate for 5 V step (rise)**
  - **47 ns settling time to 0.1% for 4 V step**
- **Rail-to-rail input and output**
- **Low distortion at ±5 V (HD2/HD3)**
  - **−112 dBc/−115 dBc at 100 kHz, V_{OUT} = 2 V p-p**
  - **−95 dBc/−79 dBc at 1 MHz, V_{OUT} = 2 V p-p**
- **Low noise**
  - **3.1 nV/√Hz, f = 100 kHz**
  - **0.7 pA/√Hz, f = 100 kHz**
- **Low input noise voltage 1/f corner: 29 Hz**
- **Low input bias current: −1.2 µA typical**
- **Linear output current: 60 mA (sourcing) for ±5 V and +5 V**
- **Low input offset voltage: ±125 µV maximum**
- **Low input offset voltage drift: 3.8 µV/°C maximum**

APPLICATIONS

- **High speed, battery operated systems**
- **High component density systems**
- **High resolution analog-to-digital converter (ADC) drivers**
- **Portable test instruments**
- **Active filters**

GENERAL DESCRIPTION

The ADA4807-1/ADA4807-2 are low power, low noise, rail-to-rail voltage feedback amplifiers with exceptionally high performance. They are designed to have the lowest input noise (3.1 nV/√Hz and 0.7 pA/√Hz) among high speed, rail-to-rail amplifiers in the industry while operating on only 1 mA or less of quiescent supply current, making them ideal for a wide range of applications from battery-powered, portable instrumentation to high speed systems where component density requires lower power dissipation. The ADA4807-1/ADA4807-2 operate over a wide range of supply voltages from ±1.5 V to ±5 V, as well as from 3 V to 10 V single supplies, and include a disable feature that allows reduction of the typical quiescent supply current to 2.4 µA or less when asserted.

For systems with high dynamic range signals, the output voltage swings to within 70 mV of each rail, maximizing the output dynamic range, and the full, rail-to-rail input stage permits input operation up to and beyond the supply rails.

PIN CONNECTION DIAGRAMS

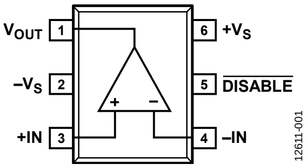

Figure 1. 6-Lead SC70 and 6-Lead SOT-23

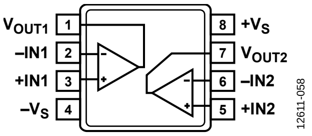

Figure 2. 8-Lead MSOP Pin Configuration

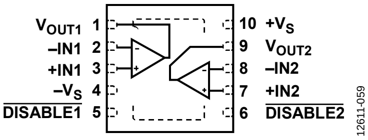

Figure 3. 10-Lead LFCSP Pin Configuration

The ADA4807-1/ADA4807-2 feature high speed performance of 180 MHz small signal −3 dB bandwidth, a 225 V/µs slew rate, and a settling time of 47 ns to 0.1% (4 V step) with a low input offset voltage of ±20 µV and 0.7 µV/°C drift. For ±5 V supplies, the HD2 is −112 dBc and HD3 is −115 dBc for a 2 V p-p, 100 kHz output signal driving a 1 kΩ load. The low distortion and fast settling time make these amplifiers ideal for driving high speed single-supply precision ADCs with up to 18-bit resolution. The ADA4807-1/ADA4807-2 deliver this excellent performance while consuming 1 mA or less of quiescent current.

The ADA4807-1 (single) is available in space-saving 6-lead SC70 and 6-lead SOT-23 packages. The ADA4807-2 (dual) is available in 10-lead LFCSP and 8-lead MSOP packages. The ADA4807-1/ADA4807-2 operate over the −40°C to +125°C industrial temperature range.

Table 1. Other Rail-to-Rail Amplifiers

Device	Bandwidth (MHz)	Slew Rate (V/µs)	Voltage Noise (nV/√Hz)	Max V_{OS} (mV)
AD8031/AD8032	80	35	15	1.5
AD8027/AD8028	190	90	4.3	0.8
AD8029/AD8030	125	62	16.5	5.0

Rev. A **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

4/15—Rev. 0 to Rev. A

Added ADA4807-2 ... Universal
Changes to Features Section, General Description Section, and Pin Connection Diagrams Heading ... 1
Added Figure 2 and Figure 3; Renumbered Sequentially ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 5
Changes to Table 3 ... 7
Changes to Table 6 and Figure 4 ... 9
Added Figure 7, Figure 8, and Table 8; Renumbered Sequentially ... 11
Reorganized Layout, Typical Performance Characteristics Section ... 12
Added Figure 36 ... 16
Changes to Figure 37 Caption, Figure 38 Caption, Figure 39 Caption, and Figure 40 Caption ... 17
Changes to Figure 44 and Figure 47 ... 18
Change to Theory of Operation Section ... 20
Changes to $\overline{\text{DISABLE}}$ Circuitry Section, Table 9, and Noise Considerations Section ... 21
Added Figure 65 and Figure 66 ... 23
Changes to Ordering Guide ... 25

12/14—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, V_S = ±5 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, $-V_S \leq V_{ICM} \leq +V_S - 1.5$ V, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 20 mV p-p		180		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 5 V step, 20% to 80%, rise/fall		225/250		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 4 V step		47		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−141		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−112		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-1		−95		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-2		−84		dBc
Third Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−144		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−79		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 1 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Noise Voltage 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage	$-V_S \leq V_{ICM} \leq +V_S - 1.5$ V	−125	±20	+125	µV
	$+V_S - 1.5\text{ V} \leq V_{ICM} \leq +V_S$	−750	±140	+750	µV
Input Offset Voltage Drift	$-V_S \leq V_{ICM} \leq +V_S - 1.2$ V, T_{MIN} to T_{MAX}		0.7	3.7	µV/°C
Input Bias Current	$-V_S \leq V_{ICM} \leq +V_S - 1.5$ V		−1.2	−1.6	µA
	$+V_S - 1.5\text{ V} \leq V_{ICM} \leq +V_S$		530	1000	nA
Input Bias Current Drift	$-V_S \leq V_{ICM} \leq +V_S - 1.2$ V, T_{MIN} to T_{MAX}		2.5	3.6	nA/°C
Input Offset Current	$-V_S \leq V_{ICM} \leq +V_S - 1.5$ V		8	100	nA
	$+V_S - 1.5\text{ V} \leq V_{ICM} \leq +V_S$		25	150	nA
Input Offset Current Drift	$-V_S \leq V_{ICM} \leq +V_S - 1.2$ V, T_{MIN} to T_{MAX}		30	250	pA/°C
Open-Loop Gain		120	130		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range			$-V_S - 0.2$ to $+V_S + 0.2$		V
Common-Mode Rejection Ratio (CMRR)	V_{ICM} = −3 V to +2 V	96	110		dB
$\overline{\text{DISABLE}}$ CHARACTERISTICS[1]					
$\overline{\text{DISABLE}}$ Low Input Voltage	Disabled		<1.3		V
$\overline{\text{DISABLE}}$ High Input Voltage	Enabled		>1.7		V
$\overline{\text{DISABLE}}$ Low Input Current	Disabled		−470		nA
$\overline{\text{DISABLE}}$ High Input Current	Enabled		−3		nA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{DISABLE}}$ On Time	$\overline{\text{DISABLE}}$ input midswing point to >90% of final V_{OUT}		1.3		µs
$\overline{\text{DISABLE}}$ Off Time	$\overline{\text{DISABLE}}$ input midswing point to <10% of enabled quiescent current		850		ns
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing					
High	$R_{LOAD} = 1\ k\Omega$	$+V_S - 0.08$	$+V_S - 0.04$		V
Low		$-V_S + 0.1$	$-V_S + 0.07$		V
Linear Output Current	Sourcing		60		mA
	Sinking		50		mA
Short-Circuit Current	Sourcing		80		mA
	Sinking		76		mA
Capacitive Load Drive	$C_{LOAD} = 15\ pF$		17		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, $T_A = 25°C$		1.0	1.1	mA
	Disabled, $T_A = 25°C$		2.4	4.0	µA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S = 3\ V$ to $5\ V$, $-V_S = -5\ V$	98	107		dB
Negative	$+V_S = 5\ V$, $-V_S = -3\ V$ to $-5\ V$	98	120		dB

[1] The disable pin is $\overline{\text{DISABLE}}$ on the ADA4807-1 and $\overline{\text{DISABLE1}}$ or $\overline{\text{DISABLE2}}$ for the ADA4807-2 LFCSP package, hereafter referred to as $\overline{\text{DISABLE}}$ for the ADA4807-1/ADA4807-2.

5 V SUPPLY

T_A = 25°C, V_S = 5 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, 0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 20 mV p-p		170		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, 20% to 80%, rise/fall		145/160		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		40		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−149		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−111		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-1		−93		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p, ADA4807-2		−83		dBc
Third Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−153		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−115		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−78		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 1 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Noise Voltage 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V	−125	±20	+125	µV
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$	−720	±110	+720	µV
Input Offset Voltage Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		0.7	3.7	µV/°C
Input Bias Current	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V		−1.2	−2.0	µA
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$		500	1000	nA
Input Bias Current Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		2.6	3.8	nA/°C
Input Offset Current	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V		8	100	nA
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$		25	150	nA
Input Offset Current Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		30	250	pA/°C
Open-Loop Gain		113	130		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.2 to $+V_S$ + 0.2		V
CMRR	V_{ICM} = 1 V to 3 V	96	110		dB
$\overline{\text{DISABLE}}$ CHARACTERISTICS					
$\overline{\text{DISABLE}}$ Low Input Voltage	Disabled		<1.3		V
$\overline{\text{DISABLE}}$ High Input Voltage	Enabled		>1.8		V
$\overline{\text{DISABLE}}$ Low Input Current	Disabled		−360		nA
$\overline{\text{DISABLE}}$ High Input Current	Enabled		−1.3		nA
$\overline{\text{DISABLE}}$ On Time	$\overline{\text{DISABLE}}$ input midswing point to >90% of final V_{OUT}		450		ns
$\overline{\text{DISABLE}}$ Off Time	$\overline{\text{DISABLE}}$ input midswing point to <10% of enabled quiescent current		850		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing					
High	R_{LOAD} = 1 kΩ	$+V_S - 0.05$	$+V_S - 0.03$		V
Low		$-V_S + 0.05$	$-V_S + 0.04$		V
Linear Output Current	Sourcing		60		mA
	Sinking		50		mA
Short-Circuit Current	Sourcing		106		mA
	Sinking		101		mA
Capacitive Load Drive	C_{LOAD} = 15 pF		24		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, T_A = 25°C		950	1000	µA
	Disabled, T_A = 25°C		1.3	2.0	µA
PSRR					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −2.5 V	98	115		dB
Negative	$+V_S$ = 2.5 V, $-V_S$ = −1.5 V to −3.5 V	98	130		dB

3 V SUPPLY

T_A = 25°C, V_S = 3 V, R_{LOAD} = 1 kΩ to midsupply, R_F = 0 Ω, G = +1, 0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, V_{OUT} = 20 mV p-p		165		MHz
	G = +1, V_{OUT} = 2 V p-p		28		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, 20% to 80%, rise/fall		118/237		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		40		ns
DISTORTION/NOISE PERFORMANCE					
Second Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−98		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−85		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−65		dBc
Third Harmonic	f_C = 1 kHz, V_{OUT} = 2 V p-p		−94		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−91		dBc
	f_C = 1 MHz, V_{OUT} = 2 V p-p		−68		dBc
Peak-to-Peak Noise	f = 0.1 Hz to 10 Hz		160		nV p-p
Input Voltage Noise	f = 100 kHz		3.1		nV/√Hz
	f = 10 kHz		3.3		nV/√Hz
	f = 10 Hz		5.8		nV/√Hz
Input Noise Voltage 1/f Corner			29		Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
	f = 10 Hz		10		pA/√Hz
Input Current Noise 1/f Corner			2		kHz
DC PERFORMANCE					
Input Offset Voltage	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V	−125	±20	+125	µV
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$	−720	±125	+720	µV
Input Offset Voltage Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		0.7	3.8	µV/°C
Input Bias Current	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V		−1.2	−2.0	µA
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$		500	1000	nA
Input Bias Current Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		2.7	3.8	nA/°C
Input Offset Current	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.5 V		8	130	nA
	$+V_S$ − 1.5 V ≤ V_{ICM} ≤ $+V_S$		25	150	nA
Input Offset Current Drift	0 V ≤ V_{ICM} ≤ $+V_S$ − 1.2 V, T_{MIN} to T_{MAX}		40	230	pA/°C
Open-Loop Gain		104	113		dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			45		MΩ
Differential Input Resistance			35		kΩ
Common-Mode Input Capacitance			1		pF
Differential Input Capacitance			1		pF
Input Common-Mode Voltage Range			$-V_S$ − 0.2 to $+V_S$ + 0.2		V
CMRR	V_{ICM} = 0.3 V to 1.3 V	92	110		dB
$\overline{\text{DISABLE}}$ CHARACTERISTICS					
$\overline{\text{DISABLE}}$ Low Input Voltage	Disabled		<1.1		V
$\overline{\text{DISABLE}}$ High Input Voltage	Enabled		>1.5		V
$\overline{\text{DISABLE}}$ Low Input Current	Disabled		−325		nA
$\overline{\text{DISABLE}}$ High Input Current	Enabled		−500		nA
$\overline{\text{DISABLE}}$ On Time	$\overline{\text{DISABLE}}$ input midswing point to >90% of final V_{OUT}		450		ns
$\overline{\text{DISABLE}}$ Off Time	$\overline{\text{DISABLE}}$ input midswing point to <10% of enabled quiescent current		850		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Saturated Output Voltage Swing					
High	R_{LOAD} = 1 kΩ	$+V_S - 0.04$	$+V_S - 0.02$		V
Low		$-V_S + 0.04$	$-V_S + 0.03$		V
Linear Output Current	Sourcing		50		mA
	Sinking		40		mA
Short-Circuit Current	Sourcing		80		mA
	Sinking		70		mA
Capacitive Load Drive	C_{LOAD} = 15 pF		30		% overshoot
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current per Amplifier	Enabled, no load, T_A = 25°C		915	1000	µA
	Disabled, T_A = 25°C		1.0	2.0	µA
PSRR					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −1.5 V	97	113		dB
Negative	$+V_S$ = 1.5 V, $-V_S$ = −1.5 V to −3.5 V	97	130		dB

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Internal Power Dissipation	See Figure 4
Input Voltage (Common Mode)	$\pm V_S \pm 0.2$ V
Differential Input Voltage	±1.4 V
Output Short-Circuit Duration	Observe power derating curves in Figure 4
Storage Temperature Range (All Packages)	−65°C to +125°C
Lead Temperature (Soldering 10 Sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the ADA4807-1/ADA4807-2 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Although the ADA4807-1/ADA4807-2 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the power derating curves shown in Figure 4.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead SC70, 4-Layer Board	209	°C/W
6-Lead SOT-23, 4-Layer Board	223	°C/W
8-Lead MSOP	123	°C/W
10-Lead LFCSP	51	°C/W

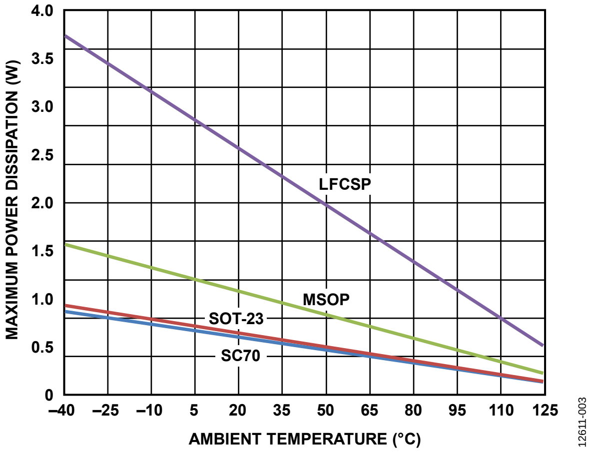


Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

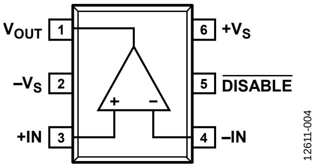


Figure 5. ADA4807-1 6-Lead SC70 Pin Configuration

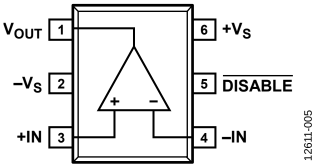


Figure 6. ADA4807-1 6-Lead SOT-23 Pin Configuration

Table 7. ADA4807-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Output
2	$-V_S$	Negative Supply
3	+IN	Noninverting Input
4	−IN	Inverting Input
5	$\overline{\text{DISABLE}}$	Active Low Power-Down
6	$+V_S$	Positive Supply

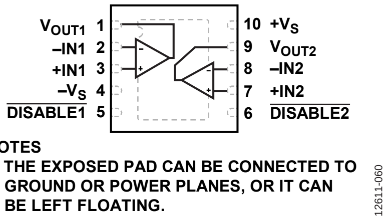


Figure 7. ADA4807-2 10-Lead LFCSP Pin Configuration

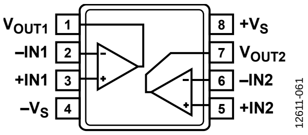


Figure 8. ADA4807-2 8-Lead MSOP Pin Configuration

Table 8. ADA4807-2 Pin Function Descriptions

Pin No.			
10-Lead LFCSP	**8-Lead MSOP**	**Mnemonic**	**Description**
1	1	V_{OUT1}	Output 1.
2	2	−IN1	Inverting Input 1.
3	3	+IN1	Noninverting Input 1.
4	4	$-V_S$	Negative Supply.
5	Not applicable	$\overline{\text{DISABLE1}}$	Active Low Power-Down 1.
6	Not applicable	$\overline{\text{DISABLE2}}$	Active Low Power-Down 2.
7	5	+IN2	Noninverting Input 2.
8	6	−IN2	Inverting Input 2.
9	7	V_{OUT2}	Output 2.
10	8	$+V_S$	Positive Supply.
	Not applicable	EPAD	Exposed Pad. For the 10-Lead LFCSP, the exposed pad can be connected to ground or power planes, or it can be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQUENCY RESPONSE

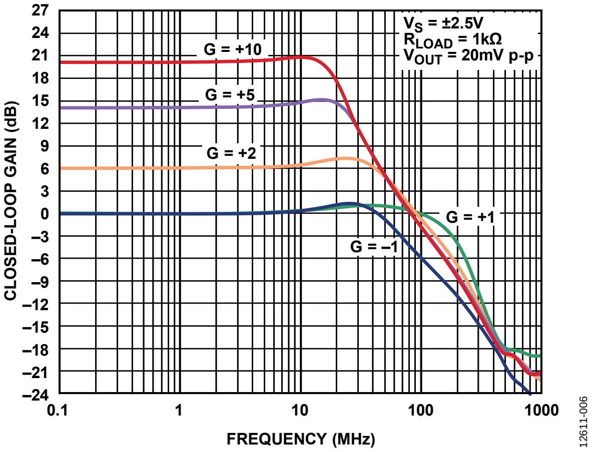


Figure 9. Small Signal Frequency Response for Various Gains, R_F = 499 Ω

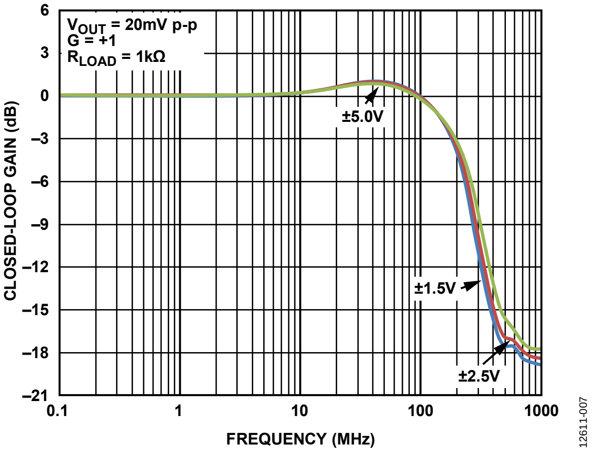


Figure 10. Small Signal Frequency Response for Various Supplies

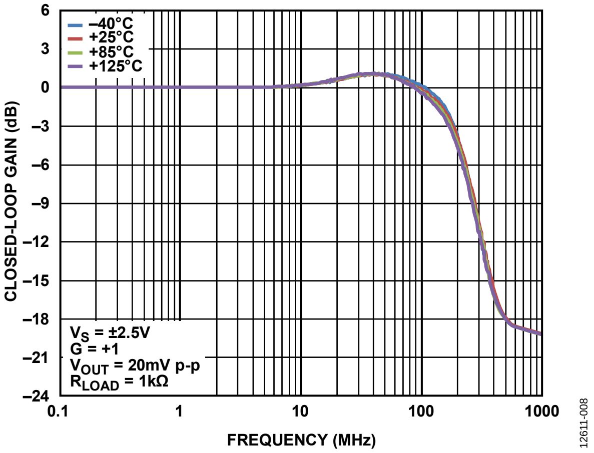


Figure 11. Small Signal Frequency Response for Various Temperatures

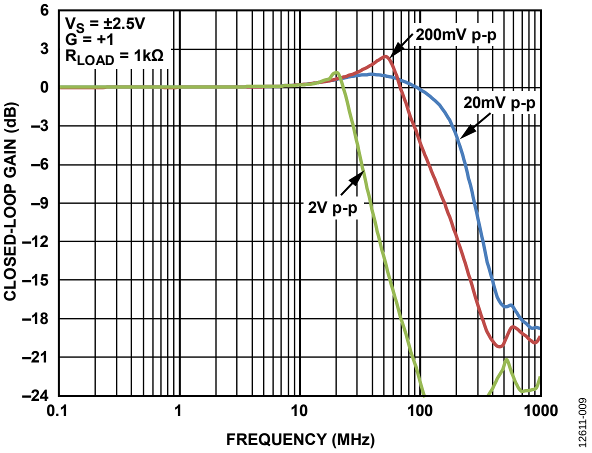


Figure 12. Frequency Response for Various Output Amplitudes

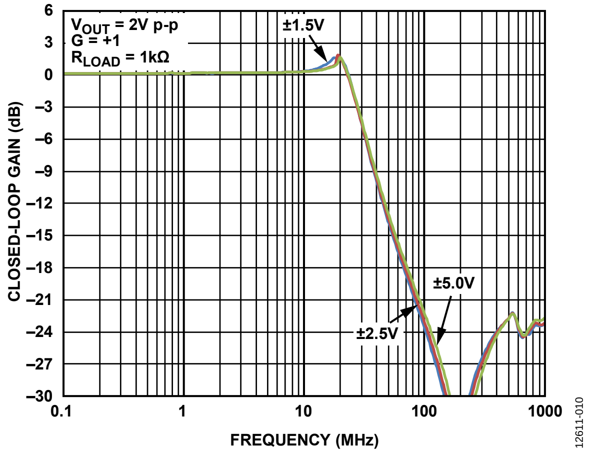


Figure 13. Large Signal Frequency Response for Various Supplies

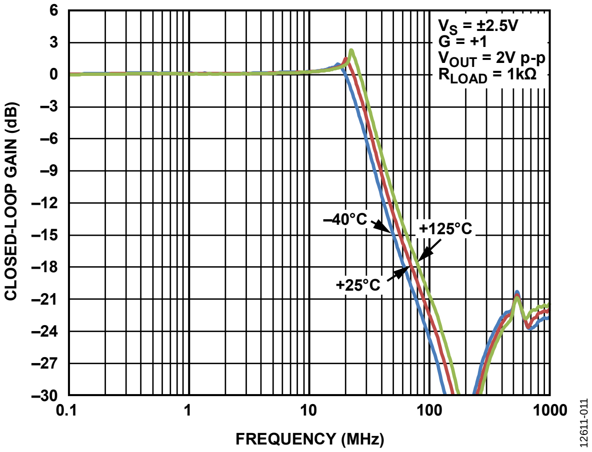


Figure 14. Large Signal Frequency Response for Various Temperatures

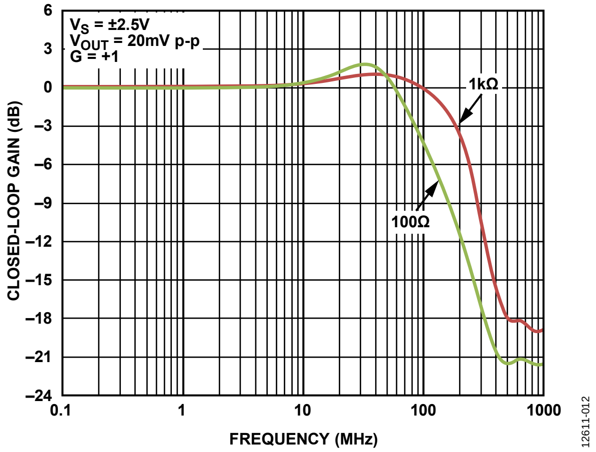


Figure 15. Small Signal Frequency Response for Various Resistive Loads

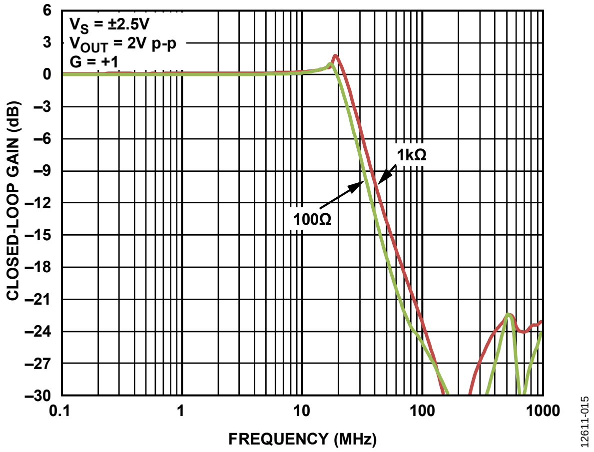


Figure 18. Large Signal Frequency Response for Various Resistive Loads

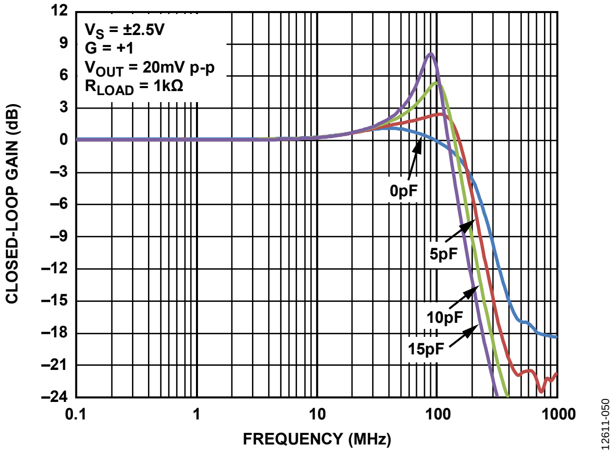


Figure 16. Small Signal Frequency Response for Various Capacitive Loads

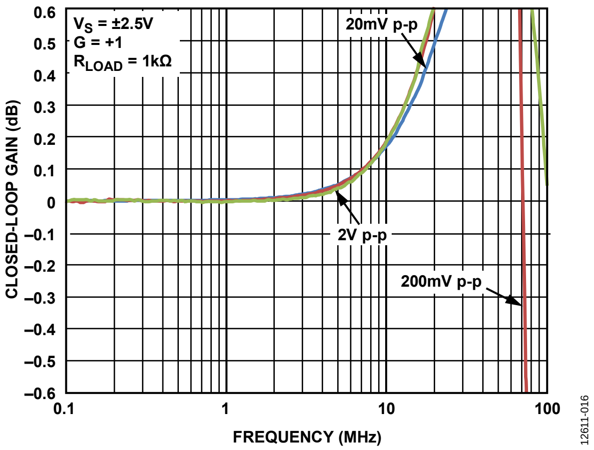


Figure 19. 0.1 dB Flatness Frequency Response for Various Output Amplitudes

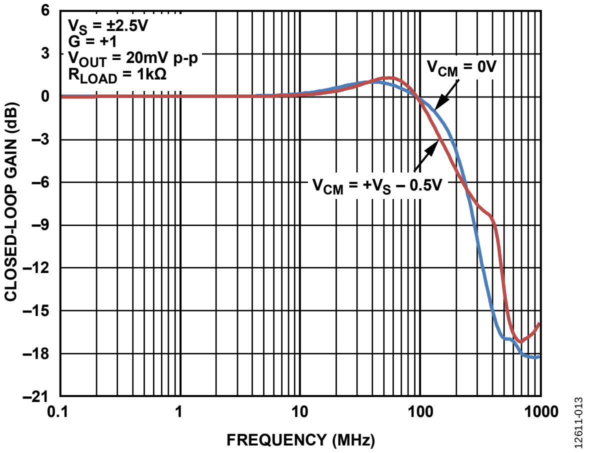


Figure 17. Small Signal Frequency Response for Various Input Common-Mode Voltages (V_{CM})

FREQUENCY AND SUPPLY CURRENT

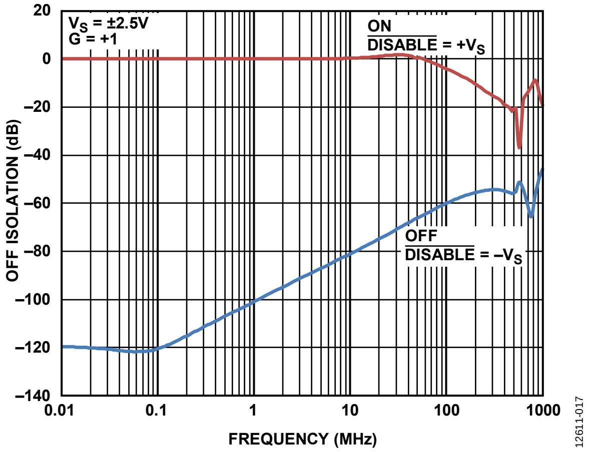


Figure 20. Off Isolation vs. Frequency

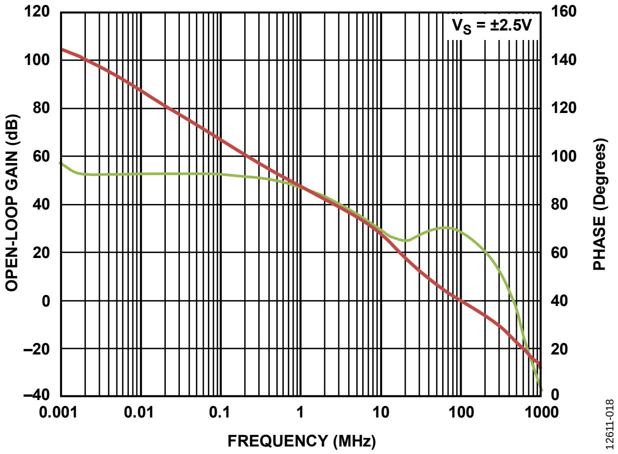


Figure 21. Open-Loop Gain and Phase vs. Frequency

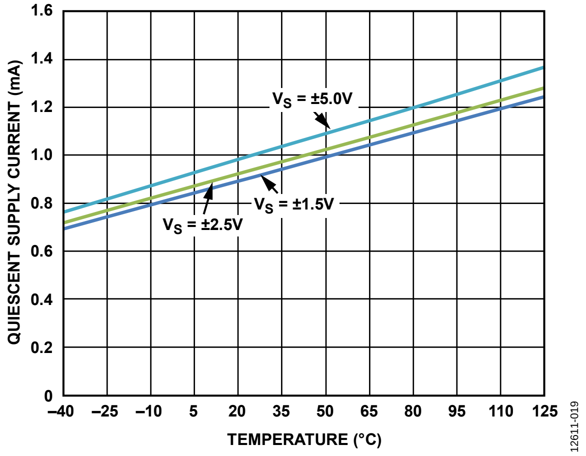


Figure 22. Quiescent Supply Current vs. Temperature

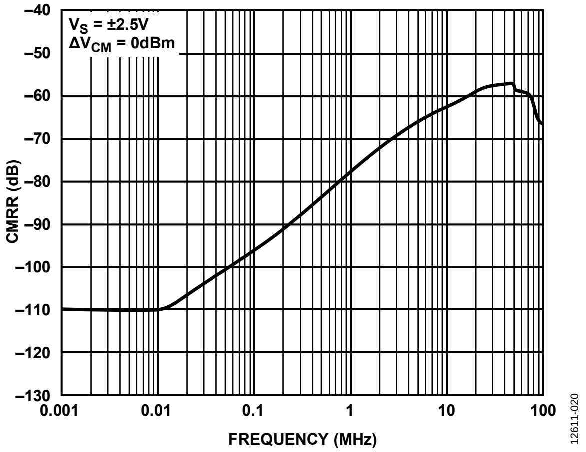


Figure 23. CMRR vs. Frequency

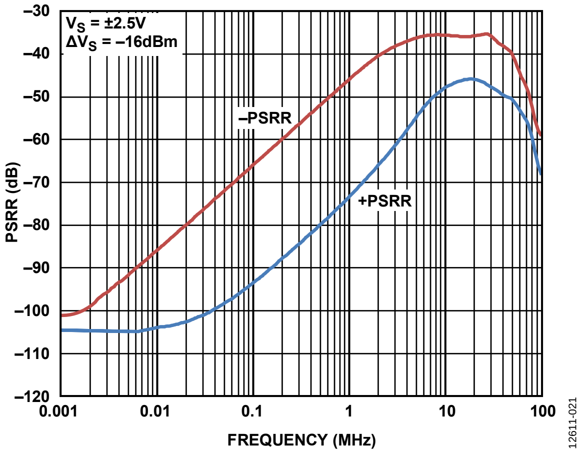


Figure 24. PSRR vs. Frequency

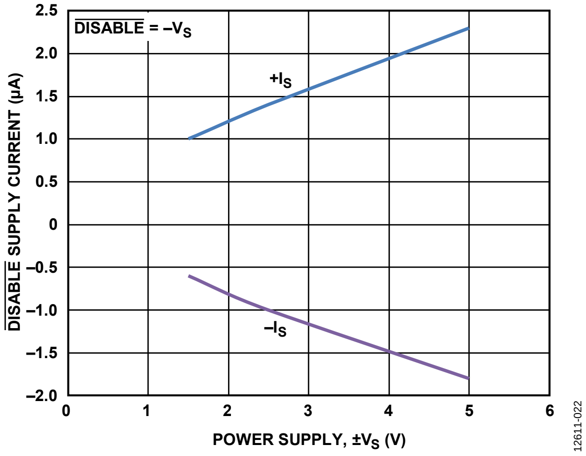


Figure 25. $\overline{\text{DISABLE}}$ Supply Current vs. Power Supply

DC AND INPUT COMMON-MODE PEFORMANCE

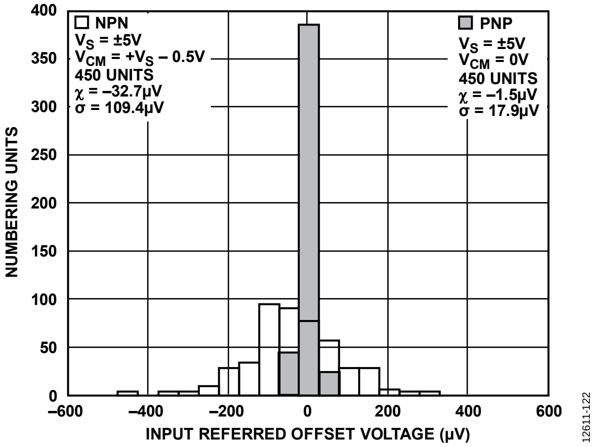


Figure 26. Input Referred Offset Voltage Distribution

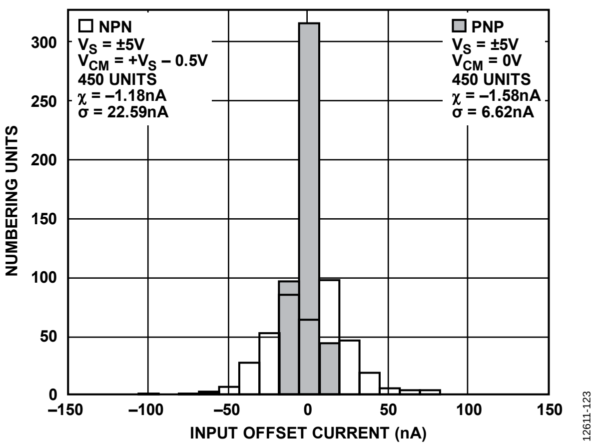


Figure 27. Input Offset Current Distribution

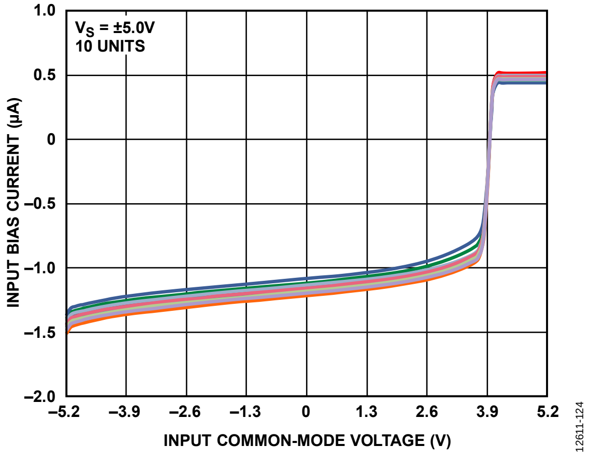


Figure 28. Input Bias Current vs. Input Common-Mode Voltage

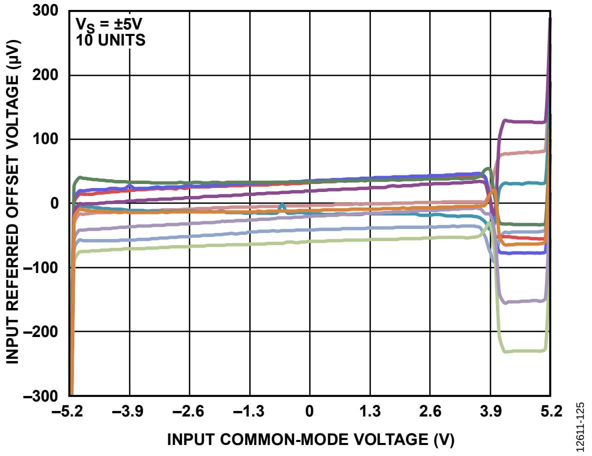


Figure 29. Input Referred Offset Voltage vs. Input Common-Mode Voltage

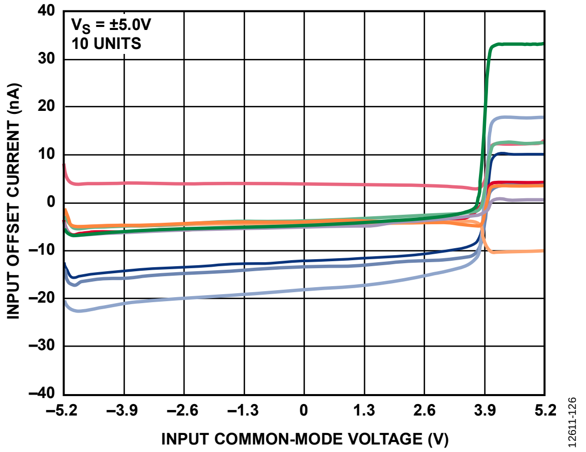


Figure 30. Input Offset Current vs. Input Common-Mode Voltage

SLEW, TRANSIENT, SETTLING TIME, AND CROSSTALK

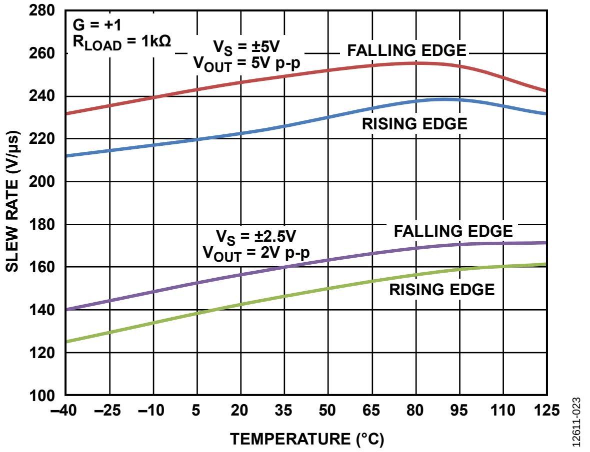


Figure 31. Slew Rate vs. Temperature

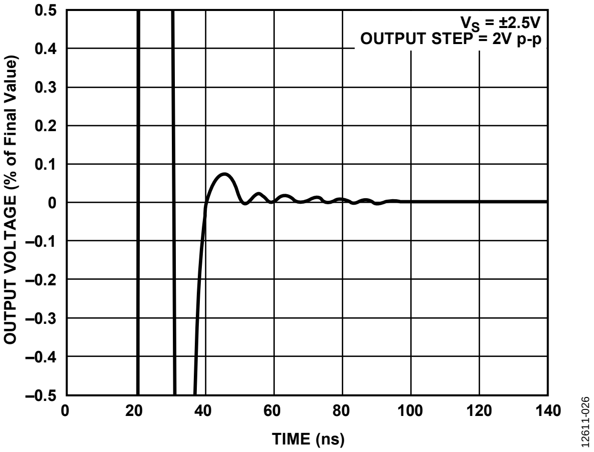


Figure 34. Settling Time to 0.1%

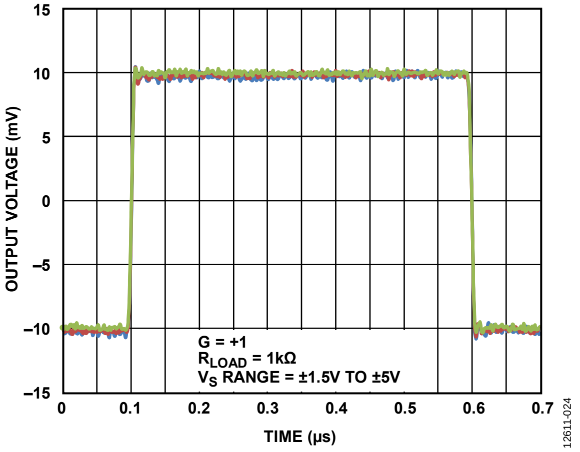


Figure 32. Small Signal Transient Response for Various Supplies

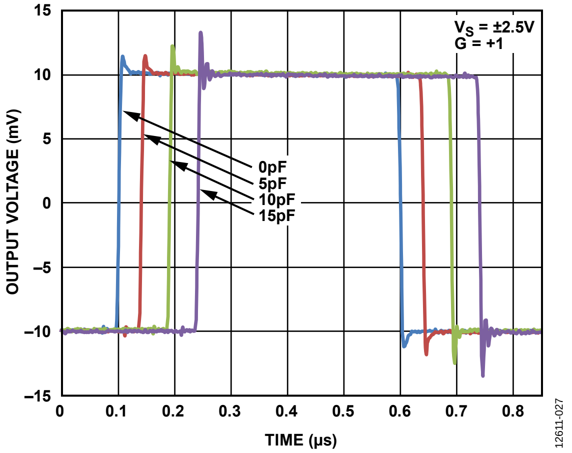


Figure 35. Small Signal Transient Response for Various Capacitive Loads

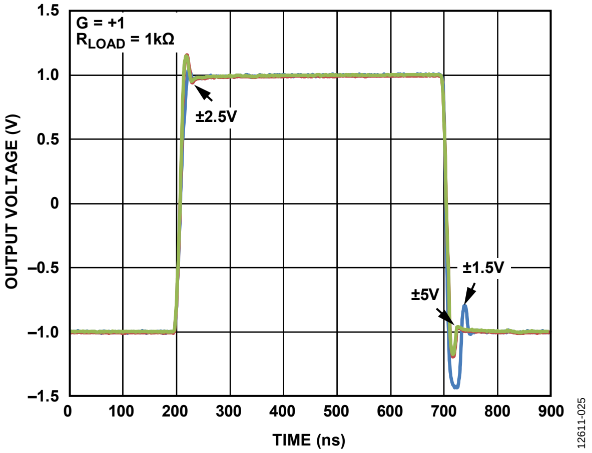


Figure 33. Large Signal Transient Response for Various Supplies

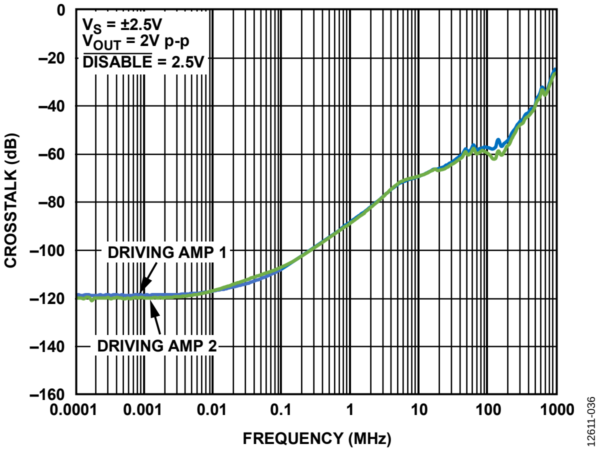


Figure 36. Crosstalk vs. Frequency

DISTORTION AND NOISE

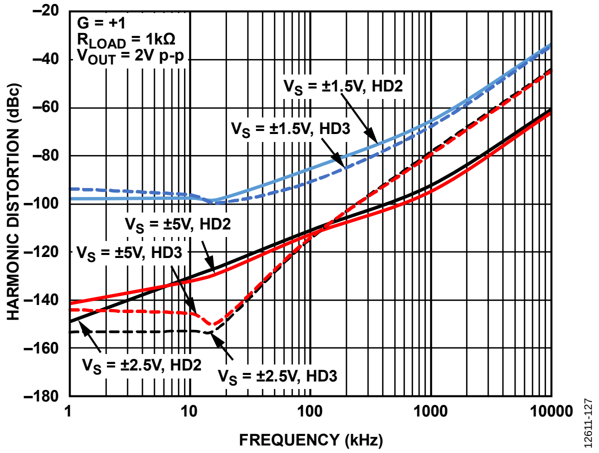


Figure 37. ADA4807-1 Harmonic Distortion vs. Frequency for Various Supplies

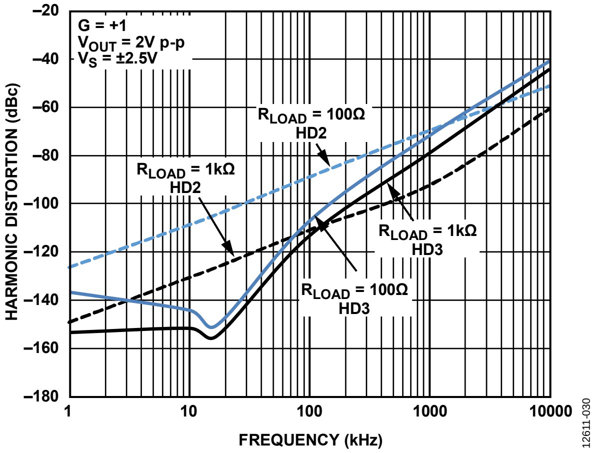


Figure 40. ADA4807-1 Harmonic Distortion vs. Frequency for Various Resistive Loads

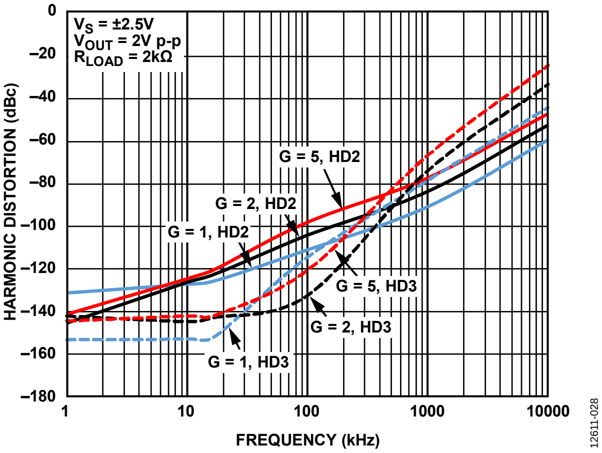


Figure 38. ADA4807-1 Harmonic Distortion vs. Frequency for Various Gains

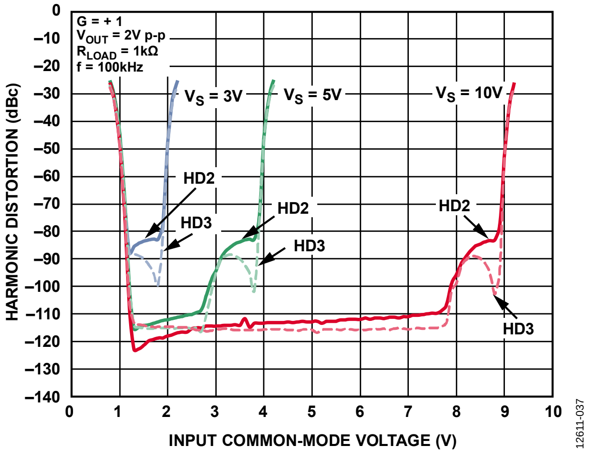


Figure 41. Harmonic Distortion vs. Input Common-Mode Voltage

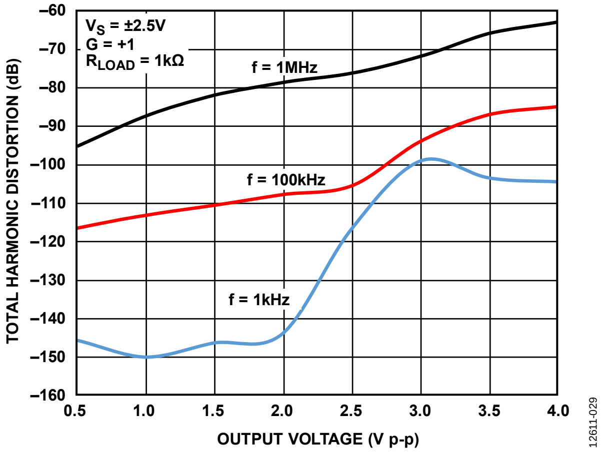


Figure 39. ADA4807-1 Total Harmonic Distortion vs. Output Voltage

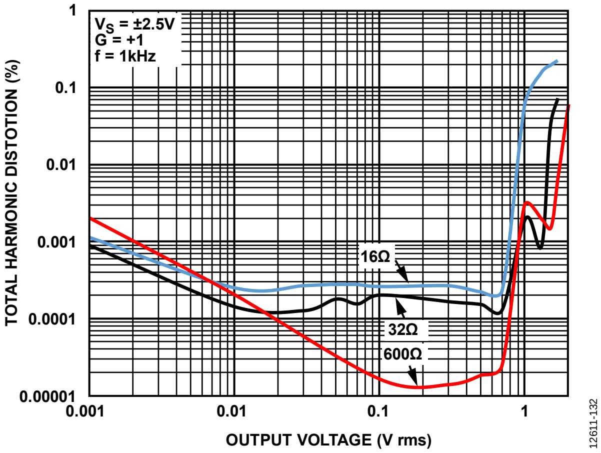


Figure 42. Total Harmonic Distortion vs. Output Voltage for Various Resistive Loads

OUTPUT CHARACTERISTICS

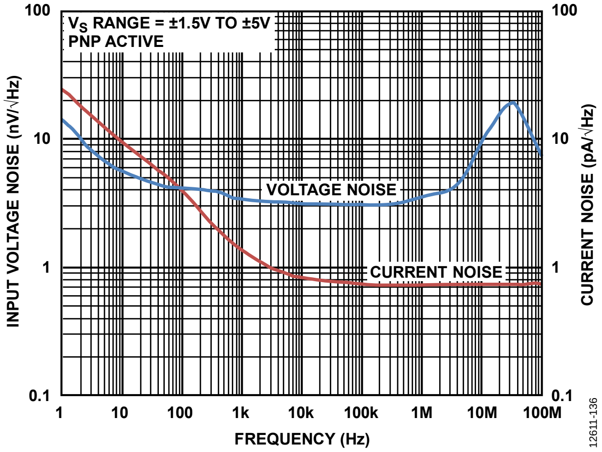


Figure 43. Input Voltage Noise and Current Noise, V_{CM} = 0 V vs. Frequency

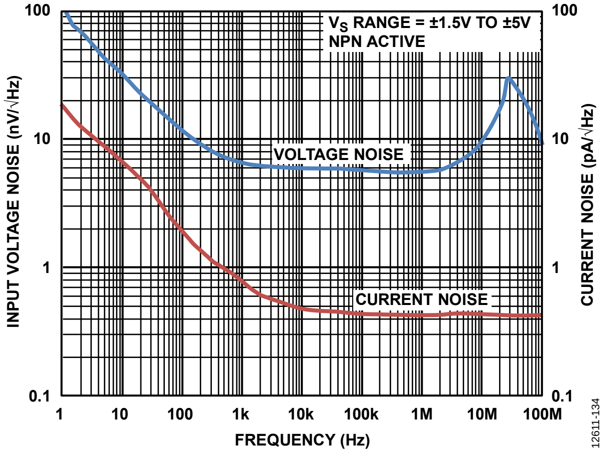


Figure 46. Input Voltage Noise and Current Noise, V_{CM} = $+V_S$ – 0.5 V vs. Frequency

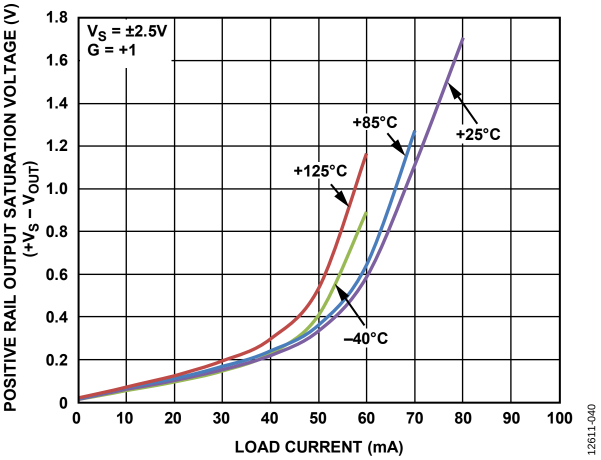


Figure 44. Positive Rail Output Saturation Voltage ($+V_S – V_{OUT}$) vs. Load Current for Various Temperatures

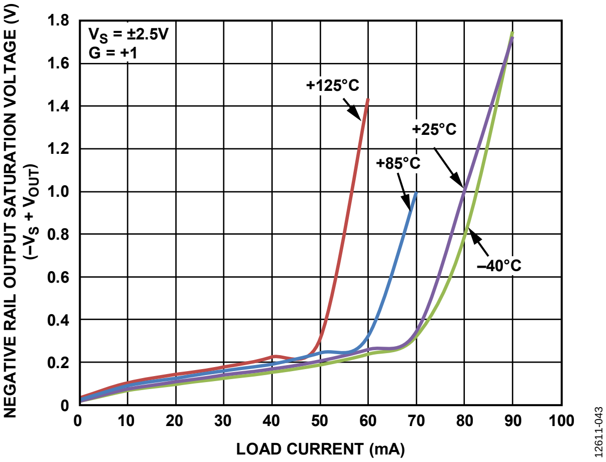


Figure 47. Negative Rail Output Saturation Voltage ($–V_S + V_{OUT}$) vs. Load Current for Various Temperatures

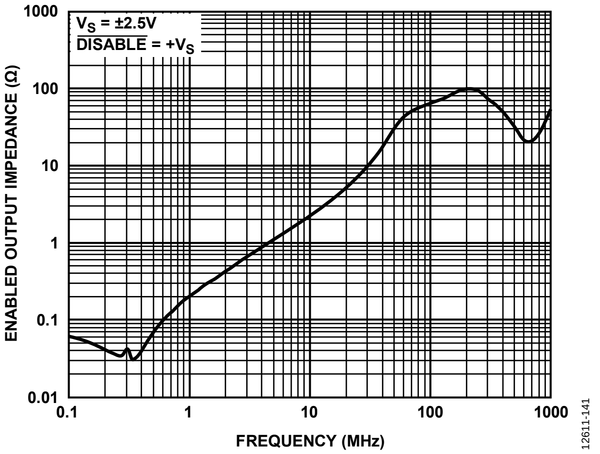


Figure 45. Enabled Output Impedance vs. Frequency

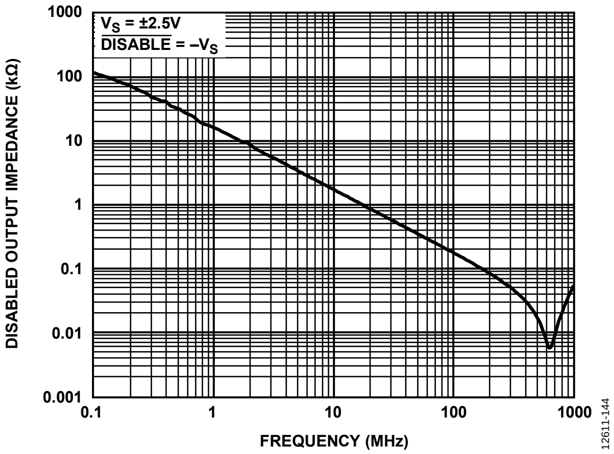


Figure 48. Disabled Output Impedance vs. Frequency

OVERDRIVE RECOVERY AND POWER-UP/POWER-DOWN

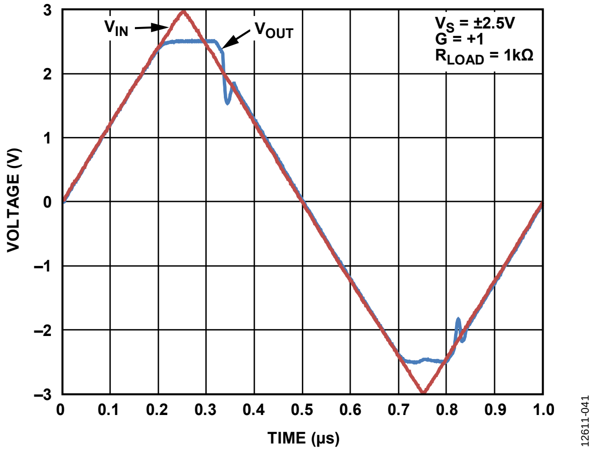


Figure 49. Input Overdrive Recovery

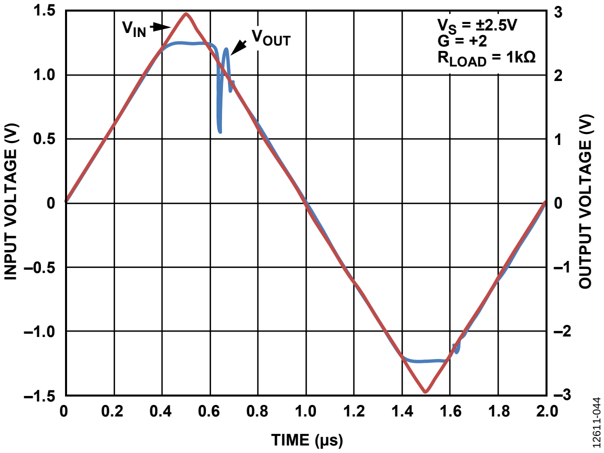


Figure 52. Output Overdrive Recovery

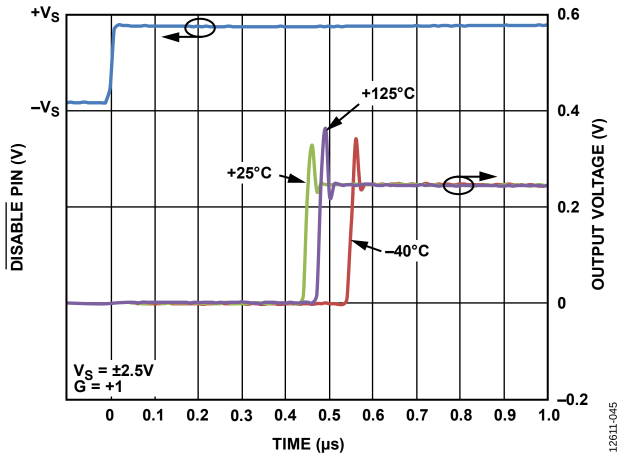


Figure 50. Power-Up Time vs. Temperature

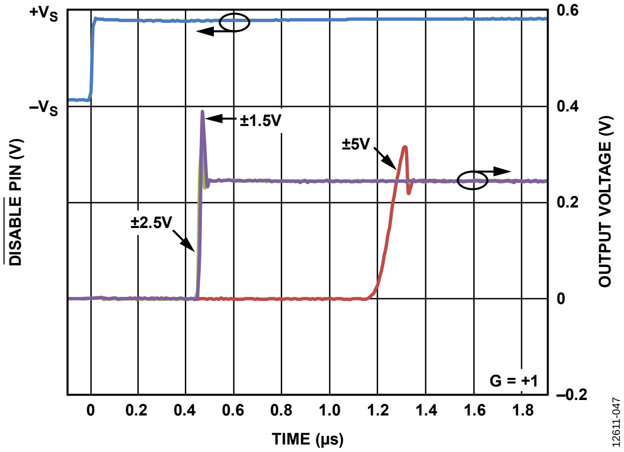


Figure 53. Power-Up Time for Various Supplies

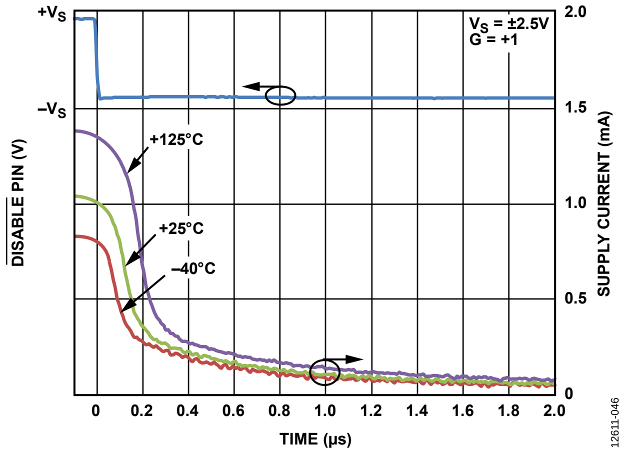


Figure 51. Power-Down Time vs. Temperature

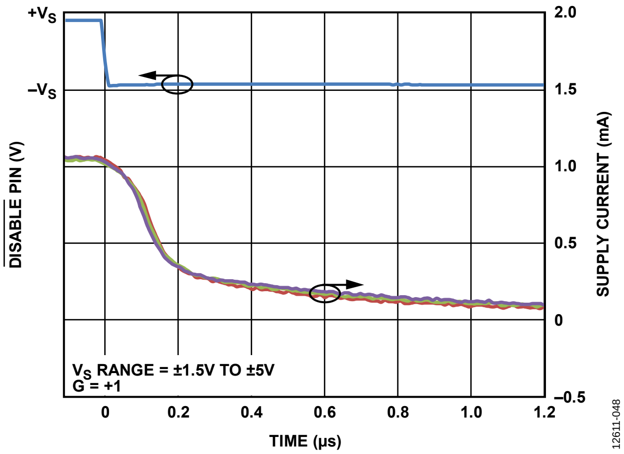


Figure 54. Power-Down Time for Various Supplies

THEORY OF OPERATION

The ADA4807-1/ADA4807-2 have a rail-to-rail input stage with an input range that goes 200 mV beyond either rail. A PNP transistor input pair is active for a majority of the input range, while an NPN transistor input pair is active for the common-mode voltages within 1.3 V of the positive rail. The ADA4807-1/ ADA4807-2 are fabricated in Analog Devices, Inc., third generation, extra fast complementary bipolar (XFCB) process resulting in exceptionally good distortion, noise, slew rate, and settling characteristics for 1 mA devices. Given traditional rail-to-rail input architecture performance, the input 1/f noise is surprisingly low, and the current noise is only 0.7 pA/√Hz for a 3 nV/√Hz voltage noise. Typical high slew rate devices suffer from increased current noise because of input pair degeneration and higher input stage current. The ADA4807-1/ADA4807-2 exceed current benchmark parameters given the performance of the XFCB process.

The multistage design of the ADA4807-1/ADA4807-2 has excellent precision specifications, such as input drift, offset, open-loop gain, CMRR, and PSRR. Typical harmonic distortion numbers fall in the range of −130 dBc for a 10 kHz fundamental (see Figure 40). This level of performance makes the ADA4807-1/ ADA4807-2 the best choices when driving 18-bit precision converters.

The ADA4807-1/ADA4807-2 are optimized for a low shutdown current (4 µA maximum), in the order of a few microamperes. In power sensitive applications, this can eliminate the use of a power FET and enable time interleaved power saving operation schemes.

The rail-to-rail input stage is useful in many different applications. Although the precision is reduced from input to input, many applications can tolerate this loss when the alternative is no functionality at all. The positive rail input range is indispensable for servo loops with a high-side input range

The ADA4807-1/ADA4807-2 input operates 200 mV beyond either rail. Internal protection circuitry prevents the output from phase inverting when the input range is exceeded. When the input exceeds a diode beyond either rail, internal electrostatic discharge (ESD) protection diodes source or sink current through the input.

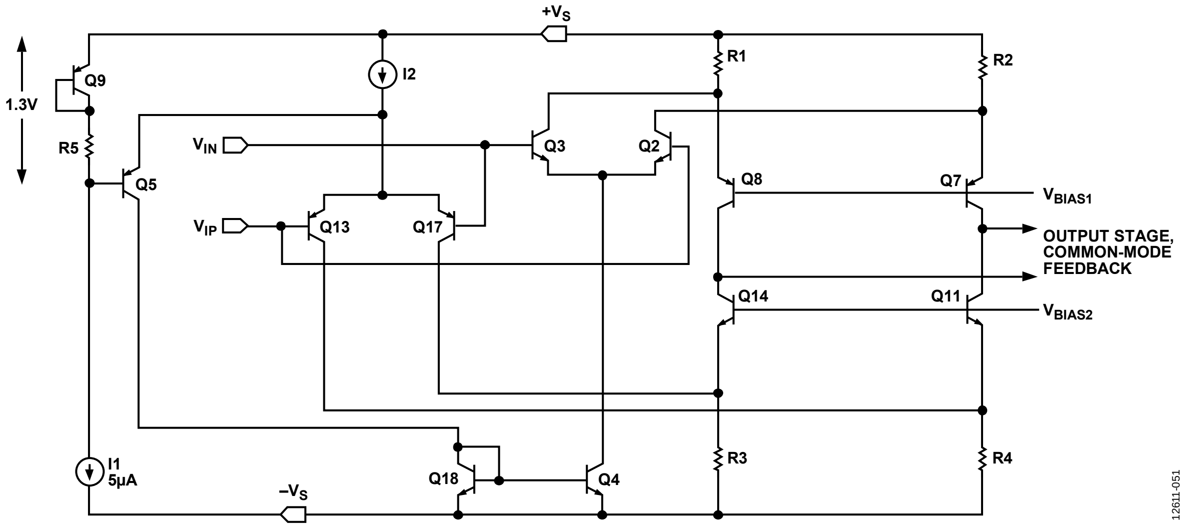


Figure 55. Simplified Schematic

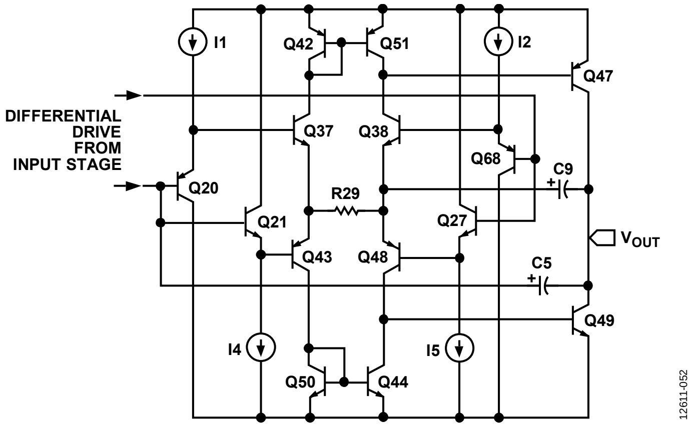


Figure 56. Differential Drive from Input Stage

$\overline{\text{DISABLE}}$ CIRCUITRY

When the $\overline{\text{DISABLE}}$ pin is an option, a pull-up resistor is necessary if the logic leakage currents exceed 300 nA. Pulling the $\overline{\text{DISABLE}}$ pin to ≥3.7 V below $+V_S$ turns the ADA4807-1/ ADA4807-2 off, which reduces the supply current to 2.4 µA for a 10 V voltage supply. Applying ≤3.4 V below $+V_S$ on the $\overline{\text{DISABLE}}$ pin enables the ADA4807-1/ADA4807-2 with a low quiescent current of 1 mA for a 10 V voltage supply. When the ADA4807-1/ ADA4807-2 device is disabled, its output enters a high impedance state. The output impedance decreases as frequency increases. When disabled, a forward isolation of 120 dB is achieved at 100 kHz (see Figure 20). ESD clamps protect the $\overline{\text{DISABLE}}$ pin, as shown in Figure 58. Voltages beyond the power supplies cause these diodes to conduct. To avoid excessive current in the ESD diodes, ensure that the voltage to the $\overline{\text{DISABLE}}$ pin does not exceed 0.7 V above the positive supply or that it does not fall 0.7 V below the negative supply. If an overvoltage condition is expected, limit the input current to less than 10 mA with a series resistor.

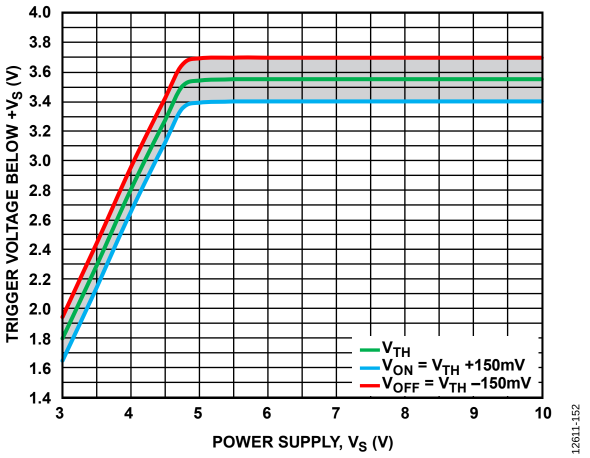


Figure 57. $\overline{\text{DISABLE}}$ Trigger Voltage

Table 9. Threshold Voltages for Disabled and Enabled Modes

Mode	+3 V	+5 V	+10 V	±5 V	+7 V/−2 V
Enabled	1.35 V	1.6 V	6.6 V	1.6 V	+3.6 V
Disabled	1.05 V	1.3 V	6.3 V	1.3 V	+3.3 V

INPUT PROTECTION

The ADA4807-1/ADA4807-2 are fully protected from ESD events, withstanding human body model ESD events of ±3 kV and charged device model events of ±1.25 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 58. For differential voltages above approximately 1.2 V at room temperature and 0.8 V at 125°C, the diode clamps begin to conduct. Too much current can cause damage due to excessive heating. If large differential voltages must be sustained across the input terminals, it is recommended that the current through the input clamps be limited to less than 10 mA. Series input resistors sized appropriately for the expected differential overvoltage provide the needed protection.

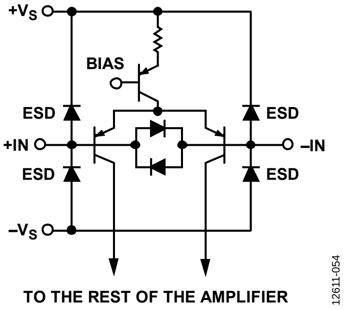


Figure 58. Input Stage and Protection Diodes

NOISE CONSIDERATIONS

Figure 59 illustrates the primary noise contributors for the typical gain configurations. The total output noise (V_{N_OUT}) is the root sum square of all the noise contributions.

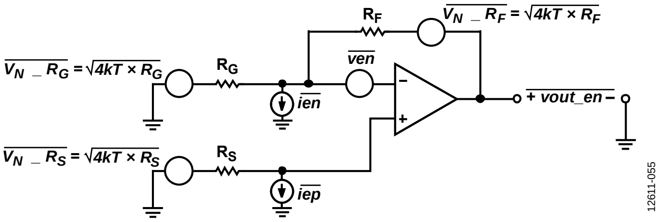


Figure 59. Noise Sources in Typical Gain Configurations

Calculate the output noise spectral density using Equation 1.

Source resistance noise, amplifier input voltage noise, and the voltage noise from the amplifier input current noise ($I_{N+} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$).

$$V_{N\_OUT} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2 \left[4kTRs + I_{N+}{}^2 R_S{}^2 + V_N{}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + I_{N-}{}^2 R_F{}^2} \qquad (1)$$

where:
k is Boltzmann's constant.
T is the absolute temperature in degrees Kelvin.
R_F and R_G are the feedback network resistances, as shown in Figure 59.
R_S is the source resistance, as shown in Figure 59.
I_{N+} and I_{N-} represent the amplifier input current noise spectral density in pA/√Hz.
V_N is the amplifier input voltage noise spectral density in nV/√Hz.

APPLICATIONS INFORMATION

CAPACITIVE LOAD DRIVE

Figure 60 shows the schematic for driving large capacitive loads, and Figure 61 shows the frequency response for a gain of +2. Note that the bandwidth decreases with larger capacitive loads (see Figure 61).

Figure 62 shows the required series resistor (R_{SERIES}) when limiting the peaking to 3 dB for a range of load capacitors (C_{LOAD}) at a gain of 2. From Figure 62, no series resistors are necessary to maintain stability for larger capacitors.

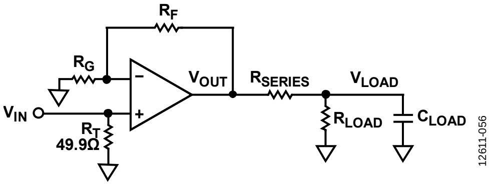


Figure 60. Schematic for Driving Large Capacitive Loads

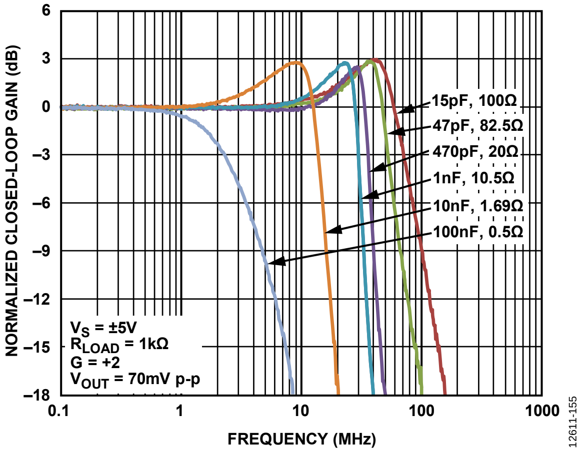


Figure 61. Frequency Response for Driving Large Capacitive Loads, $R_F = R_G = 249\ \Omega$

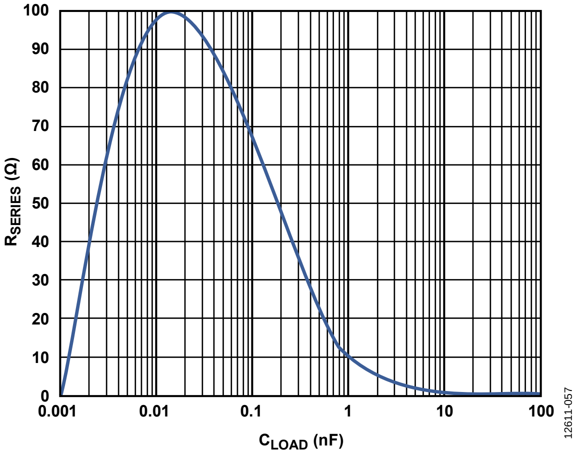


Figure 62. Required Series Resistor (R_{SERIES}) vs. Capacitive Load (C_{LOAD}) at 3 dB Peaking

LAYOUT, GROUNDING, AND BYPASSING

The ADA4807-1/ADA4807-2 are high speed devices. Realizing their superior performance requires attention to the details of high speed printed circuit board (PCB) design.

The first requirement is to use a multilayer PCB with solid ground and power planes that cover as much of the board area as possible.

Bypass each power supply pin directly to a nearby ground plane, as close to the device as possible. Use 0.1 µF high frequency ceramic chip capacitors.

Provide low frequency bulk bypassing using 10 µF tantalum capacitors from each supply to ground.

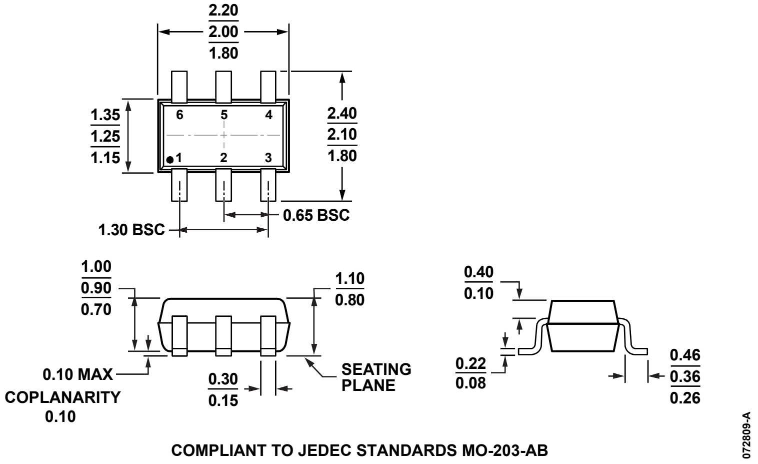
Stray transmission line capacitance in combination with package parasitics can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. Signal routing must be short and direct to avoid such parasitic effects. Provide symmetrical layout for complementary signals to maximize balanced performance.

Use radio frequency transmission lines to connect the driver and receiver to the amplifier.

Minimize stray capacitance at the input and output pins by clearing the underlying ground and low impedance planes near these pins.

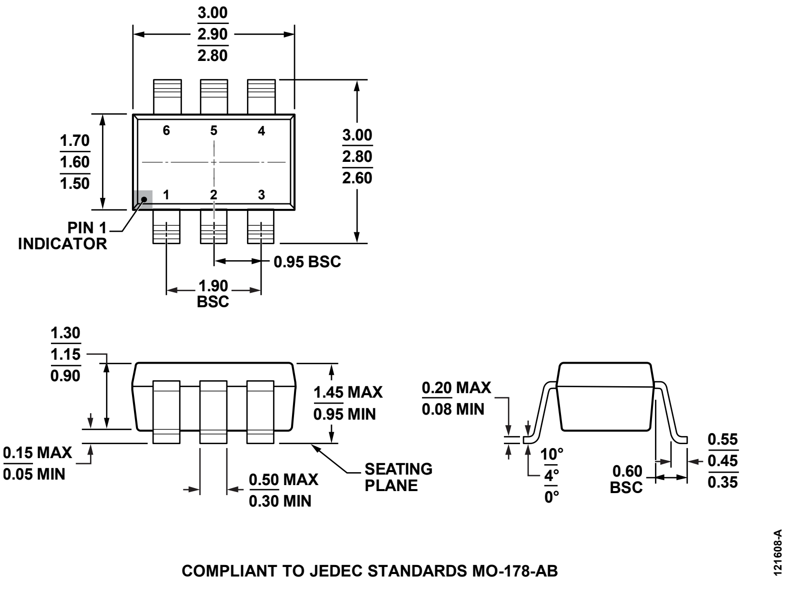
If the driver and receiver are more than one-eighth of the wavelength from the amplifier, minimize the signal trace widths. This nontransmission line configuration requires clearing of the underlying and adjacent ground and low impedance planes near the signal lines.

OUTLINE DIMENSIONS



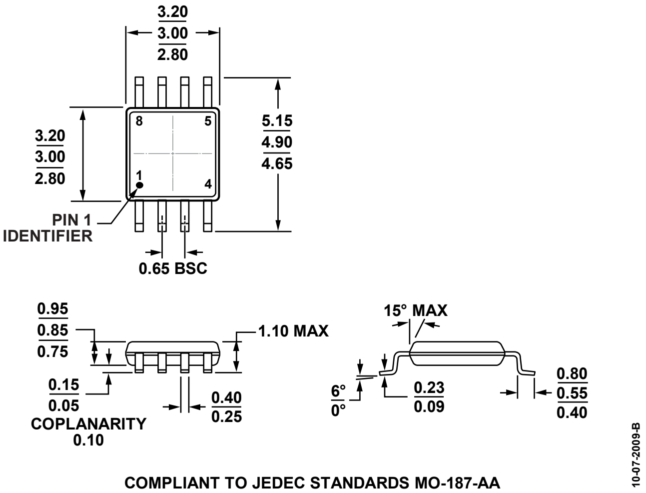
COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 63. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters



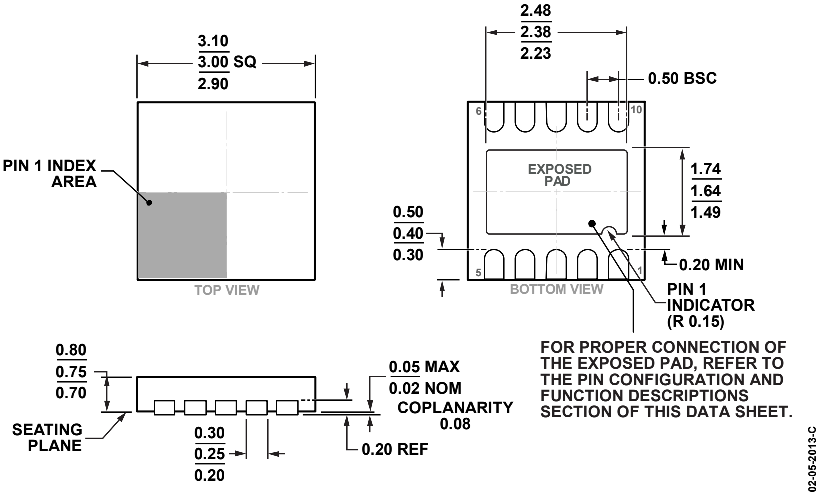
COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 64. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 65. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 66. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4807-1AKSZ-R2	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	H3J
ADA4807-1AKSZ-R7	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	H3J
ADA4807-1ARJZ-R2	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	H3J
ADA4807-1ARJZ-R7	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	H3J
ADA4807-2ACPZ-R2	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	H3S
ADA4807-2ACPZ-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	H3S
ADA4807-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	H3S
ADA4807-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	H3S
ADA4807-1AKSZ-EBZ		Evaluation Board for 6-Lead SC70		
ADA4807-1ARJZ-EBZ		Evaluation Board for 6-Lead SOT-23		
ADA4807-2ACPZ-EBZ		Evaluation Board for 10-Lead LFCSP_WD		
ADA4807-2ARMZ-EBZ		Evaluation Board for 8-Lead MSOP		

[1] Z = RoHS Compliant Part.

D12611-0-4/15(A)

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- *Комплексную поставку.*
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- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
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- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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