MAX35102

Time-to-Digital Converter Without RTC

General Description

The MAX35102 is a time-to-digital converter with built-in amplifier and comparator targeted as a low-cost, analog front-end solution for the ultrasonic heat meter and flow meter markets. It is similar to the MAX35101, but with a reduced feature set and without a real-time clock (RTC). The package size has been reduced to 4mm x 4mm x 0.75mm with 0.4mm pin pitch.

With a time measurement accuracy of 20ps and automatic differential time-of-flight (ToF) measurement, this device makes for simplified computation of liquid flow.

Power consumption is the lowest available with ultra-low $5.5\mu A$ ToF measurement and < 125nA duty-cycled temperature measurement.

Applications

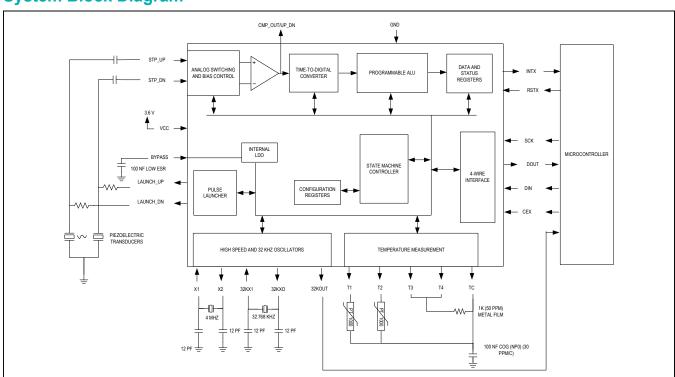
- Ultrasonic Heat Meters
- Ultrasonic Water Meters
- Ultrasonic Gas Meters

Ordering Information appears at end of data sheet.

Features and Benefits

- High-Accuracy Flow Measurement for Billing and Leak Detection
 - · Time-to-Digital Accuracy Down to 20ps
 - · Measurement Range Up to 8ms
 - · 2 Channels—Single-Stop Channel
- High-Accuracy Temperature Measurement for Precise Heat and Flow Calculations
 - · Up to Four 2-Wire Sensors
 - PT1000 and PT500 RTD Support
 - 40mK Accuracy
- Maximizes Battery Life with Low Device and Overall System Power
 - Ultra-Low 5.5µA ToF measurement and < 125nA Duty-Cycled Temperature Measurement
 - 2.3V to 3.6V Single-Supply Operation
- High-Integration Solution Minimizes Parts Count and Reduces BOM Cost
 - Small, 4mm x 4mm, 32-Pin TQFN Package
 - -40°C to +85°C Operation

System Block Diagram





Absolute Maximum Ratings

(Voltages relative to ground.)	Operating Temperature Range40°C to +85°C
Voltage Range on V _{CC} Pins0.5V to +4.0V	Junction Temperature+150°C
Voltage Range on All Other Pins	Storage Temperature Range55°C to +125°C
(not to exceed 4.0V)0.5V to (V _{CC} + 0.5V)	Lead Temperature (soldering, 10s)+300°C
Continuous Power Dissipation (T _A = +70°C)	Soldering Temperature (reflow)+260°C
TQFN (derate 29.40mW/°C above +70°C)2352.90mW	ESD Protection (All Pins, Human Body Model)±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TOFN

Junction-to-Ambient Thermal Resistance (θ_{JA}).......3°C/W Junction-to-Case Thermal Resistance (θ_{JC}).......3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Recommended Operating Conditions

 $(T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.}) \text{ (Notes 2, 3)}$

PARAMETER	SYMBOL	CONDITIONS	MIN .	TYP MAX	UNITS
Supply Voltage	V _{CC}		2.3	3.0 3.6	V
Input Logic 1 (RST, SCK, DIN, CE)	V _{IH}		V _{CC} x 0.7	V _{CC} + 0.3	V
Input Logic 0 (RST, SCK, DIN, CE)	V _{IL}		-0.3	V _{CC} x 0.3	V
Input Logic 1 (32KX1)	V _{IH32KX1}		VCC x 0.85	VCC + 0.3	V
Input Logic 0 (32KX1)	VIL32KX1		-0.3	V _{CC} x 0.15	V

Electrical Characteristics

 $(V_{CC} = 2.3V \text{ to } 3.6V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = 3.0V \text{ and } T_A = +25^{\circ}\text{C.}$) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (RST, SCK, DIN, CE)	IL		-0.1		+0.1	μΑ
Output Leakage (INT, T1,T2,T3,T4)	OL		-0.1		+0.1	μΑ
Output Voltage Low (32KOUT)	VOL32K	2mA			0.2 x Vcc	V
Output Voltage High (32KOUT)	Vон32K	-1mA	0.8 x V _C	С		V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	Voн	-4mA	0.8 x VC	С		V
Output Voltage High (TC)	Vонтс	V _{CC} = 3.3V, I _{OUT} = -4mA	2.9	3.1		٧
Output Voltage High (Launch_UP, Launch_DN)	Vohlauch	V _{CC} = 3.3V, I _{OUT} = -50mA	2.8	3.0		V
Output Voltage Low (INT, DOUT, CMP_OUT/UP_DN)	VoL	4mA			0.2 x VCC	V

Electrical Characteristics (continued)

 $(V_{CC} = 2.3V \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = 3.0V \text{ and } T_A = +25^{\circ}\text{C.})$ (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulldown Resistance (TC)	RTC		650	1000	1500	Ω
Input Voltage Low (TC)	VILTC		(0.36 x V _C	С	V
Output Voltage Low (Launch_UP, Launch_DN)	Vollauch	V _{CC} = 3.3V, I _{OUT} = 50mA		0.2	0.4	V
Resistance (T1, T2, T3, T4)	Ron			1		Ω
Input Capacitance (CE, SCK, DIN, RST)	CiN	Not tested		7		pF
RST Low Time	trst				100	ns
CURRENT						
Standby Current	IDDQ	No oscillators running, T _A = +25°C		0.1	1	μA
32kHz OSC Current	l32KHZ	32kHz oscillator only (Note 4)		0.5	0.9	μA
4MHz OSC Current	l _{4MHZ}	4MHz oscillator only (Note 4)		40	85	μA
LDO Bias Current	ICCLDO	ICCCPU = 0 (Note 4)		15	50	μA
Time Measurement Unit Current	Ісстми	(Note 4)		4.5	8	mA
Calculator Current	Ісссри			0.75	1.7	mA
Device Current Drain	ICC3	TOF_DIFF = 2 per second (3 hits), temperature = 1 per 30s		5.5		μΑ
ANALOG RECEIVER			•			•
Analog Input Voltage (STOP_UP, STOP_DN)	VANA		10	700	2 x V _{CC} x (3/8)	mV _{P-P}
Input Offset Step Size	VSTEP			1		mV
STOP_UP/STOP_DN Bias Voltage	V _{BIAS}		,	VCC x (3/8	3)	V
Receiver Sensitivity	VANA	Stop hit detect level (Note 5)	10			mV _{P-P}
TIME MEASUREMENT UNIT						
Measurement Range	tMEAS	Time of flight	8		8000	μs
Time Measurement Accuracy	tACC	Differential time measurement		20		ps
Time Measurement Resolution	tres			3.8		ps
EXECUTION TIMES						
Power-On-Reset Time	t _{RESET}	Reset to POR INT		275		μs
INIT Command Time	t _{INIT}	Command received when INIT bit set		2.5		ms
CAL Command Time	t _{CAL}	Command received when CAL bit set		1.25	·	ms

Electrical Characteristics (continued)

 $(V_{CC} = 2.3V \text{ to } 3.6V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = 3.0V \text{ and } T_A = +25^{\circ}\text{C.})$ (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PERIPHERAL INTERFACE						
DIN to SCK Setup	tDC				20	ns
SCK to DIN Hold	tcdH			2	20	ns
SCK to DOUT Delay	tcdd			5	20	ns
SCK Low Time	to	V _{CC} ≥ 3.0V	25	4		no
SCK LOW TIME	tCL	V _{CC} = 2.3V	50	30		ns
SCK High Time	tсн		25	4		ns
SCK Fragueray	4	V _{CC} ≥ 3.0V			20	MHz
SCK Frequency	tCLK	V _{CC} = 2.3V			10	IVITZ
CE to SCK Setup	tcc			5	40	ns
SCK to CE Hold	tссн				20	ns
CE Inactive Time	tcwH			2	40	ns
CE to DOUT High Impedance	tccz			5	20	ns

Recommended External Crystal Characteristics

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f32K			32.768		kHz
32kHz Frequency Tolerance	Δf32K/f32K	T _A = +25°C	-20		+20	ppm
32kHz Load Capacitance	CL32K			12.5		pF
32kHz Series Resistance	R _{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	F _{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	Δf4M/f4M	T _A = +25°C	-30	-	+30	ppm
4MHz Crystal Load Capacitance	CL4M			12.0		pF
4MHz Crystal Series Resistance	Rs4M				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		T _A = +25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF
4MHz Ceramic Series Resistance					30	Ω

- **Note 2:** All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.
- Note 3: Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
- **Note 4:** Currents are specified as individual block currents. Total current for a point in time can be calculated by taking the standby current and adding any block currents that are active at that time.
- Note 5: Receiver sensitivity includes performance degradation contributed by STOP_UP and STOP_DN device pin input offset voltage and common mode drift.

Timing Diagrams

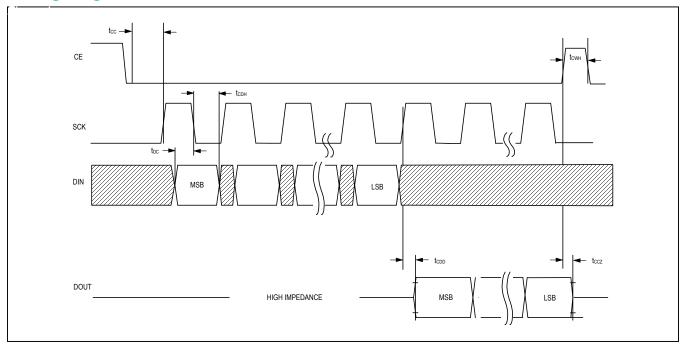


Figure 1. SPI Timing Diagram Read

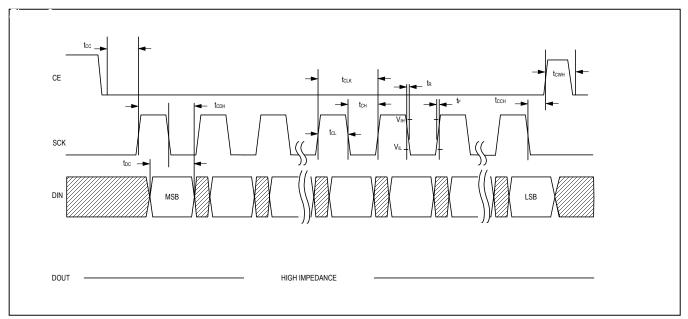
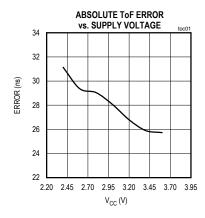
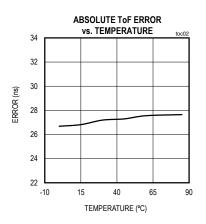


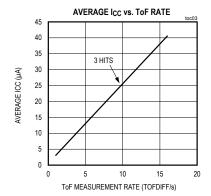
Figure 2. SPI Timing Diagram Write

Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)







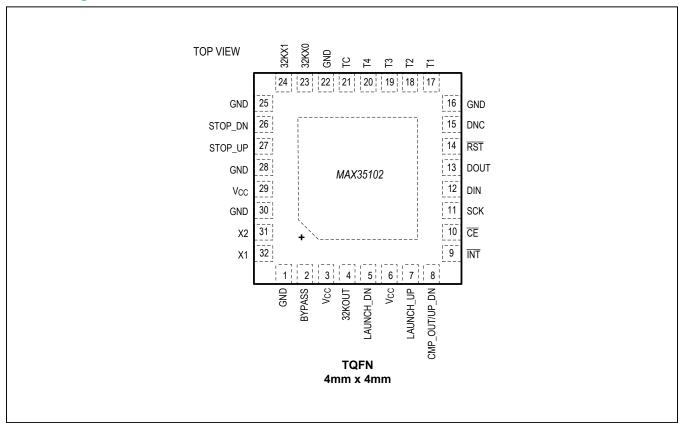
Average ICC vs. TOF Rate Configuration Settings

	3 HI	T SETTINGS
CONTOL BIT(S)	VALUE	BIT SETTINGS
Clock Settling Time	488µs	CLK_S[2:0] = 000
Bias Charge Time	61µs	CT[1:0] = 00
Pulse Launch Frequency	1MHz	DPL[3:0] = 0001
Pulse Launcher Size	15	PL[7:0] = 00001111
TOF Duty Cycle	19.97ms	TOF_CYC[2:0] = 111
Stop Hits	3	STOP[1:0] = 010
T2 Wave Selector	Wave 2	T2WV[5:0] = 000110
Temperature Port Number	4	TP[1:0] = 11
Preamble Temperature Cycle Number	1	PRECYC[2:0] = 001
Port Cycle Time	256µs	PORTCYC[1:0] = 01

- 1. This data is valid for the ceramic resonator.
 2. Crystal oscillator startup adds ~0.5µA per TOFDiff.
 3. Since the TOF cycle time is long the 4MHz oscillator powers up twice.

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Pin Configuration



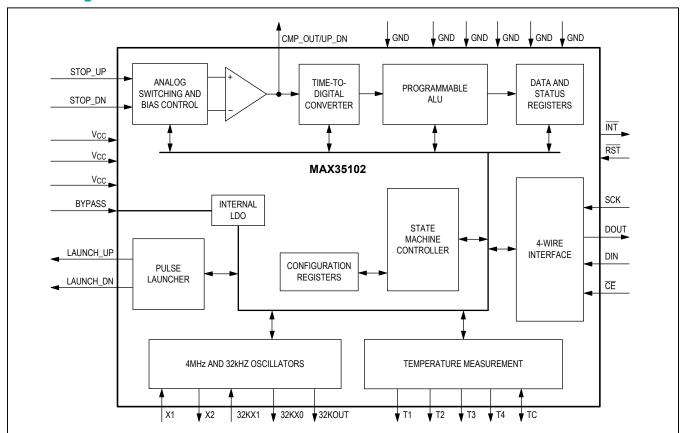
Pin Description

PIN	NAME	FUNCTION
1, 16, 22, 25, 28, 30	GND	Device Ground
2	BYPASS	Connect this pin to ground with a capacitor (100nF) to provide stability for the on-board low-dropout regulator. The effective series resistance of this capacitor needs to be in the 1Ω to 2Ω range.
3, 6, 29	Vcc	Main Supply. Typically sourced from a single lithium cell.
4	32KOUT	CMOS Output. Repeats the 32kHz crystal oscillator frequency.
5	LAUNCH_DN	CMOS Pulse Output Transmission in Downstream Direction of Water Flow
7	LAUNCH_UP	CMOS Pulse Output Transmission in Upstream Direction of Water Flow
8	CMP_OUT/UP_DN	CMOS Output. Indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output.
9	ĪNT	Active-Low Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
10	CE	Active-Low CMOS Digital Input. Serial peripheral interface chip enable input.

Pin Description (continued)

	1	
PIN	NAME	FUNCTION
11	SCK	CMOS Digital Input. Serial peripheral interface clock input.
12	DIN	CMOS Digital Input. Serial peripheral interface data input.
13	DOUT	CMOS Output. Serial peripheral interface data output.
14	RST	Active-Low CMOS Digital Reset Input
15	DNC	Do Not Connect. This pin must be left unconnected.
17	T1	Open-Drain Probe 1 Temperature Measurement
18	T2	Open-Drain Probe 2 Temperature Measurement
19	T3	Open-Drain Probe 3 Temperature Measurement
20	T4	Open-Drain Probe 4 Temperature Measurement
21	TC	Input/Output Temperature Measurement Capacitor Connection
23	32KX0	Connections for 32.768kHz Quartz Crystal. An external CMOS 32.768kHz oscillator can also
24	32KX1	drive the MAX35102. In this configuration, the 32KX1 pin is connected to the external oscillator signal and the 32KX0 pin is left unconnected.
26	STOP_DN	Downstream STOP Analog Input. Used for the signal that is received from the downstream transmission of a time-of-flight measurement.
27	STOP_UP	Upstream STOP Analog Input. Used for the signal that is received from the upstream transmission of a time-of-flight measurement.
31	X2	Connections for AMI In Overta Createl A coronic reconstructor can also be used
32	X1	Connections for 4MHz Quartz Crystal. A ceramic resonator can also be used.
	EP	Exposed Pad. Connect to GND.

Block Diagram



Detailed Description

The MAX35102 is a time-to-digital converter with built-in amplifier and comparator targeted as a complete analog front-end solution for the ultrasonic heat meter and flow meter markets.

With automatic differential time-of-flight (TOF) measurement, this device makes for simplified computation of liquid flow. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements. A programmable receiver hit accumulator can be utilized to minimize the host microprocessor access.

Multihit capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, an autozero amplifier/comparator, and programmable receiver sensisitivity provide the analog interface and control for a minimal electrical bill of material solutions.

For temperature measurement, the MAX35102 supports up to four 2-wire PT1000/500 platinum resistive temperature detectors (RTD).

A simple opcode based 4-Wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

Time-of-Flight (ToF) Measurement Operations

TOF is measured by launching pulses from one piezoelectric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The MAX35102 contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The MAX35102 can measure two separate TOFs, which are defined as TOF up and TOF down.

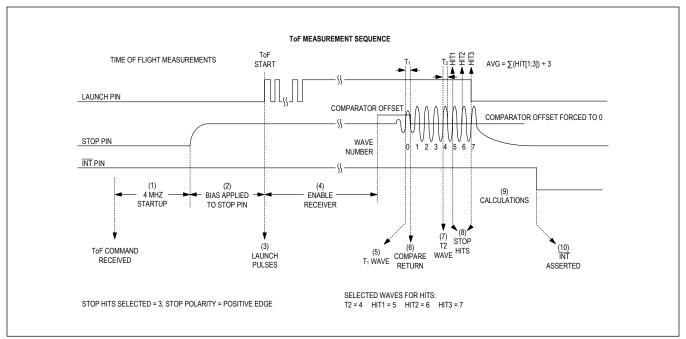


Figure 3. Time-of-Flight Sequence

A TOF up measurement has pulses launched from the LAUNCH_UP pin, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the STOP_UP pin. A TOF down measurement has pulses launched from the LAUNCH_DN pin, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the STOP_DN pin.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands.

The steps involved in a single TOF measurement are described here and shown in $\underline{\text{Figure 3}}$.

- The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
- A common-mode bias is enabled on the STOP pin. This bias charge time is set by the CT[1:0] bits in the TOF1 register.
- 3) Once the bias charge time has expired, the pulse launcher drives the appropriate LAUNCH pin with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% dutycycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses gen-

- erates a start signal for the time-to-digital converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted by the start signal in the start/stop TDC timing (Figure 3).
- 4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate STOP pin are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
- 5) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the STOP pin according to the setting of the STOP_POL bit in the TOF1 register. The first stop hit is detected when a wave received at the STOP pin exceeds the comparator offset voltage, which is set in the TOF6 and TOF7 registers. This first detected wave is wave number 0. The width of the wave's pulse that exceeds the comparator offset voltage is measured and stored as the t1 time.
- 6) The offset of the comparator then automatically and immediately switches to 0.
- 7) The t₂ wave is detected and the width of the t₂ pulse is measured and stored as the t₂ time. The wave number for the measurement of the t₂ wave width is set by the T2WV[5:0] bits in the TOF2 register.

- 8) Following the t₂ wave, 1 to 3 consecutive stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[1:0] bits in the TOF2 register.
- 9) After receiving all of the programmed hits, the MAX35102 calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t₁/t₂ and t₂/t_{ideal} are calculated and stored in the WVRUP or WVRDN register.
- 10) Once all of the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the INT pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a Read Register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is

7FFFh or (2¹⁵-1) x t_{4MHz} or ~ 8.19 ms. The maximum size of the fraction is:

FFFFh or
$$\frac{2^{16}-1}{2^{16}} \times t_{4MHz}$$
. or ~ 249.9961 ns.

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTE	R VALUE	CONVERTER VALUE
TOF_DIFFInt (hex)	TOF_DIFFFrac (hex)	TOF DIFF VALUE (ns)
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

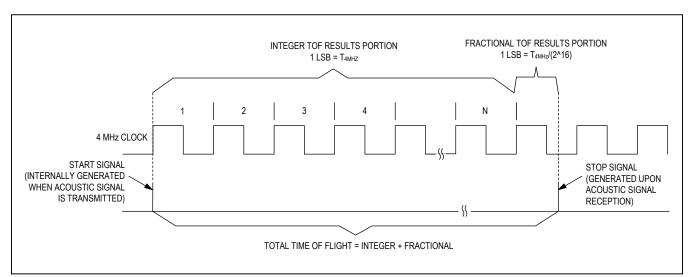


Figure 4. Start/Stop for Time-to-Digital Timing

Early Edge Detect

This early edge detect method of measuring the TOF of acoustic waves is used for all of the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the MAX35102 to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +31 LSBs if triggering on a positive edge and -32 LSBs if triggering on a negative edge, with 1 LSB = V_{CC}/3072. Separate input offset settings are available for the upstream received signal and the downstream received signal. The input offset for the upstream received signal is programmed using the C_OFFSETUP[4:0] bits in the TOF6 register. The input offset for the downstream received signal is programmed using the C OFFSETDN[4:0] bits in the TOF7 register. Once the first hit is detected, the time t1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to 0.

The MAX35102 is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5, this is the 7th wave after

the early edge detect wave. The selection of the t₂ wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{ideal} is calculated and registered for the user. For this calculation, t_{ideal} is1/2 the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all of the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

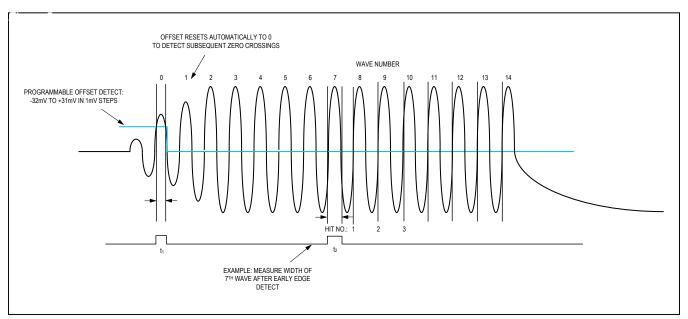


Figure 5. Early Edge Detect Received Wave Example

Temperature Measurement Operations

A temperature measurement is a time measurement of the RC circuit connected to the temperature port device pins T1 through T4 and TC. The TC device pin has a driver to charge the timing capacitor. The ports that are measured and the order in which the measurement is performed is selected with the TP[1:0] bits in the Temperature register.

<u>Figure 6</u> depicts a 1000 Ω platinum RTD with a 100nF NPO COG 30ppm/°C capacitor. It shows two dummy cycles with 4 temperature port evaluation measurements and 4 real temperature port measurements. This occurs when setting the TP[1:0] bits in the Temperature register to 11b.

The dummy 1 and dummy 2 cycles represent preamble measurements that are intended to eliminate the dielectric absorption of the temperature measurement capacitor. These dummy cycles are executed using a RTD Emulation resistor of 1000Ω internal to the MAX35102. This dummy path allows the dielectric absorption effects of the capacitor to be eliminated without causing any of the RTDs to be unduly self-heated. The number of dummy measurements to be taken ranges from 0 to 7. This parameter is configured by setting the PRECYC[2:0] bits in the Temperature register.

Following the dummy cycles, an evaluation, TXevaluate, is performed. This measurement allows the MAX35102

to maximize power efficiency by evaluating the temperature of the RTDs with a coarse measurement prior to a real measurement. The coarse measurement provides an approximation to the TDC converter. During the real measurement, the TDC can then optimize its measurement parameters to use power efficiently. These evaluate cycles are automatically inserted according to the order of ports selected with the of the Temperature Port bits. The time from the start of one port's temperature measurement to the next port's temperature measurement is set using with the PORTCYC[1:0] bits in the Temperature register.

Once all the temperature measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register is also set and the INT pin asserts (if enabled).

Actual temperature is determined by a ratiometric calculation. If T1 and T2 are connected to platinum RTDs and T3 and T4 are connected to the same reference resistor (as shown in the System Diagram), then the ratio of T1/T3 = R_{RTD1}/R_{REF} and $T2/T4 = R_{RTD2}/R_{REF}$. The ratios R_{RTD1}/R_{REF} and R_{RTD2}/R_{REF} can be determined by the host microprocessor and the temperature can be derived from a look-up table of Temperature vs. Resistance for each of the RTDs utilizing interpolation of table entries if required.

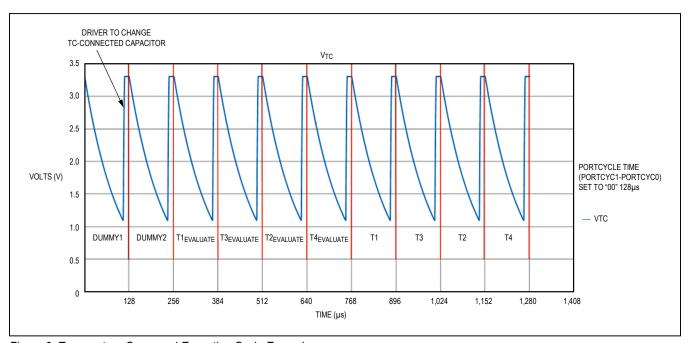


Figure 6. Temperature Command Execution Cycle Example

Temperature Error Handling

The temperature measurement unit can detect open and/ or short-circuit temperature probes. If the resultant temperature reading in less than 8µs, then the MAX35102 writes a value of 0000h to the corresponding Results registers to indicate a short-circuit temperature probe. If the measurement process does not discharge the TC pin below the threshold of the internal temperature comparator within 2µs of the time set by the PORTCYC[1:0] bits in the Temperature register, then an open circuit temperature probe error is declared. The MAX35102 writes a value of FFFFh to the corresponding results registers to indicate an open circuit temperature probe, the TO bit in the Interrupt Status register is set, and the INT pin asserts (if enabled). If the temperature measurement error is caused by any other problems, then the MAX35102 writes a value of FFFFh to each of the temperature port results registers indicating that all of the temperature port measurements are invalid.

Calibration Operation

For more accurate results, calibration of the TDC can be performed. Calibration allows the MAX35102 to perform a calibration measurement that is based upon the 32.768kHz crystal, which is the most accurate clock in the system. This calibration is used when a ceramic oscillator is used in place of an AT-cut crystal for the 4MHz reference. The MAX35102 automatically generates START and STOP signals based upon edges of the 32.768kHz clock. The number of 32.768kHz clock periods that are used and then averaged are selected with the CAL_PERIOD[3:0] bits in the Calibration and Control register. The TDC measures the number of 4MHz clock pulses that occur during the 32.768kHz pulses. The measured time of a 32.768kHz clock pulse is reported in the CalibrationInt and CalibrationFrac Results registers.

Following is a description of an example calibration. Each TDC measurement is a 15-bit fixed-point integer value concatenated with a 16-bit fractional value binary representation of the number of t_{4MHz} periods that contribute to the time result, the actual period of t_{4MHz} needs to be known. If the CAL_PERIOD[3:0] bits in the Calibration and Control register are set to 6, then 6 measurements of 32.768kHz periods are measured by the TDC and then averaged. The expected measured value would be 30.5176 μ s/250ns = 122.0703125 t_{4MHz} periods. Assume that the 4MHz ceramic resonator is actually running at 4.02MHz. The TDC measurement unit would then measure 30.5176 μ s/248.7562ns = 122.6806641 t_{4MHz} periods and this result would be

returned in the Calibration Results register. For all TDC measurements, a gain value of 122.0703125/122.6806641 = 0.995024876 would then be applied.

Calibration is performed when the Calibration command is sent to the MAX35102. At the completion of this calibration, the CAL bit in the Interrupt Status register and the INT pin asserts (if enabled).

Error Handling During Calibration

Any errors that occur during the Calibrate command stop the CalibrationInt and the CalibrationFrac Results registers from being updated with new calibration coefficients. The results for the previous Calibration data remain in these two registers and are used for scaling measured results. If the calibration error is caused by the internal calibration time measurement exceeding the time set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the INT pin asserts (if enabled).

Device Interrupt Operations

The MAX35102 is designed to optimize the power efficiency of a flow metering application by allowing the host microprocessor to remain in a low-power sleep mode, instead of requiring the microprocessor to keep track of complex real-time events being performed by the MAX35102. Upon completion of any command, the MAX35102 alerts the host microprocessor using the $\overline{\text{INT}}$ pin. The assertion of the $\overline{\text{INT}}$ pin can be used to awaken the host microprocessor from its low power mode. Upon receiving an interrupt on the $\overline{\text{INT}}$ pin, the host microprocessor should read the Interrupt Status Register to determine which tasks were completed.

Interrupt Status Register

The interrupt status register contains flags for all for all commands and events that occur within the MAX35102. These flags are set when the event occurs or at the completion of the executing command. When the Interrupt Status Register is read, all asserted bits are cleared. If another interrupt source has generated an interrupt during the read, these new flags assert following the read.

INT Pin

The INT pin asserts when any of the bits in the Interrupt Status register are set. The INT pin remains asserted until the Interrupt Status register is read by the user and all bits in this register are clear. In order for the INT pin to operate, it must first be enabled by setting the INT_EN bit in the Calibration and Control register.

Serial Peripheral Interface Operation

Four pins are used for SPI-compatible communications: DOUT (serial-data out), DIN (serial-data in), $\overline{\text{CE}}$ (chip enable), and SCK (serial clock). DIN and DOUT are the serial data input and output pins for the devices, respectively. The $\overline{\text{CE}}$ input initiates and terminates a data transfer. SCK synchronizes data movement between the master (microcontroller) and the slave (MAX35102). The SCK, which is generated by the microcontroller, is active only when $\overline{\text{CE}}$ is low and during opcode and data transfer to any device on the SPI bus. The inactive clock polarity is logic-low. DIN is latched on the falling edge of SCK. There is one clock for each bit transferred. Opcode bits are transferred in groups of sixteen, MSB first.

The serial peripheral interface is used to access the features and memory of the MAX35102 using an opcode/command structure.

Opcode Commands

 $\underline{\text{Table 2}}$ shows the opcode/commands that are supported by the device.

Execution Opcode Commands

The device supports several single byte opcode commands that cause the MAX35102 to execute various routines. All commands have the same SPI protocol sequence as shown in Figure 7. Once all 8 bits of the opcode are received by the MAX35102 and the $\overline{\text{CE}}$ device pin is deasserted, the MAX35102 begins execution of the specified command as described in that Command's description.

TOF UP Command (00h)

The TOF_UP command generates a single TOF measurement in the upstream direction. Pulses launch from the LAUNCH_UP pin and are received by the STOP_UP pin. The measured hit results are reported in the HITxUPInt and HITxUPFrac registers, with the calculated average of all the measured hits being reported in the AVGUPInt and AVGUPFrac register. The t_1/t_2 and t_2/t ideal wave ratios are reported in the WVRUP register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Note: The TOF_UP command yields a result that is only of use when used in conjunction with the TOF_DN command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

Table 2. Opcode Commands

GROUP	COMMAND	OPCODE FIELD (HEX)
	TOF_Up	00h
	TOF_Down	01h
Execution	TOF_Diff	02h
Opcode	Temperature	03h
Commands	Reset	04h
	Initialize	05h
	Calibrate	0Eh
Register Opcode	Read Register	B0h thru FFh. Each hex value represents the location of a single 16-bit register
Commands	Write Register	30h thru 43h. Each hex value represents the location of a single 16-bit register

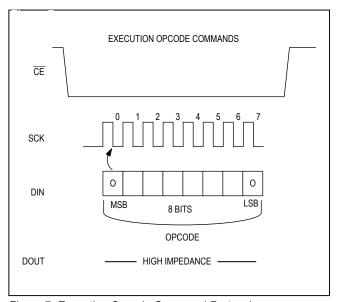


Figure 7. Execution Opcode Command Protocol

TOF_Down Command (01h)

The TOF_DOWN command generates a single TOF measurement in the downstream direction. Pulses launch from the LAUNCH_DN pin and are received by the STOP_DN pin. The measured hit results are reported in the HITxDnInt and HITxDnFrac registers, with the calculated average of all the measured hits being reported in the AVGDNInt and AVGDNFrac register. The t_1/t_2 and t_2/t_{ideal} wave ratios are reported in the WVRDN register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled).

Note: The TOF_Down command yields a result that is only of use when used in conjunction with the TOF_UP command. Absolute TOF measurements include circuit delays and cannot be considered accurate.

TOF_DIFF Command (02h)

The TOF_DIFF command performs back-to-back TOF_UP and TOF_DN measurements as required for a metering application. The TOF_UP sequence is followed by the TOF_DN sequence. The time between the start of the TOF_UP measurement and the start of the TOF_DN measurement is set by the TOF_CYC[2:0] bits in the TOF2 register. Upon completion of the TOF_DN measurement, the results of AVGUP minus AVGDN is computed and stored at the TOF_DIFFInt and TOF_DIFFFrac Results register locations. Once these results are stored, then the TOF bit in the Interrupt Status register is set and the INT pin asserts (if enabled).

Temperature Command (03h)

The temperature command initiates a temperature measurement sequence as described in the <u>Temperature Measurement Operations</u> section. The characteristics the temperature measurement sequence depends upon the settings in the Temperature register. Once all the measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The <u>TE</u> bit in the Interrupt Status register also is set and the <u>INT</u> pin asserts (if enabled).

Reset Command (04h)

The reset command essentially performs the same function as a power-on reset (POR), and causes all of the Configuration registers to be set to their power-on reset values and all of the Results registers and the Interrupt Status register to be cleared and set to zero.

Initialize Command (05h)

The initialize command must be executed before any configuration of the device is done. This initializes the time-to-digital converter so that TOF and temperature commands can be executed. The MAX35102 sets the INIT bit in the Interrupt Status register and asserts the INT device pin (if enabled) to tell the host microprocessor that the initialize command has completed and the next desired command can be sent to the MAX35102.

Calibrate Command (0Eh)

The calibrate command performs the calibration routine as described in the calibration operation section. When the calibrate command has completed the measurement, the Calibration Results register contains the measured 32kHz period measurement value, the MAX35102 sets the calibration bit in the Interrupt Status register and then asserts the $\overline{\text{INT}}$ device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source and then read the Calibration Results register to be able to calculate the 4MHz ceramic oscillator gain factor.

Register Opcode Commands

To manipulate the register memory, there are two commands supported by the device: Read Register and Write register. Each register accessed with these commands is 16 bits in length. These commands are used to access all sections of the memory map including the Configuration registers, Conversion Results registers, and Status registers. The Conversion Results registers and the Interrupt Status register of the Status registers are all read only.

Read Register Command

The opcode must be clocked into the DIN device pin before the DOUT device pin produces the register data. The SPI protocol sequence is shown in Figure 8.

The read register command can also be used to read consecutive addresses. In this case, the data bits are continuously delivered in sequence starting with the MSB of the data register that is addressed in the opcode, and continues with each SCK rising edge until the $\overline{\text{CE}}$ device pin is deasserted as shown in Figure 9. The address counter automatically increments.

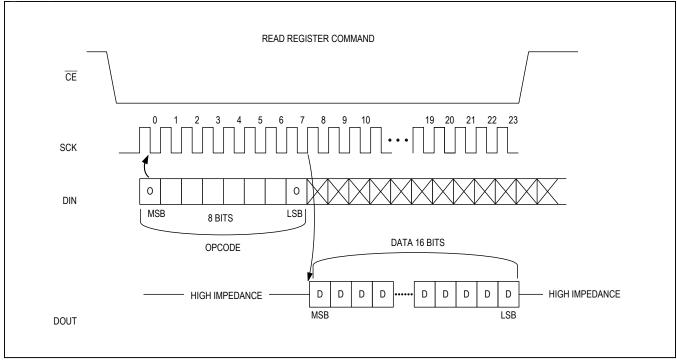


Figure 8. Read Register Opcode Command Protocol

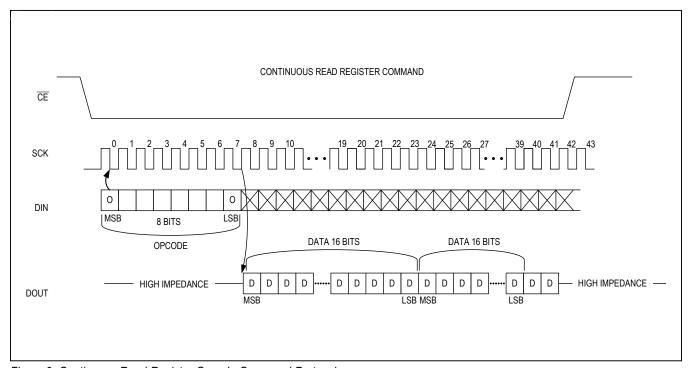


Figure 9. Continuous Read Register Opcode Command Protocol

Write Register Command

This command applies to all writable registers. See the <u>Register Memory Map</u> for more detail. The SPI protocol sequence is shown in Figure 10.

The write register command can also be used to write consecutive addresses. In this case, the data bits are continuously received on the DIN device pin and bound for the initial starting address register that is addressed in the opcode. The address counter automatically increments

after each 16 bits of data if the SCK device pin is continually clocked and the $\overline{\text{CE}}$ device pin remain asserted as shown in Figure 11.

Register Memory Map

These registers are accessed by the read register command and the Write Register command: X represents a reserved bit. All addresses omitted are reserved

The Results, Interrupt Status, and Control registers are all 0000h following a reset.

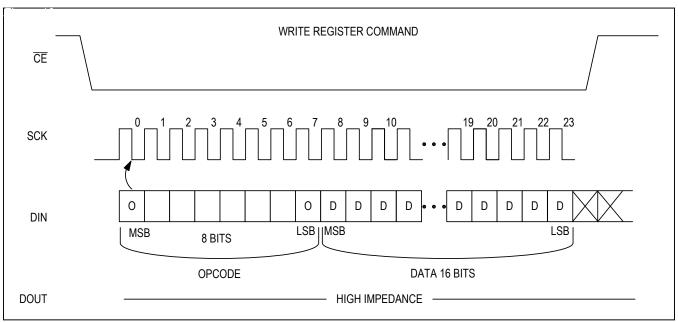


Figure 10. Write Register Opcode Command Protocol

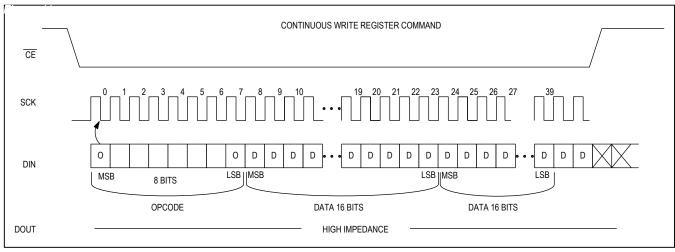


Figure 11. Continuous Write Register Opcode Command Protocol

Table 3. Register Memory Map

READ	WRITE	NAME				BITS[15:8]	15:8]							BITS	BITS[7:0]			
CONFIGUR	CONFIGURATION REGISTERS	ISTERS																
B6h	36h									Reserved	,ved							
B7h	37h									Reserved	,ved							
B8h	38h	TOF1	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DPL3	DPL2	DPL1	DPL0	STOP_POL_	×	CT1	СТО
B9h	39h	TOF2	STOP 2	STOP 1	STOP 0	T2WV 5	T2WV	T2WV 3	T2WV	T2WV	T2WV0	TOF_ CYC2	TOF_ CYC1	TOF_ CYC0	P_DN	TIM OUT2	TIM OUT1	TIM OUT0
BDh	3Dh	TOF6	C_OF FSET RUP7	C_OF FSET RUP6	C_OF FSET RUP5	C_OF FSET RUP4	C_OF FSET RUP3	C_OF FSET RUP2	C_OF FSET RUP1	C_OF FSET RUP0	C_OF FSET UP7	C_OF FSET UP6	C_OF FSET UP5	C_OF FSET UP4	C_OF FSET UP3	C_OF FSET UP2	C_OF FSET UP1	C_OF FSET UP0
BEh	3Eh	T0F7	C_OF FSET RDN7	C_OF FSET RDN6	C_OF FSET RDN5	C_OF FSET RDN4	C_OF FSET RDN3	C_OF FSET RDN2	C_OF FSET RDN1	C_OF FSET RDN0	C_OF FSET DN7	C_OF FSET DN6	C_OF FSET DN5	C_OF FSET DN4	C_OF FSET DN3	C_OF FSET DN2	C_OF FSET DN1	C_OF FSET DN0
COh	40h	Temperature	×	×	×	×	×	×	×	×	×	TP1	TP0	PREC YC2	PREC YC1	PREC YC0	PORT CYC1	PORT CYC0
C1h	41h	TOF Measure- ment Delay	DLY15	DLY14	LY13	DLY12	DLY11	DLY10	DLY9	DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
CZh	42h	Calibration and Control	×	×	×	×	CMP_ EN	CMP_ SEL	F _N N	ET_ CONT	CONT	CLK_ S2	CLK_ S1	CLK_ S0	Cal_P eriod3	Cal_P eriod2	Cal_P eriod1	Cal_P eriod0
C3h	43h	Oscillator	×	×	×	×	×	×	×	×	×	32K_ BP	32K_ EN	×	×	×	×	×
CONVERS	ION RESULT	CONVERSION RESULTS REGISTERS	s															
C4h	Read Only		WVRUP															
C5h	Read Only		Hit1UpIn1	#														
C6h	Read Only		Hit1UpFr	rac														
C7h	Read Only		Hit2UpInt	t t														
C8h	Read Only		Hit2UpFrac	rac														
C9h	Read		Hit3UpInt	<u> </u>														

Table 3. Register Memory Map (continued)

OPCODDE MACGUPINT CONTROL Read Only AVGUPINT AVGUPINT Read Only HITDDINIT AVGUPINT Read Only HITDDINIT AVGUPINT Read Only HITDDINIT AVGDNINT Read Only HITGDINIT AVGDNINT Read Only AVGDNINT AVGDNINT Read Only AVGDNINT AVGDNINT Read Only TOF_DIFFIN AVGDNINT	READ	WRITE	E A	N-TISTIA 81TSM 8-18	
Read Only Read	ЭРСОВЕ				
Read Only Read	CAh	Read Only		Hit3UpFrac	
Read Only Read	D1h	Read Only		AVGUPInt	
Read Only Read	D2h	Read Only		AVGUPFrac	
Read Only Read	D3h	Read Only		WVRDN	
Read Only Read	D4h	Read Only		Hit1DnInt	
Read Only Read	D5h	Read Only		Hit1DnFrac	
Read Only Read	D6h	Read Only		HitzDnint	
Read Only Read	D7h	Read Only		Hit2DnFrac	
Read Only	D8h	Read Only		Hit3DnInt	
Read Only	D9h	Read Only		Hit3DnFrac	
Read Only Read Only Read Only Read Only Read Only Read Only	EOh	Read Only		AVGDNInt	
Read Only Read Only Read Only Read Only Read Only	E1h	Read Only		AVGDNFrac	
Read Only Read Only Read Only Read Only	E2h	Read Only		TOF_DIFFInt	
Read Only Read Only Conly Only	E3h	Read Only		TOF_DIFFFrac	
Read Only Read Only	E7h	Read Only		T1Int	
Read	E8h	Read Only		T1Frac	
	E9h	Read		T2Int	

Table 3. Register Memory Map (continued)

													×
													×
													POR
	BITS[7:0]												IN
	ВП												×
													×
													CAL
													×
													×
													×
													ГВО
	BITS[15:8]												2
	BITS												TOF
													×
						tionInt	CalibrationFrac	pe	pe	pe	pe		×
T2Frac		T3Int	T3Frac	T4Int	T4Frac	CalibrationInt	Calibra	Reserved	Reserved	Reserved	Reserved		01
	NAME												Interrupt Status
Read	WRITE OPCODE	Read	Read	Read	Read Only	Read	Read	Read Only	Read Only	Read Only	Read Only	STATUS REGISTERS	Read
EAh	READ OPCODE	EBh	ECh	EDh	чээ	F8h	F9h	FAh	FBh	FCh	FDh	STATUS R	FEh

Configuration Register Descriptions

Table 4. TOF1 Register

WF	RITE OPCODE 38h	RI	EAD OPCODE B8h		POWE	R-ON RESET 0010h	VALUE		
Bit	15	14	13	12	11	10	9	8	
Name	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	
Bit	7	6	5	4	3	2	1	0	
Name	DPL3	DPL2	DPL1	DPL0	STOP_POL	Х	CT1	СТО	
BIT	NAME				DESCRIPTION	I			
15:8	PL[7:0]	from the PL[7:0] is	nuncher Size: Thi pulse launcher du s set to 00h, the P e pulse count is cl	ring transmiss ulse Launcher	ion. The range o	f this hex value	e is 00h to FFh.	When	
		used to d for the int clock. Th 2MHz clo	unch Divider: The rive the Pulse Landernal clock refere e range of this he lock. A value of 0h unch Frequency =	unch signal. Thence. The interior or value is 1h to is not supporte	ne 4MHz externa nal reference clo o Fh, resulting in nd and should no	I reference oso ck is first divide a range of divi	cillator is used a ed by 2 to prodi ision from ÷2 to	as the source uce a 2MHz	
7:4	DPL[3:0]		DPL[3:0]		PULSE LA	UNCH FREQU	ENCY	
	[]		000			F	RESERVED		
			000				1MHz		
			000	2b			666kHz		
							422 2241-		
			1110b 133.33kHz 1111b 125kHz						
3	STOP_POL	signal red internal T the STOR	Stop Polarity: This bit defines the edge sensitivity of the STOP_UP and STOP_DN channel. The signal received on the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the rising slope of this signal if this bit is set to 0. The signal received or the STOP_UP and STOP_DN device pins will generate a stop condition for the internal TDC time count on the falling slope of this signal if this bit is set to 1.						
2	X	Reserved	d						

Table 4. TOF1 Register (continued)

BIT	NAME			DESCRIPTION	
				otted for charging the external bia for the analog receiver/comparat	
				DESCRI	PTION
1:0	CT[1:0]	CT1	СТ2	32kHz CLOCK CYCLES (decimal)	TYPICAL TIME (µs)
		0	0	2	61
		0	1	4	122
		1	0	8	244
		1	1	16	488

Table 5. TOF2 Register

WR	ITE OPCODE 39h		REA	AD OPCODE B9h		POWER-ON RESET VALUE 0000h					
Bit	15	14	4	13	12	11	10	9	8		
Name	X	STC		STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1		
				l			1	,			
Bit	7	6	6	5 4 3 2 1							
Name	T2WV0	TOF_0	CYC2	C2 TOF_CYC1 TOF_CYC0 X TIMOUT2 TIMO					TIMOUT0		
BIT	NAME					DESCRIP	TION				
15	Х		Reserved								
			Stop	Hits: These bits	s set the number	of stop hits	o be expected a	nd measured.			
			STOP1 ST		STOP	0	DESCRIP	TION			
14:13	STOP[1:	01	0			0		1 Hi	t		
14.10	0101[1.	0]		0		1		2 Hits			
				1		0		3 Hits			
				1		1		3 Hit	s		
			Wave Selector for t ₂ : These bits determine the wave number for which t ₂ is measured ensure measurement accuracy, the first wave measurable after the early edge detect is v 2. Waves are numbered as depicted in Figure 5.								
12:7	T2WV[5:	0]		T2WV[5:0	DESCRIPTION						
	•	12WV[5:0]			0 through 2			Wave 2			
					3			Wave 3			
					4			Wave 4			

Table 5. TOF2 Register (continued)

BIT	NAME		TOF Duty Cycle: These bits determine the time delay between successive executions of										
		TOF measurements. It TOF_DN and is application.	is the start-to-start tin able only for the TOF_ DF of the acoustic path	ne of automatic exec DIFF command. It is n exceeds the progra	cution of the TOF_UP and the s based upon the 32.768kHz ammed start-to-start time in								
			DESCRIPTION										
0.4	TOF_CYC[2:0]	TOF_CYC[2:0]	32kHz CLOCK CYCLES (decimal)	TYPICAL TIME	4MHz ON BETWEEN TOF_ UP and TOF_DOWN								
6:4	TOF_CYC[2:0]	000b	0	0µs	Yes								
		001b	4	122µs	Yes								
		010b	8	244µs	Yes								
		011b	16	488µs	Yes								
		100b	24	732µs	Yes								
		101b	32	976µs	Yes								
		110b	546	16.65ms	No								
		111b	655	19.97ms	No								
3	X	Reserved											
		time, the TO bit in the	rt _{2,} or Hit1 through Hit Interrupt Status registe	t3 of the received siger is set and the INT	rement block. If the hit inal does not occur in this pin is asserted (if enabled). In if the data for that register is								
		TIMOUT2	TIMOUT1	TIMOUT0	DESCRIPTION (μs)								
		0	0	0	128								
2:0	TIMOUT[2:0]	0	0	1	256								
		0	1	0	512								
		0	1	1	1024								
		1	0	0	2048								
		1	0	1	4096								
		1	1	0	8192								
		1	1	1	16384								

Table 6. TOF6 Register

WF	RITE OPCODE 3Dh		READ OPCODE BDh		POWER-ON RESET VALUE 0000h					
Bit	15	14	13	12	11	10	9	8		
Name	Х	Х	Х	Х	Х	Х	Х	Х		
Bit	7	6	5	4	3	2	1	0		
Name	Х	Х	X C_OFFSET C_OFFSET C_OFFSET UP4 UP3 UP2 UP1							
BIT	NAME	NAME DESCRIPTION								
15:5	Х		Reserved							
4:0	C_OFFSE [4:0]	TUP	comparator Offset voltage for the analo the early edge wave the voltage present When the STOP_PO the zero crossing of When the STOP_PO the zero crossing of The following formu STOP_POL = STOP_POL =	og receiver compared to preceive to compared to preceive to compared to preceive the received according to the received ac	common-mode of register is set coustic wave, the coustic wave, the coustic wave, the comparator offset voltary of the coustic wave.	d. This comparativoltage is depertured in the comparativoltage in the comparativoltage setting tage = V _{CC} ×	ator offset is used and ent upon and a rising edge tor offset is a period of a falling edge tor offset is a new confiset in the new confiset is new confised in the new confis	ed to detect discales with deduction of positive value. e detection of egative value.		
			C_OFF	SETUP[4:0]		OF	FSET (LSBs)			
			00h t	hrough 1Fh		0	through 31			

Table 7. TOF7 Register

Bit 15 14 13 12 11 10 9 8 8 Name X X X X X X X X X X X X X X X X X X X	WR	RITE OPCODE 3Eh		READ OPCODE BEh		POW	ER-ON RESET 0000h	VALUE	
Bit 7 6 5 4 3 2 1 0 Name X X X X C_OFFSET C_OFFSET C_OFFSET C_OFFSET DN1 DN2 DN1 DN0 BIT NAME DESCRIPTION 15:5 X Reserved Comparator Offset Downstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t ₁ . The actual common-mode voltage is dependent upon and so with the voltage present at the V _{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection the zero crossing of the received acoustic wave, then the comparator offset is a positive value when the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection the zero crossing of the received acoustic wave, then the comparator offset is a negative value acoustic wave, then the comparator offset is a negative value acoustic wave, then the comparator offset is a negative value acoustic wave, then the comparator offset is a negative value acoustic wave, then the comparator offset is a negative value acoustic wave, then the comparator offset voltage setting: STOP_POL = 0 Comparator Offset Voltage = V _{CC} × (1152 + C _{OFFSETDN})/3072 STOP_POL = 1 Comparator Offset Voltage = V _{CC} × (1151-C _{OFFSETDN})/3072 where 1 LSB = V _{CC} /3072	Bit	15	14	13	12	11	10	9	8
Name X X X X C_OFFSET DNA C_OF	Name	Х	Х	Х	Х	Х	Х	Х	Х
BIT NAME 15:5 X Reserved Comparator Offset Downstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t₁. The actual common-mode voltage is dependent upon and so with the voltage present at the V _{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection the zero crossing of the received acoustic wave, then the comparator offset is a positive value when the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection the zero crossing of the received acoustic wave, then the comparator offset is a negative value that the test of the zero crossing of the received acoustic wave, then the comparator offset is a negative value that the test of the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the ze	Bit	7	6	5	4	3	2	1	0
Tomparator Offset Downstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1 . The actual common-mode voltage is dependent upon and so with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection the zero crossing of the received acoustic wave, then the comparator offset is a positive value when the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection the zero crossing of the received acoustic wave, then the comparator offset is a negative value the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the c	Name	х	Х	1 X 1 = 1 = 1 = 1					
4:0 Comparator Offset Downstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1 . The actual common-mode voltage is dependent upon and so with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection the zero crossing of the received acoustic wave, then the comparator offset is a positive value when the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection the zero crossing of the received acoustic wave, then the comparator offset is a negative value to zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset is an engative value of the zero crossing of the received acoustic wave, then the comparator offset is a negative value of the zero crossing of the received acoustic wave, then the comparator offset value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator offset is a positive value of the zero crossing of the received acoustic wave, then the comparator	BIT	NAME			-				
offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the early edge wave, t_1 . The actual common-mode voltage is dependent upon and so with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection the zero crossing of the received acoustic wave, then the comparator offset is a positive value when the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a negative value to the zero crossing of the received acoustic wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive value wave, then the comparator offset is a positive valu	15:5	Х		Reserved					
C_0113E1DN[4.0] 0113E1 (E3BS)	4:0		ΓDN	offset voltage for the a detect the early edge with the voltage prese When the STOP_POL the zero crossing of th When the STOP_POL the zero crossing of th The following formulas STOP_POL = STOP_POL = where 1 LSB =	analog receiver wave, t ₁ . The a nt at the V _{CC} point in the TOF the received according to the the cordinary of the received according to the rece	comparator from the comparator from the common- bins. I register is set ustic wave, then the comparator offset voltars of the comparator offset voltars.	nt-end. This cormode voltage is to zero indicatir in the comparate to one indicatin in the comparate voltage setting: tage = V _{CC} × age = V _{CC} ×	mparator offset dependent up ng a rising edge or offset is a po g a falling edge or offset is a ne (1152 + C _{OF})	is used to on and scales e detection of sitive value. e detection of gative value.

Table 8. Temperature Register

	E OPCODE 40h	READ C	_		POWE	R-ON RESET 0000h	VALUE	
Bit	15	14	13	12	11	10	9	8
Name	X	X X	X	X X	X	X	X	X
ivame	Λ							
Bit	7	6	5	4	3	2	1	0
Name	Х	TP1	TP0	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC
BIT	NAME			J	DESCRIPTIO	N	<u> </u>	I
15:7	Х	Reserved						
				e bits set the nu t sequence and				
		TP1	TP0			DESCRIPTION	I	
6:5	TP[1:0]	0	0	Measure port	s T1 and T3			
		0	1	Measure port	s T2 and T4			
		1	0	Measure ports	s T1, T3, and T	2		
		1	1	Measure port	s T1, T3, T2, ar	d T4		
			emberature (Svcie: These 3	bits are used to	set the numb	er of cycles to ι	use as
		preamble for comprises or	reducing die	lectric absorption	on of the tempe at sequence as	rature measure defined by the	TP[1:0] bits.	r. Each cycle
		preamble for comprises or PREC	reducing die ne temperatui	lectric absorption measuremer PRECYC1	on of the tempe at sequence as	rature measure defined by the	ement capacito TP[1:0] bits. DESCR	r. Each cycle
		preamble for comprises of	reducing die ne temperatur CYC2	lectric absorption re measurement PRECYC1	on of the tempe it sequence as PREC	rature measure defined by the CYC0	ement capacito TP[1:0] bits. DESCR 0 dumn	r. Each cycle RIPTION ny cycle
4:2	PRECYC[2:0]	preamble for comprises of PREC	reducing die ne temperatur CYC2	PRECYC1 0 0	on of the tempe it sequence as PREC	rature measure defined by the CYC0	ement capacito TP[1:0] bits. DESCR 0 dumn 1 dumm	r. Each cycle RIPTION ny cycle ny cycles
4:2	PRECYC[2:0]	preamble for comprises of PREC	reducing die ne temperatur CYC2	PRECYC1 0 0 1	on of the tempe it sequence as PREC	rature measure defined by the CYC0	pement capacito TP[1:0] bits. DESCR 0 dumn 1 dumm 2 dumm	RIPTION ny cycle ny cycles ny cycles
4:2	PRECYC[2:0]	preamble for comprises or PREC	reducing die ne temperatur CYC2))	PRECYC1 0 0 1	on of the tempe it sequence as PREC	rature measure defined by the CYC0)	DESCR 0 dumn 1 dumm 2 dumm 3 dumm	RIPTION ny cycle ny cycles ny cycles ny cycles
4:2	PRECYC[2:0]	preamble for comprises of PREC	reducing die ne temperatur CYC2	PRECYC1 0 0 1 1 0	on of the tempe it sequence as PREC	rature measure defined by the CYCO	pement capacito TP[1:0] bits. DESCR 0 dumn 1 dumm 2 dumm 3 dumm 4 dumm	RIPTION my cycle my cycles my cycles my cycles my cycles my cycles my cycles
4:2	PRECYC[2:0]	PREC	reducing die ne temperatur CYC2	PRECYC1 0 0 1 1 0 0	on of the tempe it sequence as PREC	rature measure defined by the CYCO)	DESCF O dumn 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm	RIPTION The cycle of the cycles of the cycl
4:2	PRECYC[2:0]	preamble for comprises of PREC	reducing die ne temperatur CYC2)))) 1	PRECYC1 0 0 1 1 0 0 1	on of the tempe It sequence as PREC (rature measure defined by the CYCO) I) I)	DESCR O dumn 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm 6 dumm	r. Each cycle RIPTION ny cycle ny cycles
4:2	PRECYC[2:0]	PREC	reducing die ne temperatur CYC2)))) 1	PRECYC1 0 0 1 1 0 0 1 1 1 1 1 1 1	on of the tempe it sequence as PREC	rature measure defined by the CYCO)	DESCF O dumn 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm 6 dumm 7 dumm	RIPTION The cycle of the cycles of the cycl
4:2	PRECYC[2:0]	Preamble for comprises of PREC	reducing die ne temperatur CYC2)))) 1 1 1 Fime: These t port measure te temperatur	PRECYC1 0 0 1 1 0 0 1	PREC	rature measure defined by the CYCO)	DESCF O dumn 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm 7 dumm ressive individu so define the ti	r. Each cycle RIPTION my cycle my cycles mu cycles mu cycles mu cycles mu cycles mu cycles
		Port Cycle 1 temperature function of the	reducing die ne temperatur CYC2)))) 1 1 1 Fime: These t port measure te temperatur ills.	PRECYC1 0 0 1 1 0 1 two bits define tements. It is a se measurements.	PREC	rature measure defined by the CYCO)	DESCF O dumn 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm 7 dumm ressive individu so define the ti	r. Each cycle RIPTION ny cycle ny cycles
4:2	PRECYC[2:0] PORTCYC[1:0]	Port Cycle 1 temperature function of the timeout deta	reducing die ne temperatur CYC2))))) 1 1 1 I Fime: These t port measure temperatur ils. CYC1	PRECYC1 0 0 1 1 0 0 1 two bits define tements. It is a see measurement.	PRECOME TO STATE OF THE PRECOM	rature measure defined by the CYCO)	DESCF O dumm 1 dumm 2 dumm 3 dumm 4 dumm 5 dumm 7 dumm ressive individution define the ti	r. Each cycle RIPTION ny cycle ny cycles
		Port Cycle 1 temperature function of tr timeout deta Present comprises of the comprises of the comprises of the comprises of the comprise of	reducing die ne temperatur CYC2))))) I I I I Fime: These t port measure temperatur ills.	PRECYC1 0 0 1 1 0 1 two bits define tements. It is a see measurements.	pro of the tempe at sequence as PREC ((((((((((((((((((rature measure defined by the CYCO)	DESCRIPTION (p	RIPTION The cycle of the cycles of the cycl
		Port Cycle 1 temperature function of th timeout deta PORT	reducing die ne temperatur CYC2))))) I I I I Fime: These t port measure temperatur ills.	PRECYC1 0 0 1 1 0 1 two bits define tements. It is a see measurement.	PRECO On of the tempe at sequence as PRECO ON of the t	rature measure defined by the CYCO)	DESCRIPTION (p	r. Each cycle RIPTION ny cycle ny cycles

Table 9. ToF Measurement Delay Register

WF	RITE OPCODE 41h	RE	AD OPCODE C1h		POWER-ON RESET VALUE 0000h					
Bit Name	15 DLY15	14 DLY14	13 DLY13	12 DLY12	11 DLY11	10 DLY10	9 DLY9	8 DLY8		
Bit	7	6	5	4	3	2	1	0		
Name	DLY7	DLY6 DLY5 DLY4 DLY3 DLY2 D						DLY0		
BIT	NAME				DESCRIPTIO	ON				
15:0	DLY[15:0]	4MHz cr analog c condition has expi	This is hexadecimal value ranging from 0000h to FFFFh (decimal 0 to 65535). It is a multiple of 4MHz crystal period (250ns). Settings less than 0012h are reserved and should not be used. It analog comparator driven by the STOP_UP and STOP_DN device pins does not generate a strondition until this delay, counted from the internally generated start pulse for the acoustic was has expired. This delay applies to early edge detect wave. Care must be taken to set the TIMO bits in the TOF2 register so that a timeout interrupt does not occur before this delay expires.							

Table 10. Calibration and Control Register

WR	RITE OPCODE 42h	REA	AD OPCODE C2h		POWI	ER-ON RESET 0000h	VALUE	
Bit	15	14	13	12	11	10	9	8
Name	Х	Х	Х	Х	CMP_EN	CMP_SEL	INT_EN	Х
Bit	7	6	5	4	3	2	1	0
Name	X CLK_S2 CLK_S1		CLK_S0	CAL_ PERIOD3	CAL_ PERIOD2	CAL_ PERIOD1	CAL_ PERIOD0	
BIT	NAME				DESCRIPTIO	N		
15:12	15:12 X Reserved							
11	CMP_EN	Comparator/UP_DN Output Enable: 1 = CMP_OUT/UP_DN output device pin is enabled. 0 = CMP_OUT/UP_DN output device pin is driven low.						

Table 10. Calibration and Control Register (continued)

BIT	NAME			DESCRIF	PTION						
10	CMP_SEL	pin and is only us 1 = CMP_EN: The 0 = UP_DN: The High Output: Up	ed when CMP_ e output monitor output monitors ostream measur	lect: This bit select EN = 1. rs the receiver fron the launch direction rement (Launch_Ul surement (Launch_	t end comparaton of the pulse la P to STOP_UP)	or output. auncher.	MP_OUT/UP_DN				
9	INT_EN	Interrupt Enable the INT pin.	: This bit, when	set, enables the IN	NT pin. All interru	upt sources a	re wire-ORed to				
8	X	Reserved									
7	X	Reserved									
				define the time into							
		CLK_S2	CLK_S1	CLK_S0		DESCRIPT	ION				
		CLK_52	CLK_S1	CLK_50	32kHz CLOC	K CYCLES	TYPICAL TIME				
		0	0	0	16	3	488µs				
		0	0	1	48	3	1.46ms				
6:4	CLK_S[2:0]	0	1	0	96	3	2.93ms				
		0	1	1	12	8	3.9ms				
		1	0	0	16	8	5.13ms				
		1	0	1	4MHz oscillat	or on continue	ously				
		1	1	0	4MHz oscillat	or on continue	ously				
		1	1	1	4MHz oscillat	or on continue	ously				
		oscillator periods	4MHz Ceramic Oscillator Calibration Period: These bits define the number of 32.768kHz oscillator periods to measure for determination of the 4MHz ceramic oscillator period. 32kHz clock cycles = 1+ CAL_PERIOD[3:0]								
					DESCRI	IPTION					
3:0	CAL_PERIOD[3:0]	CAL_PERIOD[3:0] (decimal) 32kHz CLOCK CYCLES (decimal)									
3.0	CAL_FERIOD[3.0]	0		1			30.5				
		1 2 61									
		14		15			457.7				
		15		16			488.0				

Table 11. Oscillator Register

Wi	RITE OPCODE 43h	REA	READ OPCODE C3h		POWER-ON RESET VALUE 0000h			
Bit	15	14	13	12	11	10	9	8
Name	Х	Х	Х	Х	Х	Х	Х	Х
Bit	7	6	5	4	3	2	1	0
Name	Х	32K_BP	32K_EN	EOSC	Х	X	Х	Х
								'
BIT	NAME				DESCRIPTIO	N		
15:7	Х	Reserved	1					
6	32K_BP	to the 32	ypass: This bit, KX1 device pin. o the MAX3510	The internal 32.			-	
5	32K_EN		32kHz Clock Output Enable: This bit enables the 32KOUT device pin to drive a CMOS-level square wave representation of the 32kHz crystal.					
4	EOSC		Enable Oscillator: This active-low bit when set to logic 0 starts the 32kHz oscillator. When this bit is set to logic 1, the oscillator is stopped.					
3:0	Х	Reserved	Reserved					

Status Register Descriptions

Table 12. Interrupt Status Register

WRITE OPCODE READ OPCODE Read Only FEh					POWER-ON RESET VALUE 0000h			
Bit	15	14	13	12	11	10	9	8
Name	ТО	Х	Х	TOF	TE	Х	Х	Х
Bit	7	6	5	4	3	2	1	0
Name	X	CAL	Х	Х	INIT	POR	Х	Х

Note: This register is read only and bits are self-clearing upon a read to this register. See the *Device Interrupt Operations* section for more information.

BIT	NAME	DESCRIPTION
15	ТО	Timeout: The TO bit is set if any one of the t ₁ , t ₂ , Hit1 through Hit3, or temperature measurements do not occur within the associated timeout window.
14:13	X	Reserved

Table 12. Interrupt Status Register (continued)

BIT	NAME	DESCRIPTION
12	TOF	Time of Flight: Set when the TOF_UP, TOF_DN, or TOF_DIFF command has completed.
11	TE	Temperature: Set when the temperature command has completed.
10:7	X	Reserved
6	CAL	Calibrate: Set after completion of the Calibrate command when the command is manually sent by the host microprocessor.
5	X	Reserved
4	Х	Reserved
3	INIT	Initialize: Set when the Initialize command has completed.
2	POR	Power-On-Reset: Set when the MAX35102 has been successfully powered by application of V _{CC} . Upon application of power, the SPI port becomes inactive until this bit has been set.
1:0	Х	Reserved

Conversion Results Register Descriptions

The devices conversion results registers are all read-only volatile SRAM. The POR value for all registers is 0000h.

Table 13. Conversion Results Registers Description

READ ONLY ADDRESS	NAME	DESCRIPTION							
		Bit 15 through Bit 8 holds the 8-bit value of the pulse width ratio (t ₁ ÷ t ₂).for the upstream measurement. Each bit is weighted as follows:							
		BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		1	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.0078125
C4h	WVRUP	Bit 7 thru bit 0 holds the 8-bit value of the pulse width ratio (t ₂ ÷ t _{ideal}) where t _{ide} al is equal to half the period of the Pulse Launch Frequency for the upstream measurement. Each bit is weighted as follows:							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		1	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.0078125
		The maximum value of each of these ratios is 1.9921875.							
C5h	Hit1UPInt	a binary re	15-bit fixed-point integer value of the first hit in the upstream direction. This integer portion is a binary representation of the number of t_{AMHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{AMHz}$.						
C6h	Hit1UPFrac	representa	16-bit fractional value of the first hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.				,		

Table 13. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME				DESCR	RIPTION			
C7h	Hit2UPInt	15-bit fixed-point integer value of the second hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.							
C8h	Hit2UPFrac	binary repr	16-bit fractional value of the second hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz} .						
C9h	Hit3UPInt	a binary re	presentation	of the numb		periods that o		his integer po the time resu	
CAh	Hit3UPFrac	representa	16-bit fractional value of the third hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz} .						
D1h	AVGUPInt	integer por	tion is a bina	ry represent		number of t ₄₁	_{MHz} periods	upstream dire that contribu	
D2h	AVGUPFrac	fractional p	16-bit fractional value of the average of the hits recorded in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.						
			_	ds the 8 bit v	-	ulse width ra	atio (t ₁ /t ₂).for	the downstr	eam
	WVRDN	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		1	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.0078125
D3h		Bit 7 thru bit 0 holds the 8 bit value of the pulse width ratio (t ₂ /t _{ideal}) where t _{ide} , the period of the pulse launch frequency for the downstream measurement. Ea as follows:							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		1	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.0078125
		The maxim	um value of	each of thes	e ratios is 1.	9921875.	•		•
D4h	Hit1DNInt	15-bit fixed-point integer value of the first hit in the downstream direction. This integer portion is a binary representation of the number of t_{AMHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{AMHz} .							
D5h	Hit1DNFrac	binary repr	16-bit fractional value of the first hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x t_{4MHz} .						
D6h	Hit2DNInt	is a binary	representati	on of the nur		z periods tha		ion. This inte	•

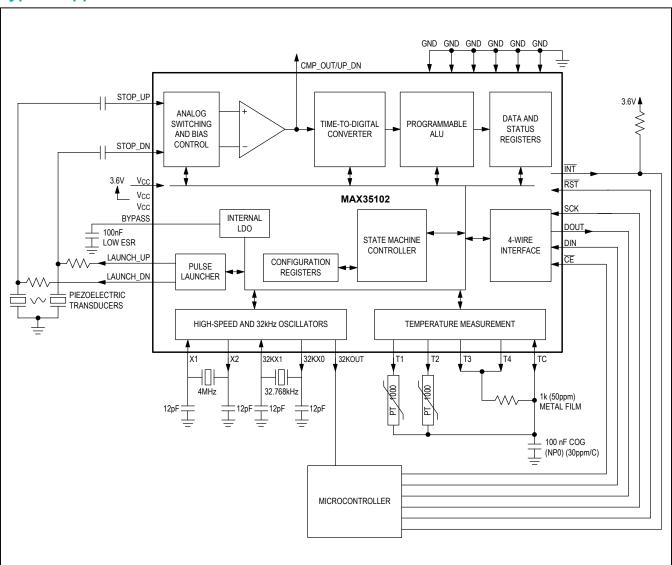
Table 13. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
D7h	Hit2DNFrac	16-bit fractional value of the second hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
D8h	Hit3DNInt	15-bit fixed-point integer value of the third hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$.
D9h	Hit3DNFrac	16-bit fractional value of the third hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E0h	AVGDNInt	15-bit fixed-point integer value of the average of the hit times recorded in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15}-1) \times t_{4MHz}$.
E1h	AVGDNFrac	16-bit fractional value of the average of the hit times recorded in the downstream direction. This fractional portion is a binary representation of one period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
E2h	TOF_DIFFInt	16-bit fixed-point two's-complement integer portion of the difference of the averages for the hits recorded in both the upstream and downstream directions. It is computed as: AVGUP – AVGDN This integer represents the number of t _{4MHz} periods that contribute to computation. The maximum size of the integer is 7FFFh or (2 ¹⁵ – 1) x t _{4MHz} . The minimum size of this integer is 8000h or -2 ¹⁵ x t _{4MHz} .
E3h	TOF_ DIFFFrac	16-bit fractional portion of the two's complement difference of the averages for the hits recorded in both the upstream and downstream directions. This fractional portion is a binary representation of one $t_{\rm 4MHz}$ period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16}$ x $t_{\rm 4MHz}$.
E7h	T1Int	15-bit fixed-point integer value of the time taken to discharge the timing capacitor through the RTD connected to the T1 device pin. This integer portion is a binary representation of the number of t _{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2 ¹⁵ - 1) x t _{4MHz} .
E8h	T1Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T1 device pin. This fractional portion is a binary representation of one t _{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2 ¹⁶ - 1)/2 ¹⁶ x t _{4MHz} .
E9h	T2Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This integer portion is a binary representation of the number of periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2 ¹⁵ - 1) x t _{4MHz} .
EAh	T2Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T2 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.

Table 19. Conversion Results Registers Description (continued)

READ ONLY ADDRESS	NAME	DESCRIPTION
EBh	T3Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This integer portion is a binary representation of the number of t_{4MHZ} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.
ECh	T3Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T3 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$.
EDh	T4Int	15-bit fixed-point integer value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This integer portion is a binary representation of the number of t_{4MHZ} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.
EEh	T4Frac	16-bit fractional value of the time taken to charge the timing capacitor through the RTD connected to the T4 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2 ¹⁶ - 1)/2 ¹⁶ x t_{4MHz} .
F8h	Calibration Int	15-bit fixed-point integer value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2 ¹⁵ - 1) x t_{4MHz} .
F9h	Calibration Frac	16-bit fractional value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the calibrate command. This fractional portion is a binary representation of one $t_{\rm 4MHz}$ period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{\rm 4MHz}$.
FAh		Reserved
FBh		Reserved
FCh		Reserved
FDh		Reserved

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX35102ETJ+	-40°C to +85°C	32 TQFN
MAX35102ETJ+T	-40°C to +85°C	32 TQFN

⁺Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
32 TQFN	T3244+1C	<u>21-0681</u>	90-0428

T = Tape and reel.

MAX35102

Time-to-Digital Converter Without RTC

Revision History

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	11/14	Initial release	_

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Комплексную поставку.
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- Наличие сертификата ISO.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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