**Freescale Semiconductor**
Data Sheet: Technical Data

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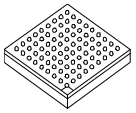
RoHS

# MCIMX31 and MCIMX31L



**Package Information**
Plastic Package
Case 1581 14 x 14 mm, 0.5 mm Pitch
Case 1931 19 x 19 mm, 0.8 mm Pitch

| Ordering Information |
|---|
| See Table 1 on page 3 for ordering information. |

# MCIMX31 and MCIMX31L

## Multimedia Applications Processors

## 1 Introduction

The MCIMX31 and MCIMX31L multimedia applications processors represent the next step in low-power, high-performance application processors. Unless otherwise specified, the material in this data sheet is applicable to both the MCIMX31 and MCIMX31L processors and referred to singularly throughout this document as MCIMX31. The MCIMX31L does not include a graphics processing unit (GPU).

Based on an ARM11™ microprocessor core, the MCIMX31 provides the performance with low power consumption required by modern digital devices.

The MCIMX31 takes advantage of the ARM1136JF-S™ core running at up to 532 MHz, and is optimized for minimal power consumption using the most advanced techniques for power saving (DPTC, DVFS, power gating, clock gating). With 90 nm technology and dual-Vt transistors (two threshold voltages), the MCIMX31 provides the optimal performance versus leakage current balance.

The performance of the MCIMX31 is boosted by a multi-level cache system, and features peripheral devices

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ARM POWERED

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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such as an MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The MCIMX31 supports connections to various types of external memories, such as DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The MCIMX31 can be connected to a variety of external devices using technology, such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and compact flash.

## 1.1 Features

The MCIMX31 is designed for the high-tier, mid-tier smartphone markets, and portable media players. They provide low-power solutions for high-performance demanding multimedia and graphics applications.

The MCIMX31 is built around the ARM11 MCU core and implemented in the 90 nm technology.

The systems include the following features:

- Multimedia and floating-point hardware acceleration supporting:
  - MPEG-4 real-time encode of up to VGA at 30 fps
  - MPEG-4 real-time video post-processing of up to VGA at 30 fps
  - Video conference call of up to QCIF-30 fps (decoder in software), 128 kbps
  - Video streaming (playback) of up to VGA-30 fps, 384 kbps
  - 3D graphics and other applications acceleration with the ARM® tightly-coupled Vector Floating Point co-processor
  - On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM CPU)
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Independent gating of power domains
- Multiple communication and expansion ports including a fast parallel interface to an external graphic accelerator (supporting major graphic accelerator vendors)
- Security

## 1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31.

**Table 1. Ordering Information[1]**

| Part Number | Silicon Revision[2, 3, 4,5] | Device Mask | Operating Temperature Range (°C) | Package[6] |
|---|---|---|---|---|
| MCIMX31DVKN5D! | 2.0.1 | M91E | –20 to 70 | 14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581 |
| MCIMX31LDVKN5D! | 2.0.1 | M91E | –20 to 70 | |
| MCIMX31CVKN5D! | 2.0.1 | M91E | –40 to 85 | |
| MCIMX31LCVKN5D! | 2.0.1 | M91E | –40 to 85 | |
| MCIMX31DVMN5D! | 2.0.1 | M91E | –20 to 70 | 19 x 19 mm, 0.8 mm pitch, Case 1931 |
| MCIMX31LDVMN5D! | 2.0.1 | M91E | –20 to 70 | |
| MCIMX31CJKN5D | 2.0.1 | M91E | –40 to 85 | 14 x 14 mm, 0.5 mm pitch, MAPBGA-457, Case 1581 |
| MCIMX31LCJKN5D | 2.0.1 | M91E | –40 to 85 | |

1 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

2 Information on reading the silicon revision register can be found in the IC Identification (IIM) chapter of the Reference Manual, see Section 6, “Product Documentation.”

3 Errata and fix information of the various mask sets can be found in the standard MCIMX31 Chip Errata, see Section 6, “Product Documentation.”

4 Changes in output buffer characteristics can be found in the I/O Setting Exceptions and Special Pad Descriptions table in the Reference Manual, see Section 6, “Product Documentation.”

5 JTAG functionality is not tested nor guaranteed at -40°C.

6 Case 1581 and 1931 are RoHS compliant, lead-free, MSL = 3.

### 1.2.1 Feature Differences Between Mask Sets

There are no silicon differences between revisions 2.0 and 2.0.1. The main difference is an updated iROM code which supports USB-HS, SD/MMC boot modes and corrects some boot mode related erratas.

## 1.3 Block Diagram

Figure 1 shows the MCIMX31 simplified interface block diagram.

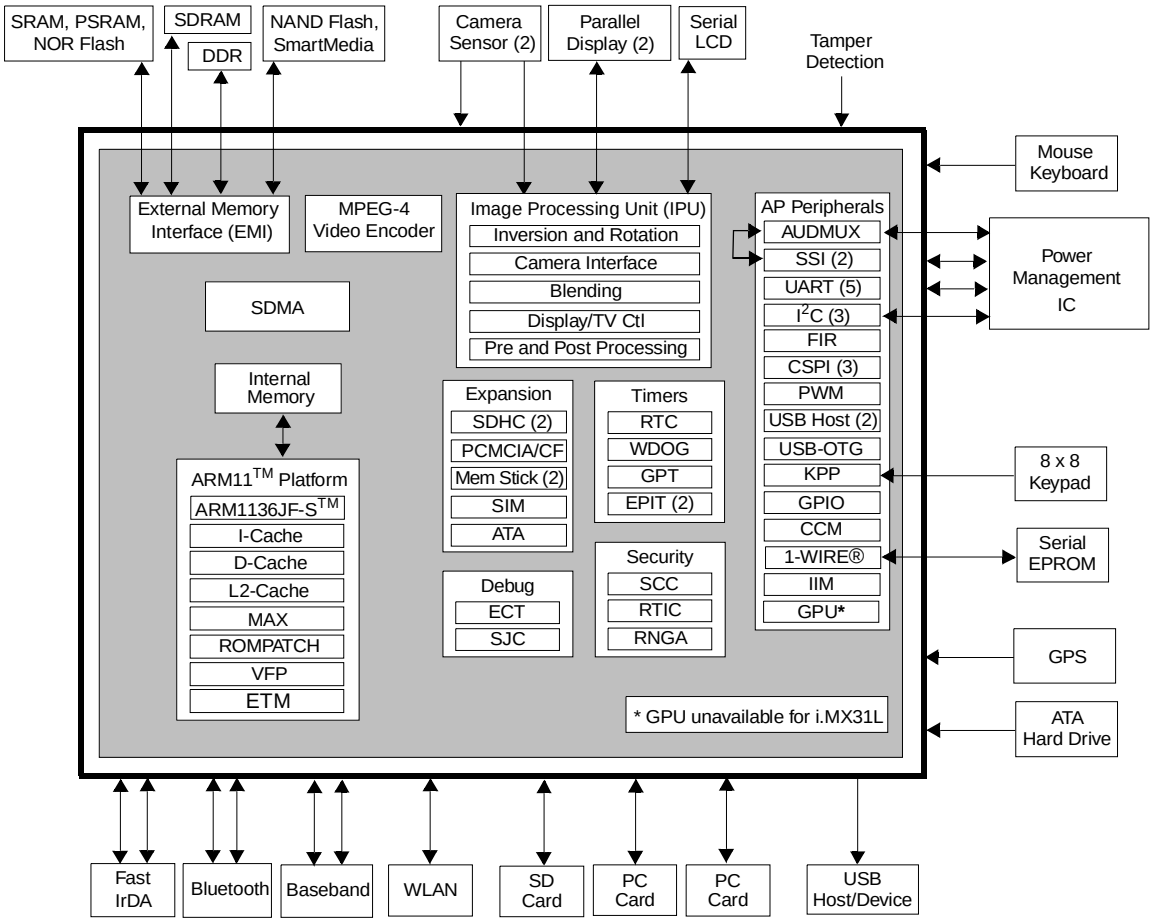



**Figure 1. MCIMX31 Simplified Interface Block Diagram**

# 2 Functional Description and Application Information

## 2.1 ARM11 Microprocessor Core

The CPU of the MCIMX31 is the ARM1136JF-S core based on the ARM v6 architecture. It supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes), and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency

- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with Hit-Under-Miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector Floating Point co-processor (VFP) for 3D graphics and other floating-point applications hardware acceleration
- ETM™ and JTAG-based debug support

### 2.1.1 Memory System

The ARM1136JF-S complex includes 16 KB Instruction and 16 KB Data L1 caches. It connects to the MCIMX31 L2 unified cache through 64-bit instruction (read-only), 64-bit data read/write (bi-directional), and 64-bit data write interfaces.

The embedded 16K SRAM can be used for audio streaming data to avoid external memory accesses for the low-power audio playback, for security, or for other applications. There is also a 32-KB ROM for bootstrap code and other frequently-used code and data.

A ROM patch module provides the ability to patch the internal ROM. It can also initiate an external boot by overriding the boot reset sequence by a jump to a configurable address.

Table 2 shows information about the MCIMX31 core in tabular form.

**Table 2. MCIMX31 Core**

| Core Acronym | Core Name | Brief Description | Integrated Memory Includes |
|---|---|---|---|
| ARM11 or ARM1136 | ARM1136 Platform | The ARM1136™ Platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a Vector Floating Processor (VFP).<br>The MCIMX31 provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities. | • 16 Kbyte Instruction Cache<br>• 16 Kbyte Data Cache<br>• 128 Kbyte L2 Cache<br>• 32 Kbyte ROM<br>• 16 Kbyte RAM |

## 2.2 Module Inventory

Table 3 shows an alphabetical listing of the modules in the multimedia applications processor. For extended descriptions of the modules, see the reference manual. A cross-reference is provided to the electrical specifications and timing information for each module with external signal connections.

**Table 3. Digital and Analog Modules**

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|---|---|---|---|---|
| 1-Wire® | 1-Wire Interface | Connectivity Peripheral | The 1-Wire module provides bi-directional communication between the ARM11 core and external 1-Wire devices. | 4.3.4/24 |
| ATA | Advanced Technology (AT) Attachment | Connectivity Peripheral | The ATA block is an AT attachment host interface. It is designed to interface with IDE hard disc drives and ATAPI optical disc drives. | 4.3.5/25 |
| AUDMUX | Digital Audio Multiplexer | Multimedia Peripheral | The AUDMUX interconnections allow multiple, simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations. | 4.3.6/34 |
| CAMP | Clock Amplifier Module | Clock | The CAMP converts a square wave/sinusoidal input into a rail-to-rail square wave. The output of CAMP feeds the predivider. | 4.3.3/23 |
| CCM | Clock Control Module | Clock | The CCM provides clock, reset, and power management control for the MCIMX31. | — |
| CSPI | Configurable Serial Peripheral Interface (x 3) | Connectivity Peripheral | The CSPI is equipped with data FIFOs and is a master/slave configurable serial peripheral interface module, capable of interfacing to both SPI master and slave devices. | 4.3.7/34 |
| DPLL | Digital Phase Lock Loop | Clock | The DPLLs produce high-frequency on-chip clocks with low frequency and phase jitters.<br>**Note:** External clock sources provide the reference frequencies. | 4.3.8/35 |
| ECT | Embedded Cross Trigger | Debug | The ECT is composed of three CTIs (Cross Trigger Interface) and one CTM (Cross Trigger Matrix—key in the multi-core and multi-peripheral debug strategy. | — |
| EMI | External Memory Interface | Memory Interface (EMI) | The EMI includes<br>• Multi-Master Memory Interface (M3IF)<br>• Enhanced SDRAM Controller (ESDCTL)<br>• NAND Flash Controller (NFC)<br>• Wireless External Interface Module (WEIM) | —<br>4.3.9.3/44,<br>4.3.9.1/36,<br>4.3.9.2/39 |
| EPIT | Enhanced Periodic Interrupt Timer | Timer Peripheral | The EPIT is a 32-bit “set and forget” timer which starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. | — |
| ETM | Embedded Trace Macrocell | Debug/Trace | The ETM (from ARM, Ltd.) supports real-time instruction and data tracing by way of ETM auxiliary I/O port. | 4.3.10/52 |
| FIR | Fast InfraRed Interface | Connectivity Peripheral | This FIR is capable of establishing a 0.576 Mbit/s, 1.152 Mbit/s or 4 Mbit/s half duplex link via a LED and IR detector. It supports 0.576 Mbit/s, 1.152 Mbit/s medium infrared (MIR) physical layer protocol and 4Mbit/s fast infrared (FIR) physical layer protocol defined by IrDA, Rev. 1.4. | 4.3.11/53 |

**Table 3. Digital and Analog Modules (continued)**

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|---|---|---|---|---|
| Fusebox | Fusebox | ROM | The Fusebox is a ROM that is factory configured by Freescale. | 4.3.12/53 See also Table 11 |
| GPIO | General Purpose I/O Module | Pins | The GPIO provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose signals that can be configured as either inputs or outputs. | — |
| GPT | General Purpose Timer | Timer Peripheral | The GPT is a multipurpose module used to measure intervals or generate periodic output. | — |
| GPU | Graphics Processing Unit | Multimedia Peripheral | The GPU provides hardware acceleration for 2D and 3D graphics algorithms. | — |
| $I^2C$ | Inter IC Communication | Connectivity Peripheral | The $I^2C$ provides serial interface for controlling the Sensor Interface and other external devices. Data rates of up to 100 Kbits/s are supported. | 4.3.13/54 |
| IIM | IC Identification Module | ID | The IIM provides an interface for reading device identification. | — |
| IPU | Image Processing Unit | Multimedia Peripheral | The IPU processes video and graphics functions in the MCIMX31 and interfaces to video, still image sensors, and displays. | 4.3.14/55, 4.3.15/57 |
| KPP | Keypad Port | Connectivity Peripheral | The KPP is used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix. | — |
| MPEG-4 | MPEG-4 Video Encoder | Multimedia Peripherals | The MPEG-4 encoder accelerates video compression, following the MPEG-4 standard | — |
| MSHC | Memory Stick Host Controller | Connectivity Peripheral | The MSHC is placed in between the AIPS and the customer memory stick to support data transfer from the MCIMX31 to the customer memory stick. | 4.3.16/82 |
| PADIO | Pads I/O | Buffers and Drivers | The PADIO serves as the interface between the internal modules and the device's external connections. | 4.3.1/20 |
| PCMCIA | PCM | Connectivity Peripheral | The PCMCIA Host Adapter provides the control logic for PCMCIA socket interfaces. | 4.3.17/84 |
| PWM | Pulse-Width Modulator | Timer Peripheral | The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. | 4.3.18/86 |
| RNGA | Random Number Generator Accelerator | Security | The RNGA module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism. | — |
| RTC | Real Time Clock | Timer Peripheral | The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050. | — |
| RTIC | Run-Time Integrity Checkers | Security | The RTIC ensures the integrity of the peripheral memory contents and assists with boot authentication. | — |

**Table 3. Digital and Analog Modules (continued)**

| Block Mnemonic | Block Name | Functional Grouping | Brief Description | Section/ Page |
|---|---|---|---|---|
| SCC | Security Controller Module | Security | The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information. | — |
| SDHC | Secured Digital Host Controller | Connectivity Peripheral | The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards. | 4.3.19/87 |
| SDMA | Smart Direct Memory Access | System Control Peripheral | The SDMA controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals. | — |
| SIM | Subscriber Identification Module | Connectivity Peripheral | The SIM interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-commerce applications. | 4.3.20/88 |
| SJC | Secure JTAG Controller | Debug | The SJC provides debug and test control with maximum security and provides a flexible architecture for future derivatives or future multi-cores architecture. | 4.3.21/92 |
| SSI | Synchronous Serial Interface | Multimedia Peripheral | The SSI is a full-duplex, serial port that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard. | 4.3.22/94 |
| UART | Universal Asynchronous Receiver/Transmitter | Connectivity Peripheral | The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility. | — |
| USB | Universal Serial Bus— 2 Host Controllers and 1 OTG (On-The-Go) | Connectivity Peripherals | • USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+ Low-Pin Count) and Legacy Full Speed transceivers.<br>• USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor.<br>• The USB-OTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver. | 4.3.23/102 |
| WDOG | Watchdog Timer Module | Timer Peripheral | The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors. | — |

# 3 Signal Descriptions

Signal descriptions are in the reference manual. Special signal considerations are listed following this paragraph. The BGA ball assignment is in Section 5, “Package Information and Pinout.”

Special Signal Considerations:

- **Tamper detect (GPIO1_6)**

  Tamper detect logic is used to issue a security violation. This logic is activated if the tamper detect input is asserted.

  The tamper detect logic is disabled after reset. After enabling the logic, it is impossible to disable it until the next reset. The GPR[16] bit functions as the tamper detect enable bit.

  GPIO1_6 functions similarly to other I/O with GPIO capabilities regardless of the status of the tamper detect enable bit. (For example, the GPIO1_6 can function as an input with GPIO capabilities, such as sampling through PSR or generating interrupts.)
- **Power ready (GPIO1_5)**

  The power ready input, GPIO1_5, should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.
- **SJC_MOD**

  SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.
- **CE_CONTROL**
  CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.
- **TTM_PAD**
  This is for Freescale factory use only. Control bits indicate that the pull-up/down is disabled. However, the TTM_PAD is actually connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
- **M_REQUEST and M_GRANT**

  These two signals are not utilized internally. The user should make no connection to these signals.
- **Clock Source Select (CLKSS)**

  The CLKSS is the input that selects the default reference clock source providing input to the DPLL. To select CKIH, tie CLKSS to NVCC1. To select CKIL, tie CLKSS to ground. After initialization, the reference clock source can be changed (initial setting is overwritten) by programming the PRCS bits in the CCMR.

# 4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31.

## 4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

**Table 4. MCIMX31 Chip-Level Conditions**

| For these characteristics, … | Topic appears … |
|---|---|
| Table 5, “Absolute Maximum Ratings” | on page 10 |
| Table 7, “Thermal Resistance Data—19 × 19 mm Package” | on page 11 |
| Table 8, “Operating Ranges” | on page 13 |
| Table 9, “Specific Operating Ranges for Silicon Revision 2.0.1” | on page 14 |
| Table 10, “Interface Frequency” | on page 14 |
| Section 4.1.1, “Supply Current Specifications” | on page 16 |
| Section 4.2, “Supply Power-Up/Power-Down Requirements and Restrictions” | on page 18 |

**CAUTION**

Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 8, "Operating Ranges," on page 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Table 5. Absolute Maximum Ratings**

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage (Core) | $QVCC_{max}$ | –0.5 | 1.65 | V |
| Supply Voltage (I/O) | $NVCC_{max}$ | –0.5 | 3.3 | V |
| Input Voltage Range | $V_{Imax}$ | –0.5 | NVCC +0.3 | V |
| Storage Temperature | $T_{storage}$ | –40 | 125 | $^{o}C$ |
| ESD Damage Immunity: | | | | |
| Human Body Model (HBM) | $V_{esd}$ | — | 1500 | V |
| Machine Model (MM) | | — | 200 | |
| Charge Device Model (CDM) | | — | 500 | |
| Offset voltage allowed in run mode between core supplies. | $V_{core_offset}$[1] | — | 15 | mV |

[1] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 6 provides the thermal resistance data for the 14 × 14 mm, 0.5 mm pitch package.

**Table 6. Thermal Resistance Data—14 × 14 mm Package**

| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to Ambient (natural convection) | Single layer board (1s) | $R_{\theta JA}$ | 56 | °C/W | 1, 2, 3 |
| Junction to Ambient (natural convection) | Four layer board (2s2p) | $R_{\theta JA}$ | 30 | °C/W | 1, 3 |
| Junction to Ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 46 | °C/W | 1, 2, 3 |
| Junction to Ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 26 | °C/W | 1, 3 |
| Junction to Board | — | $R_{\theta JB}$ | 17 | °C/W | 1, 4 |
| Junction to Case | — | $R_{\theta JC}$ | 10 | °C/W | 1, 5 |
| Junction to Package Top (natural convection) | — | $\Psi_{JT}$ | 2 | °C/W | 1, 6 |

**NOTES**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 7 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

**Table 7. Thermal Resistance Data—19 × 19 mm Package**

| Rating | Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to Ambient (natural convection) | Single layer board (1s) | $R_{\theta JA}$ | 46 | °C/W | 1, 2, 3 |
| Junction to Ambient (natural convection) | Four layer board (2s2p) | $R_{\theta JA}$ | 29 | °C/W | 1, 2, 3 |
| Junction to Ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 38 | °C/W | 1, 2, 3 |
| Junction to Ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 25 | °C/W | 1, 2, 3 |
| Junction to Board | — | $R_{\theta JB}$ | 19 | °C/W | 1, 3 |
| Junction to Case (Top) | — | $R_{\theta JCtop}$ | 10 | °C/W | 1, 4 |
| Junction to Package Top (natural convection) | — | $\Psi_{JT}$ | 2 | °C/W | 1, 5 |

## NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 8 provides the operating ranges.

**NOTE**

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

**CAUTION**

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

**Table 8. Operating Ranges**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| QVCC, QVCC1, QVCC4 | Core Operating Voltage[1,2,3]<br>$0 \le f_{ARM} \le 400$ MHz, non-overdrive<br>$0 \le f_{ARM} \le 532$ MHz, non-overdrive<br>$0 \le f_{ARM} \le 532$ MHz, overdrive[4] | <br>1.22<br>1.38<br>1.52 | <br>1.47<br>1.52<br>1.65 | V |
| | State Retention Voltage[5] | 0.95 | — | |
| NVCC1, NVCC3–10 | I/O Supply Voltage, except DDR[6]non-overdrive<br>overdrive[7] | 1.75<br>>3.1 | 3.1<br>3.3 | V |
| NVCC2, NVCC21, NVCC22 | I/O Supply Voltage, DDR only | 1.75 | 1.95 | V |
| FVCC, MVCC, SVCC, UVCC | PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[8]<br>non-overdrive<br>overdrive[4] | <br>1.3<br>>1.47 | <br>1.47<br>1.6 | V |
| IOQVDD | On-device Level Shifter Supply Voltage | 1.6 | 1.9 | V |
| FUSE_VDD | Fusebox read Supply Voltage[9, 10] | 1.65 | 1.95 | V |
| | Fusebox write (program) Supply Voltage[11] | 3.0 | 3.3 | V |
| $T_A$ | Operating Ambient Temperature Range[12] | –20 | 70 | $^0$C |

1 Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

2 The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID.

3 If the Core voltage is supplied by the MC13738, it will be 1.6 ± 0.05 V during the power-up sequence and this is allowed. After power-up the voltage should be reduced to avoid operation in overdrive mode.

4 Supply voltage is considered “overdrive” for voltages above 1.52 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1.25 years (10,950 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 25% (average 6 hours out of 24 yours per day) duty cycle for 5-year rated equipment. To tolerate the maximum operating overdrive voltage for 10 years, the device must have a duty cycle of 12.5% or less in overdrive (for example 3 out of 24 hours per day). Below 1.52 V, duty cycle restrictions may apply for equipment rated above 5 years.

5 The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

6 Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

7 Supply voltage is considered “overdrive” for voltages above 3.1 V. Operation time in overdrive—whether switching or not—must be limited to a cumulative duration of 1 year (8,760 hours) or less to sustain the maximum operating voltage without significant device degradation—for example, 20% (average 4.8 hours out of 24 hours per day) duty cycle for 5-year rated equipment. Operation at 3.3 V that exceeds a cumulative 3,504 hours may cause non-operation whenever supply voltage is reduced to 1.8 V; degradation may render the device too slow or inoperable. Below 3.1 V, duty cycle restrictions may apply for equipment rated above 5 years.

8 For normal operating conditions, PLLs’ and core supplies must maintain the following relation: PLL ≥ Core – 100 mV. In other words, for a 1.6 V core supply, PLL supplies must be set to 1.5 V or higher. This restriction is no longer necessary on mask set M91E. PLL supplies may be set independently of core supply. PLL voltage must not be altered after power up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 30, "DPLL Specifications," on page 35, are guaranteed over the entire specified voltage range.

9 Fusebox read supply voltage applies to silicon Revisions 1.2 and previous.

10 In read mode, FUSE_VDD can be floated or grounded for mask set M91E (silicon Revision 2.0.1).

11 Fuses might be inadvertently blown if written to while the voltage is below this minimum.

12 The temperature range given is for the consumer version. Please refer to Table 1 for extended temperature range offerings and the associated part numbers.

**Table 9. Specific Operating Ranges for Silicon Revision 2.0.1**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| FUSE_VDD | Fusebox read Supply Voltage[1] | — | — | V |
| | Fusebox write (program) Supply Voltage[2] | 3.0 | 3.3 | V |

1 In read mode, FUSE_VDD should be floated or grounded.

2 Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 10 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, “DPLL Electrical Specifications,” and Section 4.3.3, “Clock Amplifier Module (CAMP) Electrical Characteristics.”

**Table 10. Interface Frequency**

| ID | Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| 1 | JTAG TCK Frequency | $f_{JTAG}$ | DC | 5 | 10 | MHz |
| 2 | CKIL Frequency[1] | $f_{CKIL}$ | 32 | 32.768 | 38.4 | kHz |
| 3 | CKIH Frequency[2] | $f_{CKIH}$ | 15 | 26 | 75 | MHz |

1 CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

2 DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation.

Table 11 shows the fusebox supply current parameters.

**Table 11. Fusebox Supply Current Parameters**

| Ref. Num | Description | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| 1 | eFuse Program Current.[1]<br>Current to program one eFuse bit: efuse_pgm = 3.0 V | $I_{program}$ | — | 35 | 60 | mA |
| 2 | eFuse Read Current[2]<br>Current to read an 8-bit eFuse word<br>vdd_fusebox = 1.875 V | $I_{read}$ | — | 5 | 8 | mA |

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current $I_{read}$ is present for approximately 50 ns of the read access to the 8-bit word, and only applies to Silicon Rev. 1.2 and previous.

## 4.1.1 Supply Current Specifications

Table 12 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0.1 for the MCIMX31.

**Table 12. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0.1**

| Mode | Conditions | QVCC (Peripheral) | | QVCC1 (ARM) | | QVCC4 (L2) | | FVCC + MVCC + SVCC + UVCC (PLL) | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Deep Sleep | • QVCC = 0.95 V<br>• ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | 5.50 | — | — | — | — | 0.02 | 0.10 | mA |
| State Retention | • QVCC and QVCC1 = 0.95 V<br>• L2 caches are power gated (QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | 5.50 | 0.07 | 2.20 | — | — | 0.02 | 0.10 | mA |
| Wait | • QVCC,QVCC1, and QVCC4 = 1.22 V<br>• ARM is in wait for interrupt mode<br>• MAX is active<br>• L2 cache is stopped but powered<br>• MCU PLL is on (532 MHz), VCC = 1.4 V<br>• USB PLL and SPLL are off, VCC = 1.4 V<br>• FPM is on<br>• CKIH input is on<br>• CAMP is on<br>• 32 kHz input is on<br>• All clocks are gated off<br>• All modules are off (by programming CGR[2:0] registers)<br>• RNGA oscillator is off<br>• No external resistive loads | 6.00 | 15.00 | 2.20 | 25.00 | 0.03 | 0.29 | 3.60 | 4.40 | mA |

1 Typical column: TA = 25°C

2 Maximum column: TA = 85°C

Table 13 shows the core current consumption for –20°C to 70°C for Silicon Revision 2.0.1 for the MCIMX31.

**Table 13. Current Consumption for –20°C to 70°C[1, 2] for Silicon Revision 2.0.1**

| Mode | Conditions | QVCC (Peripheral) | | QVCC1 (ARM) | | QVCC4 (L2) | | FVCC, +MVCC, +SVCC, +UVCC (PLL) | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Deep Sleep | • QVCC = 0.95 V<br>• ARM and L2 caches are power gated (QVCC1 2= QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | — | — | — | — | — | 0.02 | — | mA |
| State Retention | • QVCC and QVCC1 = 0.95 V<br>• L2 caches are power gated (QVCC4 = 0 V)<br>• All PLLs are off, VCC = 1.4 V<br>• ARM is in well bias<br>• FPM is off<br>• 32 kHz input is on<br>• CKIH input is off<br>• CAMP is off<br>• TCK input is off<br>• All modules are off<br>• No external resistive loads<br>• RNGA oscillator is off | 0.16 | — | 0.07 | — | — | — | 0.02 | — | mA |
| Wait | • QVCC,QVCC1, and QVCC4 = 1.22 V<br>• ARM is in wait for interrupt mode<br>• MAX is active<br>• L2 cache is stopped but powered<br>• MCU PLL is on (532 MHz), VCC = 1.4 V<br>• USB PLL and SPLL are off, VCC = 1.4 V<br>• FPM is on<br>• CKIH input is on<br>• CAMP is on<br>• 32 kHz input is on<br>• All clocks are gated off<br>• All modules are off (by programming CGR[2:0] registers)<br>• RNGA oscillator is off<br>• No external resistive loads | 6.00 | — | 2.20 | — | 0.03 | — | 3.60 | — | mA |

1 Typical column: TA = 25°C

2 Maximum column: TA = 70°C

## 4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31 board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31 (worst-case scenario)

### 4.2.1 Powering Up

The Power On Reset ($\overline{\text{POR}}$) pin must be kept asserted (low) throughout the power up sequence. Power up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{\text{POR}}$. Figure 2 and Figure 3 show the power-up sequence for silicon Revision 2.0.1.

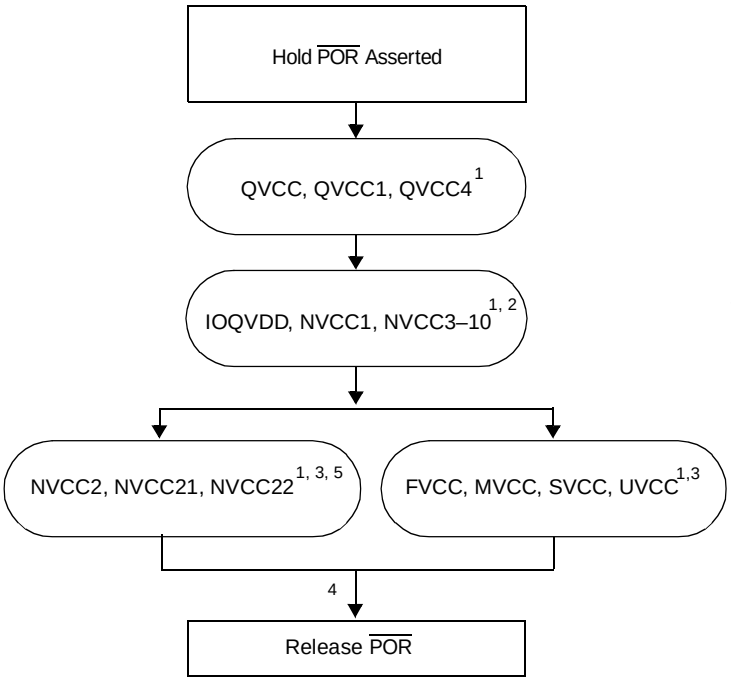
**NOTE**

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

**CAUTION**

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

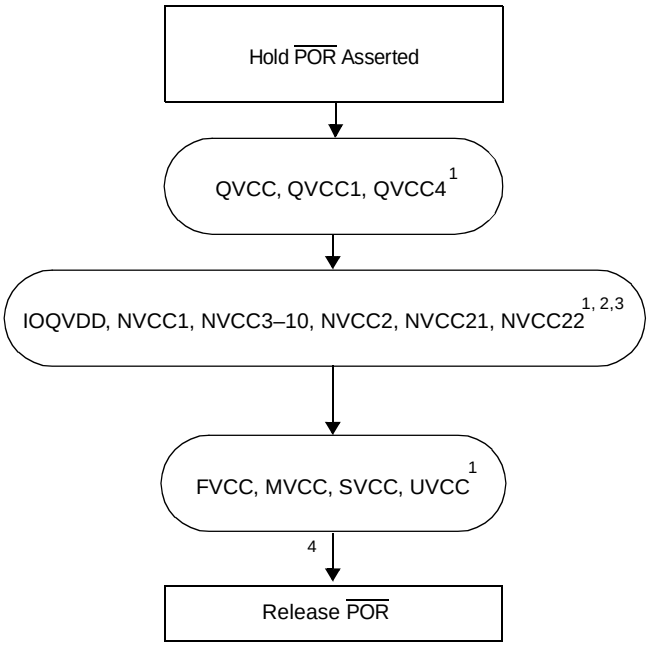
### 4.2.1.1 Power-Up Sequence for Silicon Revision 2.0.1




**Notes:**

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.
4. FUSE_VDD should not be driven on power-up for Silicon Revision 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.
5. Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

**Figure 2. Option 1 Power-Up Sequence (Silicon Revision 2.0.1)**




**Notes:**

1. The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
2. The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
3. Raising NVCC2, NVCC21, and NVCC22 at the same time as IOQVDD does not produce the slight increase in current drain on IOQVDD (as described in Figure 2, Note 5).
4. FUSE_VDD should not be driven on power-up for Silicon Revision 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

**Figure 3. Option 2 Power-Up Sequence (Silicon Revision 2.0.1)**

### 4.2.2 Powering Down

For silicon revisions beginning with Revision 2.0.1 there is no special requirements for the power down sequence.

## 4.3 Module-Level Electrical Specifications

This section contains the MCIMX31 electrical information including timing specifications, arranged in alphabetical order by module name.

### 4.3.1 I/O Pad (PADIO) Electrical Specifications

This section specifies the AC/DC characterization of functional I/O of the MCIMX31. There are two main types of I/O: regular and DDR. In this document, the “Regular” type is referred to as GPIO.

#### 4.3.1.1 DC Electrical Characteristics

The MCIMX31 I/O parameters appear in Table 14 for GPIO. See Table 8 for temperature and supply voltage ranges.

**NOTE**

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual. NVCC for Table 14 refers to NVCC1 and NVCC3–10; QVCC refers to QVCC, QVCC1, and QVCC4.

**Table 14. GPIO DC Electrical Parameters**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –1 mA | NVCC –0.15 | — | — | V |
| | | $I_{OH}$ = specified Drive | 0.8*NVCC | — | — | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | — | — | 0.15 | V |
| | | $I_{OL}$ = specified Drive | — | — | 0.2*NVCC | V |
| High-level output current, slow slew rate | $I_{OH_S}$ | $V_{OH}$=0.8*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>–2<br>–4<br>–8 | — | — | mA |
| High-level output current, fast slew rate | $I_{OH_F}$ | $V_{OH}$=0.8*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>–4<br>–6<br>–8 | — | — | mA |
| Low-level output current, slow slew rate | $I_{OL_S}$ | $V_{OL}$=0.2*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>2<br>4<br>8 | — | — | mA |

**Table 14. GPIO DC Electrical Parameters (continued)**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Low-level output current, fast slew rate | $I_{OL_F}$ | $V_{OL}$=0.2*NVCC<br>Std Drive<br>High Drive<br>Max Drive | <br>4<br>6<br>8 | — | — | mA |
| High-Level DC input voltage | $V_{IH}$ | — | 0.7*NVCC | — | NVCC | V |
| Low-Level DC input voltage | $V_{IL}$ | — | 0 | — | 0.3*QVCC | V |
| Input Hysteresis | $V_{HYS}$ | Hysteresis enabled | 0.25 | — | — | V |
| Schmitt trigger VT+ | $V_T$ + | Hysteresis enabled | 0.5*QVCC | — | — | V |
| Schmitt trigger VT– | $V_T$ – | Hysteresis enabled | — | — | 0.5*QVCC | V |
| Pull-up resistor (100 kΩ PU) | $R_{PU}$ | — | — | 100 | — | kΩ |
| Pull-down resistor (100 kΩ PD) | $R_{PD}$ | — | — | 100 | — | |
| Input current (no PU/PD) | $I_{IN}$ | $V_I$ = NVCC or GND | — | — | ±1 | µA |
| Input current (100 kΩ PU) | $I_{IN}$ | $V_I$ = 0<br>$V_I$ = NVCC | — | — | 25<br>0.1 | µA<br>µA |
| Input current (100 kΩ PD) | $I_{IN}$ | $V_I$ = 0<br>$V_I$ = NVCC | — | — | 0.25<br>28 | µA<br>µA |
| Tri-state leakage current | $I_{OZ}$ | $V_I$ = NVCC or GND<br>I/O = High Z | — | — | ±2 | µA |

The MCIMX31 I/O parameters appear in Table 15 for DDR (Double Data Rate). See Table 8, "Operating Ranges," on page 13 for temperature and supply voltage ranges.

**NOTE**

NVCC for Table 15 refers to NVCC2, NVCC21, and NVCC22.

**Table 15. DDR (Double Data Rate) I/O DC Electrical Parameters**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = –1 mA | NVCC –0.12 | — | — | V |
| | | $I_{OH}$ = specified Drive | 0.8*NVCC | — | — | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ = 1 mA | — | — | 0.08 | V |
| | | $I_{OL}$ = specified Drive | — | — | 0.2*NVCC | V |
| High-level output current | $I_{OH}$ | $V_{OH}$=0.8*NVCC<br>Std Drive<br>High Drive<br>Max Drive<br>DDR Drive[1] | <br>–3.6<br>–7.2<br>–10.8<br>–14.4 | — | — | mA |
| Low-level output current | $I_{OL}$ | $V_{OL}$=0.2*NVCC<br>Std Drive<br>High Drive<br>Max Drive<br>DDR Drive[1] | <br>3.6<br>7.2<br>10.8<br>14.4 | — | — | mA |

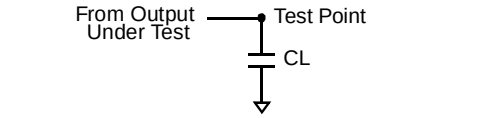
**Table 15. DDR (Double Data Rate) I/O DC Electrical Parameters (continued)**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High-Level DC input voltage | $V_{IH}$ | — | 0.7*NVCC | NVCC | NVCC+0.3 | V |
| Low-Level DC input voltage | $V_{IL}$ | — | –0.3 | 0 | 0.3*NVCC | V |
| Tri-state leakage current | $I_{OZ}$ | $V_I$ = NVCC or GND<br>I/O = High Z | — | — | ±2 | µA |

1 Use of DDR Drive can result in excessive overshoot and ringing.

## 4.3.2 AC Electrical Characteristics

Figure 4 depicts the load circuit for outputs. Figure 5 depicts the output transition time waveform. The range of operating conditions appears in Table 16 for slow general I/O, Table 17 for fast general I/O, and Table 18 for DDR I/O (unless otherwise noted).




CL includes package, probe and fixture capacitance

**Figure 4. Load Circuit for Output**

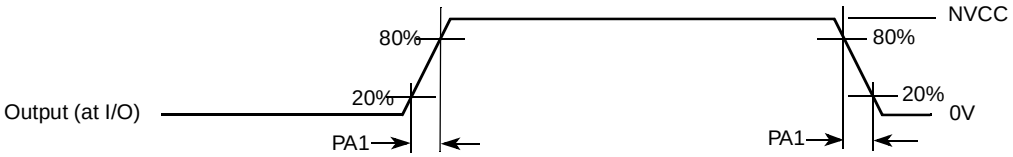



**Figure 5. Output Transition Time Waveform**

**Table 16. AC Electrical Characteristics of Slow[1] General I/O**

| ID | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PA1 | Output Transition Times (Max Drive) | tpr | 25 pF<br>50 pF | 0.92<br>1.5 | 1.95<br>2.98 | 3.17<br>4.75 | ns |
| | Output Transition Times (High Drive) | tpr | 25 pF<br>50 pF | 1.52<br>2.75 | — | 4.81<br>8.42 | ns |
| | Output Transition Times (Std Drive) | tpr | 25 pF<br>50 pF | 2.79<br>5.39 | — | 8.56<br>16.43 | ns |

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

**Table 17. AC Electrical Characteristics of Fast[1] General I/O [2]**

| ID | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PA1 | Output Transition Times (Max Drive) | tpr | 25 pF<br>50 pF | 0.68<br>1.34 | 1.33<br>2.6 | 2.07<br>4.06 | ns |
| | Output Transition Times (High Drive) | tpr | 25 pF<br>50 pF | .91<br>1.79 | 1.77<br>3.47 | 2.74<br>5.41 | ns |
| | Output Transition Times (Std Drive) | tpr | 25 pF<br>50 pF | 1.36<br>2.68 | 2.64<br>5.19 | 4.12<br>8.11 | ns |

1 Fast/slow characteristic is selected per GPIO (where available) by “slew rate” control. See reference manual.

2 Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

**Table 18. AC Electrical Characteristics of DDR I/O**

| ID | Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PA1 | Output Transition Times (DDR Drive)[1] | tpr | 25 pF<br>50 pF | 0.51<br>0.97 | 0.82<br>1.58 | 1.28<br>2.46 | ns |
| | Output Transition Times (Max Drive) | tpr | 25 pF<br>50 pF | 0.67<br>1.29 | 1.08<br>2.1 | 1.69<br>3.27 | ns |
| | Output Transition Times (High Drive) | tpr | 25 pF<br>50 pF | .99<br>1.93 | 1.61<br>3.13 | 2.51<br>4.89 | ns |
| | Output Transition Times (Std Drive) | tpr | 25 pF<br>50 pF | 1.96<br>3.82 | 3.19<br>6.24 | 4.99<br>9.73 | ns |

1 Use of DDR Drive can result in excessive overshoot and ringing.

## 4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 19 shows clock amplifier electrical characteristics.

**Table 19. Clock Amplifier Electrical Characteristics for CKIH Input**

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Input Frequency | 15 | — | 75 | MHz |
| VIL (for square wave input) | 0 | — | 0.3 | V |
| VIH (for square wave input) | (VDD [1]– 0.25) | — | 3 | V |
| Sinusoidal Input Amplitude | 0.4 [2] | — | VDD | Vp-p |
| Duty Cycle | 45 | 50 | 55 | % |

1 VDD is the supply voltage of CAMP. See reference manual.

2 This value of the sinusoidal input will be measured through characterization.

## 4.3.4 1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 20 lists the RPP timing parameters.

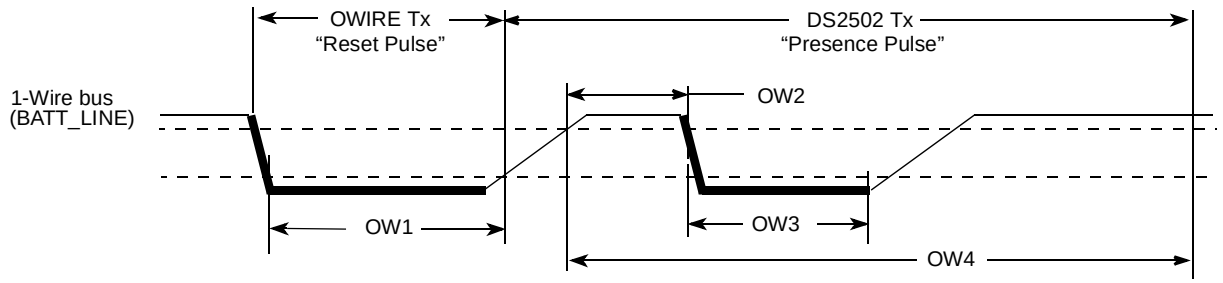



**Figure 6. Reset and Presence Pulses (RPP) Timing Diagram**

**Table 20. RPP Sequence Delay Comparisons Timing Parameters**

| ID | Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW1 | Reset Time Low | $t_{RSTL}$ | 480 | 511 | — | µs |
| OW2 | Presence Detect High | $t_{PDH}$ | 15 | — | 60 | µs |
| OW3 | Presence Detect Low | $t_{PDL}$ | 60 | — | 240 | µs |
| OW4 | Reset Time High | $t_{RSTH}$ | 480 | 512 | — | µs |

Figure 7 depicts Write 0 Sequence timing, and Table 21 lists the timing parameters.

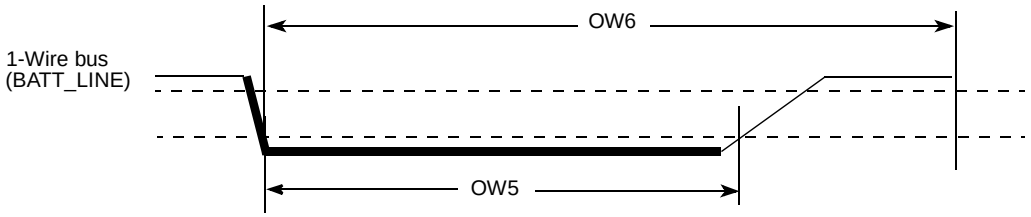



**Figure 7. Write 0 Sequence Timing Diagram**

**Table 21. WR0 Sequence Timing Parameters**

| ID | Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW5 | Write 0 Low Time | $t_{WR0_low}$ | 60 | 100 | 120 | µs |
| OW6 | Transmission Time Slot | $t_{SLOT}$ | OW5 | 117 | 120 | µs |

Figure 8 depicts Write 1 Sequence timing, Figure 9 depicts the Read Sequence timing, and Table 22 lists the timing parameters.

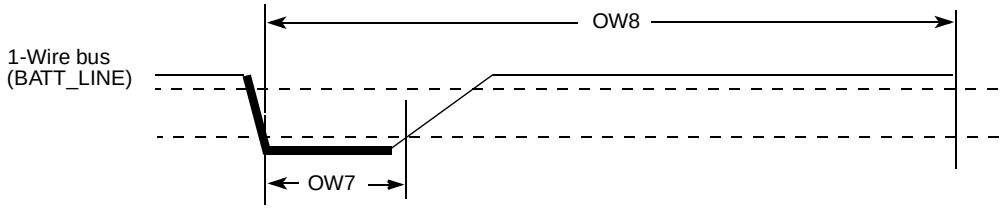



**Figure 8. Write 1 Sequence Timing Diagram**

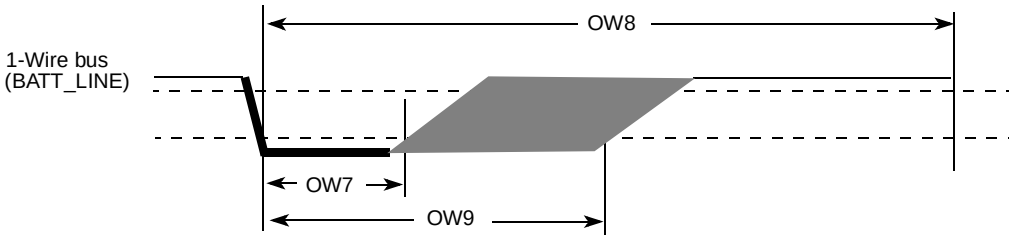



**Figure 9. Read Sequence Timing Diagram**

**Table 22. WR1/RD Timing Parameters**

| ID | Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| OW7 | Write 1 / Read Low Time | $t_{LOW1}$ | 1 | 5 | 15 | µs |
| OW8 | Transmission Time Slot | $t_{SLOT}$ | 60 | 117 | 120 | µs |
| OW9 | Release Time | $t_{RELEASE}$ | 15 | — | 45 | µs |

## 4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

### 4.3.5.1 Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 23 shows ATA timing parameters.

**Table 23. ATA Timing Parameters**

| Name | Description | Value/ Contributing Factor[1] |
|---|---|---|
| T | Bus clock period (ipg_clk_ata) | peripheral clock frequency |
| ti_ds | Set-up time ata_data to ata_iordy edge (UDMA-in only)<br>UDMA0<br>UDMA1<br>UDMA2, UDMA3<br>UDMA4<br>UDMA5 | <br>15 ns<br>10 ns<br>7 ns<br>5 ns<br>4 ns |
| ti_dh | Hold time ata_iordy edge to ata_data (UDMA-in only)<br>UDMA0, UDMA1, UDMA2, UDMA3, UDMA4<br>UDMA5 | <br>5.0 ns<br>4.6 ns |
| tco | Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en | 12.0 ns |
| tsu | Set-up time ata_data to bus clock L-to-H | 8.5 ns |
| tsui | Set-up time ata_iordy to bus clock H-to-L | 8.5 ns |
| thi | Hold time ata_iordy to bus clock H to L | 2.5 ns |
| tskew1 | Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | 7 ns |
| tskew2 | Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en | transceiver |
| tskew3 | Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read) | transceiver |
| tbuf | Max buffer propagation delay | transceiver |
| tcable1 | Cable propagation delay for ata_data | cable |
| tcable2 | Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack | cable |
| tskew4 | Max difference in cable propagation delay between ata_iordy and ata_data (read) | cable |
| tskew5 | Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write) | cable |
| tskew6 | Max difference in cable propagation delay without accounting for ground bounce | cable |

1 Values provided where applicable.

### 4.3.5.2 PIO Mode Timing

Figure 10 shows timing for PIO read, and Table 24 lists the timing parameters for PIO read.

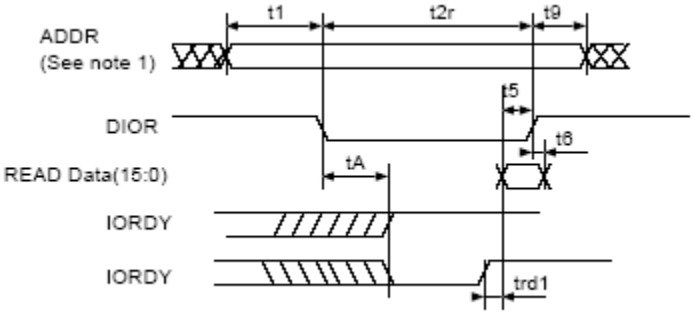



**Figure 10. PIO Read Timing Diagram**

**Table 24. PIO Read Timing Parameters**

| ATA Parameter | Parameter from Figure 10 | Value | Controlling Variable |
|---|---|---|---|
| t1 | t1 | t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5) | time_1 |
| t2 | t2r | t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5) | time_2r |
| t9 | t9 | t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6) | time_3 |
| t5 | t5 | t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 | If not met, increase time_2 |
| t6 | t6 | 0 | — |
| tA | tA | tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf) | time_ax |
| trd | trd1 | trd1 (max) = (–trd) + (tskew3 + tskew4)<br>trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi)<br>(time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4 | time_pio_rdx |
| t0 | — | t0 (min) = (time_1 + time_2 + time_9) * T | time_1, time_2r, time_9 |

Figure 11 shows timing for PIO write, and Table 25 lists the timing parameters for PIO write.

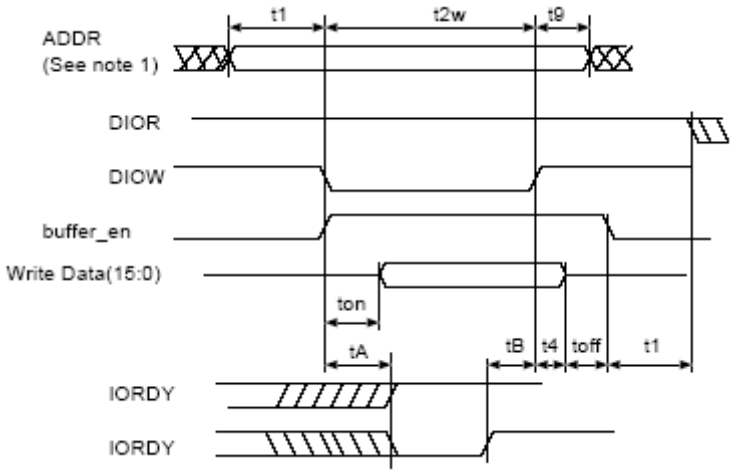



**Figure 11. Multiword DMA (MDMA) Timing**

**Table 25. PIO Write Timing Parameters**

| ATA Parameter | Parameter from Figure 11 | Value | Controlling Variable |
|---|---|---|---|
| t1 | t1 | t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5) | time_1 |
| t2 | t2w | t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5) | time_2w |
| t9 | t9 | t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6) | time_9 |
| t3 | — | t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5) | If not met, increase time_2w |
| t4 | t4 | t4 (min) = time_4 * T – tskew1 | time_4 |
| tA | tA | tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf) | time_ax |
| t0 | — | t0(min) = (time_1 + time_2 + time_9) * T | time_1, time_2r, time_9 |
| — | — | Avoid bus contention when switching buffer on by making ton long enough. | — |
| — | — | Avoid bus contention when switching buffer off by making toff long enough. | — |

Figure 12 shows timing for MDMA read, Figure 13 shows timing for MDMA write, and Table 26 lists the timing parameters for MDMA read and write.

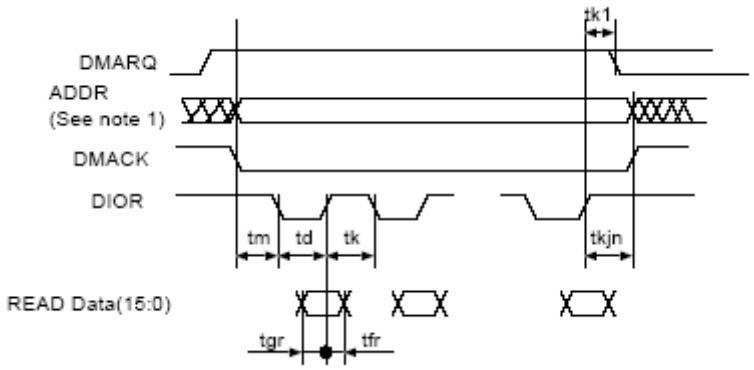



**Figure 12. MDMA Read Timing Diagram**

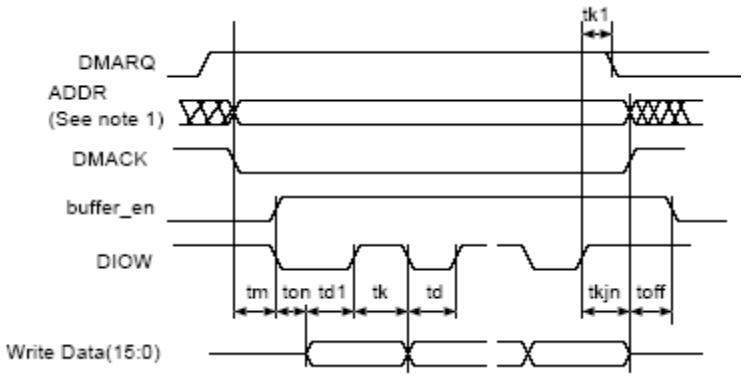



**Figure 13. MDMA Write Timing Diagram**

**Table 26. MDMA Read and Write Timing Parameters**

| ATA Parameter | Parameter from Figure 12, Figure 13 | Value | Controlling Variable |
|---|---|---|---|
| tm, ti | tm | tm (min) = ti (min) = time_m * T – (tskew1 + tskew2 + tskew5) | time_m |
| td | td, td1 | td1.(min) = td (min) = time_d * T – (tskew1 + tskew2 + tskew6) | time_d |
| tk | tk | tk.(min) = time_k * T – (tskew1 + tskew2 + tskew6) | time_k |
| t0 | — | t0 (min) = (time_d + time_k) * T | time_d, time_k |
| tg(read) | tgr | tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2<br>tgr.(min-drive) = td – te(drive) | time_d |
| tf(read) | tfr | tfr (min-drive) = 0 | — |
| tg(write) | — | tg (min-write) = time_d * T – (tskew1 + tskew2 + tskew5) | time_d |
| tf(write) | — | tf (min-write) = time_k * T – (tskew1 + tskew2 + tskew6) | time_k |
| tL | — | tL (max) = (time_d + time_k–2)*T – (tsu + tco + 2*tbuf + 2*tcable2) | time_d, time_k |
| tn, tj | tkjn | tn= tj= tkjn = (max(time_k,. time_jn) * T – (tskew1 + tskew2 + tskew6) | time_jn |
| — | ton<br>toff | ton = time_on * T – tskew1<br>toff = time_off * T – tskew1 | — |

### 4.3.5.3 UDMA In Timing

Figure 14 shows timing when the UDMA in transfer starts, Figure 15 shows timing when the UDMA in host terminates transfer, Figure 16 shows timing when the UDMA in device terminates transfer, and Table 27 lists the timing parameters for UDMA in burst.

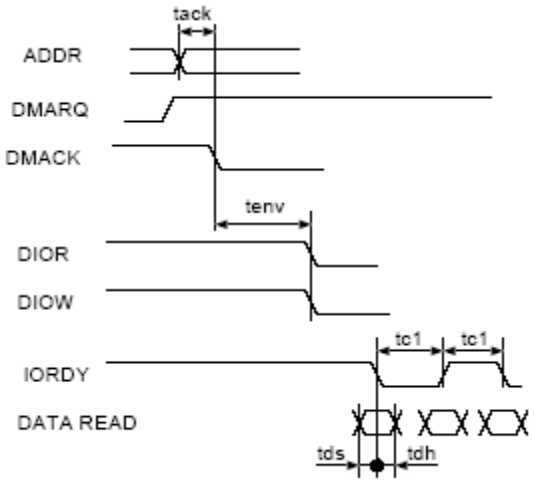



**Figure 14. UDMA In Transfer Starts Timing Diagram**

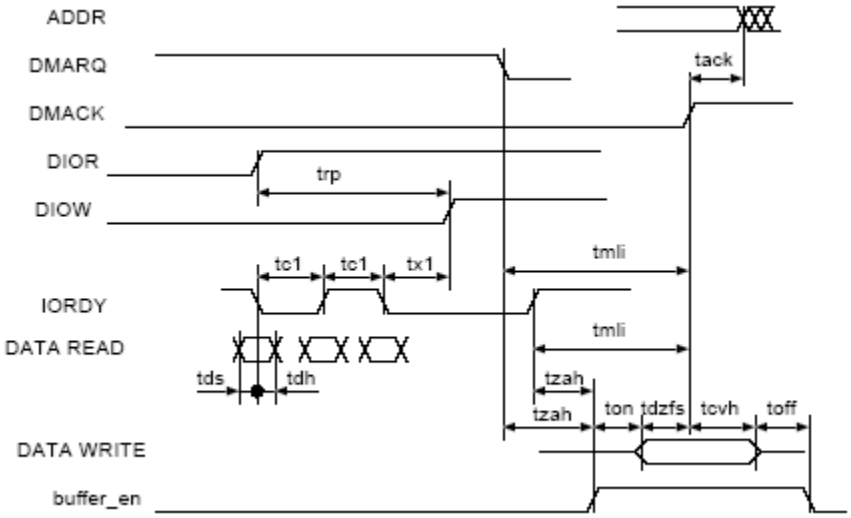



**Figure 15. UDMA In Host Terminates Transfer Timing Diagram**

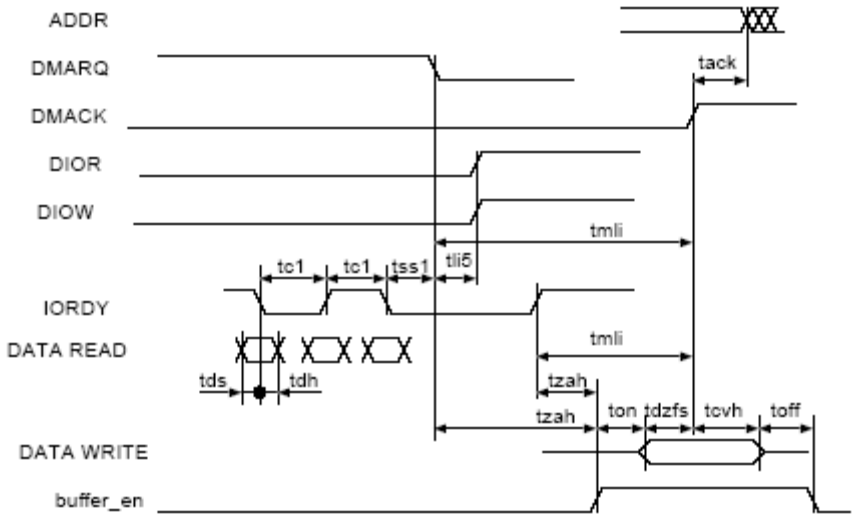



**Figure 16. UDMA In Device Terminates Transfer Timing Diagram**

**Table 27. UDMA In Burst Timing Parameters**

| ATA Parameter | Parameter from Figure 14, Figure 15, Figure 16 | Description | Controlling Variable |
|---|---|---|---|
| tack | tack | tack (min) = (time_ack * T) – (tskew1 + tskew2) | time_ack |
| tenv | tenv | tenv (min) = (time_env * T) – (tskew1 + tskew2)<br>tenv (max) = (time_env * T) + (tskew1 + tskew2) | time_env |
| tds | tds1 | tds – (tskew3) – ti_ds > 0 | tskew3, ti_ds, ti_dh should be low enough |
| tdh | tdh1 | tdh – (tskew3) – ti_dh > 0 | |
| tcyc | tc1 | (tcyc – tskew) > T | T big enough |
| trp | trp | trp (min) = time_rp * T – (tskew1 + tskew2 + tskew6) | time_rp |
| — | tx1[1] | (time_rp * T) – (tco + tsu + 3T + 2 *tbuf + 2*tcable2) > trfs (drive) | time_rp |
| tmli | tmli1 | tmli1 (min) = (time_mlix + 0.4) * T | time_mlix |
| tzah | tzah | tzah (min) = (time_zah + 0.4) * T | time_zah |
| tdzfs | tdzfs | tdzfs = (time_dzfs * T) – (tskew1 + tskew2) | time_dzfs |
| tcvh | tcvh | tcvh = (time_cvh *T) – (tskew1 + tskew2) | time_cvh |
| — | ton<br>toff | ton = time_on * T – tskew1<br>toff = time_off * T – tskew1 | — |

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2. Make ton and toff big enough to avoid bus contention

### 4.3.5.4 UDMA Out Timing

Figure 17 shows timing when the UDMA out transfer starts, Figure 18 shows timing when the UDMA out host terminates transfer, Figure 19 shows timing when the UDMA out device terminates transfer, and Table 28 lists the timing parameters for UDMA out burst.

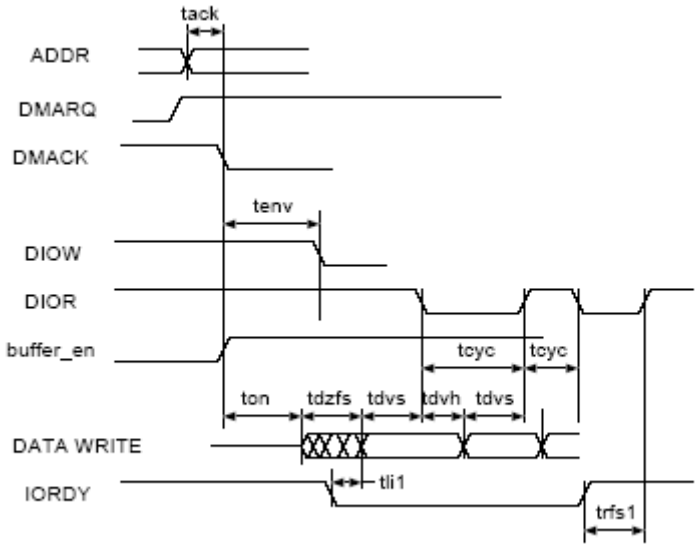



**Figure 17. UDMA Out Transfer Starts Timing Diagram**

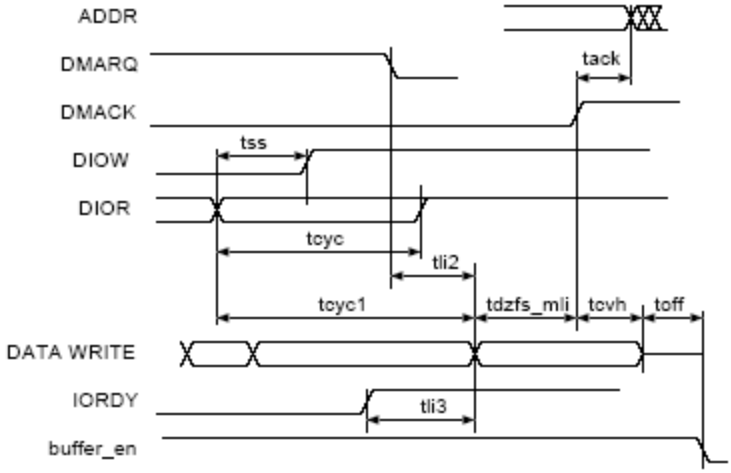



**Figure 18. UDMA Out Host Terminates Transfer Timing Diagram**

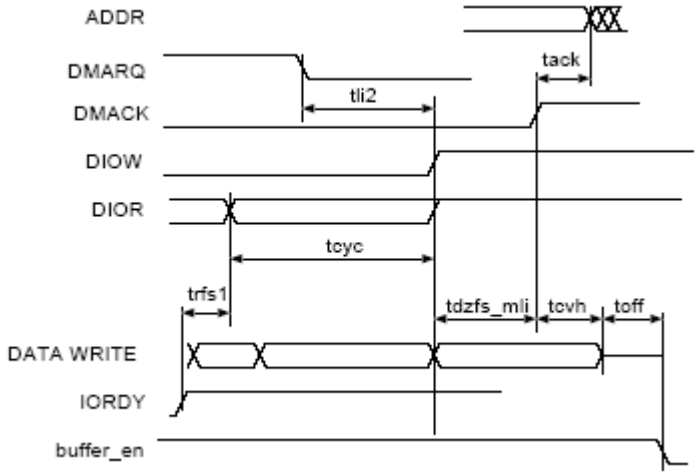



**Figure 19. UDMA Out Device Terminates Transfer Timing Diagram**

**Table 28. UDMA Out Burst Timing Parameters**

| ATA Parameter | Parameter from Figure 17, Figure 18, Figure 19 | Value | Controlling Variable |
|---|---|---|---|
| tack | tack | tack (min) = (time_ack * T) – (tskew1 + tskew2) | time_ack |
| tenv | tenv | tenv (min) = (time_env * T) – (tskew1 + tskew2)<br>tenv (max) = (time_env * T) + (tskew1 + tskew2) | time_env |
| tdvs | tdvs | tdvs = (time_dvs * T) – (tskew1 + tskew2) | time_dvs |
| tdvh | tdvh | tdvs = (time_dvh * T) – (tskew1 + tskew2) | time_dvh |
| tcyc | tcyc | tcyc = time_cyc * T – (tskew1 + tskew2) | time_cyc |
| t2cyc | — | t2cyc = time_cyc * 2 * T | time_cyc |
| trfs1 | trfs | trfs = 1.6 * T + tsui + tco + tbuf + tbuf | — |
| — | tdzfs | tdzfs = time_dzfs * T – (tskew1) | time_dzfs |
| tss | tss | tss = time_ss * T – (tskew1 + tskew2) | time_ss |
| tmli | tdzfs_mli | tdzfs_mli =max (time_dzfs, time_mli) * T – (tskew1 + tskew2) | — |
| tli | tli1 | tli1 > 0 | — |
| tli | tli2 | tli2 > 0 | — |
| tli | tli3 | tli3 > 0 | — |
| tcvh | tcvh | tcvh = (time_cvh *T) – (tskew1 + tskew2) | time_cvh |
| — | ton<br>toff | ton = time_on * T – tskew1<br>toff = time_off * T – tskew1 | — |

## 4.3.6 AUDMUX Electrical Specifications

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSI) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module. Please refer to their respective electrical specifications.

## 4.3.7 CSPI Electrical Specifications

This section describes the electrical information of the CSPI.

### 4.3.7.1 CSPI Timing

Figure 20 and Figure 21 depict the master mode and slave mode timings of CSPI, and Table 29 lists the timing parameters.

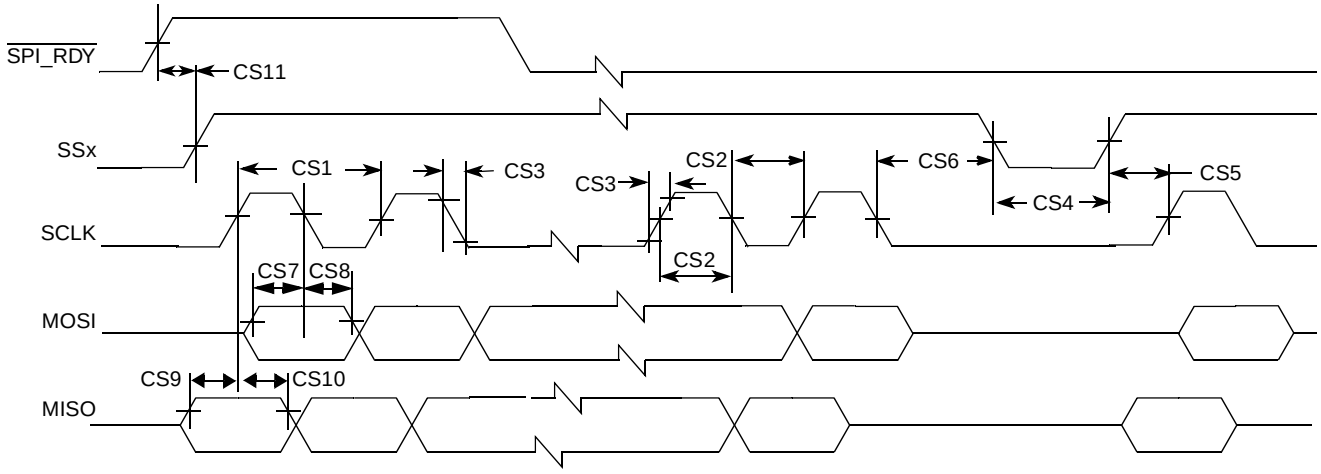



**Figure 20. CSPI Master Mode Timing Diagram**

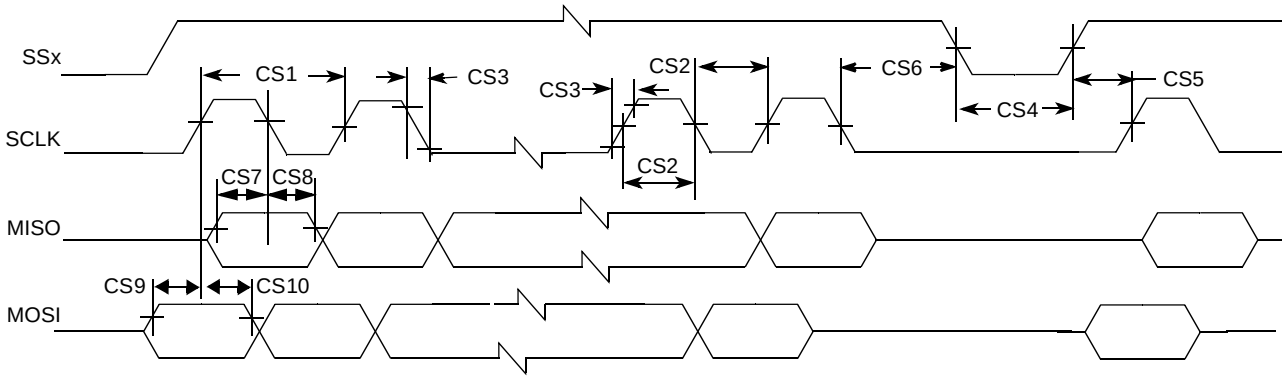



**Figure 21. CSPI Slave Mode Timing Diagram**

**Table 29. CSPI Interface Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| CS1 | SCLK Cycle Time | $t_{clk}$ | 60 | — | ns |
| CS2 | SCLK High or Low Time | $t_{SW}$ | 30 | — | ns |
| CS3 | SCLK Rise or Fall | $t_{RISE/FALL}$ | — | 7.6 | ns |
| CS4 | SSx pulse width | $t_{CSLH}$ | 25 | — | ns |
| CS5 | SSx Lead Time (CS setup time) | $t_{SCS}$ | 25 | — | ns |
| CS6 | SSx Lag Time (CS hold time) | $t_{HCS}$ | 25 | — | ns |
| CS7 | Data Out Setup Time | $t_{Smosi}$ | 5 | — | ns |
| CS8 | Data Out Hold Time | $t_{Hmosi}$ | 5 | — | ns |
| CS9 | Data In Setup Time | $t_{Smiso}$ | 6 | — | ns |
| CS10 | Data In Hold Time | $t_{Hmiso}$ | 5 | — | ns |
| CS11 | $\overline{\text{SPI_RDY}}$ Setup Time[1] | $t_{SRDY}$ | — | — | ns |

1 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

## 4.3.8 DPLL Electrical Specifications

The three PLL's of the MCIMX31 (MCU, USB, and Serial PLL) are all based on same DPLL design. The characteristics provided herein apply to all of them, except where noted explicitly. The PLL characteristics are provided based on measurements done for both sources—external clock source (CKIH), and FPM (Frequency Pre-Multiplier) source.

### 4.3.8.1 Electrical Specifications

Table 30 lists the DPLL specification.

**Table 30. DPLL Specifications**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| CKIH frequency | 15 | 26[1] | 75[2] | MHz | — |
| CKIL frequency<br>(Frequency Pre-multiplier (FPM) enable mode) | — | 32; 32.768, 38.4 | — | kHz | FPM lock time ≈ 480 µs. |
| Predivision factor (PD bits) | 1 | — | 16 | — | — |
| PLL reference frequency range after Predivider | 15 | — | 35 | MHz | 15 ≤ CKIH frequency/PD ≤ 35 MHz<br>15 ≤ FPM output/PD ≤ 35 MHz |
| PLL output frequency range:<br>MPLL and SPLL<br>UPLL | —<br>52<br>190 | — | —<br>532<br>240 | MHz | — |
| Maximum allowed reference clock phase noise. | — | — | ± 100 | ps | — |
| Frequency lock time<br>(FOL mode or non-integer MF) | — | — | 398 | — | Cycles of divided reference clock. |

**Table 30. DPLL Specifications (continued)**

| Parameter | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Phase lock time | — | — | 100 | µs | In addition to the frequency |
| Maximum allowed PLL supply voltage ripple | — | — | 25 | mV | $F_{modulation}$ < 50 kHz |
| Maximum allowed PLL supply voltage ripple | — | — | 20 | mV | 50 kHz < $F_{modulation}$ < 300 kHz |
| Maximum allowed PLL supply voltage ripple | — | — | 25 | mV | $F_{modulation}$ > 300 kHz |
| PLL output clock phase jitter | — | — | 5.2 | ns | Measured on CLKO pin |
| PLL output clock period jitter | — | — | 420 | ps | Measured on CLKO pin |

1 The user or board designer must take into account that the use of a frequency other than 26 MHz would require adjustment to the DPTC–DVFS table, which is incorporated into operating system code.

2 The PLL reference frequency must be ≤ 35 MHz. Therefore, for frequencies between 35 MHz and 70 MHz, program the predivider to divide by 2 or more. If the CKIH frequency is above 70 MHz, program the predivider to 3 or more. For PD bit description, see the reference manual.

## 4.3.9 EMI Electrical Specifications

This section provides electrical parametrics and timings for EMI module.

### 4.3.9.1 NAND Flash Controller Interface (NFC)

The NFC supports normal timing mode, using two flash clock cycles for one access of $\overline{RE}$ and $\overline{WE}$. AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 22, Figure 23, Figure 24, and Figure 25 depict the relative timing requirements among different signals of the NFC at module level, for normal mode, and Table 31 lists the timing parameters.

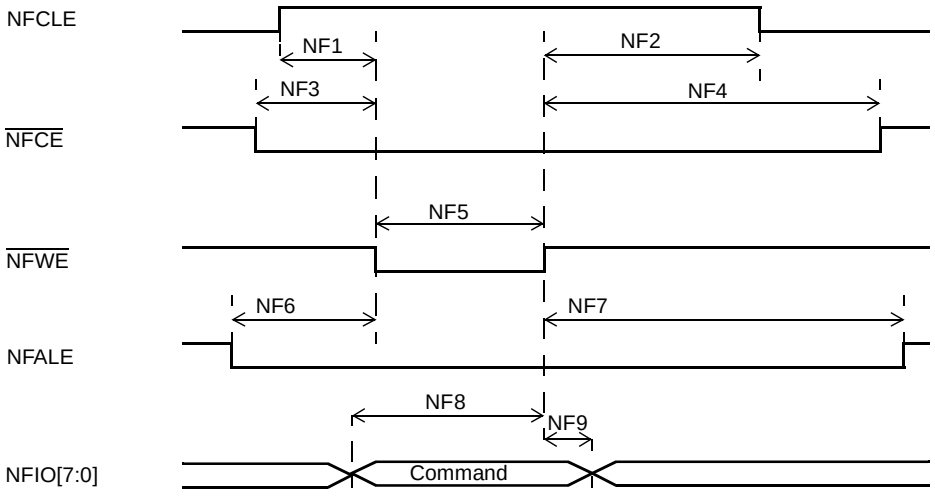



**Figure 22. Command Latch Cycle Timing Diagram**

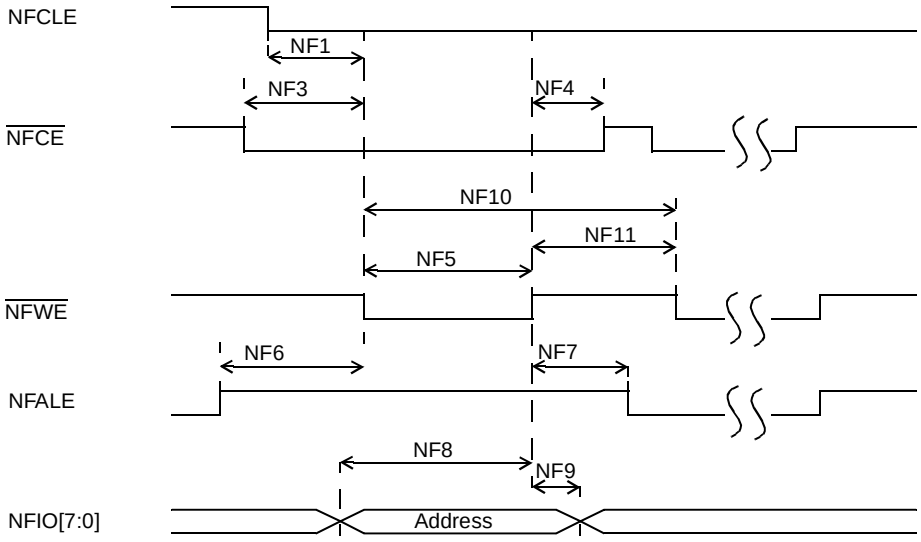



**Figure 23. Address Latch Cycle Timing Diagram**

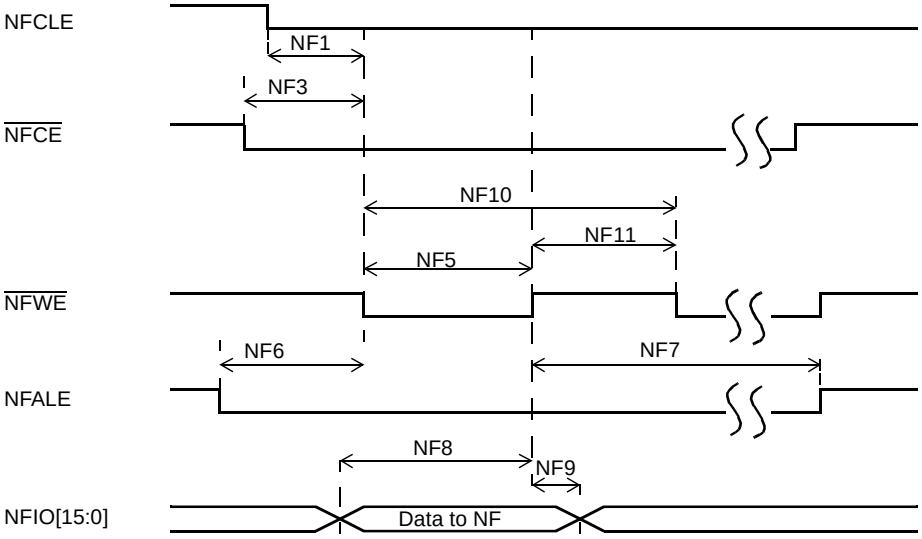



**Figure 24. Write Data Latch Cycle Timing Diagram**

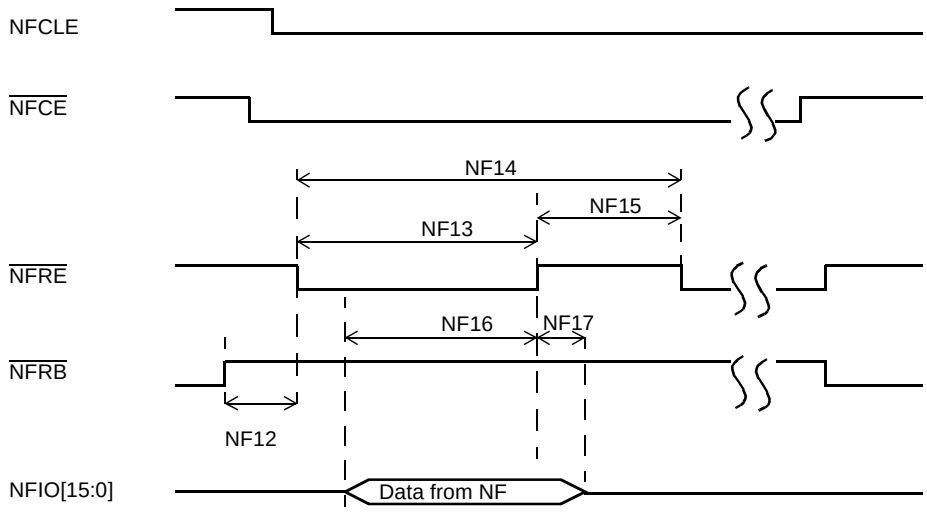



**Figure 25. Read Data Latch Cycle Timing Diagram**

**Table 31. NFC Timing Parameters[1]**

| ID | Parameter | Symbol | Timing T = NFC Clock Cycle[2] | | Example Timing for NFC Clock ≈ 33 MHz T = 30 ns | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| NF1 | NFCLE Setup Time | tCLS | T–1.0 ns | — | 29 | — | ns |
| NF2 | NFCLE Hold Time | tCLH | T–2.0 ns | — | 28 | — | ns |
| NF3 | $\overline{\text{NFCE}}$ Setup Time | tCS | T–1.0 ns | — | 29 | — | ns |
| NF4 | $\overline{\text{NFCE}}$ Hold Time | tCH | T–2.0 ns | — | 28 | — | ns |
| NF5 | $\overline{\text{NF_WP}}$ Pulse Width | tWP | T–1.5 ns | | 28.5 | | ns |
| NF6 | NFALE Setup Time | tALS | T | — | 30 | — | ns |
| NF7 | NFALE Hold Time | tALH | T–3.0 ns | — | 27 | — | ns |
| NF8 | Data Setup Time | tDS | T | — | 30 | — | ns |
| NF9 | Data Hold Time | tDH | T–5.0 ns | — | 25 | — | ns |
| NF10 | Write Cycle Time | tWC | 2T | | 60 | | ns |
| NF11 | $\overline{\text{NFWE}}$ Hold Time | tWH | T–2.5 ns | | 27.5 | | ns |
| NF12 | Ready to $\overline{\text{NFRE}}$ Low | tRR | 6T | — | 180 | — | ns |
| NF13 | $\overline{\text{NFRE}}$ Pulse Width | tRP | 1.5T | — | 45 | — | ns |
| NF14 | READ Cycle Time | tRC | 2T | — | 60 | — | ns |
| NF15 | $\overline{\text{NFRE}}$ High Hold Time | tREH | 0.5T–2.5 ns | | 12.5 | — | ns |
| NF16 | Data Setup on READ | tDSR | N/A | | 10 | — | ns |
| NF17 | Data Hold on READ | tDHR | N/A | | 0 | — | ns |

1 The flash clock maximum frequency is 50 MHz.

2 Subject to DPLL jitter specification on Table 30, "DPLL Specifications," on page 35.

**NOTE**

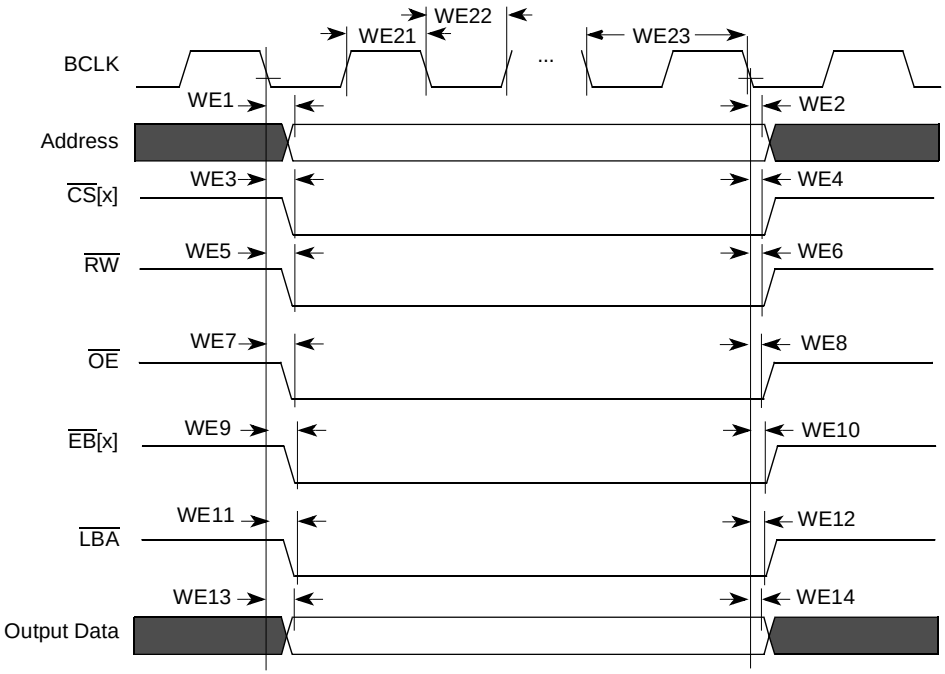
High is defined as 80% of signal value and low is defined as 20% of signal value.

Timing for HCLK is 133 MHz and internal NFC clock (flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not NFC clock related.

#### 4.3.9.2 Wireless External Interface Module (WEIM)

All WEIM output control signals may be asserted and deasserted by internal clock related to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins related to BCLK falling edge but may be ended both on rising and falling edge in muxed mode according to control register configuration. Output data begins related to BCLK rising edge except in muxed mode where both rising and falling edge may be used according to control register configuration. Input data, $\overline{\text{ECB}}$ and $\overline{\text{DTACK}}$ all captured according to BCLK rising edge time. Figure 26 depicts the timing of the WEIM module, and Table 32 lists the timing parameters.

**WEIM Outputs Timing**




**WEIM Inputs Timing**

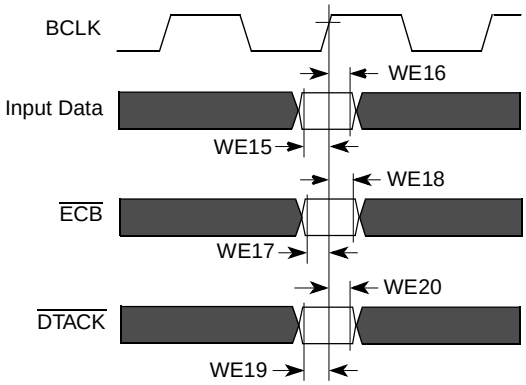



**Figure 26. WEIM Bus Timing Diagram**

**Table 32. WEIM Bus Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| WE1 | Clock fall to Address Valid | –0.5 | 2.5 | ns |
| WE2 | Clock rise/fall to Address Invalid | –0.5 | 5 | ns |
| WE3 | Clock rise/fall to $\overline{CS}$[x] Valid | –3 | 3 | ns |
| WE4 | Clock rise/fall to $\overline{CS}$[x] Invalid | –3 | 3 | ns |
| WE5 | Clock rise/fall to $\overline{RW}$ Valid | –3 | 3 | ns |
| WE6 | Clock rise/fall to $\overline{RW}$ Invalid | –3 | 3 | ns |
| WE7 | Clock rise/fall to $\overline{OE}$ Valid | –3 | 3 | ns |

**Table 32. WEIM Bus Timing Parameters (continued)**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| WE8 | Clock rise/fall to $\overline{OE}$ Invalid | –3 | 3 | ns |
| WE9 | Clock rise/fall to $\overline{EB}$[x] Valid | –3 | 3 | ns |
| WE10 | Clock rise/fall to $\overline{EB}$[x] Invalid | –3 | 3 | ns |
| WE11 | Clock rise/fall to $\overline{LBA}$ Valid | –3 | 3 | ns |
| WE12 | Clock rise/fall to $\overline{LBA}$ Invalid | –3 | 3 | ns |
| WE13 | Clock rise/fall to Output Data Valid | –2.5 | 4 | ns |
| WE14 | Clock rise to Output Data Invalid | –2.5 | 4 | ns |
| WE15 | Input Data Valid to Clock rise, FCE=0<br>FCE=1 | 8<br>2.5 | — | ns |
| WE16 | Clock rise to Input Data Invalid, FCE=0<br>FCE=1 | –2<br>–2 | — | ns |
| WE17 | $\overline{ECB}$ setup time, FCE=0<br>FCE=1 | 6.5<br>3.5 | — | ns |
| WE18 | $\overline{ECB}$ hold time, FCE=0<br>FCE=1 | –2<br>2 | — | ns |
| WE19 | $\overline{DTACK}$ setup time[1] | 0 | — | ns |
| WE20 | $\overline{DTACK}$ hold time[1] | 4.5 | — | ns |
| WE21 | BCLK High Level Width[2, 3] | — | T/2 – 3 | ns |
| WE22 | BCLK Low Level Width[2, 3] | — | T/2 – 3 | ns |
| WE23 | BCLK Cycle time[2] | 15 | — | ns |

1 Applies to rising edge timing

2 BCLK parameters are being measured from the 50% VDD.

3 The actual cycle time is derived from the AHB bus clock frequency.

**NOTE**

High is defined as 80% of signal value and low is defined as 20% of signal value.

Test conditions: load capacitance, 25 pF. Recommended drive strength for all controls, address, and BCLK is Max drive.

Figure 27, Figure 28, Figure 29, Figure 30, Figure 31, and Figure 32 depict some examples of basic WEIM accesses to external memory devices with the timing parameters mentioned in Table 32 for specific control parameter settings.

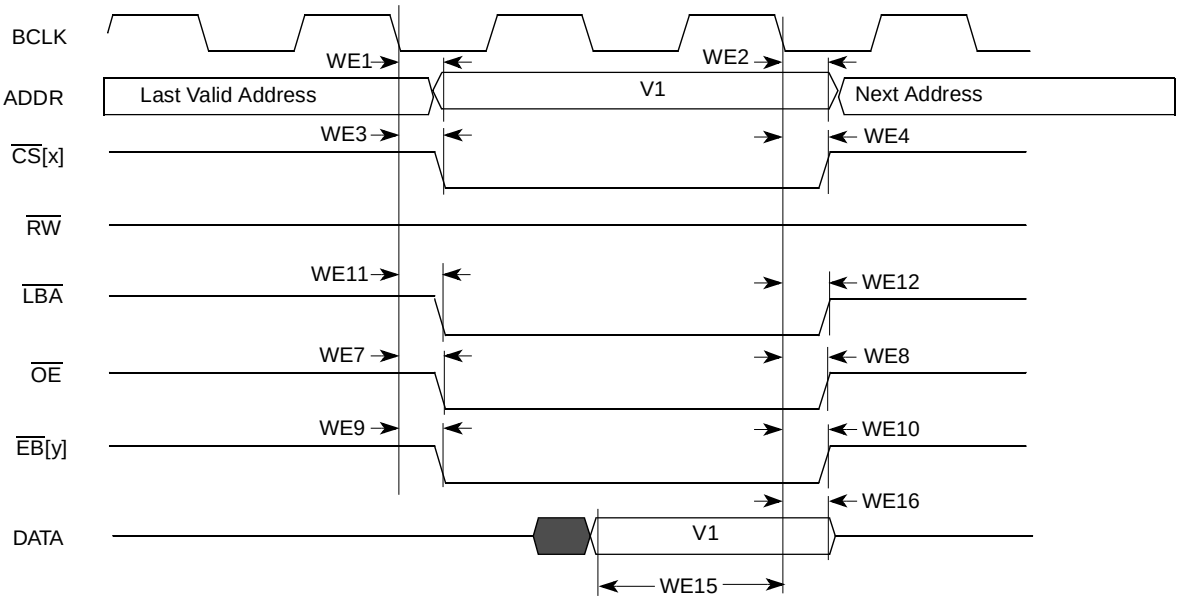



**Figure 27. Asynchronous Memory Timing Diagram for Read Access—WSC=1**

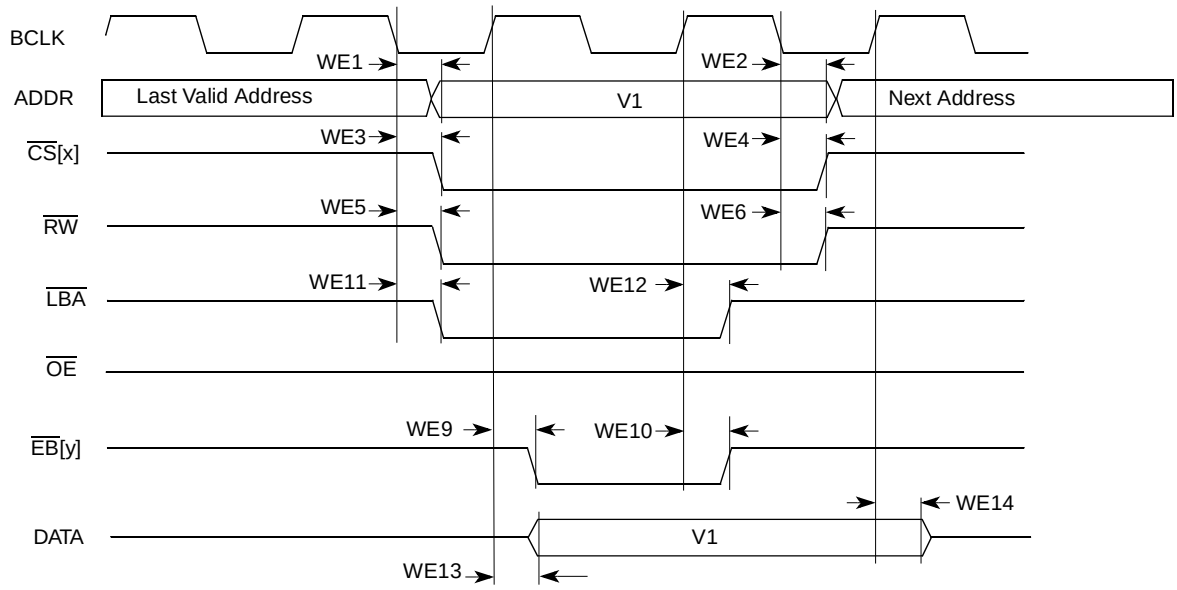



**Figure 28. Asynchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1**

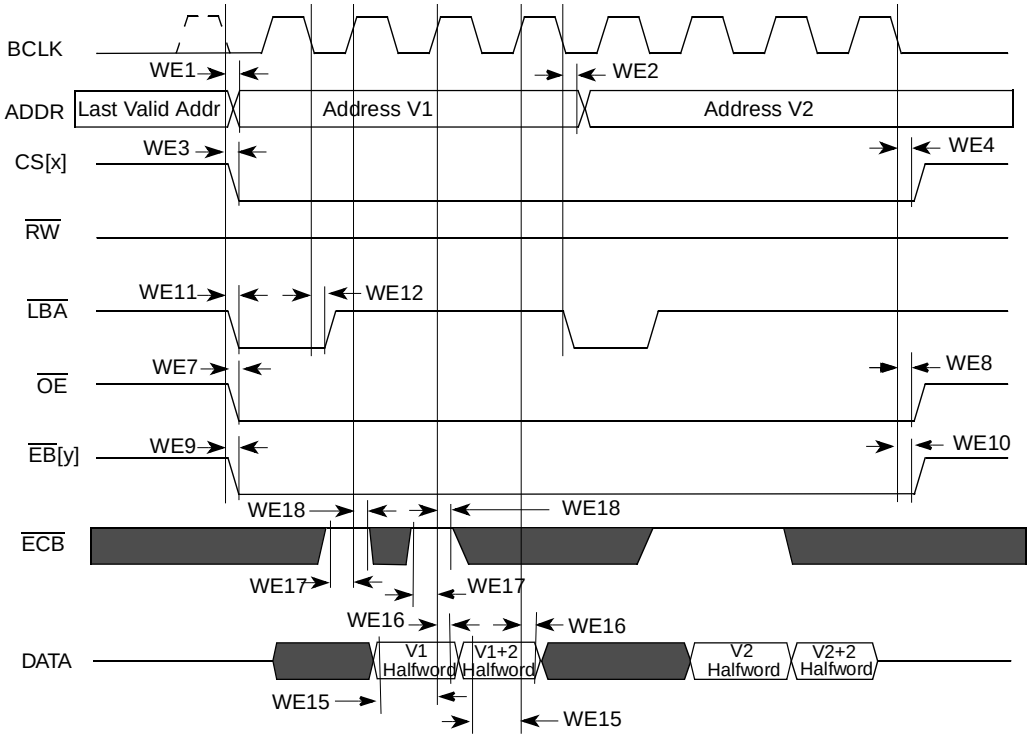



**Figure 29. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—WSC=2, SYNC=1, DOL=0**

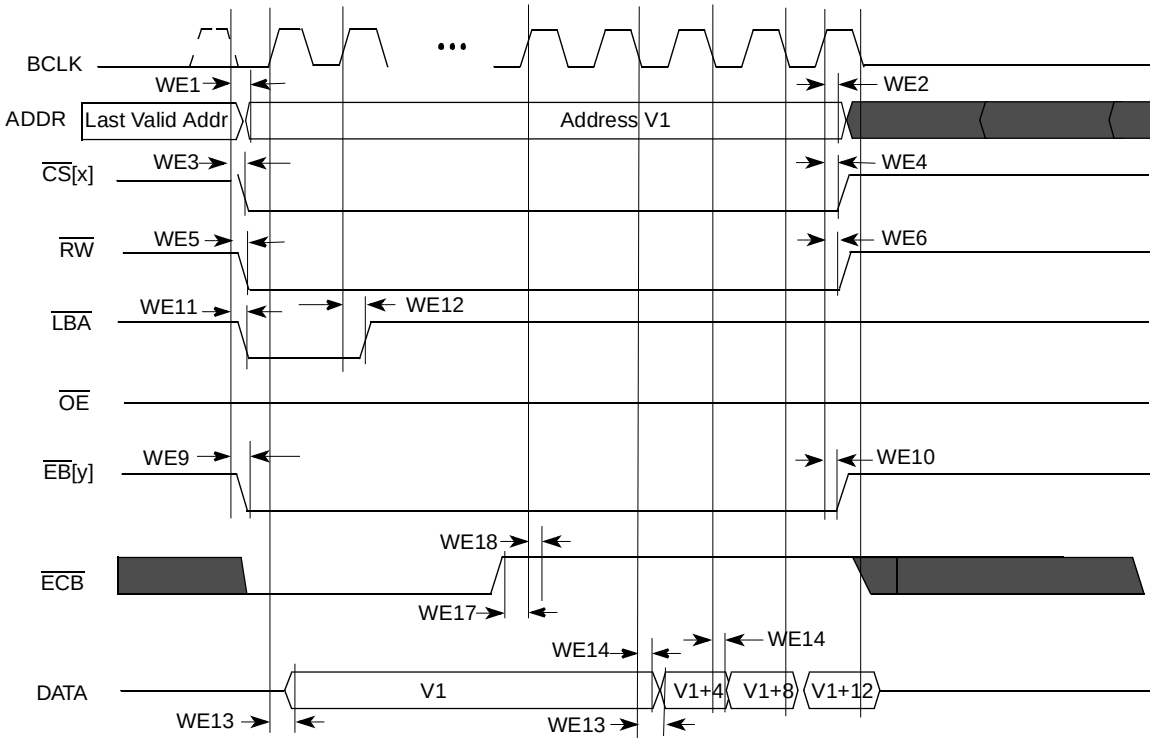



**Figure 30. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1**

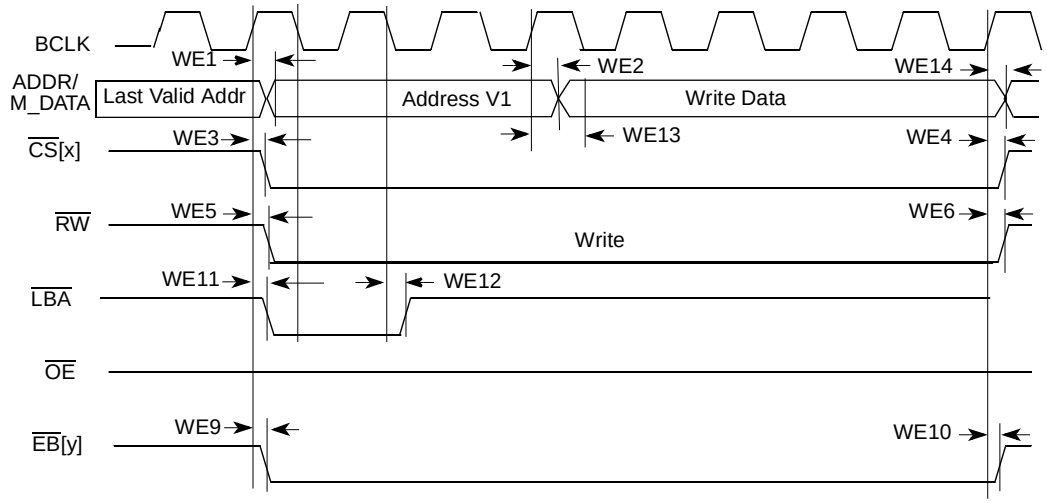



**Figure 31. Muxed A/D Mode Timing Diagram for Asynchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1**

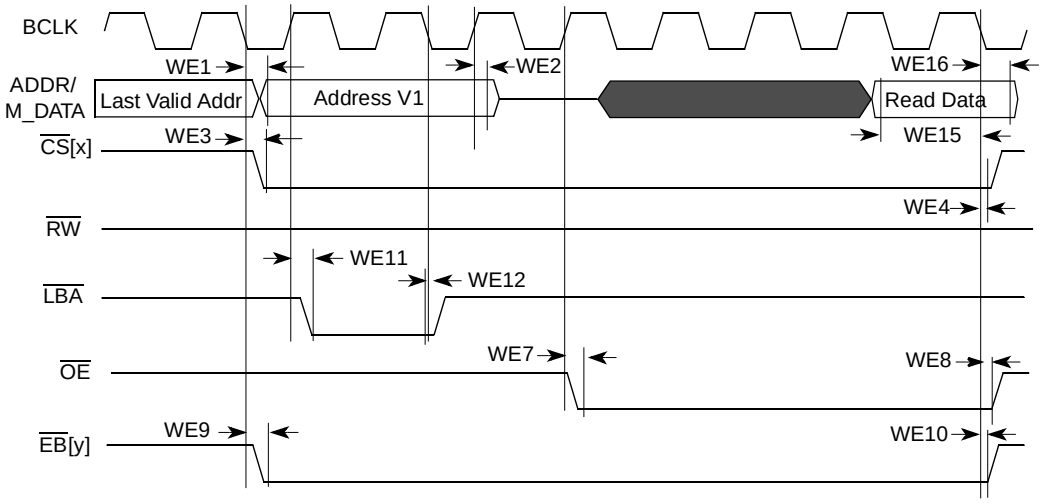



**Figure 32. Muxed A/D Mode Timing Diagram for Asynchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7**

### 4.3.9.3 ESDCTL Electrical Specifications

Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, and Figure 38 depict the timings pertaining to the ESDCTL module, which interfaces Mobile DDR or SDR SDRAM. Table 33, Table 34, Table 35, Table 36, Table 37, and Table 38 list the timing parameters.

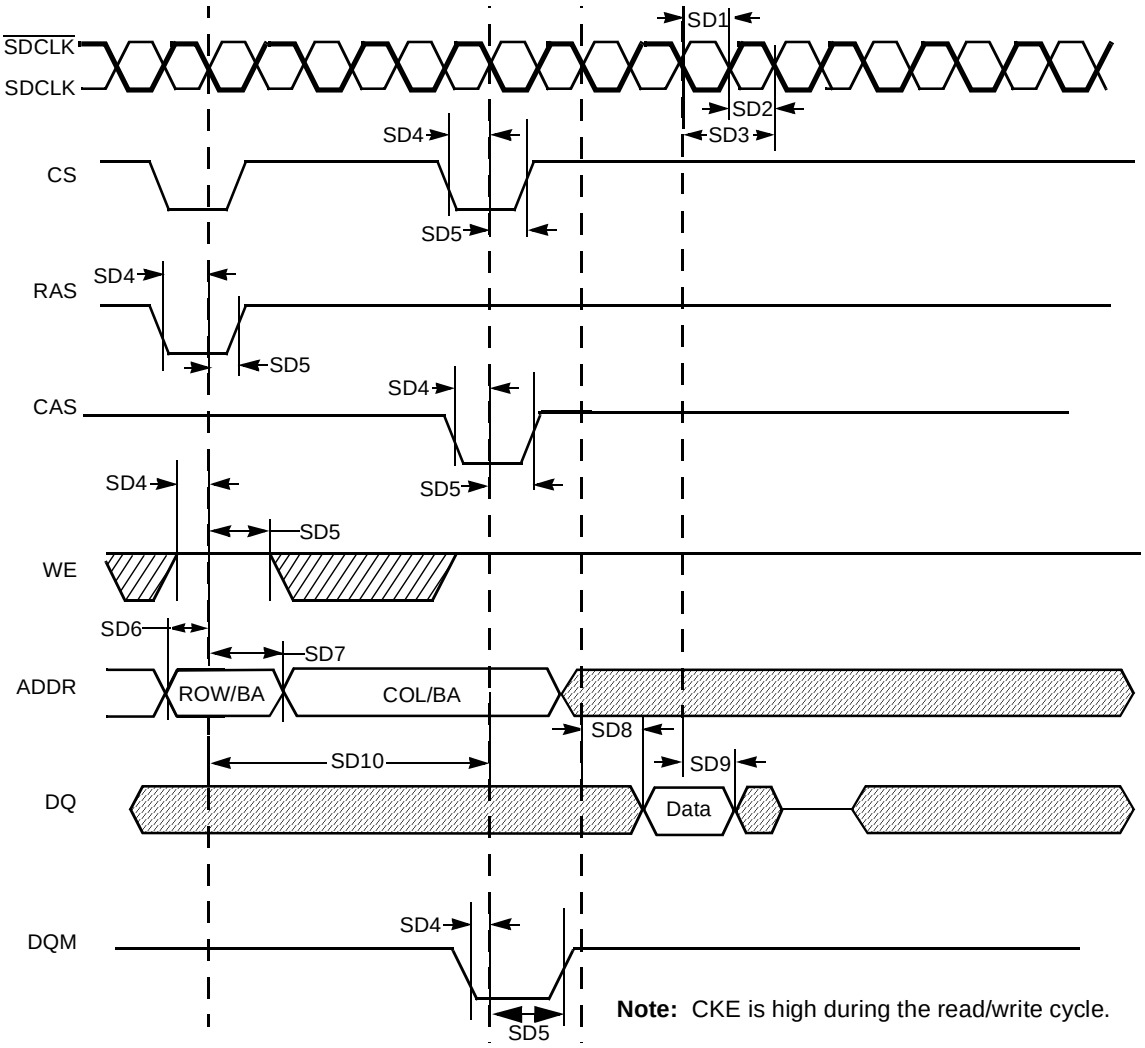



**Figure 33. SDRAM Read Cycle Timing Diagram**

**Table 33. DDR/SDR SDRAM Read Cycle Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | $\overline{\text{SDRAM clock low-level width}}$ | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD8 | SDRAM access time | tAC | — | 6.47 | ns |

**Table 33. DDR/SDR SDRAM Read Cycle Timing Parameters (continued)**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD9 | Data out hold time[1] | tOH | 1.8 | — | ns |
| SD10 | Active to read/write command period | tRC | 10 | — | clock |

1 Timing parameters are relevant only to SDR SDRAM. For the specific DDR SDRAM data related timing parameters, see Table 37 and Table 38.

**NOTE**

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value. SD1 + SD2 does not exceed 7.5 ns for 133 MHz.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 33 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

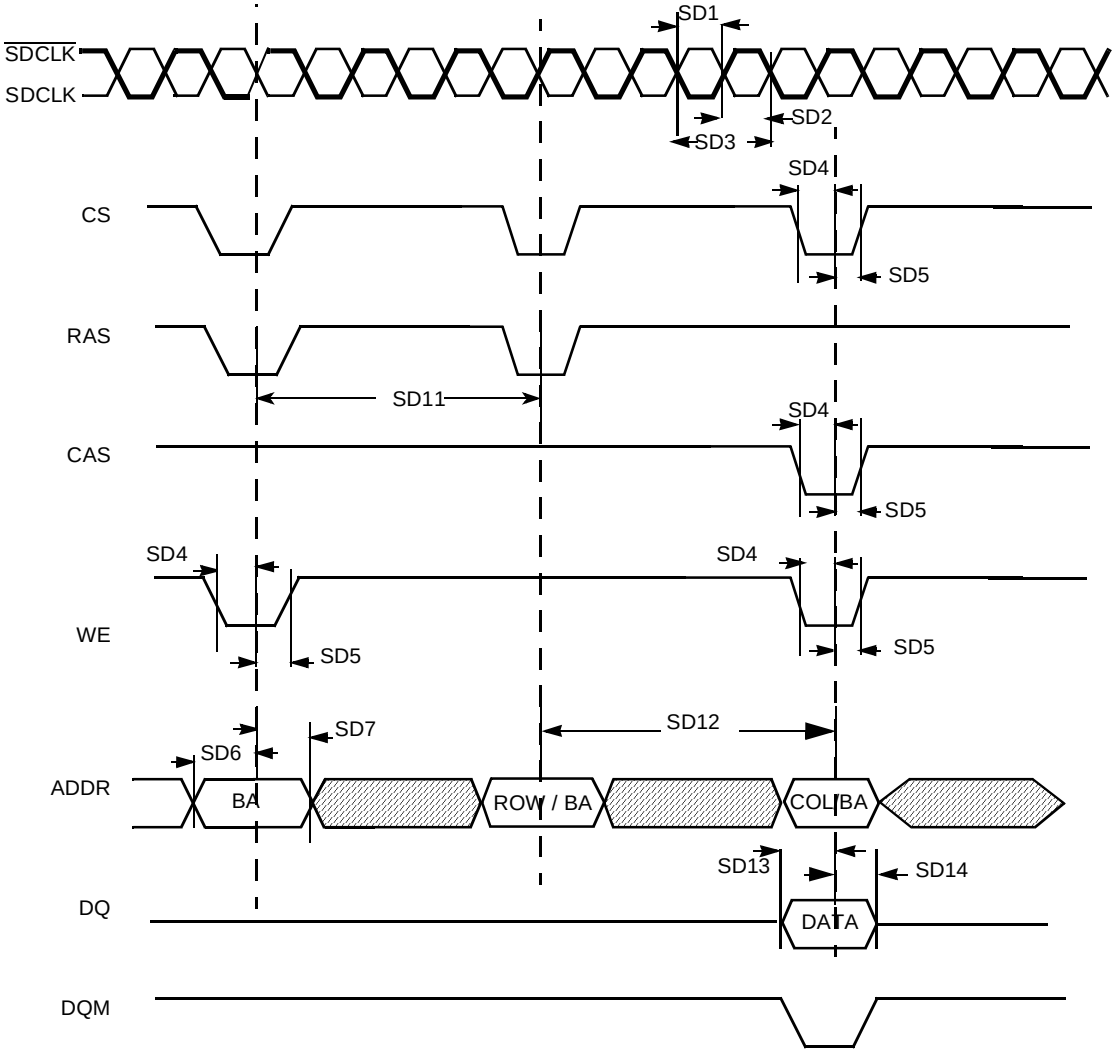



**Figure 34. SDR SDRAM Write Cycle Timing Diagram**

**Table 34. SDR SDRAM Write Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | $\overline{\text{SDRAM clock low-level width}}$ | tCL | 3.4 | 4.1 | ns |
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD4 | CS, RAS, CAS, WE, DQM, CKE setup time | tCMS | 2.0 | — | ns |
| SD5 | CS, RAS, CAS, WE, DQM, CKE hold time | tCMH | 1.8 | — | ns |
| SD6 | Address setup time | tAS | 2.0 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD11 | Precharge cycle period[1] | tRP | 1 | 4 | clock |
| SD12 | Active to read/write command delay[1] | tRCD | 1 | 8 | clock |

**Table 34. SDR SDRAM Write Timing Parameters (continued)**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD13 | Data setup time | tDS | 2.0 | — | ns |
| SD14 | Data hold time | tDH | 1.3 | — | ns |

1 SD11 and SD12 are determined by SDRAM controller register settings.

**NOTE**

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 34 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

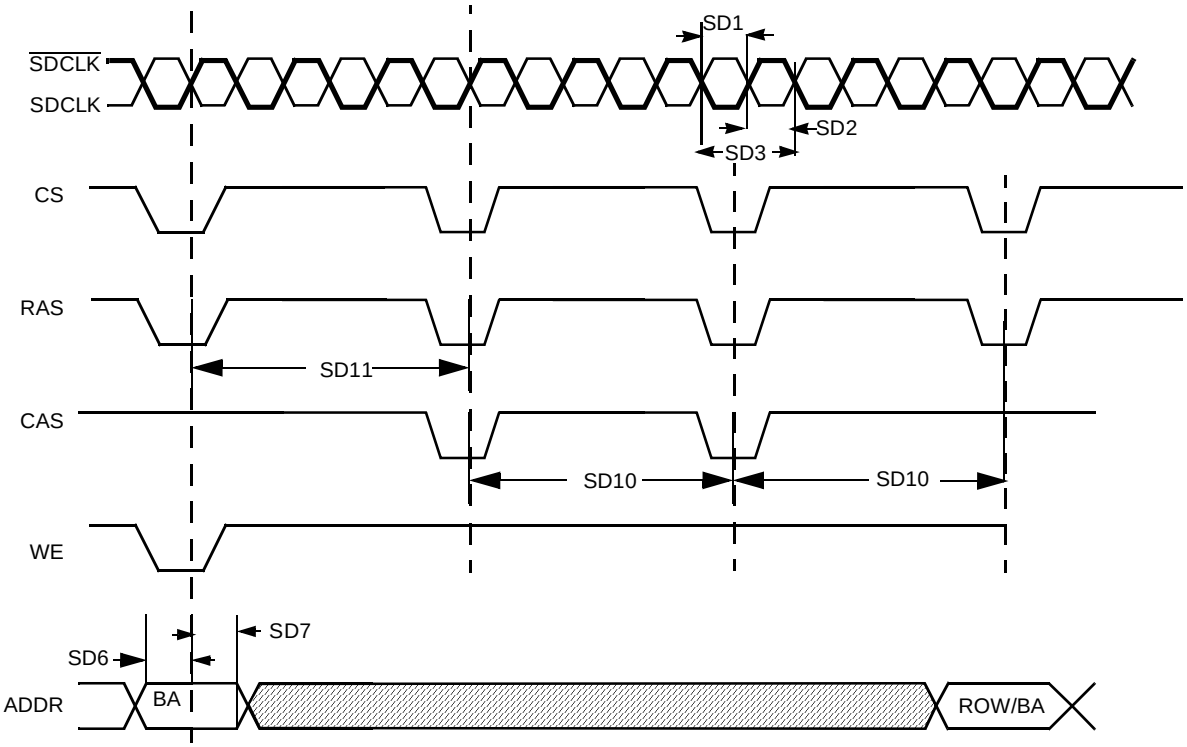



**Figure 35. SDRAM Refresh Timing Diagram**

**Table 35. SDRAM Refresh Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD1 | SDRAM clock high-level width | tCH | 3.4 | 4.1 | ns |
| SD2 | $\overline{\text{SDRAM clock low-level width}}$ | tCL | 3.4 | 4.1 | ns |

**Table 35. SDRAM Refresh Timing Parameters (continued)**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD3 | SDRAM clock cycle time | tCK | 7.5 | — | ns |
| SD6 | Address setup time | tAS | 1.8 | — | ns |
| SD7 | Address hold time | tAH | 1.8 | — | ns |
| SD10 | Precharge cycle period[1] | tRP | 1 | 4 | clock |
| SD11 | Auto precharge command period[1] | tRC | 2 | 20 | clock |

1 SD10 and SD11 are determined by SDRAM controller register settings.

**NOTE**

SDR SDRAM CLK parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 35 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

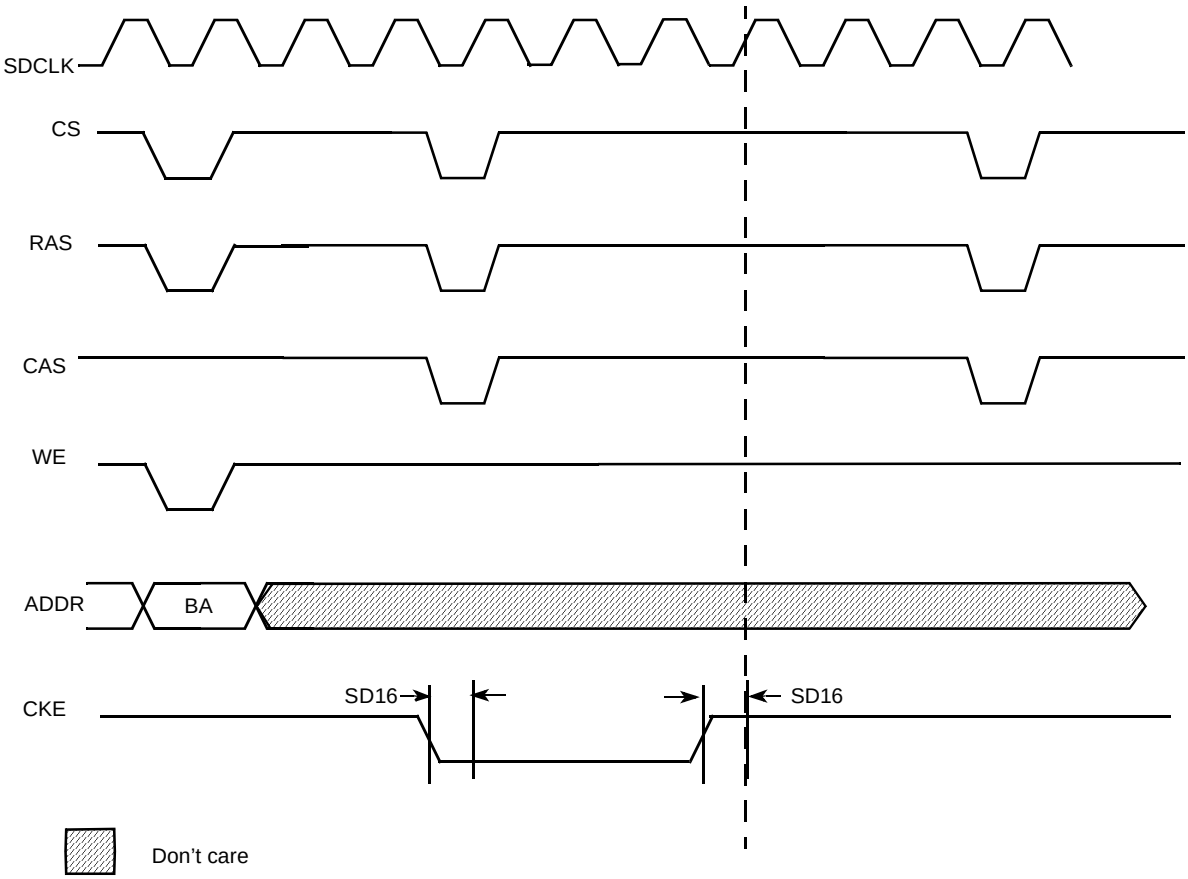



**Figure 36. SDRAM Self-Refresh Cycle Timing Diagram**

## NOTE

The clock will continue to run unless both CKEs are low. Then the clock will be stopped in low state.

**Table 36. SDRAM Self-Refresh Cycle Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD16 | CKE output delay time | tCKS | 1.8 | — | ns |

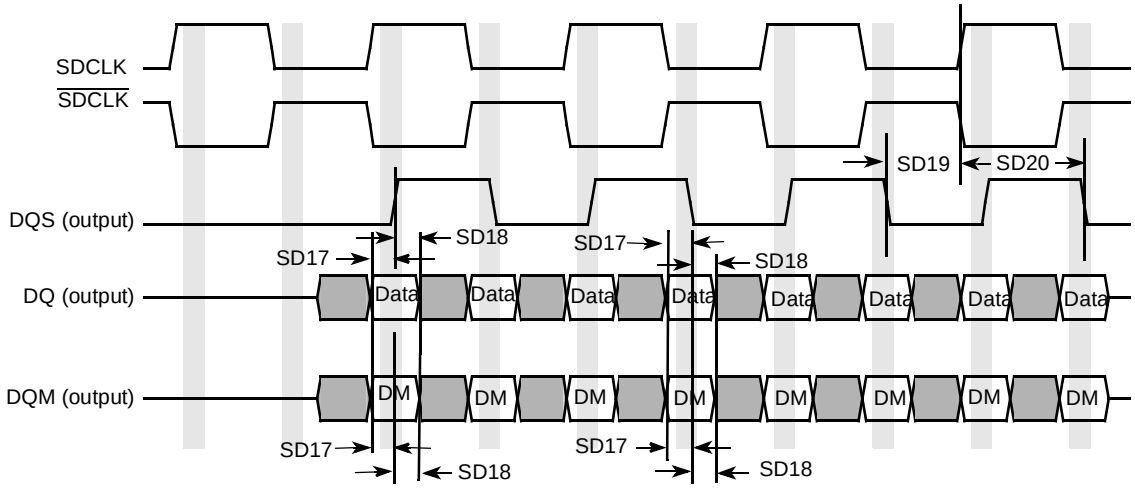



**Figure 37. Mobile DDR SDRAM Write Cycle Timing Diagram**

**Table 37. Mobile DDR SDRAM Write Cycle Timing Parameters[1]**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD17 | DQ and DQM setup time to DQS | tDS | 0.95 | — | ns |
| SD18 | DQ and DQM hold time to DQS | tDH | 0.95 | — | ns |
| SD19 | Write cycle DQS falling edge to SDCLK output delay time. | tDSS | 1.8 | — | ns |
| SD20 | Write cycle DQS falling edge to SDCLK output hold time. | tDSH | 1.8 | — | ns |

1 Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

## NOTE

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 37 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

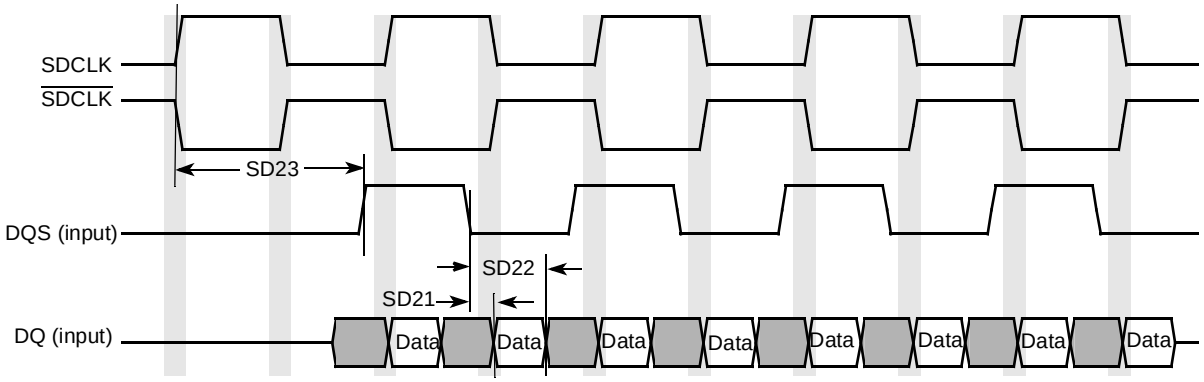



**Figure 38. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram**

**Table 38. Mobile DDR SDRAM Read Cycle Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| SD21 | DQS – DQ Skew (defines the Data valid window in read cycles related to DQS). | tDQSQ | — | 0.85 | ns |
| SD22 | DQS DQ HOLD time from DQS | tQH | 2.3 | — | ns |
| SD23 | DQS output access time from SDCLK posedge | tDQSCK | — | 6.7 | ns |

**NOTE**

SDRAM CLK and DQS related parameters are being measured from the 50% point—that is, high is defined as 50% of signal value and low is defined as 50% of signal value.

The timing parameters are similar to the ones used in SDRAM data sheets—that is, Table 38 indicates SDRAM requirements. All output signals are driven by the ESDCTL at the negative edge of SDCLK and the parameters are measured at maximum memory frequency.

## 4.3.10 ETM Electrical Specifications

ETM is an ARM protocol. The timing specifications in this section are given as a guide for a TPA that supports TRACECLK frequencies up to 133 MHz.

Figure 39 depicts the TRACECLK timings of ETM, and Table 39 lists the timing parameters.

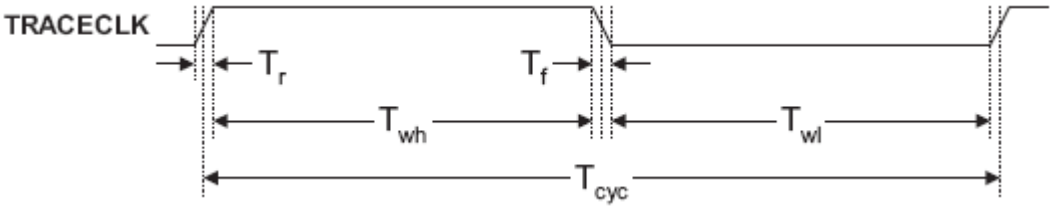



**Figure 39. ETM TRACECLK Timing Diagram**

**Table 39. ETM TRACECLK Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cyc}$ | Clock period | Frequency dependent | — | ns |
| $T_{wl}$ | Low pulse width | 2 | — | ns |
| $T_{wh}$ | High pulse width | 2 | — | ns |
| $T_r$ | Clock and data rise time | — | 3 | ns |
| $T_f$ | Clock and data fall time | — | 3 | ns |

Figure 40 depicts the setup and hold requirements of the trace data pins with respect to TRACECLK, and Table 40 lists the timing parameters.

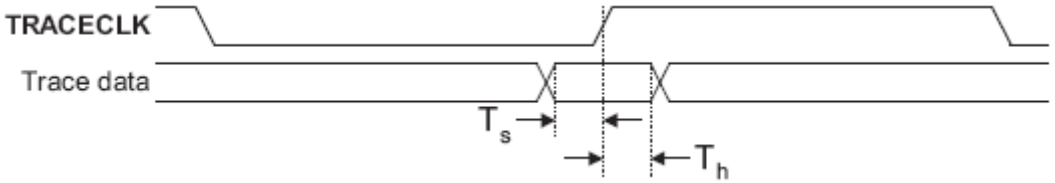



**Figure 40. Trace Data Timing Diagram**

**Table 40. ETM Trace Data Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_s$ | Data setup | 2 | — | ns |
| $T_h$ | Data hold | 1 | — | ns |

### 4.3.10.1 Half-Rate Clocking Mode

When half-rate clocking is used, the trace data signals are sampled by the TPA on both the rising and falling edges of TRACECLK, where TRACECLK is half the frequency of the clock shown in Figure 40.

## 4.3.11 FIR Electrical Specifications

FIR implements asynchronous infrared protocols (FIR, MIR) that are defined by IrDA® (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and MIR protocols.

## 4.3.12 Fusebox Electrical Specifications

**Table 41. Fusebox Timing Characteristics**

| Ref. Num | Description | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| 1 | Program time for eFuse[1] | $t_{program}$ | 125 | — | — | µs |

1 The program length is defined by the value defined in the epm_pgm_length[2:0] bits of the IIM module. The value to program is based on a 32 kHz clock source (4 * 1/32 kHz = 125 µs).

## 4.3.13 I²C Electrical Specifications

This section describes the electrical information of the I²C Module.

### 4.3.13.1 I²C Module Timing

Figure 41 depicts the timing of I²C module. Table 42 lists the I²C module timing parameters where the I/O supply is 2.7 V. 1

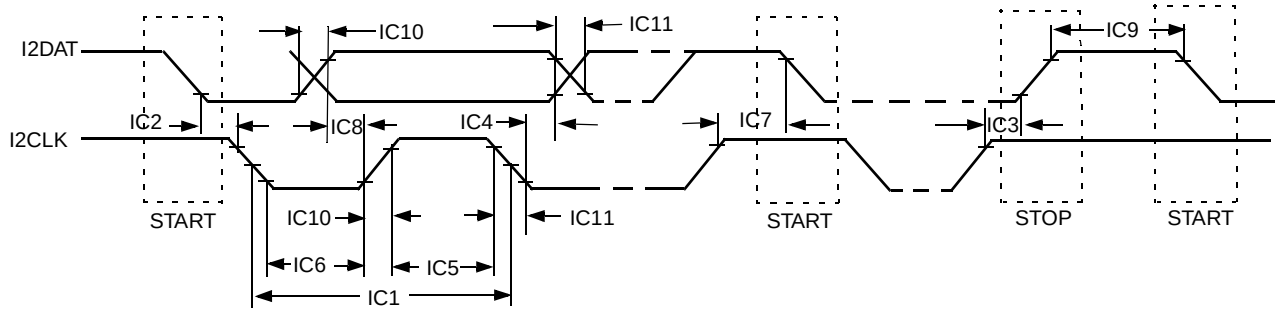



**Figure 41. I²C Bus Timing Diagram**

**Table 42. I²C Module Timing Parameters—I²C Pin I/O Supply=2.7 V**

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| IC1 | I2CLK cycle time | 10 | — | 2.5 | — | µs |
| IC2 | Hold time (repeated) START condition | 4.0 | — | 0.6 | — | µs |
| IC3 | Set-up time for STOP condition | 4.0 | — | 0.6 | — | µs |
| IC4 | Data hold time | 0[1] | 3.45[2] | 0[1] | 0.9[2] | µs |
| IC5 | HIGH Period of I2CLK Clock | 4.0 | — | 0.6 | — | µs |
| IC6 | LOW Period of the I2CLK Clock | 4.7 | — | 1.3 | — | µs |
| IC7 | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | µs |
| IC8 | Data set-up time | 250 | — | 100[3] | — | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | µs |
| IC10 | Rise time of both I2DAT and I2CLK signals | — | 1000 | $20+0.1C_b$[4] | 300 | ns |
| IC11 | Fall time of both I2DAT and I2CLK signals | — | 300 | $20+0.1C_b$[4] | 300 | ns |
| IC12 | Capacitive load for each bus line ($C_b$) | — | 400 | — | 400 | pF |

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has to be met only if the device does not stretch the LOW period (ID IC6) of the I2CLK signal.

3 A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement of set-up time (ID IC7) of 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

4 $C_b$ = total capacitance of one bus line in pF.

## 4.3.14 IPU—Sensor Interfaces

### 4.3.14.1 Supported Camera Sensors

Table 43 lists the known supported camera sensors at the time of publication.

**Table 43. Supported Camera Sensors[1]**

| Vendor | Model |
|---|---|
| Conexant | CX11646, CX20490[2], CX20450[2] |
| Agilant | HDCP–2010, ADCS–1021[2], ADCS–1021[2] |
| Toshiba | TC90A70 |
| ICMedia | ICM202A, ICM102[2] |
| iMagic | IM8801 |
| Transchip | TC5600, TC5600J, TC5640, TC5700, TC6000 |
| Fujitsu | MB86S02A |
| Micron | MI–SOC–0133 |
| Matsushita | MN39980 |
| STMicro | W6411, W6500, W6501[2], W6600[2], W6552[2], STV0974[2] |
| OmniVision | OV7620, OV6630 |
| Sharp | LZ0P3714 (CCD) |
| Motorola | MC30300 (Python)[2], SCM20014[2], SCM20114[2], SCM22114[2], SCM20027[2] |
| National Semiconductor | LM9618[2] |

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only camera suppliers.

2 These sensors not validated at time of publication.

### 4.3.14.2 Functional Description

There are three timing modes supported by the IPU.

#### 4.3.14.2.1 Pseudo BT.656 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656 standard.

This operation mode follows the recommendations of ITU BT.656 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use.

#### 4.3.14.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 42.

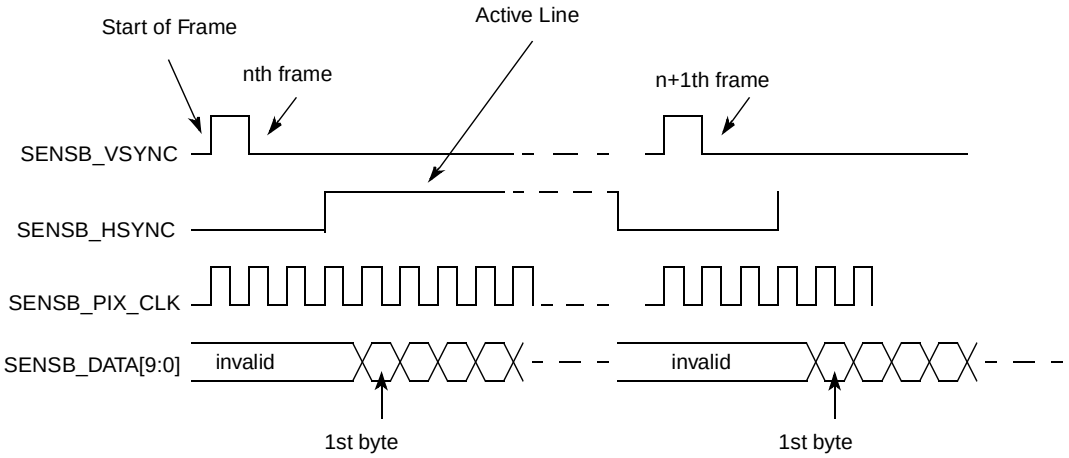



**Figure 42. Gated Clock Mode Timing Diagram**

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

#### 4.3.14.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.3.14.2.2, “Gated Clock Mode”), except for the SENSB_HSYNC signal, which is not used. See Figure 43. All incoming pixel clocks are valid and will cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

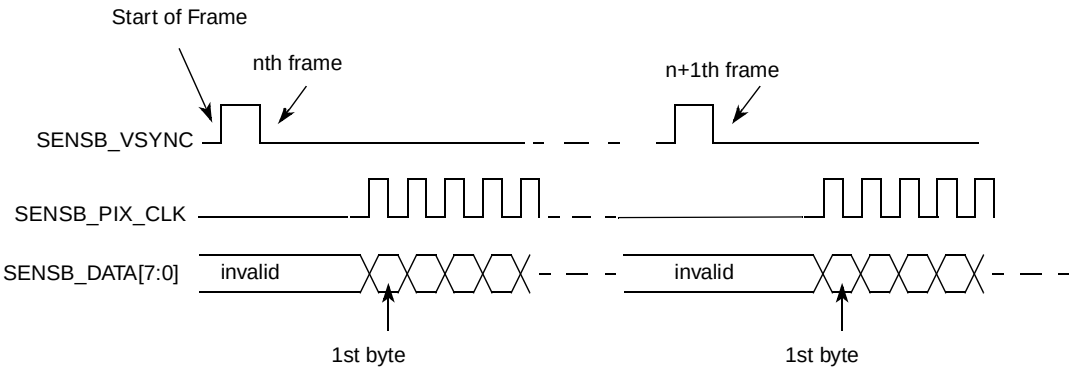



**Figure 43. Non-Gated Clock Mode Timing Diagram**

The timing described in Figure 43 is that of a Motorola sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

### 4.3.14.3 Electrical Characteristics

Figure 44 depicts the sensor interface timing, and Table 44 lists the timing parameters.

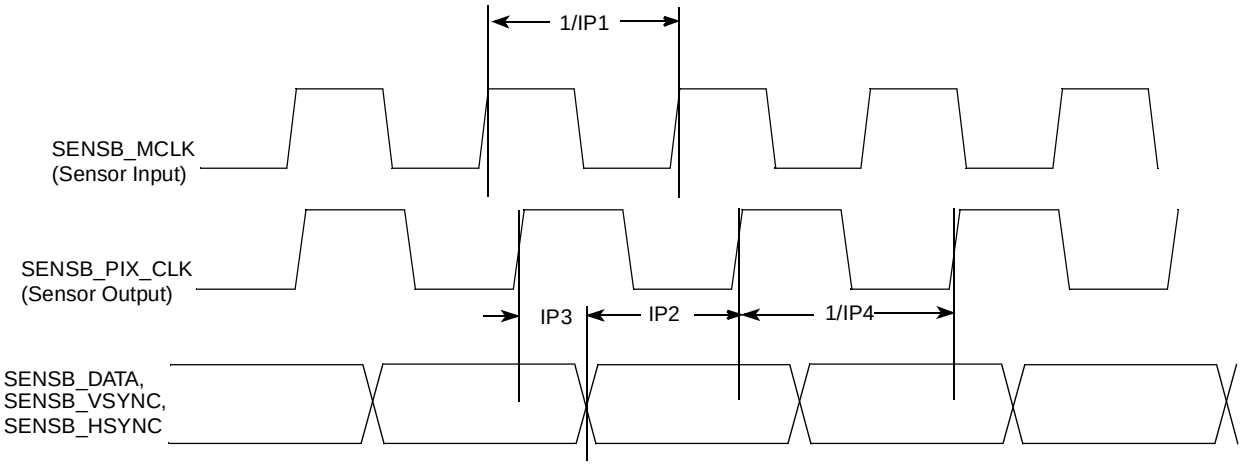



**Figure 44. Sensor Interface Timing Diagram**

**Table 44. Sensor Interface Timing Parameters[1]**

| ID | Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|
| IP1 | Sensor input clock frequency | Fmck | 0.01 | 133 | MHz |
| IP2 | Data and control setup time | Tsu | 5 | — | ns |
| IP3 | Data and control holdup time | Thd | 3 | — | ns |
| IP4 | Sensor output (pixel) clock frequency | Fpck | 0.01 | 133 | MHz |

1 The timing specifications for Figure 44 are referenced to the rising edge of SENS_PIX_CLK when the SENS_PIX_CLK_POL bit in the CSI_SENS_CONF register is cleared. When the SENS_PIX_CLK_POL is set, the clock is inverted and all timing specifications will remain the same but are referenced to the falling edge of the clock.

## 4.3.15 IPU—Display Interfaces

### 4.3.15.1 Supported Display Components

Table 45 lists the known supported display components at the time of publication.

**Table 45. Supported Display Components[1]**

| Type | Vendor | Model |
|---|---|---|
| TFT displays (memory-less) | Sharp (HR-TFT Super Mobile LCD family) | LQ035Q7 DB02, LM019LC1Sxx |
| | Samsung (QCIF and QVGA TFT modules for mobile phones) | LTS180S1-HF1, LTS180S3-HF1, LTS350Q1-PE1, LTS350Q1-PD1, LTS220Q1-HE1[2] |
| | Toshiba (LTM series) | LTM022P806[2], LTM04C380K[2], LTM018A02A[2], LTM020P332[2], LTM021P337[2], LTM019P334[2], LTM022A783[2], LTM022A05ZZ[2] |
| | NEC | NL6448BC20-08E, NL8060BC31-27 |
| Display controllers | Epson | S1D15xxx series, S1D19xxx series, S1D13713, S1D13715 |
| | Solomon Systech | SSD1301 (OLED), SSD1828 (LDCD) |
| | Hitachi | HD66766, HD66772 |
| | ATI | W2300 |
| Smart display modules | Epson | L1F10043 T[2], L1F10044 T[2], L1F10045 T[2], L2D22002[2], L2D20014[2], L2F50032[2], L2D25001 T[2] |
| | Hitachi | 120 160 65K/4096 C-STN (#3284 LTD-1398-2) based on HD 66766 controller |
| | Densitron Europe LTD | All displays with MPU 80/68K series interface and serial peripheral interface |
| | Sharp | LM019LC1Sxx |
| | Sony | ACX506AKM |
| Digital video encoders (for TV) | Analog Devices | ADV7174/7179 |
| | Crystal (Cirrus Logic) | CS49xx series |
| | Focus | FS453/4 |

1 Freescale Semiconductor does not recommend one supplier over another and in no way suggests that these are the only display component suppliers.

2 These display components not validated at time of publication.

## 4.3.15.2 Synchronous Interfaces

### 4.3.15.2.1 Interface to Active Matrix TFT LCD Panels, Functional Description

Figure 45 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DISPB_D3_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, DISPB_D3_CLK runs continuously.
- DISPB_D3_HSYNC causes the panel to start a new line.
- DISPB_D3_VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.

- DISPB_D3_DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

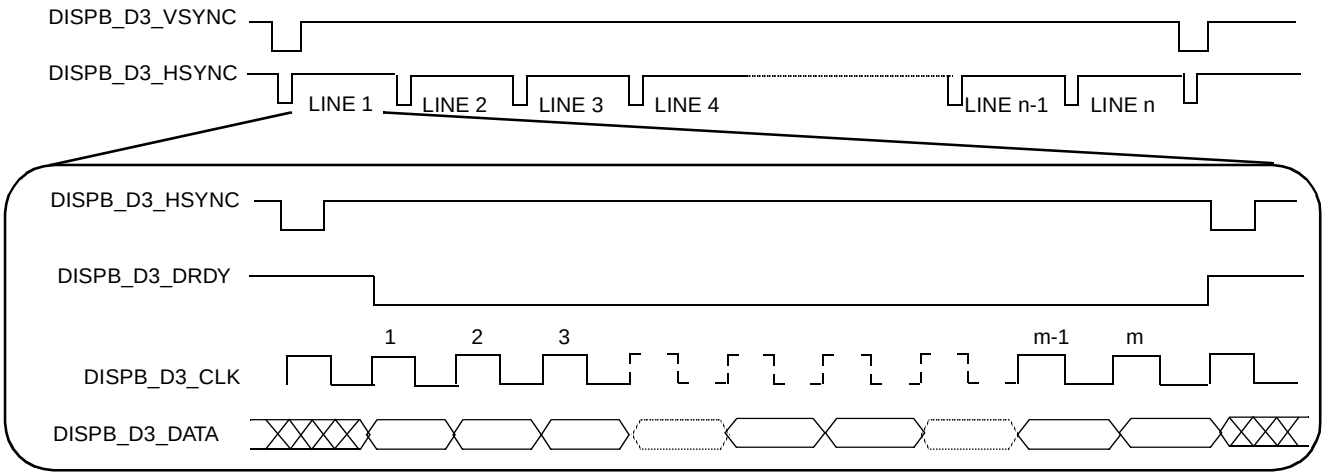



**Figure 45. Interface Timing Diagram for TFT (Active Matrix) Panels**

### 4.3.15.2.2 Interface to Active Matrix TFT LCD Panels, Electrical Characteristics

Figure 46 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All figure parameters shown are programmable. The timing images correspond to inverse polarity of the DISPB_D3_CLK signal and active-low polarity of the DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals.

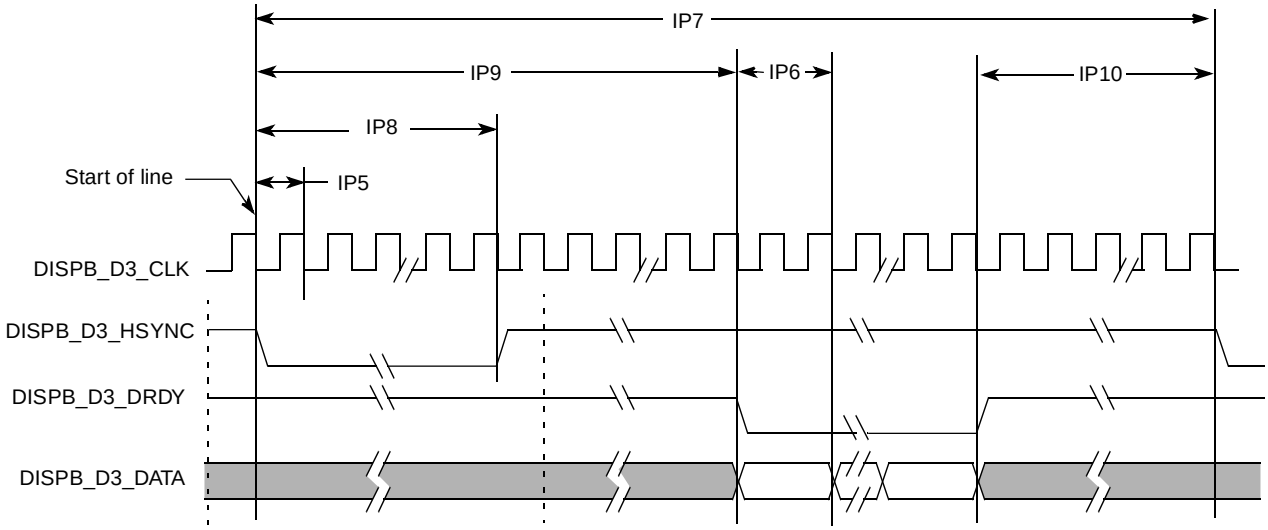



**Figure 46. TFT Panels Timing Diagram—Horizontal Sync Pulse**

Figure 47 depicts the vertical timing (timing of one frame). All figure parameters shown are programmable.

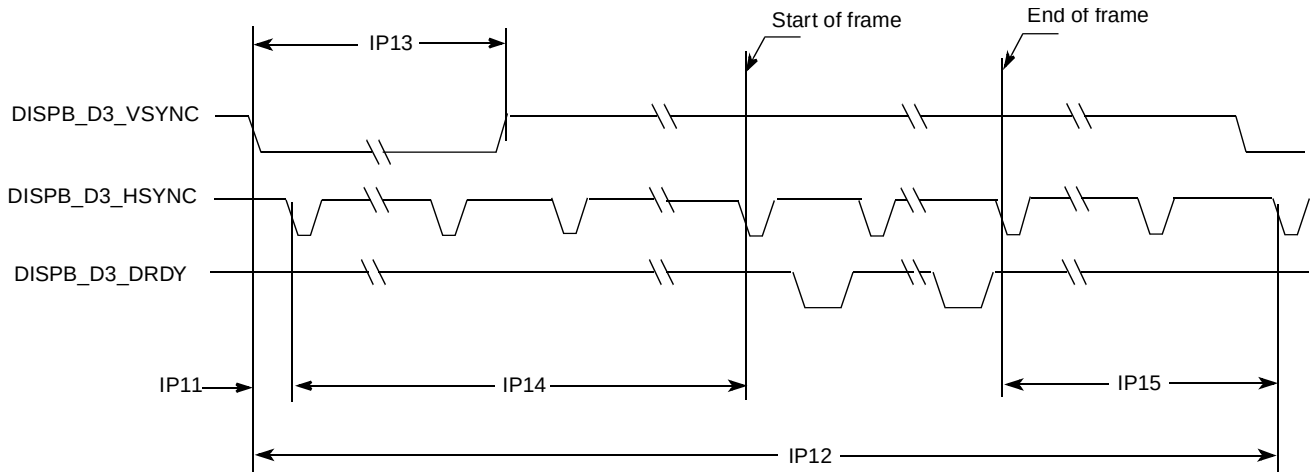



**Figure 47. TFT Panels Timing Diagram—Vertical Sync Pulse**

Table 46 shows timing parameters of signals presented in Figure 46 and Figure 47.

**Table 46. Synchronous Display Interface Timing Parameters—Pixel Level**

| ID | Parameter | Symbol | Value | Units |
|---|---|---|---|---|
| IP5 | Display interface clock period | Tdicp | Tdicp[1] | ns |
| IP6 | Display pixel clock period | Tdpcp | (DISP3_IF_CLK_CNT_D+1) * Tdicp | ns |
| IP7 | Screen width | Tsw | (SCREEN_WIDTH+1) * Tdpcp | ns |
| IP8 | HSYNC width | Thsw | (H_SYNC_WIDTH+1) * Tdpcp | ns |
| IP9 | Horizontal blank interval 1 | Thbi1 | BGXP * Tdpcp | ns |
| IP10 | Horizontal blank interval 2 | Thbi2 | (SCREEN_WIDTH – BGXP – FW) * Tdpcp | ns |
| IP11 | HSYNC delay | Thsd | H_SYNC_DELAY * Tdpcp | ns |
| IP12 | Screen height | Tsh | (SCREEN_HEIGHT+1) * Tsw | ns |
| IP13 | VSYNC width | Tvsw | if V_SYNC_WIDTH_L = 0 than<br>(V_SYNC_WIDTH+1) * Tdpcp<br>else<br>(V_SYNC_WIDTH+1) * Tsw | ns |
| IP14 | Vertical blank interval 1 | Tvbi1 | BGYP * Tsw | ns |
| IP15 | Vertical blank interval 2 | Tvbi2 | (SCREEN_HEIGHT – BGYP – FH) * Tsw | ns |

1 Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{HSP_CLK} \cdot \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD}, & \text{for integer } \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD} \\ T_{HSP_CLK} \cdot \left( \text{floor}\left[ \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD} \right] + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD} \end{cases}$$

Display interface clock period average value.

$$\overline{T}dicp = T_{HSP_CLK} \cdot \frac{DISP3_IF_CLK_PER_WR}{HSP_CLK_PERIOD}$$

**NOTE**

HSP_CLK is the High-Speed Port Clock, which is the input to the Image Processing Unit (IPU). Its frequency is controlled by the Clock Control Module (CCM) settings. The HSP_CLK frequency must be greater than or equal to the AHB clock frequency.

The SCREEN_WIDTH, SCREEN_HEIGHT, H_SYNC_WIDTH, V_SYNC_WIDTH, BGXP, BGYP and V_SYNC_WIDTH_L parameters are programmed via the SDC_HOR_CONF, SDC_VER_CONF, SDC_BG_POS Registers. The FW and FH parameters are programmed for the corresponding DMA channel. The DISP3_IF_CLK_PER_WR, HSP_CLK_PERIOD and DISP3_IF_CLK_CNT_D parameters are programmed via the DI_DISP3_TIME_CONF, DI_HSP_CLK_PER and DI_DISP_ACC_CC Registers.

Figure 48 depicts the synchronous display interface timing for access level, and Table 47 lists the timing parameters. The DISP3_IF_CLK_DOWN_WR and DISP3_IF_CLK_UP_WR parameters are set via the DI_DISP3_TIME_CONF Register.

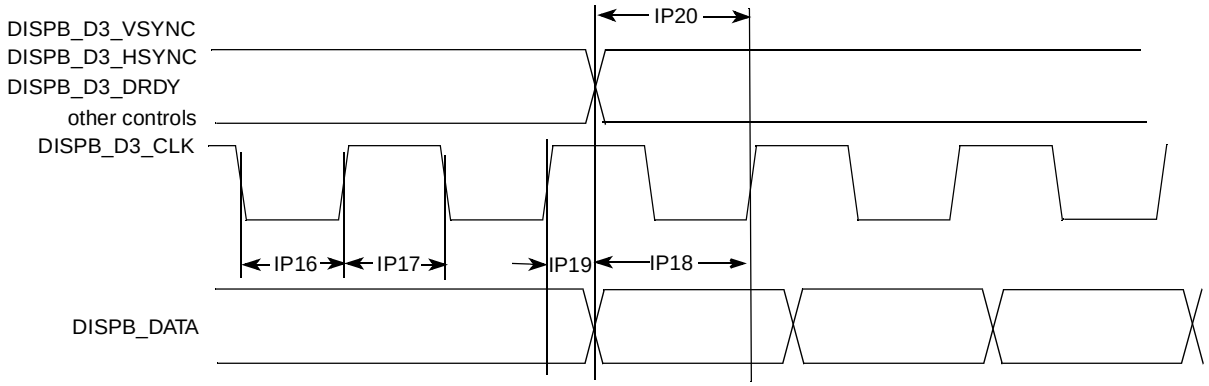



**Figure 48. Synchronous Display Interface Timing Diagram—Access Level**

**Table 47. Synchronous Display Interface Timing Parameters—Access Level**

| ID | Parameter | Symbol | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| IP16 | Display interface clock low time | Tckl | Tdicd–Tdicu–1.5 | Tdicd[2]–Tdicu[3] | Tdicd–Tdicu+1.5 | ns |
| IP17 | Display interface clock high time | Tckh | Tdicp–Tdicd+Tdicu–1.5 | Tdicp–Tdicd+Tdicu | Tdicp–Tdicd+Tdicu+1.5 | ns |
| IP18 | Data setup time | Tdsu | Tdicd–3.5 | Tdicu | — | ns |
| IP19 | Data holdup time | Tdhd | Tdicp–Tdicd–3.5 | Tdicp–Tdicu | — | ns |
| IP20 | Control signals setup time to display interface clock | Tcsu | Tdicd–3.5 | Tdicu | — | ns |

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock down time

$$Tdicd = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP3_IF_CLK_DOWN_WR}{HSP_CLK_PERIOD}\right]$$

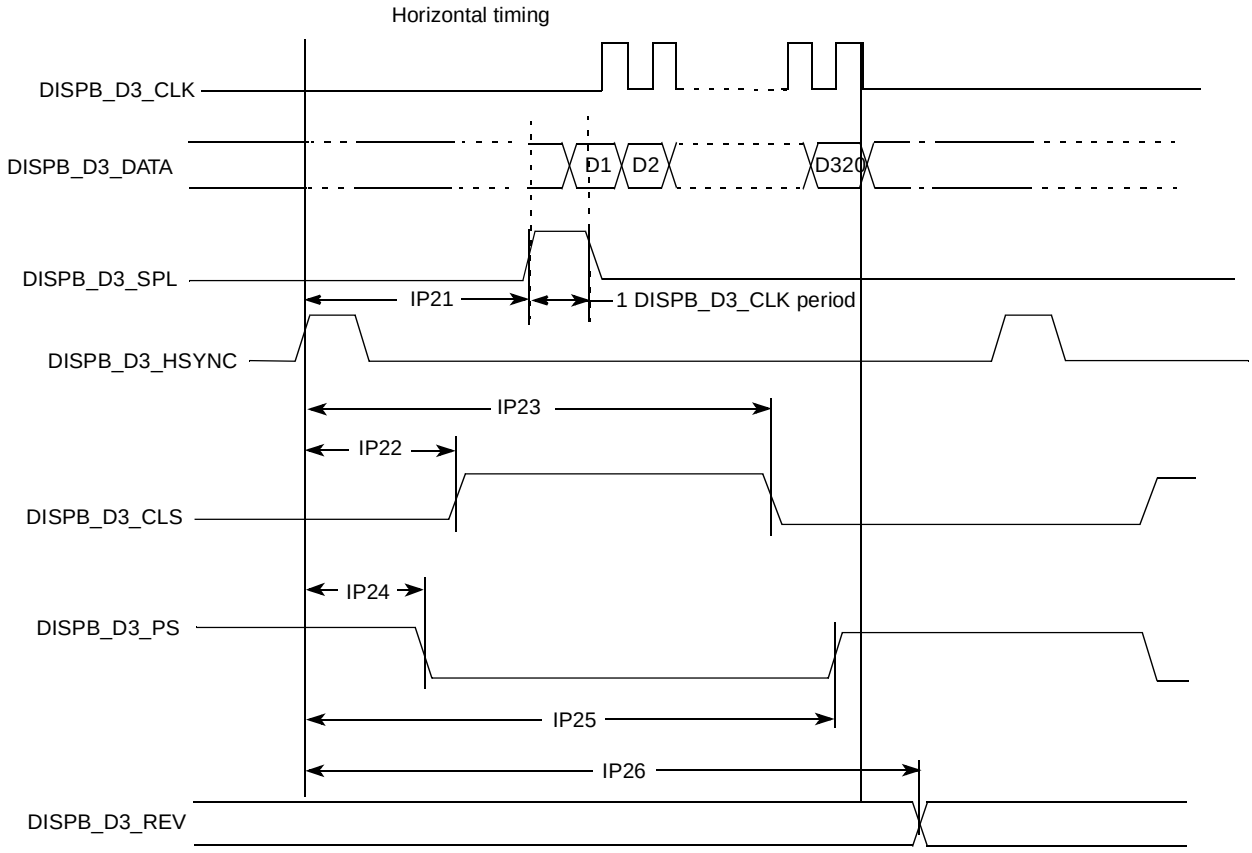
3 Display interface clock up time

$$Tdicu = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP3_IF_CLK_UP_WR}{HSP_CLK_PERIOD}\right]$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

### 4.3.15.3 Interface to Sharp HR-TFT Panels

Figure 49 depicts the Sharp HR-TFT panel interface timing, and Table 48 lists the timing parameters. The CLS_RISE_DELAY, CLS_FALL_DELAY, PS_FALL_DELAY, PS_RISE_DELAY, REV_TOGGLE_DELAY parameters are defined in the SDC_SHARP_CONF_1 and SDC_SHARP_CONF_2 registers. For other Sharp interface timing characteristics, refer to Section 4.3.15.2.2, "Interface to Active Matrix TFT LCD Panels, Electrical Characteristics." The timing images correspond to straight polarity of the Sharp signals.




Example is drawn with FW+1=320 pixel/line, FH+1=240 lines.
SPL pulse width is fixed and aligned to the first data of the line.
REV toggles every HSYNC period.

**Figure 49. Sharp HR-TFT Panel Interface Timing Diagram—Pixel Level**

**Table 48. Sharp Synchronous Display Interface Timing Parameters—Pixel Level**

| ID | Parameter | Symbol | Value | Units |
|---|---|---|---|---|
| IP21 | SPL rise time | Tsplr | (BGXP – 1) * Tdpcp | ns |
| IP22 | CLS rise time | Tclsr | CLS_RISE_DELAY * Tdpcp | ns |
| IP23 | CLS fall time | Tclsf | CLS_FALL_DELAY * Tdpcp | ns |
| IP24 | CLS rise and PS fall time | Tpsf | PS_FALL_DELAY * Tdpcp | ns |
| IP25 | PS rise time | Tpsr | PS_RISE_DELAY * Tdpcp | ns |
| IP26 | REV toggle time | Trev | REV_TOGGLE_DELAY * Tdpcp | ns |

### 4.3.15.4 Synchronous Interface to Dual-Port Smart Displays

Functionality and electrical characteristics of the synchronous interface to dual-port smart displays are identical to parameters of the synchronous interface. See Section 4.3.15.2.2, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

#### 4.3.15.4.1 Interface to a TV Encoder, Functional Description

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The bits D7–D0 of the value are mapped to bits LD17–LD10 of the data bus, respectively. Figure 50 depicts the interface timing,

- The frequency of the clock DISPB_D3_CLK is 27 MHz (within 10%).
- The DISPB_D3_HSYNC, DISPB_D3_VSYNC and DISPB_D3_DRDY signals are active low.
- The transition to the next row is marked by the negative edge of the DISPB_D3_HSYNC signal. It remains low for a single clock cycle.
- The transition to the next field/frame is marked by the negative edge of the DISPB_D3_VSYNC signal. It remains low for at least one clock cycle.
  - At a transition to an odd field (of the next frame), the negative edges of DISPB_D3_VSYNC and DISPB_D3_HSYNC coincide.
  - At a transition to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the DISPB_D3_HSYNC signal being high.

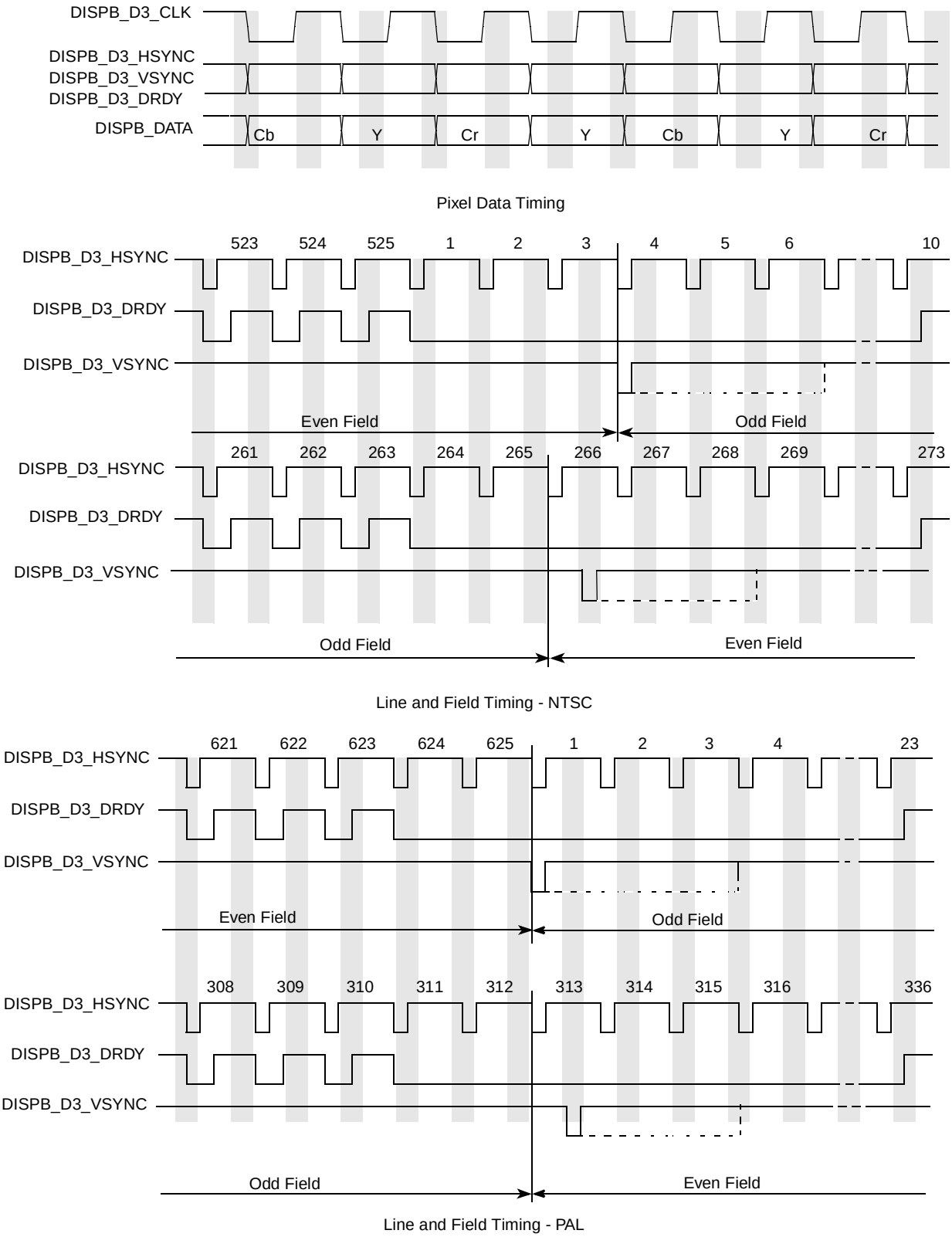



**Figure 50. TV Encoder Interface Timing Diagram**

#### 4.3.15.4.2 Interface to a TV Encoder, Electrical Characteristics

The timing characteristics of the TV encoder interface are identical to the synchronous display characteristics. See Section 4.3.15.2.2, “Interface to Active Matrix TFT LCD Panels, Electrical Characteristics.”

### 4.3.15.5 Asynchronous Interfaces

#### 4.3.15.5.1 Parallel Interfaces, Functional Description

The IPU supports the following asynchronous parallel interfaces:

- System 80 interface
  - Type 1 (sampling with the chip select signal) with and without byte enable signals.
  - Type 2 (sampling with the read and write signals) with and without byte enable signals.
- System 68k interface
  - Type 1 (sampling with the chip select signal) with or without byte enable signals.
  - Type 2 (sampling with the read and write signals) with or without byte enable signals.

For each of four system interfaces, there are three burst modes:

1. Burst mode without a separate clock. The burst length is defined by the corresponding parameters of the IDMAC (when data is transferred from the system memory) of by the HBURST signal (when the MCU directly accesses the display via the slave AHB bus). For system 80 and system 68k type 1 interfaces, data is sampled by the CS signal and other control signals changes only when transfer direction is changed during the burst. For type 2 interfaces, data is sampled by the WR/RD signals (system 80) or by the ENABLE signal (system 68k) and the CS signal stays active during the whole burst.
2. Burst mode with the separate clock DISPB_BCLK. In this mode, data is sampled with the DISPB_BCLK clock. The CS signal stays active during whole burst transfer. Other controls are changed simultaneously with data when the bus state (read, write or wait) is altered. The CS signals and other controls move to non-active state after burst has been completed.
3. Single access mode. In this mode, slave AHB and DMA burst are broken to single accesses. The data is sampled with CS or other controls according the interface type as described above. All controls (including CS) become non-active for one display interface clock after each access. This mode corresponds to the ATI single access mode.

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 51, Figure 52, Figure 53, and Figure 54. These timing images correspond to active-low DISPB_D#_CS, DISPB_D#_WR and DISPB_D#_RD signals.

Additionally, the IPU allows a programmable pause between two burst. The pause is defined in the HSP_CLK cycles. It allows to avoid timing violation between two sequential bursts or two accesses to different displays. The range of this pause is from 4 to 19 HSP_CLK cycles.

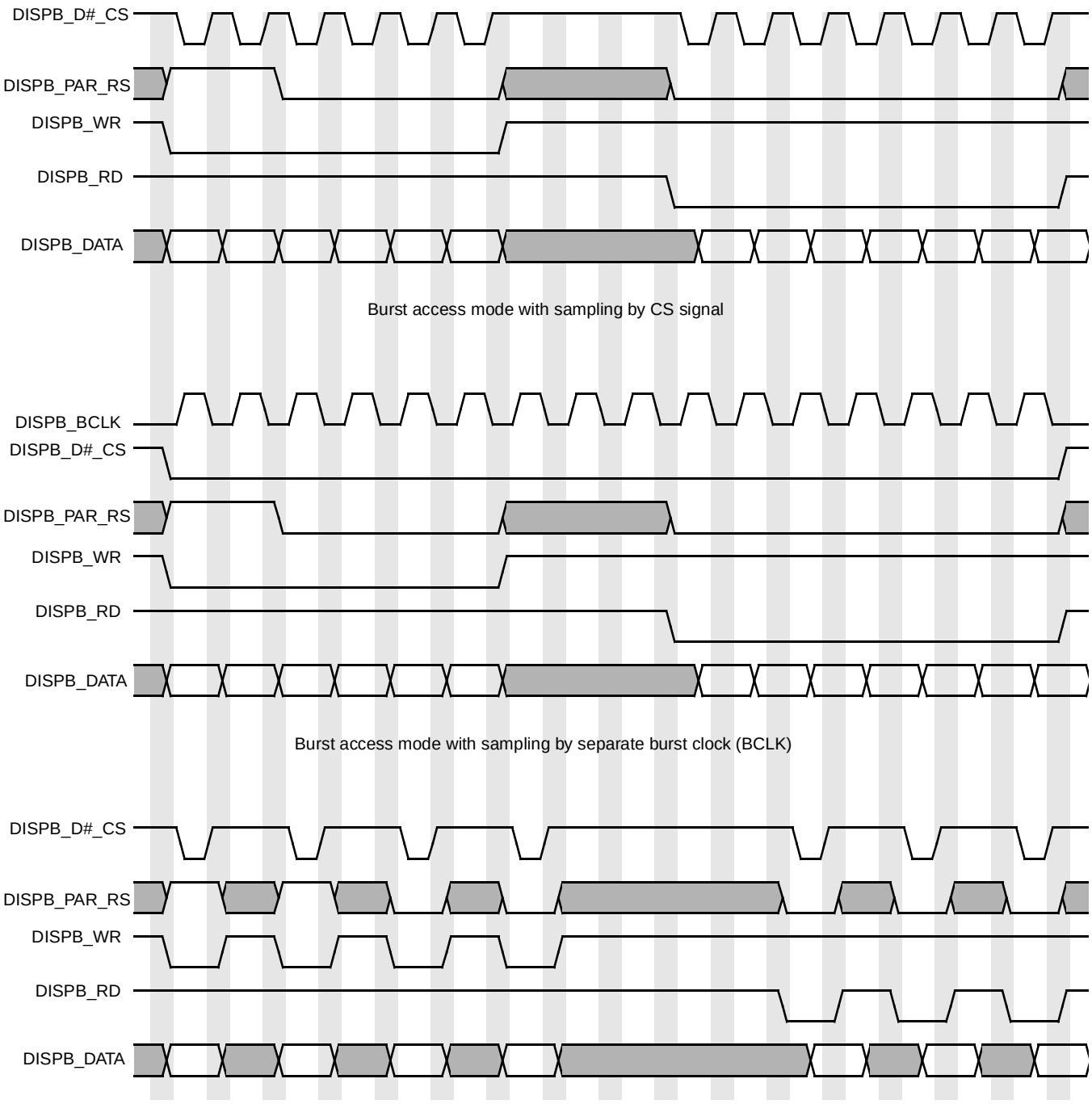



**Figure 51. Asynchronous Parallel System 80 Interface (Type 1) Burst Mode Timing Diagram**

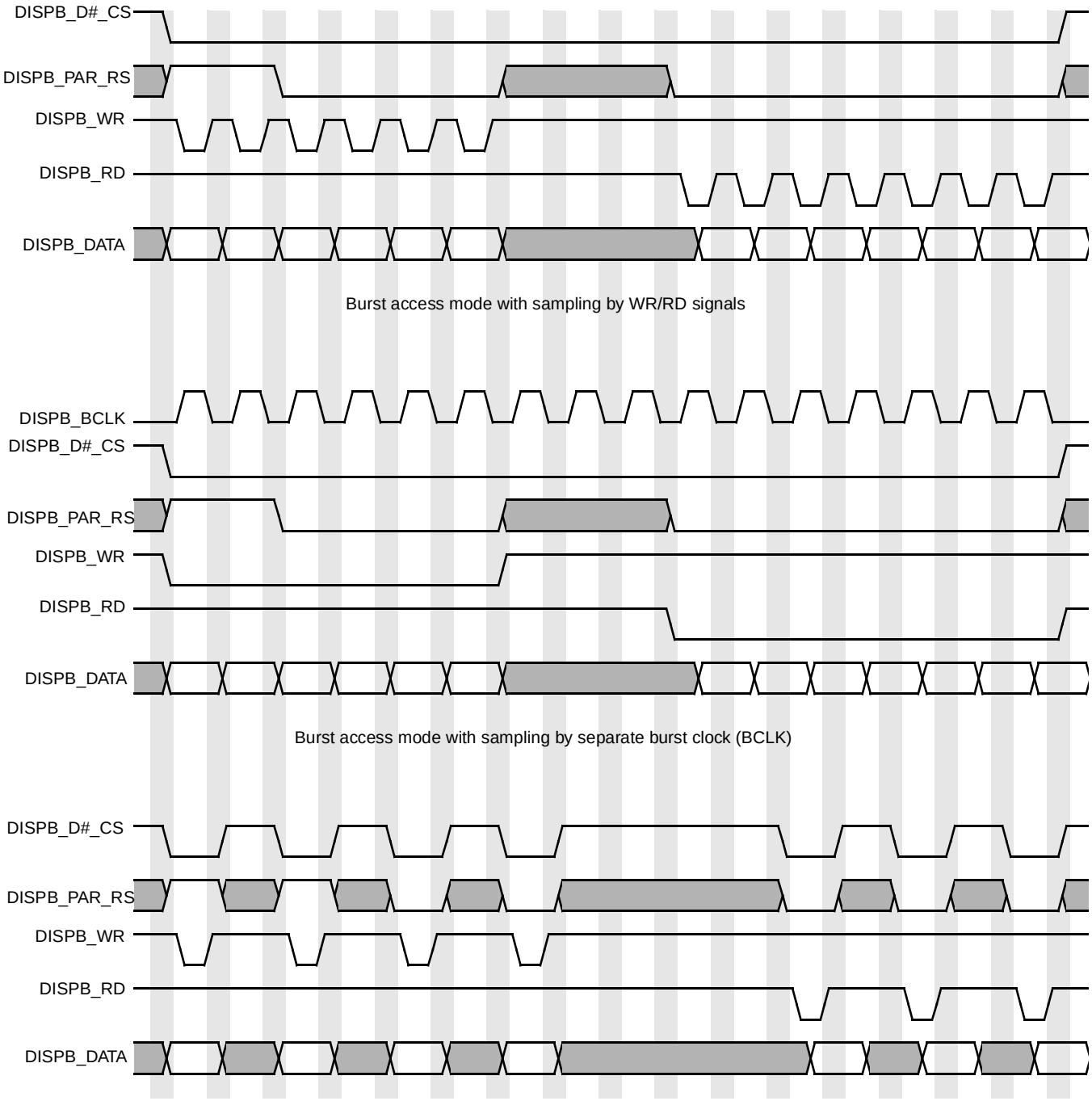
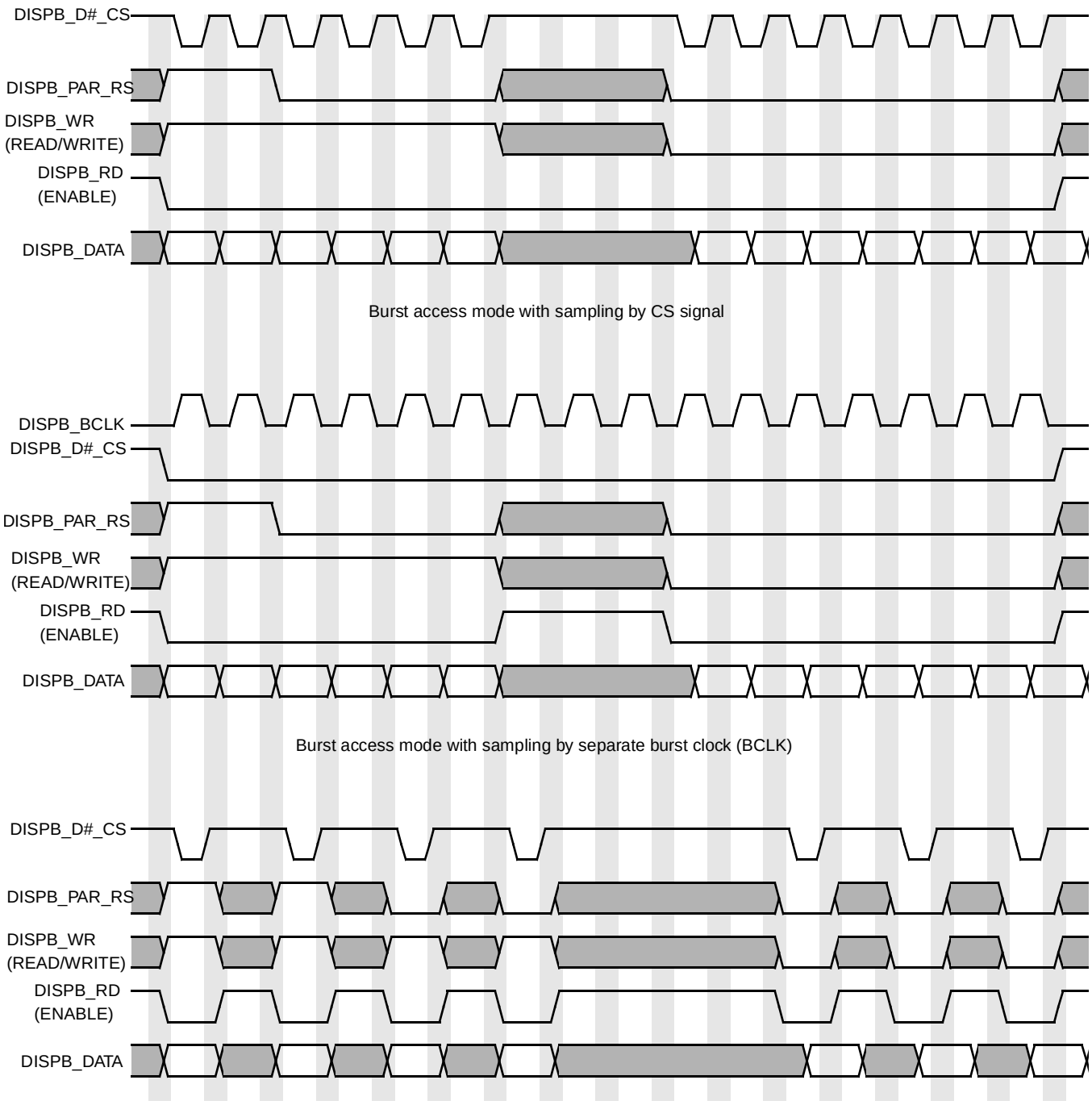



**Figure 52. Asynchronous Parallel System 80 Interface (Type 2) Burst Mode Timing Diagram**




Single access mode (all control signals are not active for one display interface clock after each display access)

**Figure 53. Asynchronous Parallel System 68k Interface (Type 1) Burst Mode Timing Diagram**

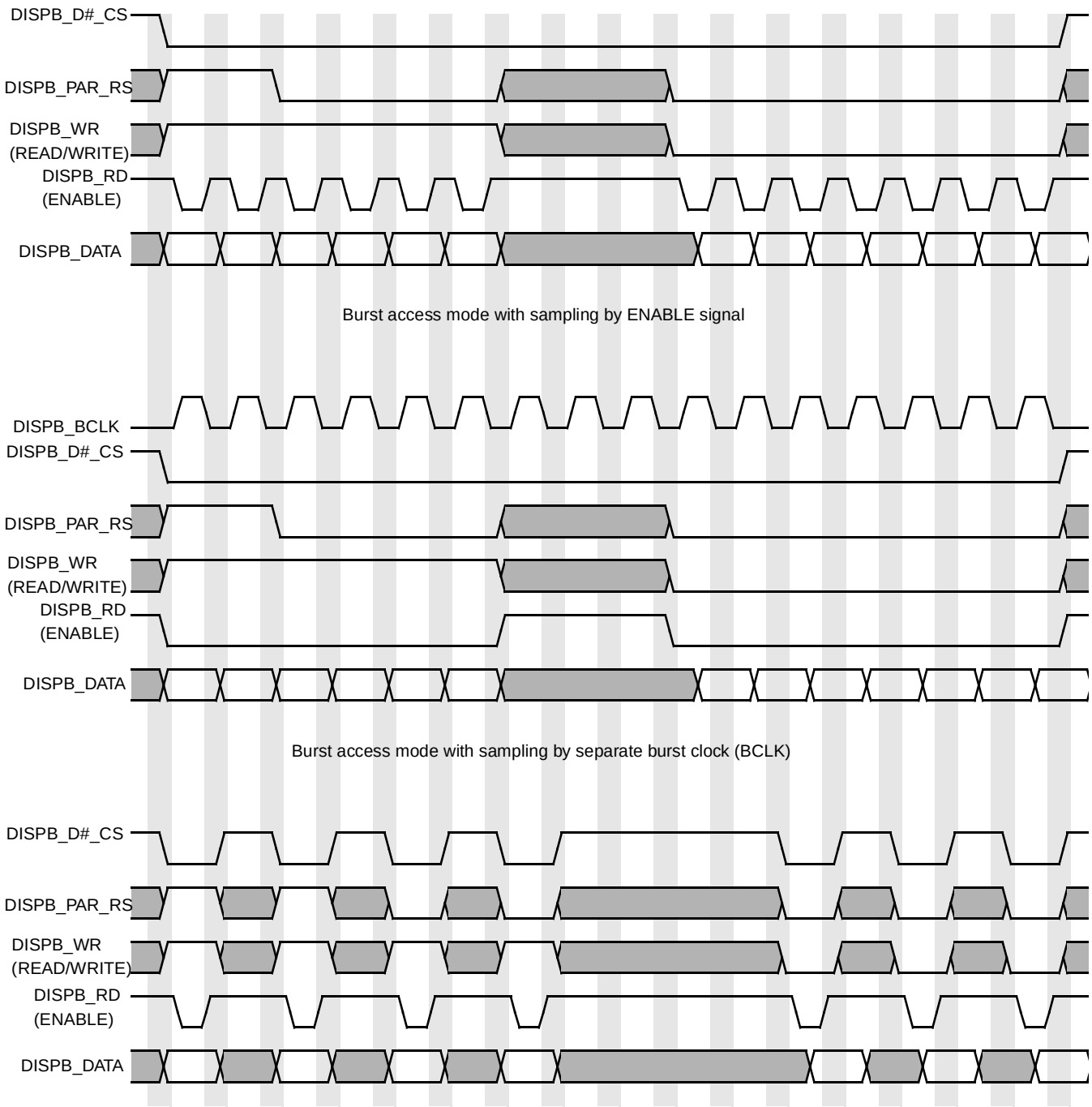



**Figure 54. Asynchronous Parallel System 68k Interface (Type 2) Burst Mode TIming Diagram**

Display read operation can be performed with wait states when each read access takes up to four display interface clock cycles according to the DISP0_RD_WAIT_ST parameter in the DI_DISP0_TIME_CONF_3, DI_DISP1_TIME_CONF_3, DI_DISP2_TIME_CONF_3 Registers. Figure 55 shows timing of the parallel interface with read wait states.

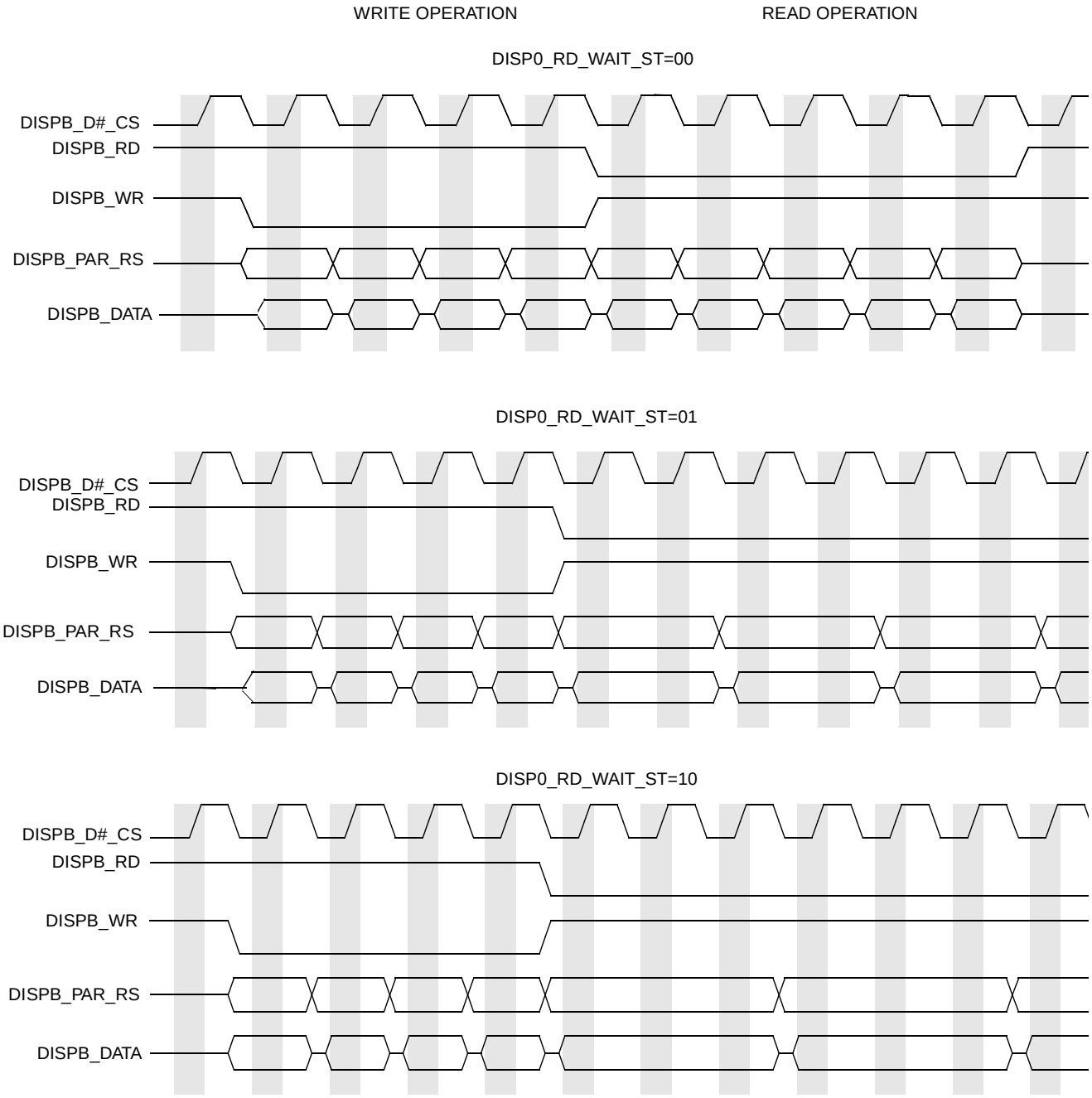



**Figure 55. Parallel Interface Timing Diagram—Read Wait States**

### 4.3.15.5.2 Parallel Interfaces, Electrical Characteristics

Figure 56, Figure 58, Figure 57, and Figure 59 depict timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 49 lists the timing parameters at display access level. All timing images are based on active low control signals (signals polarity is controlled via the DI_DISP_SIG_POL Register).

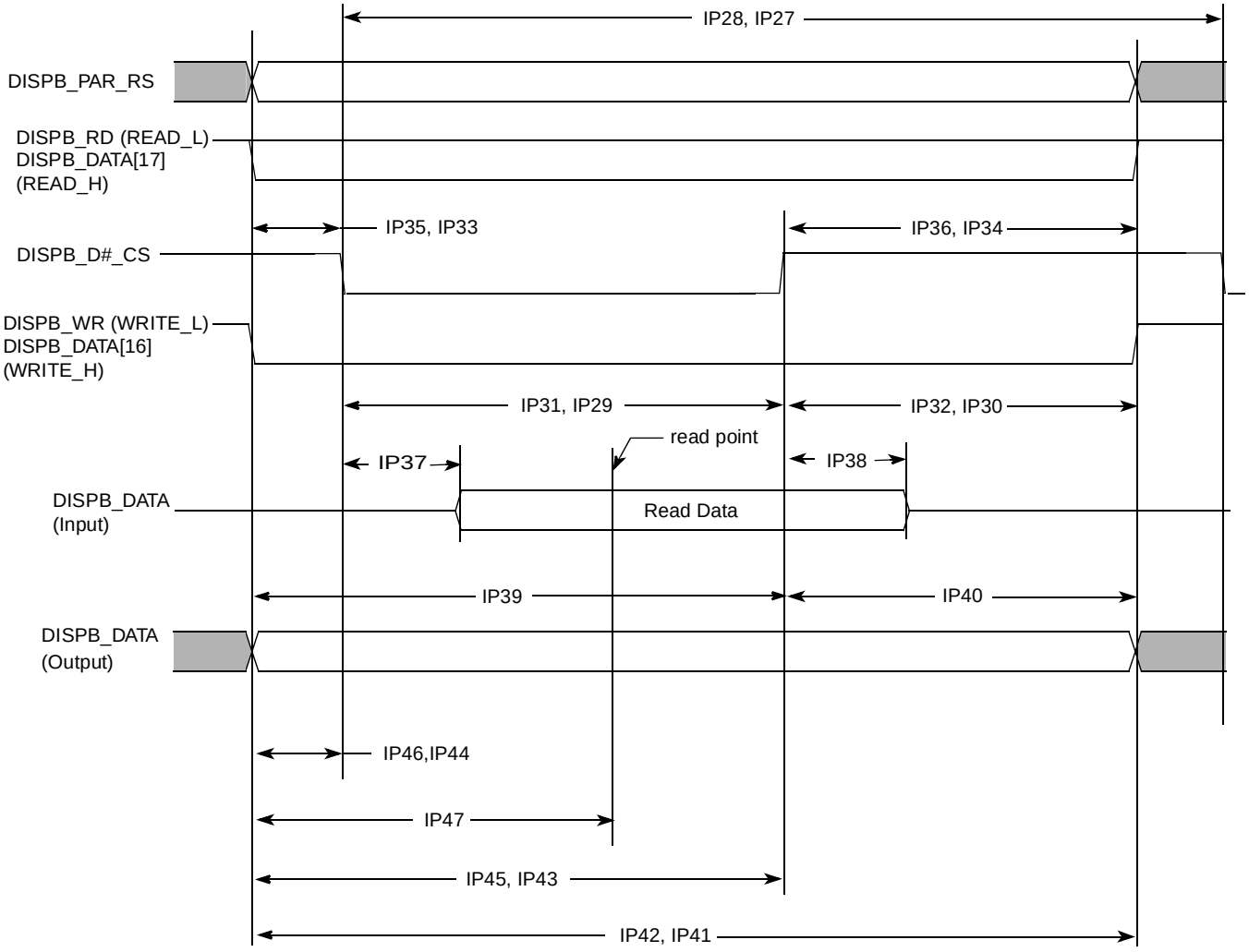



**Figure 56. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram**

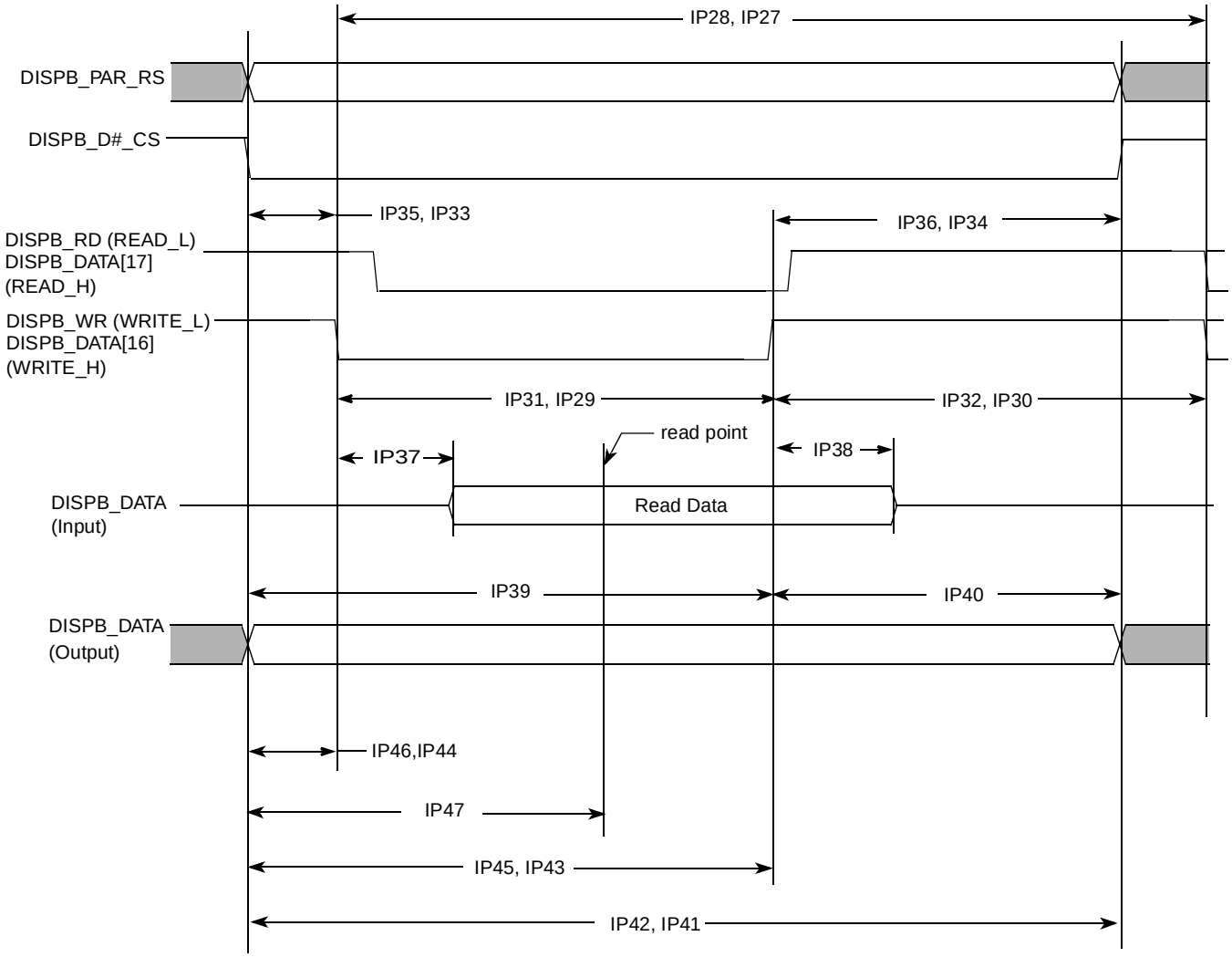



**Figure 57. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram**

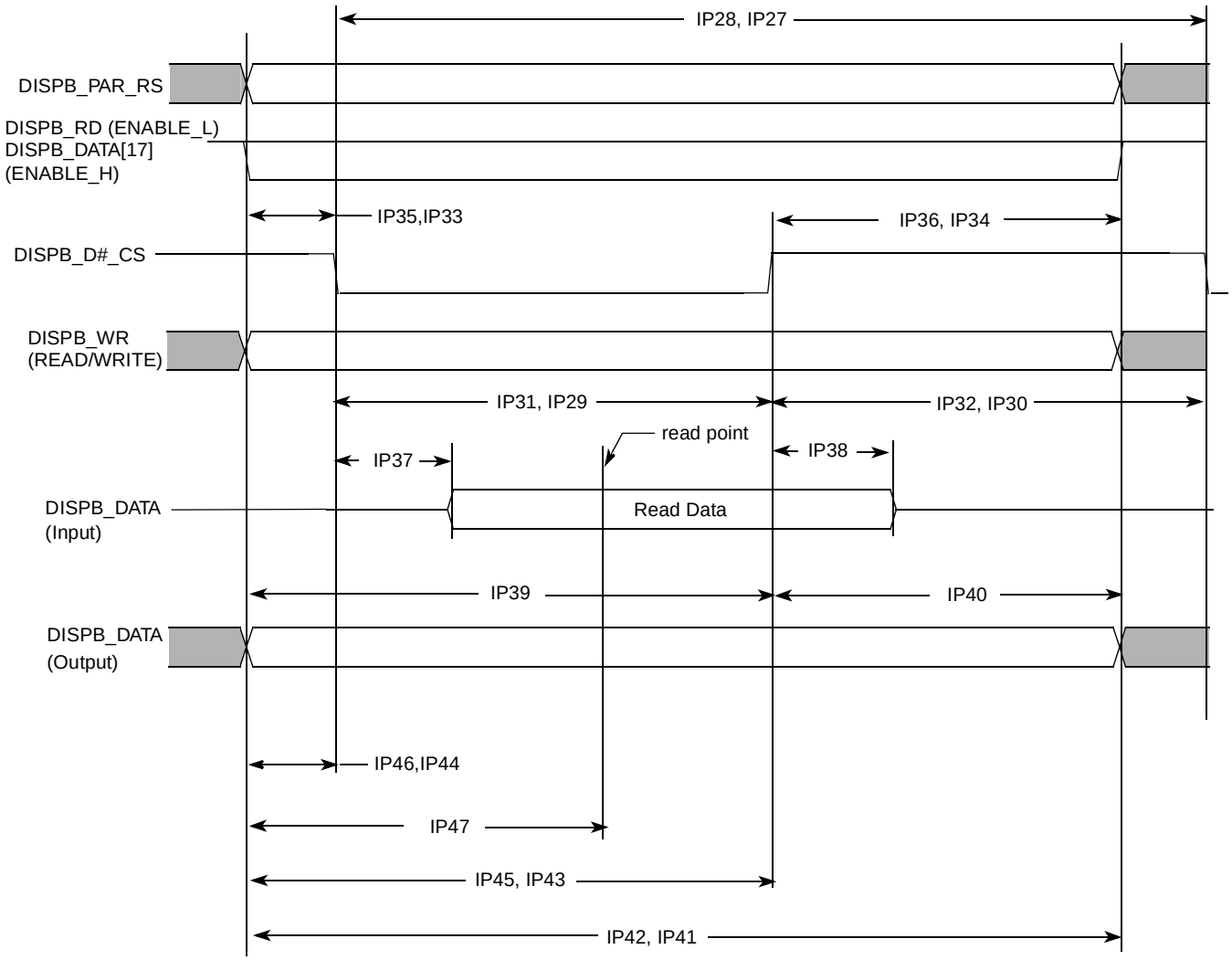



**Figure 58. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram**

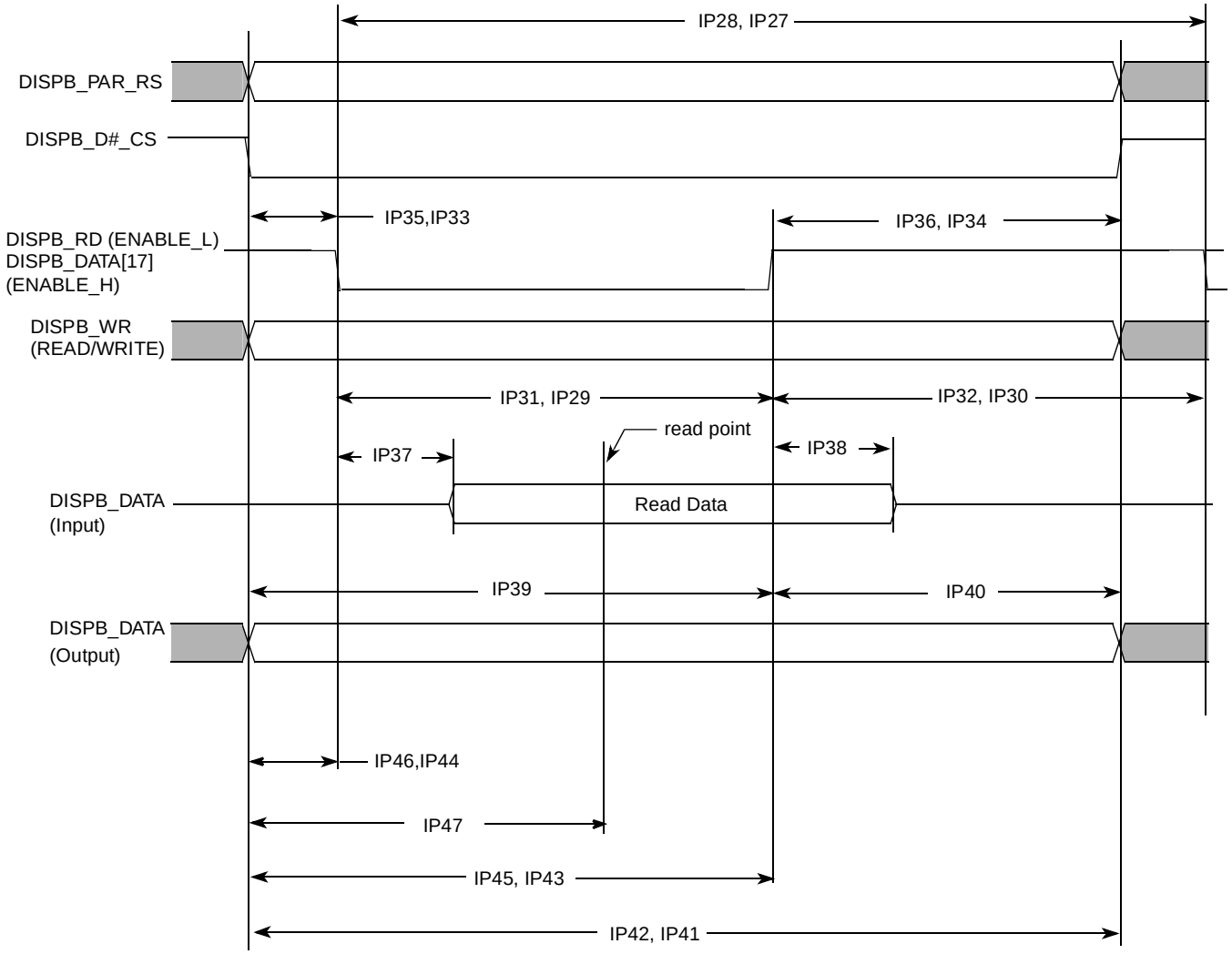



**Figure 59. Asynchronous Parallel System 68k Interface (Type 2) Timing Diagram**

**Table 49. Asynchronous Parallel Interface Timing Parameters—Access Level**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP27 | Read system cycle time | Tcycr | Tdicpr–1.5 | Tdicpr[2] | Tdicpr+1.5 | ns |
| IP28 | Write system cycle time | Tcycw | Tdicpw–1.5 | Tdicpw[3] | Tdicpw+1.5 | ns |
| IP29 | Read low pulse width | Trl | Tdicdr–Tdicur–1.5 | Tdicdr[4]–Tdicur[5] | Tdicdr–Tdicur+1.5 | ns |
| IP30 | Read high pulse width | Trh | Tdicpr–Tdicdr+Tdicur–1.5 | Tdicpr–Tdicdr+ Tdicur | Tdicpr–Tdicdr+Tdicur+1.5 | ns |
| IP31 | Write low pulse width | Twl | Tdicdw–Tdicuw–1.5 | Tdicdw[6]–Tdicuw[7] | Tdicdw–Tdicuw+1.5 | ns |
| IP32 | Write high pulse width | Twh | Tdicpw–Tdicdw+ Tdicuw–1.5 | Tdicpw–Tdicdw+ Tdicuw | Tdicpw–Tdicdw+ Tdicuw+1.5 | ns |
| IP33 | Controls setup time for read | Tdcsr | Tdicur–1.5 | Tdicur | — | ns |
| IP34 | Controls hold time for read | Tdchr | Tdicpr–Tdicdr–1.5 | Tdicpr–Tdicdr | — | ns |
| IP35 | Controls setup time for write | Tdcsw | Tdicuw–1.5 | Tdicuw | — | ns |

**Table 49. Asynchronous Parallel Interface Timing Parameters—Access Level (continued)**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP36 | Controls hold time for write | Tdchw | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP37 | Slave device data delay[8] | Tracc | 0 | — | Tdrp[9]–Tlbd[10]–Tdicur–1.5 | ns |
| IP38 | Slave device data hold time[8] | Troh | Tdrp–Tlbd–Tdicdr+1.5 | — | Tdicpr–Tdicdr–1.5 | ns |
| IP39 | Write data setup time | Tds | Tdicdw–1.5 | Tdicdw | — | ns |
| IP40 | Write data hold time | Tdh | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP41 | Read period[2] | Tdicpr | Tdicpr–1.5 | Tdicpr | Tdicpr+1.5 | ns |
| IP42 | Write period[3] | Tdicpw | Tdicpw–1.5 | Tdicpw | Tdicpw+1.5 | ns |
| IP43 | Read down time[4] | Tdicdr | Tdicdr–1.5 | Tdicdr | Tdicdr+1.5 | ns |
| IP44 | Read up time[5] | Tdicur | Tdicur–1.5 | Tdicur | Tdicur+1.5 | ns |
| IP45 | Write down time[6] | Tdicdw | Tdicdw–1.5 | Tdicdw | Tdicdw+1.5 | ns |
| IP46 | Write up time[7] | Tdicuw | Tdicuw–1.5 | Tdicuw | Tdicuw+1.5 | ns |
| IP47 | Read time point[9] | Tdrp | Tdrp–1.5 | Tdrp | Tdrp+1.5 | ns |

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

[2] Display interface clock period value for read:

$$Tdicpr = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_IF_CLK_PER_RD}{HSP_CLK_PERIOD}\right]$$

[3] Display interface clock period value for write:

$$Tdicpw = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_IF_CLK_PER_WR}{HSP_CLK_PERIOD}\right]$$

[4] Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_RD}{HSP_CLK_PERIOD}\right]$$

[5] Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_UP_RD}{HSP_CLK_PERIOD}\right]$$

[6] Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_WR}{HSP_CLK_PERIOD}\right]$$

[7] Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_UP_WR}{HSP_CLK_PERIOD}\right]$$

[8] This parameter is a requirement to the display connected to the IPU

[9] Data read point

$$Tdrp = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_READ_EN}{HSP_CLK_PERIOD}\right]$$

[10] Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

#### 4.3.15.5.3 Serial Interfaces, Functional Description

The IPU supports the following types of asynchronous serial interfaces:

- 3-wire (with bidirectional data line)
- 4-wire (with separate data input and output lines)
- 5-wire type 1 (with sampling RS by the serial clock)
- 5-wire type 2 (with sampling RS by the chip select signal)

Figure 60 depicts timing of the 3-wire serial interface. The timing images correspond to active-low DISPB_D#_CS signal and the straight polarity of the DISPB_SD_D_CLK signal.

For this interface, a bidirectional data line is used outside the device. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

Each data transfer can be preceded by an optional preamble with programmable length and contents. The preamble is followed by read/write (RW) and address (RS) bits. The order of the these bits is programmable. The RW bit can be disabled. The following data can consist of one word or of a whole burst. The interface parameters are controlled by the DI_SER_DISP1_CONF and DI_SER_DISP2_CONF Registers.

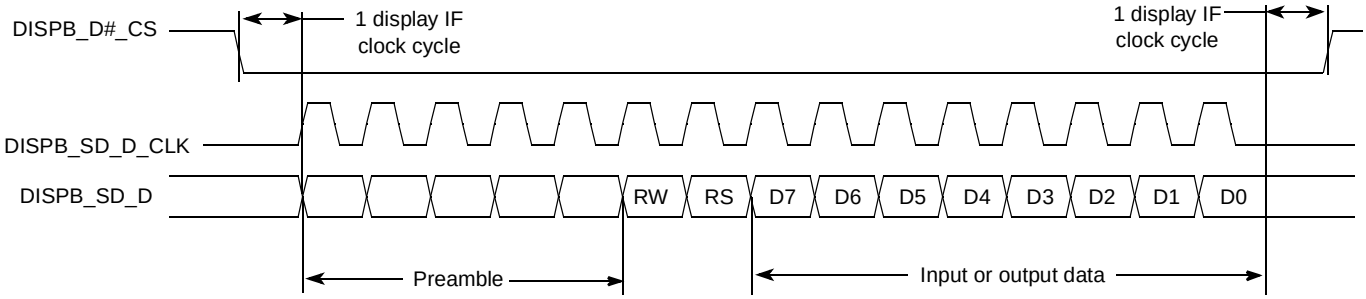



**Figure 60. 3-Wire Serial Interface Timing Diagram**

Figure 61 depicts timing of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the device.

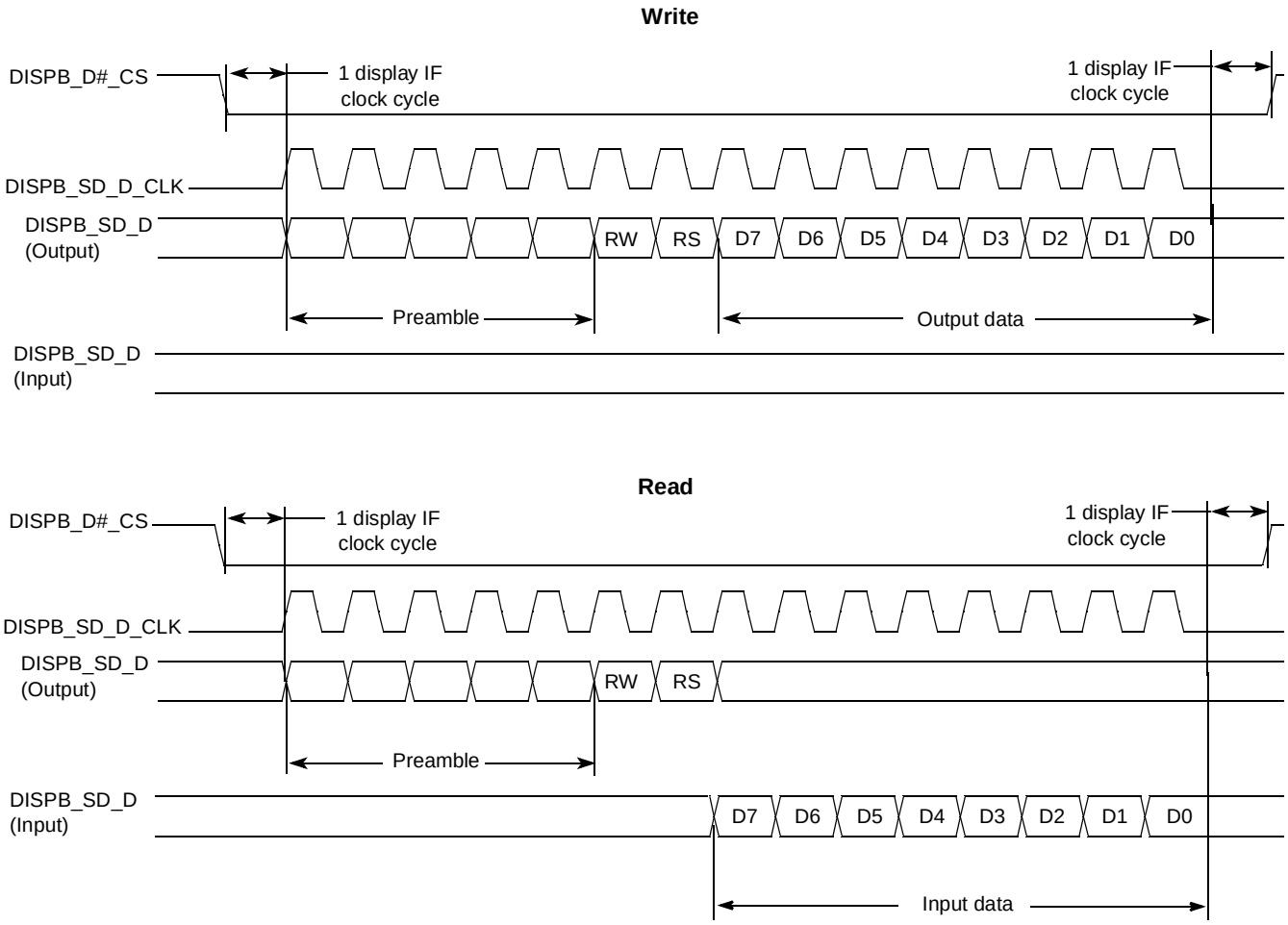



**Figure 61. 4-Wire Serial Interface Timing Diagram**

Figure 62 depicts timing of the 5-wire serial interface (Type 1). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

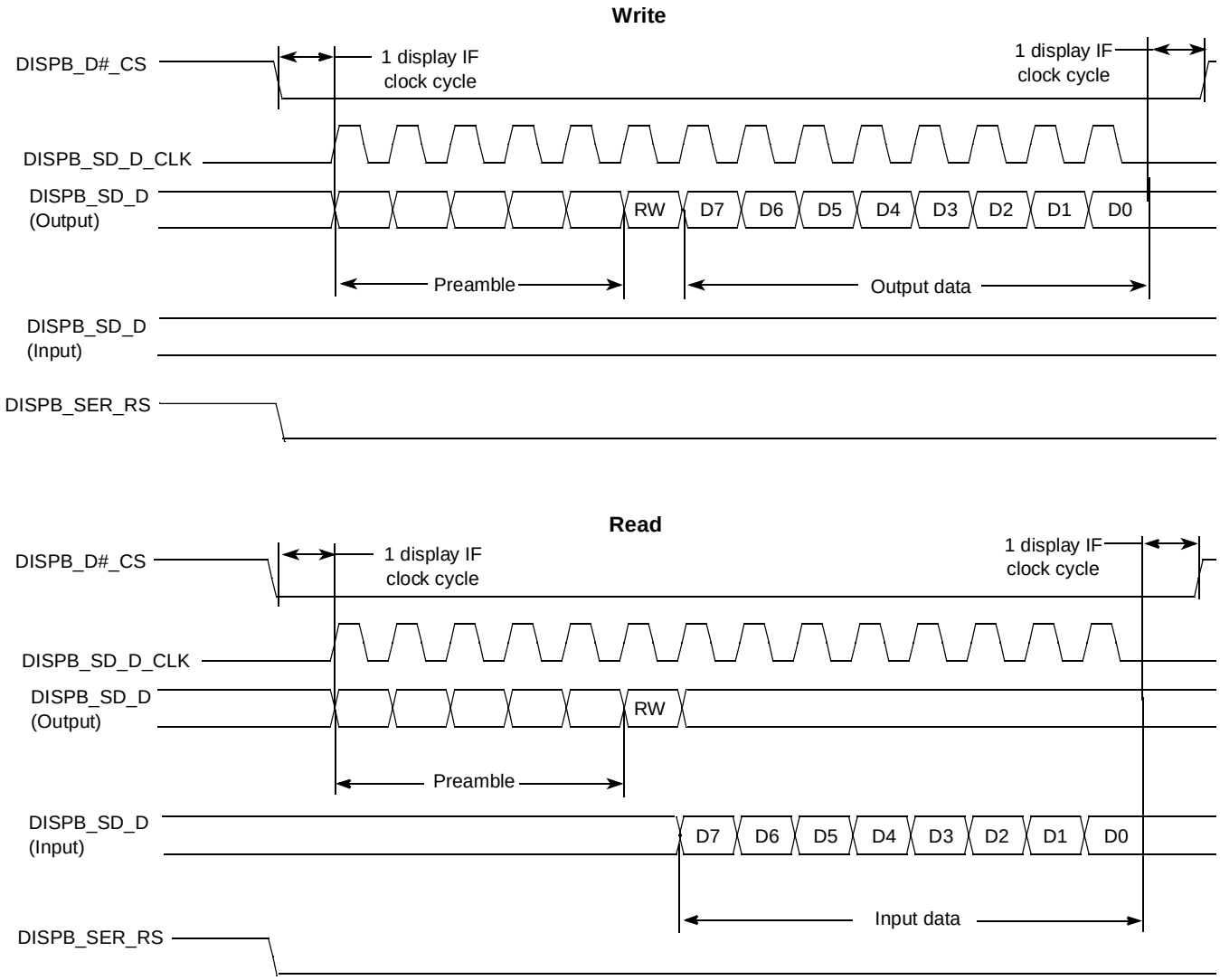



**Figure 62. 5-Wire Serial Interface (Type 1) Timing Diagram**

Figure 63 depicts timing of the 5-wire serial interface (Type 2). For this interface, a separate RS line is added. When a burst is transmitted within single active chip select interval, the RS can be changed at boundaries of words.

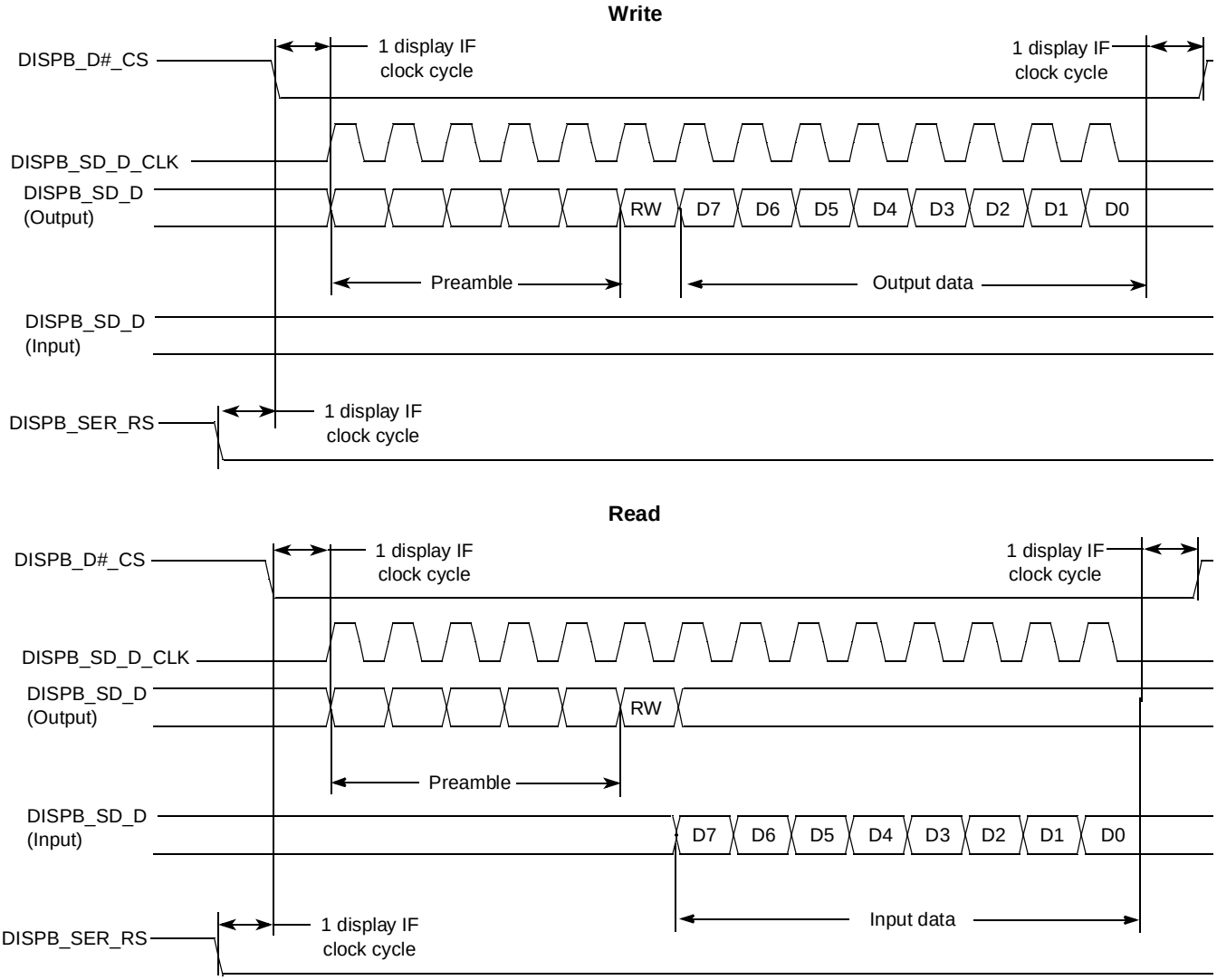



**Figure 63. 5-Wire Serial Interface (Type 2) Timing Diagram**

### 4.3.15.5.4 Serial Interfaces, Electrical Characteristics

Figure 64 depicts timing of the serial interface. Table 50 lists the timing parameters at display access level.

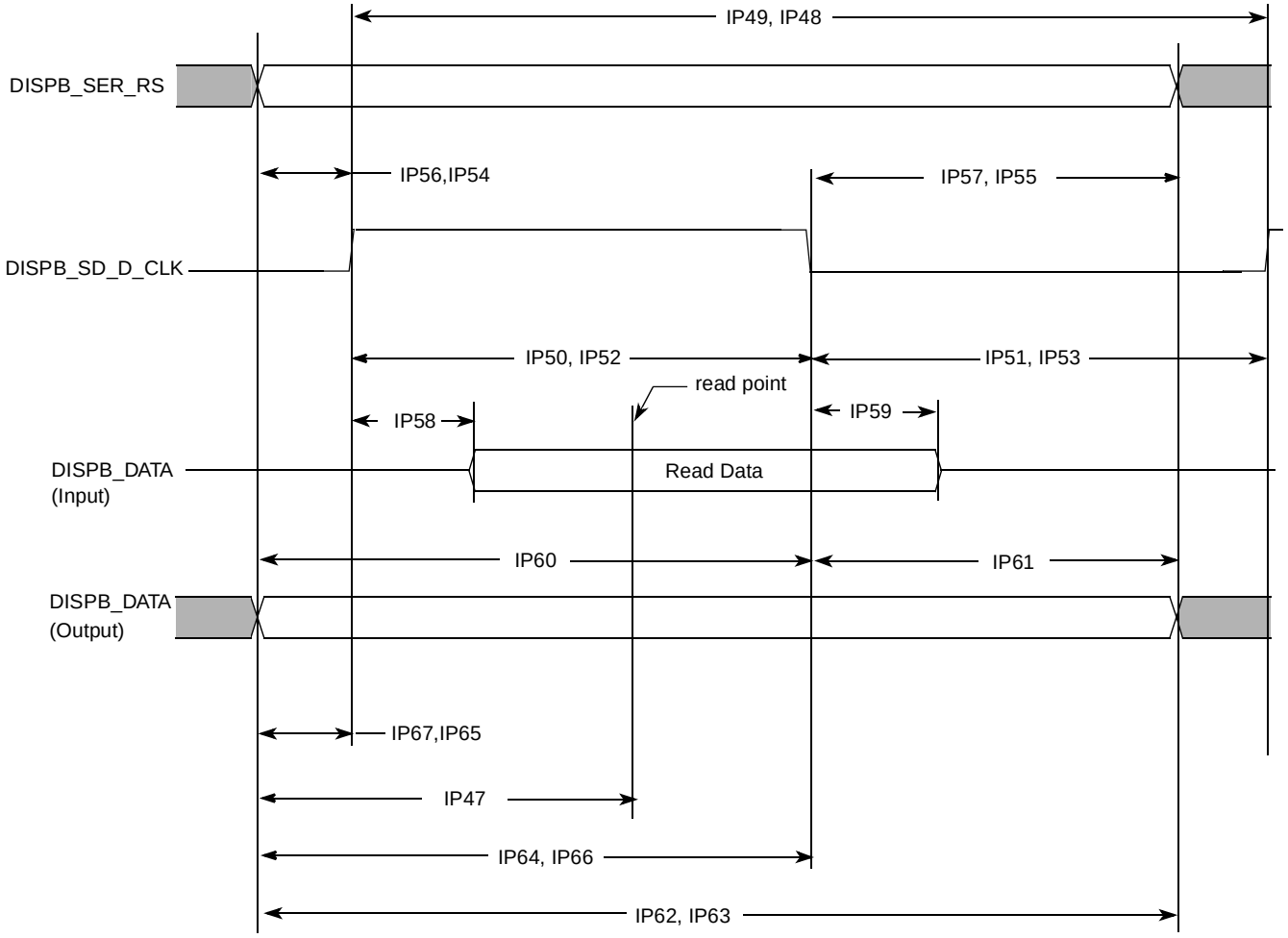



**Figure 64. Asynchronous Serial Interface Timing Diagram**

**Table 50. Asynchronous Serial Interface Timing Parameters—Access Level**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP48 | Read system cycle time | Tcycr | Tdicpr–1.5 | Tdicpr[2] | Tdicpr+1.5 | ns |
| IP49 | Write system cycle time | Tcycw | Tdicpw–1.5 | Tdicpw[3] | Tdicpw+1.5 | ns |
| IP50 | Read clock low pulse width | Trl | Tdicdr–Tdicur–1.5 | Tdicdr[4]–Tdicur[5] | Tdicdr–Tdicur+1.5 | ns |
| IP51 | Read clock high pulse width | Trh | Tdicpr–Tdicdr+Tdicur–1.5 | Tdicpr–Tdicdr+ Tdicur | Tdicpr–Tdicdr+Tdicur+1.5 | ns |
| IP52 | Write clock low pulse width | Twl | Tdicdw–Tdicuw–1.5 | Tdicdw[6]–Tdicuw[7] | Tdicdw–Tdicuw+1.5 | ns |
| IP53 | Write clock high pulse width | Twh | Tdicpw–Tdicdw+ Tdicuw–1.5 | Tdicpw–Tdicdw+ Tdicuw | Tdicpw–Tdicdw+ Tdicuw+1.5 | ns |
| IP54 | Controls setup time for read | Tdcsr | Tdicur–1.5 | Tdicur | — | ns |
| IP55 | Controls hold time for read | Tdchr | Tdicpr–Tdicdr–1.5 | Tdicpr–Tdicdr | — | ns |

**Table 50. Asynchronous Serial Interface Timing Parameters—Access Level (continued)**

| ID | Parameter | Symbol | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| IP56 | Controls setup time for write | Tdcsw | Tdicuw–1.5 | Tdicuw | — | ns |
| IP57 | Controls hold time for write | Tdchw | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP58 | Slave device data delay[8] | Tracc | 0 | — | Tdrp[9]–Tlbd[10]–Tdicur–1.5 | ns |
| IP59 | Slave device data hold time[8] | Troh | Tdrp–Tlbd–Tdicdr+1.5 | — | Tdicpr–Tdicdr–1.5 | ns |
| IP60 | Write data setup time | Tds | Tdicdw–1.5 | Tdicdw | — | ns |
| IP61 | Write data hold time | Tdh | Tdicpw–Tdicdw–1.5 | Tdicpw–Tdicdw | — | ns |
| IP62 | Read period[2] | Tdicpr | Tdicpr–1.5 | Tdicpr | Tdicpr+1.5 | ns |
| IP63 | Write period[3] | Tdicpw | Tdicpw–1.5 | Tdicpw | Tdicpw+1.5 | ns |
| IP64 | Read down time[4] | Tdicdr | Tdicdr–1.5 | Tdicdr | Tdicdr+1.5 | ns |
| IP65 | Read up time[5] | Tdicur | Tdicur–1.5 | Tdicur | Tdicur+1.5 | ns |
| IP66 | Write down time[6] | Tdicdw | Tdicdw–1.5 | Tdicdw | Tdicdw+1.5 | ns |
| IP67 | Write up time[7] | Tdicuw | Tdicuw–1.5 | Tdicuw | Tdicuw+1.5 | ns |
| IP68 | Read time point[9] | Tdrp | Tdrp–1.5 | Tdrp | Tdrp+1.5 | ns |

1 The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be device specific.

2 Display interface clock period value for read:

$$Tdicpr = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_IF_CLK_PER_RD}{HSP_CLK_PERIOD}\right]$$

3 Display interface clock period value for write:

$$Tdicpw = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_IF_CLK_PER_WR}{HSP_CLK_PERIOD}\right]$$

4 Display interface clock down time for read:

$$Tdicdr = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_RD}{HSP_CLK_PERIOD}\right]$$

5 Display interface clock up time for read:

$$Tdicur = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_UP_RD}{HSP_CLK_PERIOD}\right]$$

6 Display interface clock down time for write:

$$Tdicdw = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_DOWN_WR}{HSP_CLK_PERIOD}\right]$$

7 Display interface clock up time for write:

$$Tdicuw = \frac{1}{2}T_{HSP_CLK} \cdot ceil\left[\frac{2 \cdot DISP\#_IF_CLK_UP_WR}{HSP_CLK_PERIOD}\right]$$

8 This parameter is a requirement to the display connected to the IPU.

9 Data read point:

$$Tdrp = T_{HSP_CLK} \cdot ceil\left[\frac{DISP\#_READ_EN}{HSP_CLK_PERIOD}\right]$$

10 Loopback delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a device-level output delay, board delays, a device-level input delay, an IPU input delay. This value is device specific.

The DISP#_IF_CLK_PER_WR, DISP#_IF_CLK_PER_RD, HSP_CLK_PERIOD, DISP#_IF_CLK_DOWN_WR, DISP#_IF_CLK_UP_WR, DISP#_IF_CLK_DOWN_RD, DISP#_IF_CLK_UP_RD and DISP#_READ_EN parameters are programmed via the DI_DISP#_TIME_CONF_1, DI_DISP#_TIME_CONF_2 and DI_HSP_CLK_PER Registers.

## 4.3.16 Memory Stick Host Controller (MSHC)

Figure 65, Figure 66, and Figure 67 depict the MSHC timings, and Table 51 and Table 52 list the timing parameters.

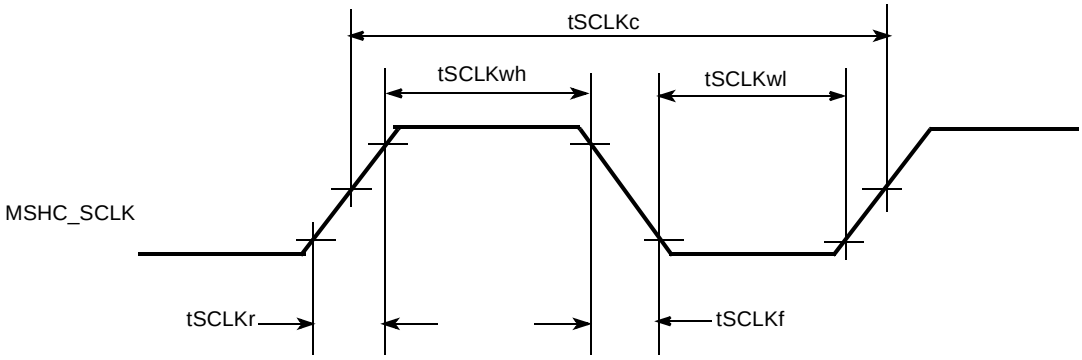



**Figure 65. MSHC_CLK Timing Diagram**

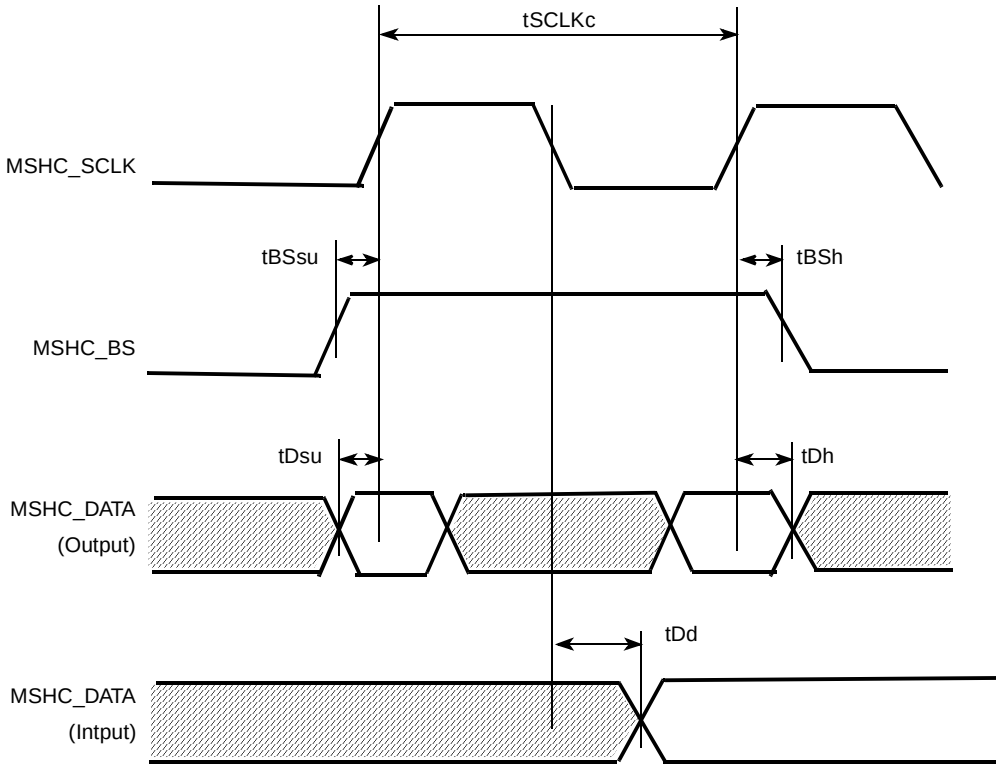



**Figure 66. Transfer Operation Timing Diagram (Serial)**

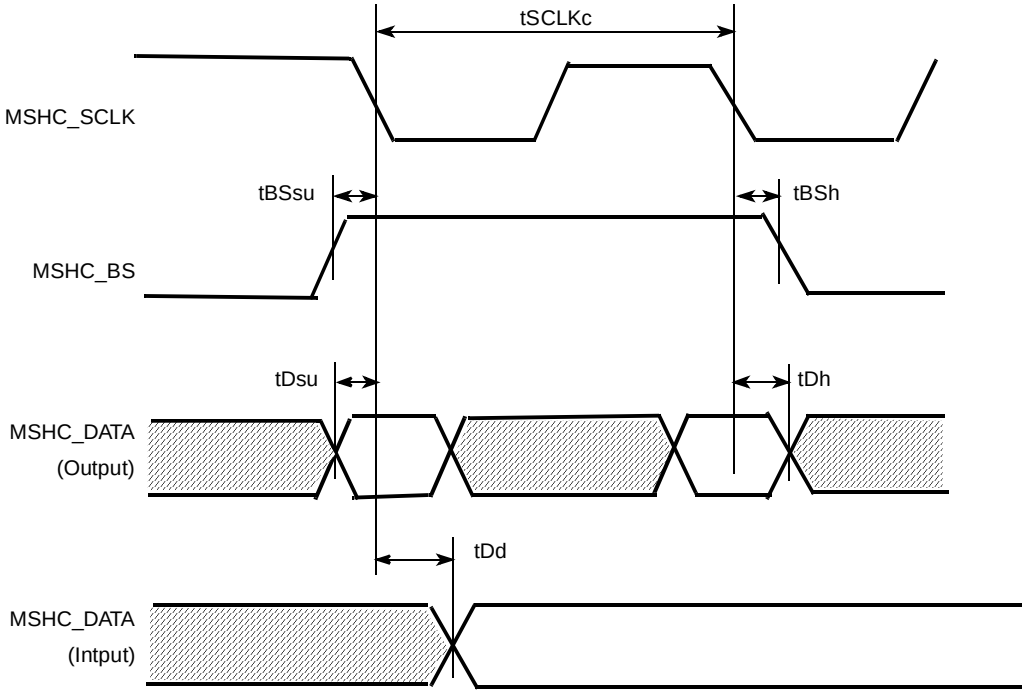



**Figure 67. Transfer Operation Timing Diagram (Parallel)**

## NOTE

The Memory Stick Host Controller is designed to meet the timing requirements per Sony's *Memory Stick Pro Format Specifications* document. Tables in this section details the specifications requirements for parallel and serial modes, and not the MCIMX31 timing.

**Table 51. Serial Interface Timing Parameters[1]**

| Signal | Parameter | Symbol | Standards | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| MSHC_SCLK | Cycle | tSCLKc | 50 | — | ns |
| | H pulse length | tSCLKwh | 15 | — | ns |
| | L pulse length | tSCLKwl | 15 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 5 | — | ns |
| | Hold time | tBSh | 5 | — | ns |
| MSHC_DATA | Setup time | tDsu | 5 | — | ns |
| | Hold time | tDh | 5 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

**Table 52. Parallel Interface Timing Parameters[1]**

| Signal | Parameter | Symbol | Standards | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| MSHC_SCLK | Cycle | tSCLKc | 25 | — | ns |
| | H pulse length | tSCLKwh | 5 | — | ns |
| | L pulse length | tSCLKwl | 5 | — | ns |
| | Rise time | tSCLKr | — | 10 | ns |
| | Fall time | tSCLKf | — | 10 | ns |
| MSHC_BS | Setup time | tBSsu | 8 | — | ns |
| | Hold time | tBSh | 1 | — | ns |
| MSHC_DATA | Setup time | tDsu | 8 | — | ns |
| | Hold time | tDh | 1 | — | ns |
| | Output delay time | tDd | — | 15 | ns |

1 Timing is guaranteed for NVCC from 2.7 through 3.1 V and up to a maximum overdrive NVCC of 3.3 V. See NVCC restrictions described in Table 8, "Operating Ranges," on page 13.

## 4.3.17 Personal Computer Memory Card International Association (PCMCIA)

Figure 68 and Figure 69 depict the timings pertaining to the PCMCIA module, each of which is an example of one clock of strobe set-up time and one clock of strobe hold time. Table 53 lists the timing parameters.

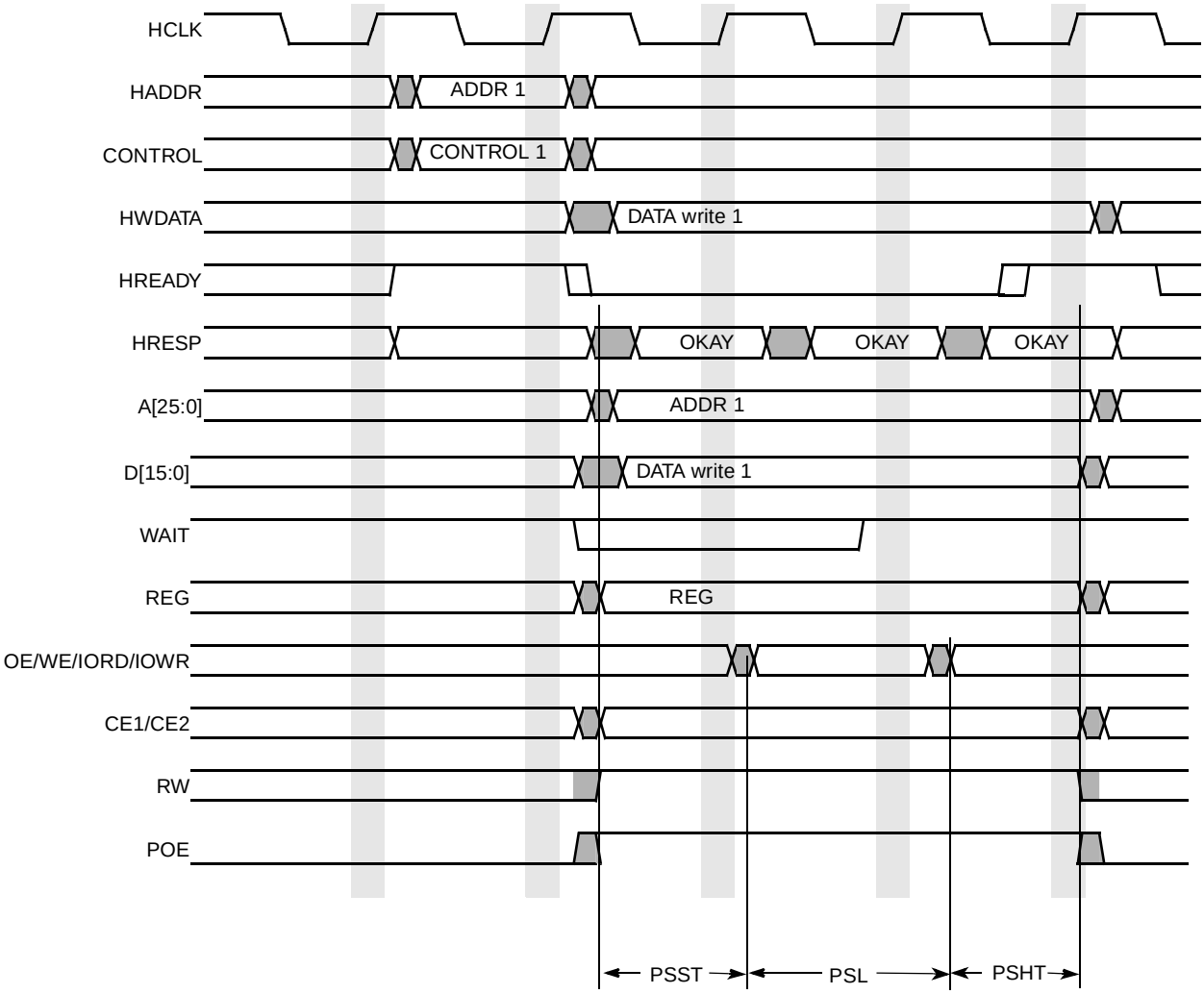



**Figure 68. Write Accesses Timing Diagram—PSHT=1, PSST=1**

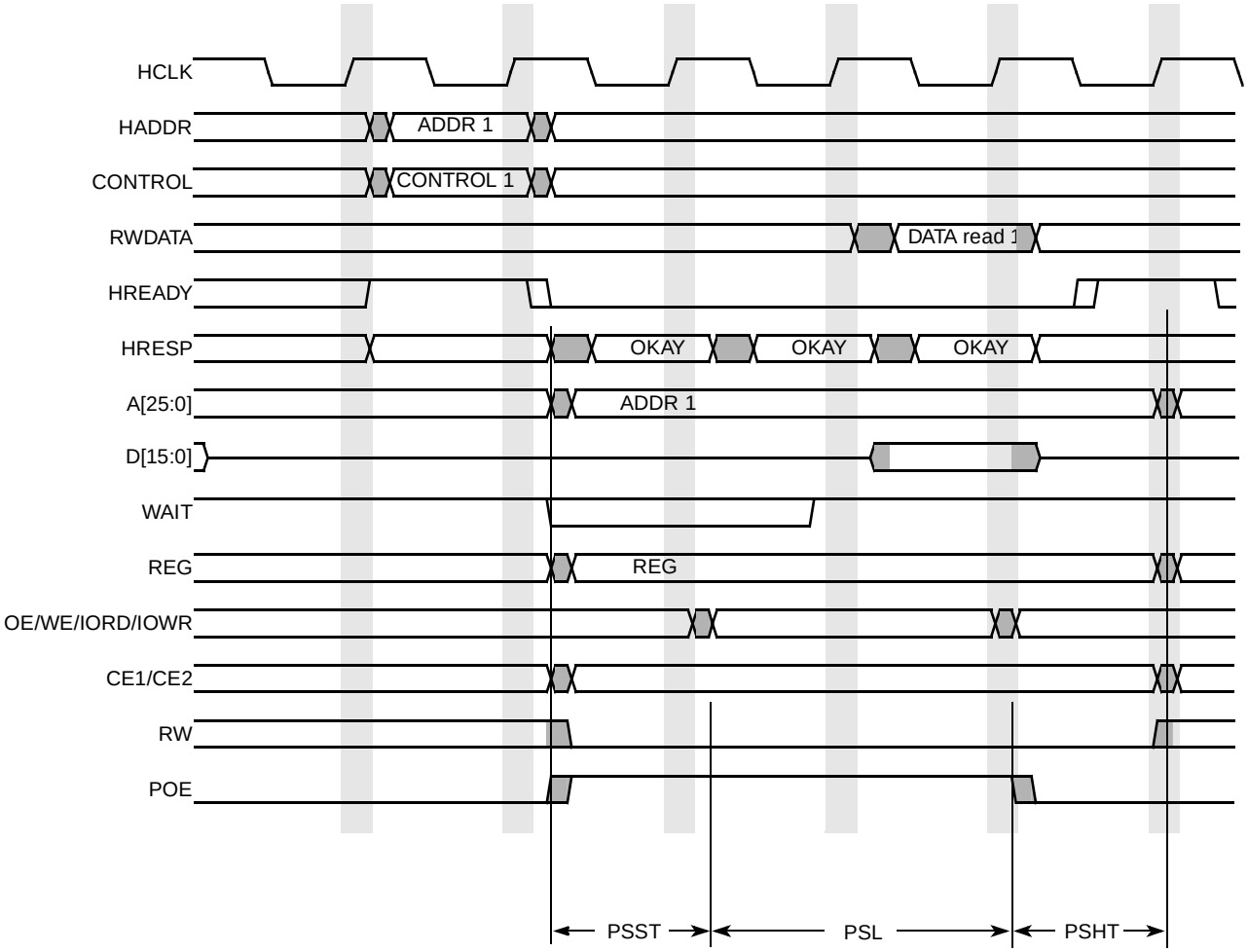



**Figure 69. Read Accesses Timing Diagram—PSHT=1, PSST=1**

**Table 53. PCMCIA Write and Read Timing Parameters**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| PSHT | PCMCIA strobe hold time | 0 | 63 | clock |
| PSST | PCMCIA strobe set up time | 1 | 63 | clock |
| PSL | PCMCIA strobe length | 1 | 128 | clock |

## 4.3.18 PWM Electrical Specifications

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

### 4.3.18.1 PWM Timing

Figure 70 depicts the timing of the PWM, and Table 54 lists the PWM timing characteristics.

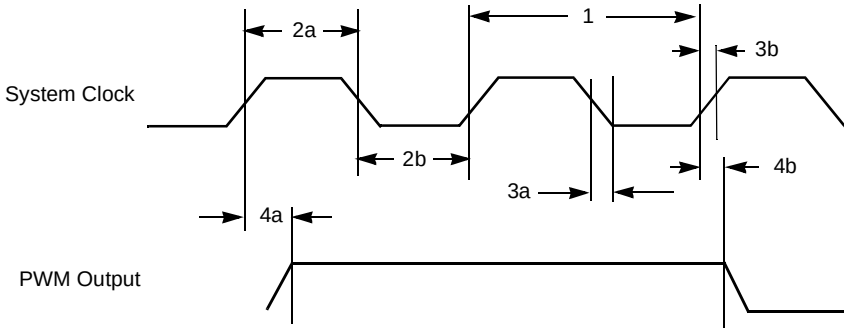



**Figure 70. PWM Timing**

**Table 54. PWM Output Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | System CLK frequency[1] | 0 | ipg_clk | MHz |
| 2a | Clock high time | 12.29 | — | ns |
| 2b | Clock low time | 9.91 | — | ns |
| 3a | Clock fall time | — | 0.5 | ns |
| 3b | Clock rise time | — | 0.5 | ns |
| 4a | Output delay time | — | 9.37 | ns |
| 4b | Output setup time | 8.71 | — | ns |

[1] CL of PWMO = 30 pF

## 4.3.19 SDHC Electrical Specifications

This section describes the electrical information of the SDHC.

### 4.3.19.1 SDHC Timing

Figure 71 depicts the timings of the SDHC, and Table 55 lists the timing parameters.

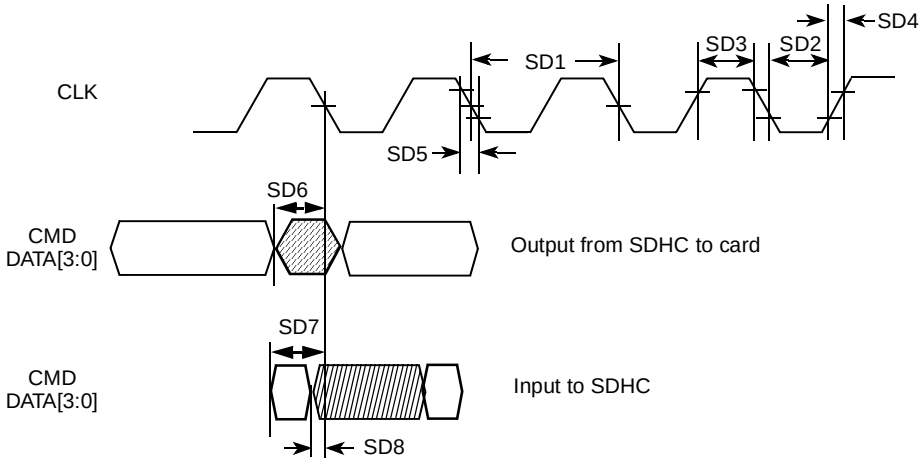



**Figure 71. SDHC Timing Diagram**

**Table 55. SDHC Interface Timing Parameters**

| ID | Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | $f_{PP}$[1] | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed) | $f_{PP}$[2] | 0 | 25 | MHz |
| | Clock Frequency (MMC Full Speed) | $f_{PP}$[3] | 0 | 20 | MHz |
| | Clock Frequency (Identification Mode) | $f_{OD}$[4] | 100 | 400 | kHz |
| SD2 | Clock Low Time | $t_{WL}$ | 10 | — | ns |
| SD3 | Clock High Time | $t_{WH}$ | 10 | — | ns |
| SD4 | Clock Rise Time | $t_{TLH}$ | — | 10 | ns |
| SD5 | Clock Fall Time | $t_{THL}$ | — | 10 | ns |
| SDHC Output/Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | SDHC output delay | $t_{ODL}$ | –6.5 | 3 | ns |
| SDHC Input/Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | SDHC input setup | $t_{IS}$ | — | 18.5 | ns |
| SD8 | SDHC input hold | $t_{IH}$ | — | –11.5 | ns |

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 V–3.3 V.
2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 MHz–25 MHz.
3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 MHz–20 MHz.
4 In card identification mode, card clock must be 100 kHz–400 kHz, voltage ranges from 2.7 V–3.3 V.

## 4.3.20 SIM Electrical Specifications

Each SIM card interface consist of a total of 12 pins (for 2 separate ports of 6 pins each. Mostly one port with 5 pins is used).

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the TX/RX pins, however SIM module can work with CLK equal to 16 times the data rate on TX/RX pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the aim card will be used by the SIM card to recover the clock from the data much like a standard UART. All six (or 5 in case bi-directional TXRX is used) of the pins for each half of the SIM module are asynchronous to each other.

There are no required timing relationships between the signals in normal mode, but there are some in two specific cases: reset and power down sequences.

### 4.3.20.1 General Timing Requirements

Figure 72 shows the timing of the SIM module, and Figure 56 lists the timing parameters.

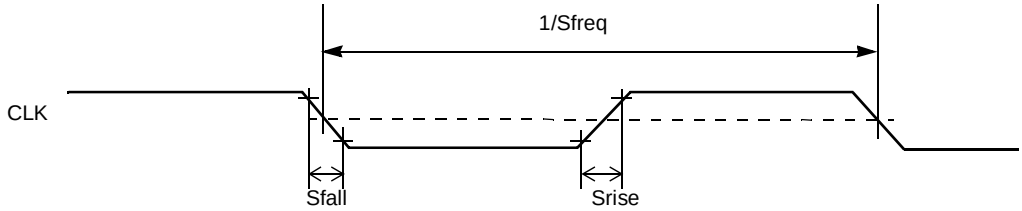



**Figure 72. SIM Clock Timing Diagram**

**Table 56. SIM Timing Specification—High Drive Strength**

| Num | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | SIM Clock Frequency (CLK)[1] | $S_{freq}$ | 0.01 | 5 (Some new cards may reach 10) | MHz |
| 2 | SIM CLK Rise Time [2] | $S_{rise}$ | — | 20 | ns |
| 3 | SIM CLK Fall Time [3] | $S_{fall}$ | — | 20 | ns |
| 4 | SIM Input Transition Time (RX, SIMPD) | $S_{trans}$ | — | 25 | ns |

1 50% duty cycle clock
2 With C = 50pF
3 With C = 50pF

### 4.3.20.2 Reset Sequence

#### 4.3.20.2.1 Cards with Internal Reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 73):

- After powerup, the clock signal is enabled on SGCLK (time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

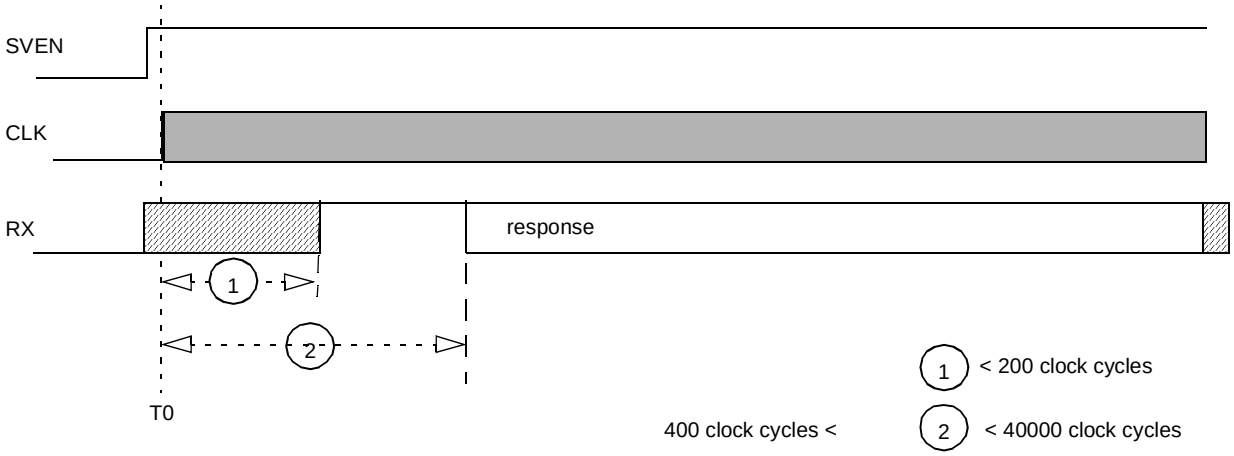



**Figure 73. Internal-Reset Card Reset Sequence**

### 4.3.20.2.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 74):

1. After powerup, the clock signal is enabled on CLK (time T0)
2. After 200 clock cycles, RX must be high.
3. RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
4. RST is set High (time T1)
5. RST must remain High for at least 40000 clock cycles after T1 and a response must be received on RX between 400 and 40000 clock cycles after T1.

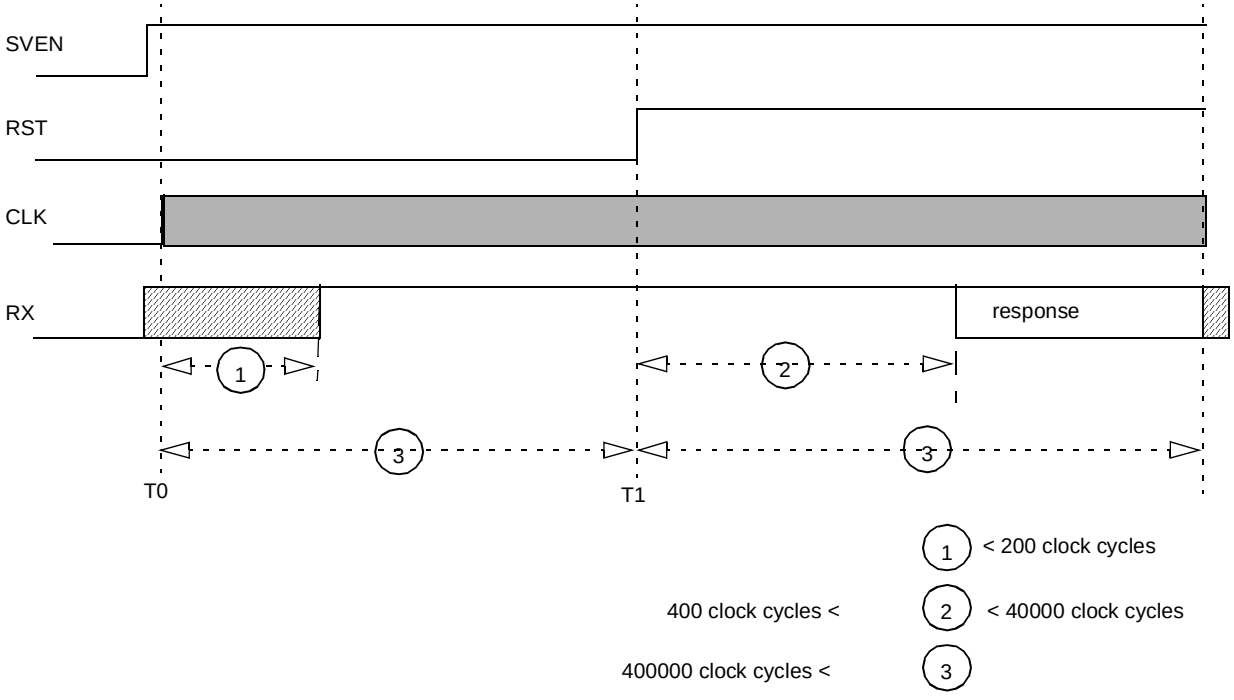



**Figure 74. Active-Low-Reset Card Reset Sequence**

### 4.3.20.3 Power Down Sequence

Power down sequence for SIM interface is as follows:

1. SIMPD port detects the removal of the SIM Card
2. RST goes Low
3. CLK goes Low
4. TX goes Low
5. VEN goes Low

Each of this steps is done in one CKIL period (usually 32 kHz). Power down can be started because of a SIM Card removal detection or launched by the processor. Figure 75 and Table 57 show the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

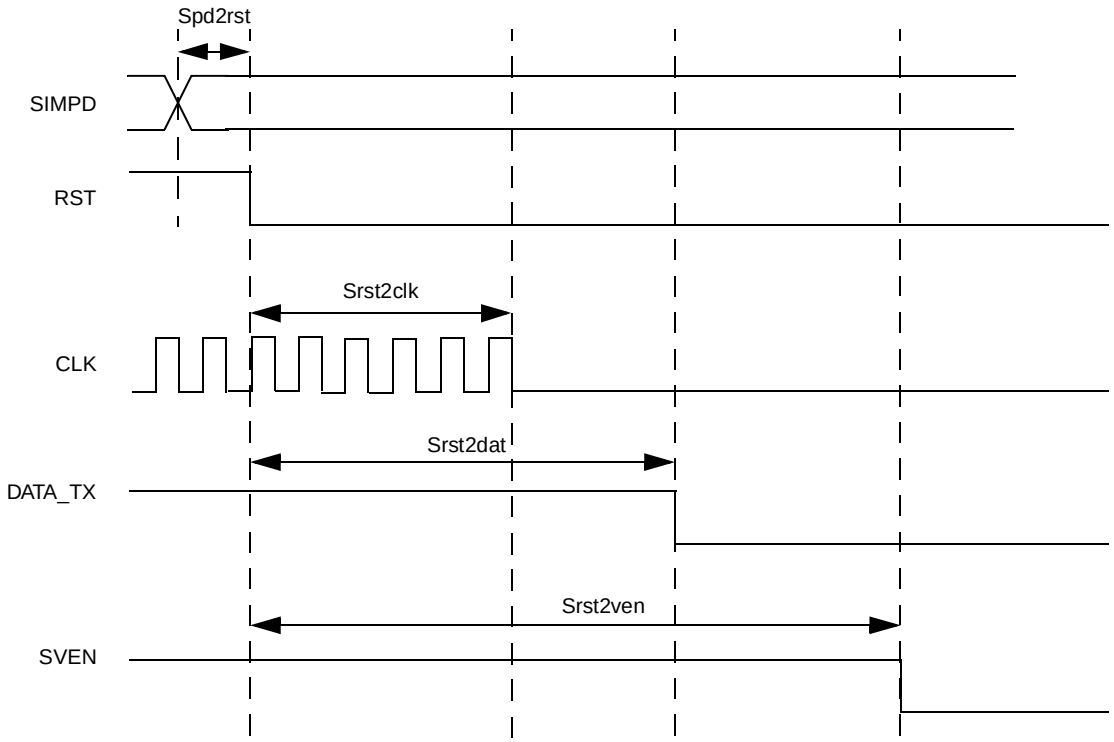



**Figure 75. SmartCard Interface Power Down AC Timing**

**Table 57. Timing Requirements for Power Down Sequence**

| Num | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | SIM reset to SIM clock stop | $S_{rst2clk}$ | 0.9*1/FCKIL | 0.8 | µs |
| 2 | SIM reset to SIM TX data low | $S_{rst2dat}$ | 1.8*1/FCKIL | 1.2 | µs |
| 3 | SIM reset to SIM Voltage Enable Low | $S_{rst2ven}$ | 2.7*1/FCKIL | 1.8 | µs |
| 4 | SIM Presence Detect to SIM reset Low | $S_{pd2rst}$ | 0.9*1/FCKIL | 25 | ns |

## 4.3.21 SJC Electrical Specifications

This section details the electrical characteristics for the SJC module. Figure 76 depicts the SJC test clock input timing. Figure 77 depicts the SJC boundary scan timing, Figure 78 depicts the SJC test access port, Figure 79 depicts the SJC $\overline{\text{TRST}}$ timing, and Table 58 lists the SJC timing parameters.

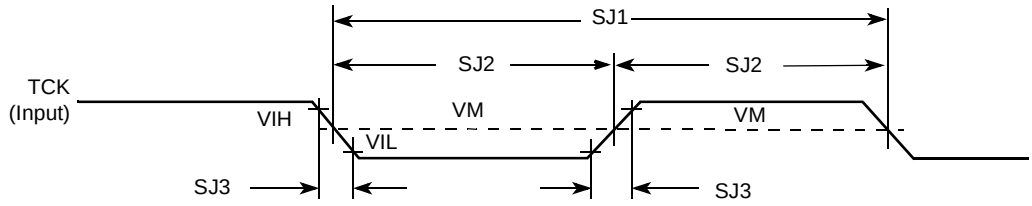



**Figure 76. Test Clock Input Timing Diagram**

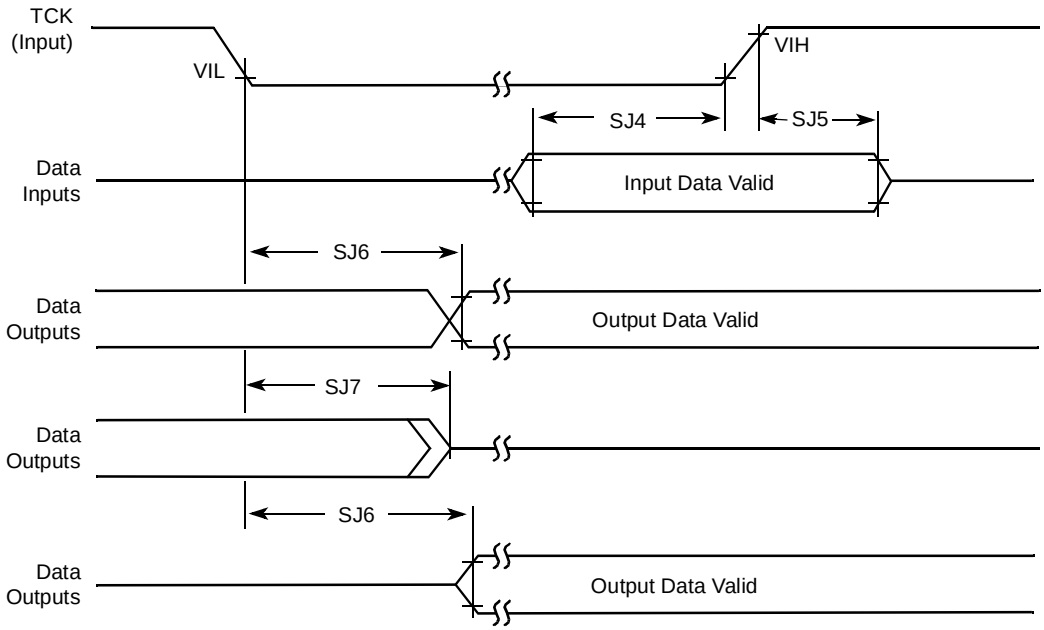



**Figure 77. Boundary Scan (JTAG) Timing Diagram**

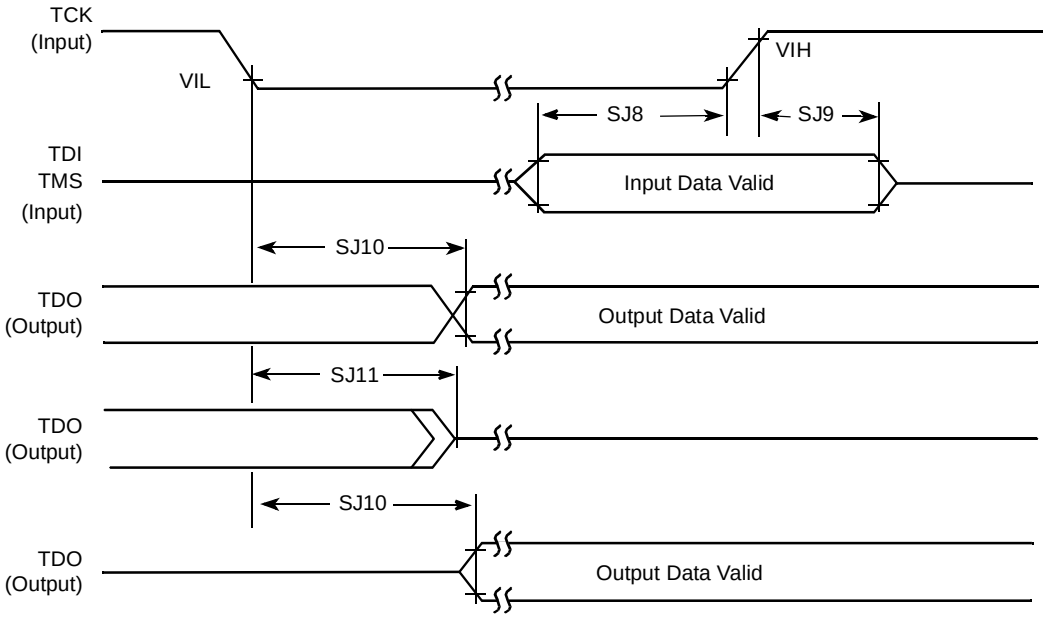



**Figure 78. Test Access Port Timing Diagram**

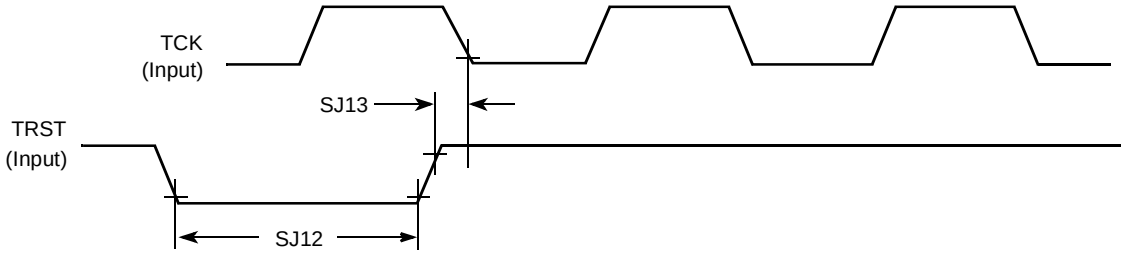



**Figure 79. $\overline{\text{TRST}}$ Timing Diagram**

**Table 58. SJC Timing Parameters**

| ID | Parameter | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SJ1 | TCK cycle time | 100[1] | — | ns |
| SJ2 | TCK clock pulse width measured at $V_M$[2] | 40 | — | ns |
| SJ3 | TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 10 | — | ns |
| SJ5 | Boundary scan input data hold time | 50 | — | ns |
| SJ6 | TCK low to output data valid | — | 50 | ns |
| SJ7 | TCK low to output high impedance | — | 50 | ns |
| SJ8 | TMS, TDI data set-up time | 10 | — | ns |
| SJ9 | TMS, TDI data hold time | 50 | — | ns |
| SJ10 | TCK low to TDO data valid | — | 44 | ns |

**Table 58. SJC Timing Parameters (continued)**

| ID | Parameter | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SJ11 | TCK low to TDO high impedance | — | 44 | ns |
| SJ12 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| SJ13 | $\overline{\text{TRST}}$ set-up time to TCK low | 40 | — | ns |

1 On cases where SDMA TAP is put in the chain, the max TCK frequency is limited by max ratio of 1:8 of SDMA core frequency to TCK limitation. This implies max frequency of 8.25 MHz (or 121.2 ns) for 66 MHz IPG clock.

2 $V_{M}$ - mid point voltage

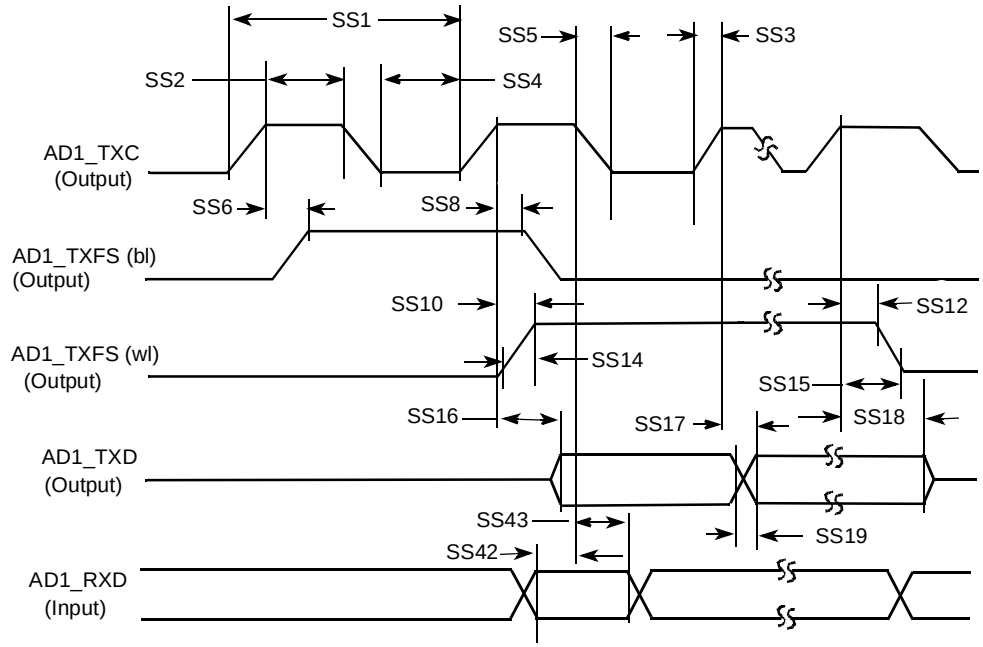
## 4.3.22 SSI Electrical Specifications

This section describes the electrical information of SSI. Note the following pertaining to timing information:

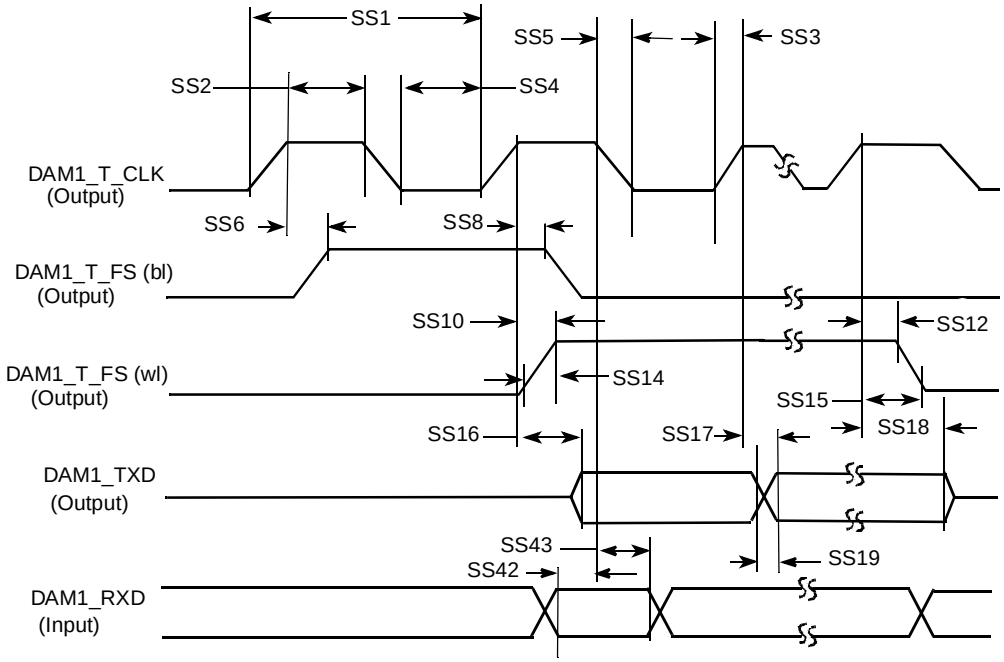
- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on AUDMUX signals when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing will be same as that of Tx Data (for example, during AC97 mode of operation).

### 4.3.22.1 SSI Transmitter Timing with Internal Clock

Figure 80 depicts the SSI transmitter timing with internal clock, and Table 59 lists the timing parameters.




**Note:** SRXD Input in Synchronous mode only




**Note:** SRXD Input in Synchronous mode only

**Figure 80. SSI Transmitter with Internal Clock Timing Diagram**

**Table 59. SSI Transmitter with Internal Clock Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6 | ns |
| SS6 | (Tx) CK high to FS (bl) high | — | 15.0 | ns |
| SS8 | (Tx) CK high to FS (bl) low | — | 15.0 | ns |
| SS10 | (Tx) CK high to FS (wl) high | — | 15.0 | ns |
| SS12 | (Tx) CK high to FS (wl) low | — | 15.0 | ns |
| SS14 | (Tx/Rx) Internal FS rise time | — | 6 | ns |
| SS15 | (Tx/Rx) Internal FS fall time | — | 6 | ns |
| SS16 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS17 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS18 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| SS19 | STXD rise/fall time | — | 6 | ns |
| Synchronous Internal Clock Operation | | | | |
| SS42 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS43 | SRXD hold after (Tx) CK falling | 0 | — | ns |
| SS52 | Loading | — | 25 | pF |

### 4.3.22.2 SSI Receiver Timing with Internal Clock

Figure 81 depicts the SSI receiver timing with internal clock, and Table 60 lists the timing parameters.

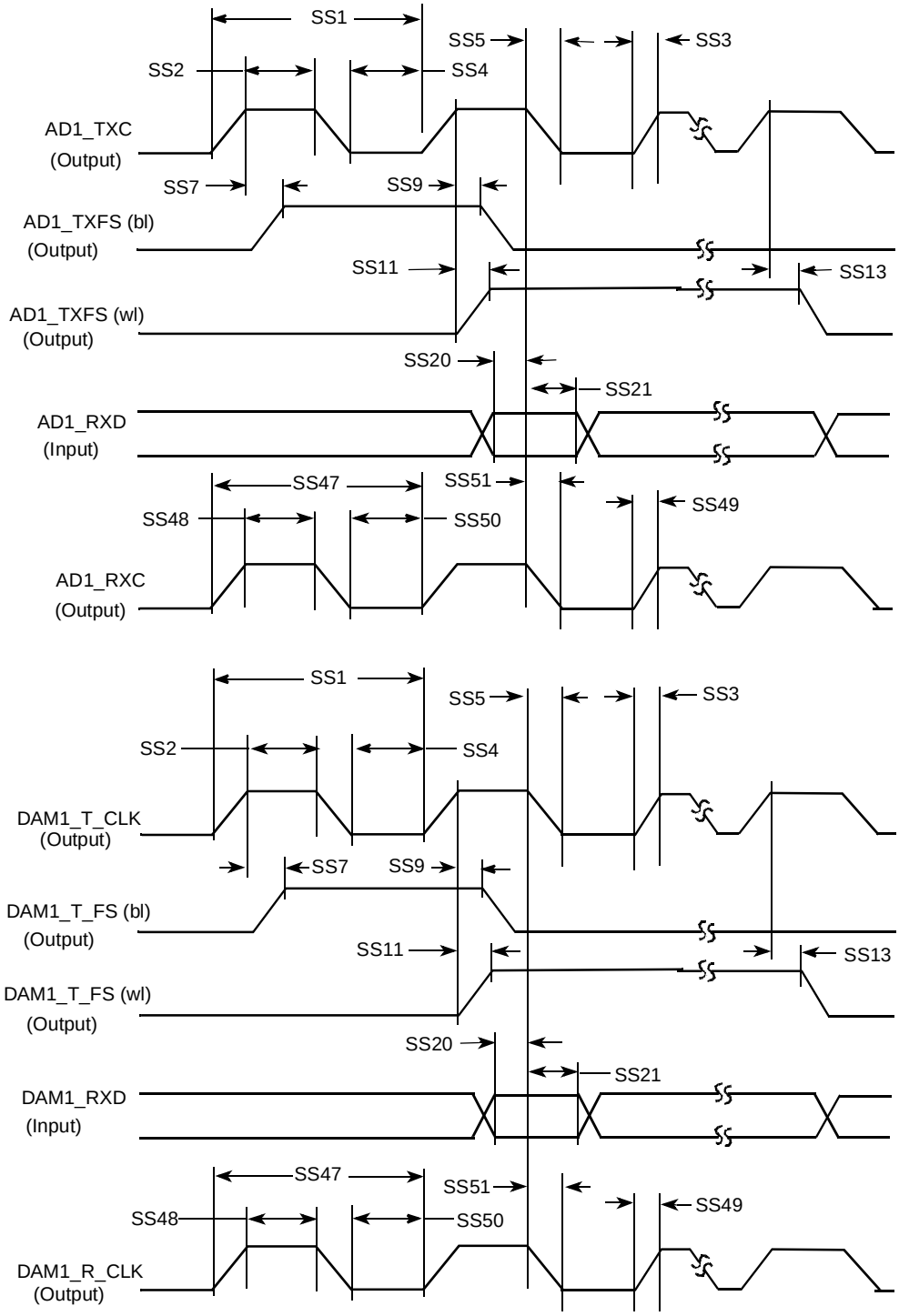


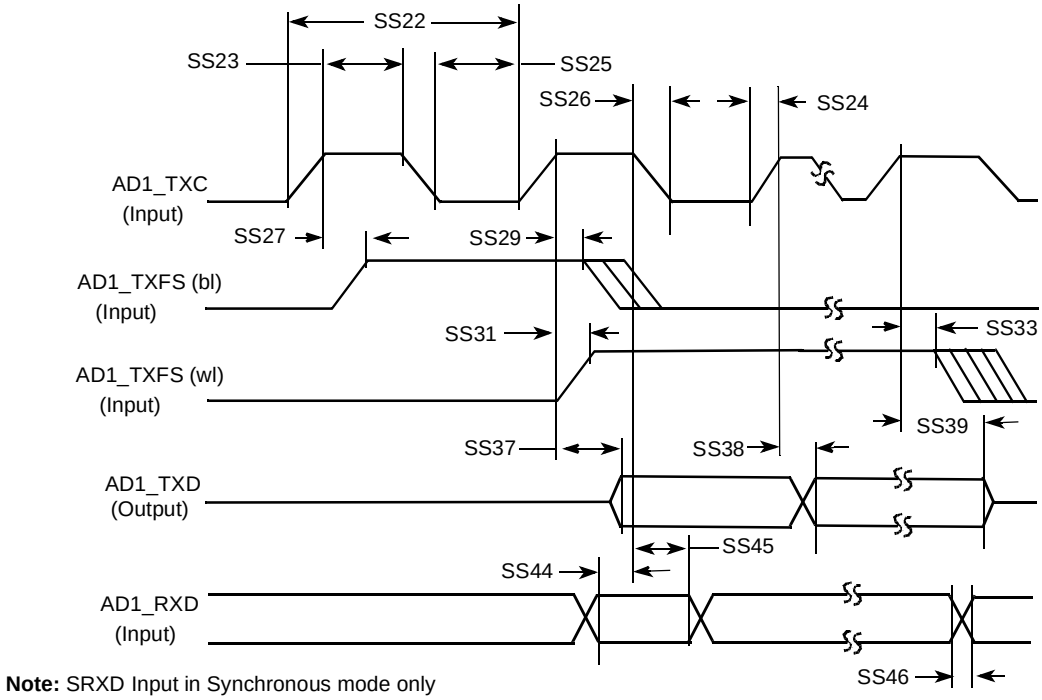

**Figure 81. SSI Receiver with Internal Clock Timing Diagram**

**Table 60. SSI Receiver with Internal Clock Timing Parameters**

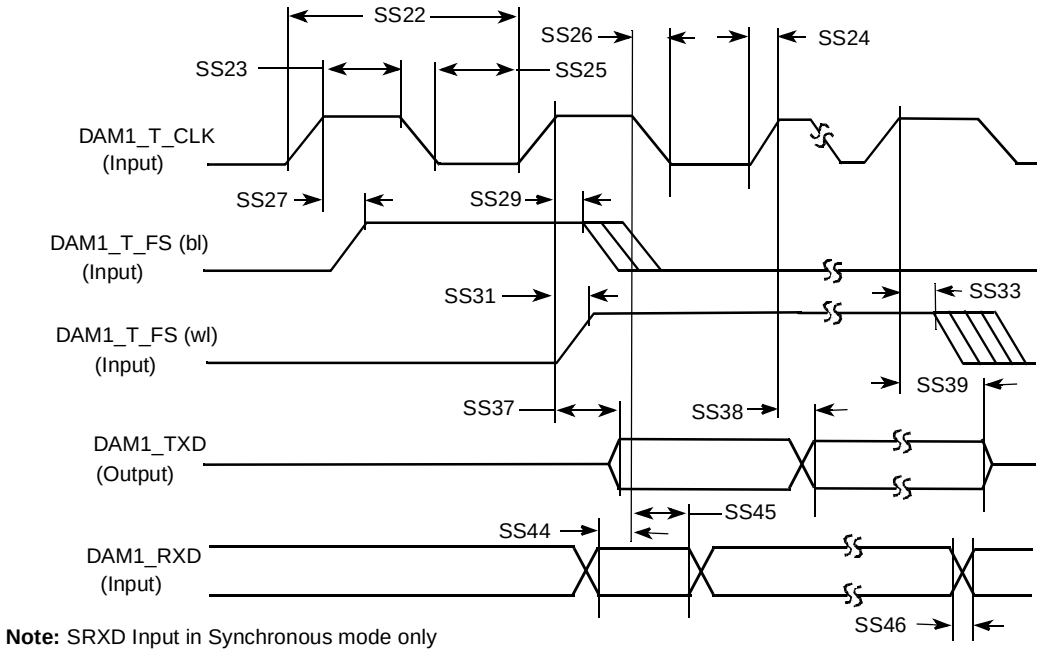
| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Internal Clock Operation | | | | |
| SS1 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS2 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS3 | (Tx/Rx) CK clock rise time | — | 6 | ns |
| SS4 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS5 | (Tx/Rx) CK clock fall time | — | 6 | ns |
| SS7 | (Rx) CK high to FS (bl) high | — | 15.0 | ns |
| SS9 | (Rx) CK high to FS (bl) low | — | 15.0 | ns |
| SS11 | (Rx) CK high to FS (wl) high | — | 15.0 | ns |
| SS13 | (Rx) CK high to FS (wl) low | — | 15.0 | ns |
| SS20 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS21 | SRXD hold time after (Rx) CK low | 0 | — | ns |
| Oversampling Clock Operation | | | | |
| SS47 | Oversampling clock period | 15.04 | — | ns |
| SS48 | Oversampling clock high period | 6 | — | ns |
| SS49 | Oversampling clock rise time | — | 3 | ns |
| SS50 | Oversampling clock low period | 6 | — | ns |
| SS51 | Oversampling clock fall time | — | 3 | ns |

### 4.3.22.3 SSI Transmitter Timing with External Clock

Figure 82 depicts the SSI transmitter timing with external clock, and Table 61 lists the timing parameters.




**Note:** SRXD Input in Synchronous mode only




**Note:** SRXD Input in Synchronous mode only

**Figure 82. SSI Transmitter with External Clock Timing Diagram**

**Table 61. SSI Transmitter with External Clock Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |
| SS27 | (Tx) CK high to FS (bl) high | –10.0 | 15.0 | ns |
| SS29 | (Tx) CK high to FS (bl) low | 10.0 | — | ns |
| SS31 | (Tx) CK high to FS (wl) high | –10.0 | 15.0 | ns |
| SS33 | (Tx) CK high to FS (wl) low | 10.0 | — | ns |
| SS37 | (Tx) CK high to STXD valid from high impedance | — | 15.0 | ns |
| SS38 | (Tx) CK high to STXD high/low | — | 15.0 | ns |
| SS39 | (Tx) CK high to STXD high impedance | — | 15.0 | ns |
| Synchronous External Clock Operation | | | | |
| SS44 | SRXD setup before (Tx) CK falling | 10.0 | — | ns |
| SS45 | SRXD hold after (Tx) CK falling | 2.0 | — | ns |
| SS46 | SRXD rise/fall time | — | 6.0 | ns |

### 4.3.22.4 SSI Receiver Timing with External Clock

Figure 83 depicts the SSI receiver timing with external clock, and Table 62 lists the timing parameters.

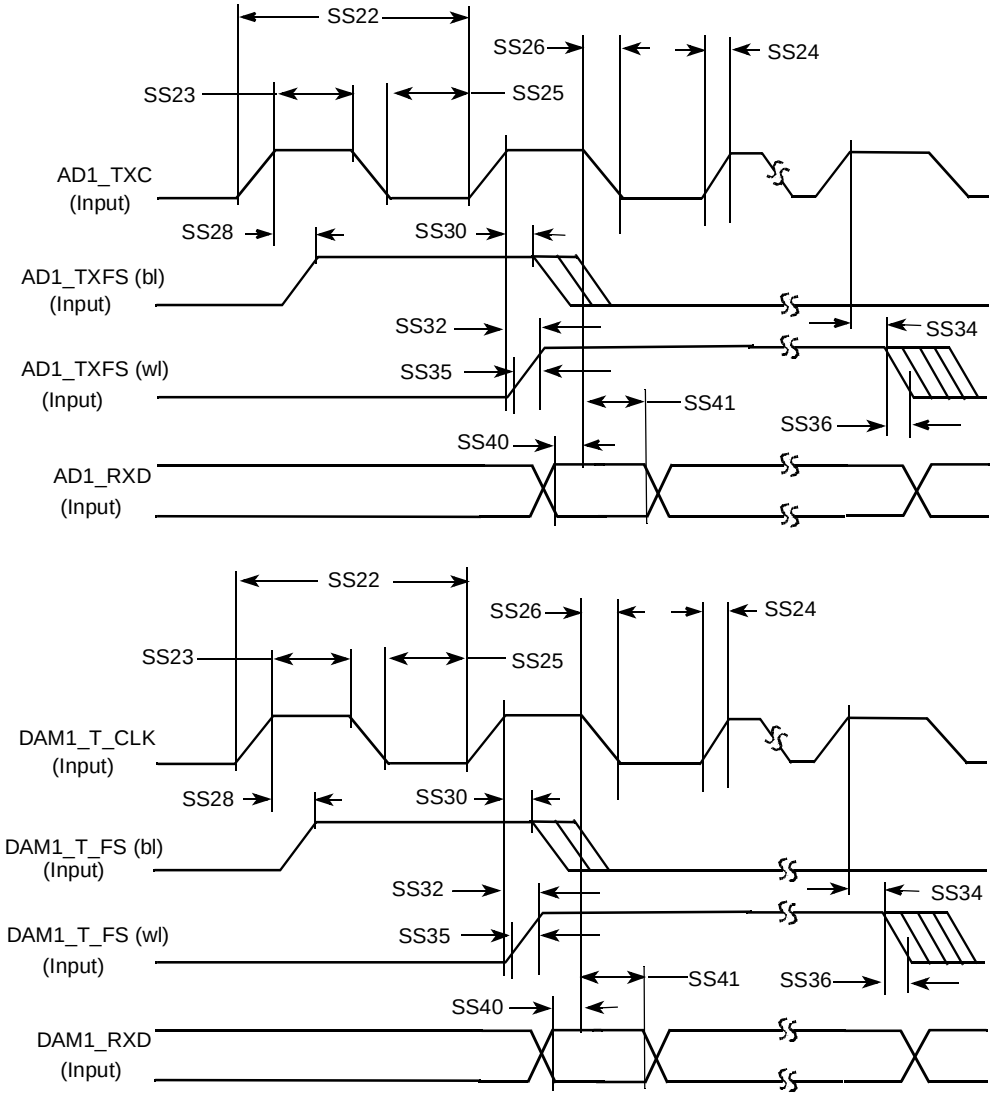



**Figure 83. SSI Receiver with External Clock Timing Diagram**

**Table 62. SSI Receiver with External Clock Timing Parameters**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| External Clock Operation | | | | |
| SS22 | (Tx/Rx) CK clock period | 81.4 | — | ns |
| SS23 | (Tx/Rx) CK clock high period | 36.0 | — | ns |
| SS24 | (Tx/Rx) CK clock rise time | — | 6.0 | ns |
| SS25 | (Tx/Rx) CK clock low period | 36.0 | — | ns |
| SS26 | (Tx/Rx) CK clock fall time | — | 6.0 | ns |

**Table 62. SSI Receiver with External Clock Timing Parameters (continued)**

| ID | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| SS28 | (Rx) CK high to FS (bl) high | –10.0 | 15.0 | ns |
| SS30 | (Rx) CK high to FS (bl) low | 10.0 | — | ns |
| SS32 | (Rx) CK high to FS (wl) high | –10.0 | 15.0 | ns |
| SS34 | (Rx) CK high to FS (wl) low | 10.0 | — | ns |
| SS35 | (Tx/Rx) External FS rise time | — | 6.0 | ns |
| SS36 | (Tx/Rx) External FS fall time | — | 6.0 | ns |
| SS40 | SRXD setup time before (Rx) CK low | 10.0 | — | ns |
| SS41 | SRXD hold time after (Rx) CK low | 2.0 | — | ns |

## 4.3.23 USB Electrical Specifications

This section describes the electrical information of the USBOTG port. The OTG port supports both serial and parallel interfaces.

The high speed (HS) interface is supported via the ULPI (Ultra Low Pin Count Interface). Figure 84 depicts the USB ULPI timing diagram, and Table 63 lists the timing parameters.

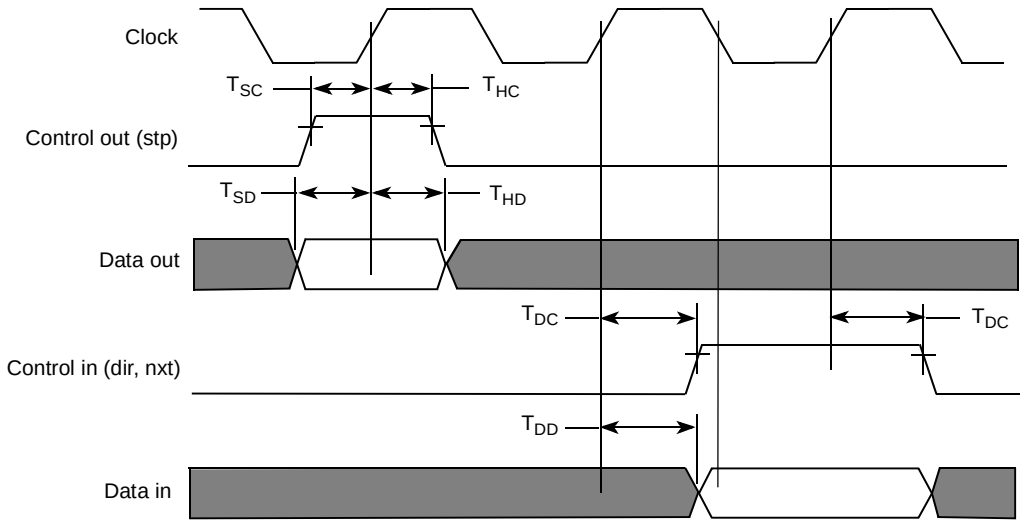



**Figure 84. USB ULPI Interface Timing Diagram**

**Table 63. USB ULPI Interface Timing Specification[1]**

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Setup time (control in, 8-bit data in) | $T_{SC}$, $T_{SD}$ | 6 | — | ns |
| Hold time (control in, 8-bit data in) | $T_{HC}$, $T_{HD}$ | 0 | — | ns |
| Output delay (control out, 8-bit data out) | $T_{DC}$, $T_{DD}$ | — | 9 | ns |

1 Timing parameters are given as viewed by transceiver side.

# 5 Package Information and Pinout

This section includes the contact assignment information and mechanical package drawing for the MCIMX31.

## 5.1 MAPBGA Production Package—457 14 x 14 mm, 0.5 mm Pitch

This section contains the outline drawing, signal assignment map (see Section 7, “Revision History,” Table 69 for the 0.5 mm 14 × 14 MAPBGA signal assignments), and MAPBGA ground/power ID by ball grid location for the 457 14 x 14 mm, 0.5 mm pitch package.

### 5.1.1 Production Package Outline Drawing–14 x 14 mm 0.5 mm

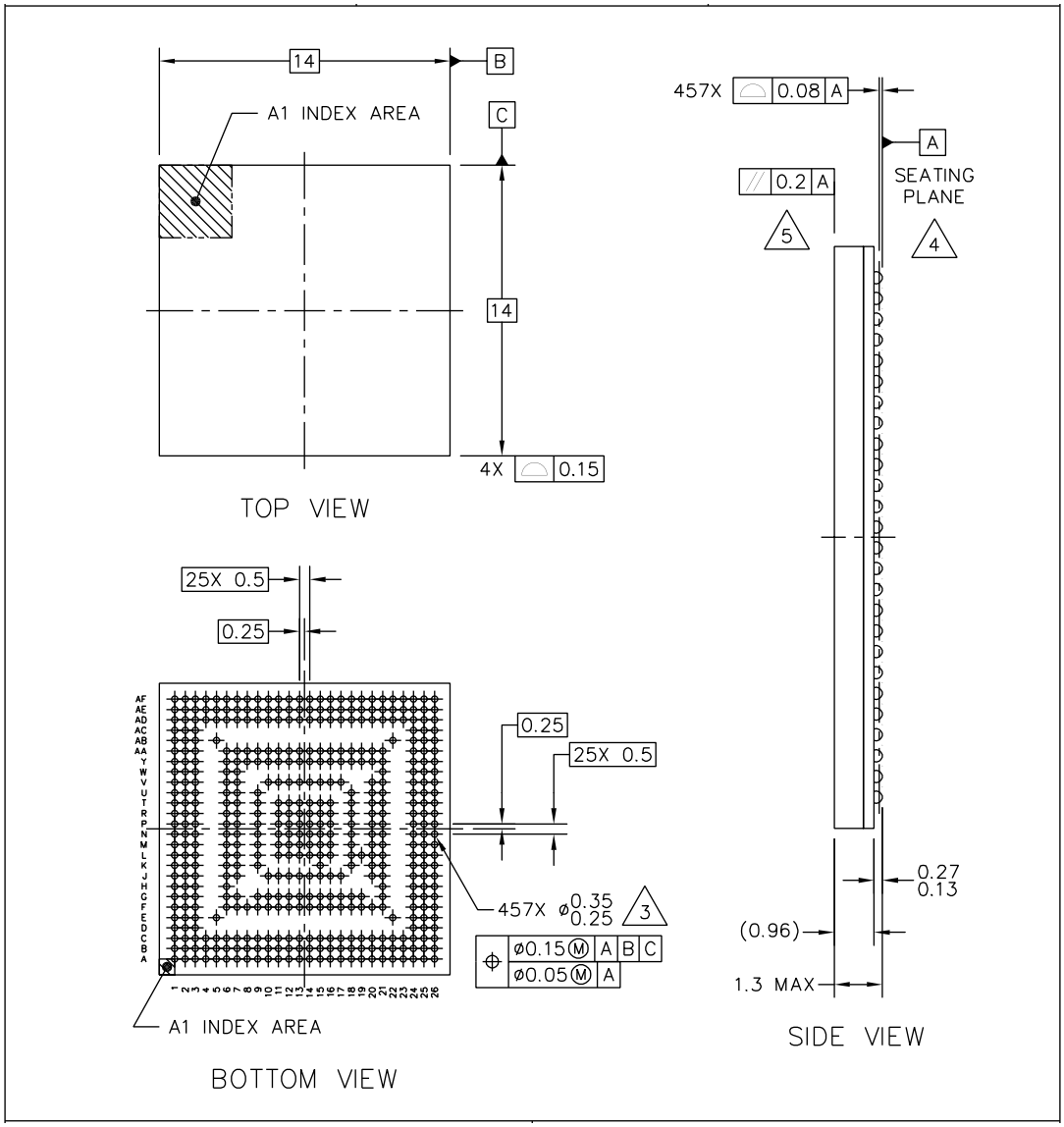



**Figure 85. Production Package: Case 1581—0.5 mm Pitch**

### 5.1.2 MAPBGA Signal Assignment–14 × 14 mm 0.5 mm

See Section 7, "Revision History," Figure 69 for the 0.5 mm 14 × 14 MAPBGA signal assignments.

### 5.1.3 Connection Tables–14 x 14 mm 0.5 mm

Table 64 shows the device connection list for power and ground, alpha-sorted. Table 65 shows the device connection list for signals.

#### 5.1.3.1 Ground and Power ID Locations–14 x 14 mm 0.5 mm

**Table 64. 14 x 14 MAPBGA Ground/Power ID by Ball Grid Location**

| GND/PWR ID | Ball Location |
|---|---|
| FGND | AB24 |
| FUSE_VDD | AC24 |
| FVCC | AA24 |
| GND | A1, A2, A25, A26, B1, B2, B25, B26, C1, C2, C24, C25, C26, D1, D25, E22, E24, F21, L12, M11, M12, M13, M14, M15, M16, N12, N13, N14, N15, N16, P12, P13, P14, P15, P16, R12, R13, R14, R15, R16, T12, T13, V17, AC2, AC26, AD1, AD2, AD24, AD25, AD26, AE1, AE2, AE24, AE25, AE26, AF1, AF2, AF25, AF26 |
| IOQVDD | Y6 |
| MGND | T15 |
| MVCC | V15 |
| NVCC1 | G19, G21, K18 |
| NVCC2 | Y17, Y18, Y19, Y20 |
| NVCC3 | L9, M9, N11 |
| NVCC4 | L18, L19 |
| NVCC5 | E5, F6, G7 |
| NVCC6 | J15, J16, K15 |
| NVCC7 | N18, P18, R18, T18 |
| NVCC8 | J12, J13 |
| NVCC9 | J17 |
| NVCC10 | P9, P11, R11, T11 |
| NVCC21 | Y14, Y15, Y16 |
| NVCC22 | W7, Y7, Y8, Y9, Y10, Y11, Y12, Y13, AA6 |
| QVCC | J14, L13, L14, L15, L16, M18, U18, V10, V11, V12, V13 |
| QVCC1 | J10, J11, K9, L11 |
| QVCC4 | N9, R9, T9, U9 |
| SGND | T14 |
| SVCC | V14 |
| UVCC | V16 |
| UGND | T16 |

### 5.1.3.2 BGA Signal ID by Ball Grid Location–14 x 14 0.5 mm

Table 65 shows the device connection list for signals only, alpha-sorted by signal identification.

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location**

| Signal ID | Ball Location |
|---|---|
| A0 | AD6 |
| A1 | AF5 |
| A10 | AF18 |
| A11 | AC3 |
| A12 | AD3 |
| A13 | AD4 |
| A14 | AF17 |
| A15 | AF16 |
| A16 | AF15 |
| A17 | AF14 |
| A18 | AF13 |
| A19 | AF12 |
| A2 | AB5 |
| A20 | AF11 |
| A21 | AF10 |
| A22 | AF9 |
| A23 | AF8 |
| A24 | AF7 |
| A25 | AF6 |
| A3 | AE4 |
| A4 | AA3 |
| A5 | AF4 |
| A6 | AB3 |
| A7 | AE3 |
| A8 | AD5 |
| A9 | AF3 |
| ATA_CS0 | J6 |
| ATA_CS1 | F2 |
| ATA_DIOR | E2 |
| ATA_DIOW | H6 |
| ATA_DMACK | F1 |
| $\overline{\text{ATA_RESET}}$ | H3 |
| BATT_LINE | F7 |
| BCLK | AB26 |
| BOOT_MODE0 | F20 |
| BOOT_MODE1 | C21 |
| BOOT_MODE2 | D24 |
| BOOT_MODE3 | C22 |
| BOOT_MODE4 | D26 |
| CAPTURE | A22 |
| CAS | AD20 |
| CE_CONTROL | A14 |
| CKIH | F24 |

| Signal ID | Ball Location |
|---|---|
| CKIL | H21 |
| CLKO | C23 |
| CLKSS | G26 |
| COMPARE | G18 |
| CONTRAST | R24 |
| CS0 | AE23 |
| CS1 | AF23 |
| CS2 | AE21 |
| CS3 | AD22 |
| CS4 | AF24 |
| CS5 | AF22 |
| CSI_D10 | M24 |
| CSI_D11 | L26 |
| CSI_D12 | M21 |
| CSI_D13 | M25 |
| CSI_D14 | M20 |
| CSI_D15 | M26 |
| CSI_D4 | L21 |
| CSI_D5 | K25 |
| CSI_D6 | L24 |
| CSI_D7 | K26 |
| CSI_D8 | L20 |
| CSI_D9 | L25 |
| CSI_HSYNC | K20 |
| CSI_MCLK | K24 |
| CSI_PIXCLK | J26 |
| CSI_VSYNC | J25 |
| CSPI1_MISO | P7 |
| CSPI1_MOSI | P2 |
| CSPI1_SCLK | N2 |
| CSPI1_SPI_RDY | N3 |
| CSPI1_SS0 | P3 |
| CSPI1_SS1 | P1 |
| CSPI1_SS2 | P6 |
| CSPI2_MISO | A4 |
| CSPI2_MOSI | E3 |
| CSPI2_SCLK | C7 |
| CSPI2_SPI_RDY | B6 |
| CSPI2_SS0 | B5 |
| CSPI2_SS1 | C6 |
| CSPI2_SS2 | A5 |
| CSPI3_MISO | G3 |
| CSPI3_MOSI | D2 |

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| CSPI3_SCLK | E1 |
| CSPI3_SPI_RDY | G6 |
| CTS1 | B11 |
| CTS2 | G13 |
| D0 | AB2 |
| D1 | Y3 |
| D10 | Y1 |
| D11 | U7 |
| D12 | W2 |
| D13 | V3 |
| D14 | W1 |
| D15 | U6 |
| D2 | AB1 |
| D3 | W6 |
| D3_CLS | R20 |
| D3_REV | T26 |
| D3_SPL | U25 |
| D4 | AA2 |
| D5 | V7 |
| D6 | AA1 |
| D7 | W3 |
| D8 | Y2 |
| D9 | V6 |
| DCD_DCE1 | B12 |
| DCD_DTE1 | B13 |
| $\overline{DE}$ | C18 |
| DQM0 | AE19 |
| DQM1 | AD19 |
| DQM2 | AA20 |
| DQM3 | AE18 |
| DRDY0 | N26 |
| DSR_DCE1 | A11 |
| DSR_DTE1 | A12 |
| DTR_DCE1 | C11 |
| DTR_DCE2 | F12 |
| DTR_DTE1 | C12 |
| DVFS0 | E25 |
| DVFS1 | G24 |
| EB0 | W21 |
| EB1 | Y24 |
| ECB | AD23 |
| FPSHIFT | N21 |
| GPIO1_0 | F18 |
| GPIO1_1 | B23 |
| GPIO1_2 | C20 |
| LD7 | W25 |

| Signal ID | Ball Location |
|---|---|
| GPIO1_3 | F25 |
| GPIO1_4 | F19 |
| GPIO1_5 (PWR RDY) | B24 |
| GPIO1_6 | A23 |
| GPIO3_0 | K21 |
| GPIO3_1 | H26 |
| HSYNC | N25 |
| I2C_CLK | J24 |
| I2C_DAT | H25 |
| IOIS16 | J3 |
| KEY_COL0 | C15 |
| KEY_COL1 | B17 |
| KEY_COL2 | G15 |
| KEY_COL3 | A17 |
| KEY_COL4 | C16 |
| KEY_COL5 | B18 |
| KEY_COL6 | F15 |
| KEY_COL7 | A18 |
| KEY_ROW0 | F13 |
| KEY_ROW1 | B15 |
| KEY_ROW2 | C14 |
| KEY_ROW3 | A15 |
| KEY_ROW4 | G14 |
| KEY_ROW5 | B16 |
| KEY_ROW6 | F14 |
| KEY_ROW7 | A16 |
| L2PG | See VPG1 |
| LBA | AE22 |
| LCS0 | P26 |
| LCS1 | P21 |
| LD0 | T24 |
| LD1 | U26 |
| LD10 | V24 |
| LD11 | Y25 |
| LD12 | Y26 |
| LD13 | V21 |
| LD14 | AA25 |
| LD15 | W24 |
| LD16 | AA26 |
| LD17 | V20 |
| LD2 | T21 |
| LD3 | V25 |
| LD4 | T20 |
| LD5 | V26 |
| LD6 | U24 |
| SCK6 | T2 |

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| LD8 | U21 |
| LD9 | W26 |
| M_GRANT | Y21 |
| M_REQUEST | AC25 |
| MA10 | AC1 |
| MCUPG | See VPG0 |
| NFALE | V1 |
| $\overline{\text{NFCE}}$ | T6 |
| NFCLE | U3 |
| NFRB | U1 |
| $\overline{\text{NFRE}}$ | V2 |
| $\overline{\text{NFWE}}$ | T7 |
| $\overline{\text{NFWP}}$ | U2 |
| OE | AB25 |
| PAR_RS | R21 |
| PC_BVD1 | H2 |
| PC_BVD2 | K6 |
| $\overline{\text{PC_CD1}}$ | L7 |
| $\overline{\text{PC_CD2}}$ | K1 |
| PC_POE | J7 |
| PC_PWRON | K3 |
| PC_READY | J2 |
| PC_RST | H1 |
| $\overline{\text{PC_RW}}$ | G2 |
| PC_VS1 | J1 |
| PC_VS2 | K7 |
| $\overline{\text{PC_WAIT}}$ | L6 |
| $\overline{\text{POR}}$ | H24 |
| POWER_FAIL | E26 |
| PWMO | G1 |
| RAS | AF19 |
| READ | P20 |
| $\overline{\text{RESET_IN}}$ | J21 |
| RI_DCE1 | F11 |
| RI_DTE1 | G12 |
| RTCK | C17 |
| RTS1 | G11 |
| RTS2 | B14 |
| RW | AB22 |
| RXD1 | A10 |
| RXD2 | A13 |
| SCK3 | R2 |
| SCK4 | C4 |
| SCK5 | D3 |
| SDCKE0 | AD21 |
| SDCKE1 | AF21 |

| Signal ID | Ball Location |
|---|---|
| SCLK0 | B22 |
| SD_D_CLK | P24 |
| SD_D_I | N20 |
| SD_D_IO | P25 |
| SD0 | AD18 |
| SD1 | AE17 |
| SD1_CLK | M7 |
| SD1_CMD | L2 |
| SD1_DATA0 | M6 |
| SD1_DATA1 | L1 |
| SD1_DATA2 | L3 |
| SD1_DATA3 | K2 |
| SD10 | AE15 |
| SD11 | AE14 |
| SD12 | AD14 |
| SD13 | AA14 |
| SD14 | AE13 |
| SD15 | AD13 |
| SD16 | AA13 |
| SD17 | AD12 |
| SD18 | AA12 |
| SD19 | AE11 |
| SD2 | AA19 |
| SD20 | AE10 |
| SD21 | AA11 |
| SD22 | AE9 |
| SD23 | AA10 |
| SD24 | AE8 |
| SD25 | AD10 |
| SD26 | AE7 |
| SD27 | AA9 |
| SD28 | AA8 |
| SD29 | AD9 |
| SD3 | AA18 |
| SD30 | AE6 |
| SD31 | AA7 |
| SD4 | AD17 |
| SD5 | AA17 |
| SD6 | AE16 |
| SD7 | AA16 |
| SD8 | AD15 |
| SD9 | AA15 |
| SDBA0 | AD7 |
| SDBA1 | AE5 |
| TRSTB | B20 |
| TTM_PAD | U20 |

**Table 65. 14 x 14 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| SDCLK | AA21 |
| $\overline{\text{SDCLK}}$ | AE20 |
| SDQS0 | AD16 |
| SDQS1 | AE12 |
| SDQS2 | AD11 |
| SDQS3 | AD8 |
| SDWE | AF20 |
| SER_RS | T25 |
| SFS3 | R6 |
| SFS4 | F3 |
| SFS5 | A3 |
| SFS6 | T3 |
| SIMPD0 | G17 |
| SJC_MOD | A20 |
| SRST0 | C19 |
| SRX0 | B21 |
| SRXD3 | R3 |
| SRXD4 | C3 |
| SRXD5 | B4 |
| SRXD6 | R7 |
| STX0 | F17 |
| STXD3 | R1 |
| STXD4 | B3 |
| STXD5 | C5 |
| STXD6 | T1 |
| SVEN0 | A21 |
| TCK | B19 |
| TDI | F16 |
| TDO | A19 |
| TMS | G16 |

| Signal ID | Ball Location |
|---|---|
| TXD1 | F10 |
| TXD2 | C13 |
| USB_BYP | A9 |
| USB_OC | C10 |
| USB_PWR | B10 |
| USBH2_CLK | N1 |
| USBH2_DATA0 | M1 |
| USBH2_DATA1 | M3 |
| USBH2_DIR | N7 |
| USBH2_NXT | N6 |
| USBH2_STP | M2 |
| USBOTG_CLK | G10 |
| USBOTG_DATA0 | F9 |
| USBOTG_DATA1 | B8 |
| USBOTG_DATA2 | G9 |
| USBOTG_DATA3 | A7 |
| USBOTG_DATA4 | C8 |
| USBOTG_DATA5 | B7 |
| USBOTG_DATA6 | F8 |
| USBOTG_DATA7 | A6 |
| USBOTG_DIR | B9 |
| USBOTG_NXT | A8 |
| USBOTG_STP | C9 |
| VPG0 | G25 |
| VPG1 | J20 |
| VSTBY | F26 |
| VSYNC0 | N24 |
| VSYNC3 | R26 |
| WATCHDOG_RST | A24 |
| WRITE | R25 |

## 5.2 MAPBGA Production Package—473 19 x 19 mm, 0.8 mm Pitch

This section contains the outline drawing, signal assignment map (see Section 7, “Revision History,” Table 70 for the 19 x 19 mm, 0.8 mm pitch signal assignments), and MAPBGA ground/power ID by ball grid location for the 473 19 x 19 mm, 0.8 mm pitch package.

### 5.2.1 Production Package Outline Drawing–19 x 19 mm 0.8 mm

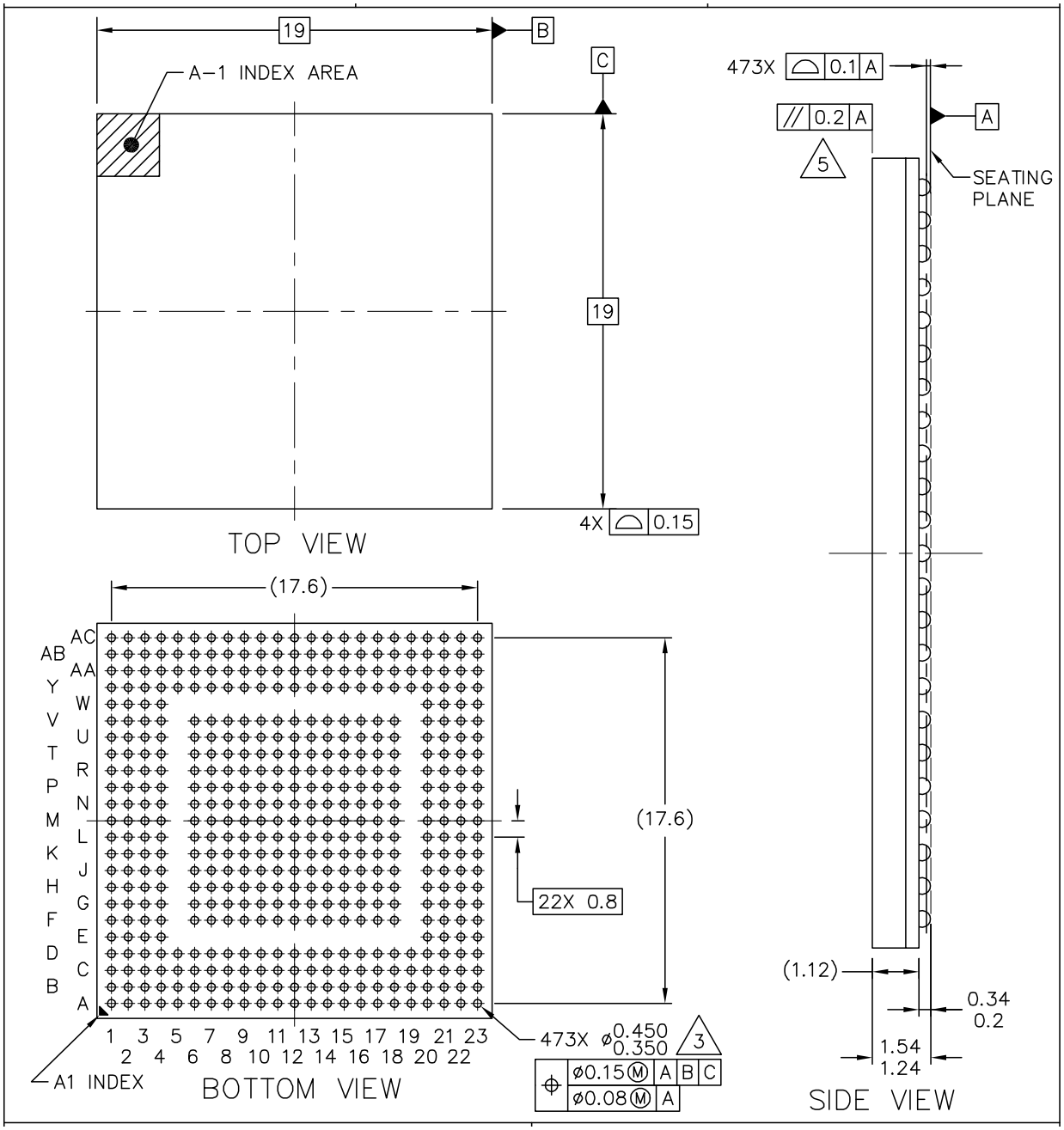



**Figure 86. Production Package: Case 1931—0.8 mm Pitch**

### 5.2.2 MAPBGA Signal Assignment–19 × 19 mm 0.8 mm

See Table 70 for the 19 × 19 mm, 0.8 mm pitch signal assignments/ball map.

### 5.2.3 Connection Tables–19 x 19 mm 0.8 mm

Table 66 shows the device connection list for power and ground, alpha-sorted followed by Table 67, which shows the no-connects. Table 68 shows the device connection list for signals.

#### 5.2.3.1 Ground and Power ID Locations—19 x 19 mm 0.8 mm

**Table 66. 19 x 19 BGA Ground/Power ID by Ball Grid Location**

| GND/PWR ID | Ball Location |
|---|---|
| FGND | U16 |
| FUSE_VDD | T15 |
| FVCC | T16 |
| GND | A1, A2, A3, A21, A22, A23, B1, B2, B22, B23, C1, C2, C22, C23, D22, D23, J12, J13, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14, R12, Y1, Y23, AA1, AA2, AA22, AA23, AB1, AB2, AB21, AB22, AB23, AC1, AC2, AC21, AC22, AC23 |
| IOQVDD | T8 |
| MGND | U14 |
| MVCC | U15 |
| NVCC1 | G15, G16, H16, J17 |
| NVCC2 | N16, P16, R15, R16, T14 |
| NVCC3 | K7, K8, L7, L8 |
| NVCC4 | H14, J15, K15 |
| NVCC5 | G9, G10, H8, H9 |
| NVCC6 | G11, G12, G13, H12 |
| NVCC7 | H15, J16, K16, L16, M16 |
| NVCC8 | H10, H11, J11 |
| NVCC9 | G14 |
| NVCC10 | P8, R7, R8, R9, T9 |
| NVCC21 | T11, T12, T13, U11 |
| NVCC22 | T10, U7, U8, U9, U10, V6, V7, V8, V9, V10 |
| QVCC | H13, J14, L15, M15, N9, N15, P9, P15, R10, R11, R13, R14 |
| QVCC1 | J8, J9, J10, K9 |
| QVCC4 | L9, M7, M8, N8 |
| SGND | U13 |
| SVCC | U12 |
| UVCC | P18 |
| UGND | P17 |

**Table 67. 19 x 19 BGA No Connects[1]**

| Signal | Ball Location |
|---|---|
| NC | N7 |
| NC | P7 |
| NC | U21 |

1 These contacts are not used and must be floated by the user.

### 5.2.3.2 BGA Signal ID by Ball Grid Location—19 x 19 0.8 mm

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location**

| Signal ID | Ball Location |
|---|---|
| A0 | Y6 |
| A1 | AC5 |
| A10 | V15 |
| A11 | AB3 |
| A12 | AA3 |
| A13 | Y3 |
| A14 | Y15 |
| A15 | Y14 |
| A16 | V14 |
| A17 | Y13 |
| A18 | V13 |
| A19 | Y12 |
| A2 | AB5 |
| A20 | V12 |
| A21 | Y11 |
| A22 | V11 |
| A23 | Y10 |
| A24 | Y9 |
| A25 | Y8 |
| A3 | AA5 |
| A4 | Y5 |
| A5 | AC4 |
| A6 | AB4 |
| A7 | AA4 |
| A8 | Y4 |
| A9 | AC3 |
| ATA_CS0 | E1 |
| ATA_CS1 | G4 |
| ATA_DIOR | E3 |
| ATA_DIOW | H6 |
| ATA_DMACK | E2 |
| $\overline{\text{ATA_RESET}}$ | F3 |
| BATT_LINE | F6 |
| BCLK | W20 |

| Signal ID | Ball Location |
|---|---|
| CKIL | E21 |
| CLKO | C20 |
| CLKSS | H17 |
| COMPARE | A20 |
| CONTRAST | N21 |
| CS0 | U17 |
| CS1 | Y22 |
| CS2 | Y18 |
| CS3 | Y19 |
| CS4 | Y20 |
| CS5 | AA21 |
| CSI_D10 | K21 |
| CSI_D11 | K22 |
| CSI_D12 | K23 |
| CSI_D13 | L20 |
| CSI_D14 | L18 |
| CSI_D15 | L21 |
| CSI_D4 | J20 |
| CSI_D5 | J21 |
| CSI_D6 | L17 |
| CSI_D7 | J22 |
| CSI_D8 | J23 |
| CSI_D9 | K20 |
| CSI_HSYNC | H22 |
| CSI_MCLK | H20 |
| CSI_PIXCLK | H23 |
| CSI_VSYNC | H21 |
| CSPI1_MISO | N2 |
| CSPI1_MOSI | N1 |
| CSPI1_SCLK | M4 |
| CSPI1_SPI_RDY | M1 |
| CSPI1_SS0 | M2 |
| CSPI1_SS1 | N6 |
| CSPI1_SS2 | M3 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| BOOT_MODE0 | F17 |
| BOOT_MODE1 | C21 |
| BOOT_MODE2 | D20 |
| BOOT_MODE3 | F18 |
| BOOT_MODE4 | E20 |
| CAPTURE | D18 |
| CAS | AA20 |
| CE_CONTROL | D12 |
| CKIH | F23 |
| CSPI3_SCLK | H7 |
| CSPI3_SPI_RDY | F4 |
| CTS1 | A9 |
| CTS2 | C12 |
| D0 | U6 |
| D1 | W4 |
| D10 | V1 |
| D11 | U4 |
| D12 | U3 |
| D13 | R6 |
| D14 | U2 |
| D15 | U1 |
| D2 | W3 |
| D3 | V4 |
| D3_CLS | P20 |
| D3_REV | P21 |
| D3_SPL | N17 |
| D4 | T7 |
| D5 | W2 |
| D6 | V3 |
| D7 | W1 |
| D8 | T6 |
| D9 | V2 |
| DCD_DCE1 | C10 |
| DCD_DTE1 | D11 |
| $\overline{DE}$ | D16 |
| DQM0 | AB19 |
| DQM1 | Y16 |
| DQM2 | AA18 |
| DQM3 | AB18 |
| DRDY0 | M17 |
| DSR_DCE1 | B10 |
| DSR_DTE1 | A11 |
| DTR_DCE1 | F10 |
| DTR_DCE2 | C11 |
| DTR_DTE1 | A10 |
| DVFS0 | E22 |
| CSPI2_MISO | B4 |
| CSPI2_MOSI | D5 |
| CSPI2_SCLK | B5 |
| CSPI2_SPI_RDY | D6 |
| CSPI2_SS0 | C5 |
| CSPI2_SS1 | A4 |
| CSPI2_SS2 | F7 |
| CSPI3_MISO | D2 |
| CSPI3_MOSI | E4 |
| GPIO1_3 | G20 |
| GPIO1_4 | D21 |
| GPIO1_5 (PWR RDY) | D19 |
| GPIO1_6 | G18 |
| GPIO3_0 | G23 |
| GPIO3_1 | K17 |
| HSYNC | L23 |
| I2C_CLK | J18 |
| I2C_DAT | K18 |
| IOIS16 | J7 |
| KEY_COL0 | A15 |
| KEY_COL1 | B15 |
| KEY_COL2 | D14 |
| KEY_COL3 | C15 |
| KEY_COL4 | F13 |
| KEY_COL5 | A16 |
| KEY_COL6 | B16 |
| KEY_COL7 | A17 |
| KEY_ROW0 | A13 |
| KEY_ROW1 | B13 |
| KEY_ROW2 | C13 |
| KEY_ROW3 | A14 |
| KEY_ROW4 | F12 |
| KEY_ROW5 | D13 |
| KEY_ROW6 | B14 |
| KEY_ROW7 | C14 |
| L2PG | See VPG1 |
| LBA | V17 |
| LCS0 | M22 |
| LCS1 | N23 |
| LD0 | R23 |
| LD1 | R22 |
| LD10 | U22 |
| LD11 | R18 |
| LD12 | U20 |
| LD13 | V23 |
| LD14 | V22 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| DVFS1 | E23 |
| EB0 | W22 |
| EB1 | W21 |
| ECB | Y21 |
| FPSHIFT | M23 |
| GPIO1_0 | C19 |
| GPIO1_1 | G17 |
| GPIO1_2 | B20 |
| LD7 | T20 |
| LD8 | R17 |
| LD9 | U23 |
| M_GRANT | U18 |
| M_REQUEST | T17 |
| MA10 | Y2 |
| MCUPG | See VPG0 |
| NFALE | T2 |
| $\overline{\text{NFCE}}$ | R4 |
| NFCLE | T1 |
| NFRB | R3 |
| $\overline{\text{NFRE}}$ | T4 |
| $\overline{\text{NFWE}}$ | T3 |
| $\overline{\text{NFWP}}$ | P6 |
| OE | T18 |
| PAR_RS | P22 |
| PC_BVD1 | G2 |
| PC_BVD2 | H4 |
| $\overline{\text{PC_CD1}}$ | J3 |
| $\overline{\text{PC_CD2}}$ | H1 |
| PC_POE | J6 |
| PC_PWRON | K6 |
| PC_READY | H2 |
| PC_RST | F1 |
| $\overline{\text{PC_RW}}$ | G3 |
| PC_VS1 | H3 |
| PC_VS2 | G1 |
| $\overline{\text{PC_WAIT}}$ | J4 |
| $\overline{\text{POR}}$ | F21 |
| POWER_FAIL | F20 |
| PWMO | F2 |
| RAS | AA19 |
| READ | N18 |
| $\overline{\text{RESET_IN}}$ | F22 |
| RI_DCE1 | D10 |
| RI_DTE1 | B11 |
| RTCK | D15 |
| RTS1 | B9 |

| Signal ID | Ball Location |
|---|---|
| LD15 | V21 |
| LD16 | V20 |
| LD17 | W23 |
| LD2 | R21 |
| LD3 | R20 |
| LD4 | T23 |
| LD5 | T22 |
| LD6 | T21 |
| SCK6 | R2 |
| SCLK0 | B19 |
| SD_D_CLK | M21 |
| SD_D_I | M20 |
| SD_D_IO | M18 |
| SD0 | AC18 |
| SD1 | AA17 |
| SD1_CLK | K2 |
| SD1_CMD | K3 |
| SD1_DATA0 | K4 |
| SD1_DATA1 | J1 |
| SD1_DATA2 | J2 |
| SD1_DATA3 | L6 |
| SD10 | AB14 |
| SD11 | AC14 |
| SD12 | AA13 |
| SD13 | AB13 |
| SD14 | AC13 |
| SD15 | AA12 |
| SD16 | AC12 |
| SD17 | AA11 |
| SD18 | AB11 |
| SD19 | AC11 |
| SD2 | AB17 |
| SD20 | AA10 |
| SD21 | AB10 |
| SD22 | AC10 |
| SD23 | AC9 |
| SD24 | AA9 |
| SD25 | AC8 |
| SD26 | AB8 |
| SD27 | AC7 |
| SD28 | AA8 |
| SD29 | AB7 |
| SD3 | AC17 |
| SD30 | AA7 |
| SD31 | AC6 |
| SD4 | AA16 |

**Table 68. 19 x 19 BGA Signal ID by Ball Grid Location (continued)**

| Signal ID | Ball Location |
|---|---|
| RTS2 | B12 |
| RW | V18 |
| RXD1 | C9 |
| RXD2 | A12 |
| SCK3 | P1 |
| SCK4 | G6 |
| SCK5 | D4 |
| SDCKE0 | Y17 |
| SDCKE1 | V16 |
| SDCLK | AC20 |
| $\overline{\text{SDCLK}}$ | AC19 |
| SDQS0 | AB16 |
| SDQS1 | AB12 |
| SDQS2 | AB9 |
| SDQS3 | AB6 |
| SDWE | AB20 |
| SER_RS | P23 |
| SFS3 | P2 |
| SFS4 | D3 |
| SFS5 | G7 |
| SFS6 | P4 |
| SIMPD0 | B18 |
| SJC_MOD | C17 |
| SRST0 | C18 |
| SRX0 | A19 |
| SRXD3 | N3 |
| SRXD4 | C3 |
| SRXD5 | C4 |
| SRXD6 | R1 |
| STX0 | F16 |
| STXD3 | N4 |
| STXD4 | B3 |
| STXD5 | D1 |
| STXD6 | P3 |
| SVEN0 | D17 |
| TCK | F14 |
| TDI | A18 |
| TDO | B17 |
| TMS | C16 |

| Signal ID | Ball Location |
|---|---|
| SD5 | AC16 |
| SD6 | AA15 |
| SD7 | AB15 |
| SD8 | AC15 |
| SD9 | AA14 |
| SDBA0 | AA6 |
| SDBA1 | Y7 |
| TRSTB | F15 |
| TXD1 | D9 |
| TXD2 | F11 |
| USB_BYP | C8 |
| USB_OC | B8 |
| USB_PWR | A8 |
| USBH2_CLK | L1 |
| USBH2_DATA0 | M6 |
| USBH2_DATA1 | K1 |
| USBH2_DIR | L2 |
| USBH2_NXT | L4 |
| USBH2_STP | L3 |
| USBOTG_CLK | D8 |
| USBOTG_DATA0 | G8 |
| USBOTG_DATA1 | C7 |
| USBOTG_DATA2 | A6 |
| USBOTG_DATA3 | F8 |
| USBOTG_DATA4 | D7 |
| USBOTG_DATA5 | B6 |
| USBOTG_DATA6 | A5 |
| USBOTG_DATA7 | C6 |
| USBOTG_DIR | A7 |
| USBOTG_NXT | B7 |
| USBOTG_STP | F9 |
| VPG0 | G21 |
| VPG1 | G22 |
| VSTBY | H18 |
| VSYNC0 | L22 |
| VSYNC3 | N20 |
| WATCHDOG_RST | B21 |
| WRITE | N22 |
| | |

## 5.3 Ball Maps

**Table 69. Ball Map—14 x 14 0.5 mm Pitch**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | SFS5 | CSPI2_MISO | CSPI2_SS2 | USBOTG_DATA7 | USBOTG_DATA3 | USBOTG_NXT | USB_BYP | RXD1 | DSR_DCE1 | DSR_DTE1 | RXD2 | CE_CONTROL | KEY_ROW3 | KEY_ROW7 | KEY_COL3 | KEY_COL7 | TDO | SJC_MOD | SVEN0 | CAPTURE | GPIO1_6 | WATCHDOG_RST | GND | GND | A |
| B | GND | GND | STXD4 | SRXD5 | CSPI2_SS0 | CSPI2_SPI_RDY | USBOTG_DATA5 | USBOTG_DATA1 | USBOTG_DIR | USB_PWR | CTS1 | DCD_DCE1 | DCD_DTE1 | RTS2 | KEY_ROW1 | KEY_ROW5 | KEY_COL1 | KEY_COL5 | TCK | TRSTB | SRX0 | SCLK0 | GPIO1_1 | GPIO1_5 | GND | GND | B |
| C | GND | GND | SRXD4 | SCK4 | STXD5 | CSPI2_SS1 | CSPI2_SCLK | USBOTG_DATA4 | USBOTG_STP | USB_OC | DTR_DCE1 | DTR_DTE1 | TXD2 | KEY_ROW2 | KEY_COL0 | KEY_COL4 | RTCK | DE | SRST0 | GPIO1_2 | BOOT_MODE1 | BOOT_MODE3 | CLKO | GND | GND | GND | C |
| D | GND | CSPI3_MOSI | SCK5 | | | | | | | | | | | | | | | | | | | | | BOOT_MODE2 | GND | BOOT_MODE4 | D |
| E | CSPI3_SCLK | ATA_DIOR | CSPI2_MOSI | | NVCC5 | | | | | | | | | | | | | | | | | GND | | GND | DVFS0 | POWER_FAIL | E |
| F | ATA_DMACK | ATA_CS1 | SFS4 | | | NVCC5 | BATT_LINE | USBOTG_DATA6 | USBOTG_DATA0 | TXD1 | RI_DCE1 | DTR_DCE2 | KEY_ROW0 | KEY_ROW6 | KEY_COL6 | TDI | STX0 | GPIO1_0 | GPIO1_4 | BOOT_MODE0 | GND | | | CKIH | GPIO1_3 | VSTBY | F |
| G | PWMO | PC_RW | CSPI3_MISO | | | CSPI3_SPI_RDY | NVCC5 | | USBOTG_DATA2 | USBOTG_CLK | RTS1 | RI_DTE1 | CTS2 | KEY_ROW4 | KEY_COL2 | TMS | SIMPD0 | COMPARE | NVCC1 | | NVCC1 | | | DVFS1 | VPG0 | CLKSS | G |
| H | PC_RST | PC_BVD1 | ATA_RESET | | | ATA_DIOW | | | | | | | | | | | | | | | CKIL | | | POR | I2C_DAT | GPIO3_1 | H |
| J | PC_VS1 | PC_READY | IOIS16 | | | ATA_CS0 | PC_POE | | | QVCC1 | QVCC1 | NVCC8 | NVCC8 | QVCC | NVCC6 | NVCC6 | NVCC9 | | | VPG1 | RESET_IN | | | I2C_CLK | CSI_VSYNC | CSI_PIXCLK | J |
| K | PC_CD2 | SD1_DATA3 | PC_PWRON | | | PC_BVD2 | PC_VS2 | | QVCC1 | | | | | | NVCC6 | | | NVCC1 | | CSI_HSYNC | GPIO3_0 | | | CSI_MCLK | CSI_D5 | CSI_D7 | K |
| L | SD1_DATA1 | SD1_CMD | SD1_DATA2 | | | PC_WAIT | PC_CD1 | | NVCC3 | | QVCC1 | GND | QVCC | QVCC | QVCC | QVCC | | NVCC4 | NVCC4 | CSI_D8 | CSI_D4 | | | CSI_D6 | CSI_D9 | CSI_D11 | L |
| M | USBH2_DATA0 | USBH2_STP | USBH2_DATA1 | | | SD1_DATA0 | SD1_CLK | | NVCC3 | | GND | GND | GND | GND | GND | GND | | QVCC | | CSI_D14 | CSI_D12 | | | CSI_D10 | CSI_D13 | CSI_D15 | M |
| N | USBH2_CLK | CSPI1_SCLK | CSPI1_SPI_RDY | | | USBH2_NXT | USBH2_DIR | | QVCC4 | | NVCC3 | GND | GND | GND | GND | GND | | NVCC7 | | SD_D_I | FPSHIFT | | | VSYNC0 | HSYNC | DRDY0 | N |
| P | CSPI1_SS1 | CSPI1_MOSI | CSPI1_SS0 | | | CSPI1_SS2 | CSPI1_MISO | | NVCC10 | | NVCC10 | GND | GND | GND | GND | GND | | NVCC7 | | READ | LCS1 | | | SD_D_CLK | SD_D_IO | LCS0 | P |
| R | STXD3 | SCK3 | SRXD3 | | | SFS3 | SRXD6 | | QVCC4 | | NVCC10 | GND | GND | GND | GND | GND | | NVCC7 | | D3_CLS | PAR_RS | | | CONTRAST | WRITE | VSYNC3 | R |
| T | STXD6 | SCK6 | SFS6 | | | NFCE | NFWE | | QVCC4 | | NVCC10 | GND | GND | SGND | MGND | UGND | | NVCC7 | | LD4 | LD2 | | | LD0 | SER_RS | D3_REV | T |
| U | NFRB | NFWP | NFCLE | | | D15 | D11 | | QVCC4 | | | | | | | | | QVCC | | TTM_PAD | LD8 | | | LD6 | D3_SPL | LD1 | U |
| V | NFALE | NFRE | D13 | | | D9 | D5 | | | QVCC | QVCC | QVCC | QVCC | SVCC | MVCC | UVCC | GND | | | LD17 | LD13 | | | LD10 | LD3 | LD5 | V |
| W | D14 | D12 | D7 | | | D3 | NVCC22 | | | | | | | | | | | | | | EB0 | | | LD15 | LD7 | LD9 | W |
| Y | D10 | D8 | D1 | | | IOQVDD | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC21 | NVCC21 | NVCC21 | NVCC2 | NVCC2 | NVCC2 | NVCC2 | M_GRANT | | | EB1 | LD11 | LD12 | Y |
| AA | D6 | D4 | A4 | | | NVCC22 | SD31 | SD28 | SD27 | SD23 | SD21 | SD18 | SD16 | SD13 | SD9 | SD7 | SD5 | SD3 | SD2 | DQM2 | SDCLK | | | FVCC | LD14 | LD16 | AA |
| AB | D2 | D0 | A6 | | A2 | | | | | | | | | | | | | | | | | RW | | FGND | OE | BCLK | AB |
| AC | MA10 | GND | A11 | | | | | | | | | | | | | | | | | | | | | FUSE_VDD | M_REQUEST | GND | AC |
| AD | GND | GND | A12 | A13 | A8 | A0 | SDBA0 | SDQS3 | SD29 | SD25 | SDQS2 | SD17 | SD15 | SD12 | SD8 | SDQS0 | SD4 | SD0 | DQM1 | CAS | SDCKE0 | CS3 | ECB | GND | GND | GND | AD |
| AE | GND | GND | A7 | A3 | SDBA1 | SD30 | SD26 | SD24 | SD22 | SD20 | SD19 | SDQS1 | SD14 | SD11 | SD10 | SD6 | SD1 | DQM3 | DQM0 | SDCLK | CS2 | LBA | CS0 | GND | GND | GND | AE |
| AF | GND | GND | A9 | A5 | A1 | A25 | A24 | A23 | A22 | A21 | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A10 | RAS | SDWE | SDCKE1 | CS5 | CS1 | CS4 | GND | GND | AF |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | |

## Table 70. Ball Map—19 x 19 0.8 mm Pitch

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | GND | CSPI2_SS1 | USBOTG_DATA6 | USBOTG_DATA2 | USBOTG_DIR | USB_PWR | CTS1 | DTR_DTE1 | DSR_DTE1 | RXD2 | KEY_ROW0 | KEY_ROW3 | KEY_COL0 | KEY_COL5 | KEY_COL7 | TDI | SRX0 | COMPARE | GND | GND | GND | A |
| B | GND | GND | STXD4 | CSPI2_MISO | CSPI2_SCLK | USBOTG_DATA5 | USBOTG_NXT | USB_OC | RTS1 | DSR_DCE1 | RI_DTE1 | RTS2 | KEY_ROW1 | KEY_ROW6 | KEY_COL1 | KEY_COL6 | TDO | SIMPD0 | SCLK0 | GPIO1_2 | WATCHDOG_RST | GND | GND | B |
| C | GND | GND | SRXD4 | SRXD5 | CSPI2_SS0 | USBOTG_DATA7 | USBOTG_DATA1 | USB_BYP | RXD1 | DCD_DCE1 | DTR_DCE2 | CTS2 | KEY_ROW2 | KEY_ROW7 | KEY_COL3 | TMS | SJC_MOD | SRST0 | GPIO1_0 | CLKO | BOOT_MODE1 | GND | GND | C |
| D | STXD5 | CSPI3_MISO | SFS4 | SCK5 | CSPI2_MOSI | CSPI2_SPI_RDY | USBOTG_DATA4 | USBOTG_CLK | TXD1 | RI_DCE1 | DCD_DTE1 | CE_CONTROL | KEY_ROW5 | KEY_COL2 | RTCK | $\overline{DE}$ | SVEN0 | CAPTURE | GPIO1_5 | BOOT_MODE2 | GPIO1_4 | GND | GND | D |
| E | ATA_CS0 | ATA_DMACK | ATA_DIOR | CSPI3_MOSI | | | | | | | | | | | | | | | | BOOT_MODE4 | CKIL | DVFS0 | DVFS1 | E |
| F | PC_RST | PWMO | $\overline{ATA_RESET}$ | CSPI3_SPI_RDY | | BATT_LINE | CSPI2_SS2 | USBOTG_DATA3 | USBOTG_STP | DTR_DCE1 | TXD2 | KEY_ROW4 | KEY_COL4 | TCK | TRSTB | STX0 | BOOT_MODE0 | BOOT_MODE3 | | POWER_FAIL | $\overline{POR}$ | $\overline{RESET_IN}$ | CKIH | F |
| G | PC_VS2 | PC_BVD1 | $\overline{PC_RW}$ | ATA_CS1 | | SCK4 | SFS5 | USBOTG_DATA0 | NVCC5 | NVCC5 | NVCC6 | NVCC6 | NVCC6 | NVCC9 | NVCC1 | NVCC1 | GPIO1_1 | GPIO1_6 | | GPIO1_3 | VPG0 | VPG1 | GPIO3_0 | G |
| H | $\overline{PC_CD2}$ | PC_READY | PC_VS1 | PC_BVD2 | | ATA_DIOW | CSPI3_SCLK | NVCC5 | NVCC5 | NVCC8 | NVCC8 | NVCC6 | QVCC | NVCC4 | NVCC7 | NVCC1 | CLKSS | VSTBY | | CSI_MCLK | CSI_VSYNC | CSI_HSYNC | CSI_PIXCLK | H |
| J | SD1_DATA1 | SD1_DATA2 | $\overline{PC_CD1}$ | $\overline{PC_WAIT}$ | | PC_POE | IOIS16 | QVCC1 | QVCC1 | QVCC1 | NVCC8 | GND | GND | QVCC | NVCC4 | NVCC7 | NVCC1 | I2C_CLK | | CSI_D4 | CSI_D5 | CSI_D7 | CSI_D8 | J |
| K | USBH2_DATA1 | SD1_CLK | SD1_CMD | SD1_DATA0 | | PC_PWRON | NVCC3 | NVCC3 | QVCC1 | GND | GND | GND | GND | GND | NVCC4 | NVCC7 | GPIO3_1 | I2C_DAT | | CSI_D9 | CSI_D10 | CSI_D11 | CSI_D12 | K |
| L | USBH2_CLK | USBH2_DIR | USBH2_STP | USBH2_NXT | | SD1_DATA3 | NVCC3 | NVCC3 | QVCC4 | GND | GND | GND | GND | GND | QVCC | NVCC7 | CSI_D6 | CSI_D14 | | CSI_D13 | CSI_D15 | VSYNC0 | HSYNC | L |
| M | CSPI1_SPI_RDY | CSPI1_SS0 | CSPI1_SS2 | CSPI1_SCLK | | USBH2_DATA0 | QVCC4 | QVCC4 | GND | GND | GND | GND | GND | GND | QVCC | NVCC7 | DRDY0 | SD_D_IO | | SD_D_I | SD_D_CLK | LCS0 | FPSHIFT | M |
| N | CSPI1_MOSI | CSPI1_MISO | SRXD3 | STXD3 | | CSPI1_SS1 | NC[1] | QVCC4 | QVCC | GND | GND | GND | GND | GND | QVCC | NVCC2 | D3_SPL | READ | | VSYNC3 | CONTRAST | WRITE | LCS1 | N |
| P | SCK3 | SFS3 | STXD6 | SFS6 | | $\overline{NFWP}$ | NC[1] | NVCC10 | QVCC | GND | GND | GND | GND | GND | QVCC | NVCC2 | UGND | UVCC | | D3_CLS | D3_REV | PAR_RS | SER_RS | P |
| R | SRXD6 | SCK6 | NFRB | $\overline{NFCE}$ | | D13 | NVCC10 | NVCC10 | NVCC10 | QVCC | QVCC | GND | QVCC | QVCC | NVCC2 | NVCC2 | LD8 | LD11 | | LD3 | LD2 | LD1 | LD0 | R |
| T | NFCLE | NFALE | $\overline{NFWE}$ | $\overline{NFRE}$ | | D8 | D4 | IOQVDD | NVCC10 | NVCC22 | NVCC21 | NVCC21 | NVCC21 | NVCC2 | FUSE_VDD | FVCC | M_REQUEST | OE | | LD7 | LD6 | LD5 | LD4 | T |
| U | D15 | D14 | D12 | D11 | | D0 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC21 | SVCC | SGND | MGND | MVCC | FGND | CS0 | M_GRANT | | LD12 | NC | LD10 | LD9 | U |
| V | D10 | D9 | D6 | D3 | | NVCC22 | NVCC22 | NVCC22 | NVCC22 | NVCC22 | A22 | A20 | A18 | A16 | A10 | SDCKE1 | LBA | RW | | LD16 | LD15 | LD14 | LD13 | V |
| W | D7 | D5 | D2 | D1 | | | | | | | | | | | | | | | | BCLK | EB1 | EB0 | LD17 | W |
| Y | GND | MA10 | A13 | A8 | A4 | A0 | SDBA1 | A25 | A24 | A23 | A21 | A19 | A17 | A15 | A14 | DQM1 | SDCKE0 | CS2 | CS3 | CS4 | ECB | CS1 | GND | Y |
| AA | GND | GND | A12 | A7 | A3 | SDBA0 | SD30 | SD28 | SD24 | SD20 | SD17 | SD15 | SD12 | SD9 | SD6 | SD4 | SD1 | DQM2 | RAS | CAS | CS5 | GND | GND | AA |
| AB | GND | GND | A11 | A6 | A2 | SDQS3 | SD29 | SD26 | SDQS2 | SD21 | SD18 | SDQS1 | SD13 | SD10 | SD7 | SDQS0 | SD2 | DQM3 | DQM0 | SDWE | GND | GND | GND | AB |
| AC | GND | GND | A9 | A5 | A1 | SD31 | SD27 | SD25 | SD23 | SD22 | SD19 | SD16 | SD14 | SD11 | SD8 | SD5 | SD3 | SD0 | $\overline{SDCLK}$ | SDCLK | GND | GND | GND | AC |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | |

1 These contacts are not used and must be floated by the user.

# 6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

*MCIMX31 Product Brief* (order number MCIMX31PB)

*MCIMX31 Reference Manual* (order number MCIMX31RM)

*MCIMX31 Chip Errata* (order number MCIMX31CE)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. ARM Ltd. documentation is available from http://www.arm.com.

# 7 Revision History

Table 71 summarizes revisions to this document since the release of Rev. 4.1.

**Table 71. Revision History**

| Rev. | Location | Revision |
|---|---|---|
| 4.3 | Table 1, "Ordering Information," on page 3 | Added a footnote and new part numbers for silicon revision 2.0.1. |
| 4.2 | Global | Replaced all references to silicon 2.0 with silicon revision 2.0.1. |
| 4.2 | Table 1, "Ordering Information," on page 3 | Added new part numbers for revision 2.0.1. |
| 4.2 | Section 1.2.1, “Feature Differences Between Mask Sets | Updated for revision 2.0.1. |
| 4.2 | Table 8, "Operating Ranges," on page 13 | Updated Core Operating voltage ranges and respective footnotes. |
| 4.2 | Table 12, "Current Consumption for –40×C to 85×C, for Silicon Revision 2.0.1," on page 16 | Updated for silicon revision 2.0.1. |
| 4.2 | Table 13, "Current Consumption for –20×C to 70×C, for Silicon Revision 2.0.1," on page 17 | Updated values for silicon revision 2.0.1. |
| 4.2 | Section 3, “Signal Descriptions | Removed reference to the TTM_PAD as it is no longer connected. |

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