



MCP37231/21-200

MCP37D31/21-200

200 Msps, 16-/14-Bit Low-Power ADC with 8-Channel MUX

Features:

- Sample Rates:
 - 200 Msps for single-channel mode
 - 200 Msps/Number of channel used
- SNR with $f_{IN} = 15$ MHz and -1 dBFS:
 - >74 dBFS for 200 Msps
- SFDR with $f_{IN} = 15$ MHz and -1 dBFS:
 - >90 dBFS at 200 Msps
- Power Dissipation with LVDS Digital I/O:
 - 490 mW for 200 Msps
- Power Dissipation with CMOS Digital I/O:
 - 436 mW for 200 Msps, Output Clock = 100 MHz
- Power Dissipation Excluding Digital I/O:
 - 390 mW for 200 Msps
- Power Saving modes:
 - 80 mW during Standby
 - 33 mW during Shutdown
- Supply Voltage:
 - Digital Section: 1.2V, 1.8V
 - Analog Section: 1.2V, 1.8V
- Selectable Input Range: up to 2.98 V_{P-P}
- Input Channel Bandwidth: 500 MHz
- Channel-to-Channel Crosstalk: >95 dB in Multi-Channel mode (Input = 15 MHz, -1 dBFS)
- Output Data Format:
 - Parallel CMOS, DDR LVDS
 - Serialized DDR LVDS (16-bit, octal-channel mode)
- Optional Output Data Randomizer

- Digital Signal Post-Processing (DSPP) Options:
 - Decimation Filters for improved SNR
 - Fractional Delay Recovery (FDR) for time-delay corrections in multi-channel operations (dual/octal-channel modes)
 - Phase, Offset and Gain adjust of individual channels
 - Digital Down-Conversion (DDC) with I/Q or $f_s/8$ output (MCP37D31/21-200)
 - Continuous Wave Beamforming for octal-channel mode (MCP37D31/21-200)
- Built-In ADC Linearity Calibration Algorithms:
 - Harmonic Distortion Correction (HDC)
 - DAC Noise Cancellation (DNC)
 - Dynamic Element Matching (DEM)
 - Flash Error Calibration
- Serial Peripheral Interface (SPI)
- Package Options:
 - VTLA-124 (9 mm x 9 mm x 0.9 mm)
 - TFBGA-121 (8 mm x 8 mm x 1.08 mm)
- No External Reference Decoupling Capacitor Required for TFBGA Package
- Industrial Temperature Range: -40°C to +85°C

Typical Applications:

- Communication Instruments
- Cellular Base Stations
- Radar
- Ultrasound and Sonar Imaging
- Scanners and Low-Power Portable Instruments
- Industrial and Consumer Data Acquisition System

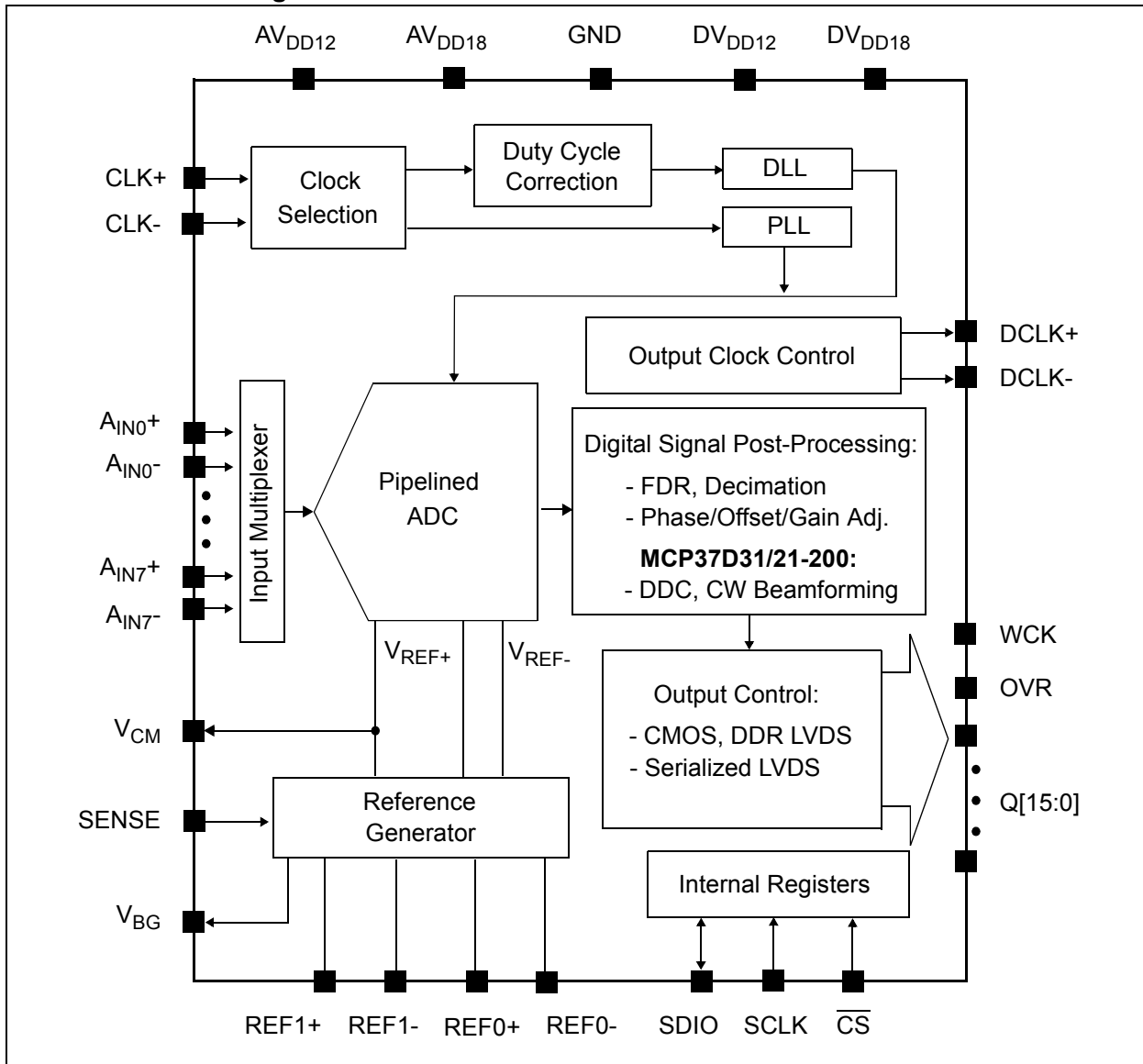
Device Offering (Note 1):

| Part Number | Sample Rate | Resolution | Decimation | Digital Down-Conversion | CW Beamforming |
|--------------|-------------|------------|------------|-------------------------|----------------|
| MCP37231-200 | 200 Msps | 16 | Yes | No | No |
| MCP37221-200 | 200 Msps | 14 | Yes | No | No |
| MCP37D31-200 | 200 Msps | 16 | Yes | Yes | Yes |
| MCP37D21-200 | 200 Msps | 14 | Yes | Yes | Yes |

Note 1: For 14-bit devices and TFBGA package, contact Microchip Technology Inc. for availability. The devices in the same package type are pin-compatible.

MCP37231/21-200 AND MCP37D31/21-200

Functional Block Diagram



MCP37231/21-200 AND MCP37D31/21-200

Description:

The MCP37231/21-200 is Microchip's baseline 16-/14-bit 200 Msps pipelined ADC family, featuring a built-in high-order digital decimation filter, gain and offset adjustment per channel, and fractional delay recovery.

The MCP37D31/21-200 device family features a digital down-conversion and CW beamforming capability, in addition to the features offered by the MCP37231/21-200.

All devices feature harmonic distortion correction and DAC noise cancellation that enable high-performance specifications with SNR of greater than 74 dBFS, and SFDR of greater than 90 dBFS.

These A/D converters exhibit industry leading low-power performance with only 490 mW operation while using the LVDS interface at 200 Msps. This superior low-power operation coupled with high dynamic performance makes these devices ideal for various high-performance, high-speed data acquisition systems including communications equipment, radar and portable instrumentation.

The output decimation filter option improves SNR performance up to 93.5 dBFS with the 512x decimation setting. The digital down-conversion option in conjunction with the decimation and quadrature output options offer great flexibility in digital communication system design, including cellular base-stations and narrow-band communications. Gain, phase and DC offset can be adjusted independently for each input channel, allowing for simplified implementation of CW beamforming and ultrasound Doppler imaging applications.

These devices can have up to eight differential input channels through an input MUX. The sampling rate is up to 200 Msps when a single channel is used, or 25 Msps per channel when all 8-input channels are used.

The differential full-scale analog input range is programmable up to 2.975 V_{P-P}. The ADC output data can be coded in two's complement or offset binary representation, with or without the data randomizer option. The output data is available as full rate CMOS or double data rate (DDR) LVDS. Additionally, a serialized LVDS option is also available for the 16-bit octal-channel mode.

The device is available in a Pb-free VTLA-124 and TFBGA-121 packages. The device operates over the commercial temperature range of -40°C to +85°C.

Package Types

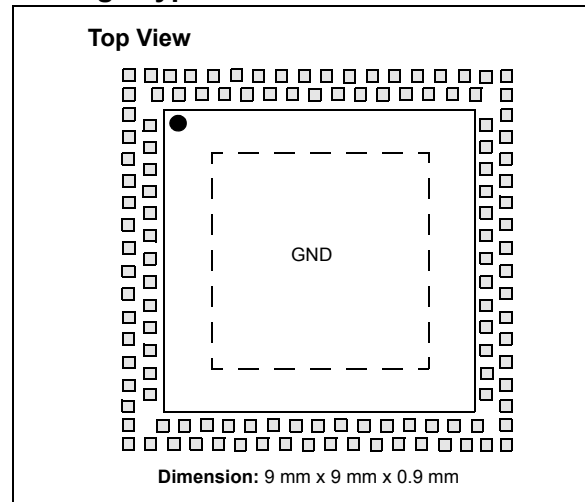


FIGURE 1: VTLA-124 Package.

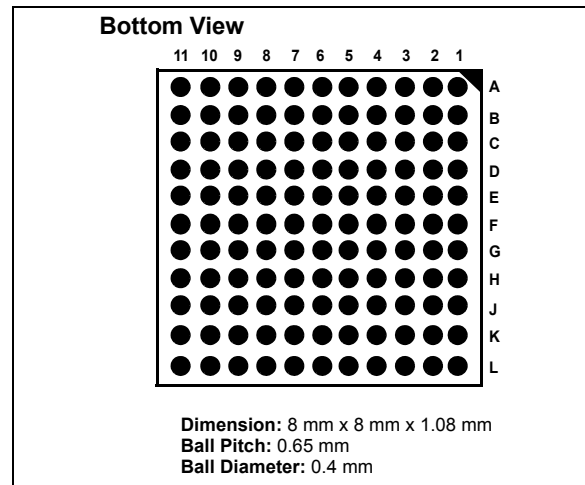


FIGURE 2: TFBGA-121 Package.
(Contact Microchip Technology Inc. for availability)

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124

| Pin No. | Name | I/O Type | Description |
|---|--------------------|------------------------------|---|
| Power Supply Pins | | | |
| A2, A22, A65, B1, B52 | AV _{DD18} | Supply | Supply voltage input (1.8V) for analog section |
| A12, A56, A60, A63, B10, B11, B12, B13, B15, B16, B45, B49, B53 | AV _{DD12} | | Supply voltage input (1.2V) for analog section |
| A25, A30, B39 | DV _{DD12} | | Supply voltage input (1.2V) for digital section |
| A41, B24, B27, B31, B36, B43 | DV _{DD18} | | Supply voltage input (1.8V) for digital section and all digital I/O |
| EP | GND | | Exposed pad: Common ground pin for digital and analog sections |
| ADC Analog Input Pins | | | |
| A3 | A _{IN6+} | Analog Input | Channel 6 differential analog input (+) |
| B2 | A _{IN6-} | | Channel 6 differential analog input (-) |
| A4 | A _{IN2+} | | Channel 2 differential analog input (+) |
| B3 | A _{IN2-} | | Channel 2 differential analog input (-) |
| A5 | A _{IN4+} | | Channel 4 differential analog input (+) |
| B4 | A _{IN4-} | | Channel 4 differential analog input (-) |
| A6 | A _{IN0+} | | Channel 0 differential analog input (+) |
| B5 | A _{IN0-} | | Channel 0 differential analog input (-) |
| B6 | A _{IN1+} | | Channel 1 differential analog input (+) |
| A8 | A _{IN1-} | | Channel 1 differential analog input (-) |
| B7 | A _{IN7+} | | Channel 7 differential analog input (+) |
| A9 | A _{IN7-} | | Channel 7 differential analog input (-) |
| B8 | A _{IN3+} | | Channel 3 differential analog input (+) |
| A10 | A _{IN3-} | | Channel 3 differential analog input (-) |
| B9 | A _{IN5+} | | Channel 5 differential analog input (+) |
| A11 | A _{IN5-} | | Channel 5 differential analog input (-) |
| A21 | CLK+ | | Differential clock input (+) |
| B17 | CLK- | Differential clock input (-) | |
| Reference Pins (Note 1) | | | |
| A57, B46 | REF1+ | Analog Output | Differential reference 1 (+) voltage |
| A58, B47 | REF1- | | Differential reference 1 (-) voltage |
| A61, B50 | REF0+ | | Differential reference 0 (+) voltage |
| A62, B51 | REF0- | | Differential reference 0 (-) voltage |
| SENSE, Bandgap and Common Mode Voltage Pins | | | |
| B48 | SENSE | Analog Input | Analog input full-scale range selection. See Table 4-2 for SENSE voltage settings. |
| A59 | V _{BG} | Analog Output | Internal bandgap output voltage Connect a decoupling capacitor (2.2 μF) |
| A7 | V _{CMIN} | Analog Input | Common-Mode voltage input for auto-calibration Connect V _{CM} voltage (Note 2) |
| A55 | V _{CM} | | Common-Mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 μF) (Note 3) |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

| Pin No. | Name | I/O Type | Description |
|---------------------------------|---------------------------|--------------------------|---|
| Digital I/O Pins | | | |
| B18 | ADR0 | Digital Input | SPI address selection pin (A0 bit). Tie to GND or DV _{DD18} . (Note 4) |
| A23 | SLAVE | | Not used. Tie to GND. |
| B19 | SYNC | Digital Input/ Output | Not used. Leave this pin floating. |
| B21 | $\overline{\text{RESET}}$ | Digital Input | Reset control input: High: Normal operating mode Low: Reset mode (Note 5) |
| A26 | CAL | Digital Output | Calibration status flag digital output: High: Calibration is complete Low: Calibration is not complete (Note 6) |
| B22 | DCLK+ | | LVDS: Differential digital clock output (+) CMOS: Digital clock output (Note 7) |
| A27 | DCLK- | | LVDS: Differential digital clock output (-) CMOS: Unused (leave floating) |
| ADC Output Pins (Note 8) | | | |
| B23 | DM2/DM- | Digital Output | 18-bit mode: Digital data output (last two LSB bits) (Note 9) Other modes: Not used |
| A28 | DM1/DM+ | | |
| A29 | Q0/Q0- | | Digital data output: CMOS = Q0 DDR LVDS = Q0- (Even bit first), Q8- (MSB byte first) Serialized LVDS = Q- for the last selected channel (n=8) |
| B25 | Q1/Q0+ | | Digital data output: CMOS = Q1 DDR LVDS = Q0+ (Even bit first), Q8+ (MSB byte first) Serialized LVDS = Q+ for the last selected channel (n=8) |
| B26 | Q2/Q1- | | Digital data output: CMOS = Q2 DDR LVDS = Q1- (Even bit first), Q9- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 7 |
| A31 | Q3/Q1+ | | Digital data output: CMOS = Q3 DDR LVDS = Q1+ (Even bit first), Q9+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 7 |
| B30 | Q4/Q2- | | Digital data output: CMOS = Q4 DDR LVDS = Q2- (Even bit first), Q10- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 6 |
| A38 | Q5/Q2+ | | Digital data output: CMOS = Q5 DDR LVDS = Q2+ (Even bit first), Q10+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 6 |
| A39 | Q6/Q3- | | Digital data output: CMOS = Q6 DDR LVDS = Q3- (Even bit first), Q11- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 5 |
| B32 | Q7/Q3+ | | Digital data output: CMOS = Q7 DDR LVDS = Q3+ (Even bit first), Q11+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 5 |
| A40 | Q8/Q4- | | Digital data output: CMOS = Q8 DDR LVDS = Q4- (Even bit first), Q12- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 4 |
| B33 | Q9/Q4+ | | Digital data output: CMOS = Q9 DDR LVDS = Q4+ (Even bit first), Q12+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 4 |
| B34 | Q10/Q5- | | Digital data output: CMOS = Q10 DDR LVDS = Q5- (Even bit first), Q13- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 3 |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

| Pin No. | Name | I/O Type | Description |
|--|-----------------|----------------------|--|
| A42 | Q11/Q5+ | Digital Output | Digital data output: CMOS = Q11 DDR LVDS = Q5+ (Even bit first), Q13+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 3 |
| B35 | Q12/Q6- | | Digital data output: CMOS = Q12 DDR LVDS = Q6- (Even bit first), Q14- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 2 |
| A43 | Q13/Q6+ | | Digital data output: CMOS = Q13 DDR LVDS = Q6+ (Even bit first), Q14+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 2 |
| A44 | Q14/Q7- | | Digital data output: CMOS = Q14 DDR LVDS = Q7- (Even bit first), Q15- (MSB byte first) Serialized LVDS = Q- for the first selected channel (n = 1) |
| B37 | Q15/Q7+ | | Digital data output: CMOS = Q15 DDR LVDS = Q7+ (Even bit first), Q15+ (MSB byte first) Serialized LVDS = Q+ for the first selected channel (n = 1) |
| B38 | WCK/OVR+ (OVR) | | WCK: Word clock sync digital output OVR: Input over-range indication digital output (Note 10). |
| A45 | WCK/OVR- (WCK) | | |
| SPI Interface Pins | | | |
| A53 | SDIO | Digital Input/Output | SPI data input/output |
| A54 | SCLK | Digital Input | SPI serial clock input |
| B44 | \overline{CS} | | SPI Chip Select input |
| Not Connected Pins | | | |
| A1, A13 - A20, A32 - A37, A46 - A52, A66 - A68, B14, B28, B29, B40, B41, B42, B55, B56 | NC | | These pins can be tied to ground or left floating. |
| Pins that need to be grounded | | | |
| A24, A64, B20, B54 | GND | | These pins are not supply pins, but need to be tied to ground. |

Notes:

1. These pins are internal reference voltage outputs. They should not be driven. External decoupling circuits are required. See [Section 4.5.3 “Decoupling Circuits for Internal Voltage Reference and Band Gap Output”](#) for details.
2. V_{CMIN} is used for Auto-Calibration only. V_{CMIN+} and V_{CMIN-} should be tied together always. There should be no voltage difference between the two pins. Typically both V_{CMIN+} and V_{CMIN-} are tied to the V_{CM} output pin together, but they can be tied to another common mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
3. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), V_{CM} pin should be decoupled with a 0.1 μF capacitor, and should be directly tied to V_{CMIN+} and V_{CMIN-} pins.
4. ADR1 (for A1 bit) is internally bonded to GND ('0'). If ADR0 is dynamically controlled, ADR0 must be held constant while \overline{CS} is "Low".
5. The device is in Reset mode while this pin stays "Low". On the rising edge of \overline{RESET} , the device exits the Reset mode, initializes all internal user registers to default values, and begins power-up calibration.
6. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or Soft

MCP37231/21-200 AND MCP37D31/21-200

Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.

7. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the DSPP, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D ([Registers 5-7](#), [5-21](#) and [5-27](#)) for more details.
8. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first", which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 ([Register 5-19](#)). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12, Q14) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15) appear when DCLK+ is "Low". See Addresses 0x65 ([Register 5-22](#)) and 0x68 ([Register 5-25](#)) for output polarity control. See [Figures 2-2 to 2-4](#) for LVDS output timing diagrams.
9. **18-bit mode:** DM1/DM+ and DM2/DM- are the last LSB bits. DM2/DM- is the LSB. In LVDS output, DM1/DM+ and DM2/DM- are the LSB pair. DM1/DM+ appears at the falling edge and DM2/DM- is at the rising edge of the DCLK+.
When 18-bit mode is not selected: DM1/DM+ and DM2/DM- are High Z in LVDS mode and driven "Low" in CMOS mode. These pins can be connected to GND or left floating (No Connect).
10. **CMOS output mode:** WCK/OVR+ is OVR and WCK/OVR- is WCK.
DDR LVDS output mode: The rising edge of DCLK+ is OVR and the falling edge is WCK.
OVR: OVR will be held "High" when analog input over-range is detected. Digital post-processing will cause OVR to assert early relative to the output data. See [Figure 2-2](#) for LVDS timing of these bits.
WCK: Normally "Low". "High" while data from the first channel is sent out. In serialized LVDS (octal) output mode, the WCK output is asserted "High" on the MSB bit.

MCP37231/21-200 AND MCP37D31/21-200

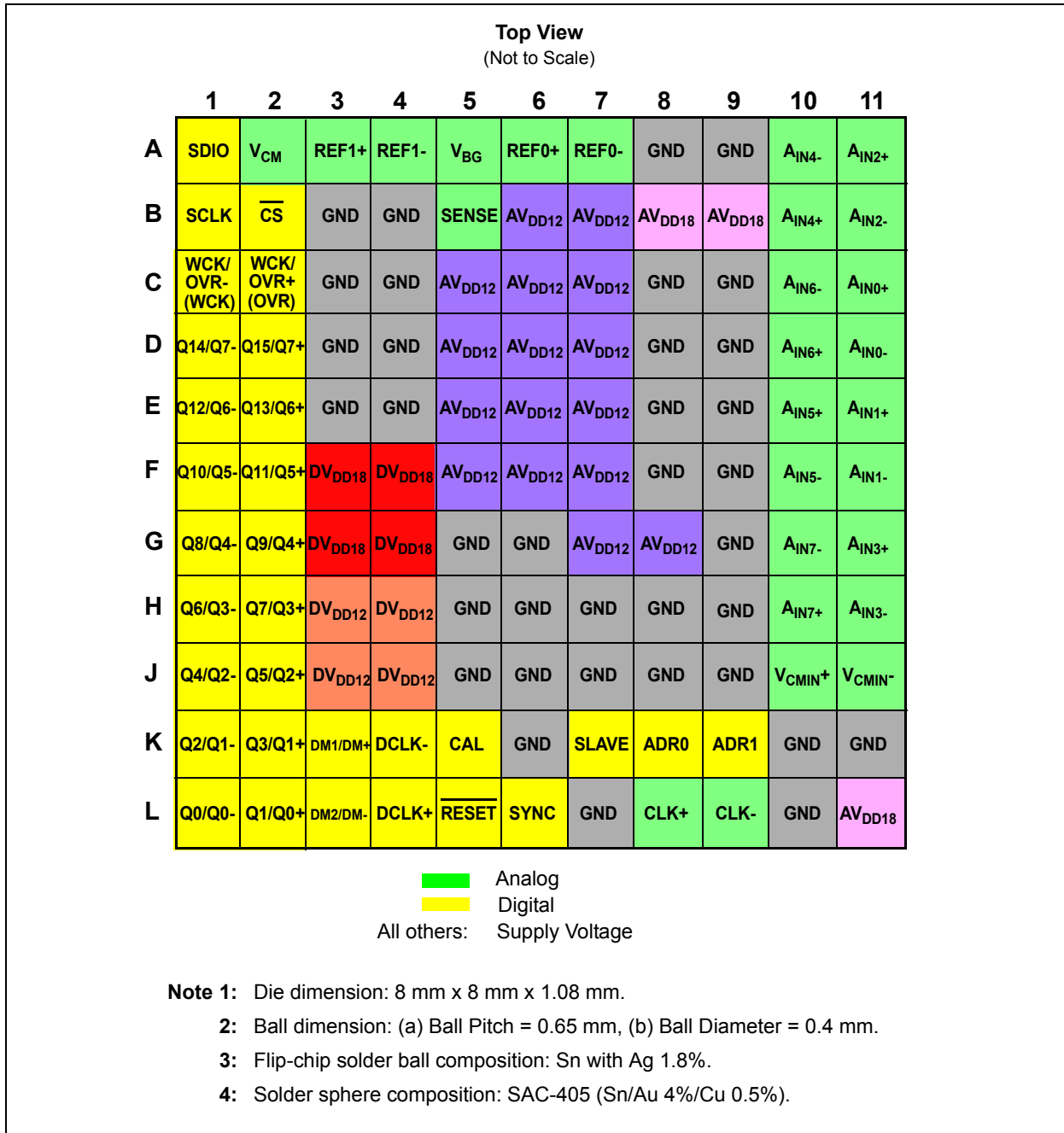


FIGURE 1-2: TFBGA-121 Package. See [Table 1-2](#) for the pin descriptions and [Table 1-3](#) for active and inactive ADC output pins for various ADC resolution modes. Decoupling capacitors for reference pins and V_{BG} are embedded in the package.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121

| Ball No. | Name | I/O Type | Description | | |
|----------|------------------------|--------------------------|---|---|--|
| A1 | SDIO | Digital Input/ Output | SPI data input/output | | |
| A2 | V _{CM} | Analog Output | Common-Mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 µF) (Note 1) | | |
| A3 | REF1+ | | Differential reference voltage 1 (+/-). Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating. | | |
| A4 | REF1- | | | | |
| A5 | V _{BG} | | Internal bandgap output voltage A decoupling capacitor (2.2 µF) is embedded in the TFBGA package. Leave this pin floating. | | |
| A6 | REF0+ | | Differential reference 0 (+/-) voltage. Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating. | | |
| A7 | REF0- | | | | |
| A8 | GND | | Supply | Common ground for analog and digital sections | |
| A9 | | | | | |
| A10 | A _{IN4-} | Analog Input | Channel 4 differential analog input (-) | | |
| A11 | A _{IN2+} | | Channel 2 differential analog input (+) | | |
| B1 | SCLK | Digital Input | SPI serial clock input | | |
| B2 | $\overline{\text{CS}}$ | | SPI Chip Select input | | |
| B3 | GND | Supply | Common ground for analog and digital sections | | |
| B4 | | | | | |
| B5 | SENSE | Analog Input | Analog input range selection. See Table 4-2 for SENSE voltage settings. | | |
| B6 | AV _{DD12} | Supply | Supply voltage input (1.2V) for analog section | | |
| B7 | | | | | |
| B8 | AV _{DD18} | Supply | Supply voltage input (1.8V) for analog section | | |
| B9 | | | | | |
| B10 | A _{IN4+} | Analog Input | Channel 4 differential analog input (+) | | |
| B11 | A _{IN2-} | | Channel 2 differential analog input (-) | | |
| C1 | WCK/OVR- (WCK) | Digital Output | WCK: Word clock sync digital output OVR: Input over-range indication digital output (Note 2) | | |
| C2 | WCK/OVR+ (OVR) | | | | |
| C3 | GND | Supply | Common ground for analog and digital sections | | |
| C4 | | | | | |
| C5 | | | | AV _{DD12} | Supply voltage input (1.2V) for analog section |
| C6 | | | | | |
| C7 | | | | | |
| C8 | GND | Supply | Common ground pin for analog and digital sections | | |
| C9 | | | | | |
| C10 | A _{IN6-} | Analog Input | Channel 6 differential analog input (-) | | |
| C11 | A _{IN0+} | | Channel 0 differential analog input (+) | | |
| D1 | Q14/Q7- | Digital Output | Digital data output: (Note 3) CMOS = Q14 DDR LVDS = Q7- (Even bit first), Q15- (MSB byte first) Serialized LVDS = Q- for the first selected channel (n = 1) | | |
| D2 | Q15/Q7+ | | Digital data output: (Note 3) CMOS = Q15 DDR LVDS = Q7+ (Even bit first), Q15+ (MSB byte first) Serialized LVDS = Q+ for the first selected channel (n = 1) | | |
| D3 | GND | Supply | Common ground for analog and digital sections | | |
| D4 | | | | | |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

| Ball No. | Name | I/O Type | Description |
|----------|--------------------|----------------|---|
| D5 | AV _{DD12} | Supply | Supply voltage input (1.2V) for analog section |
| D6 | | | |
| D7 | | | |
| D8 | GND | | Common ground for analog and digital sections |
| D9 | | | |
| D10 | A _{IN6+} | Analog Input | Channel 6 differential analog input (+) |
| D11 | A _{IN0-} | | Channel 0 differential analog input (-) |
| E1 | Q12/Q6- | Digital Output | Digital data output: (Note 3) CMOS = Q12 DDR LVDS = Q6- (Even bit first), Q14- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 2 |
| E2 | Q13/Q6+ | | Digital data output: (Note 3) CMOS = Q13 DDR LVDS = Q6+ (Even bit first), Q14+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 2 |
| E3 | GND | Supply | Common ground for analog and digital sections |
| E4 | | | |
| E5 | AV _{DD12} | | Supply voltage input (1.2V) for analog section |
| E6 | | | |
| E7 | | | |
| E8 | GND | | Common ground for analog and digital sections |
| E9 | | | |
| E10 | A _{IN5+} | Analog Input | Channel 5 differential analog input (+) |
| E11 | A _{IN1+} | | Channel 1 differential analog input (+) |
| F1 | Q10/Q5- | Digital Output | Digital data output: (Note 3) CMOS = Q10 DDR LVDS = Q5- (Even bit first), Q13- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 3 |
| F2 | Q11/Q5+ | | Digital data output: (Note 3) CMOS = Q11 DDR LVDS = Q5+ (Even bit first), Q13+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 3 |
| F3 | DV _{DD18} | Supply | Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV _{DD18} potential. |
| F4 | | | |
| F5 | AV _{DD12} | | Supply voltage input (1.2V) for analog section |
| F6 | | | |
| F7 | | | |
| F8 | GND | | Common ground for analog and digital sections |
| F9 | | | |
| F10 | A _{IN5-} | Analog Input | Channel 5 differential analog input (-) |
| F11 | A _{IN1-} | | Channel 1 differential analog input (-) |
| G1 | Q8/Q4- | Digital Output | Digital data output: (Note 3) CMOS = Q8 DDR LVDS = Q4- (Even bit first), Q12- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 4 |
| G2 | Q9/Q4+ | | Digital data output: (Note 3) CMOS = Q9 DDR LVDS = Q4+ (Even bit first), Q12+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 4 |
| G3 | DV _{DD18} | Supply | Supply voltage input (1.8V) for digital section |
| G4 | | | All digital input pins are driven by the same DV _{DD18} potential |
| G5 | GND | | Common ground for analog and digital sections |
| G6 | | | |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

| Ball No. | Name | I/O Type | Description | |
|----------|--------------------|---|---|---|
| G7 | AV _{DD12} | Supply | Supply voltage input (1.2V) for analog section | |
| G8 | | | | |
| G9 | | | GND | Common ground for analog and digital sections |
| G10 | A _{IN7-} | Analog Input | Channel 7 differential analog input (-) | |
| G11 | A _{IN3+} | | Channel 3 differential analog input (+) | |
| H1 | Q6/Q3- | Digital Output | Digital data output: (Note 3) CMOS = Q6 DDR LVDS = Q3- (Even bit first), Q11- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 5 | |
| H2 | Q7/Q3+ | | Digital data output: (Note 3) CMOS = Q7 DDR LVDS = Q3+ (Even bit first), Q11+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 5 | |
| H3 | DV _{DD12} | Supply | Supply voltage input (1.2V) for digital section | |
| H4 | | | | |
| H5 | | | GND | Common ground for analog and digital sections |
| H6 | | | | |
| H7 | | | | |
| H8 | | | | |
| H9 | | | | |
| H10 | | | A _{IN7+} | Analog Input |
| H11 | A _{IN3-} | Channel 3 differential analog input (-) | | |
| J1 | Q4/Q2- | Digital Output | Digital data output: (Note 3) CMOS = Q4 DDR LVDS = Q2- (Even bit first), Q10- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 6 | |
| J2 | Q5/Q2+ | | Digital data output: (Note 3) CMOS = Q5 DDR LVDS = Q2+ (Even bit first), Q10+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 6 | |
| J3 | DV _{DD12} | Supply | DC supply voltage input pin for digital section (1.2V) | |
| J4 | | | | |
| J5 | | | GND | Common ground for analog and digital sections |
| J6 | | | | |
| J7 | | | | |
| J8 | | | | |
| J9 | | | | |
| J10 | V _{CMIN+} | Analog Input | Common-Mode voltage input for auto-calibration (Note 4) These two pins should be tied together and connected to V _{CM} voltage. | |
| J11 | V _{CMIN-} | | | |
| K1 | Q2/Q1- | Digital Output | Digital data output: (Note 3) CMOS = Q2 DDR LVDS = Q1- (Even bit first), Q9- (MSB byte first) Serialized LVDS = Q- for channel order (n) = 7 | |
| K2 | Q3/Q1+ | | Digital data output: (Note 3) CMOS = Q3 DDR LVDS = Q1+ (Even bit first), Q9+ (MSB byte first) Serialized LVDS = Q+ for channel order (n) = 7 | |
| K3 | DM1/DM+ | | 18-bit mode: Digital data output. DM1 and DM2 are the last two LSB bits (Note 5) Other modes: Not used | |
| K4 | DCLK- | | LVDS: Differential digital clock output (-) CMOS: Unused (leave floating) | |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

| Ball No. | Name | I/O Type | Description |
|----------|---------|--------------------------|--|
| K5 | CAL | Digital Output | Calibration status flag digital output (Note 6): High: Calibration is complete Low: Calibration is not complete |
| K6 | GND | Supply | Common ground pin for analog and digital sections |
| K7 | SLAVE | Digital Input | Not used. Tie this pin to GND |
| K8 | ADRO | | SPI address selection pin (A0 bit). Tie to GND or DVDD18 (Note 7) |
| K9 | ADR1 | | SPI address selection pin (A1 bit). Tie to GND or DVDD18 (Note 7) |
| K10 | GND | Supply | Common ground for analog and digital sections |
| K11 | | | |
| L1 | Q0/Q0- | Digital Output | Digital data output: (Note 3) CMOS = Q0 DDR LVDS = Q0- (Even bit first), Q8- (MSB byte first) Serialized LVDS = Q- for the last selected channel (n=8) |
| L2 | Q1/Q0+ | | Digital data output: (Note 8) CMOS = Q1 DDR LVDS = Q0+ (Even bit first), Q8+ (MSB byte first) Serialized LVDS = Q+ for the last selected channel (n=8) |
| L3 | DM2/DM- | | 18-bit mode: Digital data output. DM1 and DM2 are the last two LSB bits (Note 5) Other modes: Not used |
| L4 | DCLK+ | | LVDS: Differential digital clock output (+) CMOS: Digital clock output (Note 8) |
| L5 | RESET | Digital Input | Reset control input: High: Normal operating mode Low: Reset mode (Note 9) |
| L6 | SYNC | Digital Input/ Output | Not used. Leave this pin floating |
| L7 | GND | Supply | Common ground for analog and digital sections |
| L8 | CLK+ | Analog Input | Differential clock input (+) |
| L9 | CLK- | | Differential clock input (-) |
| L10 | GND | Supply | Common ground for analog and digital sections |
| L11 | AVDD18 | Analog Input | Supply voltage input (1.8V) for analog section |

Notes:

- When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), V_{CM} pin should be decoupled with a 0.1 μ F capacitor, and should be directly tied to V_{CMIN+} and V_{CMIN-} pins.
- CMOS output mode:** WCK/OVR- is WCK and WCK/OVR+ is OVR.
DDR LVDS output mode: The rising edge of DCLK+ is OVR and the falling edge is WCK.
OVR: OVR will be held "High" when analog input over-range is detected. Digital post-processing will cause OVR to assert early relative to the output data. See [Figure 2-2](#) for LVDS timing of these bits.
WCK: Normally "Low". "High" while data from the first channel is sent out. In serialized LVDS (octal) output mode, the WCK output is asserted "High" on the MSB bit.
- DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first", which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 ([Register 5-19](#)). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12, Q14) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15) appear when DCLK+ is "Low". See Addresses 0x65 ([Register 5-22](#)) and 0x68 ([Register 5-25](#)) for output polarity control. See [Figures 2-2 to 2-4](#) for LVDS output timing diagrams.
- V_{CMIN} is used for Auto-Calibration only. V_{CMIN+} and V_{CMIN-} should be tied together always. There should be no voltage difference between the two pins. Typically both V_{CMIN+} and V_{CMIN-} are tied to the V_{CM} output pin together, but they can be tied to another common mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
- 18-bit mode:** DM1/DM+ and DM2/DM- are the last LSB bits. DM2/DM- is the LSB. In LVDS output, DM1/DM+ and DM2/DM- are the LSB pair. DM1/DM+ appears at the falling edge and DM2/DM- is at the rising edge of the DCLK+.

MCP37231/21-200 AND MCP37D31/21-200

When 18-bit mode is not selected: DM1/DM+ and DM2/DM- are High Z in LVDS mode and driven "Low" in CMOS mode. These pins can be connected to GND or left floating (No Connect).

6. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or Soft Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes this pin will maintain the prior condition.
7. In most applications, the Address pin will be tied to either GND or DV_{DD18} . If the SPI address is dynamically controlled, the Address pin must be held constant while \overline{CS} is "Low".
8. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital post-processing, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D ([Registers 5-7](#), [5-21](#) and [5-27](#)) for more details.
9. The device is in Reset mode while this pin stays "Low". On the rising edge of \overline{RESET} , the device exits the Reset mode, initializes all internal user registers to default values, and begins power-up calibration.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 1-3: DATA OUTPUT PINS FOR EACH RESOLUTION OPTION

| ADC Resolution | Output Pin Name | | | | | | | | | | | | | | | | | |
|----------------|---|-------------|-------------|-------------|-------------|-------------|------------|------------|-------------------------|------------|-------------------------|------------|------------|------------|-------------------------|------------|-------------------------|-------------|
| | Q15/ Q7+ | Q14/ Q7- | Q13/ Q6+ | Q12/ Q6- | Q11/ Q5+ | Q10/ Q5- | Q9/ Q4+ | Q8/ Q4- | Q7/ Q3+ | Q6/ Q3- | Q5/ Q2+ | Q4/ Q2- | Q3/ Q1+ | Q2/ Q1- | Q1/ Q0+ | Q0/ Q0- | DM1/ DM+ | DM2/ DM- |
| 18-bit mode | Q15 pin is MSB (bit 17), and DM2 is LSB (bit 0) | | | | | | | | | | | | | | | | | |
| 16-bit mode | Q15 pin is MSB, and Q0 is LSB | | | | | | | | | | | | | | | | Not used ⁽¹⁾ | |
| 14-bit mode | Q15 pin is MSB, and Q2 is LSB | | | | | | | | | | | | | | Not used ⁽¹⁾ | | | |
| 12-bit mode | Q15 pin is MSB, and Q4 is LSB | | | | | | | | | | Not used ⁽¹⁾ | | | | | | | |
| 10-bit mode | Q15 pin is MSB, and Q6 is LSB | | | | | | | | Not used ⁽¹⁾ | | | | | | | | | |

- Note 1:** Output condition at “not-used” output pin:
- '0' in CMOS mode. These pins can be grounded or left floating.
 - High Z state in LVDS mode.

MCP37231/21-200 AND MCP37D31/21-200

2.0 ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings†

| | |
|--|--------------------------------------|
| Analog and Digital Supply Voltage (AV_{DD12} , DV_{DD12})..... | -0.3V to 1.32V |
| Analog and Digital Supply Voltage (AV_{DD18} , DV_{DD18})..... | -0.3V to 1.98V |
| All inputs and outputs w.r.t GND | -0.3V to $AV_{DD18} + 0.3V$ |
| Differential Input Voltage | $ AV_{DD18} - GND $ |
| Current at Input Pins | ± 2 mA |
| Current at Output and Supply Pins | ± 250 mA |
| Storage Temperature | -65°C to +150°C |
| Ambient Temp. with power applied | -55°C to +125°C |
| Maximum Junction Temperature (T_J)..... | +150°C |
| ESD protection on all pins..... | 2 kV HBM |
| Solder Reflow Profile | See Microchip Application Note AN233 |

Notice†: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Electrical Specifications

TABLE 2-1: ELECTRICAL CHARACTERISTICS

| Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $GND = 0\text{V}$, $SENSE = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $DCLK_PHDLY_DEC<2:0> = 000$, $+25^\circ\text{C}$ is applied for typical value. | | | | | | |
|---|--------------------|-----------------------------|------|------|-------------|---|
| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
| Power Supply Requirements | | | | | | |
| Analog Supply Voltage | AV_{DD18} | 1.71 | 1.8 | 1.89 | V | |
| | AV_{DD12} | 1.14 | 1.2 | 1.26 | V | |
| Digital Supply Voltage | DV_{DD18} | 1.71 | 1.8 | 1.89 | V | Note 1 |
| | DV_{DD12} | 1.14 | 1.2 | 1.26 | V | |
| Analog Supply Current | | | | | | |
| Analog Supply Current during Conversion | I_{DD_A18} | — | 27 | 46 | mA | at AV_{DD18} Pin |
| | I_{DD_A12} | — | 185 | 252 | mA | at AV_{DD12} Pin |
| Digital Supply Current | | | | | | |
| Digital Supply Current during Conversion | I_{DD_D12} | — | 97 | 226 | mA | at DV_{DD12} Pin |
| Digital I/O Current in CMOS Output Mode | I_{DD_D18} | — | 27 | — | mA | at DV_{DD18} Pin $DCLK = 100\text{ MHz}$ |
| Digital I/O Current in LVDS Mode | I_{DD_D18} | Measured at DV_{DD18} Pin | | | | |
| | | — | 55 | 81 | mA | 3.5 mA mode |
| | | — | 39 | — | mA | 1.8 mA mode |
| — | — | 69 | — | — | 5.4 mA mode | |
| Supply Current during Power Saving Modes | | | | | | |
| During Standby Mode | $I_{STANDBY_AN}$ | — | 21 | — | mA | Address $0x00<4:3> = 1, 1$. (Note 2) |
| | $I_{STANDBY_DIG}$ | — | 41 | — | mA | |
| During Shutdown Mode | I_{DD_SHDN} | — | 25 | — | mA | Address $0x00<7,0> = 1, 1$ (Note 3) |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^{\circ}\text{C}$ is applied for typical value.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions | |
|---|---------------------|------|----------------------------|-------------|---------------|--|---|
| PLL Circuit | | | | | | | |
| PLL Circuit Current | I_{DD_PLL} | — | 21 | — | mA | PLL enabled. Included in analog supply current specification. | |
| Total Power Dissipation (Note 4) | | | | | | | |
| Power Dissipation during conversion, excluding digital I/O | P_{DISS_ADC} | — | 387 | 689.2 | mW | | |
| Total Power Dissipation during conversion with CMOS output mode | P_{DISS_CMOS} | — | 436 | — | mW | $f_S = 200\text{ Msps}$, $\text{DCLK} = 100\text{ MHz}$ | |
| Total Power Dissipation during conversion with LVDS output mode | P_{DISS_LVDS} | — | 486 | 842.3 | mW | 3.5 mA mode | |
| | | | 457 | — | | 1.8 mA mode | |
| | | | 511 | — | | 5.4 mA mode | |
| During Standby Mode | $P_{DISS_STANDBY}$ | — | 80.4 | — | mW | Address $0x00<4:3> = 1, 1$ (Note 2) | |
| During Shutdown Mode | P_{DISS_SHDN} | — | 33 | — | mW | Address $0x00<7:0> = 1, 1$ (Note 3) | |
| Power-On Reset (POR) Voltage | | | | | | | |
| Threshold Voltage | V_{POR} | — | 800 | — | mV | Applicable to AV_{DD12} only. (POR tracks AV_{DD12}) | |
| Hysteresis | V_{POR_HYST} | — | 40 | — | mV | | |
| SENSE Input (Note 5), (Note 7) | | | | | | | |
| SENSE Input Voltage | V_{SENSE} | GND | — | AV_{DD12} | V | V_{SENSE} selects reference | |
| SENSE Pin Input Resistance | R_{IN_SENSE} | — | 500 | — | Ω | To virtual ground at 0.55V. $400\text{ mV} < V_{SENSE} < 800\text{ mV}$ | |
| Current Sink into SENSE Pin | I_{SENSE} | — | 500 | — | μA | $\text{SENSE} = 0.8\text{V}$ | |
| Reference and Common Mode Voltages | | | | | | | |
| Internal Reference Voltage (Selected by V_{SENSE}) | V_{REF} | — | 0.74 | — | V | $V_{SENSE} = \text{GND}$ | |
| | | | 1.49 | — | | $V_{SENSE} = AV_{DD12}$ | |
| | | | $1.86 \times V_{SENSE}$ | — | | $400\text{ mV} < V_{SENSE} < 800\text{ mV}$ | |
| Common Mode Voltage Output | V_{CMD} | — | 0.9 | — | V | Available at V_{CM} pin. | |
| Reference Voltage Output (Note 7, Note 8) | V_{REF1} | — | 0.4 | — | V | $V_{SENSE} = \text{GND}$ | |
| | | | 0.8 | — | | $V_{SENSE} = AV_{DD12}$ | |
| | | | 0.4 - 0.8 | — | | $400\text{ mV} < V_{SENSE} < 800\text{ mV}$ | |
| | V_{REF0} | — | — | 0.7 | — | V | $V_{SENSE} = \text{GND}$ |
| | | | | 1.4 | — | | $V_{SENSE} = AV_{DD12}$ |
| | | | | 0.7 - 1.4 | — | | $400\text{ mV} < V_{SENSE} < 800\text{ mV}$ |
| Bandgap Voltage Output | V_{BG} | — | 0.55 | — | V | Available at V_{BG} pin. | |
| Analog Inputs | | | | | | | |
| Full Scale Differential Analog Input Range (Note 5, Note 7) | A_{FS} | — | 1.4875 | — | V_{P-P} | $V_{SENSE} = \text{GND}$ | |
| | | | 2.975 | — | | $V_{SENSE} = AV_{DD12}$ | |
| | | | $3.71875 \times V_{SENSE}$ | — | | $400\text{ mV} < V_{SENSE} < 800\text{ mV}$ | |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^\circ\text{C}$ is applied for typical value.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--|----------------|------|-----------|----------|-------------------|--------------------------------|
| Analog Input Bandwidth | f_{IN_3dB} | — | 500 | — | MHz | $A_{IN} = -3\text{ dBFS}$ |
| Differential Input Capacitance | C_{IN} | 5 | 6 | 7 | pF | (Note 5, Note 9) |
| Analog Input Channel Cross-Talk | XTALK | — | 100 | — | dBc | (Note 10) |
| Analog Input Leakage Current (A_{IN+} , A_{IN-} pins) | I_{LI_AH} | — | — | +1 | μA | $V_{IH} = AV_{DD12}$ |
| | I_{LI_AL} | -1 | — | — | μA | $V_{IL} = \text{GND}$ |
| ADC Conversion Rate (Note 11) | | | | | | |
| Conversion Rate | f_S | 40 | — | 200 | MSPS | Tested at 200 Msps |
| Clock Inputs (CLK+, CLK-) (Note 12) | | | | | | |
| Clock Input Frequency | f_{CLK} | — | — | 250 | MHz | Note 5 |
| Differential Input Voltage | V_{CLK_IN} | 300 | — | 800 | mV _{P-P} | Note 5 |
| Clock Jitter | CLK_{JITTER} | — | 175 | — | f_{SRMS} | Note 5 |
| Clock Input Duty Cycle (Note 5) | | 49 | 50 | 51 | % | Duty cycle correction disabled |
| | | 30 | 50 | 70 | % | Duty cycle correction enabled |
| Input Leakage Current at CLK input pin | I_{LI_CLKH} | — | — | +110 | μA | $V_{IH} = AV_{DD12}$ |
| | I_{LI_CLKL} | -10 | — | — | μA | $V_{IL} = \text{GND}$ |
| Converter Accuracy (Note 6) | | | | | | |
| ADC Resolution (with no missing code) | | — | — | 16 | bits | MCP37231/MCP37D31 |
| | | — | — | 14 | bits | MCP37221/MCP37D21 (Note 15) |
| Offset Error | | — | ± 5 | ± 61 | LSB | MCP37231/MCP37D31 |
| Gain Error | G_{ER} | — | ± 0.5 | — | % of FS | |
| Integral Nonlinearity | INL | — | ± 2 | — | LSB | MCP37231/MCP37D31 |
| | | — | ± 0.5 | — | LSB | MCP37221/MCP37D21 (Note 15) |
| Differential Nonlinearity | DNL | — | ± 0.4 | — | LSB | MCP37231/MCP37D31 |
| | | — | ± 0.1 | — | LSB | MCP37221/MCP37D21 (Note 15) |
| Analog Input Common-Mode Rejection Ratio | $CMRR_{DC}$ | — | 70 | — | dB | DC measurement |
| DC Power Supply Rejection Ratio (PSRR) | $PSRR_{DC}$ | — | -117 | — | dB | DC measurement |
| Dynamic Accuracy (Note 6) | | | | | | |
| Spurious Free Dynamic Range (for all resolutions) | SFDR | 78 | 90 | — | dBc | $f_{IN} = 15\text{ MHz}$ |
| | | 77 | 85 | — | dBc | $f_{IN} = 70\text{ MHz}$ |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^\circ\text{C}$ is applied for typical value.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|----------------------------------|-------------------|------------------|-----------------|-------|--|
| Signal-to-Noise Ratio (for all resolutions) | SNR $f_{IN} = 15\text{ MHz}$ | 73.3 | 74.7 | — | dBFS | MCP37231/MCP37D31 |
| | | — | 74.2 | — | dBFS | MCP37221/MCP37D21 (Note 15) |
| | SNR $f_{IN} = 70\text{ MHz}$ | — | 74.2 | — | dBFS | MCP37231/MCP37D31 |
| | | — | 73.7 | — | dBFS | MCP37221/MCP37D21 (Note 15) |
| Effective Number of Bits (ENOB) (Note 13) | ENOB $f_{IN} = 15\text{ MHz}$ | — | 12.1 | — | bits | MCP37231/MCP37D31 |
| | | — | 12 | — | bits | MCP37221/MCP37D21 (Note 15) |
| | ENOB $f_{IN} = 70\text{ MHz}$ | — | 12 | — | bits | MCP37231/MCP37D31 |
| | | — | 11.7 | — | bits | MCP37221/MCP37D21 (Note 15) |
| Total Harmonic Distortion (for all resolutions, first 13 harmonics) | THD | 78 | 89 | — | dBc | $f_{IN} = 15\text{ MHz}$ |
| | | 77 | 82 | — | dBc | $f_{IN} = 70\text{ MHz}$ |
| Worst Second or Third Harmonic Distortion | HD2 or HD3 | — | 90 | — | dBc | $f_{IN} = 15\text{ MHz}$ |
| | | — | 83 | — | dBc | $f_{IN} = 70\text{ MHz}$ |
| Two-Tone Intermodulation Distortion $f_{IN1} = 15\text{ MHz}$, $f_{IN2} = 17\text{ MHz}$ | IMD | — | 90.5 | — | dBc | $A_{IN} = -7\text{ dBFS}$, with two input frequencies |
| Digital Logic Input and Output (Except LVDS Output) | | | | | | |
| Schmitt Trigger High-Level Input voltage | V_{IH} | $0.7 DV_{DD18}$ | — | DV_{DD18} | V | |
| Schmitt Trigger Low-Level input voltage | V_{IL} | GND | — | $0.3 DV_{DD18}$ | V | |
| Hysteresis of Schmitt Trigger Inputs (All digital inputs) | V_{HYST} | — | $0.05 DV_{DD18}$ | — | V | |
| Low-Level output voltage | V_{OL} | — | — | 0.3 | V | $I_{OL} = -3\text{ mA}$, all digital I/O pins |
| High-Level output voltage | V_{OH} | $DV_{DD18} - 0.5$ | 1.8 | — | V | $I_{OL} = +3\text{ mA}$, all digital I/O pins |
| Digital Data Output (CMOS Mode) | | | | | | |
| Maximum External Load Capacitance | C_{LOAD} | — | 10 | — | pF | From output pin to GND |
| Internal I/O Capacitance | C_{INT} | — | 4 | — | pF | Note 5 |
| Digital Data Output (LVDS Mode) (Note 5) | | | | | | |
| LVDS High Level Differential Output Voltage | V_{H_LVDS} | 200 | 300 | 400 | mV | 100 Ω differential termination, LVDS bias = 3.5 mA |
| LVDS Low Level Differential Output Voltage | V_{L_LVDS} | -400 | -300 | -200 | mV | 100 Ω differential termination, LVDS bias = 3.5 mA |
| LVDS Common Mode Voltage | V_{CM_LVDS} | 1 | 1.15 | 1.4 | V | |

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^{\circ}\text{C}$ is applied for typical value.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|--|-----------------|------|------|------|---------------|---|
| Output Capacitance | C_{INT_LVDS} | — | 4 | — | pF | Internal capacitance from output pin to GND |
| Differential Load Resistance (LVDS) | R_{LVDS} | — | 100 | — | Ω | Across LVDS output pairs |
| Input Leakage Current on Digital I/O Pins | | | | | | |
| Data Output Pins | I_{LI_DH} | — | — | +1 | μA | $V_{IH} = DV_{DD18}$ |
| | I_{LI_DL} | -1 | — | — | μA | $V_{IL} = \text{GND}$ |
| I/O Pins except Data Output Pins | I_{LI_DH} | — | — | +6 | μA | $V_{IH} = DV_{DD18}$ |
| | I_{LI_DL} | -35 | — | — | μA | $V_{IL} = \text{GND}$ (Note 14) |

Notes:

1. This 1.8V digital supply voltage is used for the digital I/O circuit, including SPI, CMOS and LVDS data output drivers.
2. Standby Mode: Most of the internal circuits are turned off except internal reference, clock, bias circuits and SPI interface.
3. Shutdown Mode: All circuits including reference and clock are turned-off except the SPI interface.
4. The total power dissipation is calculated by using the following equation:
 $P_{DISS} = 1.8\text{V} \times (I_{DD_A18} + I_{DD_D18}) + 1.2\text{V} \times (I_{DD_A12} + I_{DD_D12})$, where I_{DD_D18} is the digital I/O current for LVDS or CMOS output.
5. This parameter is ensured by design, and not 100% tested.
6. This parameter is ensured by characterization, and not 100% tested.
7. See [Table 4-2](#) for details.
8. Differential reference voltage output at REF1+/- and REF0+/- pins. $V_{REF1} = V_{REF1+} - V_{REF1-}$.
 $V_{REF0} = V_{REF0+} - V_{REF0-}$. These references should not be driven.
9. Input capacitance refers to the effective capacitance between one differential input pin pair.
10. Channel Cross-talk is measured when $A_{IN} = -1\text{ dBFS}$ at 12 MHz is applied on one channel while other channel(s) are terminated with 50 Ω . See [Figure 3-86](#) and [Section 6](#) for details.
11. ADC core conversion rate. In multi-channel mode, the conversion rate of an individual channel is f_S/N , where N is the number of input channels used.
12. See [Figure 4-8](#) for details of clock input circuit.
13. $\text{ENOB} = (\text{SINAD} - 1.76)/6.02$.
14. This leakage current is due to internal pull-up resistor.
15. Not released. Contact Microchip Technology Inc. for availability.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-2: TIMING REQUIREMENTS - LVDS AND CMOS OUTPUTS

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_s = 200\text{ Msp}$ s (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^{\circ}\text{C}$ is applied for typical value.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|------------------|-------|----------|-------|--------|---|
| Aperture Delay | t_A | — | 1 | — | ns | Note 1 |
| Out-of-Range Recovery Time | t_{OVR} | — | 1 | — | Clocks | Note 1 |
| Output Clock Duty Cycle | | — | 50 | — | % | Note 1 |
| Pipeline Latency | $T_{LATENCY}$ | — | 28 | — | Clocks | Note 2, Note 4 |
| System Calibration (Note 1) | | | | | | |
| Power-Up Calibration Time | T_{PCAL} | — | 2^{27} | — | Clocks | First 2^{27} sample clocks after power-up |
| Background Calibration Update Rate | T_{BCAL} | — | 2^{30} | — | Clocks | Per 2^{30} sample clocks after T_{PCAL} |
| $\overline{\text{RESET}}$ Low Time | T_{RESET} | 5 | — | — | ns | See Figure 2-8 for details. (Note 1) |
| LVDS Data Output Mode | | | | | | |
| Input Clock to Output Clock Propagation Delay | t_{CPD} | — | — | 3.2 | ns | |
| Output Clock to Data Propagation Delay | t_{DC} | -0.25 | — | +0.25 | ns | Note 1 |
| Input Clock to Output Data Propagation Delay | t_{PD} | — | — | 3.25 | ns | |
| Rise Time (20% to 80% of output amplitude) (Note 2, Note 3) | t_{RISE_DATA} | — | 0.25 | 0.5 | ns | |
| | t_{RISE_CLK} | — | 0.25 | 0.5 | ns | |
| Fall Time (80% to 20% of output amplitude) (Note 2, Note 3) | t_{FALL_DATA} | — | 0.25 | 0.5 | ns | |
| | t_{FALL_CLK} | — | 0.25 | 0.5 | ns | |
| CMOS Data Output Mode | | | | | | |
| Input Clock to Output Clock Propagation Delay | t_{CPD} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| Output Clock to Data Propagation Delay | t_{DC} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| Input Clock to Output Data Propagation Delay | t_{PD} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| Rise Time (20% to 80% of output amplitude) | t_{RISE_DATA} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| | t_{RISE_CLK} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| Fall Time (80% to 20% of output amplitude) | t_{FALL_DATA} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |
| | t_{FALL_CLK} | | TBD | | ns | DCLK=100 MHz, $f_s = 200\text{ Msp}$ s |

Note 1: This parameter is ensured by design, but not tested 100% in production.

Note 2: This parameter is ensured by characterization, but not tested 100% in production.

Note 3: t_{RISE} = approximately less than 10% of duty cycle.

Note 4: Output latency is measured without using decimation filter and digital down-converter options.

MCP37231/21-200 AND MCP37D31/21-200

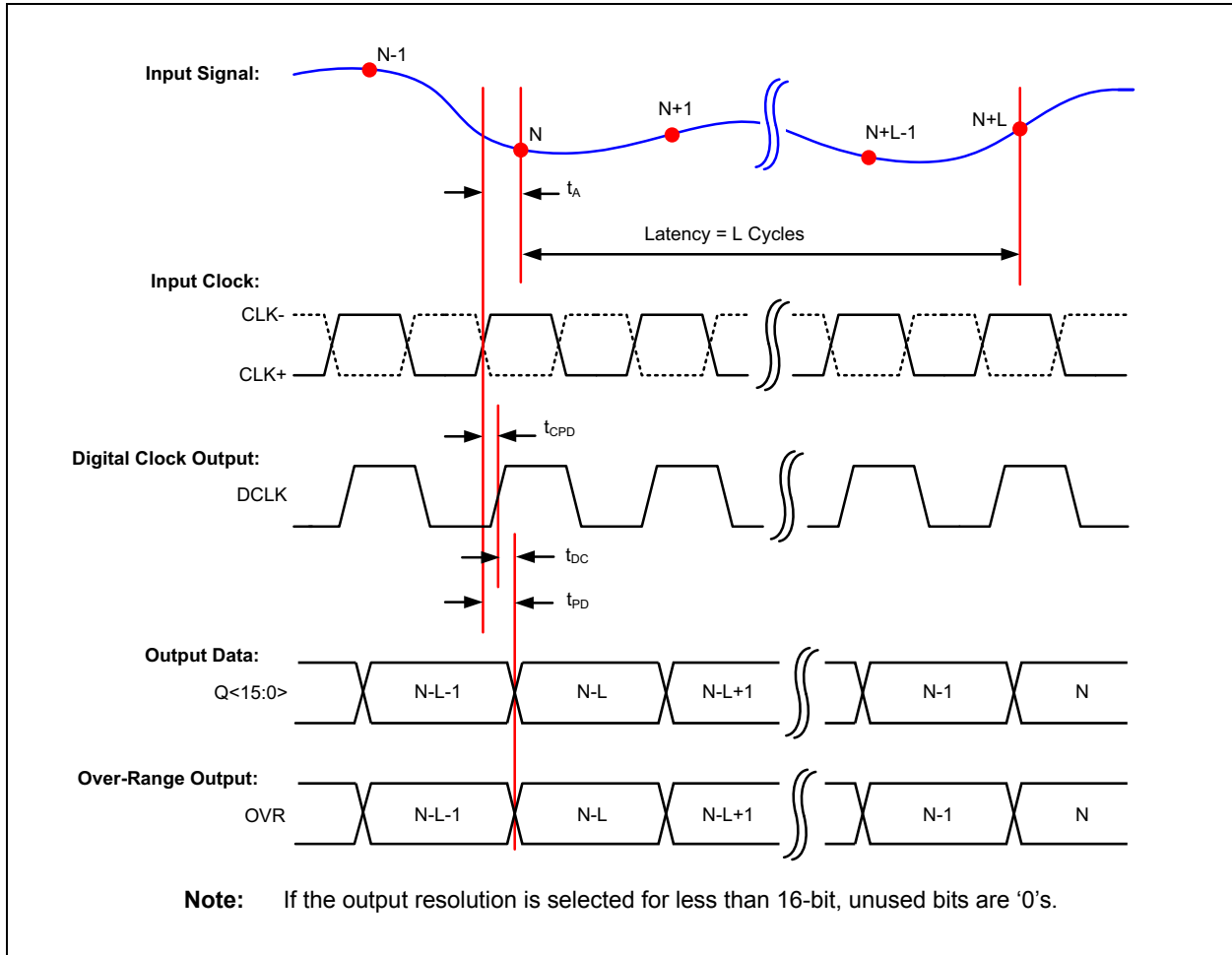


FIGURE 2-1: Timing Diagram - CMOS Output.

MCP37231/21-200 AND MCP37D31/21-200

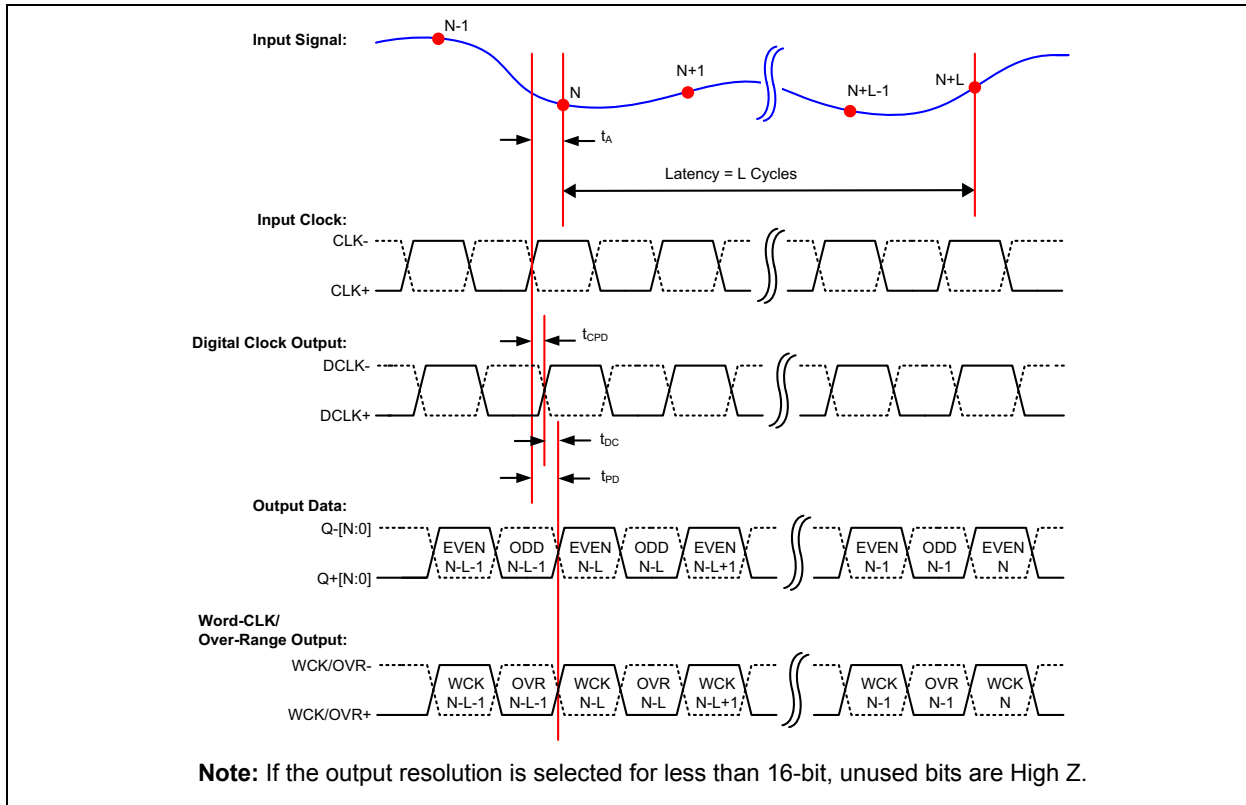


FIGURE 2-2: Timing Diagram - LVDS Output with Even Bit First Option.

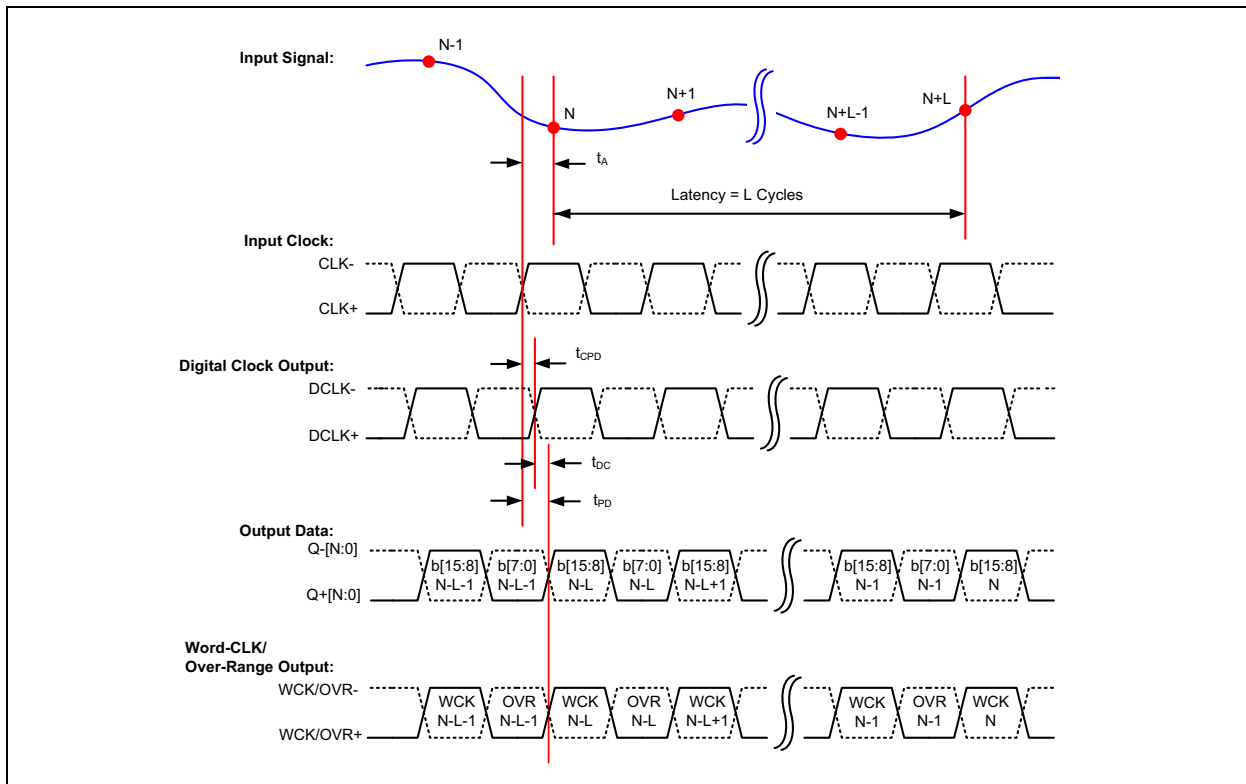


FIGURE 2-3: Timing Diagram - LVDS Output with MSB Byte First Option. This output option is available for 16-bit mode only.

MCP37231/21-200 AND MCP37D31/21-200

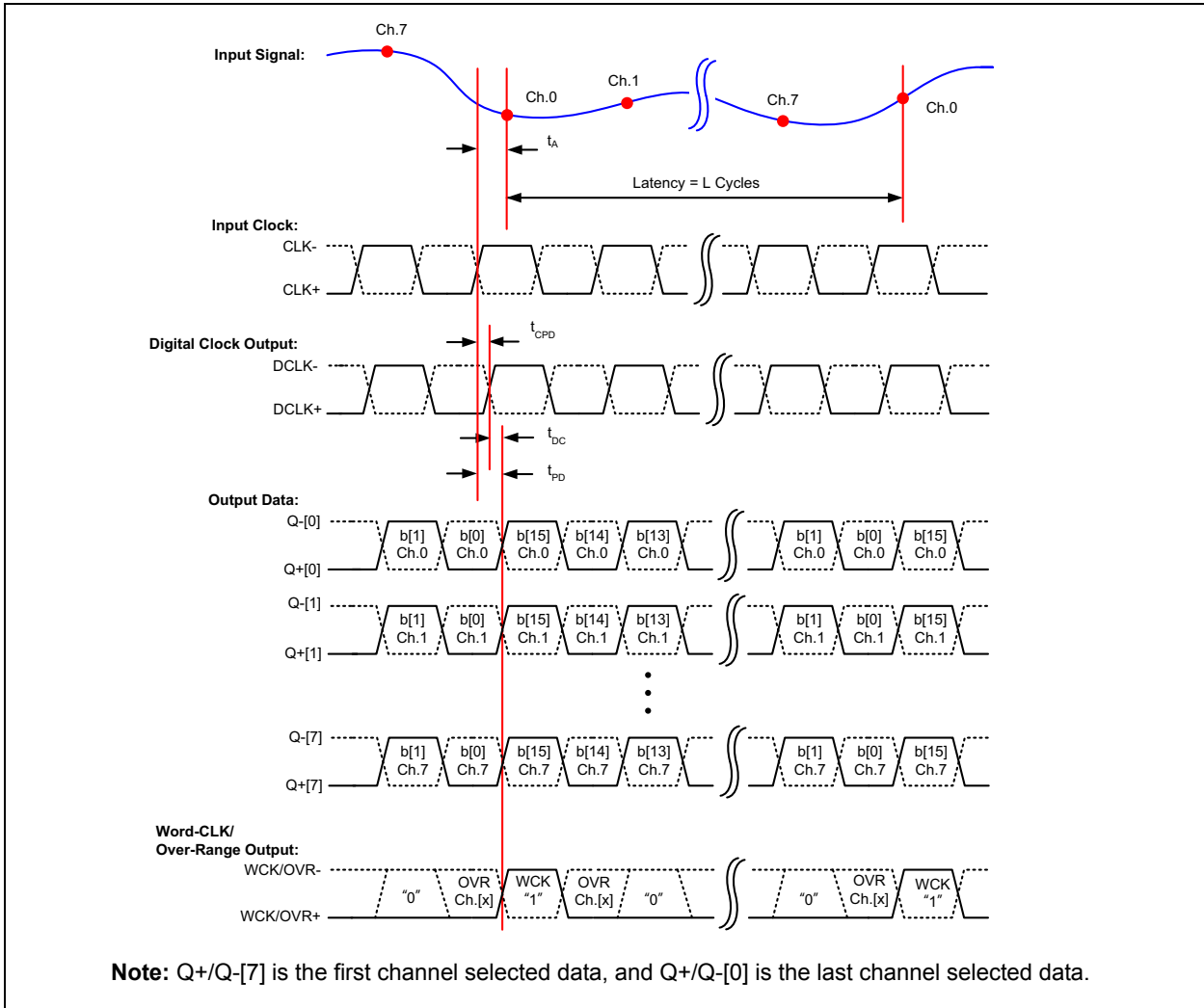


FIGURE 2-4: Timing Diagram - LVDS Serial Output in Octal-Channel Mode. This output is available for octal-channel with 16-bit mode only.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 2-3: SPI SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC}<2:0> = 000$, $+25^\circ\text{C}$ is applied for typical value. All timings are measured at 50%.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|-----------|------|------|------|-------|------------|
| Serial Clock frequency, $f_{SCK} = 50\text{ MHz}$ | | | | | | |
| $\overline{\text{CS}}$ setup time | t_{CSS} | 10 | — | — | ns | |
| $\overline{\text{CS}}$ hold time | t_{CSH} | 20 | — | — | ns | |
| $\overline{\text{CS}}$ disable time | t_{CSD} | 20 | — | — | ns | |
| Data setup time | t_{SU} | 2 | — | — | ns | |
| Data hold time | t_{HD} | 4 | — | — | ns | |
| Serial Clock high time | t_{HI} | 8 | — | — | ns | |
| Serial Clock low time | t_{LO} | 8 | — | — | ns | Note 1 |
| Serial Clock delay time | t_{CLD} | 20 | — | — | ns | |
| Serial Clock enable time | t_{CLE} | 20 | — | — | ns | |
| Output valid from SCK low | t_{DO} | — | — | 20 | ns | |
| Output disable time | t_{DIS} | — | — | 10 | ns | Note 1 |

Note 1: This parameter is ensured by design, and not 100% tested.

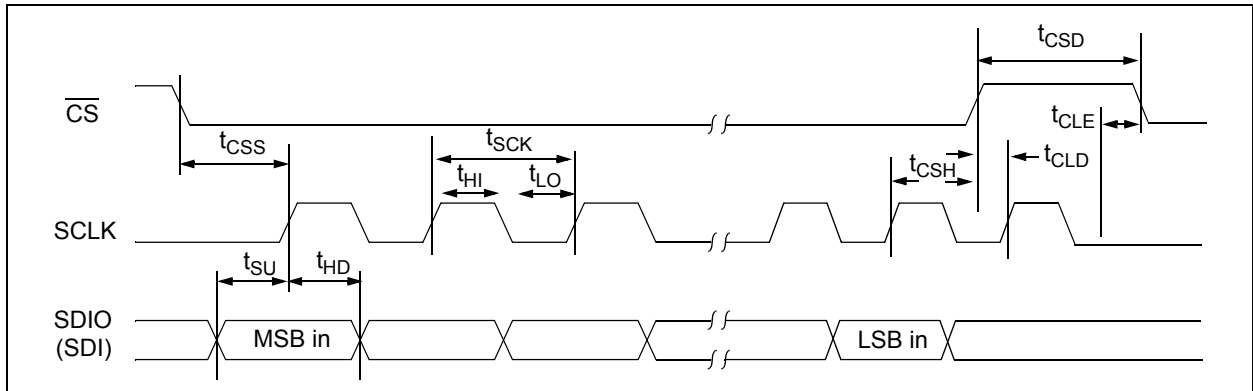


FIGURE 2-5: SPI Serial Input Timing Diagram.

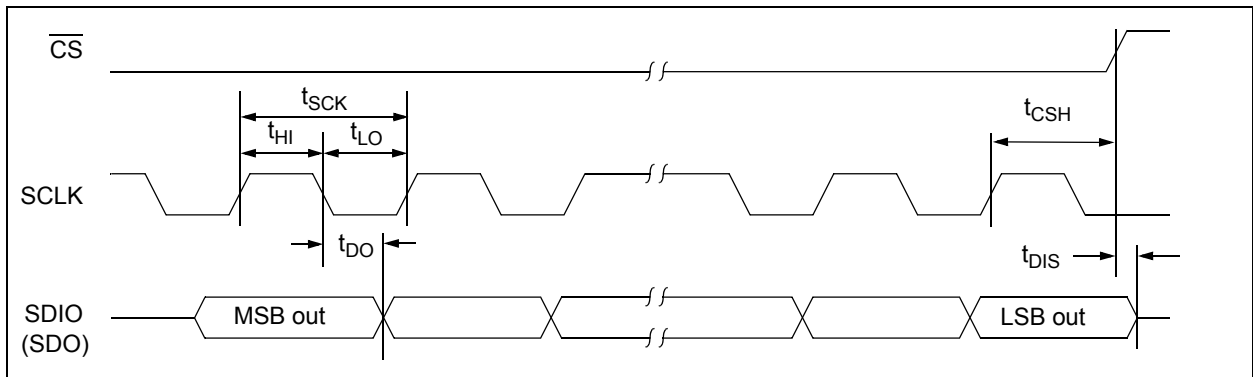


FIGURE 2-6: SPI Serial Output Timing Diagram.

MCP37231/21-200 AND MCP37D31/21-200

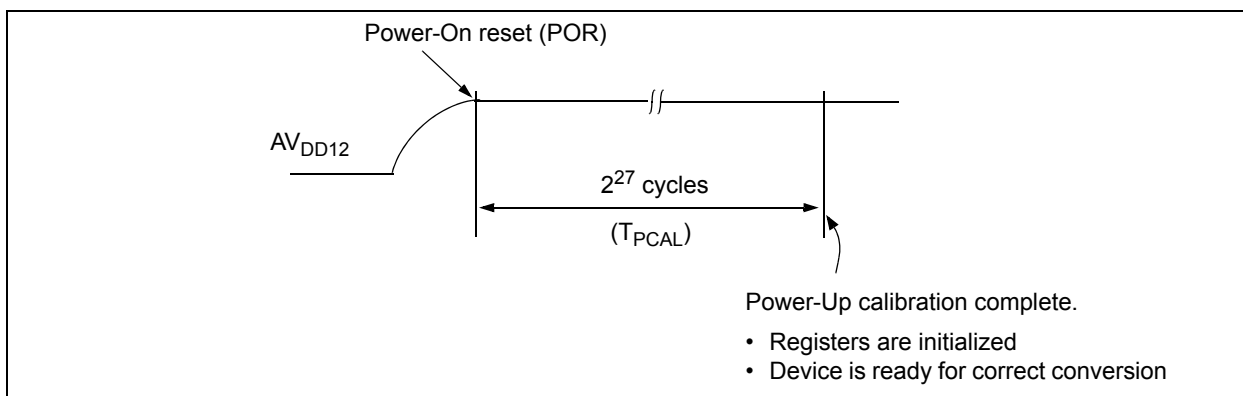


FIGURE 2-7: POR Related Events: Register Initialization and Power-Up Calibration.

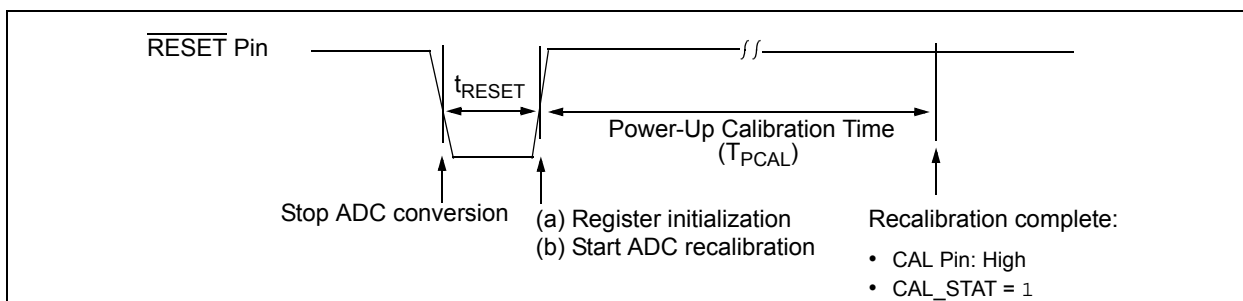


FIGURE 2-8: RESET Pin Timing Diagram.

TABLE 2-4: TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $\text{GND} = 0\text{V}$, $\text{SENSE} = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz, $f_S = 200\text{ Msps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100 Ω termination, LVDS driver current setting = 3.5 mA, $\text{DCLK_PHDLY_DEC} <2:0> = 000$, $+25^\circ\text{C}$ is applied for typical value.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|------------------------------------|---------------|------|------|------|--------------------|------------|
| Temperature Ranges | | | | | | |
| Specified Temperature Range | T_A | -40 | — | +85 | $^\circ\text{C}$ | |
| Operating Temperature Range | T_A | -40 | — | +85 | $^\circ\text{C}$ | |
| Storage Temperature Range | T_A | -65 | — | +150 | $^\circ\text{C}$ | |
| Thermal Package Resistances | | | | | | |
| 121L Ball-TFBGA (8mm x 8mm) | θ_{JA} | — | 40.2 | — | $^\circ\text{C/W}$ | |
| | θ_{JC} | — | 8.4 | — | $^\circ\text{C/W}$ | |
| 124L – VTLA (9mm x 9mm) | θ_{JA} | — | 20.8 | — | $^\circ\text{C/W}$ | |
| | θ_{JC} | — | 8.7 | — | $^\circ\text{C/W}$ | |

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $AV_{DD18} = DV_{DD18} = 1.8\text{V}$, $AV_{DD12} = DV_{DD12} = 1.2\text{V}$, $GND = 0\text{V}$, $SENSE = AV_{DD12}$, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS , $f_{IN} = 70\text{ MHz}$, Clock Input = 200 MHz , $f_S = 200\text{ Mpsps}$ (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled.

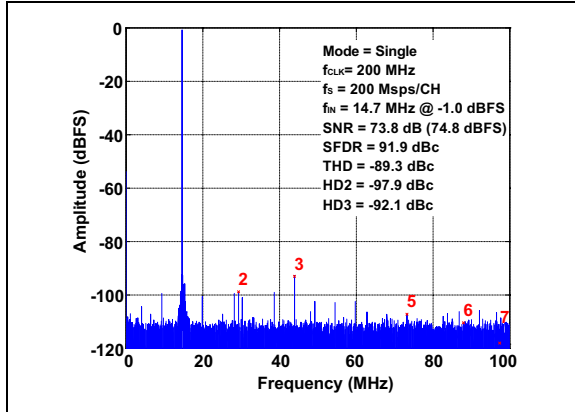


FIGURE 3-1: FFT for 14.7 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -1\text{ dBFS}$.

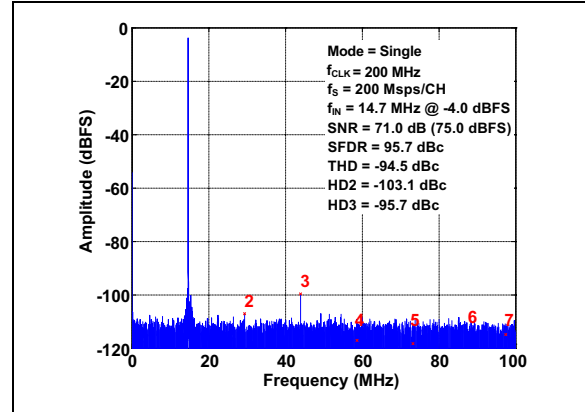


FIGURE 3-4: FFT for 14.7 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -4\text{ dBFS}$.

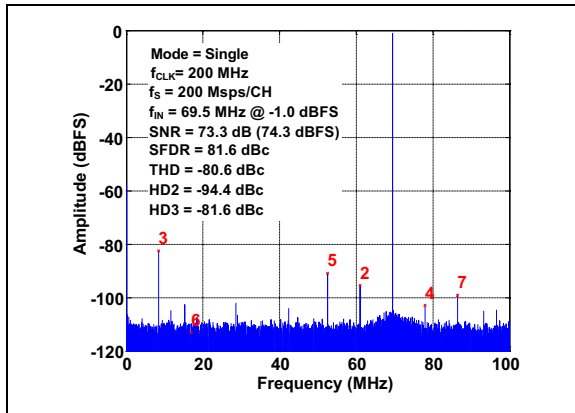


FIGURE 3-2: FFT for 69.5 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -1\text{ dBFS}$.

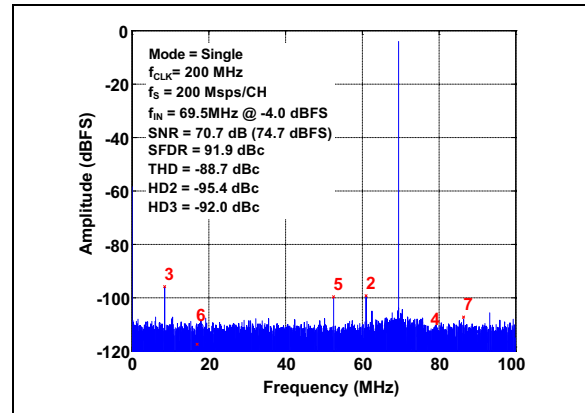


FIGURE 3-5: FFT for 69.5 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -4\text{ dBFS}$.

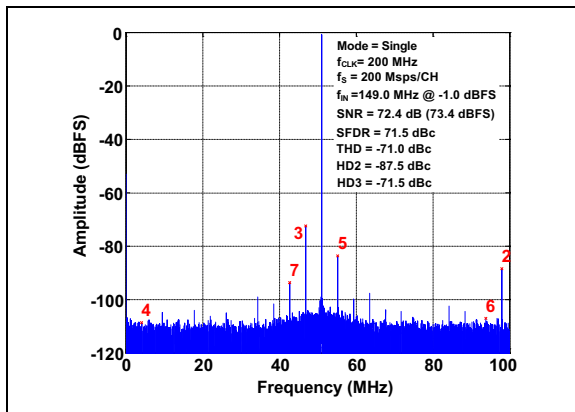


FIGURE 3-3: FFT for 149 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -1\text{ dBFS}$.

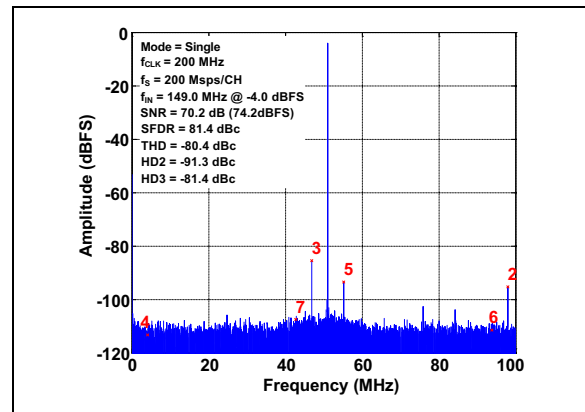


FIGURE 3-6: FFT for 149 MHz Input Signal: $f_S = 200\text{ Mpsps/Ch.}$, $A_{IN} = -4\text{ dBFS}$.

MCP37231/21-200 AND MCP37D31/21-200

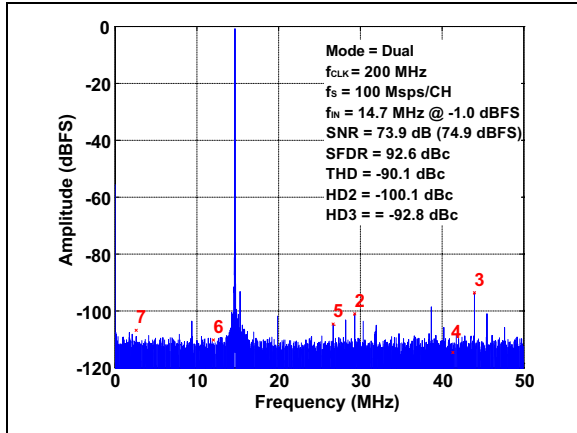


FIGURE 3-7: FFT for 14.7 MHz Input
 Signal: $f_s = 100 \text{ Msps/Ch.}$, Dual, $A_{IN} = -1 \text{ dBFS}$.

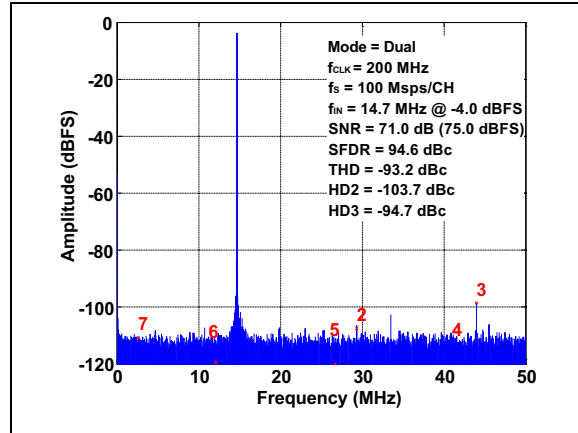


FIGURE 3-10: FFT for 14.7 MHz Input
 Signal: $f_s = 100 \text{ Msps/Ch.}$, Dual, $A_{IN} = -4 \text{ dBFS}$.

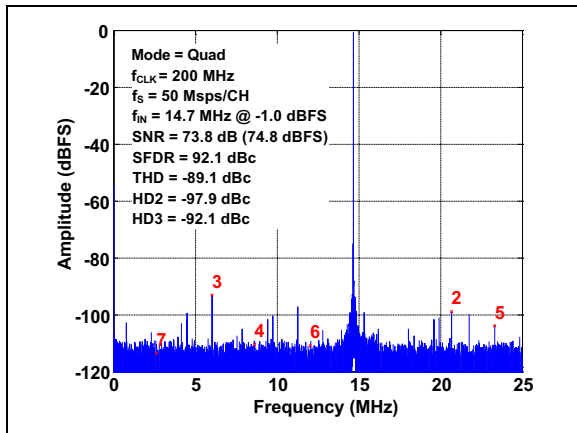


FIGURE 3-8: FFT for 14.7 MHz Input
 Signal: $f_s = 50 \text{ Msps/Ch.}$, Quad, $A_{IN} = -1 \text{ dBFS}$.

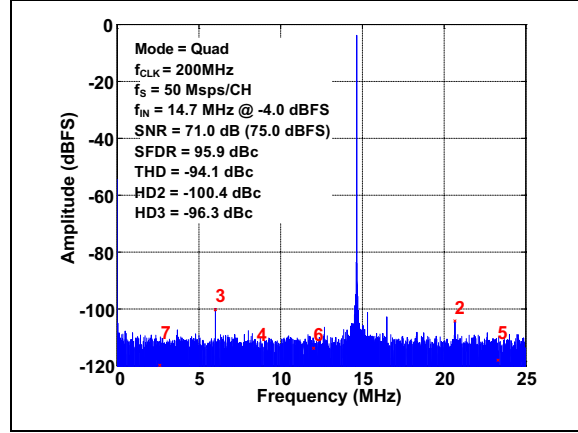


FIGURE 3-11: FFT for 14.7 MHz Input
 Signal: $f_s = 50 \text{ Msps/Ch.}$, Quad, $A_{IN} = -4 \text{ dBFS}$.

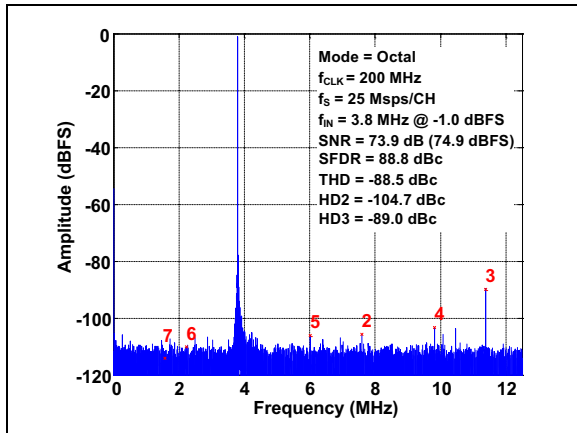


FIGURE 3-9: FFT for 3.8 MHz Input
 Signal: $f_s = 25 \text{ Msps/Ch.}$, Octal, $A_{IN} = -1 \text{ dBFS}$.

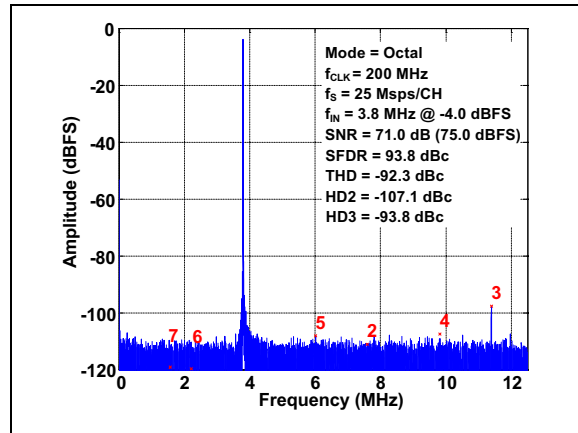


FIGURE 3-12: FFT for 3.8 MHz Input
 Signal: $f_s = 25 \text{ Msps/Ch.}$, Octal, $A_{IN} = -4 \text{ dBFS}$.

MCP37231/21-200 AND MCP37D31/21-200

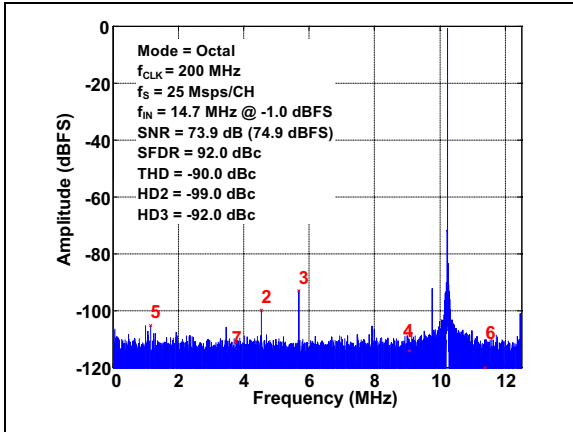


FIGURE 3-13: FFT for 14.7 MHz Input Signal: $f_S = 25$ Msps/Ch., Octal, $A_{IN} = -1$ dBFS.

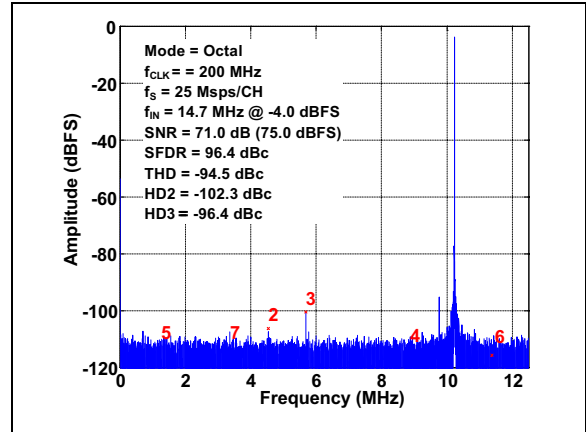


FIGURE 3-15: FFT for 14.7 MHz Input Signal: $f_S = 25$ Msps/Ch., Octal, $A_{IN} = -4$ dBFS.

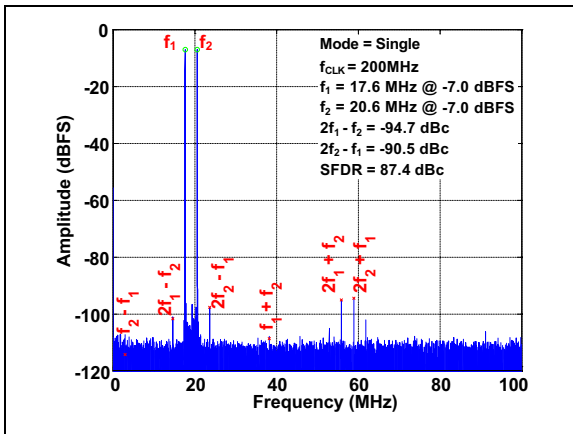


FIGURE 3-14: Two-Tone FFT: $f_{IN1} = 17.6$ MHz and $f_{IN2} = 20.6$ MHz, $A_{IN} = -7$ dBFS per Tone, $f_S = 200$ Msps.

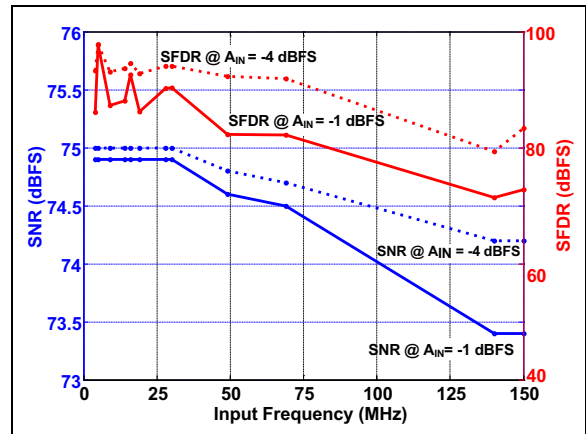


FIGURE 3-16: SNR/SFDR vs. Input Frequency.

MCP37231/21-200 AND MCP37D31/21-200

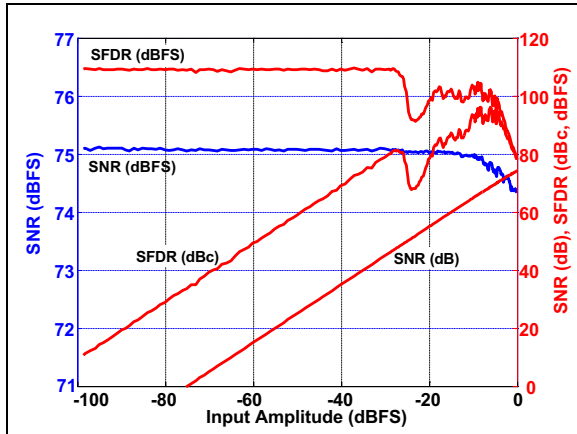


FIGURE 3-17: SNR/SFDR vs. Analog Input Amplitude: $f_s = 200$ Mpsps, $f_{IN} = 70$ MHz.

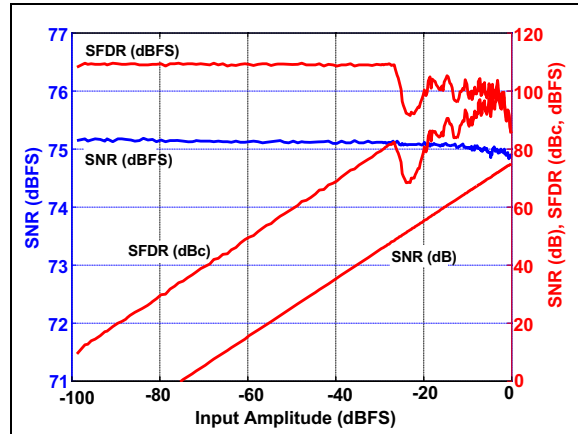


FIGURE 3-20: SNR/SFDR vs. Analog Input Amplitude: $f_s = 200$ Mpsps, $f_{IN} = 15$ MHz.

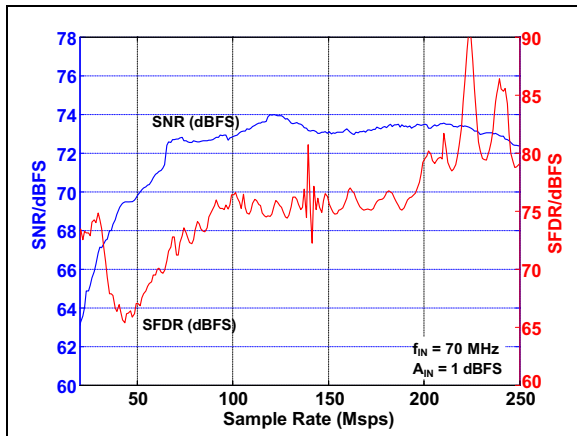


FIGURE 3-18: SNR/SFDR vs. Sample Rate (Mpsps): $f_{IN} = 70$ MHz.

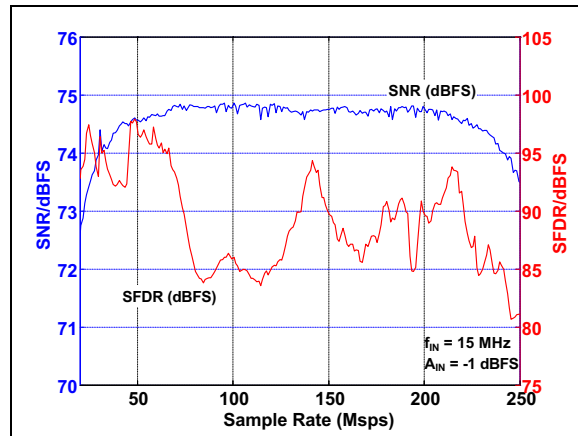


FIGURE 3-21: SNR/SFDR vs. Sample Rate (Mpsps): $f_{IN} = 15$ MHz.

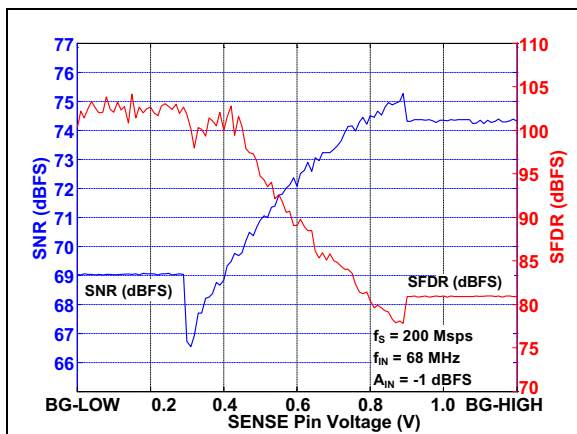


FIGURE 3-19: SNR/SFDR vs. SENSE Pin Voltage: $f_s = 200$ Mpsps, $f_{IN} = 68$ MHz.

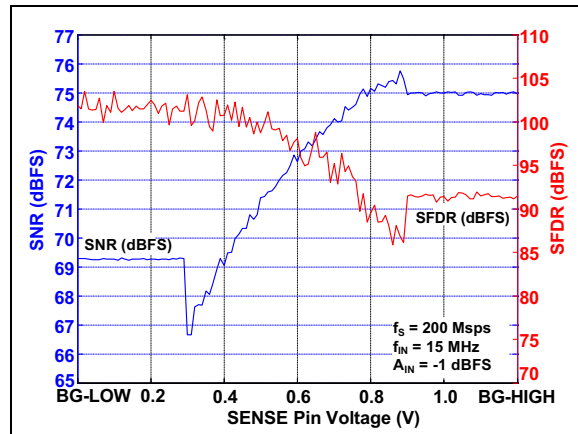


FIGURE 3-22: SNR/SFDR vs. SENSE Pin Voltage: $f_s = 200$ Mpsps, $f_{IN} = 15$ MHz.

MCP37231/21-200 AND MCP37D31/21-200

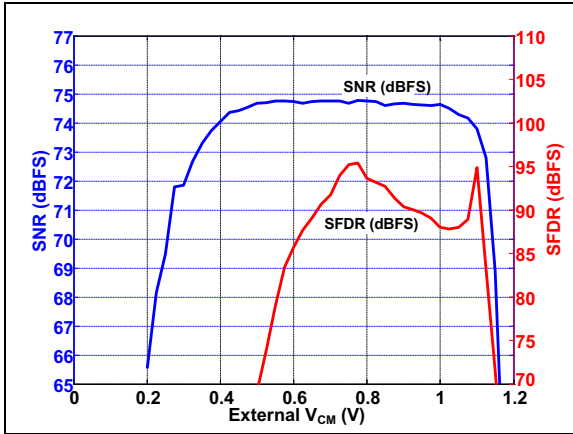


FIGURE 3-23: SNR/SFDR vs. V_{CM} Voltage (Externally Applied): $f_S = 200$ Msps, $f_{IN} = 15$ MHz.

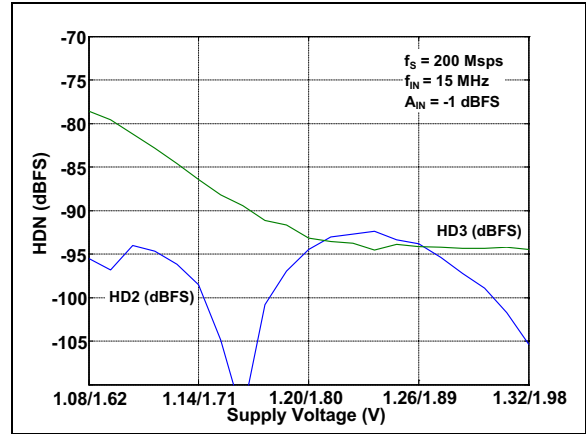


FIGURE 3-26: HD2/HD3 vs. Supply Voltage: $f_S = 200$ Msps, $f_{IN} = 15$ MHz.

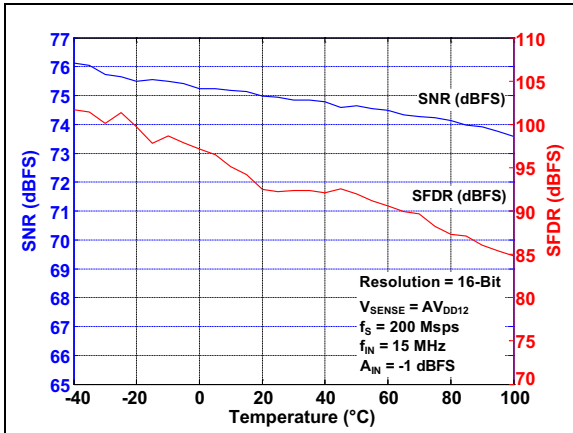


FIGURE 3-24: SNR/SFDR vs. Temperature: $f_S = 200$ Msps, $f_{IN} = 15$ MHz.

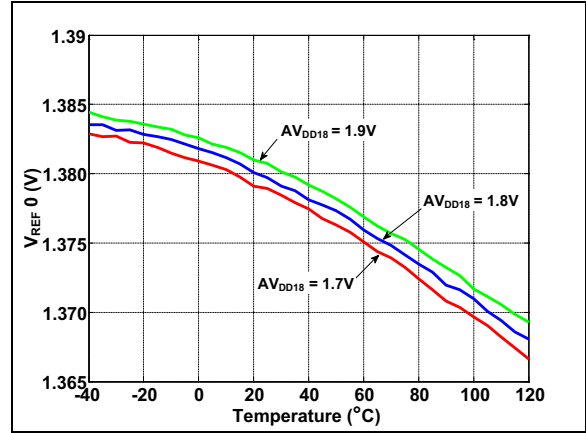


FIGURE 3-27: V_{REF0} Vs. Temperature.

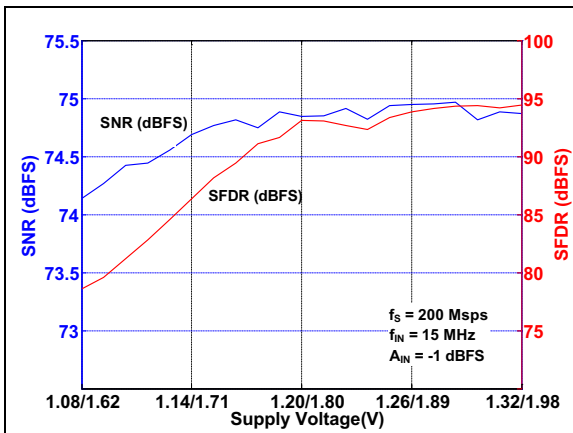


FIGURE 3-25: SNR/SFDR vs. Supply Voltage: $f_S = 200$ Msps, $f_{IN} = 15$ MHz.

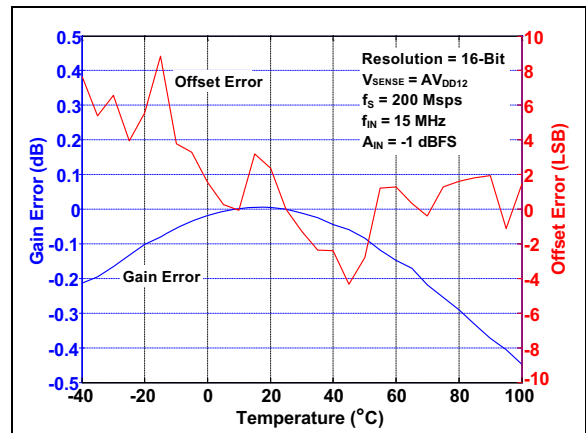


FIGURE 3-28: Gain and Offset Error Drifts Vs. Temperature Using Internal Reference, with Respect to 25 °C: $f_S = 200$ Msps.

MCP37231/21-200 AND MCP37D31/21-200

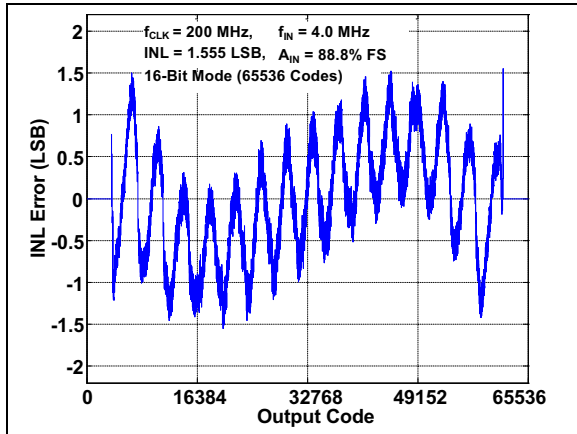


FIGURE 3-29: INL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 16-bit Mode.

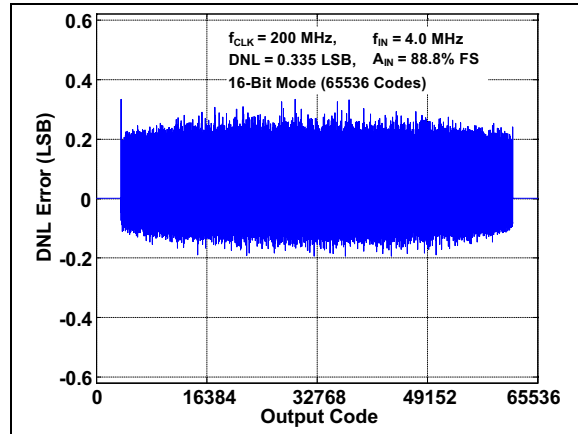


FIGURE 3-32: DNL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 16-bit Mode.

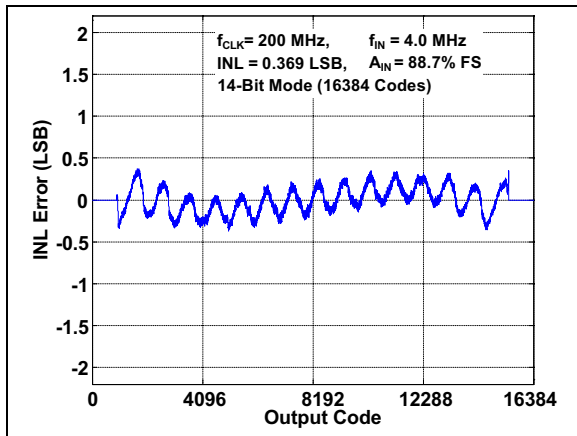


FIGURE 3-30: INL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 14-bit Mode.

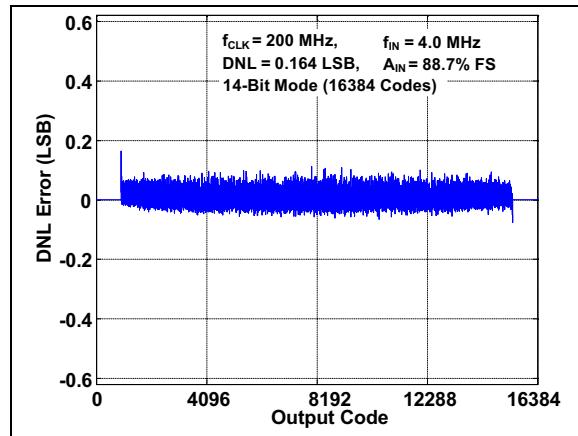


FIGURE 3-33: DNL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 14-bit Mode.

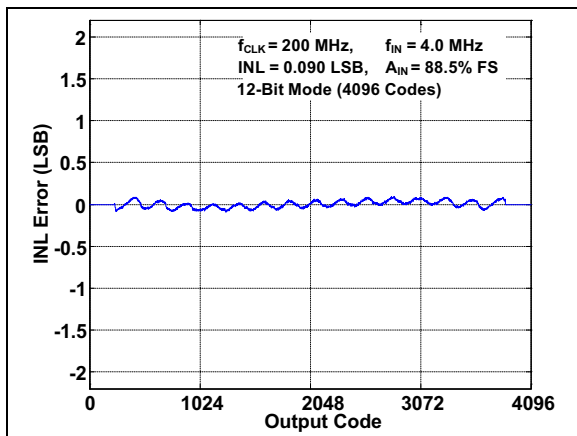


FIGURE 3-31: INL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 12-bit Mode.

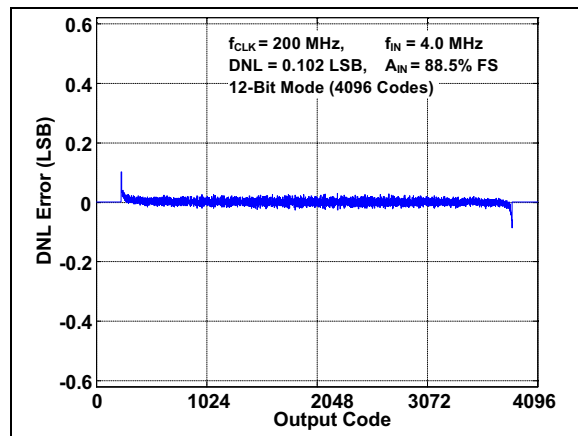


FIGURE 3-34: DNL Error Vs. Output Code: $f_S = 200$ Msp/s, $f_{IN} = 4$ MHz, 12-bit Mode.

MCP37231/21-200 AND MCP37D31/21-200

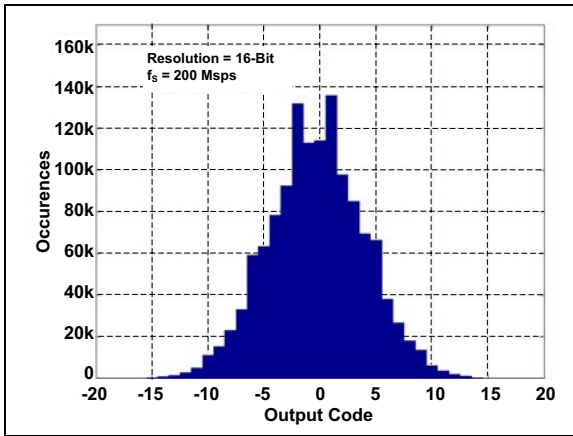


FIGURE 3-35: Shorted Input Histogram: $f_s = 200$ Msps, Resolution = 16-Bit Shorted Input.

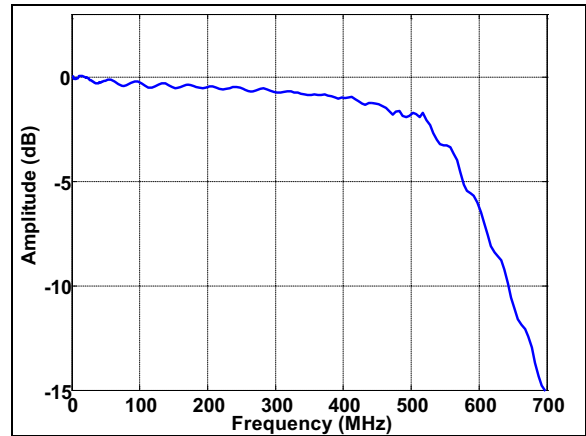


FIGURE 3-38: Input Bandwidth.

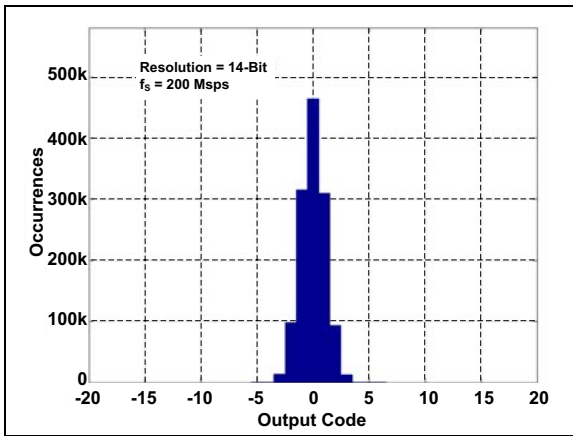


FIGURE 3-36: Shorted Input Histogram: $f_s = 200$ Msps, Resolution = 14-Bit.

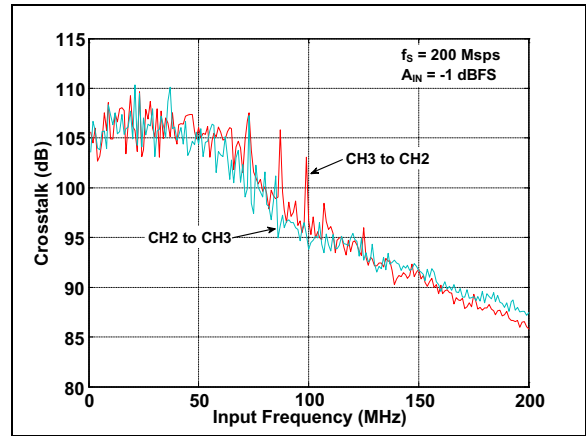


FIGURE 3-39: Input Channel Cross-Talk.

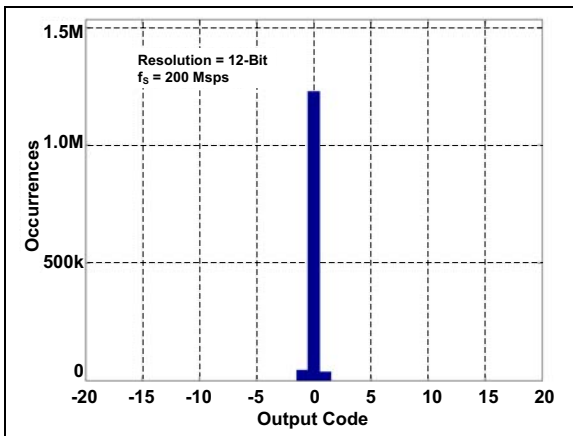


FIGURE 3-37: Shorted Input Histogram: $f_s = 200$ Msps, Resolution = 12-bit.

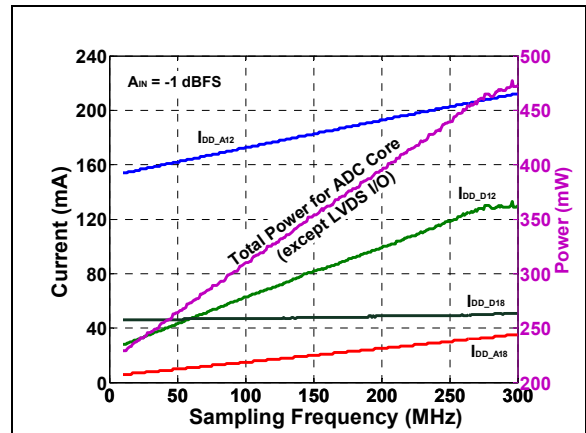


FIGURE 3-40: Power Consumption vs. Sampling Frequency.

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

4.0 THEORY OF OPERATION

The MCP37231/21-200 and MCP37D31/21-200 device family is a low-power, 16/14-bit, 200 Msps analog-to-digital converter (ADC) with built-in features including harmonic distortion correction (HDC), DAC noise cancellation (DNC), dynamic element matching (DEM) and flash error calibration.

Depending on the product number selection, the device offers various built-in digital signal post-processing features, such as FIR decimation filters, digital down-conversion (DDC), fractional delay recovery (FDR), continuous CW beamforming, and digital gain and offset correction. These built-in advanced digital signal post-processing sub-blocks, which are individually controlled, can be used for various special applications such as I/Q demodulator, digital down-converter and ultrasound imaging.

The device's operational modes and feature sets are configured using the user-programmable internal registers. All user registers, except the factory controlled registers, are re-programmable using the SPI interface. When the device is first powered-up, the device is running with default settings. The user can select external clock input or on-board phase-locked loop (PLL) output as the input-sampling frequency by setting the clock source selection bit. In multi-channel mode, the input channel selection and MUX scan order are user-configurable, and the inputs are sequentially multiplexed by the input MUX defined by the scan order.

The device samples the analog input on the rising edge of the clock. The digital output code is available after 28 clock cycles of data latency. Latency will increase if any of the various digital signal post-processing (DSPP) options are enabled.

The output data can be coded in two's complement or offset binary format, and randomized using the user option. Data can be output using either the CMOS or LVDS (Low Voltage Differential Signaling) interface. Serialized LVDS output is also available in 16-bit octal-channel mode. In this mode, each input channel is output serially over a unique LVDS pair.

4.1 ADC Core Architecture

Figure 4-1 shows the simplified block diagram of the ADC core. The first stage consists of a 17-level flash ADC, multi-level digital-to-analog converter (DAC) and a residue amplifier with a gain of 8. Stages 2 to 6 consist of a 9-level (3-bit) flash ADC, multi-level DAC and a residue amplifier with a gain of 4. The last stage is a 9-level 3-bit flash ADC. Dither is added in each of the first 3 stages. The digital outputs from all seven stages are combined in a digital error correction logic block and digitally processed for the final output.

The first three stages include patented digital calibration features:

- Harmonic Distortion Correction (HDC) algorithm that digitally measures and cancels ADC errors arising from distortions introduced by the residue amplifiers
- DAC Noise Cancellation (DNC) algorithm that corrects DAC's nonlinearity errors
- Dynamic Element Matching (DEM) which randomizes DAC errors thereby converting harmonic distortion to white noise

These digital correction algorithms are first applied during the power-on reset sequence, and then operate in the background during normal operation of the pipelined ADC. These algorithms automatically track and correct any environmental changes in the ADC. More details of the system correction algorithms are shown in [Section 4.16 "System Calibration"](#).

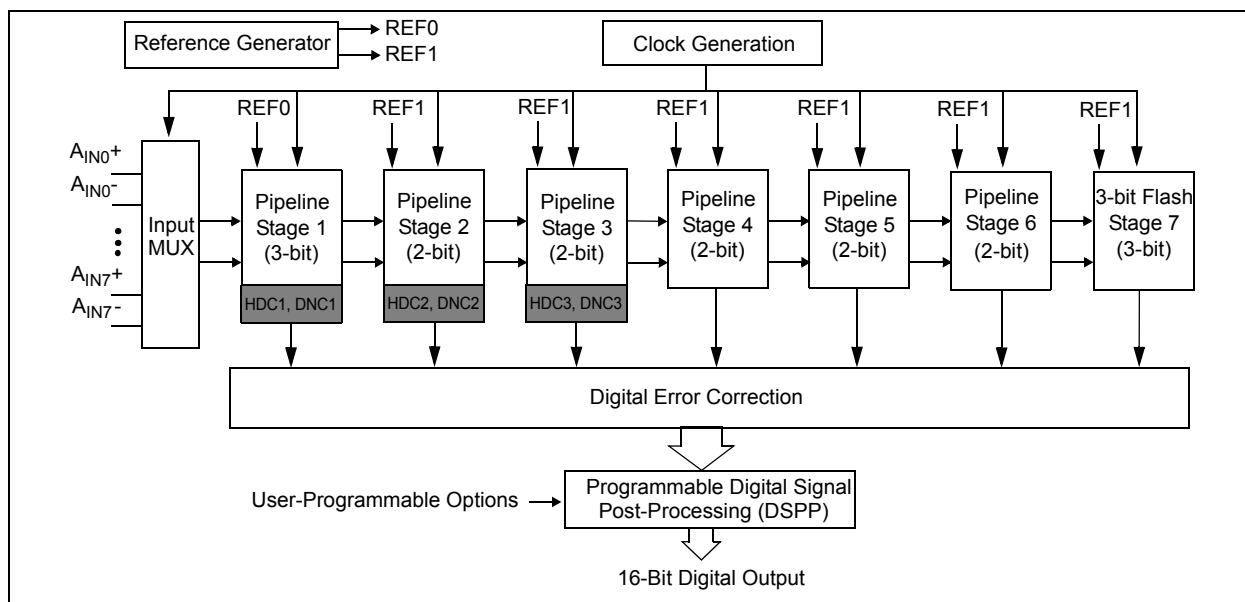


FIGURE 4-1: ADC Core Block Diagram.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 4-1: EXAMPLE: CHANNEL ORDER SELECTION USING ADDRESSES 0X7D – 0X7F

| No. of Channels (Note 1) | Selected Channels | Channel Order (Note 2) | Address 0x7F | | | | Address 0x7E | | | | Address 0x7D | | | |
|-----------------------------|-------------------|---------------------------|----------------------------|---------|---------|---------|--------------|---------|---------|---------|--------------|----|--|--|
| | | | b7 | | | | b0 | b7 | | | b0 | b7 | | |
| 7 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | 4th Ch. | 5th Ch. | 3rd Ch. | 6th Ch. | 2nd Ch. | 7th Ch. | 1st Ch. | | | | |
| | [0 1 2 3 4 5 6] | [0 1 2 3 4 5 6 7] | 1 1 1 | 0 1 1 | 1 0 0 | 0 1 0 | 1 0 1 | 0 0 1 | 1 1 0 | 0 0 0 | | | | |
| | [0 2 4 6 1 3 5] | [0 2 4 6 1 3 5 7] | 1 1 1 | 1 1 0 | 0 0 1 | 1 0 0 | 0 1 1 | 0 1 0 | 1 0 1 | 0 0 0 | | | | |
| 6 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | 4th Ch. | 3rd Ch. | 5th Ch. | 2nd Ch. | 6th Ch. | 1st Ch. | | | | |
| | [0 1 2 3 4 5] | [0 1 2 3 4 5 6 7] | 1 1 1 | 1 1 0 | 0 1 1 | 0 1 0 | 1 0 0 | 0 0 1 | 1 0 1 | 0 0 0 | | | | |
| | [0 2 4 6 1 3] | [0 2 4 6 1 3 5 7] | 1 1 1 | 1 0 1 | 1 1 0 | 1 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 0 0 0 | | | | |
| 5 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | Unused | 3rd Ch. | 4th Ch. | 2nd Ch. | 5th Ch. | 1st Ch. | | | | |
| | [0 1 2 3 4] | [0 1 2 3 4 5 6 7] | 1 1 0 | 1 0 1 | 1 1 1 | 0 1 0 | 0 1 1 | 0 0 1 | 1 0 0 | 0 0 0 | | | | |
| | [0 2 4 6 1] | [0 2 4 6 1 3 5 7] | 1 0 1 | 0 1 1 | 1 1 1 | 1 0 0 | 1 1 0 | 0 1 0 | 0 0 1 | 0 0 0 | | | | |
| 4 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | Unused | Unused | 3rd Ch. | 2nd Ch. | 4th Ch. | 1st Ch. | | | | |
| | [0 1 2 3] | [0 1 2 3 4 5 6 7] | 1 1 0 | 1 0 1 | 1 1 1 | 1 0 0 | 0 1 0 | 0 0 1 | 0 1 1 | 0 0 0 | | | | |
| | [4 5 6 7] | [4 5 6 7 0 1 2 3] | 0 1 0 | 0 0 1 | 0 1 1 | 0 0 0 | 1 1 0 | 1 0 1 | 1 1 1 | 1 0 0 | | | | |
| | [0 2 4 6] | [0 2 4 6 1 3 5 7] | 1 0 1 | 0 1 1 | 1 1 1 | 0 0 1 | 1 0 0 | 0 1 0 | 1 1 0 | 0 0 0 | | | | |
| | [1 3 5 7] | [1 3 5 7 0 2 4 6] | 1 0 0 | 0 1 0 | 1 1 0 | 0 0 0 | 1 0 1 | 0 1 1 | 1 1 1 | 0 0 1 | | | | |
| 3 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | Unused | Unused | Unused | 2nd Ch. | 3rd Ch. | 1st Ch. | | | | |
| | [0 1 2] | [0 1 2 3 4 5 6 7] | 1 0 1 | 1 0 0 | 1 1 0 | 0 1 1 | 1 1 1 | 0 0 1 | 0 1 0 | 0 0 0 | | | | |
| | [0 2 4] | [0 2 4 6 1 3 5 7] | 0 1 1 | 0 0 1 | 1 0 1 | 1 1 0 | 1 1 1 | 0 1 0 | 1 0 0 | 0 0 0 | | | | |
| 2 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | Unused | Unused | Unused | Unused | 2nd Ch. | 1st Ch. | | | | |
| | [0 1] | [0 1 2 3 4 5 6 7] | 1 0 1 | 1 0 0 | 1 1 0 | 0 1 1 | 1 1 1 | 0 1 0 | 0 0 1 | 0 0 0 | | | | |
| | [2 3] | [2 3 0 1 4 5 6 7] | 1 0 1 | 1 0 0 | 1 1 0 | 0 0 1 | 1 1 1 | 0 0 0 | 0 1 1 | 0 1 0 | | | | |
| | [4 5] | [4 5 0 1 2 3 6 7] | 0 1 1 | 0 1 0 | 1 1 0 | 0 0 1 | 1 0 1 | 0 0 0 | 1 0 1 | 1 0 0 | | | | |
| | [6 7] | [6 7 0 1 2 3 4 5] | 0 1 1 | 0 1 0 | 1 0 0 | 0 0 1 | 1 0 1 | 0 0 0 | 1 1 1 | 1 1 0 | | | | |
| 1 | | | Channel Order Bit Settings | | | | | | | | | | | |
| | | | Unused | Unused | Unused | Unused | Unused | Unused | Unused | 1st Ch. | | | | |
| | [0] | [0 1 2 3 4 5 6 7] | 1 0 0 | 0 1 1 | 1 0 1 | 0 1 0 | 1 1 0 | 0 0 1 | 1 1 1 | 0 0 0 | | | | |
| | [1] | [1 0 2 3 4 5 6 7] | 1 0 0 | 0 1 1 | 1 0 1 | 0 1 0 | 1 1 0 | 0 0 0 | 1 1 1 | 0 0 1 | | | | |
| | [2] | [2 0 1 3 4 5 6 7] | 1 0 0 | 0 1 1 | 1 0 1 | 0 0 1 | 1 1 0 | 0 0 0 | 1 1 1 | 0 1 0 | | | | |
| | [3] | [3 0 1 2 4 5 6 7] | 1 0 0 | 0 1 0 | 1 0 1 | 0 0 1 | 1 1 0 | 0 0 0 | 1 1 1 | 0 1 1 | | | | |
| | [4] | [4 0 1 2 3 5 6 7] | 0 1 1 | 0 1 0 | 1 0 1 | 0 0 1 | 1 1 0 | 0 0 0 | 1 1 1 | 1 0 0 | | | | |
| | [5] | [5 0 1 2 3 4 6 7] | 0 1 1 | 0 1 0 | 1 0 0 | 0 0 1 | 1 1 0 | 0 0 0 | 1 1 1 | 1 0 1 | | | | |
| | [6 0 1 2 3 4 5 7] | 0 1 1 | 0 1 0 | 1 0 0 | 0 0 1 | 1 0 1 | 0 0 0 | 1 1 1 | 1 1 0 | | | | | |
| | [7 0 1 2 3 4 5 6] | 0 1 1 | 0 1 0 | 1 0 0 | 0 0 1 | 1 0 1 | 0 0 0 | 1 1 0 | 1 1 1 | | | | | |

Note 1: Defined by SEL_NCH<2:0> in Address 0x01 (Register 5-2).

Note 2: Individual channel order should not be repeated. Unused channels are still assigned after the selected channel address. The order of the unused channel address has no meaning since they are not used.

MCP37231/21-200 AND MCP37D31/21-200

4.5 Analog Input Circuit

The analog input of the MCP37231/21-200 and MCP37D31/21-200 is a differential CMOS switched capacitor sample-and-hold circuit. Figure 4-2 shows the equivalent input structure of the device.

The input impedance of the device is mostly governed by the input sampling capacitor ($C_S = 6\text{ pF}$) and input sampling frequency (f_S). The performance of the device can be affected by the input signal conditioning network (see Figure 4-3). The analog input signal source must have sufficiently low output impedance to charge the sampling capacitors ($C_S = 6\text{ pF}$) within one clock cycle. A small external resistor (e.g. 5Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low-pass filter with the capacitor, and their values must be determined by application requirements and input frequency.

The V_{CM} pin provides a common-mode voltage reference ($0.9V$), which can be used for a center-tap voltage of an RF transformer or balun. If the V_{CM} pin voltage is not used, the user may create a common mode voltage at mid-supply level ($AV_{DD18}/2$).

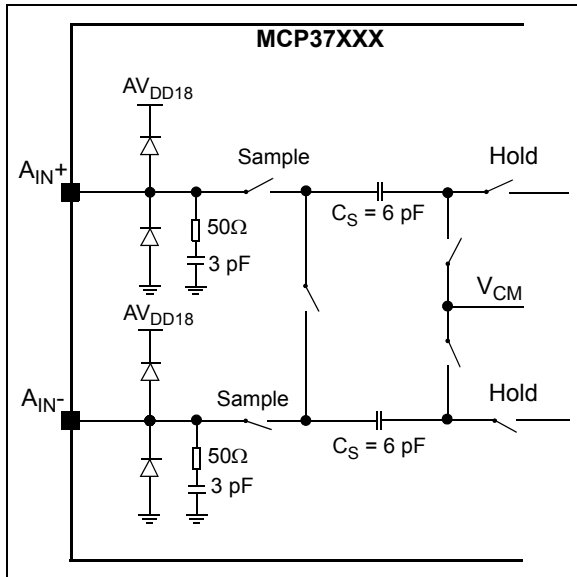


FIGURE 4-2: Equivalent Input Circuit.

4.5.1 ANALOG INPUT DRIVING CIRCUIT

4.5.1.1 Differential Input Configuration

The device achieves optimum performance when the input is driven differentially, where common-mode noise immunity and even-order harmonic rejection are significantly improved. If the input is single ended, it must be converted to a differential signal in order to properly drive the ADC input. The differential conversion and common mode application can be accomplished by using an RF transformer or balun with a center-tap. Additionally, one or more anti-aliasing filters may be added for optimal noise performance and should be tuned such that the corner frequency is appropriate for the system.

Figure 4-3 shows an example of the differential input circuit with transformer. Note that the input driving circuits are terminated by 50Ω near the ADC side through a pair of 25Ω resistors from each input to the common-mode (V_{CM}) from the device. The RF transformer must be carefully selected to avoid artificial high harmonic distortion. The transformer can be damaged due to excessive input power, or due to an RF input being applied while the MCP37XXX is powered off. Figure 4-4 shows an input configuration example when a differential output amplifier is used.

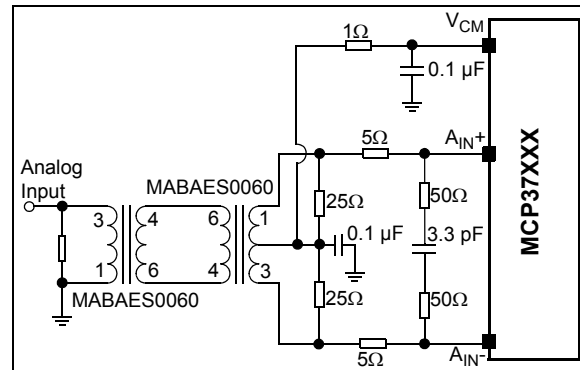


FIGURE 4-3: Transformer Coupled Input Configuration.

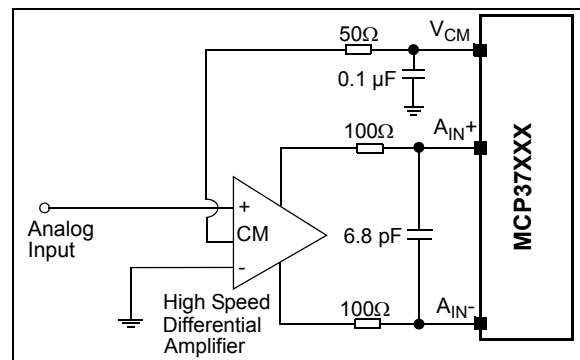


FIGURE 4-4: DC-Coupled Input Configuration with Pre-Amplifier: the external signal conditioning circuit and associated component values are for reference only. Typically the amplifier manufacturer provides reference circuits and component values.

MCP37231/21-200 AND MCP37D31/21-200

4.5.1.2 Single-Ended Input Configuration

SNR and SFDR performance degrades significantly when the device is operated in a single-ended configuration. The unused negative side of the input should be AC coupled to ground using a capacitor. [Figure 4-5](#) shows an example of a single-ended input configuration.

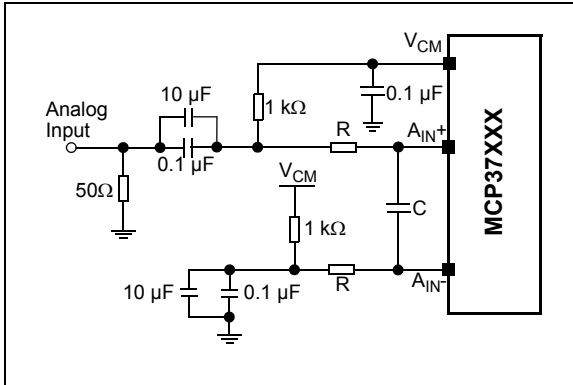


FIGURE 4-5: Single-Ended Input Configuration.

4.5.2 SENSE VOLTAGE AND INPUT FULL-SCALE RANGE

The device has a bandgap-based differential internal reference voltage. The SENSE pin voltage is used to select the internal reference voltage source and configures the input full-scale range. A comparator detects the SENSE pin voltage and configures the full-scale input range into one of the possible three modes which are summarized in [Table 4-2](#). [Figure 4-6](#) shows an example of how the SENSE pin should be driven.

The SENSE pin can sink or source currents as high as 500 µA across all operational conditions. Therefore, it may require a driver circuit, unless the SENSE reference source provides sufficient output current.

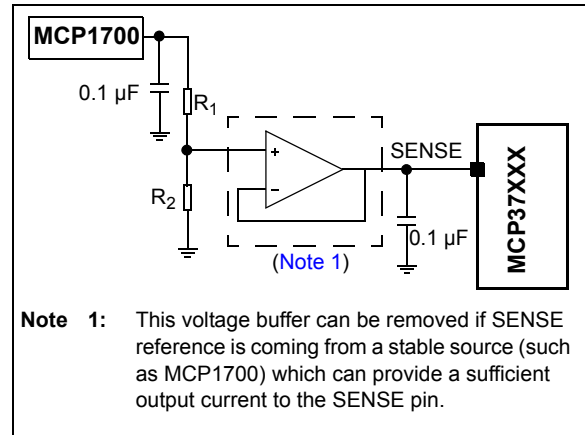


FIGURE 4-6: SENSE Pin Voltage Setup.

TABLE 4-2: SENSE PIN VOLTAGE AND INPUT FULL-SCALE RANGE

| SENSE Pin Voltage (V_{SENSE}) | Selected Reference Voltage (V_{REF}) | Full-Scale Input Voltage Range (A_{FS}) | Condition |
|-----------------------------------|--|---|---|
| Tied to GND | 0.74375V | 1.4875 V_{P-P} (Note 1) | Low Reference Mode (Note 4) |
| 0.4V – 0.8 V | 0.74375V – 1.4875V | 1.4875 V_{P-P} to 2.975 V_{P-P} (Note 2) | Bandgap Mode (Note 5) |
| Tied to AV_{DD12} | 1.4875V | 2.975 V_{P-P} (Note 3) | High Reference Mode (Note 4) |

Note 1: $A_{FS} = (17/16) \times 1.4 V_{P-P} = 1.487 V_{P-P}$

2: $A_{FS} = (17/16) \times 2.8 V_{P-P} \times (V_{SENSE}/0.8) = 1.4875 V_{P-P}$ to $2.975 V_{P-P}$

3: $A_{FS} = (17/16) \times 2.8 V_{P-P} = 2.975 V_{P-P}$

4: Based on internal bandgap voltage.

5: Based on V_{SENSE} .

MCP37231/21-200 AND MCP37D31/21-200

4.5.3 DECOUPLING CIRCUITS FOR INTERNAL VOLTAGE REFERENCE AND BAND GAP OUTPUT

The device has two internal voltage references: REF0 and REF1. REF0 is the internal voltage reference for the ADC input stage, and REF1 is for all remaining stages. These internal references require external capacitors for stable operation. These capacitors are embedded in the TFBGA-121 package. In the VTLA-124 package, the user must provide these external capacitors on the PCB at the REF1+/REF1- and REF0+/REF0- pins.

Figure 4-7 shows the recommended circuit for the REF1 and REF0 pins for VTLA-124 package. Three parallel capacitors are recommended between the positive and negative reference pins. The negative reference pin is then grounded through a 220 nF capacitor. The values for the parallel capacitors are 22 nF, 220 nF and 2.2 μ F. The capacitors should be placed as close to the ADC as possible with short and thick traces. Vias on the PCB are not recommended for this reference pin circuit.

The internal band gap voltage output, which is a part of the reference circuit, is also available at the V_{BG} pin. This pin needs an external decoupling capacitor (2.2 μ F) for VTLA-124 package as shown in Figure 4-7. In the TFBGA-121 package, the decoupling capacitor is also embedded the same as the reference. Therefore, this circuit is not required.

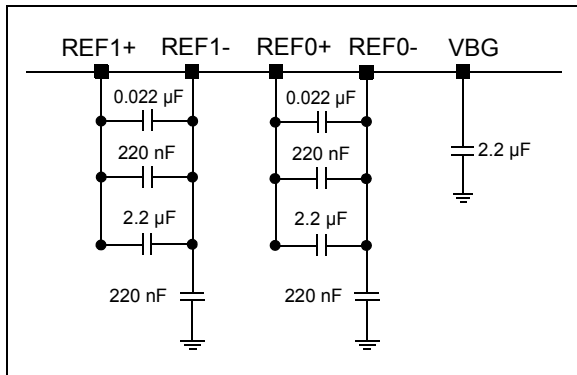


FIGURE 4-7: External Circuit for Voltage Reference and V_{BG} pins for VTLA-124 Package. Note that this external circuit is not required for TFBGA-121 package.

4.6 External Clock Input

For optimum performance, the MCP37XXX requires a low jitter differential clock input at CLK+ and CLK- pins. Figure 4-8 shows the equivalent clock input circuit.

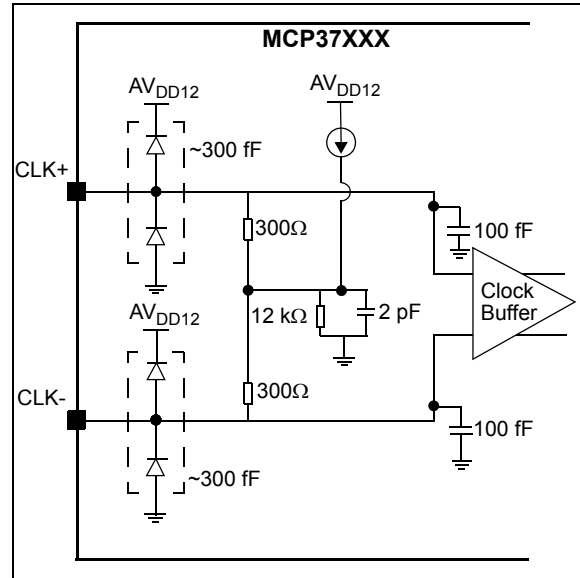


FIGURE 4-8: Equivalent Clock Input Circuit.

The clock input amplitude range is between 300 mV_{P-P} and 800 mV_{P-P}. When a single-ended clock source is used, an RF transformer or balun can be used to convert the clock into a differential signal for the best ADC performance. Figure 4-9 shows an example clock input circuit. The common-mode voltage is internally generated, and a center-tap is not required. The back-to-back Schottky diodes across the transformer secondary limit the clock amplitude to approximately 0.8 V_{P-P} differential. This limiter helps preventing large voltage swings of the clock while preserving the high slew rate that is critical for low jitter.

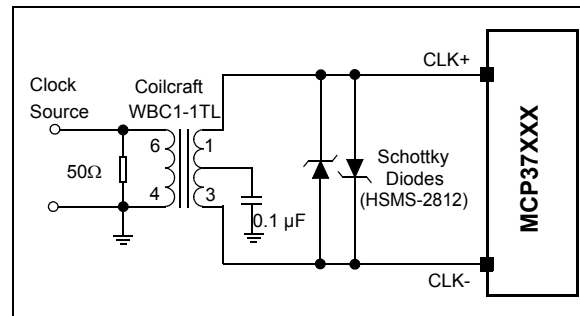


FIGURE 4-9: Transformer-Coupled Differential Clock Input Configuration.

MCP37231/21-200 AND MCP37D31/21-200

4.6.1 CLOCK JITTER AND SNR PERFORMANCE

In a high speed-pipelined ADC, the SNR performance is directly limited by linearity, thermal noise and clock jitter. Thermal noise is independent of input clock and dominant at low input frequency. On the other hand, the clock jitter becomes a dominant term as input frequency increases. Equation 4-2 shows the SNR jitter component, which is expressed in terms of the input frequency (f_{IN}) and the total amount of clock jitter (T_{Jitter}), where T_{Jitter} is a sum of two components:

- Input clock jitter (phase noise)
- Internal aperture jitter (due to noise of the clock input buffer).

EQUATION 4-2: SNR VS. CLOCK JITTER

$$SNR_{Jitter}(dBc) = -20 \times \log_{10}(2\pi \times f_{IN} \times T_{Jitter})$$

where the total jitter term (T_{jitter}) is given by:

$$T_{Jitter} = \sqrt{(t_{Jitter, Clock Input})^2 + (t_{Aperture, ADC})^2}$$

The clock jitter and aperture jitter are not statistically correlated to each other. The clock jitter can be minimized by using a high-quality clock source and jitter cleaners as well as a band-pass filter at the external clock input, while a faster clock slew rate improves the ADC aperture jitter.

With a fixed amount of clock jitter, the SNR degrades as the input frequency increases. This is illustrated in Figure 4-10. If the input frequency increases from 10 MHz to 20 MHz, the maximum achievable SNR degrades about 6 dB. For every decade (e.g. 10 MHz to 100 MHz), the maximum achievable SNR due to clock jitter is reduced by 20 dB.

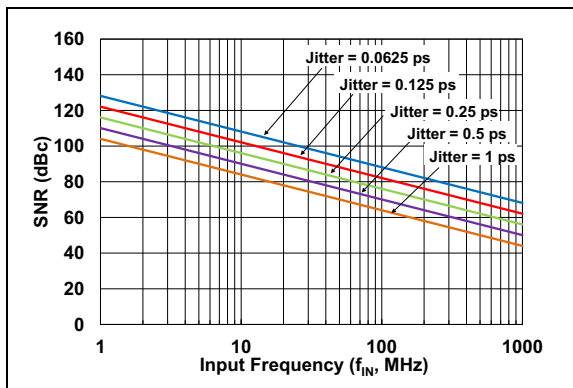


FIGURE 4-10: SNR vs. Clock Jitter.

4.6.2 CLOCK DUTY CYCLE

The ADC performance is sensitive to the clock duty cycle. The ADC achieves optimum performance with 50% duty cycle and all performance characteristics are ensured when the duty cycle is 50% with $\pm 1\%$ tolerance. This device has an internal clock duty cycle correction circuit, which can be enabled by using the EN_DUTY bit setting in Address 0x52 (Register 5-7). However, the duty cycle correction process adds additional jitter noise to the clock signal, and therefore using this option is only recommended when an asymmetrical input clock source causes significant performance degradation or the input clock source is not stable. See more details of setting EN_DUTY in Address 0x52 (Register 5-7).

4.7 ADC Clock Selection and PLL Output Frequency Control

4.7.1 ADC CLOCK SELECTION

The user can select the ADC timing source (internal PLL or external clock) using the clock source selection bit setting: See CLK_SOURCE in Address 0x53 (Register 5-8).

4.7.1.1 External Clock for ADC Timing

When CLK_SOURCE = 0, the external clock input (at CLK+ and CLK- pins) becomes the sampling frequency (f_S) of the ADC core and also the input frequency for the DLL circuit. See Figure 4-11 for the details of the DLL block. The user can control the phase of the DLL output using DLL_PHDLY<2:0> in Address 0x52 (Register 5-7).

Note: The on-board phase-locked loop (PLL) is not used for this setting.

4.7.1.2 Phase-Locked Loop (PLL) Output for ADC Timing:

When CLK_SOURCE = 1, the PLL output frequency is used as the sampling frequency (f_S) of the ADC core. The recommended PLL output clock range is from 80 MHz to 250 MHz. The external clock input is used as the PLL reference frequency. The range of the clock input frequency is from 5 MHz to 250 MHz.

Note: The PLL mode is only supported for sampling frequencies greater than 80 Msp.

MCP37231/21-200 AND MCP37D31/21-200

4.7.2 PLL OUTPUT FREQUENCY AND CONTROL PARAMETERS

The internal PLL can provide a stable timing output ranging from 80 MHz to 250 MHz. [Figure 4-11](#) shows the charge-pump based integer-N PLL and output control. The PLL includes various user control parameters for the desired output frequency. [Table 4-3](#) summarizes the PLL control register bits and [Table 4-4](#) shows an example of settings for the PLL charge pump and loop filter.

The PLL block consists of:

- Reference Frequency Divider (R)
- Prescaler - which is a feedback divider (N)
- Phase/Frequency Detector (PFD)
- Current Charge-Pump
- Loop Filter - a 3rd order RC low-pass filter
- Voltage-Controlled Oscillator (VCO)

The final ADC core sampling frequency (f_S) is then obtained by dividing down the VCO output using `PLL_OUTDIV<3:0>`.

The external clock at the CLK+ and CLK- pins is the input frequency to the PLL. The range of input frequency (f_{REF}) is from 5 MHz to 250 MHz. This input frequency is divided by the reference frequency divider (R) which is controlled by the 10-bit wide `PLL_REFDIV<9:0>` setting. In the feedback loop, the VCO frequency is divided by the prescaler (N) using `PLL_PRE<11:0>`.

The final ADC core sampling frequency (f_S), ranging from 80 MHz to 250 MHz, is obtained after the output frequency divider (`PLL_OUTDIV<3:0>`). For stable operation, the user needs to configure the PLL with the following limits:

- Input clock frequency (f_{REF}) = 5 MHz to 250 MHz
- Maximum frequency at charge pump input (after PLL reference divider) = 50 MHz
- VCO output frequency = 1.075 to 1.325 GHz
- PLL output frequency after output divider = 80 MHz to 250 MHz

The charge pump is controlled by the PFD, and forces sink (DOWN) or source (UP) current pulses onto the loop filter. The charge pump bias current is controlled by the `PLL_CHAGPUMP<3:0>` bits, approximately 25 μ A per step. The loop filter consists of a 3rd order passive RC filter. [Table 4-4](#) shows the recommended settings of the charge pump and loop filter parameters, depending on the charge pump input frequency range (output of the reference frequency divider).

When the PLL is locked, it tracks the input frequency (f_{REF}) with the ratio of dividers (N/R). The PLL operating status is monitored by the PLL status indication bits: `<PLL_VCOL_STAT>` and `<PLL_VCOH_STAT>` in Address 0xD1 ([Register 5-81](#)).

[Equation 4-3](#) shows the VCO output frequency (f_{VCO}) as a function of the two dividers and reference frequency:

EQUATION 4-3: VCO OUTPUT FREQUENCY

$$f_{VCO} = \left(\frac{N}{R}\right)f_{REF} = 1.075 \text{ (GHz) to } 1.325 \text{ (GHz)}$$

Where:

- N = 1 to 4095 controlled by `PLL_PRE<11:0>`
- R = 1 to 1023 controlled by `PLL_REFDIV<9:0>`

See Address 0x54 to 0x57 (Register 5-9 to 5-12) for these bits settings.

The tuning range of the VCO is 1.075 GHz to 1.325 GHz. N and R values must be chosen such that the VCO is within this range. In general, lower values of the VCO frequency (f_{VCO}) and higher values of the charge pump frequency (f_Q) should be chosen to optimize the clock jitter. Once the VCO output frequency is determined to be within this range, the user needs to set the final ADC sampling frequency (f_S) with the PLL output divider using `PLL_OUTDIV<3:0>`.

EQUATION 4-4: SAMPLING FREQUENCY

$$f_S = \left(\frac{f_{VCO}}{PLL_OUTDIV}\right) = 80 \text{ MHz to } 250 \text{ MHz}$$

[Table 4-5](#) shows an example of generating $f_S = 200$ MHz output using the PLL control parameters.

Note 1: In normal operation, the PLL maintains lock across all temperature ranges. It is not necessary to actively monitor the PLL unless extreme variations in the supply voltage are expected or the chip input frequency has been changed.

2: PLL recalibration is recommended when PLL control parameter settings are changed.

MCP37231/21-200 AND MCP37D31/21-200

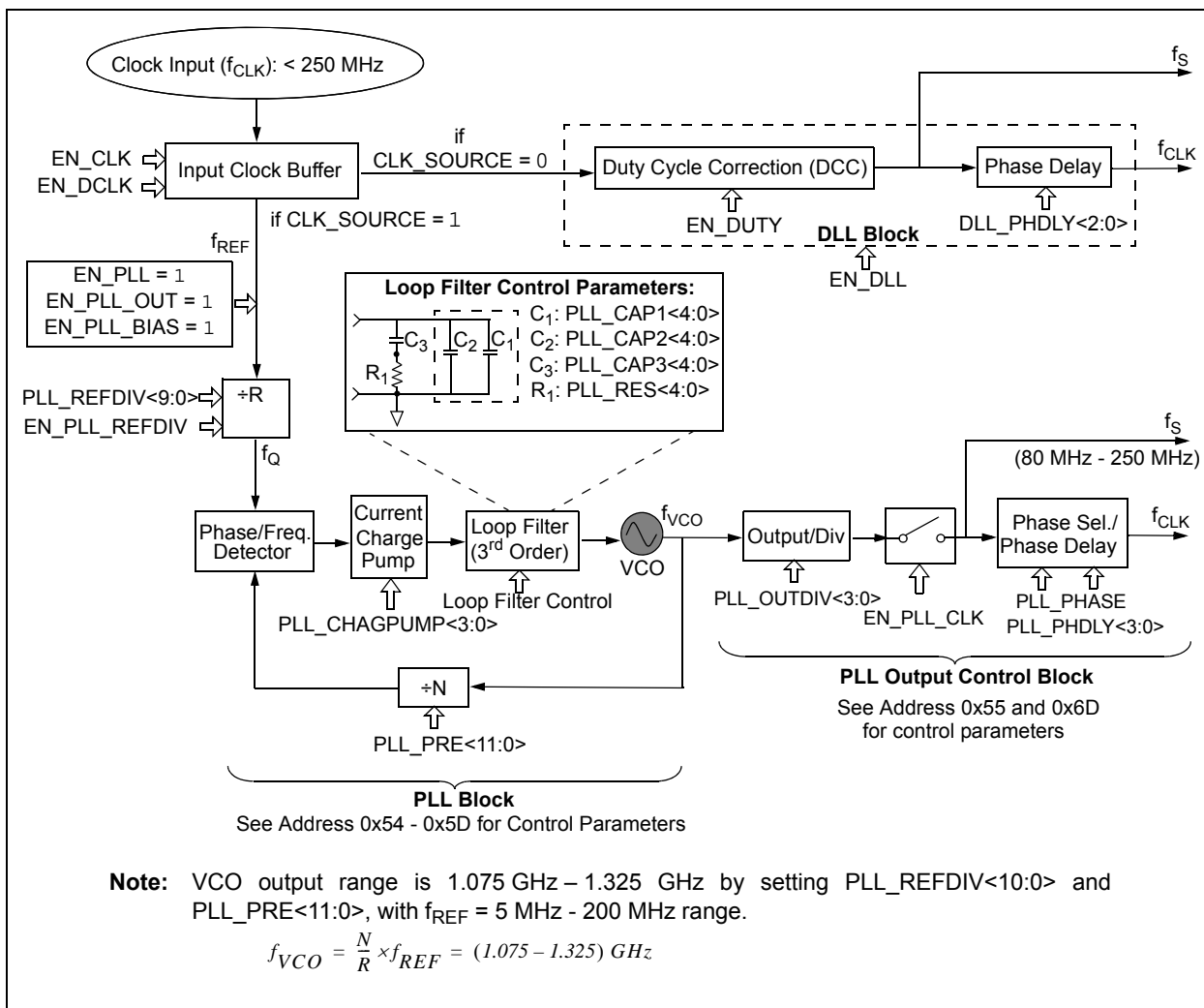


FIGURE 4-11: PLL and DLL Control Blocks.

TABLE 4-3: CONTROL PARAMETERS FOR PLL AND CLK

| Control Parameter | Register | Descriptions |
|---|----------|--|
| Clock Source Control | | |
| CLK_SOURCE | 0x53 | Select internal timing source CLK_SOURCE = 1 selects the PLL output as the ADC clock source. |
| EN_DUTY | 0x52 | Enable duty cycle correction of the clock input when external clock input is selected as timing source (Note 1) |
| PLL Calibration and Status Indication Bits | | |
| PLL_CALTRIG | 0x6B | PLL circuit calibration (Note 2) |
| PLL_CAL_STAT | 0xD1 | PLL auto-calibration status indication |
| PLL_VCOL_STAT | 0xD1 | PLL drifts out-of-lock with low VCO frequency |
| PLL_VCOH_STAT | 0xD1 | PLL drifts out-of-lock with high VCO frequency |

Note 1: Duty cycle correction is not recommended when high quality external clock is used.

Note 2: PLL recalibration is needed after reprogramming of the PLL block.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 4-3: CONTROL PARAMETERS FOR PLL AND CLK (CONTINUED)

| Control Parameter | Register | Descriptions |
|--|-----------|---|
| PLL Global Variable Setting Bits | | |
| EN_PLL | 0x59 | Master enable bit for the PLL circuit |
| EN_PLL_OUT | 0x5F | Master enable bit for the PLL output |
| EN_PLL_BIAS | 0x5F | Master enable bit to enable the PLL bias |
| EN_PLL_REFDIV | 0x59 | Master enable bit for the PLL circuit. Enable PLL reference divider |
| EN_PLL_CLK | 0x6D | EN_PLL_CLK = 1 enable PLL output clock to the ADC circuits |
| PLL_PHDLY<3:0> | 0x6D | Delay PLL Output up to 15 cycles of VCO clocks |
| PLL_PHASE | 0x6D | Select PLL phase for delay line |
| PLL Block and PLL Output Control Settings | | |
| PLL_REFDIV<9:0> | 0x54-0x55 | PLL Reference Divider (R) (See Table 4-5) |
| PLL_PRE<11:0> | 0x56-0x57 | PLL Prescaler (N) (See Table 4-5) |
| PLL_OUTDIV<3:0> | 0x55 | PLL Output Divider (See Table 4-5) |
| PLL_CHAGPUMP<3:0> | 0x58 | PLL charge pump bias current control: from 25 μ A to 375 μ A, 25 μ A per step |
| PLL_RES<4:0> | 0x5A | PLL loop filter resistor value selection (See Table 4-4) |
| PLL_CAP3<4:0> | 0x5A | PLL loop filter capacitor 3 value selection (See Table 4-4) |
| PLL_CAP2<4:0> | 0x5D | PLL loop filter capacitor 2 value selection (See Table 4-4) |
| PLL_CAP1<4:0> | 0x5C | PLL loop filter capacitor 1 value selection (See Table 4-4) |

Note 1: Duty cycle correction is not recommended when high quality external clock is used.

2: PLL recalibration is needed after reprogramming of the PLL block.

TABLE 4-4: RECOMMENDED PLL CHARGE PUMP AND LOOP FILTER PARAMETER VALUE SETTINGS EXAMPLE

| PLL Charge Pump and Loop Filter Parameter (Note 1) | $f_Q = f_{REF}/PLL_REFDIV$ | | |
|--|-----------------------------|---|--------------------------|
| | $5\text{ MHz} > f_Q$ | $5\text{ MHz} \leq f_Q < 25\text{ MHz}$ | $25\text{ MHz} \leq f_Q$ |
| PLL_CHAGPUMP<3:0> | 0x04 | 0x04 | 0x04 |
| PLL_RES<4:0> | 0x1F | 0x1F | 0x07 |
| PLL_CAP3<4:0> | 0x07 | 0x02 | 0x07 |
| PLL_CAP2<4:0> | 0x07 | 0x01 | 0x08 |
| PLL_CAP1<4:0> | 0x07 | 0x01 | 0x08 |

Note 1: See [Table 4-3](#) for the parameter details.

TABLE 4-5: EXAMPLE PLL CONTROL PARAMETERS FOR GENERATING $f_S = 200\text{ MHz}$ WITH $f_{REF} = 100\text{ MHz}$

| PLL Control Parameter | Value | Descriptions |
|---------------------------|---------|--|
| f_{REF} | 100 MHz | f_{REF} is coming from the external clock input |
| Target f_{VCO} | 1.2 GHz | Range of $f_{VCO} = 1.0375\text{ GHz} - 1.325\text{ GHz}$ |
| Target f_S | 200 MHz | ADC sampling frequency (Note 2) |
| Target f_Q | 10 MHz | $f_Q = f_{REF}/PLL_REFDIV$ (See Table 4-4) |
| PLL Reference Divider (R) | 10 | PLL_REFDIV<9:0> = 0x0A (Note 1) |
| PLL Prescaler (N) | 120 | PLL_PRE<11:0> = 0x78 (Note 1) |
| PLL Output Divider | 6 | PLL_OUTDIV<3:0> = 0x06 (Note 2) |

Note 1: $f_{VCO} = (N/R) \times f_{REF} = (12) \times 100\text{ MHz} = 1.2\text{ GHz}$

2: $f_S = f_{VCO}/PLL_OUTDIV = 1.2\text{ GHz}/6 = 200\text{ MHz}$

MCP37231/21-200 AND MCP37D31/21-200

4.8 Digital Signal Post-Processing (DSPP) Options

While the device converts the analog input signals to digital output codes, the user can enable various digital signal post-processing options for special applications.

These options are individually enabled or disabled by setting the configuration bits. Table 4-6 summarizes the digital signal post-processing (DSPP) options that are available for each device family.

TABLE 4-6: DIGITAL SIGNAL POST PROCESSING (DSPP) OPTIONS

| Digital Signal Post Processing Option | Available Operating Mode | Offering Device |
|--|--|------------------------------------|
| Fractional Delay Recovery (FDR) | Dual and octal-channel modes | MCP37231/21-200 MCP37D31/21-200 |
| FIR Decimation Filters | Single and dual-channel modes CW octal-channel mode DDC for I and Q data | |
| Digital Gain and Offset correction per channel | Available for all channels | |
| Digital-Down Conversion (DDC) | Single and dual-channel modes CW octal-channel mode | MCP37D31/21-200 |
| Continuous Wave (CW) Beamforming | CW octal-channel mode | |

4.8.1 FRACTIONAL DELAY RECOVERY FOR DUAL AND OCTAL-CHANNEL MODES

When the device is used in multi-channel mode, it samples the channel inputs sequentially using a MUX while the ADC core is operating at a constant full speed. This sequential sampling of multiple channels introduces a time delay between the sampling of different input channels relative to a multi-core ADC which would sample all inputs at the same instant. The fractional delay recovery (FDR) option digitally compensates the time delay of the sampling events.

This FDR feature is available in dual and octal-channel modes only. When the FDR is enabled, a high-order, band-limited interpolation filter de-skews the sampling instant within a limited input bandwidth and synthetically removes the time delay of the input sampling. Figure 4-12 shows the simplified block diagram for the ADC output data path with FDR. The related configuration register bits are listed in Table 4-7.

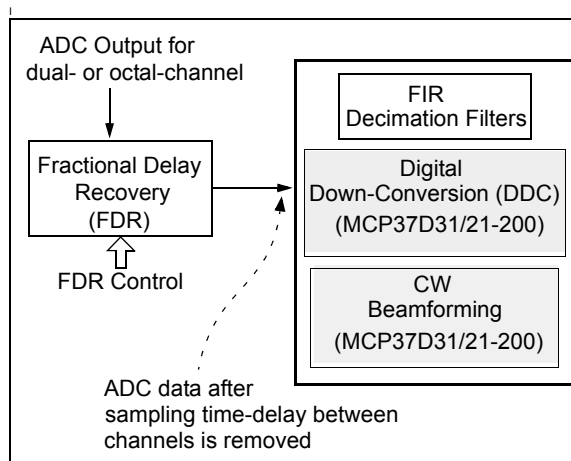


FIGURE 4-12: Simplified Block Diagram for ADC Output Data Path with Fractional Delay Recovery Option. Note that Fractional Delay Recovery occurs prior to other DSPP features.

TABLE 4-7: CONTROL PARAMETERS FOR FRACTIONAL DELAY RECOVERY (FDR)

| Channel Operation | Control Parameter | Register | Descriptions |
|--|-------------------|----------|---|
| Global Control for both dual and octal-channel modes | EN_FDR = 1 | 0x7A | Enable FDR features |
| | FDR_BAND | 0x81 | Select 1 st or 2 nd Nyquist band |
| Dual-Channel | SEL_FDR = 0 | 0x81 | Select FDR for dual-channel mode |
| | SEL_DSPP = 0 | 0x81 | Select digital signal post-processing (DSPP) feature for dual-channel mode |
| | EN_DSPPDUAL = 1 | 0x79 | Enable all digital post-processing functions for dual-channel operation |
| Octal-Channel | SEL_FDR = 1 | 0x81 | Select FDR for octal-channel mode |
| | SEL_DSPP = 1 | 0x81 | Select digital signal post-processing (DSPP) feature for octal-channel mode |

MCP37231/21-200 AND MCP37D31/21-200

Table 4-8 shows the input bandwidth limits of the FDR feature for distortion less than 0.1 mdB (0.1×10^{-3} dB), where f_s is the sampling frequency per channel. Figures 4-13 and 4-14 show the responses of the dual-channel and octal-channel FDRs, respectively.

TABLE 4-8: INPUT BANDWIDTH REQUIREMENT FOR FDR

| Bandwidth in percentage of f_s (1) | Nyquist Band |
|--------------------------------------|------------------------------|
| Dual-Channel Mode | |
| 0 – 45% | 1 st Nyquist Band |
| 55 – 100% | 2 nd Nyquist Band |
| 45 – 55% | Avoid |
| Octal-Channel Mode | |
| 0 – 38% | 1 st Nyquist Band |

Note 1: f_s is sampling frequency per channel. Distortion is less than 0.1 mdB

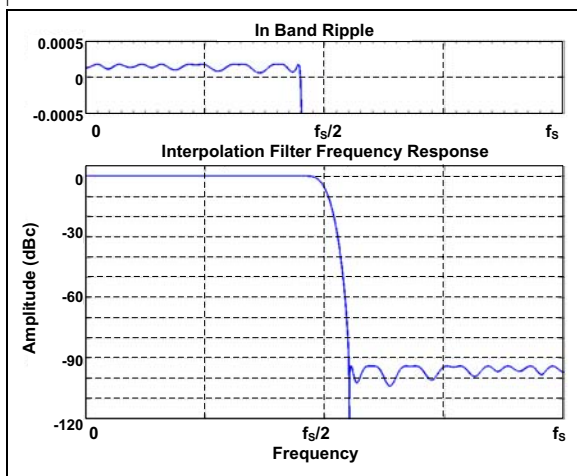


FIGURE 4-13: Response of the Dual-Channel Fractional Delay Recovery. f_s is the Sampling Frequency.

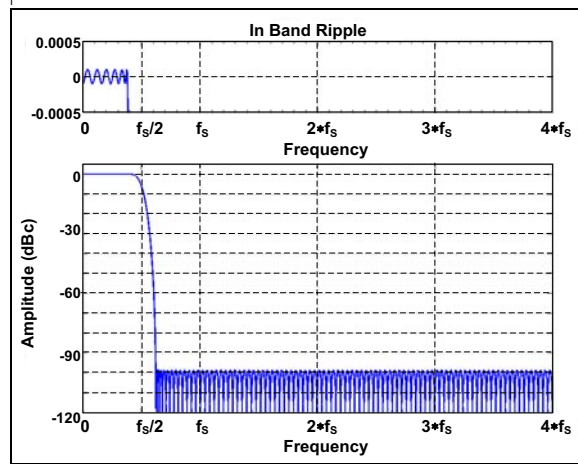


FIGURE 4-14: Response of the Octal-Channel Fractional Delay Recovery. f_s is the Sampling Frequency.

4.8.2 DECIMATION FILTERS

The decimation feature is available in single and dual-channel modes. Figure 4-15 shows a simplified decimation filter block, and Table 4-11 shows the Register settings. The decimation rate is controlled by FIR_A<8:0> and FIR_B<7:0> settings in Addresses 0x7A – 0x7C (Registers 5-35 to 5-37). These registers are thermometer encoded.

In single-channel mode, FIR B is disabled and only FIR A is used. In this mode, the maximum programmable decimation rate is 512x using nine cascaded decimation stages.

In dual-channel mode or when using the Digital Down-Conversion (DDC) in I/Q mode, both FIR A and FIR B are used (see Figure 4-15). In this case, both channels are set to the same decimation rate. Note that stage 1A in FIR A is unused: the user must clear FIR_A<0> in Address 0x7A (Register 5-35). In dual-channel mode, the maximum programmable decimation rate is up to 256x, which is $\frac{1}{2}$ of the single channel decimation rate (512x).

The overall SNR performance can be improved with higher decimation rate. In theory, 3 dB improvement is expected with each successive stage of decimation (2x per stage), but the actual improvement is approximately 2.5 dB per stage due to finite attenuation in the FIR filters.

When using a high decimation rate option (128x or above), the user may consider enabling two additional output bits using DM1DM2 bit setting in Address 0x68 (Register 5-26).

Table 4-9 summarizes the decimation rate versus SNR performance in 16-bit and 18-bit output modes. The results indicate that the SNR is marginally improved with higher decimation rates. Therefore, the user may have a benefit with the 18-bit output mode when high

MCP37231/21-200 AND MCP37D31/21-200

decimation rate is used. When a low decimation rate is used, there is no benefit to SNR or SFDR of the ADC by enabling the 18-bit output.

When decimation is used, it also reduces the output clock rate and output bandwidth by a factor equal to the decimation rate applied: the output clock rate is therefore no longer equal to the ADC sampling clock. The user needs to adjust the output clock and data rates in Address 0x02 ([Register 5-3](#)) based on the decimation applied. The DLL should also be disabled in this mode. This allows the output data to be synchronized to the output data clock.

Phase shifts in the output clock can be achieved using DCLK_PHDLY_DEC<2:0> in Address 0x64 ([Register 5-22](#)). When decimation of 2x is used, only four output sampling phases are available, while all eight clock phases are available for other decimation rates. [Table 4-10](#) summarizes the related control parameters for using decimation filters.

4.8.2.1 Using Decimation with CW beamforming and Digital Down-Conversion

Decimation can be used in conjunction with CW octal-channel mode or DDC. In CW octal-channel mode operation, the 8-input channels are summed into a single channel prior to entering the decimation filters. When DDC is enabled, the I and Q outputs can be decimated using the same signal path for the dual-channel mode: I and Q data are fed into Channel A and B, respectively.

In DDC mode, the half-band filter already includes a 2x decimation. Therefore, the maximum decimation rate setting for I/Q filtering is 128x for the FIR_A<8:1> and FIR_B<7:0>. See [Section 4.8.3 “Digital Down-Conversion \(MCP37D31/21-200 only\)”](#) for details.

Note: Fractional Delay Recovery, Digital Gain/Offset adjustment and DDC for I/Q data options occur prior to the decimation filters if they are enabled.

TABLE 4-9: DECIMATION RATE VS. SNR PERFORMANCE

| Decimation Rate | SNR (dBFS) | |
|-----------------|--------------------|---|
| | 16-Bit Output Mode | 18-Bit Output Mode (Note 1) |
| 8x | 82.3 | — |
| 16x | 84.8 | — |
| 32x | 87.1 | 87.4 |
| 64x | 89.2 | 89.7 |
| 128x | 91.0 | 91.8 |
| 256x | 92.0 | 93.2 |
| 512x | 92.3 | 93.5 |

Note 1: DM1DM2 bit is enabled.

TABLE 4-10: REGISTER CONTROL PARAMETERS FOR USING DECIMATION FILTERS

| Control Parameter | Register | Descriptions |
|--|------------|--|
| Decimation Filter Settings | | |
| FIR_A<8:0> | 0x7A, 0x7B | Channel A FIR configuration for single or dual-channel mode |
| FIR_B<7:0> | 0x7C | Channel B FIR configuration for single or dual-channel mode |
| Output Data Rate and Clock Rate Settings (Note 1) | | |
| OUT_DATARATE<3:0> | 0x02 | Output data rate: Equal to decimation rate |
| OUT_CLKRATE<3:0> | 0x02 | Output clock rate: Equal to decimation rate |
| Output Clock Phase Control Settings (Note 2) | | |
| EN_PHDLY_DEC | 0x64 | Enable digital output phase delay when decimation filter is used |
| DCLK_PHDLY_DEC<2:0> | 0x64 | Digital output clock phase delay control |
| Digital Signal Post-Processing (DSPP) Function Block Settings | | |
| EN_DSPPDUAL | 0x79 | Enable dual-channel decimation. |

Note 1: The output data and clock rates must be updated when decimation rates are changed.

Note 2: Output clock (DCLK) phase control is used when the output clock is divided by OUT_CLKRATE<3:0> bit settings.

MCP37231/21-200 AND MCP37D31/21-200

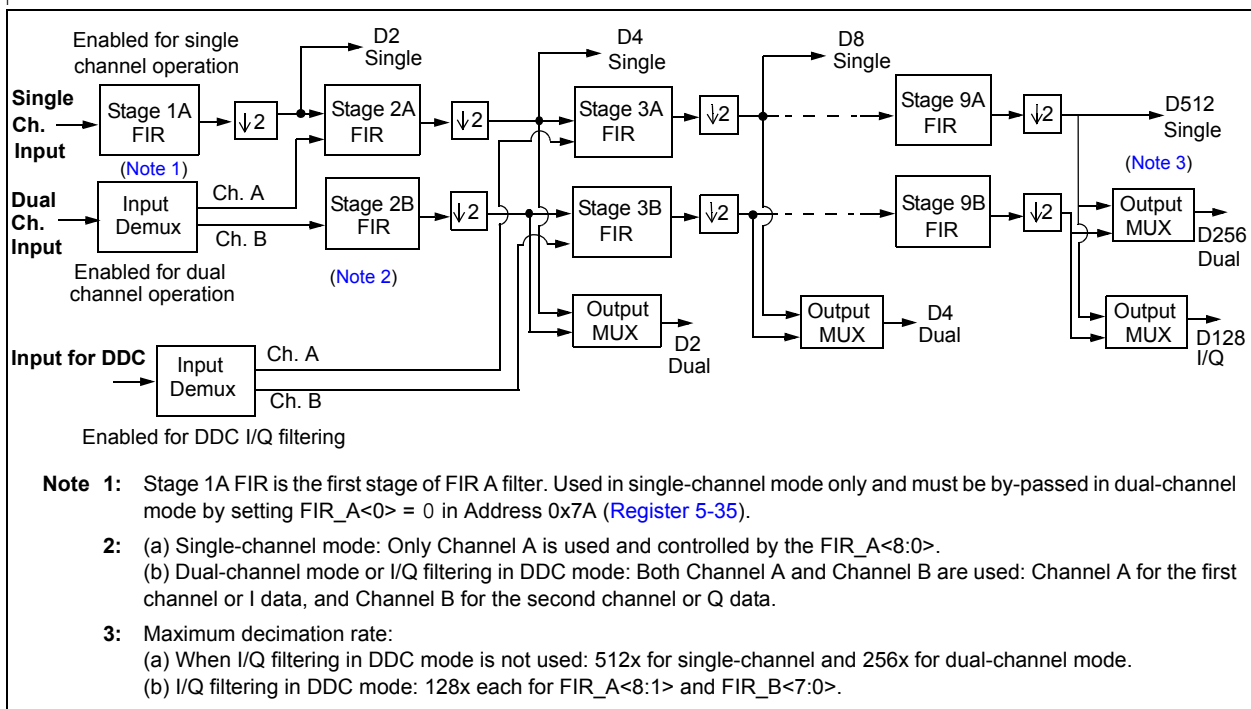


FIGURE 4-15: Simplified Block Diagram of Decimation Filters.

4.8.3 DIGITAL DOWN-CONVERSION (MCP37D31/21-200 ONLY)

The Digital Down-Conversion (DDC) feature is available in single, dual and CW octal-channel modes in MCP37D31/21-200. This feature can be optionally combined with the decimation filter and used to:

- translate a portion of the input frequency spectrum to lower frequencies
- remove the unwanted out-of-band portion
- output the resulting signal as either I/Q data or a real signal centered at $\frac{1}{4}$ of the output data rate.

For example, if the ADC is sampling a single-channel input at 200 Msps, but the user is only interested in a 5 MHz span which is centered at 67 MHz, the digital down-conversion may be used to mix the sampled ADC data with 67 MHz to convert it to DC. The resulting signal can then be decimated by 16x such that the bandwidth of the ADC output is 6.25 MHz (200 Msps/16x decimation gives 12.5 Msps with 6.25 MHz Nyquist bandwidth). If $f_s/8$ mode is selected, then a single 25 Msps channel is output, where 6.25 MHz in the output data corresponds to 67 MHz at the ADC input. If I/Q mode is selected, then two 12.5 Msps channels are output, where DC corresponds to 67 MHz and the channels represents In-Phase and Quadrature components of the down-conversion. Figure 4-16 and Figure 4-17 show the DDC block diagrams of single and dual-channels, respectively. Figure 4-18 and Figure 4-19 show the half-band filter responses.

This DDC feature can be used in a variety of high-speed signal-processing applications, including digital radio, wireless base stations, radar, cable modems, digital video, etc. Since the processing is achieved completely in the digital domain, the result is not affected by classical nonlinearities typical in analog implementations.

4.8.3.1 Single-Channel DDC

Figure 4-16 shows the single-channel DDC configuration. The DDC includes a 32-bit numerically controlled oscillator (NCO), a selectable (high/low) half-band filter, optional decimation, and two output modes (I/Q or $f_s/8$). Phase and amplitude dither may be enabled for the NCO with a negligible performance penalty. Each of these processing sub-blocks are individually controlled. Examples of setting registers for selected output type are shown in Tables 4-11 and 4-12 in Section 4.8.4 “Examples of Register Settings for Using Decimation and DDC”.

MCP37231/21-200 AND MCP37D31/21-200

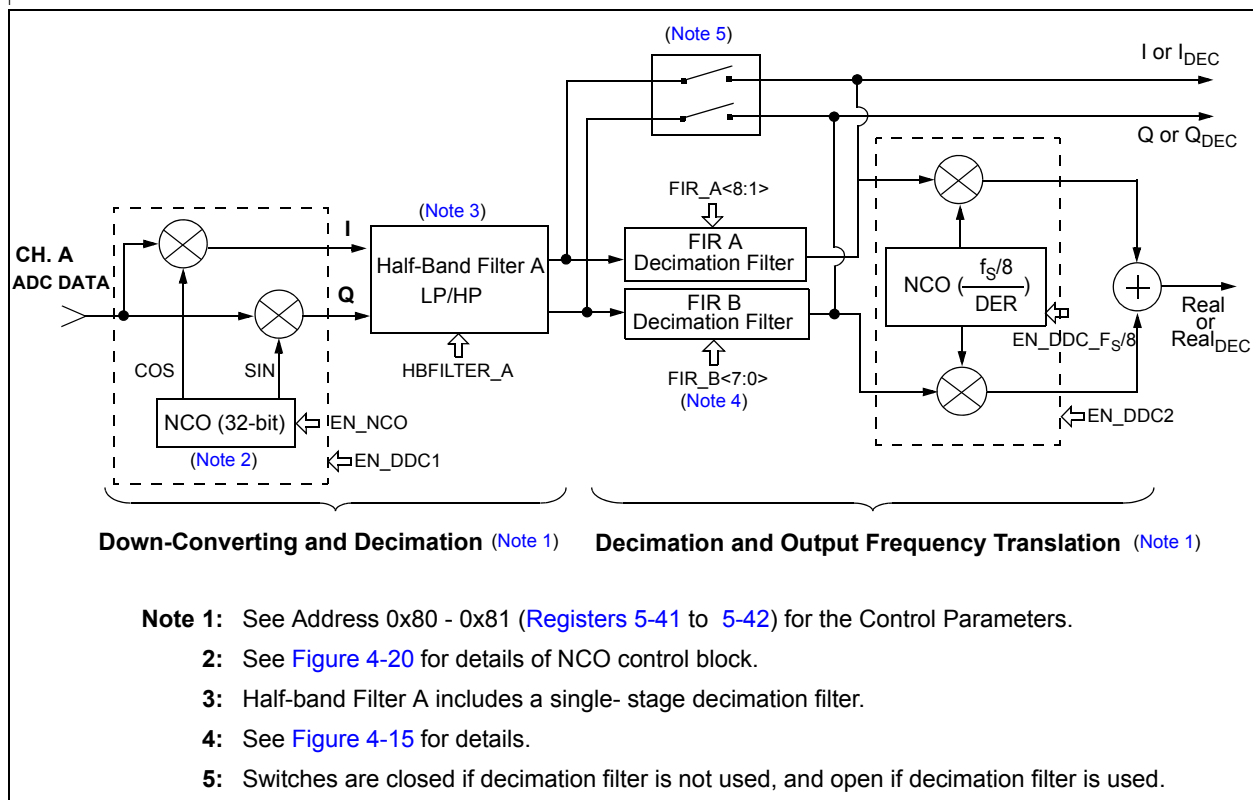


FIGURE 4-16: Simplified DDC Block Diagram for Single-Channel Mode. See Tables 4-11 and 4-12 for Using this DDC Block.

4.8.3.2 Dual-Channel DDC

Figure 4-17 shows the dual-channel DDC configuration. Each channel includes the same processing elements as shown in the single-channel DDC, however the I/Q outputs cannot be separately decimated since the device only supports two channels of decimation (four would be required for I/Q of Channel A and I/Q of Channel B). The decimation option can be used if the DDC output after the half-band filter is up-converted by $f_s/8$ for each channel. Otherwise, I/Q of each channel will be output separately similar to a 4-channel input device with the WCK output pin toggling synchronously with the I-data of Channel A. Note that the NCO phase can be adjusted uniquely for each of the two input channels (see Figure 4-20). Examples of setting registers for selected output type are shown in Tables 4-13 and 4-14.

MCP37231/21-200 AND MCP37D31/21-200

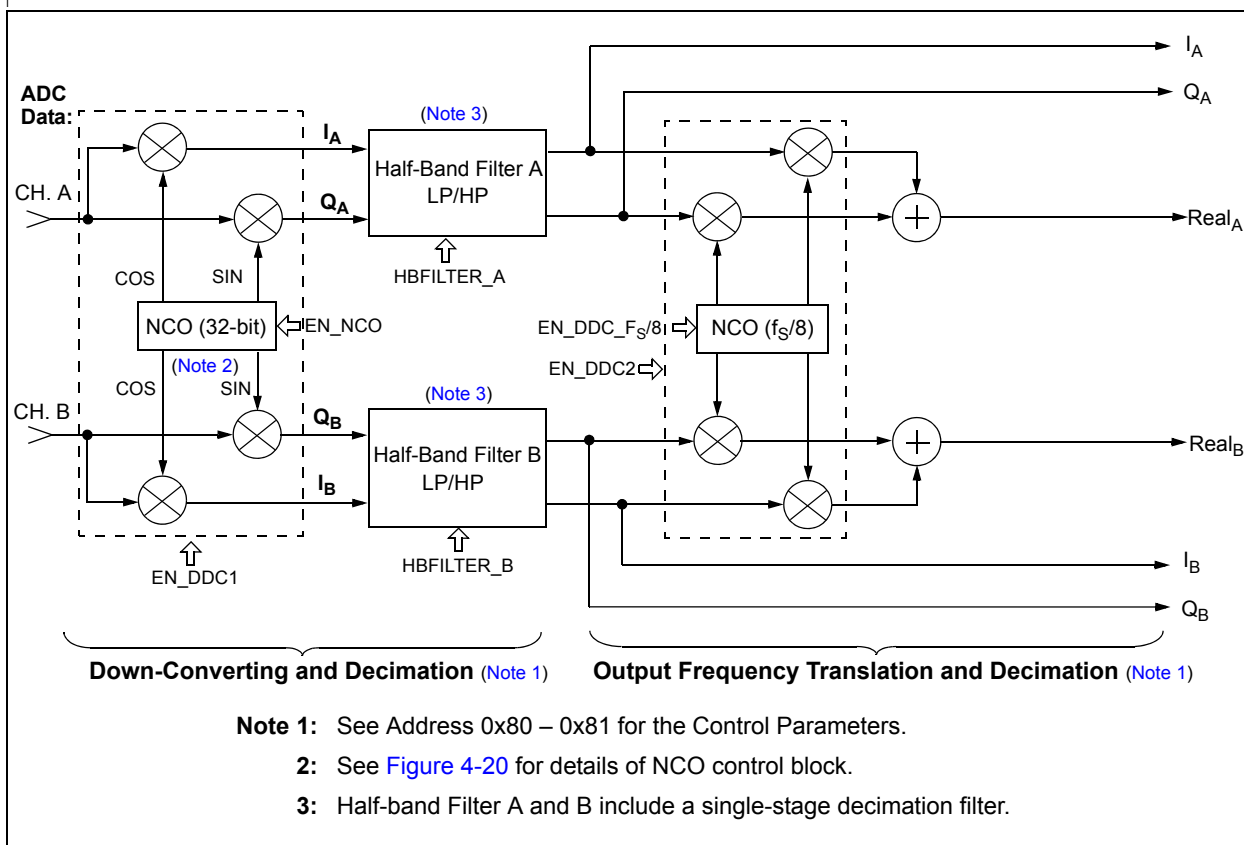


FIGURE 4-17: Simplified DDC Block Diagram for Dual-Channel Mode. See Tables 4-13 and 4-14 for Using this DDC Block.

4.8.3.3 Half-Band Filter

The half-band digital filter is used to reduce the sample rate by a factor of 2 while rejecting aliases that fall into the band of interest. This filter is designed to operate as either a low-pass or a high-pass filter, and to provide greater than 90 dB of attenuation for 20% of the input sampling rate (f_s). For an ADC sample rate of 200 Msps, this provides a 1 mdB (10^{-3} dB) bandwidth of 40 MHz. The half-band filter is configured using the HBFILTER_A and HBFILTER_B parameters in Address 0x80 (Register 5-41). The filter responses of the half-band filter shown in Figures 4-18 and 4-19 indicate a ripple of 0.5 mdB and an alias rejection of 90 dB. The output of the half-band filter is a DC-centered complex signal (I and Q). This I and Q signal is then carried to the next down-conversion stage (DDC2) for frequency translation (up-conversion), if the DDC is enabled.

Note: The half-band filter delays the data output by 80 clock cycles: 2 (due to decimation) x 40 cycles (due to propagations)

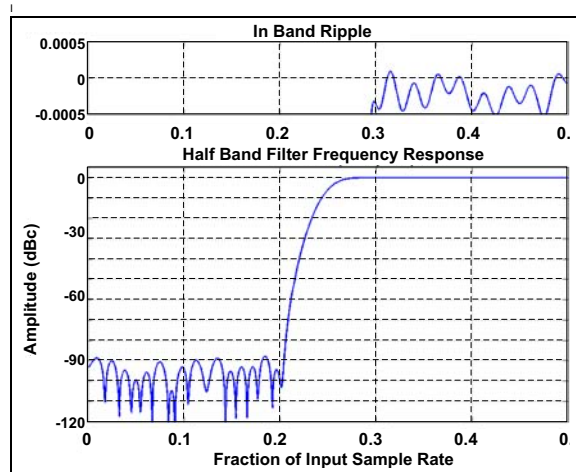


FIGURE 4-18: High-Pass (HP) Response of Half-Band Filter.

MCP37231/21-200 AND MCP37D31/21-200

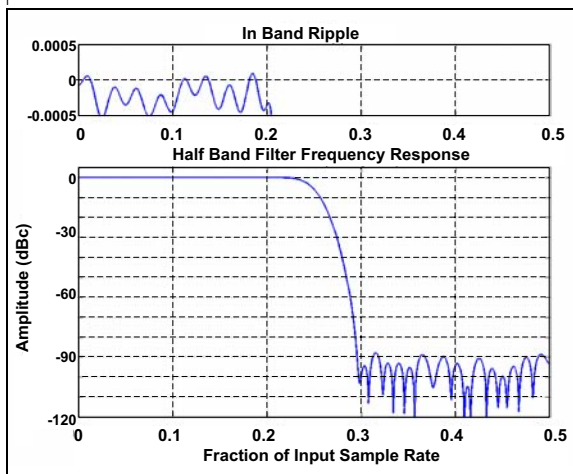


FIGURE 4-19: Low-Pass (LP) Response of Half-Band Filter.

4.8.3.4 Numerically Controlled Oscillator (NCO)

The on-board Numerically Controlled Oscillator (NCO) provides the frequency reference for the In-Phase and Quadrature mixers in the digital down-converter (DDC). Figure 4-20 shows the control signals associated with the NCO. In Octal or dual-channel mode, the NCO allows the output phase to be adjusted on a per-channel basis.

Note: The NCO is only used for DDC or CW octal-channel mode. It should be disabled when not in use.

The NCO frequency is programmed using the 32-bit wide unsigned register variable NCO_TUNE<31:0> in Addresses 0x82 – 0x85 (Registers 5-43 to 5-46). The following equation is used to setup the NCO_TUNE<31:0> setting:

EQUATION 4-5: NCO FREQUENCY

$$NCO_TUNE<31:0> = \text{round}\left(2^{32} \times \frac{\text{Mod}(f_{NCO}, f_S)}{f_S}\right)$$

Where:

f_S = sampling frequency (Hz)

f_{NCO} = desired NCO frequency (Hz)

Mod (f_{NCO}, f_S) = gives the remainder of f_{NCO}/f_S

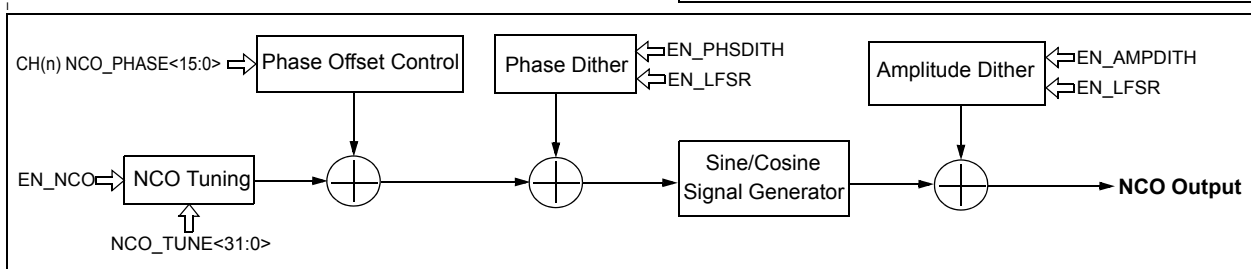


FIGURE 4-20: NCO block diagram

4.8.3.5 NCO Amplitude and Phase Dither

The EN_AMPDITH and EN_PHSDITH parameters in Address 0x80 (Register 5-41) can be used for amplitude and phase dithering, respectively. In principle, these will dither the quantization error created by the use of digital circuits in the mixer and local oscillator, thus reducing spurs at the expense of noise. In practice, the DDC circuitry has been designed with sufficient noise and spurious performance for most applications. In the worst case scenario, the NCO has an SFDR of greater than 116 dB when the amplitude dither is enabled and 112 dB when disabled. Although the SNR (~93 dB) of the DDC is not significantly affected by the dithering option, using the NCO with dithering options enabled is always recommended for the best performance.

4.8.3.6 NCO for $f_S/8$ and $f_S/(8xDER)$

The output of the first down-conversion block (DDC1) is a complex signal (comprising I and Q data) which can then be optionally decimated further up to 64x to provide both a lower output data rate and input channel filtering. If $f_S/8$ mode is enabled, a second mixer stage (DDC2) will convert the I/Q signals to a real signal centered at half of the current Nyquist frequency; i.e., if the output data rate in I/Q mode is 25 Msps per channel (12.5 MHz Nyquist), then in $f_S/8$ mode the output data rate would be 50 Msps, and the signal would be re-centered around 12.5 MHz. In single-channel mode, this is done at the output of the decimation filters (if used). In dual-channel mode, this must be done prior to the decimation. When decimation is enabled, the I/Q outputs are up-converted by $f_S/(8xDER)$, where DER is the additional decimation rate added by the FIR decimation filters. This provides a decimated output signal centered at $f_S/8$ or $f_S/(8xDER)$ in the frequency domain.

MCP37231/21-200 AND MCP37D31/21-200

4.8.3.7 NCO Phase Offset Control

The user can add phase offset to the NCO frequency using the NCO phase offset control registers (Addresses 0x86 to 0x95 – [Registers 5-47](#) to [5-62](#)). CH(n)_NCO_PHASE<15:0> is the 16-bit wide NCO phase offset control parameter for Channel *n*. A 0x0000 value in the register corresponds to no offset, and a 0xFFFF corresponds to an offset of 359.995°. The phase offset can be controlled with 0.005° per step. The following equation is used to program the NCO phase offset register:

EQUATION 4-6: NCO PHASE OFFSET

$$CH(n)_NCO_PHASE<15:0> = 2^{16} \times \frac{\text{Offset Value } (\phi)}{360}$$

Where:

n = channel number

Offset Value (ϕ) = desired phase offset value in degrees

A decimal number is used for the binary contents of the CH(n)_NCO_PHASE<15:0>.

4.8.3.8 In-Phase and Quadrature Signals

When the first down-conversion is enabled, it produces In-phase (I) and Quadrature (Q) components given by:

EQUATION 4-7: I AND Q SIGNALS

$$I = ADC \times \cos(2\pi f_{NCO}t + \phi) \quad (a)$$

$$Q = ADC \times \sin(2\pi f_{NCO}t + \phi) \quad (b)$$

where:

$$\phi = 360 \times \frac{CH(n)_NCO_PHASE<15:0>}{2^{16}} \quad (c)$$

$$= 0.005493164^\circ \times CH(n)_NCO_PHASE<15:0>$$

where:

ADC = output of the ADC block

ϕ = NCO phase offset of selected channel which is defined by the CH(n)_NCO_PHASE<15:0> in Address 0x86 - 0x95

t = *k*/f_S, with *k* = 1, 2, 3, ..., *n*

f_{NCO} = NCO frequency

I and Q data are output in an interleaved fashion where I data is output on the rising edge of the WCK. If I and Q output are selected in dual-channel mode with DDC enabled, I data of Channel 0 is output at the rising edge of WCK, followed by Q data of Channel 0, then I and Q data of Channel 1.

MCP37231/21-200 AND MCP37D31/21-200

4.8.4 EXAMPLES OF REGISTER SETTINGS FOR USING DECIMATION AND DDC

The following tables show examples of setting registers for using decimation and digital down-conversion (DDC) depending on the output type selection. This feature is available in MCP37D31/21-200 device only.

TABLE 4-11: REGISTER SETTINGS FOR DECIMATION AND DDC OPTIONS FOR SINGLE-CHANNEL MODE – EXAMPLE

| Decimation Rate (by FIR A and FIR B) (Note 6) | DDC Mode | Addr. 0x02 (Note 1) | FIR A Filter | | FIR B Filter | DDC1 | DDC2 | Dual-Channel DSPP Control | Output |
|---|----------|---------------------------|-----------------------|----------------------|----------------------|-------------------------|-------------------------|------------------------------|--|
| | | | 0x7A<6> (FIR_A<0>) | 0x7B (FIR_A<8:1>) | 0x7C (FIR_B<7:0>) | 0x80<5,1,0> (Note 2) | 0x81<6,3,2> (Note 3) | 0x79<7> (EN_DSPPDUAL) | |
| 0 | Disabled | 0x00 | 0 | 0x00 | 0x00 | 0,0,0 | 0,0,0 | 0 | ADC |
| 8 | Disabled | 0x33 | 1 | 0x03 | 0x00 | 0,0,0 | 0,0,0 | 0 | ADC with decimation (÷8) |
| 512 | Disabled | 0x99 | 1 | 0xFF | 0x00 | 0,0,0 | 0,0,0 | 0 | ADC with decimation (÷512) |
| 0 | I/Q | 0x00 (Note 4) | 0 | 0x00 | 0x00 | 1,0,1 | 0,0,0 | 0 | I/Q Data |
| 8 | I/Q | 0x33 | 0 | 0x07 | 0x07 | 1,0,1 | 0,0,0 | 0 | Decimated I/Q (÷8) |
| 0 | $f_S/8$ | 0x11 (Note 5) | 0 | 0x00 | 0x00 | 1,1,1 | 0,0,0 | 0 | Real without using decimation filter (÷2) |
| 8 | $f_S/8$ | 0x44 | 0 | 0x07 | 0x07 | 1,0,1 | 1,0,0 | 0 | Real with decimation (÷16) |

- Note 1:** Output data and clock rate control register.
Note 2: 0x80<5,1,0> = <EN_NCO, EN_DDC_FS/8, EN_DDC1>.
Note 3: 0x81<6,3,2> = <EN_DDC, SEL_DSPP, 8CH_CW>.
Note 4: Each of I/Q has 1/2 of f_S bandwidth. The combined bandwidth is the same as the f_S bandwidth. Therefore the data rate adjustment is not needed.
Note 5: Data rate is reduced by half since the Half-Band Filter A includes decimation of 2.
Note 6: This decimation value is set using the decimation filter. When DDC is used, the actual total decimation is 2x larger since 2x is included from the DDC Half-Band Filter. Example: “single-channel, Decimation = 8x, DDC-IQ” option actually has 16x decimation with 8x provided by the decimation filter and 2x from the DDC Half-Band Filter.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 4-12: OUTPUT TYPE VS. CONTROL PARAMETERS FOR SINGLE-CHANNEL DDC – EXAMPLE

| Output Type | Control Parameter | Register | Descriptions |
|--|-------------------------|----------|---|
| Complex: I and Q | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | EN_DDC_FS/8 = 0 | 0x81 | NCO($f_S/8/DER$) is disabled |
| | EN_DDC2 = 0 | 0x80 | DDC2 is disabled |
| | FIR_A<8:1> = 0x00 | 0x7B | FIR A decimation filter is disabled |
| | FIR_B<7:0> = 0x00 | 0x7C | FIR B decimation filter is disabled |
| | OUT_CLKRATE<3:0> | 0x02 | Output clock rate is not affected (no need to change) |
| Decimated I and Q: I_{DEC} , Q_{DEC} | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | EN_DDC_FS/8 = 0 | 0x81 | NCO($f_S/8/DER$) is disabled |
| | EN_DDC2 = 0 | 0x80 | DDC2 is disabled |
| | FIR_A<8:1> | 0x7B | Program FIR A filter for extra decimation (Note 1) |
| | FIR_B<7:0> | 0x7C | Program FIR B filter for extra decimation (Note 1) |
| | OUT_CLKRATE<3:0> | 0x02 | Adjust the output clock rate to the decimation rate |
| Real: $Real_A$ after DDC($f_S/8/DER$) without using Decimation Filter | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | EN_DDC_FS/8 = 1 | 0x81 | NCO($f_S/8/DER$) is enabled. This translates the input signal from dc to $f_S/8$ (Note 3) |
| | EN_DDC2 = 1 | 0x80 | DDC2 is enabled |
| | FIR_A<8:1> = 0x00 | 0x7B | Decimation filter FIR A is disabled |
| | FIR_B<7:0> = 0x00 | 0x7C | Decimation filter FIR B is disabled |
| | OUT_CLKRATE<3:0> = 0001 | 0x02 | Adjust the output clock rate to divided by 2 (Note 2) |
| Decimated Real: $Real_{A_DEC}$ after Decimation Filter and DDC($f_S/8/DER$) | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | EN_DDC_FS/8 = 1 | 0x81 | NCO($f_S/8/DER$) is enabled. This translates the input signal from dc to $f_S/8/DER$ (Note 3) |
| | EN_DDC2 = 1 | 0x80 | DDC2 is enabled |
| | FIR_A<8:1> | 0x7B | Program FIR B filter for extra decimation (Note 4) |
| | FIR_B<7:0> | 0x7C | Program FIR B filter for extra decimation (Note 4) |
| | OUT_CLKRATE<3:0> | 0x02 | Adjust the output clock rate to the total decimation rate including the 2x decimation by the Half-Band Filter A |

Note 1: For I/Q decimation, the maximum decimation rate for the FIR A and FIR B is 128x each since the input is already decimated by 2x in the Half-Band Filter. See [Figure 4-15](#) for details.

2: Divided by 2 is due to the 2x decimation included in the Half-Band Filter A.

3: DER is the decimation rate setting of FIR A and FIR B filters.

4: When this filter is used, the up-conversion frequency is reduced by the extra decimation rates (DER).

MCP37231/21-200 AND MCP37D31/21-200

TABLE 4-13: REGISTER SETTINGS FOR DECIMATION AND DDC OPTIONS FOR DUAL-CHANNEL MODE EXAMPLE

| Decimation Rate (by FIR A and FIR B) (Note 7) | DDC-Mode | Address 0x02 (Note 1) | FIR A Filter | | FIR B Filter | DDC1 | DDC2 | Dual-Channel DSPP Control | Output |
|---|----------|--------------------------|-----------------------|----------------------|----------------------|-------------------------|-------------------------|---------------------------------|---|
| | | | 0x7A<6> (FIR_A<0>) | 0x7B (FIR_A<8:1>) | 0x7C (FIR_B<7:0>) | 0x80<5,1,0> (Note 2) | 0x81<6,3,2> (Note 3) | 0x79<7> (EN_DSPPDUAL) | |
| 0 | Disabled | 0x00 | 0 | 0x00 | 0x00 | 0,0,0 | 0,0,0 | 0 | ADC |
| 8 | Disabled | 0x33 | 0 | 0x07 | 0x07 | 0,0,0 | 0,0,0 | 0 | ADC with decimation (+8) |
| 256 | Disabled | 0x88 | 0 | 0xFF | 0xFF | 0,0,0 | 0,0,0 | 0 | ADC with decimation (+256) |
| 0 | I/Q | 0x00 (Note 4) | 0 | 0x00 | 0x00 | 1,0,1 | 0,0,0 | 1 | I/Q data |
| 0 | $f_S/8$ | 0x11 (Note 5) | 0 | 0x00 | 0x00 | 1,1,1 | 0,0,0 | 1 | Real _A /Real _B without using decimation filter (+2) |
| 8 | $f_S/8$ | 0x44 | 0 | 0x0E | 0x0E (Note 6) | 1,1,1 | 0,0,0 | 1 | Real with decimation filter (+16) |

- Note**
- 1: Output data and clock rate control register.
 - 2: 0x80<5,1,0> = <EN_NCO, EN_DDC_FS/8, EN_DDC1>.
 - 3: 0x81<6,3,2> = <EN_DDC, SEL_DSPP, 8CH_CW>.
 - 4: Each of I/Q has 1/2 of f_S bandwidth. The combined bandwidth is the same as the f_S bandwidth. Therefore the data rate adjustment is not needed.
 - 5: Data rate is reduced by half since the Half-Band Filter A/B includes decimation of 2.
 - 6: 0x0E takes into account the stages 1 and 2 are bypassed. See Figure 4-15 for “dual-channel Input” for DDC.
 - 7: This decimation value is from the decimation filter. When DDC is used, the actual total decimation is 2x larger since 2x is included from the DDC Half-Band Filter. Example: “Dual-Ch., Decimation=8x, DDC- $f_S/8$ ” option actually has 16x decimation with 8x provided by the decimation filter and 2x by the DDC Half-Band Filter.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 4-14: OUTPUT TYPE VS. CONTROL PARAMETERS FOR DUAL-CHANNEL DDC EXAMPLE

| Output Type | Control Parameter | Register | Descriptions |
|--|-------------------------|----------|---|
| Complex: I and Q | EN_DSPPDUAL = 1 | 0x79 | Enable all digital post-processing functions for dual-channel operations |
| | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | HBFILTER_B = 1 | 0x80 | Enable Half-Band Filter B, includes 2x decimation |
| | EN_DDC_FS/8 = 0 | 0x81 | NCO($f_S/8/DER$) is disabled |
| | EN_DDC2 = 0 | 0x80 | DDC2 is disabled |
| | FIR_A<8:1> = 0x00 | 0x7B | FIR A decimation filter is disabled |
| | FIR_B<7:0> = 0x00 | 0x7C | FIR B decimation filter is disabled |
| | OUT_CLKRATE<3:0> | 0x02 | Output clock rate is not affected (no need to change) |
| Real: Real _A for Channel A and Real _B for Channel B after NCO($f_S/8/DER$) without using Decimation Filter | EN_DSPPDUAL = 1 | 0x79 | Enable all digital post-processing functions for dual-channel operations |
| | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | HBFILTER_B = 1 | 0x80 | Enable Half-Band Filter B, includes 2x decimation |
| | EN_DDC_FS/8 = 1 | 0x81 | NCO($f_S/8/DER$) is enabled. This translates the input signal from DC to $f_S/8$ (Note 1) |
| | EN_DDC2 = 1 | 0x80 | DDC2 is enabled |
| | FIR_A<8:1> = 0x00 | 0x7B | Decimation filter FIR A is disabled |
| | FIR_B<7:0> = 0x00 | 0x7C | Decimation filter FIR B is disabled |
| | OUT_CLKRATE<3:0> = 0001 | 0x02 | Adjust the output clock rate to divided by 2 (Note 2) |
| Decimated Real: Real _{A_DEC} for Channel A and Real _{B_DEC} for Channel B after NCO($f_S/8/DER$) and Decimation Filter | EN_DSPPDUAL = 1 | 0x79 | Enable all digital post-processing functions for dual-channel operation |
| | EN_DDC1 = 1 | 0x80 | Enable DDC1 block |
| | EN_NCO = 1 | 0x80 | Enable 32-bit NCO |
| | HBFILTER_A = 1 | 0x80 | Enable Half-Band Filter A, includes 2x decimation |
| | HBFILTER_B = 1 | 0x80 | Enable Half-Band Filter B, includes 2x decimation |
| | EN_DDC_FS/8 = 1 | 0x81 | NCO($f_S/8/DER$) is enabled. This translates the input signal from DC to $f_S/8/DER$ (Note 1) |
| | EN_DDC2 = 1 | 0x80 | DDC2 is enabled |
| | FIR_A<8:1> | 0x7B | Program FIR A filter for extra decimation (Note 3) |
| | FIR_B<7:0> | 0x7C | Program FIR B filter for extra decimation (Note 3) |
| | OUT_CLKRATE<3:0> | 0x02 | Adjust the output clock rate to the total decimation rate including the 2x decimation by the Half-Band Filter A |

Note 1: DER is the decimation rate setting of FIR A and FIR B filters.

Note 2: Divided by 2 is due to the 2x decimation included in the Half-Band Filter A.

Note 3: When this filter is used, the up-conversion frequency is reduced by the extra decimation rates (DER).

MCP37231/21-200 AND MCP37D31/21-200

4.9 Digital Offset and Digital Gain Settings

Offset and gain can be individually adjusted for each input channel. [Figure 4-21](#) shows a simplified block diagram of the digital offset and gain settings. Offset is applied prior to the gain.

Offset and gain adjustments occur prior to DDC, Decimation, or FDR when these features are used.

4.9.1 DIGITAL OFFSET SETTINGS

The offset of an individual channel can be controlled using CH(N)_DIG_OFFSET<7:0> in Addresses 0x9E – 0xA7 ([Registers 5-71 to 5-79](#)) together with the offset weight control register, DIG_OFFSET_WEIGHT<1:0> in 0xA7 ([Register 5-79](#)).

Note that, except for the octal-channel mode, the offset setting registers, 0x9E – 0xA7 ([Registers 5-71 to 5-79](#)), are not sequentially corresponding to the channel order defined by CH_ORDER<23:0>. [Table 4-15](#) shows the details of the offset registers that are corresponding to the actual channels depending on the number of channel used.

4.9.2 DIGITAL GAIN SETTINGS

CH(N)_DIG_GAIN<7:0> in Addresses 0x96 – 0x9D ([Registers 5-63 to 5-70](#)) is used to adjust the digital gain per channel.

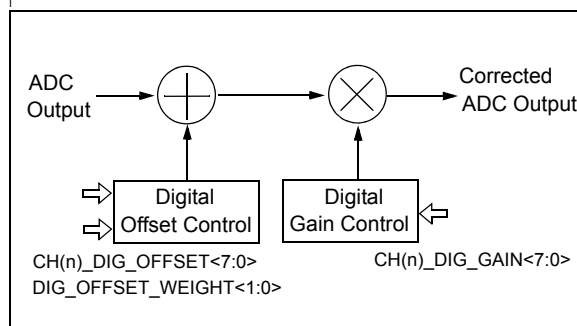


FIGURE 4-21: Simplified Block Diagram for Digital Offset and Gain Settings.

Note 1: Digital Offset Setting: Register mapping (0x9E – 0xA7) to the corresponding channel is not sequential to the channel order defined by CH_ORDER<23:0>, except for the octal-channel mode. See [Table 4-15](#) for details.

2: Gain and NCO Phase Offset: Register mapping to the corresponding channel is sequential to the channel order defined by CH_ORDER<23:0>.

TABLE 4-15: REGISTER ASSIGNMENT FOR OFFSET SETTING

| Number of Channel Used | Register Address for Offset Setting | | | | | | | |
|------------------------|-------------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | 1 st Channel | 2 nd Channel | 3 rd Channel | 4 th Channel | 5 th Channel | 6 th Channel | 7 th Channel | 8 th Channel |
| 1 | 0x9F | — | — | — | — | — | — | — |
| 2 | 0xA0 | 0x9F | — | — | — | — | — | — |
| 3 | 0xA1 | 0x9F | 0xA0 | — | — | — | — | — |
| 4 | 0xA2 | 0x9F | 0xA0 | 0xA1 | — | — | — | — |
| 5 | 0xA3 | 0x9F | 0xA0 | 0xA1 | 0xA2 | — | — | — |
| 6 | 0xA4 | 0x9F | 0xA0 | 0xA1 | 0xA2 | 0xA3 | — | — |
| 7 | 0xA5 | 0x9F | 0xA0 | 0xA1 | 0xA2 | 0xA3 | 0xA4 | — |
| 8 | 0x9E | 0x9F | 0xA0 | 0xA1 | 0xA2 | 0xA3 | 0xA4 | 0xA5 |

MCP37231/21-200 AND MCP37D31/21-200

4.10 Continuous Wave (CW) Beamforming and Ultrasound Doppler-Signal Processing Using CW octal-channel Mode (MCP37D31/21-200 only)

In modern ultrasound medical applications, large numbers of transducers are often used. The signals from these sensors are then coherently combined for higher transducer gain and directivity. The signals from each sensor arrive at the detection device with a different time delay. Also, in multi-channel scanning operations using the MUX, there is a time delay between acquiring input signals (see [Section 4.8.1 “Fractional Delay Recovery for Dual and Octal-Channel modes”](#)). These time-delays may need to be corrected before all input signals are combined for the signal processing.

Digital beamforming is a digital signal-processing technique that requires summing all input signals from different channels after correcting for time delay. The time-delay correction involves the phase alignment of the detected signals with respect to a reference.

Along with the beamforming, many modern medical ultrasound devices support Doppler imaging which processes phase information in addition to the classical magnitude detection (for brightness imaging). The ultrasound Doppler signal processing is used to determine movement in the body as represented by blood flow, which can help to diagnose the functioning of a heart valve or blood vessel, etc. In a traditional ultrasound system, all of these functions are typically accomplished with discrete components. [Figure 4-23](#) shows an example of an ultrasound system implementation using various specialized components.

The MCP37D31/21-200 device has a built-in feature that can perform some of the functions that are done traditionally using extra components. The continuous wave (CW) digital beamforming and Doppler signal processing features are available, but these are offered in the octal-channel operation only.

[Figure 4-22](#) shows a simplified block diagram for the ultrasound CW beamforming with DDC I/Q decimation. Note that the sub-blocks shown after the MUX are commonly used for all input channels.

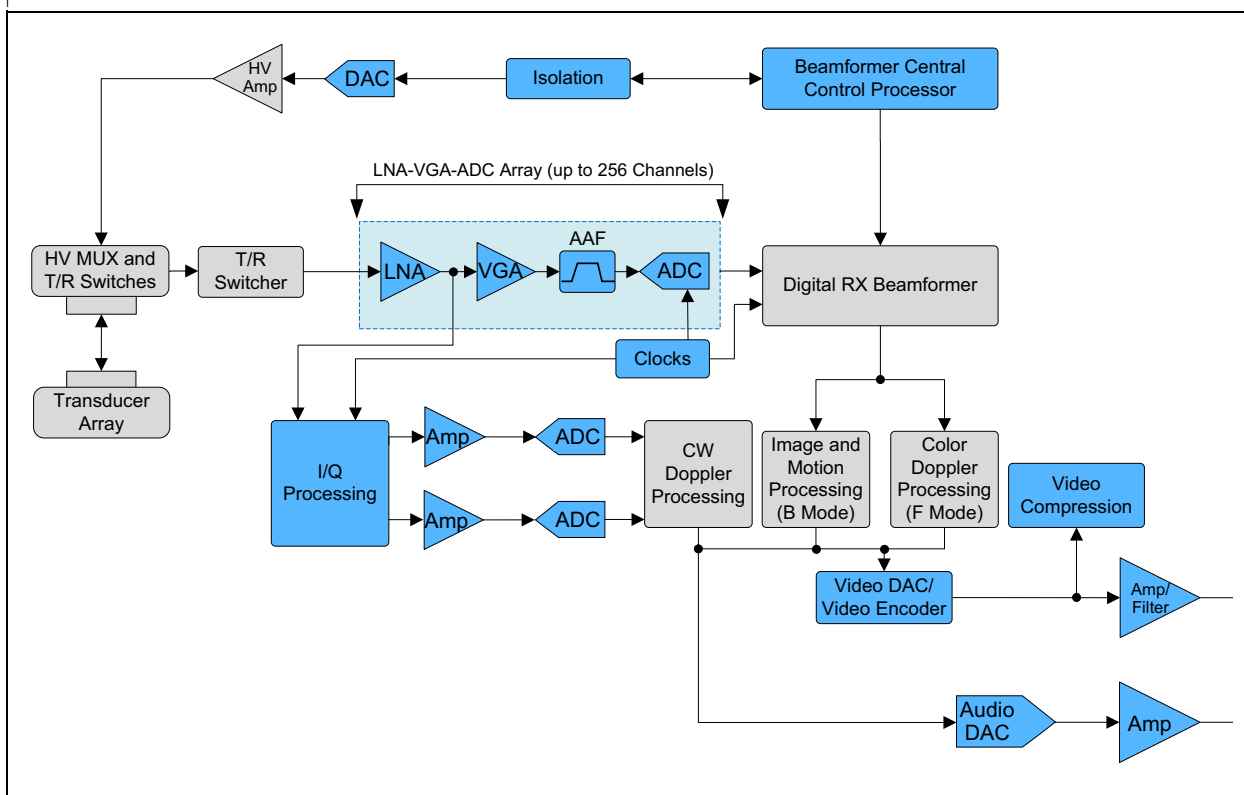


FIGURE 4-22: Example of Ultrasound System Building Block.

MCP37231/21-200 AND MCP37D31/21-200

4.10.1 BEAMFORMING

Beamforming is achieved by scanning all inputs while correcting the phase of each channel with respect to a reference. This can be done using:

- Fractional Delay Recovery (FDR)
- Phase offset settings of each individual channel
- Gain setting per channel

While the CW input channel is multiplexed sequentially, the phase offset can be added to the NCO output (each channel individually). $CH(n)_NCO_PHASE<15:0>$, in Addresses 0x86 to 0x95 ([Registers 5-47](#) to [5-62](#)), corrects the time delay of the incoming signals with respect to the reference.

The phase-compensated input signal is then down-converted by a wide dynamic range I/Q demodulator. The digital beamforming of the inputs is then obtained by summing I and Q data from individual channels. This summed I and Q data are fed to the half-band filter. [Equation 4-8](#) shows the I and Q data of an individual channel with phase correction (phase offset), and the resulting digital beamforming signal.

The processing blocks after the digital beamforming are the same as for the DDC single-channel operation described in [Section 4.8.3.1 “Single-Channel DDC”](#), except only limited decimation rates of the FIR A and FIR B filters are used due to the processing time-requirement for summing of the input signals from all channels.

EQUATION 4-8: BEAMFORMING SIGNALS

$$I_{CH(n)} = ADC \times \cos(2\pi f_{NCO}t + \phi(n))$$

$$Q_{CH(n)} = ADC \times \sin(2\pi f_{NCO}t + \phi(n))$$

$$I = \sum_{n=0}^N I_{CH(n)}$$

$$Q = \sum_{n=0}^N Q_{CH(n)}$$

$$\begin{aligned} \phi(n) &= 360^\circ \times \frac{CH(n)_NCO_PHASE<15:0>}{2^{16}} \\ &= 0.005493164^\circ \times CH(n)_NCO_PHASE<15:0> \end{aligned}$$

Where:

$\phi(n)$ = NCO phase offset of channel n

ADC = the output of the ADC block

The NCO phase offset can be controlled by 0.005493164° per step. See [Section 4.8.3.7 “NCO Phase Offset Control”](#) for details.

4.10.2 ULTRASOUND DOPPLER SIGNAL PROCESSING

Doppler shift measurement requires summing the input signals from multiple transducer channels and mixing them with a phase-controlled local oscillator frequency. The resulting low-frequency output is then centered near DC and can measure a Doppler shift produced by moving objects, such as blood flow and changes in blood pressure in arteries, etc. In traditional Doppler measurement, many discrete analog components are used along with, typically, a high-resolution ADC (~18-bit range).

This device has unique built-in features that are suitable for ultrasound Doppler shift measurements. By utilizing these features, system engineers can reduce many discrete components which are otherwise necessary for an ultrasound Doppler measurement system.

The following built-in digital signal post-processing (DSPP) features in the MCP37D31/21-200 can be effectively used for the ultrasound Doppler signal processing applications:

- **Fractional Delay Recovery (FDR):** Correct the time delay of signal sampling between channels. See details in [Section 4.8.1 “Fractional Delay Recovery for Dual and Octal-Channel modes”](#),
- **Digital Gain and Offset adjustment for each channel:** See details in [Section 4.9 “Digital Offset and Digital Gain Settings”](#)
- **Down-Conversion for each channel** with a unique phase of the same NCO frequency prior to summing the eight channels as shown in [Figure 4-23](#).
- After down-conversion by the DDC, the resulting signal can then be decimated to achieve very high SNR in a narrow bandwidth.

MCP37231/21-200 AND MCP37D31/21-200

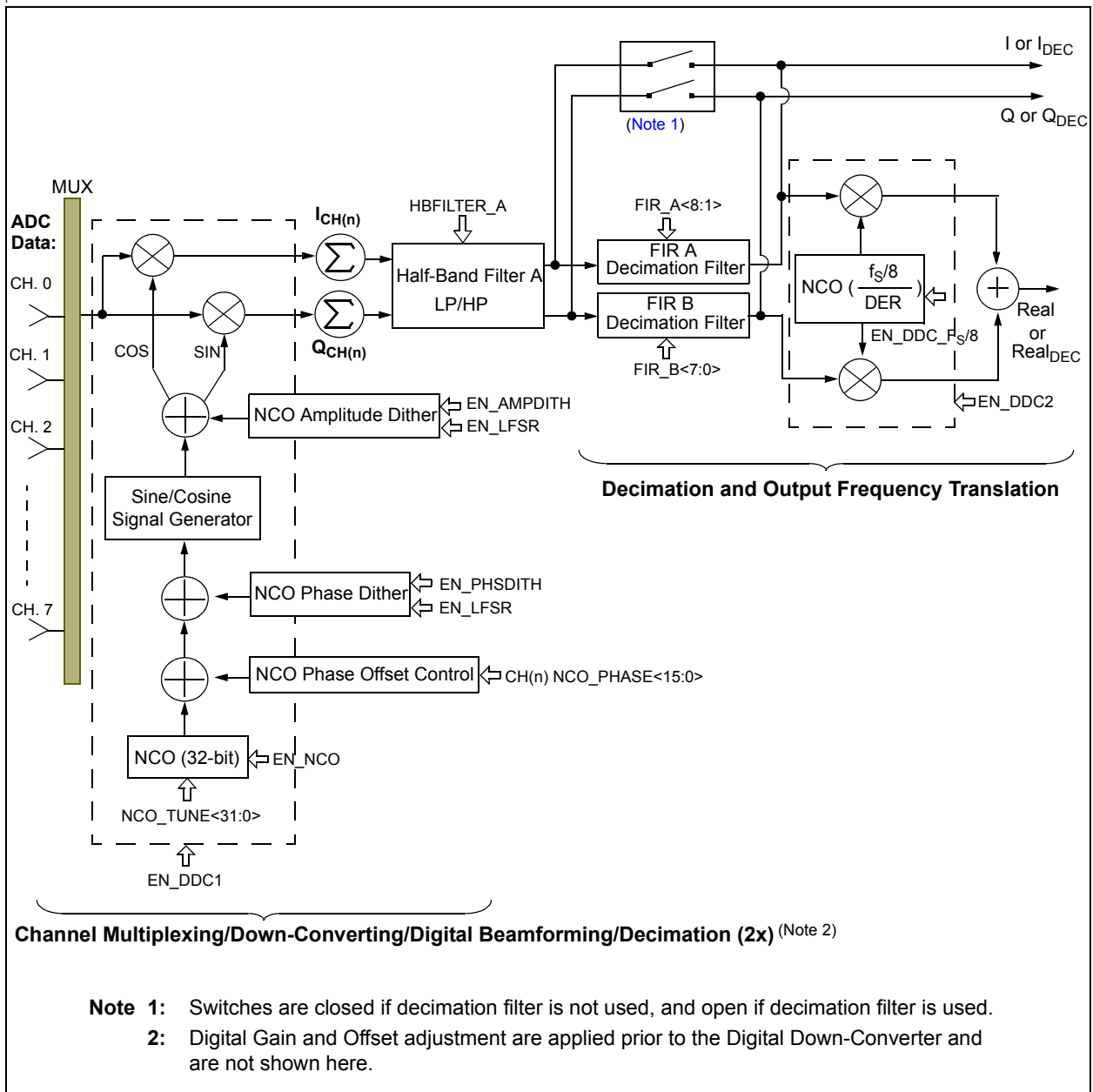


FIGURE 4-23: Simplified Block Diagram of CW Beamforming and I/Q Signal Processing - Available in MCP37D31/21-200 only.

MCP37231/21-200 AND MCP37D31/21-200

4.11 Digital Output

The MCP37231/21-200 and MCP37D31/21-200 can operate in one of three digital output modes:

- Full Rate CMOS
- Double Data Rate (DDR) LVDS
- Serialized DDR LVDS.

The outputs are powered by DV_{DD18} and GND. LVDS mode is recommended for data rates above 80 Msp. The digital output mode is selected by the `OUTPUT_MODE<1:0>` bits in Address 0x62 (Register 5-20). Figures 2-1 to 2-4 show the timing diagrams of the digital output.

4.11.1 FULL RATE CMOS MODE

In full rate CMOS mode, the data outputs (Q15 to Q0, DM1 and DM2), over-range indicator (OVR), word clock (WCK) and the data output clock (DCLK+, DCLK-) have CMOS output levels. The digital output should drive minimal capacitive loads. If the load capacitance is larger than 10 pF, a digital buffer should be used.

4.11.2 DOUBLE DATA RATE LVDS MODE

In double data rate (DDR) LVDS mode, the output is a parallel data stream which changes on each edge of the output clock. Even-bit first and MSB-byte first modes are available:

- Even-bit first option: Available for all resolution options including 18-bit option. See Figure 2-2 for details.
- MSB-byte first option: Available for 16-bit option only. See Figure 2-3 for details.

In multi-channel configuration, the data is output sequentially with the WCK that is synchronized to the first sampled channel.

For 16-bit output, the digital output data is clocked out through eight LVDS output pairs (Q7+/Q7- through Q0+/Q0-). Word clock and over-range (WCK/OVR), and digital output clock (DCLK+, DCLK-) are also LVDS output pairs.

A 100Ω differential termination resistor is required for each LVDS output pin pair. The termination resistor should be located as close as possible to the LVDS receiver. By default the outputs are standard LVDS levels: 3.5 mA output current with a 1.15V output common-mode voltage on 100Ω differential load. See Address 0x63 (Register 5-21) for more details of the LVDS mode control.

Note: LVDS output polarity can be controlled independently for each LVDS pair. See `POL_LVDS<7:0>` setting in Address 0x65 (Register 5-23).

4.11.3 SERIALIZED LVDS MODE

This output mode is only available for the octal-channel operation with 16-bit data output, and uses 8-output lanes: a single LVDS pair for each channel output as shown in Figure 2-4.

Each channel's data is serialized by the data serializer, and the outputs are available through eight LVDS output lanes. Each differential LVDS output pair holds a single input channel's data, and clocks out data with double data rate (DDR), which is synchronized with WCK/OVR bit:

- Q7+/Q7- pair: 1st channel selected
- Q6+/Q6- pair: 2nd channel selected
- .
- .
- Q0+/Q0- pair: last channel selected

Note: **Output Data Rate in LVDS Mode:** In octal-channel mode, the input sample rate per channel is $f_S/8$. Therefore, the output data rate to shift out all 16-bit in DDR is still equivalent to f_S . For example, if $f_S = 200$ Msp, each channel's sample rate is $f_S/8 = 25$ Msp, and output clock rate (DCLK) for 16-bit DDR output is 200 MHz.

4.11.4 PROGRAMMABLE LVDS OUTPUT CURRENT

In LVDS mode, the default output driver current is 3.5 mA. This current can be adjusted by using `LVDS_IMODE<2:0>` bit setting in Address 0x63 (Register 5-21). Available output drive currents are 1.8 mA, 3.5 mA, 5.4 mA, and 7.2 mA.

4.11.5 OPTIONAL LVDS DRIVER INTERNAL TERMINATION

In most cases, using an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by setting the `LVDS_LOAD` bit in Address 0x63 (Register 5-21). The internal termination helps for absorbing any reflections caused by imperfect impedance termination at the receiver.

MCP37231/21-200 AND MCP37D31/21-200

4.11.6 OVER-RANGE BIT (OVR)

The input over-range status bit is asserted (logic high) when the analog input has exceeded the full-scale range of the ADC in either the positive or negative direction. In LVDS DDR Output mode, the OVR bit is multiplexed with the word clock (WCK) output bit, such that OVR is output on the falling edge of the data output clock and WCK on the rising edge.

The OVR bit has the same pipeline latency as the ADC data bits. In multi-channel mode, the OVR is output independently for each input channel and is synchronized to the data. In serialized LVDS mode (for 16-bit octal channel), WCK is asserted when the MSB comes out. OVR will be asserted if any of the channels is over-ranged, but it does not specify which channel is over-ranged. See Address 0x68 ([Register 5-26](#)) for OVR and WCK control options.

If DSPP options are enabled, OVR pipeline latency will be unaffected, however the data will incur additional delay. This has the effect of allowing the OVR indicator to precede the affected data.

4.11.7 WORD CLOCK (WCK)

The word clock output bit indicates the start of a new data set. In single-channel mode, this bit is disabled. In DDR output with multi-channel mode, it is always asserted coincidentally with the data from the first sampled channel, and multiplexed with the OVR bit. See Address 0x68 ([Register 5-26](#)) for OVR and WCK control options.

4.12 Output Data format

The device can output the ADC data in offset binary or two's complement. The data format is selected by the DATA_FORMAT bit in Address 0x62 ([Register 5-20](#)). [Table 4-16](#) shows the relationship between the analog input voltage, the digital data output bits and the over-range bit. By default, the output data format is two's complement.

TABLE 4-16: ADC OUTPUT CODE VS. INPUT VOLTAGE

| Input Range | Offset Binary ⁽¹⁾ | Two's Complement ⁽¹⁾ | Over-Range (OVR) |
|------------------------------------|------------------------------|---------------------------------|------------------|
| $A_{IN} > A_{FS}$ | 1111-1111-1111-1111 | 0111-1111-1111-1111 | 1 |
| $A_{IN} = A_{FS}$ | 1111-1111-1111-1111 | 0111-1111-1111-1111 | 0 |
| $A_{IN} = A_{FS} - 1 \text{ LSB}$ | 1111-1111-1111-1110 | 0111-1111-1111-1110 | 0 |
| $A_{IN} = A_{FS} - 2 \text{ LSB}$ | 1111-1111-1111-1100 | 0111-1111-1111-1100 | 0 |
| | • | | |
| | • | | |
| | • | | |
| $A_{IN} = A_{FS}/2$ | 1100-0000-0000-0000 | 0100-0000-0000-0000 | 0 |
| $A_{IN} = 0$ | 1000-0000-0000-0000 | 0000-0000-0000-0000 | 0 |
| $A_{IN} = -A_{FS}/2$ | 0011-1111-1111-1111 | 1011-1111-1111-1111 | 0 |
| | • | | |
| | • | | |
| | • | | |
| $A_{IN} = -A_{FS} + 2 \text{ LSB}$ | 0000-0000-0000-0010 | 1000-0000-0000-0010 | 0 |
| $A_{IN} = -A_{FS} + 1 \text{ LSB}$ | 0000-0000-0000-0001 | 1000-0000-0000-0001 | 0 |
| $A_{IN} = -A_{FS}$ | 0000-0000-0000-0000 | 1000-0000-0000-0000 | 0 |
| $A_{IN} < -A_{FS}$ | 0000-0000-0000-0000 | 1000-0000-0000-0000 | 1 |

Note 1: MSB is sign bit

MCP37231/21-200 AND MCP37D31/21-200

4.12.1 PHASE SHIFTING OF OUTPUT CLOCK (DCLK)

In full rate CMOS mode, the data output bit transition occurs at the rising edge of DCLK+. In double data rate LVDS mode, the data transition occurs at both the rising and falling edges of DCLK+. For adequate setup and hold time when latching the data into the external host device, the user can adjust the phase of the digital clock output (DCLK+, DCLK-), relative to the data output bits.

This digital output clock (DCLK+, DCLK-) phase delay can be achieved by using the phase delay control registers. [Table 4-17](#) shows the output clock phase control registers. [Figure 4-24](#) shows an example of the output clock phase delay control using the DLL_PHDLY<2:0> in DLL block (PLL and decimation are not used).

TABLE 4-17: OUTPUT CLOCK (DCLK) PHASE CONTROL PARAMETERS

| Control Parameter | Register | Operating Condition |
|---------------------|----------|---|
| DLL_PHDLY<2:0> | 0x52 | External clock is used as timing source without using PLL or decimation. The phase delay is controlled in DLL Block. See Figure 4-11 for details. |
| PLL_PHDLY<3:0> | 0x6D | PLL is used without using decimation. The phase delay is controlled in PLL Block. Figure 4-11 for details. |
| DCLK_PHDLY_DEC<2:0> | 0x64 | The decimation filter is used. See details in Section 4.8.2 "Decimation Filters" . |

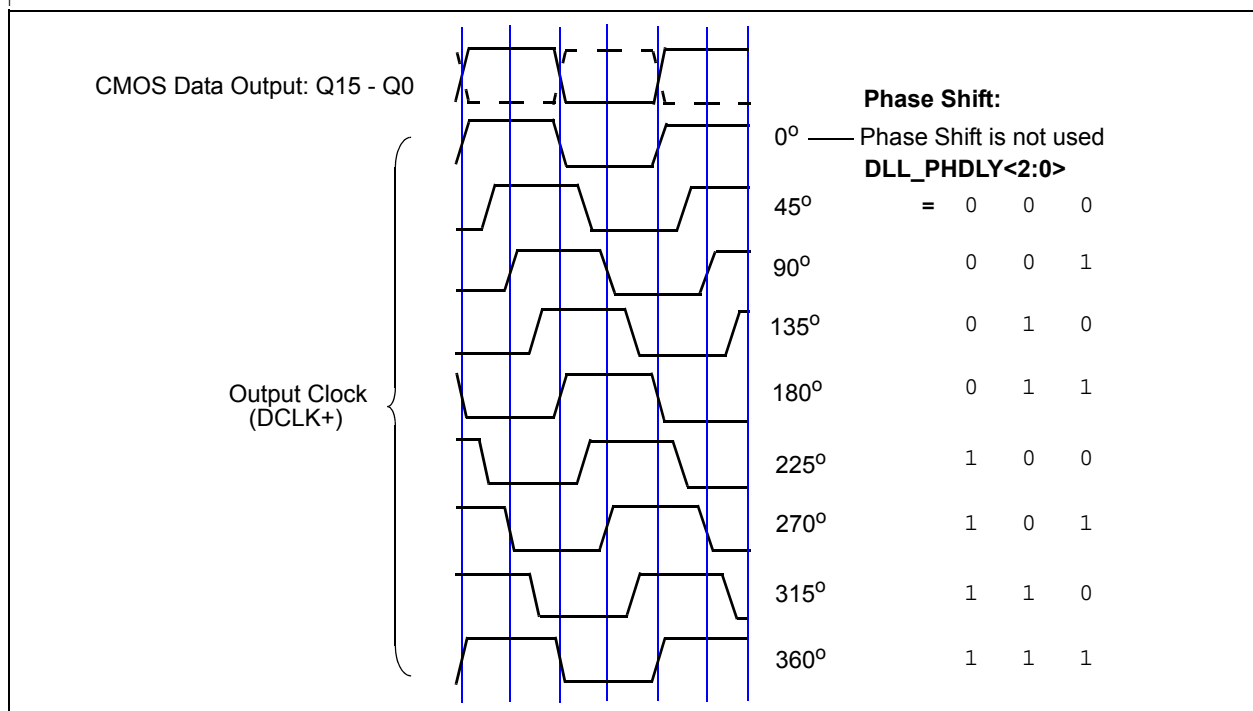


FIGURE 4-24: Phase Shifting of Digital Output Clock (DCLK).

MCP37231/21-200 AND MCP37D31/21-200

4.13 Digital Output Randomizer

Depending on PCB considerations and power supply coupling, SFDR may be improved by de-correlating the ADC input from the ADC digital output data. The device includes an output data randomizer option. When this option is enabled, the digital output is randomized by applying an exclusive-OR logic operation between the LSB (D0) and all other data output bits.

To decode the randomized data, the reverse operation is applied: an exclusive-OR operation is applied between the LSB (D0) and all other bits. The DCLK, OVR, WCK, DM1, DM2 and LSB (D0) outputs are not affected. Figure 4-25 shows the block diagram of the data randomizer and decoder logic. The output randomizer is enabled by setting the EN_OUT_RANDOM bit in Address 0x07 (Register 5-5).

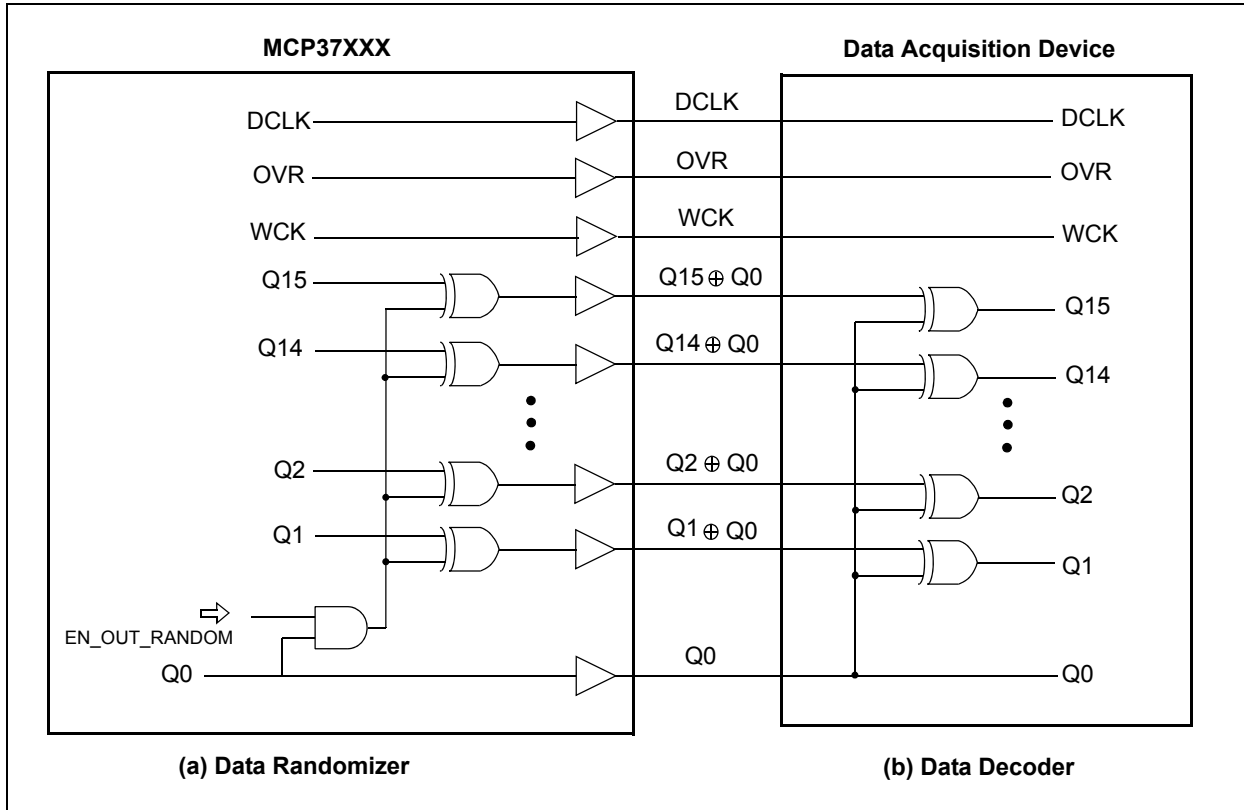


FIGURE 4-25: Logic Diagram for Digital Output Randomizer and Decoder.

4.14 Output Disable

The digital output can be disabled by setting OUTPUT_MODE<1:0> = 00 in Address 0x62 (Register 5-20). All digital outputs are disabled, including OVR, WCK, DCLK, etc.

4.15 Output Test Patterns

To facilitate testing of the I/O interface, the device can produce various pre-defined or user-defined patterns on the digital outputs. See TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20) for the pre-defined, and for the user-defined test patterns. For the user-defined pattern, the Addresses 0x74 – 0x77 (Registers 5-29 to 5-32) can be programmed using the SPI interface. When an output test mode is enabled, the ADC's analog section can still be operational, but does not drive the digital outputs. The outputs are driven only with the selected test pattern.

4.15.1 PSEUDO-RANDOM NUMBER (PN) SEQUENCE OUTPUT

When TEST_PATTERNS<2:0> = 111, the device outputs a pseudo-random number (PN) sequence which is defined by the polynomial of degree 16, as shown in Equation 4-9. Figure 4-26 shows the block diagram of a 16-bit Linear Feedback Shift Register (LFSR) for the PN sequence.

EQUATION 4-9: POLYNOMIAL FOR PN

$$P(x) = 1 + x^4 + x^{13} + x^{15} + x^{16}$$

MCP37231/21-200 AND MCP37D31/21-200

The output PN[15:0] is directly applied to the output pins Qn[15:0]. In addition to the output at the Qn[15:0] pins, the two MSBs, PN[15] and PN[14], are copied to OVR and WCK pins, respectively. The two LSBs, PN[1] and PN[0], are also copied to DM1 and DM2 pins, respectively. In CMOS output mode, the pattern is always applied to all CMOS I/O pins, regardless whether or not they are enabled. In LVDS output mode, the pattern is only applied to the LVDS pairs that are enabled.

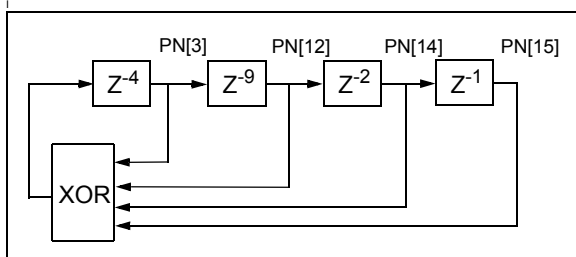


FIGURE 4-26: Block Diagram of 16-bit LFSR for Pseudo-Random Number (PN) Sequence for Output Test Pattern.

4.16 System Calibration

The built-in system calibration algorithm includes:

- Harmonic Distortion Correction (HDC)
- DAC Noise Cancellation (DNC)
- Dynamic Element Matching (DEM)

HDC and DNC correct the nonlinearity in the residue amplifier and DAC, respectively. The system calibration is performed by:

- Power-p calibration, which takes place during the power-on reset sequence (requires 2^{27} clock cycles)
- Background calibration, which takes place during normal operation (per 2^{30} clock cycles).

Background calibration time is invisible to the user, and primarily affects the ADC's ability to track variations in ambient temperature.

The calibration status is monitored by CAL pin or the CAL_STAT bit in Address 0xC0 (Register 5-80). See also Address 0x07 (Register 5-5) and 0x1E (Register 5-6) for time delay control of the auto-calibration. Table 4-18 shows the calibration time for various ADC core sample rates.

TABLE 4-18: CALIBRATION TIME VS. ADC CORE SAMPLE RATE

| f_s (MSPS) | 200 | 150 | 100 | 70 | 50 |
|---------------------------------|------|------|-------|-------|-------|
| Power-Up Calibration Time (s) | 0.67 | 0.9 | 1.34 | 1.92 | 2.68 |
| Background Calibration Time (s) | 5.37 | 7.16 | 10.73 | 15.34 | 21.48 |

4.16.1 RESET COMMAND

Although the background calibration will track changes in temperature or supply voltage, changes in clock frequency or register configuration should be followed by a recalibration of the ADC. This can be accomplished either via the Hard or Soft Reset commands. The recalibration time is the same as the power-up calibration time (2^{27} clock cycles). During the reset, the device has the following state:

- No ADC output
- No change in power-on condition of internal reference
- Most of the internal clocks are not distributed
- Contents of internal user registers:
 - Not affected by Soft Reset
 - Reset to default values by Hardware Reset
- Current consumption of the digital section is negligible, but no change in the analog section.

4.16.1.1 Hardware Reset

A hard reset is triggered by toggling the $\overline{\text{RESET}}$ pin. On the rising edge, the internal user-registers are initialized to their default states and recalibration of the ADC commences. The recalibration time is the same as the power-up calibration time. See Figure 2-8 for the timing details of the hardware $\overline{\text{RESET}}$ pin.

4.16.1.2 Soft Reset

The user can issue a Soft Reset command for a fast recalibration of the ADC, by setting the $\overline{\text{SOFT_RESET}}$ bit to '0' in Address 0x00 (Register 5-1). During Soft Reset, all internal calibration registers are initialized to their initial default states. User registers are unaffected. When exiting the Soft Reset (changing from '0' to '1'), an automatic device calibration takes place.

MCP37231/21-200 AND MCP37D31/21-200

4.17 Power Dissipation and Power Savings

The power dissipation of the ADC core is proportional to the sample rate (f_S). The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load condition on each output pin. The maximum digital load current (I_{LOAD}) can be calculated as:

EQUATION 4-10: CMOS OUTPUT LOAD CURRENT

$$I_{LOAD} = DV_{DD1.8} \times f_{DCLK} \times N \times C_{LOAD}$$

Where:

N = Number of bits

C_{LOAD} = Capacitive load of output pin

The capacitive load presented at the output pins needs to be minimized to minimize digital power consumption. The output load current of the LVDS output is constant, since it is set by LVDS_IMODE<2:0> in Address 0x63 ([Register 5-21](#)).

4.17.1 POWER SAVING MODES

This device has two power-saving modes:

- Shutdown
- Standby

They are set by the SHUTDOWN and STANDBY bits in Address 0x00 ([Register 5-1](#)).

In Shutdown mode, most of the internal circuitry, including the reference and clock, are turned off with the exception of the SPI interface. During Shutdown, the device consumes 25 mA (typical), primarily due to digital leakage. When exiting from Shutdown, issuing a Soft Reset at the same time is highly recommended. This will perform a fast recalibration of the ADC. The contents of the internal registers are not affected by the Soft Reset.

In Standby mode, most of the internal circuitry is disabled except for the reference, clock and SPI interface. If the device has been in standby for an extended period of time, the existing calibration may not be accurate. Therefore, when exiting from Standby mode, executing the device Soft Reset at the same time is highly recommended.

MCP37231/21-200 AND MCP37D31/21-200

5.0 SERIAL PERIPHERAL INTERFACE (SPI)

The user can configure the ADC for specific functions or optimized performance by setting the device's internal registers through the serial peripheral interface (SPI). The SPI communication uses three pins: $\overline{\text{CS}}$, SCLK and SDIO. Table 5-1 summarizes the SPI pin functions. The SCLK is used as serial timing clock and can be used up to 50 MHz. SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent or read from the internal registers. The Chip Select pin ($\overline{\text{CS}}$) enables the SPI communication when active-low. The falling edge of $\overline{\text{CS}}$ followed by a rising edge of SCLK determines the start of the SPI communication. When $\overline{\text{CS}}$ is tied to high, the SPI communication is disabled and SPI pins are placed in high-impedance mode. The internal registers are accessible by their address.

Figures 5-1 and 5-2 show the SPI data communication protocols for this device with MSB-first and LSB-first option, respectively. It consists of:

- 16-bit wide instruction header + Data byte 1 + Data byte 2 + . . . + Data Byte N

Table 5-2 summarizes the bit functions. The $\overline{\text{R/W}}$ bit of the instruction header indicates whether the command is a read ('1') or a write ('0'):

- If the $\overline{\text{R/W}}$ bit is '1', the SDIO pin changes direction from an input (SDI) to an output (SDO) after the 16-bit wide instruction header.

By selecting the $\overline{\text{R/W}}$ bit, the user can write the register or read back the register contents. The W1 and W2 bits in the instruction header indicate the number of data bytes to transmit or receive in the following data frame.

A2 – A0 bits are the SPI device address bits. These bits are used when multiple devices are used in the same SPI bus. A2 is internally hardcoded to '0'. A1 and A0 bits are correspond to the logic level of ADR1 and ADR0 pins, respectively.

Note: In VTLA-124 package, ADR1 is internally bonded to ground (logic '0').

The R9-R0 bits represent the starting address of the configuration register to write or read. The data bytes following the instruction header are the register data. All register data is 8-bit wide. Data can be sent in MSB-first mode (default) or in LSB-first mode, which is determined by <LSB_FIRST> bit setting in Address 0x00 (Register 5-1). In Write mode, the data is clocked in at the rising edge of the SCLK. In the Read mode, the data is clocked out at the falling edge of the SCLK.

TABLE 5-1: SPI PIN FUNCTIONS

| Pin Name | Descriptions |
|------------------------|--|
| $\overline{\text{CS}}$ | Chip Select pin. SPI mode is initiated at the falling edge. It needs to maintain active-low for the entire period of the SPI communication. The device exits the SPI communication at the rising edge. |
| SCLK | Serial clock input pin. <ul style="list-style-type: none"> • Writing to the device: Data is latched at the rising edge of SCLK • Reading from the device: Data is latched at the falling edge of SCLK |
| SDIO | Serial data input/output pin. This pin is initially input pin (SDI) during the first 16-bit instruction header. After the instruction header, it's I/O status can be changed depending on $\overline{\text{R/W}}$ bit: <ul style="list-style-type: none"> • if $\overline{\text{R/W}} = 0$: Data input pin (SDI) for writing • if $\overline{\text{R/W}} = 1$: Data output pin (SDO) for reading |

TABLE 5-2: SPI DATA PROTOCOL BIT FUNCTIONS

| Bit Name | Descriptions |
|-------------------------|---|
| $\overline{\text{R/W}}$ | 1 = Read Mode 0 = Write Mode |
| W1, W0 (Data Length) | 00 = Data for one register (1 byte) 01 = Data for two registers (2 bytes) 10 = Data for three registers (3 bytes) 11 = Continuous reading or writing by clocking SCLK (Note). |
| A2 - A0 | Device SPI Address for multiple devices in SPI bus. A2: Internally hardcoded to '0' A1: Logic level of ADR1 pin A0: Logic level of ADR0 pin |
| R9 - R0 | Address of starting register. |
| D7 - D0 | Register data. MSB or LSB first, depending on LSB_FIRST bit setting in 0x00. |

Note: The register address counter is incremented by one per step. The counter does not automatically reset to 0x00 after reaching the last address (0x15F). The user also needs to be aware the user-registers are not sequentially allocated.

MCP37231/21-200 AND MCP37D31/21-200

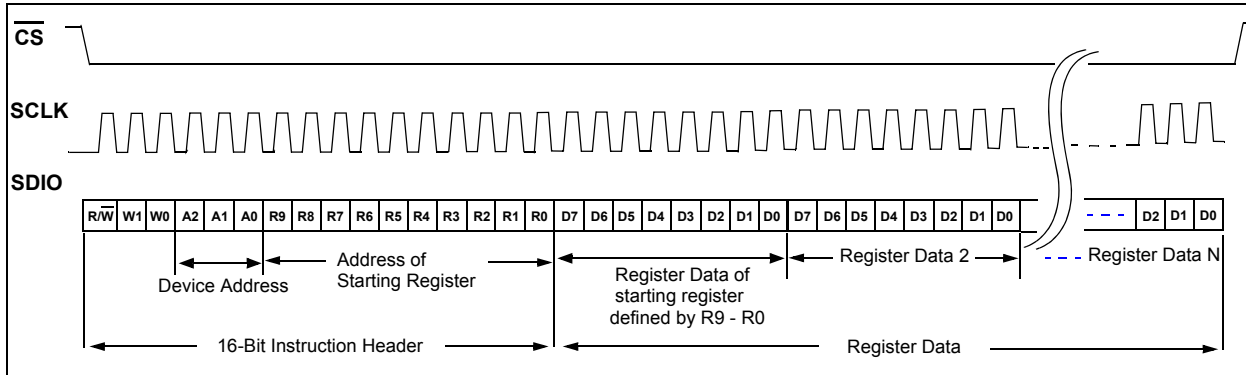


FIGURE 5-1: SPI Serial Data Communication Protocol with MSB-first. See Figures 2-5 and 2-6 for Timing Specifications.

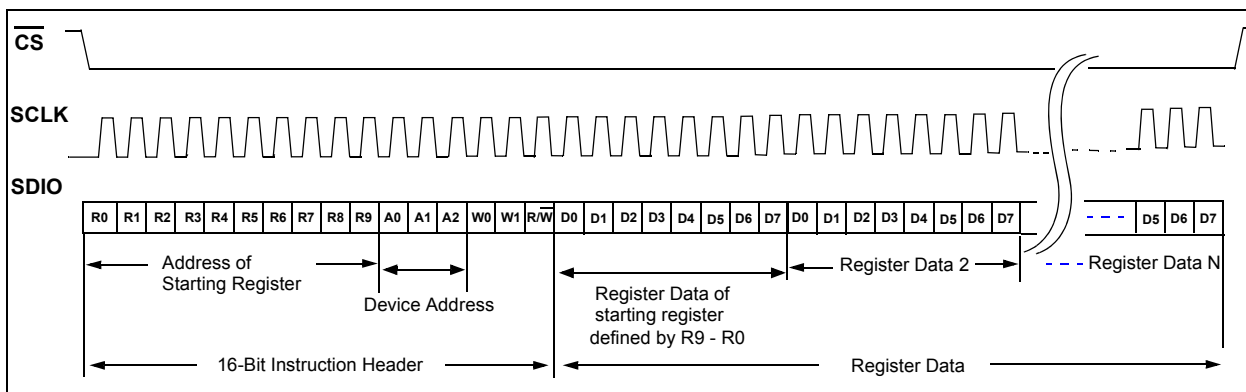


FIGURE 5-2: SPI Serial Data Communication Protocol - with LSB-First. See Figures 2-5 and 2-6 for Timing Specifications.

5.1 Register Initialization

The internal configuration registers are initialized to their default values in two different conditions:

- After 2^{20} clock cycles of delay from the power-on reset (POR).
- By the hardware reset pin ($\overline{\text{RESET}}$).

Figures 2-5 and 2-6 show the timing details.

5.2 Configuration Registers

The internal registers are mapped from address 0x00 to 0x15F. Among them, 83 registers are user-configuration registers. These user registers are not sequentially located, but mixed with factory controlled registers. Some user-configuration registers also have factory-controlled bits. The factory controlled registers and bits cannot be overwritten by the user. All user configuration registers are read/write, except for the last four registers, which are read-only. Each register is made of an 8-bit wide volatile memory, and their default values are loaded during the power-up sequence or by using the hardware $\overline{\text{RESET}}$ pin. All registers are accessible by the SPI command using the register

address. Table 5-3 shows the user-configuration memory map, and Registers 5-1 to 5-83 show the details of the register bit functions.

Note 1: All address and bit locations that are not included in the following table should not be written or modified by the user. Contact Microchip Technology Inc. for more information on the factory programming bit settings.

- 2: Some registers include factory-controlled bits (FCB). Do not overwrite these bits.

TABLE 5-3: REGISTER MAP TABLE

| Addr. | Register Name | Bits | | | | | | | | Default Value | |
|-------|--|--------------------------|---|--|--|---------------------------|----------------------------|---|--------------------------|---------------|------|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | | |
| 0x00 | SPI Bit Ordering and ADC Mode Selection | SHUTDOWN 1 = Shutdown | LSB-First 1 = LSB first 0 = MSB first | SOFT_RESET 0 = Soft Reset | STANDBY 1 = Standby | STANDBY 1 = Standby | SOFT_RESET 0=Soft Reset | LSB-First 1 = LSB first 0 = MSB first | SHUTDOWN 1 = Shutdown | 0x24 | |
| 0x01 | No. of Channel Selection and Independence Control of Output Data and Clock Divider | EN_DATCLK_IND | FCB<3> = 0 | SEL_NCH<2:0> | | | FCB<2:0> = 111 | | | 0x0F | |
| 0x02 | Output Data and Clock Rate | OUT_DATARATE<3:0> | | | | OUT_CLKRATE<3:0> | | | | 0x00 | |
| 0x04 | SPI SDO Timing Control | SDO_TIME | FCB<6:0> = 001111 | | | | | | | 0x9F | |
| 0x07 | Output Randomizer and WCK Polarity | POL_WCK | EN_AUTOCAL_TIMEDLY | FCB<4:0> = 100001 | | | | | EN_OUT_RANDOM | 0x62 | |
| 0x1E | Auto-Calibration Time Delay | AUTOCAL_TIMEDLY<7:0> | | | | | | | | 0x80 | |
| 0x52 | DLL Control | EN_DUTY | DLL_PHDLY<2:0> | | | EN_DCLK | EN_DLL | EN_CLK | RESET_DLL | 0x0A | |
| 0x53 | Clock Source Selection | FCB<6:4> = 001 | | | CLK_SOURCE | FCB<3:0> = 0101 | | | | 0x45 | |
| 0x54 | PLL Reference Divisor | PLL_REFDIV<7:0> | | | | | | | | | |
| 0x55 | PLL Output and Reference Divisor | PLL_OUTDIV<3:0> | | | | U<1:0> | | PLL_REFDIV<9:8> | | | 0x40 |
| 0x56 | PLL Prescaler (LSB) | PLL_PRESCALER (LSB)<7:0> | | | | | | | | | |
| 0x57 | PLL Prescaler (MSB) | FCB<3:0> = 0100 | | | | PLL_PRESCALER (MSB)<11:8> | | | | | 0x40 |
| 0x58 | PLL Charge-pump | FCB<2:0> = 001 | | | PLL_BIAS | PLL_CHAGPUMP<3:0> | | | | 0x22 | |
| 0x59 | PLL Enable Control 1 | U | FCB<4:3> = 1000 | | EN_PLL_REVDIF | FCB<2:1> | | EN_PLL | FCB<0> = 1 | 0x41 | |
| 0x5A | PLL Loop Filter Resistor | U | FCB<1:0> = 01 | | PLL_RES<4:0> | | | | | 0x2F | |
| 0x5B | PLL Loop Filter Cap3 | U | FCB<1:0> = 01 | | PLL_CAP3<4:0> | | | | | 0x27 | |
| 0x5C | PLL Loop Filter Cap1 | U | FCB<1:0> = 01 | | PLL_CAP1<4:0> | | | | | 0x27 | |
| 0x5D | PLL Loop Filter Cap2 | U | FCB<1:0> = 01 | | PLL_CAP2<4:0> | | | | | 0x27 | |
| 0x5F | PLL Enable Control 2 | FCB<7:4> | | | | EN_PLL_OUT | EN_PLL_BIAS | FCB<1:0> | | | 0xF1 |
| 0x62 | Output Data Format and Output Test Patterns | U | LVDS_8CH 1 = Serialized 0 = Interleaved | DATA_FORMAT 1 = Offset binary 0 = two's complement | OUTPUT_MODE<1:0> 11 = LVDS,MSB byte first 10 = LVDS, even bit first 01 = CMOS 00 = Output disabled | | | TEST_PATTERNS<2:0> | | 0x10 | |
| 0x63 | ADC Output Bits (Resolution) and LVDS Output Load | OUTPUT_BIT<3:0> | | | | LVDS_LOAD | LVDS_IMODE<1:0> | | | | 0x01 |

Legend: U = Unimplemented bit, read as '0' FCB = Factory-Controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Not used for this device. Do not change the factory default setting.
2: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

| Addr. | Register Name | Bits | | | | | | | Default Value | |
|-------|--|------------------|--------------------------|-----------|----------------|-----------------------------|----------------------------|----------------------------|----------------------------|------|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | | b0 |
| 0x64 | Output Clock Phase Control when Decimation Filter is used | EN_PHDLY_DEC | DCLK_PHDLY_DEC<2:0> | | | FCB<3:0> = 0011 | | | | 0x03 |
| 0x65 | LVDS Output Polarity | POL_LVDS<7:0> | | | | | | | 0x00 | |
| 0x66 | Digital Offset Correction - Lower Byte | DIG_OFFSET<7:0> | | | | | | | 0x00 | |
| 0x67 | Digital Offset Correction - Upper Byte | DIG_OFFSET<15:8> | | | | | | | 0x00 | |
| 0x68 | WCK/OVR and DM1/DM2 | FCB<3:0> = 0010 | | | | POL_WCK_OVR 1 = Inverted | EN_WCK_OVR 1 = Enabled | DM1DM2 1 = Added | POL_DM1DM2 1 = Inverted | 0x24 |
| 0x6B | PLL Calibration | FCB<4:0>=0001 | | | | PLL_CALTRIG | FCB<1:0>=00 | | | 0x08 |
| 0x6D | PLL Output and Output Clock Phase | U<1:0> | EN_PLL_CLK | PLL_PHASE | PLL_PHDLY<3:0> | | | | 0x00 | |
| 0x74 | User-Defined Output Pattern A - Lower Byte | PATTERN A<7:0> | | | | | | | 0x00 | |
| 0x75 | User-Defined Output Pattern A - Upper Byte | PATTERN A<15:8> | | | | | | | 0x00 | |
| 0x76 | User-Defined Output Pattern B - Lower Byte | PATTERN B<7:0> | | | | | | | 0x00 | |
| 0x77 | User-Defined Output Pattern B - Upper Byte | PATTERN B<15:8> | | | | | | | 0x00 | |
| 0x78 | Noise Shaping Requantizer Channel A Filter ⁽¹⁾ | NSR_RESET | NSRA<6:0> | | | | | | | 0x00 |
| 0x79 | Dual-Channel DSPP and Noise Shaping Requantizer Channel B Filter | EN_DSPPDUAL | NSRB<6:0> ⁽¹⁾ | | | | | | | 0x00 |
| 0x7A | FIRA0 Filter, FDR, and NSR Control | U | FIR_A<0> | EN_FDR | FCB<0> = 0 | EN_NS RB_11 ⁽¹⁾ | EN_NS RB_12 ⁽¹⁾ | EN_NS RA_11 ⁽¹⁾ | EN_NS RA_12 ⁽¹⁾ | 0x00 |
| 0x7B | FIR A Filter (for Single, Dual) | FIR_A<8:1> | | | | | | | 0x00 | |
| 0x7C | FIR B Filter for Channel B | FIR_B<7:0> | | | | | | | 0x00 | |
| 0x7D | Auto-Scan Channel Order - Lower Byte | CH_ORDER<7:0> | | | | | | | 0x78 | |
| 0x7E | Auto-Scan Channel Order - Middle Byte | CH_ORDER<15:8> | | | | | | | 0xAC | |
| 0x7F | Auto-Scan Channel Order - Upper Byte | CH_ORDER<23:16> | | | | | | | 0x8E | |

Legend: U = Unimplemented bit, read as '0' FCB = Factory-Controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Not used for this device. Do not change the factory default setting.

Note 2: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

| Addr. | Register Name | Bits | | | | | | | | Default Value |
|-------|--|---------------------|------------|--------------|------------|------------|---------|---------------|---------|---------------|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0x80 | Digital Down-Converter Control 1 | HBFILTER_B | HBFILTER_A | EN_NCO | EN_AMPDITH | EN_PHSDITH | EN_LFSR | EN_DDC_FS/8 | EN_DDC1 | 0x00 |
| 0x81 | Digital Down-Converter Control 2 | FDR_BAND | EN_DDC2 | GAIN_HBF_DDC | SEL_FDR | SEL_DSPP | 8CH_CW | GAIN_8CH<1:0> | | 0x00 |
| 0x82 | Numerically Controlled Oscillator (NCO) Tuning - Lower Byte | NCO_TUNE<7:0> | | | | | | | | 0x00 |
| 0x83 | Numerically Controlled Oscillator (NCO) Tuning - Middle Lower Byte | NCO_TUNE<15:8> | | | | | | | | 0x00 |
| 0x84 | Numerically Controlled Oscillator (NCO) Tuning - Middle Upper Byte | NCO_TUNE<23:16> | | | | | | | | 0x00 |
| 0x85 | Numerically Controlled Oscillator (NCO) Tuning - Upper Byte | NCO_TUNE<31:24> | | | | | | | | 0x00 |
| 0x86 | CH0 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH0_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x87 | CH0 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH0_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x88 | CH1 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH1_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x89 | CH1 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH1_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x8A | CH2 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH2_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x8B | CH2 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH2_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x8C | CH3 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH3_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x8D | CH3 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH3_NCO_PHASE<15:8> | | | | | | | | 0x00 |

Legend: U = Unimplemented bit, read as '0' FCB = Factory-Controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Not used for this device. Do not change the factory default setting.

Note 2: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

| Addr. | Register Name | Bits | | | | | | | | Default Value |
|-------|---|---------------------|----|----|----|----|----|----|----|---------------|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| 0x8E | CH4 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH4_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x8F | CH4 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH4_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x90 | CH5 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH5_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x91 | CH5 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH5_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x92 | CH6 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH6_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x93 | CH6 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH6_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x94 | CH7 NCO Phase Offset in CW or DDC Mode - Lower Byte | CH7_NCO_PHASE<7:0> | | | | | | | | 0x00 |
| 0x95 | CH7 NCO Phase Offset in CW or DDC Mode - Upper Byte | CH7_NCO_PHASE<15:8> | | | | | | | | 0x00 |
| 0x96 | CH0 Digital Gain | CH0_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x97 | CH1 Digital Gain | CH1_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x98 | CH2 Digital Gain | CH2_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x99 | CH3 Digital Gain | CH3_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x9A | CH4 Digital Gain | CH4_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x9B | CH5 Digital Gain | CH5_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x9C | CH6 Digital Gain | CH6_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x9D | CH7 Digital Gain | CH7_DIG_GAIN<7:0> | | | | | | | | 0x3C |
| 0x9E | CH0 Digital Offset | CH0_DIG_OFFSET<7:0> | | | | | | | | 0x00 |
| 0x9F | CH1 Digital Offset | CH1_DIG_OFFSET<7:0> | | | | | | | | 0x00 |
| 0xA0 | CH2 Digital Offset | CH2_DIG_OFFSET<7:0> | | | | | | | | 0x00 |
| 0xA1 | CH3 Digital Offset | CH3_DIG_OFFSET<7:0> | | | | | | | | 0x00 |
| 0xA2 | CH4 Digital Offset | CH4_DIG_OFFSET<7:0> | | | | | | | | 0x00 |
| 0xA3 | CH5 Digital Offset | CH5_DIG_OFFSET<7:0> | | | | | | | | 0x00 |

Legend: U = Unimplemented bit, read as '0' FCB = Factory-Controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Not used for this device. Do not change the factory default setting.

Note 2: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

| Addr. | Register Name | Bits | | | | | | | Default Value | |
|-------|---|---------------------|---------------------|--------------|------------------------|----|----------------|---------------|---------------|----|
| | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | | b0 |
| 0xA4 | CH6 Digital Offset | CH6_DIG_OFFSET<7:0> | | | | | | | 0x00 | |
| 0xA5 | CH7 Digital Offset | CH7_DIG_OFFSET<7:0> | | | | | | | 0x00 | |
| 0xA7 | Digital Offset Weight Control | FCB<5:3> = 010 | | | DIG_OFFSET_WEIGHT<1:0> | | FCB<2:0> = 111 | | 0x47 | |
| 0xC0 | Calibration Status Indication (Read only) | CAL_STAT | FCB<6:0> = xxx-xxxx | | | | | | - | |
| 0xD1 | PLL Calibration and Status Indication (Read only) | FCB<4:3> = xx | | PLL_CAL_STAT | FCB<2:1> = xx | | PLL_VCOL_STAT | PLL_VCOH_STAT | FCB<0> = x | - |
| 0x15C | CHIP ID - Lower Byte ⁽²⁾ (Read only) | CHIP_ID<7:0> | | | | | | | - | |
| 0x15D | CHIP ID - Upper Byte ⁽²⁾ (Read only) | CHIP_ID<15:8> | | | | | | | - | |

Legend: U = Unimplemented bit, read as '0' FCB = Factory-Controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Not used for this device. Do not change the factory default setting.

Note 2: Read-only register. Preprogrammed at the factory for internal use.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-1: ADDRESS 0X00 – SPI BIT ORDERING AND ADC MODE SELECTION (Note 1)

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
|----------|-----------|------------|---------|---------|------------|-----------|----------|
| SHUTDOWN | LSB_FIRST | SOFT_RESET | STANDBY | STANDBY | SOFT_RESET | LSB_FIRST | SHUTDOWN |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 7 **SHUTDOWN:** Shutdown mode setting for power-saving (Note 2)
 1 = ADC in shutdown mode
 0 = Not in shutdown mode (**Default**)
- bit 6 **LSB_FIRST:** Select SPI communication bit order
 1 = Start SPI communication with LSB first
 0 = Start SPI communication with MSB first (**Default**)
- bit 5 **SOFT_RESET:** Soft Reset control bit (Note 4)
 1 = Not in Soft Reset mode (**Default**)
 0 = ADC in Soft Reset
- bit 4 **STANDBY:** Send the device into a power-saving standby mode (Note 3)
 1 = ADC in Standby mode
 0 = Not in Standby mode (**Default**)
- bit 3 **STANDBY:** Send the device into a power-saving standby mode (Note 3)
 1 = ADC in Standby mode
 0 = Not in Standby mode (**Default**)
- bit 2 **SOFT_RESET:** Soft Reset control bit (Note 4)
 1 = Not in Soft Reset mode (**Default**)
 0 = ADC in Soft Reset
- bit 1 **LSB_FIRST:** Select SPI communication bit order
 1 = Start SPI communication with LSB first
 0 = Start SPI communication with MSB first (**Default**)
- bit 0 **SHUTDOWN:** Shutdown mode setting for power-saving (Note 2)
 1 = ADC in Shutdown mode
 0 = Not in Shutdown mode (**Default**)

- Note 1:** Upper and lower nibble are mirrored, which makes the MSB- or LSB-first mode interchangeable. The lower nibble (bit <3:0>) has a higher priority when the mirrored bits have different values.
- 2:** During Shutdown mode, most of the internal circuits including the reference and clock are turned-off except for the SPI interface. When exiting from shutdown (changing from '1' to '0'), executing the device Soft Reset simultaneously is highly recommended for a fast recalibration of the ADC. The internal user registers are not affected.
 - 3:** During Standby mode, most of the internal circuits are turned off except for the reference, clock and SPI interface. When exiting from Standby mode (changing from '1' to '0') after an extended amount of time, executing Soft Reset simultaneously is highly recommended. The internal user registers are not affected.
 - 4:** This bit forces the device into the Soft Reset mode, which initializes the internal calibration registers to their initial default states. The user-registers are not affected. When exiting the Soft Reset mode (changing from '0' to '1'), the device performs an automatic device calibration. During the Soft Reset, the device has the following states:
 - no ADC output
 - no change in power-on condition of internal reference
 - most of the internal clocks are not distributed.

The power consumption of the digital section is negligible, but no change in the analog section.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-2: ADDRESS 0X01 – NUMBER OF CHANNELS, INDEPENDENCY CONTROL OF OUTPUT DATA AND CLOCK DIVIDER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---------------|-------|--------------|-------|-------|----------|-------|-------|
| EN_DATCLK_IND | FCB | SEL_NCH<2:0> | | | FCB<2:0> | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 7 **EN_DATCLK_IND:** Enable data and clock divider independently ([Note 1](#))

1 = Enable
0 = Disable (**Default**)

bit 6 **FCB:** Factory-Controlled bits. This is not for the user. Do not change the default settings.

bit 5-3 **SEL_NCH<2:0>:** Select the total number of input channels to be used ([Note 2](#))

111 = 7 inputs
110 = 6 inputs
101 = 5 inputs
100 = 4 inputs
011 = 3 inputs
010 = 2 inputs
001 = 1 input (**Default**)
000 = 8 inputs

bit 2-0 **FCB<2:0>:** Factory-Controlled bits. This is not for the user. Do not change the default settings.

Note 1: EN_DATCLK_IND = 1 enables OUT_CLKRATE<3:0> settings in Address 0x02 ([Register 5-3](#)).

- 2:** The total number of input channel varies with the device part number (P/N):
- Single/Dual/Quad-Channel devices: SEL_NCH<2:0> bits are pre-programmed at the factory.
 - Octal-Channel devices: SEL_NCH<2:0> bits are programmed by the user. See Addresses 0x7D – 0x7F ([Registers 5-38 to 5-40](#)) for selecting the input channel order.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-3: ADDRESS 0X02 – OUTPUT DATA AND CLOCK RATE CONTROL (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|------------------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| OUT_DATARATE<3:0> | | | | OUT_CLKRATE<3:0> | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **OUT_DATARATE<3:0>**: Output data rate control bits (Note 2)

- 1111 = Output data is all 0's
- 1110 = Output data is all 0's
- 1101 = Output data is all 0's
- 1100 = Internal test only
- 1011 = Internal test only
- 1010 = Internal test only
- 1001 = Full speed divided by 512
- 1000 = Full speed divided by 256
- 0111 = Full speed divided by 128
- 0110 = Full speed divided by 64
- 0101 = Full speed divided by 32
- 0100 = Full speed divided by 16
- 0011 = Full speed divided by 8
- 0010 = Full speed divided by 4
- 0001 = Full speed divided by 2
- 0000 = Full speed rate (Default)

bit 3-0 **OUT_CLKRATE<3:0>**: Output clock rate control bits (Note 3, Note 4)

- 1111 = Full speed rate
- 1110 = No clock output
- 1101 = No clock output
- 1100 = No clock output
- 1011 = No clock output
- 1010 = No clock output
- 1001 = Full speed divided by 512
- 1000 = Full speed divided by 256
- 0111 = Full speed divided by 128
- 0110 = Full speed divided by 64
- 0101 = Full speed divided by 32
- 0100 = Full speed divided by 16
- 0011 = Full speed divided by 8
- 0010 = Full speed divided by 4
- 0001 = Full speed divided by 2
- 0000 = No clock output (Default)

- Note 1:** This register should be used when the decimation filter selection option (see Addresses 0x7B and 0x7C - [Registers 5-36](#) and [5-37](#)) or digital down conversion (DDC) option (see Address 0x80 - [Register 5-41](#)) is used in single or dual channel mode.
- 2:** 1100 - 1010: Do not reprogram. These settings are used for the internal test only. If these bits are reprogrammed with different settings, the outputs will be in undefined state.
- 3:** Bits <3:0> become active if EN_DATCLK_IND = 1 in Address 0x01 ([Register 5-2](#)). This setting is only used with DDC mode. See Addresses 0x80 and 0x81 ([Registers 5-41](#) and [5-42](#)) for DDC settings.
- 4:** When no clock output is selected (Bits 1110 - 1010): clock output is not available at the DCLK+/DCLK- pins.

REGISTER 5-4: ADDRESS 0X04 – SPI SDO OUTPUT TIMING CONTROL

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-4: ADDRESS 0X04 – SPI SDO OUTPUT TIMING CONTROL (CONTINUED)

| | |
|----------|----------|
| SDO_TIME | FCB<6:0> |
| bit 7 | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **SDO_TIME**: SPI SDO output timing control bit
 1 = SDO output at the falling edge of clock (**Default**)
 0 = SDO output at the rising edge of clock

bit 6-0 **FCB<6:0>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.

REGISTER 5-5: ADDRESS 0X07 – OUTPUT RANDOMIZER AND WCK POLARITY CONTROL

| | | | | | | | |
|---------|------------------------|----------|-------|-------|-------|---------------|-------|
| R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| POL_WCK | EN_AUTOCAL_ TIMEDLY | FCB<4:0> | | | | EN_OUT_RANDOM | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **POL_WCK**: WCK polarity control bit ([Note 1](#))
 1 = Inverted
 0 = Not inverted (**Default**)

bit 6 **EN_AUTOCAL_TIMEDLY**: Auto-calibration starter time delay counter control bit ([Note 2](#))
 1 = Enabled (**Default**)
 0 = Disabled

bit 5-1 **FCB<4:0>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.

bit 0 **EN_OUT_RANDOM**: Output randomizer control bit
 1 = Enabled: ADC data output is randomized
 0 = Disabled (**Default**)

- Note 1:** See Address 0x68 ([Register 5-26](#)) for WCK/OVR pair control.
2: This bit enables the AUTOCAL_TIMEDLY<7:0> settings. See Address 0x1E ([Register 5-6](#)).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-6: ADDRESS 0X1E – AUTOCAL TIME DELAY CONTROL (Note 1)

| | | | | | | | |
|----------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| AUTOCAL_TIMEDLY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **AUTOCAL_TIMEDLY<7:0>**: Auto-calibration start time delay control bits

1111-1111 = Maximum value

•
•
•

1000-0000 = **(Default)**

•
•
•

0000-0000 = Minimum value

Note 1: EN_AUTOCAL_TIMEDLY in Address 0x07 (Register 5-5) enables this register setting. This register controls the time delay before the auto-calibration starts. The value increases linearly with the bit settings, from minimum to maximum values.

REGISTER 5-7: ADDRESS 0X52 – DLL CONTROL

| | | | | | | | |
|---------|----------------|-------|-------|---------|--------|--------|-----------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 |
| EN_DUTY | DLL_PHDLY<2:0> | | | EN_DCLK | EN_DLL | EN_CLK | RESET_DLL |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **EN_DUTY**: Enable DLL circuit for duty cycle correction (DCC) of input clock (Note 1)

1 = Correction is ON
 0 = Correction is OFF **(Default)**

bit 6-4 **DLL_PHDLY<2:0>**: Select the phase delay of the clock output (Note 2)

111 = 360°
 110 = 315°
 101 = 270°
 100 = 225°
 011 = 180°
 010 = 135°
 001 = 90°
 000 = 45° **(Default)**

Note 1: Enable the DLL circuitry for the duty cycle correction. Analog clock output: Rising edge is unaffected and only falling edge is modified. The duty cycle correction will affect the SNR performance significantly.

2: Phase of output data:

- In CMOS output, the data transition occurs at the rising edge of the DCLK+.
- In DDR LVDS output, the data transition occurs at both rising and falling edges of the DCLK+.

3: DLL must be reset if clock is removed or clock frequency is changed significantly. DLL resets automatically during power-up process. The DLL reset control procedure: Set this bit to '0' (reset) and then to '1'.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-7: ADDRESS 0X52 – DLL CONTROL (CONTINUED)

- bit 3 **EN_DCLK:** Enable digital clock to the circuit
 1 = Enabled (**Default**)
 0 = Disabled: Digital clock is turned off, therefore ADC output is not available.
- bit 2 **EN_DLL:** Enable DLL circuitry to provide a selectable phase clock to digital output clock.
 1 = Enabled
 0 = Disabled. Phase selection of digital output is not available (**Default**)
- bit 1 **EN_CLK:** Enable internal clock circuitry
 1 = Enabled (**Default**).
 0 = Disabled. No clock is available to the internal circuits, ADC output is not available.
- bit 0 **RESET_DLL:** DLL circuit reset control (**Note 3**)
 1 = DLL is active
 0 = DLL circuit is held in reset (**Default**)

Note 1: Enable the DLL circuitry for the duty cycle correction. Analog clock output: Rising edge is unaffected and only falling edge is modified. The duty cycle correction will affect the SNR performance significantly.

2: Phase of output data:

- In CMOS output, the data transition occurs at the rising edge of the DCLK+.
- In DDR LVDS output, the data transition occurs at both rising and falling edges of the DCLK+.

3: DLL must be reset if clock is removed or clock frequency is changed significantly. DLL resets automatically during power-up process. The DLL reset control procedure: Set this bit to '0' (reset) and then to '1'.

REGISTER 5-8: ADDRESS 0X53 – CLOCK SOURCE SELECTION

| | | | | | | | |
|----------|-------|-------|------------|----------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| FCB<6:4> | | | CLK_SOURCE | FCB<3:0> | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 7-5 **FCB<6:4>:** Factory-Controlled bits. This is not for the user. Do not change the default settings.
- bit 4 **CLK_SOURCE:** Select internal timing source
 1 = PLL output is selected as timing source
 0 = External clock input is selected as timing source (PLL is not used) (**Default**)
- bit 3-0 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not change the default settings.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-9: ADDRESS 0X54 – PLL REFERENCE DIVISOR

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PLL_REFDIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **PLL_REFDIV<7:0>**: PLL Reference clock divisor control bits (**Note 1**)

1111-1111 = PLL reference divided by 255 (if PLL_REFDIV<9:8> = 00)

1111-1110 = PLL reference divided by 254 (if PLL_REFDIV<9:8> = 00)

•

•

•

0000-0011 = PLL reference divided by 3 (if PLL_REFDIV<9:8> = 00)

0000-0010 = **Do not use (No effect)**

0000-0001 = PLL reference divided by 1 (if PLL_REFDIV<9:8> = 00)

0000-0000 = PLL reference not divided (if PLL_REFDIV<9:8> = 00) (**Default**)

Note 1: PLL_REFDIV is a 10-bit wide setting. See Address 0x55 ([Register 5-10](#)) for the upper two bits and [Table 4-3](#) for PLL_REFDIV<9:0> bit settings. This setting controls the clock division ratio of the PLL reference clock (external clock input at the clock input pin) before the PLL phase-frequency detector circuitry. Note that the divider value of 2 is not supported. EN_PLL_REFDIV in Address 0x59 ([Register 5-14](#)) must be set.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-10: ADDRESS 0X55 – PLL OUTPUT AND REFERENCE DIVISOR

| | | | | | | | |
|-----------------|-------|-------|-------|---------------|-------|-----------------|-------|
| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| PLL_OUTDIV<3:0> | | | | Unimplemented | | PLL_REFDIV<9:8> | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **PLL_OUTDIV<3:0>**: PLL output divisor control bits ([Note 1](#))

1111 = PLL output divided by 15

1110 = PLL output divided by 14

•

•

•

0100 = PLL output divided by 4 (**Default**)

0011 = PLL output divided by 3

0010 = PLL output divided by 2

0001 = PLL output divided by 1

0000 = PLL output not divided

bit 3-2 **Unimplemented**: Not used.

bit 1-0 **PLL_REFDIV<9:8>**: Upper two MSB bits of PLL_REFDIV<9:0> ([Note 2](#))

00 = see [Table 5-4](#). (**Default**)

Note 1: PLL_OUTDIV<3:0> controls the PLL output clock divider: VCO output is divided by the PLL_OUTDIV<3:0> setting.

2: See Address 0x54 ([Register 5-9](#)) and [Table 5-4](#) for PLL_REFDIV<9:0> bit settings. EN_PLL_REFDIV in Address 0x59 ([Register 5-14](#)) must be set.

TABLE 5-4: Example – PLL Reference Divisor Bit Settings Vs. PLL Reference Input Frequency

| PLL_REFDIV<9:0> | PLL Reference Frequency |
|-----------------|-------------------------------------|
| 11-1111-1111 | Reference frequency divided by 1023 |
| 11-1111-1110 | Reference frequency divided by 1022 |
| --- | --- |
| 00-0000-0011 | Reference frequency divided by 3 |
| 00-0000-0010 | Do not use (Not supported) |
| 00-0000-0001 | Reference frequency divided by 1 |
| 00-0000-0000 | Reference frequency divided by 1 |

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-11: ADDRESS 0X56 – PLL PRESCALER (LSB)

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PLL_PRE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **PLL_PRE<7:0>**: PLL prescaler selection (**Note 1**)
 1111-1111 = VCO clock divided by 255 (if PLL_PRE<11:8> = 0000)
 .
 .
 .
 0111-1000 = VCO clock divided by 120 (if PLL_PRE<11:8> = 0000) (**Default**)
 .
 .
 .
 0000-0010 = VCO clock divided by 2 (if PLL_PRE<11:8> = 0000)
 0000-0001 = VCO clock divided by 1 (if PLL_PRE<11:8> = 0000)
 0000-0000 = VCO clock not divided (if PLL_PRE<11:8> = 0000)

Note 1: PLL_PRE is a 12 bit-wide setting. The upper four bits (PLL_PRE<11:8>) are defined in Address 0x57. See [Table 4-3](#) for the PLL_PRE<11:0> bit settings. The PLL Prescaler is used to divide down the VCO output clock in the PLL phase-frequency detector loop circuit.

REGISTER 5-12: ADDRESS 0X57 – PLL PRESCALER (MSB)

| | | | | | | | |
|----------|-------|-------|-------|---------------|-------|-------|-------|
| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FCB<3:0> | | | | PLL_PRE<11:8> | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **FCB<3:0>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.
 bit 3-0 **PLL_PRE<11:8>**: PLL prescaler selection (**Note 1**)
 1111 = $2^{12} - 1$ (max), if PLL_PRE<7:0> = 0xFF
 .
 .
 .
 0000 = (**Default**)

Note 1: PLL_PRE is a 12 bit-wide setting. See the lower eight bit settings (PLL_PRE<7:0>) in Address 0x56 ([Register 5-11](#)). See [Table 4-3](#) for the PLL_PRE<11:0> bit settings for PLL feedback frequency.

MCP37231/21-200 AND MCP37D31/21-200

TABLE 5-5: Example: PLL Prescaler Bit Settings and PLL Feedback Frequency

| PLL_PRE<11:0> | PLL Feedback Frequency |
|----------------|--|
| 1111-1111-1111 | VCO clock divided by 4095 ($2^{12} - 1$) |
| 1111-1111-1110 | VCO clock divided by 4094 ($2^{12} - 2$) |
| --- | --- |
| 0000-0000-0011 | VCO clock divided by 3 |
| 0000-0000-0010 | VCO clock divided by 2 |
| 0000-0000-0001 | VCO clock divided by 1 |
| 0000-0000-0000 | VCO clock divided by 1 |

REGISTER 5-13: ADDRESS 0X58 – PLL CHARGE-PUMP

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
|----------|-------|-------|----------|-------------------|-------|-------|-------|
| FCB<2:0> | | | PLL_BIAS | PLL_CHAGPUMP<3:0> | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **FCB<2:0>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.

bit 5 **PLL_BIAS**: PLL charge-pump bias source selection bit (**Note 1**)
 1 = Self-biasing coming from AVDD
 0 = Bandgap voltage from the reference generator (1.2V) (**Default**)

bit 4-0 **PLL_CHAGPUMP<3:0>**: PLL charge-pump bias current control bits (**Note 2**)
 1111 = Maximum current
 .
 .
 .
 0010 = (**Default**)
 .
 .
 .
 0000 = Minimum current

- Note 1:** This bit can be controlled by the factory.
2: PLL_CHAGPUMP<3:0> bits should be set based on the phase detector comparison frequency. The bias current amplitude increases linearly with increasing the bit setting values. The increase is from approximately 25 μ A to 375 μ A, 25 μ A per step. See [Section 4.7.2 “PLL output frequency and control Parameters”](#) for more details of the PLL block.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-14: ADDRESS 0X59 – PLL ENABLE CONTROL 1

| | | | | | | | |
|-------|----------|---------------|----------|--------|--------|-------|-------|
| U-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| — | FCB<4:3> | EN_PLL_REFDIV | FCB<2:1> | EN_PLL | FCB<0> | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **Unimplemented:** Not used.
- bit 6-5 **FCB<4:3>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.
- bit 4 **EN_PLL_REFDIV**: Enable PLL Reference Divider (PLL_REFDIV<9:0>).
 1 = Enable PLL_REFDIV<9:0> register
 0 = Reference divider is bypassed (**Default**)
- bit 3-2 **FCB<2:1>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.
- bit 1 **EN_PLL**: Master enable bit for PLL circuit.
 1 = Enable PLL circuit
 0 = Disable PLL circuit (**Default**)
- bit 0 **FCB<0>**: Factory-Controlled bits. This is not for the user. Do not change the default settings.

REGISTER 5-15: ADDRESS 0X5A – PLL LOOP FILTER RESISTOR

| | | | | | | | |
|-------|----------|--------------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| — | FCB<1:0> | PLL_RES<4:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **Unimplemented:** Not used.
- bit 6-5 **FCB<1:0>**: Factory-Controlled bits. This is not for the user. Do not program.
- bit 4-0 **PLL_RES<4:0>**: Resistor value selection bits for PLL loop filter (**Note 1**)
 11111 = Maximum value
 .
 .
 .
 00111 = (**Default**)
 .
 .
 .
 00000 = Minimum value

Note 1: PLL_RES<4:0> bits should be set based on the phase detector comparison frequency. The resistor value increases linearly with the bit settings, from minimum to maximum values. See the PLL loop filter section in [Section 4.7 “ADC Clock Selection and PLL Output Frequency Control”](#).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-16: ADDRESS 0X5B – PLL LOOP FILTER CAP3

| | | | | | | | |
|-------|----------|-------|---------------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| — | FCB<1:0> | | PLL_CAP3<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.
bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not program.
bit 4-0 **PLL_CAP3<4:0>:** Capacitor 3 value selection bits for PLL loop filter ([Note 1](#))
11111 = Maximum value
.
.
.
01111 = **(Default)**
.
.
.
00000 = Minimum value

Note 1: This capacitor is in series with the shunt resistor, which is set by PLL_RES<4:0> bits. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-17: ADDRESS 0X5C – PLL LOOP FILTER CAP1

| | | | | | | | |
|-------|----------|-------|---------------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| — | FCB<1:0> | | PLL_CAP1<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.
bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not program.
bit 4-0 **PLL_CAP1<4:0>:** Capacitor 1 value selection bits for PLL loop filter ([Note 1](#))
11111 = Maximum value
.
.
.
00111 = **(Default)**
.
.
.
00000 = Minimum value

Note 1: This capacitor is located between the charge-pump output and ground, and in parallel with the shunt resistor which is defined by the PLL_RES<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-18: ADDRESS 0X5D – PLL LOOP FILTER CAP2

| | | | | | | | |
|-------|----------|-------|---------------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| — | FCB<1:0> | | PLL_CAP2<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.
 bit 6-5 **FCB<1:0>:** Factory-Controlled bits. This is not for the user. Do not program.
 bit 4-0 **PLL_CAP2<4:0>:** Capacitor 2 value selection bits for PLL loop filter ([Note 1](#))
 11111 = Maximum value
 .
 .
 .
 00111 = **(Default)**
 .
 .
 .
 00000 = Minimum value

Note 1: This capacitor is located between the charge-pump output and ground, and in parallel with CAP1 which is defined by the PLL_CAP1<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-19: ADDRESS 0X5F – PLL ENABLE CONTROL 2 ([Note 1](#))

| | | | | | | | |
|----------|-------|-------|-------|------------|-------------|----------|-------|
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| FCB<5:2> | | | | EN_PLL_OUT | EN_PLL_BIAS | FCB<1:0> | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **FCB<5:2>:** Factory-Controlled bits. This is not for the user. Do not change the default settings.
 bit 3 **EN_PLL_OUT:** Enable PLL output.
 1 = Enable PLL output
 0 = Disable PLL output (**Default**)
 bit 2 **EN_PLL_BIAS:** Enable PLL bias
 1 = Enable PLL bias
 0 = Disable PLL bias (**Default**)
 bit 1-0 **FCB<2:1>:** Factory-Controlled bits. This is not for the user. Do not change the default settings.
Note 1: To enable PLL output, EN_PLL_OUT, EN_PLL_BIAS and EN_PLL in Address 0x59 ([Register 5-14](#)) must be set.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-20: ADDRESS 0X62 – OUTPUT DATA FORMAT AND OUTPUT TEST PATTERN

| U-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|----------|-------------|-------------|-------|---------------|-------|-------|
| — | LVDS_8CH | DATA_FORMAT | OUTPUT_MODE | | TEST_PATTERNS | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

| | |
|---------|--|
| bit 7 | Unimplemented: Not used. |
| bit 6 | LVDS_8CH: LVDS data stream type selection for octal-channel mode (Note 1) 1 = Serialized data stream (Note 2) 0 = Interleaved with parallel data stream (Note 3)(Default) |
| bit 5 | DATA_FORMAT: Output data format selection 1 = Offset binary (unsigned) 0 = two's complement (Default) |
| bit 4-3 | OUTPUT_MODE<1:0>: Output mode selection (Note 7) 11 = Select DDR LVDS output mode with MSB byte first (Note 4) 10 = Select DDR LVDS output mode with even bit first (Note 5)(Default) 01 = Select CMOS output mode 00 = Output disabled |
| bit 2-0 | TEST_PATTERNS<2:0>: Test output data pattern selection 111 = Output data is pseudo-random number (PN) sequence (Note 6) 110 = Sync Pattern for LVDS output. 18-bit mode: '11111111 00000000 10' 16-bit mode: '11111111 00000000' 14-bit mode: '11111111 0000000' 12-bit mode: '11111111 0000' 10-bit mode: '11111111 00' 101 = Alternating Sequence for LVDS output 16-bit mode: '01010101 10101010' 14-bit mode: '01010101 101010' 100 = Alternating Sequence for CMOS. Output: '11111111 11111111' alternating with '00000000 00000000' 011 = Alternating Sequence for CMOS. Output: '01010101 01010101' alternating with '10101010 10101010' 010 = Ramp Pattern. Outputs are incremented by: 18-bit mode: 1 LSB per clock cycle 16-bit mode: 1 LSB per 4 clock cycles 14-bit mode: 1 LSB per 16 clock cycles 001 = Double Custom Patterns. Output: Alternating custom pattern A (see Addresses 0X74 – 0X75 - Registers 5-29 to 5-30) and custom pattern B (see Address 0X76 - 0X77 - Registers 5-31 to 5-32) (Note 8) 000 = Normal Operation. Output: ADC data (Default) |

- Note 1:** This bit setting is valid for the octal-channel mode only. See Address 0x7D - 0x7F ([Registers 5-38 to 5-40](#)) for channel order selection.
- Note 2:** Serialized LVDS is available in octal-channel with 16-bit mode only: Each LVDS output pair holds a single input channel's data and outputs in a serial data stream (synchronized with WCK): Q7+/Q7- is for the first channel selected data, and Q0+/Q0- is for the last channel selected data. This bit function is enabled only when SEL_DSPP = 1 in Address 0x81 ([Register 5-42](#)). See [Figure 2-4](#) for the timing diagram.
- Note 3:** The output is in parallel data stream. The first sampled data is clocked out first in parallel LVDS output pins, followed by the next sampled channel data. See [Figures 2-2 and 2-3](#) for the timing diagram.
- Note 4:** Only 16-bit mode is available for this option.
Rising edge: Q15-Q8.
Falling edge: Q7-Q0
- Note 5:** Rising edge: Q14, Q12, Q10,.... Q0.
Falling edge: Q15, Q13, Q11,.... Q1.
- Note 6:** Pseudo-random number (PN) code is generated by the linear feedback shift register (LFSR).
- Note 7:** See [Figures 2-1 to 2-4](#) for the timing diagram.
- Note 8:** The alternating patterns A and B are applied to Q<15:0>. Pattern A<15:14> and Pattern B<15:14> are also applied to OVR and WCK pins, respectively. Pattern A<1:0> and Pattern B<1:0> are also applied to DM1/DM+ and DM2/DM-.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-21: ADDRESS 0X63 – ADC OUTPUT BIT (RESOLUTION) AND LVDS LOAD

| | | | | | | | |
|------------|-------|-------|-------|-----------|------------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| OUTPUT_BIT | | | | LVDS_LOAD | LVDS_IMODE | | |
| bit 7 | | | | | bit 0 | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-4 **OUTPUT_BIT<3:0>**: Select number of output data bits ([Note 1](#))

1111 = 15
 1110 = 14
 1101 = 13
 1100 = 12
 1011 = 11
 1010 = 10
 1001 = 9
 1000 = 8
 0111 = 7
 0110 = 6
 0101 = 5
 0100 = 4
 0011 = 3
 0010 = 2
 0001 = 1

0000 = 16-bit (**Default**)

bit 3 **LVDS_LOAD**: Internal LVDS load termination

1 = Enable internal load termination
 0 = Disable internal load termination (**Default**)

bit 2-0 **LVDS_IMODE<2:0>**: LVDS driver current control bits

111 = 7.2 mA
 011 = 5.4 mA
 001 = 3.5 mA (**Default**)
 000 = 1.8 mA

Do not use the following settings ([Note 2](#)):

110, 101, 100, 010

Note 1: These bits can be preprogrammed at the factory. See Address 0x68 ([Register 5-26](#)) for additional DM1 and DM2 bits. Serialized LVDS output or LVDS output with MSB byte first mode: only 16-bit is available.

2: These settings can result in unknown outputs currents.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-22: ADDRESS 0X64 – OUTPUT CLOCK PHASE CONTROL WHEN DECIMATION FILTER IS USED

| | | | | | | | |
|--------------|---------------------|-------|-------|----------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
| EN_PHDLY_DEC | DCLK_PHDLY_DEC<2:0> | | | FCB<3:0> | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **EN_PHDLY_DEC:** Enable digital output clock phase delay control when decimation filter is used.

- 1 = DCLK_PHDLY_DEC<2:0> setting is enabled (**Note 1**)
- 0 = DCLK_PHDLY_DEC<2:0> setting is disabled (**Default**)

bit 6-4 **DCLK_PHDLY_DEC<2:0>:** Digital output clock phase delay control when decimation filter is used (**Note 2**)

- 111 = 315° phase-shifted (**Note 3**)
- 110 = 270° phase-shifted
- 101 = 225° phase-shifted (**Note 3**)
- 100 = 180° phase-shifted
- 011 = 135° phase-shifted (**Note 3**)
- 010 = 90° phase-shifted
- 001 = 45° phase-shifted (**Note 3**)
- 000 = In-Phase (**Default**)

bit 3-0 **FCB<3:0>:** Factory-Controlled bits. This is not for the user. Do not program.

- Note 1:** This feature is only used in conjunction with the decimation filter options where the core clock frequency is faster than the output clock frequency.
- 2:** This bit is enabled only if EN_PHDLY_DEC = 1. These bits are used when the divided clocks are used. See OUT_CLKRATE<3:0> bits in Address 0x02 (**Register 5-3**). When the full speed clock is selected, the same feature is provided by the DLL phases. See Address 0x52 (**Register 5-7**).
- 3:** Only available when the decimation filter setting is greater than 2. When FIR_A/B <8:1> = 0's (default) and FIR_A<6> = 0, only 4-phases are available (0, 90, 180, 270). See Addresses 0x7A, 0x7B and 0x7C (**Registers 5-35 to 5-37**). See address 0x6D and 0x52 DCLK (**Registers 5-28 and 5-7**) phase shift for other modes.

REGISTER 5-23: ADDRESS 0X65 – LVDS OUTPUT POLARITY

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| POL_LVDS<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **POL_LVDS<7:0>:** Control polarity of LVDS data pairs

- 1111-1111 = Invert all LVDS pairs
- 1111-1110 = Invert all LVDS pairs except the LSB pair
-
-
-
- 1000-0000 = Invert MSB LVDS pair
-
-
-
- 0000-0001 = Invert LSB LVDS pair
- 0000-0000 = No inversion of LVDS bit pairs (**Default**)

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-24: ADDRESS 0X66 – DIGITAL OFFSET CORRECTION (LOWER BYTE)

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DIG_OFFSET <7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **DIG_OFFSET <7:0>**: Lower byte of DIG_OFFSET<15:0> (**Note 1**)
 0000-0000 = **Default**

Note 1: Offset is added to the ADC output. Setting is two's complement. Step size of each bit setting of the combined register is equal to:

- 0.125 LSB for 12-bit ADC
- 0.25 LSB for 14-bit, ADC
- 0.5 LSB for 16-bit ADC
- 1 LSB for 18-bit ADC.

REGISTER 5-25: ADDRESS 0X67 – DIGITAL OFFSET CORRECTION (UPPER BYTE)

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DIG_OFFSET<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **DIG_OFFSET <15:8>**: Upper byte of DIG_OFFSET<15:0> (**Note 1**)
 0000-0000 = **Default**

Note 1: Offset is added to the ADC output. Setting is two's complement. Step size of each bit setting of the combined register is equal to:

- 0.125 LSB for 12-bit ADC
- 0.25 LSB for 14-bit, ADC
- 0.5 LSB for 16-bit ADC
- 1 LSB for 18-bit ADC.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-26: ADDRESS 0X68 – WCK/OVR PAIR AND DM1/DM2

| | | | | | | | |
|----------|-------|-------|-------|-------------|------------|--------|------------|
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
| FCB<3:0> | | | | POL_WCK_OVR | EN_WCK_OVR | DM1DM2 | POL_DM1DM2 |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7-4 **FCB<3:0>**: Factory-Controlled bits. This is not for the user. Do not program.
- bit 3 **POL_WCK_OVR**: Polarity control for WCK and OVR bit pair in LVDS mode
 1 = Inverted
 0 = Not inverted (**Default**)
- bit 2 **EN_WCK_OVR**: Enable WCK and OVR output bit pair
 1 = Enabled (**Default**)
 0 = Disabled
- bit 1 **DM1DM2**: Add two additional LSB bits (DM1/DM+ and DM2/DM- bits) to the data stream.
 1 = Added (**Note 1**)
 0 = Not added (**Default**)
- bit 0 **POL_DM1DM2**: Polarity control for DM1/DM+ and DM2/DM- pair in LVDS mode
 1 = Inverted
 0 = Not inverted (**Default**)

Note 1: When this bit is set, two additional LSB bits (DM1/DM+ and DM2/DM-, DM2/DM- is the LSB) can be added by using the decimation filters. See Address 0x7B and 0x7C ([Registers 5-36](#) and [5-37](#)) for the decimation filter settings. Requirement of decimation factor for two additional bits: 256x for single channel and 128x for dual channel mode. See Address 0x63 ([Register 5-21](#)) for the output bit control.

REGISTER 5-27: ADDRESS 0X6B – PLL CALIBRATION

| | | | | | | | |
|----------|-------|-------|-------|-------|-------------|-------------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| FCB<4:0> | | | | | PLL_CALTRIG | FCBFCB<1:0> | |
| bit 7 | | | | | bit 0 | | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7-3 **FCB<4:0>**: Factory-Controlled bits. This is not for the user. Do not program.
- bit 3 **PLL_CALTRIG**: Manually force recalibration of the PLL at the state of bit transition (**Note 1**)
 Toggle from "1" to "0", or "0" to "1" = Start PLL calibration
- bit 2-0 **FCBFCB<1:0>**: Factory-Controlled bits. This is not for the user. Do not program.

Note 1: PLL calibration status is observed by the PLL calibration status bit PLL_CAL in Address 0xD1 ([Register 5-81](#)). PLL should be recalibrated following a change in input frequency or PLL configuration registers (Address 0x54 - 0x57, [Registers 5-9](#) to [5-12](#)).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-28: ADDRESS 0X6D – PLL OUTPUT AND OUTPUT CLOCK PHASE (Note 1)

| | | | | | | | |
|-------|-----|------------|-----------|----------------|-------|-------|-------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| – | | EN_PLL_CLK | PLL_PHASE | PLL_PHDLY<3:0> | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-3 **Unimplemented:** Not used

bit 3 **EN_PLL_CLK:** Enable PLL output clock
 1 = PLL output clock is enabled to the ADC core
 0 = PLL clock output is disabled (**Default**)

bit 2-0 **PLL_PHASE:** Select PLL phase for internal delay line
 1 = Falling Edge
 0 = Rising Edge (**Default**)

bit 2-0 **PLL_PHDLY<3:0>:** Output clock is delayed by the number of VCO clock cycles from the nominal PLL output (**Note 2**)
 1111 = Delay of 15 cycles
 1110 = Delay of 14 cycles
 .
 .
 .
 0001 = Delay of one cycle
 0000 = No delay (**Default**)

- Note 1:** This register has effect only when the PLL clock is selected by CLK_SOURCE bit in Address 0x53 (Register 5-8) and PLL circuit is enabled by EN_PLL bit in Address 0x59 (Register 5-14).
Note 2: This bit setting enables the output clock phase delay. This phase delay control option is applicable when PLL is used as the clock source and the decimation is not used.

REGISTER 5-29: ADDRESS 0X74 – USER-DEFINED OUTPUT PATTERN A (LOWER BYTE)

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PATTERN_A<7:0> | | | | | | | |
| bit 7 | | | | | | bit 0 | |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **PATTERN_A<7:0>:** Lower byte of PATTERN_A<15:0> (**Note 1**)

- Note 1:** See PATTERN_A<15:8> in Address 0x75 (Register 5-30) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-30: ADDRESS 0X75 – USER-DEFINED OUTPUT PATTERN A (UPPER BYTE)

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PATTERN_A<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **PATTERN_A<15:8>**: Upper byte of PATTERN_A<15:0> ([Note 1](#))

Note 1: See PATTERN_A<7:0> in Address 0x74 ([Register 5-29](#)) and TEST_PATTERNS<2:0> in Address 0x62 ([Register 5-20](#)).

REGISTER 5-31: ADDRESS 0X76 – USER-DEFINED OUTPUT PATTERN B (LOWER BYTE)

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PATTERN_B<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **PATTERN_B<7:0>**: Lower byte of PATTERN_B<15:0> ([Note 1](#))

Note 1: See PATTERN_B<15:8> in Address 0x77 ([Register 5-32](#)) and TEST_PATTERNS<2:0> in Address 0x62 ([Register 5-20](#)).

REGISTER 5-32: ADDRESS 0X77 – USER-DEFINED OUTPUT PATTERN B (UPPER BYTE)

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PATTERN_B<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **PATTERN_B<15:8>**: Upper byte of PATTERN_B<15:0> ([Note 1](#))

Note 1: See PATTERN_B<7:0> in Address 0x76 ([Register 5-31](#)) and TEST_PATTERNS<2:0> in Address 0x62 ([Register 5-20](#)).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-33: ADDRESS 0X78 – NOISE SHAPING REQUANTIZER CHANNEL A FILTER (NSRA)(Note 1)

| | | | | | | | |
|-----------|-----------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| NSR_RESET | NSRA<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **NSR_RESET:** Toggle of this bit causes a reset of the NSRA and NSRB state.
 - Toggle from '1' to '0', or '0' to '1' = Reset of NSRA and NSRB
 - Otherwise = No effect (**Default**)

bit 6-0 **NSRA<6:0>:** Noise-Shaping requantizer (NSR) filter settings for single or dual channel (Channel A only)
 000-0000 = (**Default**)

Note 1: This register setting is not used for this device. Do not change the factory default setting.

REGISTER 5-34: ADDRESS 0X79 – DUAL-CH DSPP AND NOISE SHAPING REQUANTIZER CHANNEL B FILTER (NSRB) (Note 1)

| | | | | | | | |
|-------------|-----------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| EN_DSPPDUAL | NSRB<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **EN_DSPPDUAL:** Enable all digital post-processing functions for dual channel operations (**Note 2**)
 1 = Dual channel DDC is enabled.
 0 = Disabled (**Default**)

bit 6-0 **NSRB<6:0>:** Noise-Shaping requantizer (NSR) filter settings for single or dual channel (Channel B only)(**Note 2**)

111-1111 =
 111-1110 =
 •
 •
 •
 000-0001 =
 000-0000 = (**Default**)

Note 1: This register is used for single and dual-channel modes only. NSRB is not used for this device.

Note 2: This bit setting is not used for this device. Do not change the factory default setting.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-35: ADDRESS 0X7A – FRACTIONAL DELAY RECOVERY AND FIR_A0 (Note 1)

| | | | | | | | |
|-------|----------|--------|-------|-------------|-------------|-------------|-------------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | FIR_A<0> | EN_FDR | FCB | EN_NS RB_11 | EN_NS RB_12 | EN_NS RA_11 | EN_NS RA_12 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **Unimplemented:** Not used
- bit 6 **FIR_A<0>:** Enable the first 2x decimation (Stage 1A in FIR A) in single-channel mode (Note 2)
 - 1 = Enabled
 - 0 = Disabled (**Default**)
- bit 5 **EN_FDR:** Fractional Delay Recovery (FDR) control bit
 - 1 = Enabled (with delay of 59 samples)
 - 0 = Disabled (**Default**)
- bit 4 **FCB:** Factory-Controlled bits. This is not for the user. Do not program.
- bit 3 **EN_NS RB_11:** Enable 11-bit noise-shaping requantizer for Channel B (Note 3)
 - 1 = Enabled
 - 0 = Disabled (**Default**)
- bit 2 **EN_NS RB_12:** Enable 12-bit noise shaping requantizer for Channel B (Note 3)
 - 1 = Enabled
 - 0 = Disabled (**Default**)
- bit 1 **EN_NS RA_11:** Enable 11-bit noise shaping requantizer for Channel A (Note 3)
 - 1 = Enabled
 - 0 = Disabled (**Default**)
- bit 0 **EN_NS RA_12:** Enable 12-bit noise shaping requantizer for Channel A (Note 3)
 - 1 = Enabled
 - 0 = Disabled (**Default**)

- Note 1:** This register is used only for single and dual-channel modes.
- 2:** FIR_A<0> = 1 for single channel mode, and FIR_A<0> = 0 for dual channel mode. See Address 0x7B (Register 5-36) for FIR_A<8:1>.
- 3:** This bit setting is not used for this device. Do not change the factory default setting.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-36: ADDRESS 0X7B – FIR A FILTER (Note 1, Note 2)

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FIR_A<8:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **FIR_A<8:0>**: Decimation Filter FIR A settings for Channel A (or I)(Note 3, Note 6)

Single-Channel Mode: (Note 4)

- 1-1111-1111 = Enabled stage 1 - 9 filters (decimation rate: 512)
- 0-1111-1111 = Enabled stage 1 - 8 filters
- 0-0111-1111 = Enabled stage 1 - 7 filters
- 0-0011-1111 = Enabled stage 1 - 6 filters
- 0-0001-1111 = Enabled stage 1 - 5 filters
- 0-0000-1111 = Enabled stage 1 - 4 filters
- 0-0000-0111 = Enabled stage 1 - 3 filters (decimation rate = 8)
- 0-0000-0011 = Enabled stage 1 - 2 filters (decimation rate = 4)
- 0-0000-0001 = Enabled stage 1 filter (decimation rate = 2)
- 0-0000-0000 = Disabled all FIR A filters. **(Default)**

Dual-Channel Mode: (Note 5)

- 1-1111-1110 = Enabled stage 2 - 9 filters (decimation rate: 256)
- 0-1111-1110 = Enabled stage 2 - 8 filters
- 0-0111-1110 = Enabled stage 2 - 7 filters
- 0-0011-1110 = Enabled stage 2 - 6 filters
- 0-0001-1110 = Enabled stage 2 - 5 filters
- 0-0000-1110 = Enabled stage 2 - 4 filters
- 0-0000-0110 = Enabled stage 2 - 3 filters
- 0-0000-0010 = Enabled stage 2 filter (decimation rate = 2)
- 0-0000-0000 = Disabled all FIR A filters. **(Default)**

- Note 1:** This register is used only for single and dual-channel modes. The register values are thermometer encoded.
- 2:** By using the decimation filters, two additional bits can be obtained. See DM1DM2 bit setting in Address 0x68 (Register 5-26) for details. The register value can be pre-programmed at the factory.
- 3:** SNR is improved by approximately 2.5 dB per each filter stage, but output data rate is reduced by a factor of 2 per stage. The data and clock rates in Address 0X02 (Register 5-3) need to be updated accordingly when this register is updated. Address 0x64 (Register 5-22) setting is also affected. The maximum decimation factor for the single-channel mode is 512, and 256 for the dual channel mode.
- 4:** In single-channel mode, the 1st stage filter is selected by FIR_A<0> = 1 in Address 0x7A (Register 5-35).
- 5:** In dual-channel mode, the 1st stage filter is disabled by setting FIR_A<0> = 0 in Address 0x7A (Register 5-35).
- 6:** LSB is corresponding to FIR_A<0> in Address 0x7A. See Section 4.8.2 “Decimation Filters” for the decimation filter.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-37: ADDRESS 0X7C – FIR B FILTER (Note 1, Note 2)

| | | | | | | | |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FIR_A<8:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **FIR_B<7:0>**: Decimation Filter FIR B settings for Channel B (or Q) (Note 3, Note 4)

1111-1111 = Enabled stage 2 - 9 filters (decimation rate = 256)

0111-1111 = Enabled stage 2 - 8 filters

0011-1111 = Enabled stage 2 - 7 filters

0001-1111 = Enabled stage 2 - 6 filters

0000-1111 = Enabled stage 2 - 5 filters

0000-0111 = Enabled stage 2 - 4 filters

0000-0011 = Enabled stage 2 - 3 filters

0000-0001 = Enabled stage 2 filter (decimation rate = 2)

0000-0000 = Disabled all FIR B Filters. (Default)

- Note 1:** This register is used for the dual-channel mode only. The register values are thermometer encoded and they can be pre-programmed at the factory.
- 2:** EN_DSPPDUAL bit in Address 0x79 (Register 5-34) must be set when using decimation in dual-channel mode.
- 3:** By using the decimation filters, two additional bits can be obtained. See DM1DM2 bit setting in Address 0x68 (Register 5-26) for details. SNR is improved by approximately 2.5 dB per each filter stage, but output data rate is reduced by a factor of 2 per stage. The maximum decimation factor for the dual-channel mode is 256. The data and clock rates in Address 0x02 (Register 5-3) need to be updated accordingly when this register is updated. Address 0x64 (Register 5-22) setting is also affected.
- 4:** See Section 4.8.2 “Decimation Filters” for the decimation filter.

REGISTER 5-38: ADDRESS 0X7D – AUTO-SCAN CHANNEL ORDER (LOWER BYTE)

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
| CH_ORDER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **CH_ORDER<7:0>**: Lower byte of CH_ORDER<31:0> (Note 1)

0111-1000 = Default

- Note 1:** See Table 4-1 for the channel order selection. See SEL_NCH<2:0> in Address 0x01 (Register 5-2) for the number of channels to be selected.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-39: ADDRESS 0X7E – AUTO-SCAN CHANNEL ORDER (MIDDLE BYTE)

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH_ORDER<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH_ORDER<15:8>**: Middle byte of CH_ORDER<31:0> (**Note 1**)
1010-1100 = **Default**

Note 1: See [Table 4-1](#) for the channel order selection. See SEL_NCH<2:0> in Address 0x01 ([Register 5-2](#)) for the number of channels to be selected.

REGISTER 5-40: ADDRESS 0X7F – AUTO-SCAN CHANNEL ORDER (UPPER BYTE)

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 |
| CH_ORDER<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH_ORDER<23:16>**: Upper byte of CH_ORDER<31:0> (**Note 1**)
1000-1110 = **Default**

Note 1: See [Table 4-1](#) for the channel order selection. See SEL_NCH<2:0> in Address 0x01 ([Register 5-2](#)) for the number of channels to be selected.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-41: ADDRESS 0X80 – DIGITAL DOWN-CONVERTER CONTROL 1 (Note 1)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------------|------------|--------|------------|------------|---------|-------------|---------|
| HBFILTER_B | HBFILTER_A | EN_NCO | EN_AMPDITH | EN_PHSDITH | EN_LFSR | EN_DDC_FS/8 | EN_DDC1 |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 7 **HBFILTER_B**: Select half-bandwidth filter at DDC output of channel B in dual-channel mode (Note 2).
 1 = Select High-Pass filter at DDC output
 0 = Select Low-Pass filter at DDC output (Default)
- bit 6 **HBFILTER_A**: Select half-bandwidth filter at DDC output of channel A (Note 2)
 1 = Select High-Pass filter at DDC output
 0 = Select Low-Pass filter at DDC output (Default)
- bit 5 **EN_NCO**: Enable NCO of DDC1
 1 = Enabled
 0 = Disabled (Default)
- bit 4 **EN_AMPDITH**: Enable amplitude dithering for NCO (Note 3, Note 4)
 1 = Enabled
 0 = Disabled (Default)
- bit 3 **EN_PHSDITH**: Enable phase dithering for NCO (Note 3, Note 4)
 1 = Enabled
 0 = Disabled (Default)
- bit 2 **EN_LFSR**: Enable linear feedback shift register (LFSR) for amplitude and phase dithering for NCO
 1 = Enabled
 0 = Disabled (Default)
- bit 1 **EN_DDC_FS/8**: Enable NCO for the DDC2 to center the DDC output signal to be around $f_s/8/DER$ (Note 5)
 1 = Enabled
 0 = Disabled (Default)
- bit 0 **EN_DDC1**: Enable digital down converter 1 (DDC1)
 1 = Enabled (Note 6)
 0 = Disabled (Default)

- Note 1:** This register is used for single, dual-channel and octal-channel modes when CW feature is enabled (8CH_CW = 1).
- 2:** This filter includes a decimation of 2.
 -Single-Channel mode: use only HBFILTER_A
 -Dual-Channel mode: use both HBFILTER_A and HBFILTER_B.
- 3:** This requires the LFSR to be enabled: <EN_LFSR>=1
- 4:** EN_AMPDITH = 1 and EN_PHSDITH = 1 are recommended for the best performance.
- 5:** DER is the decimation filters defined by FIR A or FIR B filter. If up-converter is not enabled (disabled), output is I/Q data.
- 6:** DDC and NCO are enabled. For DDC function, bits 0, 2 and 5 need to be enabled all together.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-42: ADDRESS 0X81 – DIGITAL DOWN-CONVERTER CONTROL 2

| | | | | | | | |
|----------|---------|--------------|---------|----------|--------|---------------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| FDR_BAND | EN_DDC2 | GAIN_HBF_DDC | SEL_FDR | SEL_DSPP | 8CH_CW | GAIN_8CH<1:0> | |
| bit 7 | | | | | | bit 0 | |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 7 **FDR_BAND:** Select 1st or 2nd Nyquist band
 1 = 2nd Nyquist band
 0 = 1st Nyquist band (**Default**)
- bit 6 **EN_DDC2:** Enable DDC2 after the digital half-band filter (HBF) in DDC.
 1 = Enabled
 0 = Disabled (**Default**)
- bit 5 **GAIN_HBF_DDC:** Gain select for the output of the digital half-band filter (HBF) in DDC (**Note 1**)
 1 = x2
 0 = x1 (**Default**)
- bit 4 **SEL_FDR:** Select fractional delay recovery (FDR) for 8-channel or dual-channel mode (**Note 2, Note 3**)
 1 = FDR for 8-channel
 0 = FDR for dual-channel (**Default**)
- bit 3 **SEL_DSPP:** Select digital signal post-processing (DSPP) features for 8-channel or dual-channel mode (**Note 2, Note 3**)
 1 = DSPP for 8-channel
 0 = DSPP for dual-channel (**Default**)
- bit 2 **8CH_CW:** Enable CW mode in octal-channel mode (**Note 3, Note 4**)
 1 = Enabled
 0 = Disabled (**Default**)
- bit 1-0 **GAIN_8CH<1:0>:** Select gain factor for CW signal in octal-channel modes.
 11 = x8, 10 = x4, 01 = x2, 00 = x1 (**Default**)

- Note 1:** The half-band filters (HBF) are used by splitting a full-band signal of bandwidth B into two half-bandwidth (B/2). Since the bandwidth is reduced by a factor of 2, the sampling rate requirement is also reduced by a factor of 2, which is equivalent to oversampling by a factor of 2 (x2). The HBFs are used in the sub-band coding of digital video and audio signal applications. Also used for digital interpolation and decimation in signal processing.
- 2:** Fractional delay compensates digitally for the sampling skew caused by round-robin style sampling of the inputs. See [Section 4.8.1 “Fractional Delay Recovery for Dual and Octal-Channel modes”](#) for details.
- 3:** By enabling this bit, the phase offset corrections in the Address 0x086 – 0x095 ([Registers 5-47 to 5-62](#)) are also enabled. SEL_DSPP is a global set bit to enable SEL_FDR bit and LVDS_8CH bit (Address 0x62 - [Register 5-20](#)).
- 4:** When CW mode is enabled, the ADC output is the result of the summation (addition) of all 8 channel data after each channel’s digital phase offset, digital gain, and digital offset are controlled using the Address 0x86 - 0xA7 ([Registers 5-47 to 5-79](#)). The result is similar to the beamforming in the phased-array sensors.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-43: ADDRESS 0X82 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (LOWER BYTE) (Note 1)

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NCO_TUNE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **NCO_TUNE <7:0>**: Lower byte of NCO_TUNE<31:0> (Note 2).
 0000-0000 = DC (0 Hz) when NCO_TUNE<31:0> = 0000 0000 (Default)

- Note 1:** This Register is used only when DDC is enabled: EN_DDC1 = 1 in Address 0x80 (Register 5-41). See Section 4.8.3.4 “Numerically Controlled Oscillator (NCO)” for the details of NCO.
- 2:** NCO frequency = $(\text{NCO_TUNE}<31:0>/2^{32}) \times f_s/2$, where f_s is the sampling clock frequency.

REGISTER 5-44: ADDRESS 0X83 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE LOWER BYTE) (Note 1)

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NCO_TUNE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **NCO_TUNE<15:8>**: Middle lower byte of NCO_TUNE<31:0> (Note 2).
 0000-0000 = Default

- Note 1:** This Register is used only when DDC is enabled: EN_DDC1 = 1 in Address 0x80 (Register 5-41). See Section 4.8.3.4 “Numerically Controlled Oscillator (NCO)” for the details of NCO.
- 2:** NCO frequency = $(\text{NCO_TUNE}<31:0>/2^{32}) \times f_s/2$, where f_s is the sampling clock frequency.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-45: ADDRESS 0X84 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE UPPER BYTE) (Note 1)

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NCO_TUNE<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **NCO_TUNE<23:16>**: Middle upper byte of NCO_TUNE<31:0> (Note 2).
 0000-0000 = **Default**

- Note 1:** This Register is used only when DDC is enabled: EN_DDC1 = 1 in Address 0x80 (Register 5-41). See [Section 4.8.3.4 “Numerically Controlled Oscillator \(NCO\)”](#) for the details of NCO.
- 2:** NCO frequency = (NCO_TUNE<31:0>/2³²) x f_S/2, where f_S is the sampling clock frequency.

REGISTER 5-46: ADDRESS 0X85 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (UPPER BYTE) (Note 1)

| | | | | | | | |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| NCO_TUNE<31:24> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **NCO_TUNE<31:24>**: Upper byte of NCO_TUNE<31:0> (Note 2).
 1111-1111 = f_S/2 if NCO_TUNE<31:0> = 0xFFFF FFFF
 •
 •
 •
 0000-0000 = **Default**

- Note 1:** This Register is used only when DDC is enabled: EN_DDC1 = 1 in Address 0x80 (Register 5-41). See [Section 4.8.3.4 “Numerically Controlled Oscillator \(NCO\)”](#) for the details of NCO.
- 2:** NCO frequency = (NCO_TUNE<31:0>/2³²) x f_S/2, where f_S is the sampling clock frequency.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-47: ADDRESS 0X86 – CH0 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1, Note 2)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH0_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH0_NCO_PHASE<7:0>**: Lower byte of CH0_NCO_PHASE<15:0> (Note 3)
 1111-1111 = 1.4° when CH0_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH0_NCO_PHASE<15:0> = 0x0000 (Default)

Note 1: This register (Addresses 0x86 – 0xA7, Registers 5-47 to 5-79) has effect only when the following modes are used:

- CW with DDC mode in octal-channel mode
- Single and dual-channel mode with DDC.

See 8CH_CW bit setting in Address 0x81 (Register 5-42). See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

- 2: CH0 is the 1st channel selected by CH_ORDER<23:0>.
- 3: CH(n)_NCO_PHASE_OFFSET<15:0> = 2¹⁶ x Phase Offset Value/360.

REGISTER 5-48: ADDRESS 0X87: CH0 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH0_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH0_NCO_PHASE<15:8>**: Upper byte of CH0_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995° when CH0_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH0_NCO_PHASE<15:0> = 0x0000 (Default)

Note 1: See Note 1 and Note 2 in Registers 5-47 has effect only when the following modes are used:

- 2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2¹⁶ x Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-49: ADDRESS 0X88 – CH1 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH1_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH1_NCO_PHASE<7:0>**: Lower byte of CH1_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4^0 when CH1_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 .
 .
 .
 0000-0000 = 0^0 when CH1_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH1 is the 2nd channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times \text{Phase Offset Value}/360$.

REGISTER 5-50: ADDRESS 0X89 – CH1 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH1_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH1_NCO_PHASE <15:8>**: Upper byte of CH1_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995^0 when CH1_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 .
 .
 .
 0000-0000 = 0^0 when CH1_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH1 is the 2nd channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times \text{Phase Offset Value}/360$.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-51: ADDRESS 0X8A – CH2 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH2_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH2_NCO_PHASE<7:0>**: Lower byte of CH2_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4° when CH2_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH2_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH2 is the 3rd channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-52: ADDRESS 0X8B – CH2 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH2_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH2_NCO_PHASE <15:8>**: Upper byte of CH2_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995° when CH2_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH2_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH2 is the 3rd channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-53: ADDRESS 0X8C – CH3 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH3_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH3_NCO_PHASE<7:0>**: Lower byte of CH3_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4^0 when CH3_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH3_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH3 is the 4th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-54: ADDRESS 0X8D – CH3 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH3_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH3_NCO_PHASE <15:8>**: Upper byte of CH3_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995^0 when CH3_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH3_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH3 is the 4th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-55: ADDRESS 0X8E – CH4 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH4_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH4_NCO_PHASE<7:0>**: Lower byte of CH4_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4^0 when CH4_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH4_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH4 is the 5th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-56: ADDRESS 0X8F – CH4 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH4_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH4_NCO_PHASE <15:8>**: Upper byte of CH4_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995^0 when CH4_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH4_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH4 is the 5th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-57: ADDRESS 0X90 – CH5 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH5_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH5_NCO_PHASE<7:0>**: Lower byte of CH5_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4^0 when CH5_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH5_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH5 is the 6th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times$ Phase Offset Value/360.

REGISTER 5-58: ADDRESS 0X91 – CH5 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH5_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH5_NCO_PHASE <15:8>**: Upper byte of CH5_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995^0 when CH5_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH5_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH5 is the 6th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times$ Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-59: ADDRESS 0X92 – CH6 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH6_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH6_NCO_PHASE<7:0>**: Lower byte of CH6_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4° when CH6_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH6_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH6 is the 7th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-60: ADDRESS 0X93 – CH6 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH6_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH6_NCO_PHASE <15:8>**: Upper byte of CH6_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995° when CH6_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0° when CH6_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH6 is the 7th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-61: ADDRESS 0X94 – CH7 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

| | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH7_NCO_PHASE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH7_NCO_PHASE<7:0>**: Lower byte of CH7_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 1.4^0 when CH7_NCO_PHASE<15:0> = 0x00FF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH7_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH7 is the 8th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times \text{Phase Offset Value}/360$.

REGISTER 5-62: ADDRESS 0X95 – CH7 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH7_NCO_PHASE<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH7_NCO_PHASE <15:8>**: Upper byte of CH7_NCO_PHASE<15:0> (Note 2)
 1111-1111 = 359.995^0 when CH7_NCO_PHASE<15:0> = 0xFFFF for 16-bit ADC
 •
 •
 •
 0000-0000 = 0^0 when CH7_NCO_PHASE<15:0> = 0x0000 (Default)

- Note 1:** See Note 1 in Registers 5-47. CH7 is the 8th channel selected by CH_ORDER<23:0> bits.
2: CH(n)_NCO_PHASE_OFFSET<15:0> = $2^{16} \times \text{Phase Offset Value}/360$.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-63: ADDRESS 0X96 – CH0 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH0_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **CH0_DIG_GAIN<7:0>**: Digital gain setting for channel 0 (Note 2, Note 3, Note 4)

```

1111-1111 = -0.03125
1111-1110 = -0.0625
1111-1101 = -0.09375
1111-1100 = -0.125
•
•
•
1000-0011 = -3.90625
1000-0010 = -3.9375
1000-0001 = -3.96875
1000-0000 = -4
0111-1111 = 3.96875 (MAX)
0111-1110 = 3.9375
0111-1101 = 3.90625
0111-1100 = 3.875
•
•
•
0011-1100 = 1.875 (Default)
•
•
•
0000-0011 = 0.09375
0000-0010 = 0.0625
0000-0001 = 0.03125
0000-0000 = 0.0

```

- Note 1:** CH0 is the 1st channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.
- 2:** This register's bits can be pre-programmed at the factory.
- 3:** Max = 0x7F(3.96875), Min = 0x80 (-4), Step size = 0x01 (0.03125). Bits from 0x81-0xFF is two's complementary of 0x00-0x80. Negative gain setting inverts output.
- 4:** Default value for 12-/14-/16-bit ADC: 0x38(1.75).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-64: ADDRESS 0X97 – CH1 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH1_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **CH1_DIG_GAIN<7:0>**: Digital gain setting for channel 1 (Note 2)

1111-1111 = -0.03125

1111-1110 = -0.0625

1111-1101 = -0.09375

1111-1100 = -0.125

•

•

•

1000-0011 = -3.90625

1000-0010 = -3.9375

1000-0001 = -3.96875

1000-0000 = -4

0111-1111 = 3.96875 (MAX)

0111-1110 = 3.9375

0111-1101 = 3.90625

0111-1100 = 3.875

•

•

•

0011-1100 = 1.875 (Default)

•

•

•

0000-0011 = 0.09375

0000-0010 = 0.0625

0000-0001 = 0.03125

0000-0000 = 0.0

Note 1: CH1 is the 2nd channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-65: ADDRESS 0X98 – CH2 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH2_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH2_DIG_GAIN<7:0>**: Digital gain setting for channel 2 (Note 2)

1111-1111 = -0.03125
1111-1110 = -0.0625
1111-1101 = -0.09375
1111-1100 = -0.125
•
•
•
1000-0011 = -3.90625
1000-0010 = -3.9375
1000-0001 = -3.96875
1000-0000 = -4
0111-1111 = 3.96875 (MAX)
0111-1110 = 3.9375
0111-1101 = 3.90625
0111-1100 = 3.875
•
•
•
0011-1100 = 1.875 (Default)
•
•
•
0000-0011 = 0.09375
0000-0010 = 0.0625
0000-0001 = 0.03125
0000-0000 = 0.0

Note 1: CH2 is the 3rd channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-66: ADDRESS 0X99 – CH3 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH3_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **CH3_DIG_GAIN<7:0>**: Digital gain setting for channel 3 (Note 2)

1111-1111 = -0.03125
 1111-1110 = -0.0625
 1111-1101 = -0.09375
 1111-1100 = -0.125
 •
 •
 •
 1000-0011 = -3.90625
 1000-0010 = -3.9375
 1000-0001 = -3.96875
 1000-0000 = -4
 0111-1111 = 3.96875 (MAX)
 0111-1110 = 3.9375
 0111-1101 = 3.90625
 0111-1100 = 3.875
 •
 •
 •
 0011-1100 = 1.875 (Default)
 •
 •
 •
 0000-0011 = 0.09375
 0000-0010 = 0.0625
 0000-0001 = 0.03125
 0000-0000 = 0.0

Note 1: CH3 is the 4th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-67: ADDRESS 0X9A – CH4 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH4_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **CH4_DIG_GAIN<7:0>**: Digital gain setting for channel 4 (Note 2)

1111-1111 = -0.03125
 1111-1110 = -0.0625
 1111-1101 = -0.09375
 1111-1100 = -0.125
 •
 •
 •
 1000-0011 = -3.90625
 1000-0010 = -3.9375
 1000-0001 = -3.96875
 1000-0000 = -4
 0111-1111 = 3.96875 (MAX)
 0111-1110 = 3.9375
 0111-1101 = 3.90625
 0111-1100 = 3.875
 •
 •
 •
 0011-1100 = 1.875 (Default)
 •
 •
 •
 0000-0011 = 0.09375
 0000-0010 = 0.0625
 0000-0001 = 0.03125
 0000-0000 = 0.0

Note 1: CH4 is the 5th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-68: ADDRESS 0X9B – CH5 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH5_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **CH5_DIG_GAIN<7:0>**: Digital gain setting for channel 5 (Note 2)

1111-1111 = -0.03125

1111-1110 = -0.0625

1111-1101 = -0.09375

1111-1100 = -0.125

•

•

•

1000-0011 = -3.90625

1000-0010 = -3.9375

1000-0001 = -3.96875

1000-0000 = -4

0111-1111 = 3.96875 (MAX)

0111-1110 = 3.9375

0111-1101 = 3.90625

0111-1100 = 3.875

•

•

•

0011-1100 = 1.875 (Default)

•

•

•

0000-0011 = 0.09375

0000-0010 = 0.0625

0000-0001 = 0.03125

0000-0000 = 0.0

Note 1: CH5 is the 6th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-69: ADDRESS 0X9C – CH6 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH6_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

bit 7-0 **CH6_DIG_GAIN<7:0>**: Digital gain setting for channel 6 (Note 2)

1111-1111 = -0.03125
 1111-1110 = -0.0625
 1111-1101 = -0.09375
 1111-1100 = -0.125
 •
 •
 •
 1000-0011 = -3.90625
 1000-0010 = -3.9375
 1000-0001 = -3.96875
 1000-0000 = -4
 0111-1111 = 3.96875 (MAX)
 0111-1110 = 3.9375
 0111-1101 = 3.90625
 0111-1100 = 3.875
 •
 •
 •
 0011-1100 = 1.875 (Default)
 •
 •
 •
 0000-0011 = 0.09375
 0000-0010 = 0.0625
 0000-0001 = 0.03125
 0000-0000 = 0.0

Note 1: CH6 is the 7th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-70: ADDRESS 0X9D – CH7 DIGITAL GAIN (Note 1)

| | | | | | | | |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| CH7_DIG_GAIN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **CH7_DIG_GAIN<7:0>**: Digital gain setting for channel 7 (Note 2)

1111-1111 = -0.03125

1111-1110 = -0.0625

1111-1101 = -0.09375

1111-1100 = -0.125

•

•

•

1000-0011 = -3.90625

1000-0010 = -3.9375

1000-0001 = -3.96875

1000-0000 = -4

0111-1111 = 3.96875 (MAX)

0111-1110 = 3.9375

0111-1101 = 3.90625

0111-1100 = 3.875

•

•

•

0011-1100 = 1.875 (Default)

•

•

•

0000-0011 = 0.09375

0000-0010 = 0.0625

0000-0001 = 0.03125

0000-0000 = 0.0

Note 1: CH7 is the 8th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 to 5-40) for channel selection bit settings.

2: See Notes 2, 3 and 4 in Register 5-63.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-71: ADDRESS 0X9E – CH0 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH0_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH0_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 0 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-72: ADDRESS 0X9F – CH1 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH1_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH1_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 1 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-73: ADDRESS 0XA0 – CH2 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH2_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH2_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 2 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 or the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-74: ADDRESS 0XA1 – CH3 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH3_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH3_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 3 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-75: ADDRESS 0XA2 – CH4 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH4_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH4_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 4 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-76: ADDRESS 0XA3 – CH5 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH5_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH5_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 5 (Note 2)

1111-1111 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-77: ADDRESS 0XA4 – CH6 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH6_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH6_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 6 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-78: ADDRESS 0XA5 – CH7 DIGITAL OFFSET (Note 1)

| | | | | | | | |
|---------------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH7_DIG_OFFSET<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **CH7_DIG_OFFSET <7:0>**: Digital offset setting bits for channel 7 (Note 2)

1111-1111 = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

0000-0001 = 0x01 x DIG_OFFSET_WEIGHT<1:0>

0000-0000 = 0 (Default)

Note 1: See Table 4-14 for the corresponding channel.

2: Offset value is two's complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-79: ADDRESS 0xA7 – DIGITAL OFFSET WEIGHT CONTROL

| | | | | | | | |
|----------|-------|-------|------------------------|-------|----------|-------|-------|
| R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| FCB<5:3> | | | DIG_OFFSET_WEIGHT<1:0> | | FCB<2:0> | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7-5 **FCB<7:5>**: Factory-Controlled bits. This is not for the user. Do not program.
- bit 4-3 **DIG_OFFSET_WEIGHT<1:0>**: Control the weight of the digital offset settings (**Note 1**)
 11 = 2 LSB x Digital Gain
 10 = LSB x Digital Gain
 01 = LSB/2 x Digital Gain
 00 = LSB/4 x Digital Gain, (**Default**)
- bit 2-0 **FCB<2:0>**: Factory-Controlled bits. This is not for the user. Do not program.

Note 1: This bit setting is used for the digital offset setting registers in Addresses 0x9E - 0xA7 (Registers 5-71 to 5-79).

REGISTER 5-80: ADDRESS 0xC0 – CALIBRATION STATUS INDICATION

| | | | | | | | |
|----------|----------|-----|-----|-----|-----|-----|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CAL_STAT | FCB<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **CAL_STAT**: Power-Up auto-calibration status indication flag bit
 1 = Device power-up calibration is completed
 0 = Device power-up calibration is not completed
- bit 6-0 **FCB<6:0>**: Factory-Controlled bits. These bits are readable, but have no meaning for the user.

REGISTER 5-81: ADDRESS 0xD1 – PLL CALIBRATION AND STATUS INDICATION

| | | | | | | |
|----------|--------------|----------|---------------|---------------|--------|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| FCB<4:3> | PLL_CAL_STAT | FCB<2:1> | PLL_VCOL_STAT | PLL_VCOH_STAT | FCB<0> | |
| bit 7 | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7-6 **FCB<4:3>**: Factory-Controlled bits. These bits are readable, but have no meaning for the user.
- bit 5 **PLL_CAL_STAT**: PLL auto-calibration status indication flag bit (**Note 1**)
 1 = Complete: PLL auto-calibration is completed
 0 = Incomplete: PLL auto-calibration is not completed
- bit 4-3 **FCB<2:1>**: Factory-Controlled bits. These bits are readable, but have no meaning for the user.

MCP37231/21-200 AND MCP37D31/21-200

REGISTER 5-81: ADDRESS 0XD1 – PLL CALIBRATION AND STATUS INDICATION (CONTINUED)

- bit 2 **PLL_VCOL_STAT:** PLL drift status indication bit
 1 = PLL drifts out of lock with low VCO frequency
 0 = PLL operates as normal
- bit 1 **PLL_VCOH_STAT:** PLL drift status indication bit
 1 = PLL drifts out of lock with high VCO frequency
 0 = PLL operates as normal
- bit 0 **FCB<0>:** Factory-Controlled bits. This bit is readable, but have no meaning for the user.
- Note 1:** See PLL_CALTRIG bit setting in Address 0x6B ([Register 5-27](#)).

REGISTER 5-82: ADDRESS 0X15C – CHIP ID (LOWER BYTE)([Note 1](#))

| | | | | | | | |
|--------------|-----|-----|-----|-----|-----|-----|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| CHIP_ID<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 7-0 **CHIP_ID<7:0>:** Chip ID of the device: Lower byte of the CHIP ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.

Example: MCP37231-200: '0000 1000 0111 0000'

 MCP37221-200: '0000 1000 0101 0000'

 MCP37D31-200: '0000 1010 0111 0000'

 MCP37D21-200: '0000 1010 0101 0000'

REGISTER 5-83: ADDRESS 0X15D – CHIP ID (UPPER BYTE)([Note 1](#))

| | | | | | | | |
|---------------|-----|-----|-----|-----|-----|-----|-------|
| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| CHIP_ID<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|--|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

bit 7-0 **CHIP_ID<15:8>:** Chip ID of the device: Lower byte of the CHIP ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.

Example: MCP37231-200: '0000 1000 0111 0000'

 MCP37221-200: '0000 1000 0101 0000'

 MCP37D31-200: '0000 1010 0111 0000'

 MCP37D21-200: '0000 1010 0101 0000'

MCP37231/21-200 AND MCP37D31/21-200

6.0 DEVELOPMENT SUPPORT

Microchip offers a high speed ADC evaluation platform which can be used to evaluate Microchip's high speed ADC products. The platform consists of an MCP37XXX evaluation board, an FPGA-based data capture card board, and a PC-based Graphical User Interface (GUI) software. Figure 6-1 and Figure 6-2 show this evalua-

tion tool. This evaluation platform allows users to quickly evaluate the ADC's performance for their specific application requirements. More information is available at

<http://www.microchip.com>.

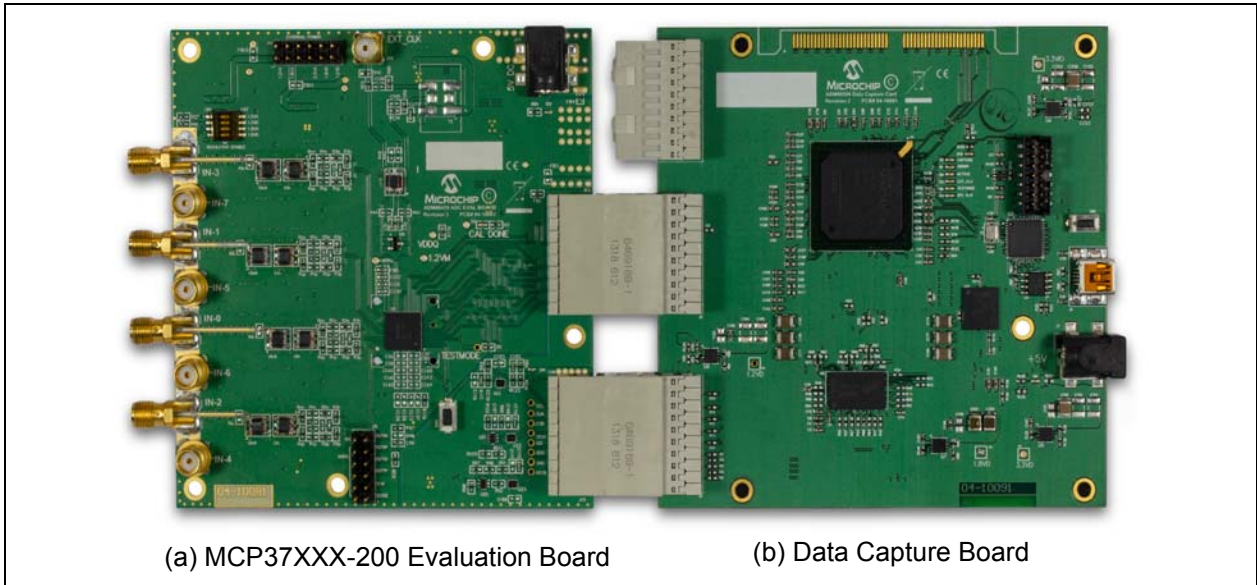


FIGURE 6-1: MCP37XXX Evaluation Kit.

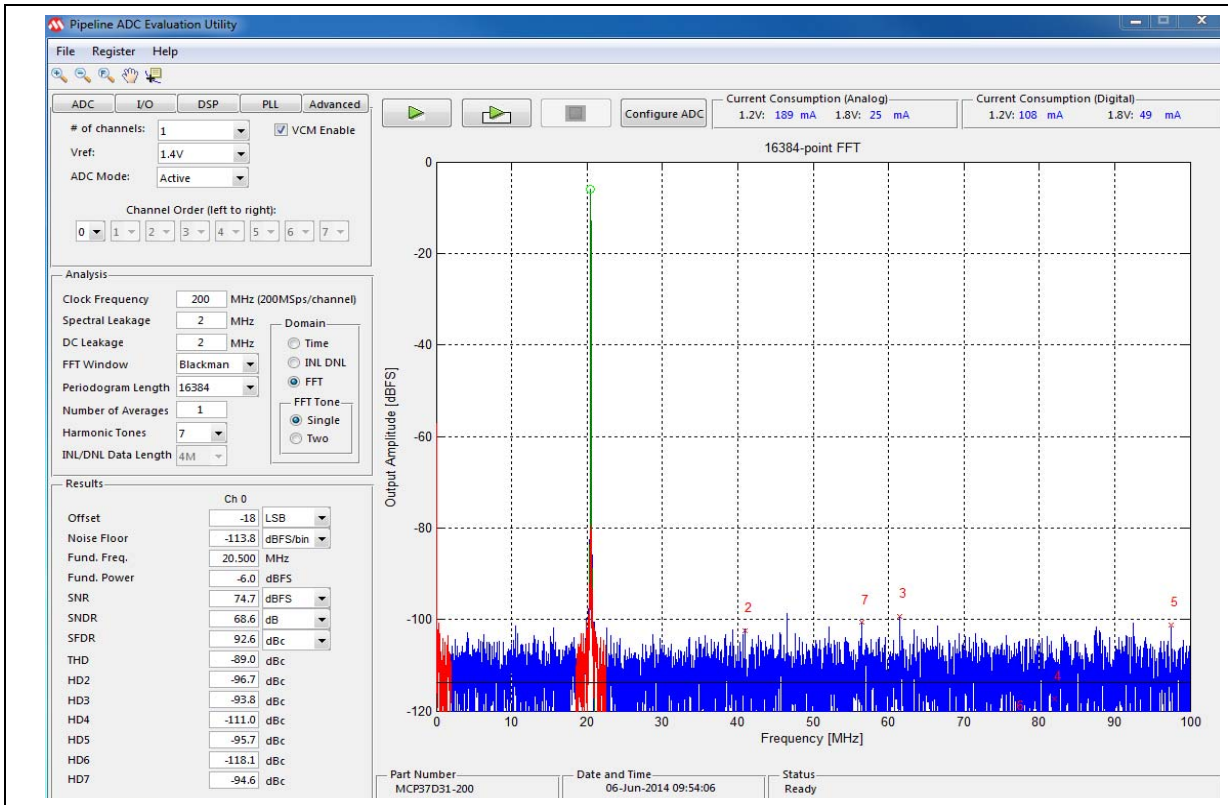


FIGURE 6-2: PC-based Graphical User Interface Software

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

7.0 TERMINOLOGY

Analog Input Bandwidth (Full Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay or Sampling Delay

This is the time delay between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty

The sample-to-sample variation in aperture delay.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal-to-noise ratio due to the jitter alone will be:

EQUATION 7-1:

$$SNR_{JITTER} = -20\log(2\pi \times f_{IN} \times t_{JITTER})$$

Calibration Algorithms

This device utilizes two patented analog and digital calibration algorithms, Harmonic Distortion Correction (HDC) and DAC Noise Cancellation (DNC), to improve the ADC performance. The algorithms compensate various sources of linear impairments such as capacitance mismatch, charge injection error, and finite gain of operational amplifiers. These algorithms execute in both power-up sequence (foreground) and background mode:

- Power-Up Calibration: The calibration is conducted within the first 2^{27} clock cycles after power-up. The user needs to wait this Power-Up Calibration period, after the device is powered-up, for an accurate ADC performance.
- Background Calibration: This calibration is conducted in background while the ADC is performing conversions. The update rate is about every 2^{30} clock cycles.

Channel Crosstalk

This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest in the multi-channel mode. It is measured by applying a full-scale input signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as

measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

Pipeline Delay (LATENCY)

LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available after the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

Clock Pulse Width and Duty Cycle

The clock duty cycle is the ratio of the time the clock signal remains at a logic high (clock pulse width) to one clock period. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. No missing codes to 16-bit resolution indicates that all 65,536 codes must be present over all operating conditions.

Integral Nonlinearity (INL)

INL is the maximum deviation of each individual code from an ideal straight line drawn from negative full scale through positive full scale.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), below the Nyquist frequency and excluding the power at DC and the first nine harmonics.

EQUATION 7-2:

$$SNR = 10\log\left(\frac{P_S}{P_N}\right)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D) below the Nyquist frequency, but excluding DC:

MCP37231/21-200 AND MCP37D31/21-200

EQUATION 7-3:

$$SINAD = 10\log\left(\frac{P_S}{P_D + P_N}\right)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

EQUATION 7-4:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Gain error is usually expressed in LSB or as a percentage of full-scale range (%FSR).

Gain-Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

Offset Error

The major carry transition should occur for an analog value of $\frac{1}{2}$ LSB below $A_{IN+} = A_{IN-}$. Offset error is defined as the deviation of the actual transition from that point.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (+25°C) value to the value at across the T_{MIN} to T_{MAX} range.

Maximum Conversion Rate

The maximum clock rate at which parametric testing is performed.

Minimum Conversion Rate

The minimum clock rate at which parametric testing is performed.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier) or dBFS.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the summed power of the first 13 harmonics (P_D).

EQUATION 7-5:

$$THD = 10\log\left(\frac{P_S}{P_D}\right)$$

THD is typically given in units of dBc (dB to carrier). THD is also shown by:

EQUATION 7-6:

$$THD = -20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_1}$$

Where:

V_1 = RMS amplitude of the fundamental frequency

V_1 through V_n = Amplitudes of the second through nth harmonics

Two-Tone Intermodulation Distortion (Two-Tone IMD, IMD3)

Two-Tone IMD is the ratio of the power of the fundamental (at frequencies f_{IN1} and f_{IN2}) to the power of the worst spectral component at either frequency $2f_{IN1} - f_{IN2}$ or $2f_{IN2} - f_{IN1}$. Two-Tone IMD is a function of the input amplitudes and frequencies (f_{IN1} and f_{IN2}). It is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the ADC full-scale range.

Power-Supply Rejection Ratio (PSRR)

Measured as the ratio of the change in the power-supply voltage to the change in the ADC output.

•AC PSRR:

EQUATION 7-7:

$$PSRR_{AC} = 20\log\left(\frac{\Delta V_{DD}}{\Delta V_{OUT}}\right)$$

The AC PSRR is typically given in units of dBc.

MCP37231/21-200 AND MCP37D31/21-200

•DC PSRR:

The DC PSRR is typically given in units of mV/V or dB.

EQUATION 7-8:

$$PSRR_{DC} = 20\log\left(\frac{\Delta V_{DD}}{\Delta V_{OFFSET}}\right)$$

Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both sides of a differential input pair. The common-mode signal can be an AC or DC signal, or a combination of the two. CMRR is measured using the ratio of the differential signal gain to the common-mode signal gain and expressed in dB with the following equation:

EQUATION 7-9:

$$CMRR = 20\log\left(\frac{A_{DIFF}}{A_{CM}}\right)$$

Where:

$A_{DIFF} = \Delta\text{Output Code}/\Delta\text{Differential Voltage}$

$A_{DIFF} = \Delta\text{Output Code}/\Delta\text{Common Mode Voltage}$

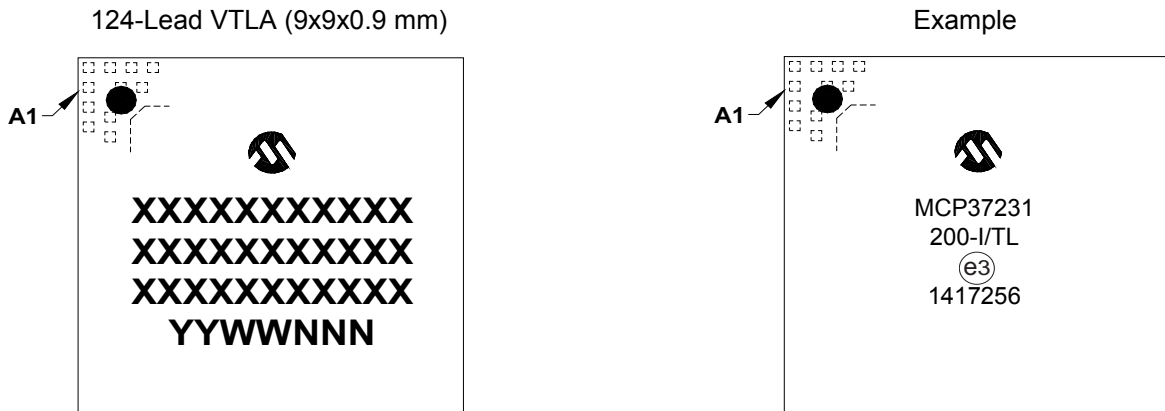
MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

8.0 PACKAGING INFORMATION

8.1 Package Marking Information



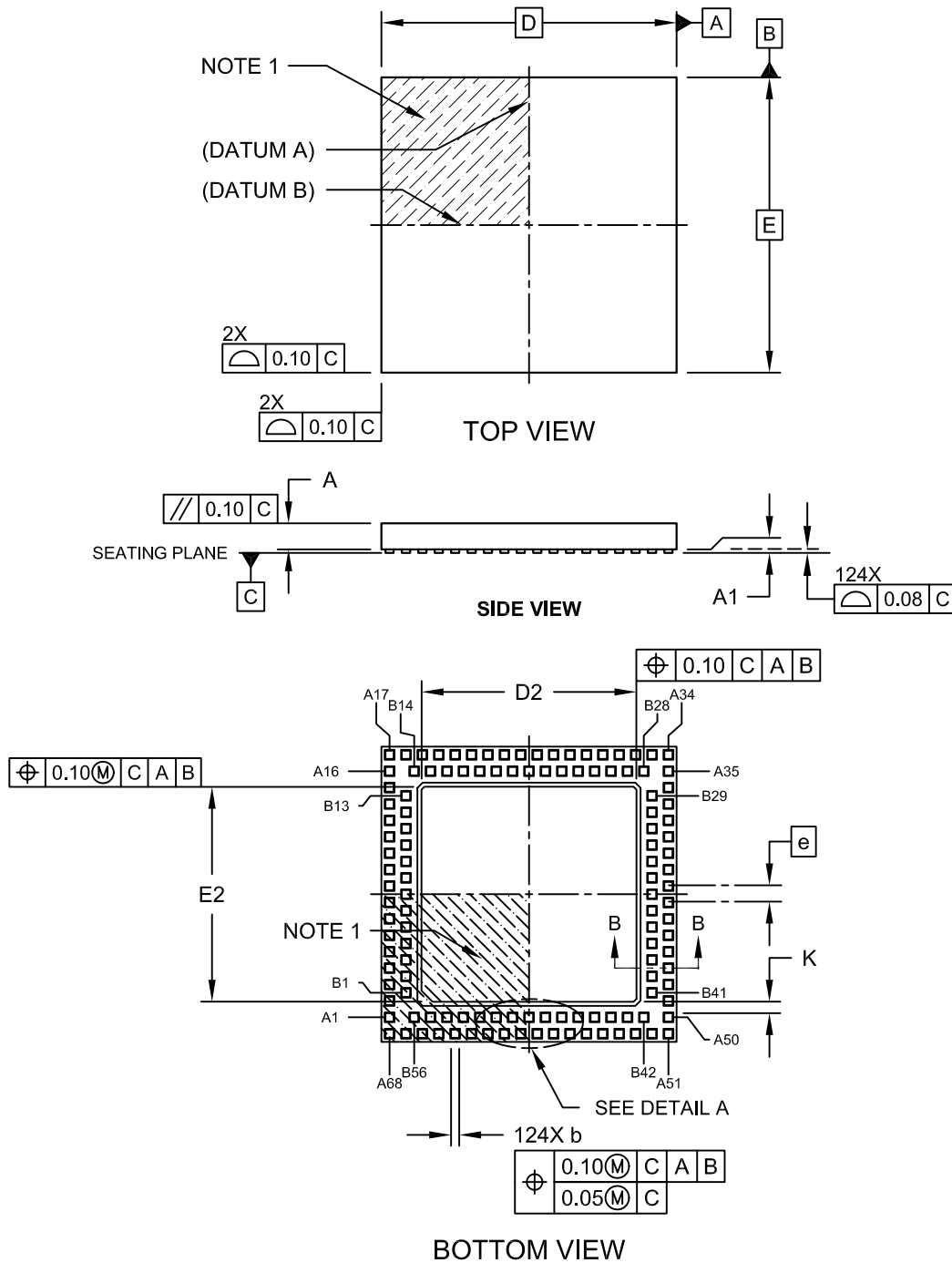
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC [®] designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP37231/21-200 AND MCP37D31/21-200

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

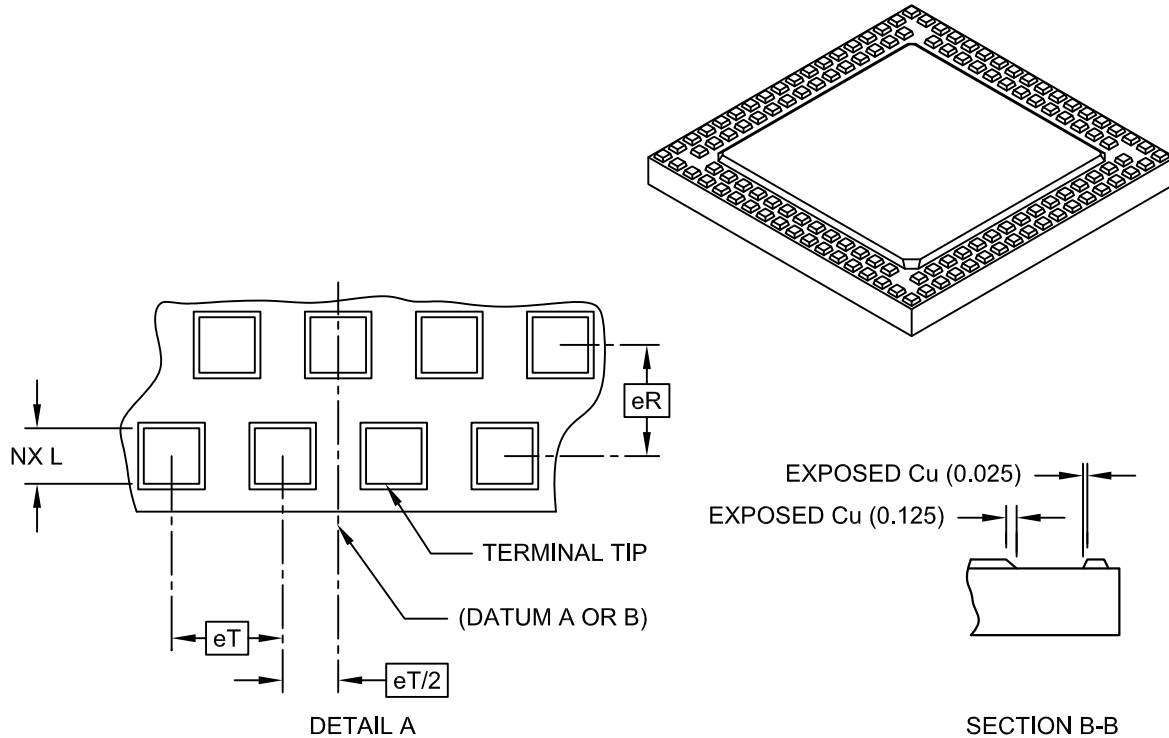


Microchip Technology Drawing C04-193A Sheet 1 of 2

MCP37231/21-200 AND MCP37D31/21-200

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 124 | | |
| Pitch | eT | 0.50 BSC | | |
| Pitch (Inner to outer terminal ring) | eR | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | - | 0.05 |
| Overall Width | E | 9.00 BSC | | |
| Exposed Pad Width | E2 | 6.40 | 6.55 | 6.70 |
| Overall Length | D | 9.00 BSC | | |
| Exposed Pad Length | D2 | 6.40 | 6.55 | 6.70 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

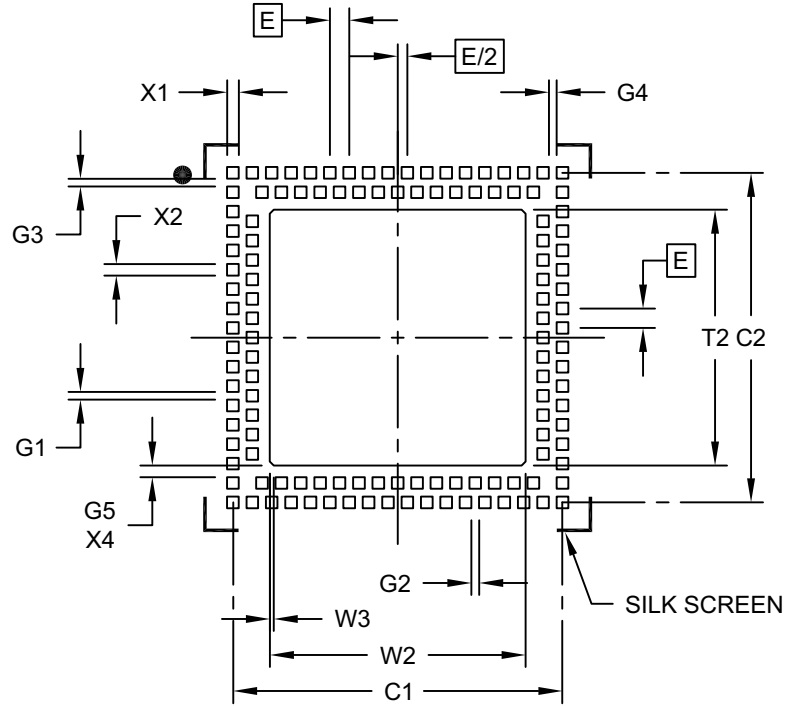
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

MCP37231/21-200 AND MCP37D31/21-200

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Pad Clearance | G1 | 0.20 | | |
| Pad Clearance | G2 | 0.20 | | |
| Pad Clearance | G3 | 0.20 | | |
| Pad Clearance | G4 | 0.20 | | |
| Contact to Center Pad Clearance (X4) | G5 | 0.30 | | |
| Optional Center Pad Width | T2 | | | 6.60 |
| Optional Center Pad Length | W2 | | | 6.60 |
| Optional Center Pad Chamfer (X4) | W3 | | 0.10 | |
| Contact Pad Spacing | C1 | | 8.50 | |
| Contact Pad Spacing | C2 | | 8.50 | |
| Contact Pad Width (X124) | X1 | | | 0.30 |
| Contact Pad Length (X124) | X2 | | | 0.30 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

MCP37231/21-200 AND MCP37D31/21-200

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>IXI⁽¹⁾</u> | <u>-XXX</u> | <u>X</u> | <u>/XX</u> | Examples: |
|--|-----------------------------|--------------------|--------------------------|----------------|--|
| Device | Tape and Reel Option | Sample Rate | Temperature Range | Package | |
| <p>Device:</p> <p>MCP37231-200: 16-Bit Low-Power ADC with 8-Channel MUX MCP37D31-200: 16-Bit Low-Power ADC with 8-Channel MUX, Digital Down-Converter and CW Beamforming MCP37221-200*: 14-Bit Low-Power ADC with 8-Channel MUX MCP37D21-200*: 14-Bit Low-Power ADC with 8-Channel MUX, Digital Down-Converter and CW Beamforming</p> <p>* Contact Microchip Technology Inc. for availability.</p> | | | | | <p>a) MCP37231-200/TE: 124LD VTLA, 200 Msps b) MCP37231-200/TL: 121LD TFBGA, 200 Msps c) MCP37231T-200/TL: Tape and Reel, Industrial temperature, 124LD VTLA, 200 Msps</p> |
| <p>Tape and Reel Option:</p> <p>Blank = Standard packaging (tube or tray) T = Tape and Reel⁽¹⁾</p> | | | | | |
| <p>Sample Rate:</p> <p>200 = 200 Msps</p> | | | | | |
| <p>Temperature Range:</p> <p>I = -40°C to +85°C (Industrial)</p> | | | | | |
| <p>Package:</p> <p>TL = Terminal Very Thin Leadless Array Package - 9x9x0.9 mm Body (VTLA), 124-Lead TE = Ball Plastic Thin Profile Fine Pitch Ball Grid Array - 8x8x1.1.00 mm Body (TFBGA), 121-Lead</p> | | | | | <p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p> |

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

MCP37231/21-200 AND MCP37D31/21-200

APPENDIX A: REVISION HISTORY

Revision A (July 2014)

- Original Release of this Document.

MCP37231/21-200 AND MCP37D31/21-200

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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ISBN: 978-1-63276-420-1

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[MCP37221-200I/TL](#)

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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