

Ultra Small, Highly Accurate, Single Voltage Detector

■ GENERAL DESCRIPTION

The XC6126 series is an ultra small, highly accurate CMOS single voltage detector with very low power consumption. The device includes a highly accurate reference voltage source and uses laser trimming technologies, it maintains high accuracy over the full operation temperature range.

The device is available in both CMOS and N-channel open drain output configurations.

Ultra small package USPN-4B02 is ideally suited for small design of portable devices and high density mounting applications. The conventional package SSOT-24 is also available for upper compatible replacements.

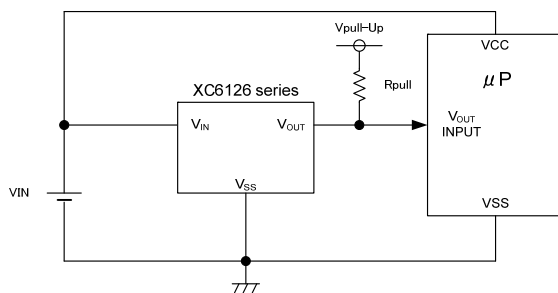
■ APPLICATIONS

- Microprocessor logic reset circuitry
- System battery life and charge voltage monitors
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection

■ FEATURES

High Accuracy	: $\pm 0.8\%$ (25°C)
Temperature Characteristics	: $\pm 50\text{ppm}/^\circ\text{C}$ (TYP.)
Low Power Consumption	: $0.6\ \mu\text{A}$ (TYP.) (Detect: $V_{\text{DF}}=1.8\text{V}$, $V_{\text{IN}}=1.62\text{V}$) $0.7\ \mu\text{A}$ (TYP.) (Release: $V_{\text{DF}}=1.8\text{V}$, $V_{\text{IN}}=1.98\text{V}$)
Operating Voltage Range	: $0.7\text{V}\sim 6.0\text{V}$
Detect Voltage Range	: $1.5\text{V}\sim 5.5\text{V}$ (0.1V increments)
Output Configuration	: N-channel open drain output CMOS output
Detect Logic	: Active Low Reset
Packages	: USPN-4B02, SSOT-24
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■ TYPICAL APPLICATION CIRCUIT



■ TYPICAL PERFORMANCE CHARACTERISTICS

- Detect Voltage vs. Ambient Temperature



PIN CONFIGURATION



PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
USPN-4B02	SSOT-24		
1	4	V _{IN}	Power Input
2	3	V _{OUT}	Signal Output (Active Low)
3	1	NC	No connection
4	2	V _{SS}	Ground

PRODUCT CLASSIFICATION

Ordering Information

XC6126①②③④⑤⑥-⑦^(*)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS Output
		N	N-ch Open Drain Output
②③	Detect Voltage	15~55	e.g. 2.7V → ②=2, ③=7
④	Detect Accuracy	A	±0.8%
⑤⑥-⑦ ^(*)	Packages (Order Unit)	7R-G	USPN-4B02 (5,000/Reel)
		NR-G	SSOT-24 (3,000/Reel)

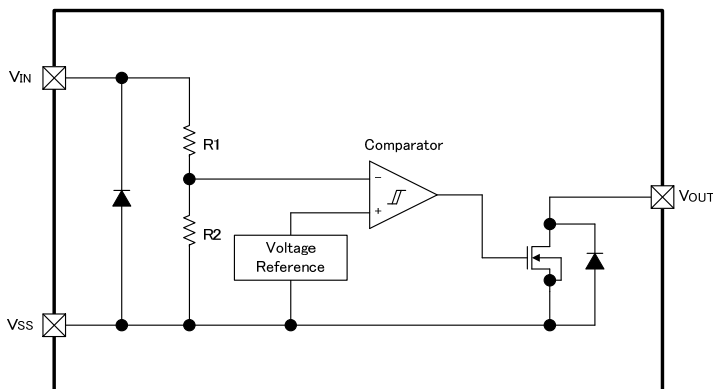
^(*) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■ BLOCK DIAGRAMS



XC6126C Series

* Diodes inside the circuits are ESD protection diodes and parasitic diodes.



XC6126N Series

* Diodes inside the circuits are ESD protection diodes.

■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	RATING	UNITS
Input Voltage	V _{IN}	V _{SS} -0.3~+6.5	V
Output Current	I _{OUT}	20	mA
Output Voltage	XC6126C ^(*1)	V _{SS} -0.3~V _{IN} +0.3 ≤ 6.5	V
	XC6126N ^(*2)		
Power Dissipation	USPN-4B02	100	mW
	SSOT-24	150	
Operating Temperature Range	T _{opr}	-40~+85	°C
Storage Temperature Range	T _{stg}	-55~+125	°C

Note:

(*1) CMOS Output

(*2) N-ch Open Drain Output

ELECTRICAL CHARACTERISTICS

XC6126 Series

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Operating Voltage	V _{IN}	V _{DF(T)} ^{(*)1} =1.5~5.5V ^{(*)2}	0.7 ^{(*)3}		6.0	V	-
Detect Voltage	V _{DFL}	V _{DF(T)} =1.5~5.5V	V _{DF(T)} ×0.992	V _{DF(T)}	V _{DF(T)} ×1.008	V	①
			E-1 ^{(*)4}				
Hysteresis Width	V _{HYS}		V _{DFL} ×0.02	V _{DFL} ×0.05	V _{DFL} ×0.08	V	①
Supply Current 1	I _{SS1}	V _{IN} =V _{DFL} ×0.9	-	0.6	1.3	μA	②
		V _{DF(T)} =1.5~1.8V	-	0.7	1.5		
		V _{DF(T)} =1.9~3.0V	-	0.9	1.85		
Supply Current 2	I _{SS2}	V _{IN} =V _{DFL} ×1.1 ^{(*)5}	-	0.7	1.55	μA	②
		V _{DF(T)} =1.5~1.8V	-	0.8	1.75		
		V _{DF(T)} =1.9~3.0V	-	1.0	2.25		
Output Current	I _{OUT1}	V _{IN} =0.7V, V _{OUT} =0.5V(N-ch)	0.008	0.2	-	mA	③
		V _{IN} =1.0V, V _{OUT} =0.5V(N-ch)	0.6	1.5	-		
		V _{IN} =2.0V ^{(*)6} , V _{OUT} =0.5V(N-ch)	4.5	7.0	-		
		V _{IN} =3.0V ^{(*)7} , V _{OUT} =0.5V(N-ch)	7.0	10.0	-		
		V _{IN} =4.0V ^{(*)8} , V _{OUT} =0.5V(N-ch)	8.5	11.5	-		
	V _{IN} =5.0V ^{(*)9} , V _{OUT} =0.5V(N-ch)	9.5	13.0	-			
	I _{OUT2} ^{(*)10}	V _{IN} =6.0V, V _{OUT} =5.5V(P-ch)	-	-4.6	-2.8	mA	③
Leakage Current	CMOS Output	I _{LEAK}	V _{IN} =V _{DFL} ×0.9, V _{OUT} =0V	-	-0.01	μA	③
	N-ch Open Drain Output						
Temperature Characteristics	ΔV _{DFL} / (ΔT _{opr} ·V _{DFL})	-40°C ≤ T _{opr} ≤ 85°C	-	±50	-	ppm/°C	①
Detect Delay Time ^{(*)11}	t _{DF}	V _{IN} =V _{DFL} ×1.1 ^{(*)5} →V _{DFL} ×0.9	-	30	100	μs	④
Release Delay Time ^{(*)12}	t _{DR}	V _{IN} =V _{DFL} ×0.9→V _{DFL} ×1.1 ^{(*)5}	-	20	50	μs	④

Note:

(*)1 V_{DF(T)}: Nominal detect voltage

(*)2 For the N-ch Open Drain, R_{pull}=1MΩ, V_{pull-Up}=V_{IN}.

R_{pull} : An External Pull-up resistor

V_{pull-Up} : Pull-up Voltage

(*)3 V_{IN} voltage for V_{OUT} ≤ 0.3V is under detect state.

(*)4 For the detail value, please refer to "Voltage Table" in next page.

(*)5 V_{IN}=6.0V where V_{DF(T)}=5.5V.

(*)6 For V_{DF(T)}>2.0V products.

(*)7 For V_{DF(T)}>3.0V products.

(*)8 For V_{DF(T)}>4.0V products.

(*)9 For V_{DF(T)}>5.0V products.

(*)10 For the XC6126C (CMOS output)

(*)11 A time between V_{IN}=V_{DFL} and V_{OUT}=V_{DFL}×0.45 when V_{IN} falls.

(*)12 A time between V_{IN}=V_{DFL}+V_{HYS} and V_{OUT}=V_{DFL}×0.55 when V_{IN} rises.

■ ELECTRICAL CHARACTERISTICS (Continued)

Voltage Table 1

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
	V _{DFL}	
V _{DF(T)}	MIN.	MAX.
1.50	1.4880	1.5120
1.60	1.5872	1.6128
1.70	1.6864	1.7136
1.80	1.7856	1.8144
1.90	1.8848	1.9152
2.00	1.9840	2.0160
2.10	2.0832	2.1168
2.20	2.1824	2.2176
2.30	2.2816	2.3184
2.40	2.3808	2.4192
2.50	2.4800	2.5200
2.60	2.5792	2.6208
2.70	2.6784	2.7216
2.80	2.7776	2.8224
2.90	2.8768	2.9232
3.00	2.9760	3.0240
3.10	3.0752	3.1248
3.20	3.1744	3.2256
3.30	3.2736	3.3264
3.40	3.3728	3.4272
3.50	3.4720	3.5280
3.60	3.5712	3.6288
3.70	3.6704	3.7296
3.80	3.7696	3.8304
3.90	3.8688	3.9312
4.00	3.9680	4.0320

Voltage Table 2

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
	V _{DFL}	
V _{DF(T)}	MIN.	MAX.
4.10	4.0672	4.1328
4.20	4.1664	4.2336
4.30	4.2656	4.3344
4.40	4.3648	4.4352
4.50	4.4640	4.5360
4.60	4.5632	4.6368
4.70	4.6624	4.7376
4.80	4.7616	4.8384
4.90	4.8608	4.9392
5.00	4.9600	5.0400
5.10	5.0592	5.1408
5.20	5.1584	5.2416
5.30	5.2576	5.3424
5.40	5.3568	5.4432
5.50	5.4560	5.5440

OPERATIONAL EXPLANATION

Typical Application Circuit



Timing Chart



The above uses a timing chart to explain the operation of the circuit indicated in the operation explanation circuit schematic.

- (1) In the initial state, an input voltage (V_{IN}) higher than the release voltage (V_{DR}) is applied, and V_{IN} gradually drops.
When a voltage higher than the detect voltage (V_{DFL}) is applied to the input voltage (V_{IN}), the output voltage (V_{OUT}) is equal to the input voltage (V_{IN}).
*On the N-ch open drain output product, the VOUT pin is in a high impedance state, and when the output is pulled up, the output voltage (V_{OUT}) is equal to the pull-up voltage.
- (2) When the input voltage (V_{IN}) drops below the detect voltage (V_{DFL}), the output voltage (V_{OUT}) is equal to the ground voltage (V_{SS}). (Detection state)
*This also applies to the N-ch open drain output product.
- (3) If the input voltage (V_{IN}) drops below the minimum operating voltage (0.7V), the output becomes unstable.
*If the output pin on the N-ch open drain output product is pulled up, the pull-up voltage may be output as the output voltage (V_{OUT}).
- (4) The output voltage (V_{OUT}) remains at the ground voltage as the input voltage (V_{IN}) rises past the minimum operating voltage (0.7V) and reaches the release voltage (V_{DR}).
- (5) If the input voltage (V_{IN}) rises higher than the release voltage (V_{DR}), the output voltage (V_{OUT}) is equal to the input voltage (V_{IN}).
*On the N-ch open drain output product, the VOUT pin is in a high impedance state, and if the output is pulled up, the pull-up voltage is output as the output voltage (V_{OUT}) as in (1).
- (6) The difference between the release voltage (V_{DR}) and the detect voltage (V_{DFL}) is the hysteresis width (V_{HYS}).

Note: For simplicity, the above explanation omits the circuit operation time.

NOTE ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. Note that there is a possibility of malfunctioning if the input voltage changes sharply or undergoes repeated, cyclical changes.
3. If the resistance R_{IN} is connected between the V_{IN} pin and the power supply V_{DD} , the voltage drop due to the flow through current in the internal circuit and R_{IN} may cause oscillation when release takes place. When using the CMOS output product, oscillation due to R_{IN} and the flow through current may occur without relation to release and detection, and thus R_{IN} should not be connected.
4. Please use N-ch open drains configuration, when a resistor R_{IN} is connected between the V_{IN} pin and the power supply V_{DD} . In such cases, please ensure that R_{IN} is less than $33k\Omega$.



[Figure 1: Circuit connected with the input resistor fro N-ch open drain]

5. When N-ch open drain output is used, the V_{OUT} voltage at detection is determined by the pull-up resistance connected to the output pin. Select the resistance based on the following considerations:

$$\text{At detection: } V_{OUT} = (V_{pull-Up}) / (1 + R_{pull} / R_{ON})$$

$V_{pull-Up}$: Voltage after pull-up

$R_{ON}(*1)$: ON resistance of N-ch driver (calculated from V_{OUT}/I_{OUT1} based on electrical characteristics) (*3)

Example:

When $V_{IN} = 2.0V$ (*2), $R_{ON} = 0.5/4.5 \times 10^{-3} \cong 111 \Omega$ (MAX.) . If it is desired to make the V_{OUT} voltage at detection 0.1V or less when $V_{pull-Up}$ is 3.0 V,

$$R_{pull} = (V_{pull-Up} / V_{OUT-1}) \times R_{ON} = (3/0.1-1) \times 111 \cong 3.2k\Omega$$

Therefore, to make the output voltage at detection 0.1 V or less under the above conditions, the pull-up resistance must be $3.2k\Omega$ or higher.

(*1) Note that R_{ON} becomes larger as V_{IN} becomes smaller.

(*2) For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

(*3) I_{OUT1} in the electrical characteristics is at $T_a = 25^\circ C$. I_{OUT1} varies depending on the ambient temperature.

To select a pull-up resistance taking ambient temperature into account, consult us.

$$\text{At release: } V_{OUT} = (V_{pull-Up}) / (1 + R_{pull} / R_{OFF})$$

$V_{pull-Up}$: Voltage after pull-up

R_{OFF} : $40M\Omega$ (MIN.) resistance when N-ch driver is OFF (calculated from V_{OUT}/I_{LEAK} based on electrical characteristics)

Example:

Making V_{OUT} 5.99 V or higher when $V_{pull-Up}$ is 6.0 V:

$$R_{pull} = (V_{pull-Up} / V_{OUT-1}) \times R_{OFF} = (6/5.99-1) \times 40 \times 10^6 \cong 66k\Omega$$

Therefore, to make the output voltage at release 5.99 V or higher under the above conditions, the pull-up resistance must be $66k\Omega$ or less.

6. Torex places an importance on improving our products and its reliability.

However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

TEST CIRCUITS

Circuit 1



Circuit 2



Circuit 3

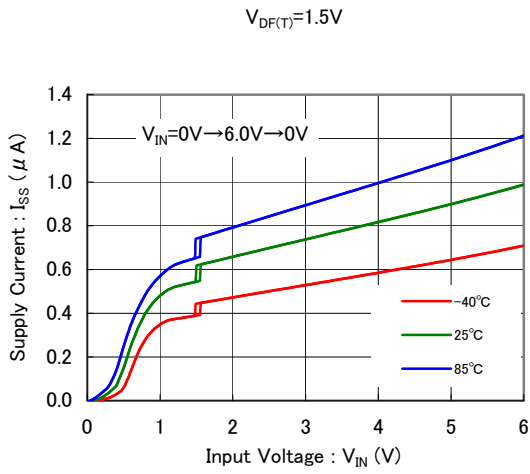


Circuit 4



TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Input Voltage



(2) Supply Current vs. Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Output Voltage vs. Input Voltage1



(4) Detect Voltage, Release Voltage

vs. Ambient Temperature



■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Output Voltage vs. Input Voltage²($V_{IN} \leq 1.4V$)



(6) Output Current (Nch Driver) vs. Input Voltage



(7) Output Current (Pch Driver) vs. Input Voltage



(8) Detect Delay Time vs. Ambient Temperature



(9) Release Delay Time vs. Ambient Temperature



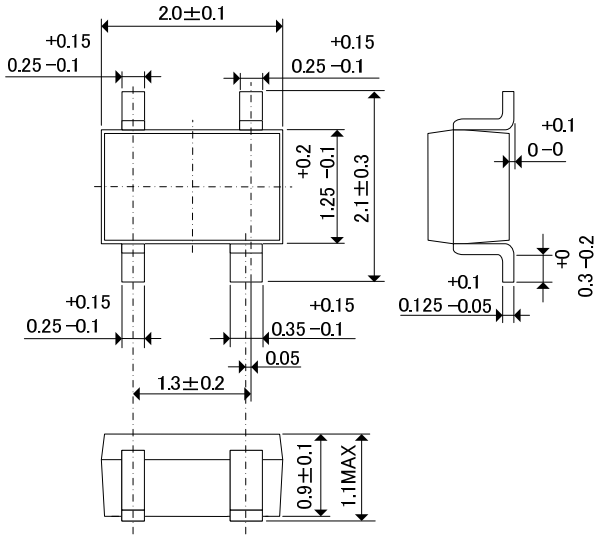
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(10) Leakage Current vs. Ambient temperature

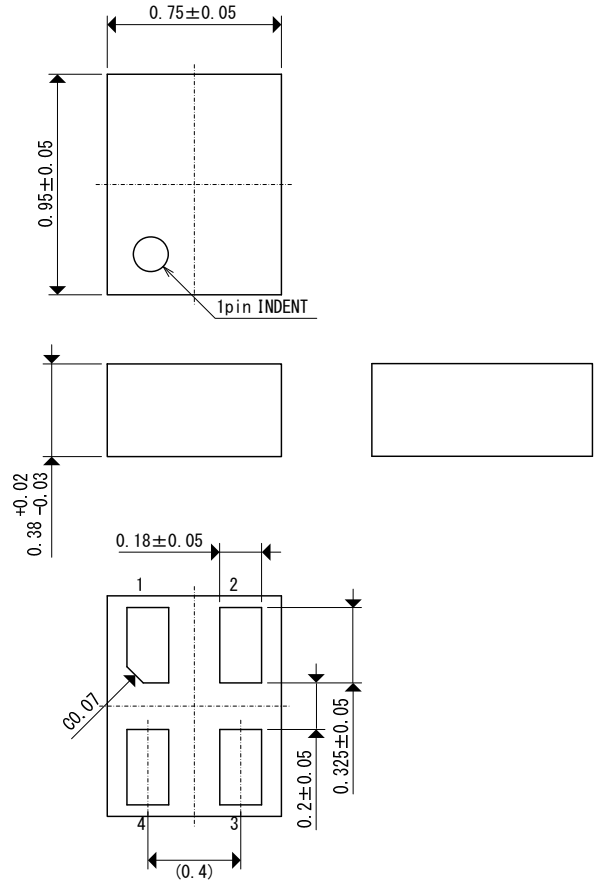


PACKAGING INFORMATION

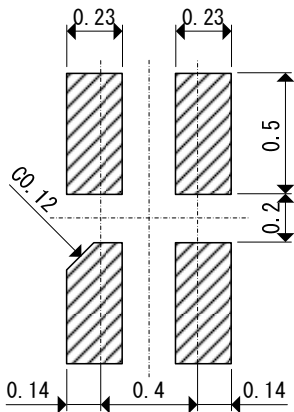
●SSOT-24 (unit: mm)



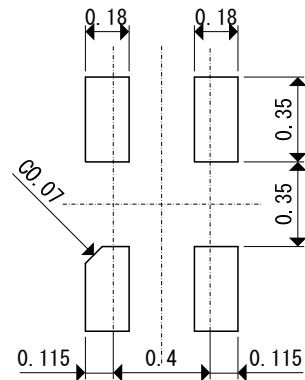
●USPN-4B02 (unit: mm)



●USPN-4B02 Reference Pattern Layout (unit : mm)



●USPN-4B02 Reference Metal Mask Design (unit : mm)



MARKING RULE

SSOT-24 (With the orientation bar at the top)



① represents product series, detect voltage range and output configuration.

MARK	OUTPUT CONFIGURATION	DETECT VOLTAGE RANGE[V]	PRODUCT SERIES
1	CMOS	1.5~2.5	XC6126C15A**-G ~ XC6126C25A**-G
2	CMOS	2.6~5.5	XC6126C26A**-G ~ XC6126C55A**-G
3	Nch	1.5~2.5	XC6126N15A**-G ~ XC6126N25A**-G
4	Nch	2.6~5.5	XC6126N26A**-G ~ XC6126N55A**-G

② represents detect voltage.

MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)	
0	-	2.6	A	-	3.6	N	1.6	4.6
1	-	2.7	B	-	3.7	P	1.7	4.7
2	-	2.8	C	-	3.8	R	1.8	4.8
3	-	2.9	D	-	3.9	S	1.9	4.9
4	-	3.0	E	-	4.0	T	2.0	5.0
5	-	3.1	F	-	4.1	U	2.1	5.1
6	-	3.2	H	-	4.2	V	2.2	5.2
7	-	3.3	K	-	4.3	X	2.3	5.3
8	-	3.4	L	-	4.4	Y	2.4	5.4
9	-	3.5	M	1.5	4.5	Z	2.5	5.5

③④ represents production lot number

01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to AZ, B1 to ZZ repeated

(G, I, J, O, Q, W excluded)

*No character inversion used.

MARKING RULE (Continued)

USPN-4B02



① represents product series, detect voltage range and output configuration.

MARK	OUTPUT CONFIGURATION	DETECT VOLTAGE RANGE[V]	PRODUCT SERIES
4	CMOS	1.5~2.5	XC6126C15A**-G ~ XC6126C25A**-G
5	CMOS	2.6~5.5	XC6126C26A**-G ~ XC6126C55A**-G
6	Nch	1.5~2.5	XC6126N15A**-G ~ XC6126N25A**-G
7	Nch	2.6~5.5	XC6126N26A**-G ~ XC6126N55A**-G

② represents detect voltage.

MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)		MARK	DETECT VOLTAGE (V)	
0	-	2.6	A	-	3.6	N	1.6	4.6
1	-	2.7	B	-	3.7	P	1.7	4.7
2	-	2.8	C	-	3.8	R	1.8	4.8
3	-	2.9	D	-	3.9	S	1.9	4.9
4	-	3.0	E	-	4.0	T	2.0	5.0
5	-	3.1	F	-	4.1	U	2.1	5.1
6	-	3.2	H	-	4.2	V	2.2	5.2
7	-	3.3	K	-	4.3	X	2.3	5.3
8	-	3.4	L	-	4.4	Y	2.4	5.4
9	-	3.5	M	1.5	4.5	Z	2.5	5.5

③ represents production lot number

0 to 9, A to Z repeated. (G, I, J, O, Q, W excluded)

*No character inversion used.

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