

1. General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series DN" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with very sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

3. Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

4. Quick reference data

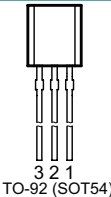

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Values | Unit |
|--------------------------------|-------------------------------------|---|--------|------|
| Absolute maximum rating | | | | |
| V_{DRM} | repetitive peak off-state voltage | | 1000 | V |
| $I_{T(RMS)}$ | RMS on-state current | square-wave pulse; $T_{lead} \leq 57\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | 0.8 | A |
| I_{TSM} | non-repetitive peak forward current | full sine wave; $t_p = 20\text{ ms}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4 ; Fig. 5 | 9 | A |
| | | full sine wave; $t_p = 16.7\text{ ms}$; $T_{j(init)} = 25\text{ °C}$ | 9.9 | A |
| T_j | junction temperature | | 125 | °C |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|---|------|-----|-----|------|
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 0.1 A; T2+ G+ T _j = 25 °C; Fig. 7 | 0.25 | - | 5 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2+ G- T _j = 25 °C; Fig. 7 | 0.25 | - | 5 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2- G- T _j = 25 °C; Fig. 7 | 0.25 | - | 5 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 9 | - | - | 10 | mA |
| V _T | on-state voltage | I _T = 0.85 A; T _j = 25 °C; Fig. 10 | - | 1.3 | 1.6 | V |
| Dynamic characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V _{DM} = 670 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit | - | 150 | - | V/μs |
| dI _{com} /dt | rate of change of commutating current | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 0.8 A; dV _{com} /dt = 10 V/μs; gate open circuit; | 0.5 | - | - | A/ms |
| | | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 0.8 A; dV _{com} /dt = 1 V/μs; gate open circuit | 1 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|--|---|
| 1 | T2 | main terminal 2 |  <p>TO-92 (SOT54)</p> |  <p>sym051</p> |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|----------------|---------|---|---------|
| | Name | Description | Version |
| BTA2008-1000DN | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

7. Marking

Table 4. Marking codes

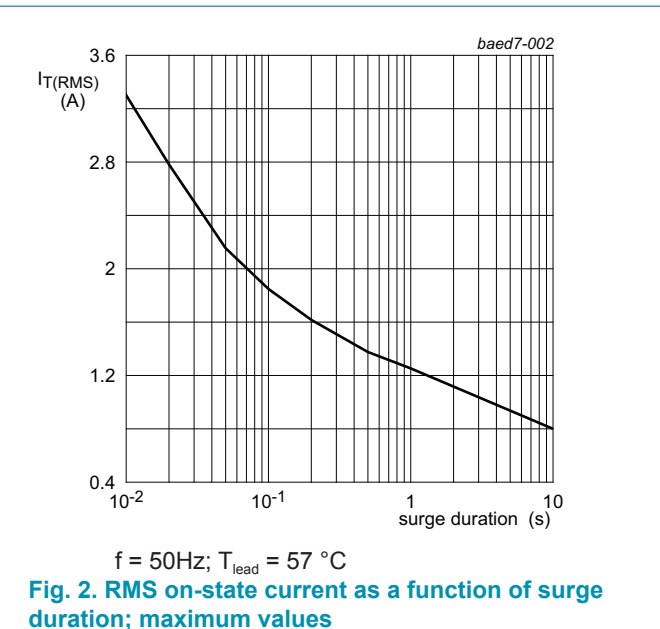
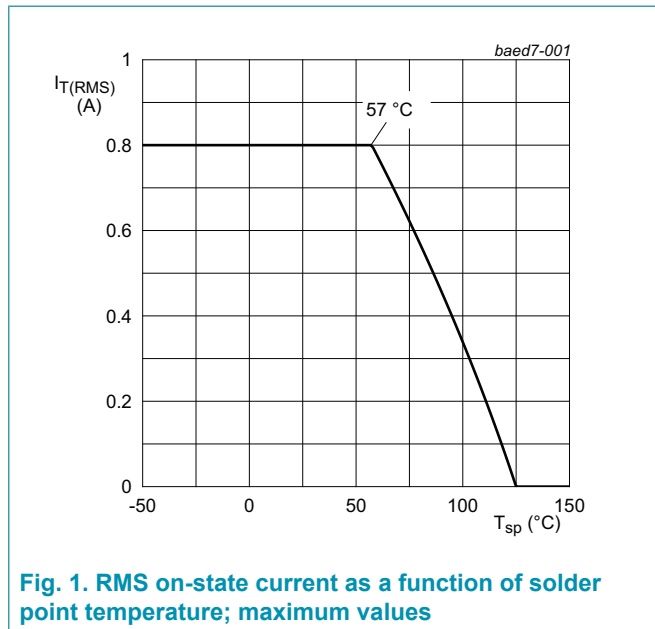
| Type number | Marking codes |
|----------------|----------------|
| BTA2008-1000DN | BTA2008-1000DN |

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Values | Unit |
|--------------|--------------------------------------|--|------------|-------------|
| V_{DRM} | repetitive peak off-state voltage | | 1000 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 57^{\circ}C$; Fig. 1 ; Fig. 2 ; Fig. 3 | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $t_p = 20$ ms; $T_{j(init)} = 25^{\circ}C$; Fig. 4 ; Fig. 5 | 9 | A |
| | | full sine wave; $t_p = 16.7$ ms; $T_{j(init)} = 25^{\circ}C$ | 9.9 | A |
| I^2t | I^2t for fusing | $t_p = 10$ ms; sine wave | 0.41 | A^2/s |
| dI_T/dt | rate of rise of on-state current | $I_G = 10$ mA | 100 | $A/\mu s$ |
| I_{GM} | peak gate current | | 1 | A |
| P_{GM} | peak gate power | | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | 0.1 | W |
| T_{stg} | storage temperature | | -40 to 150 | $^{\circ}C$ |
| T_j | junction temperature | | 125 | $^{\circ}C$ |



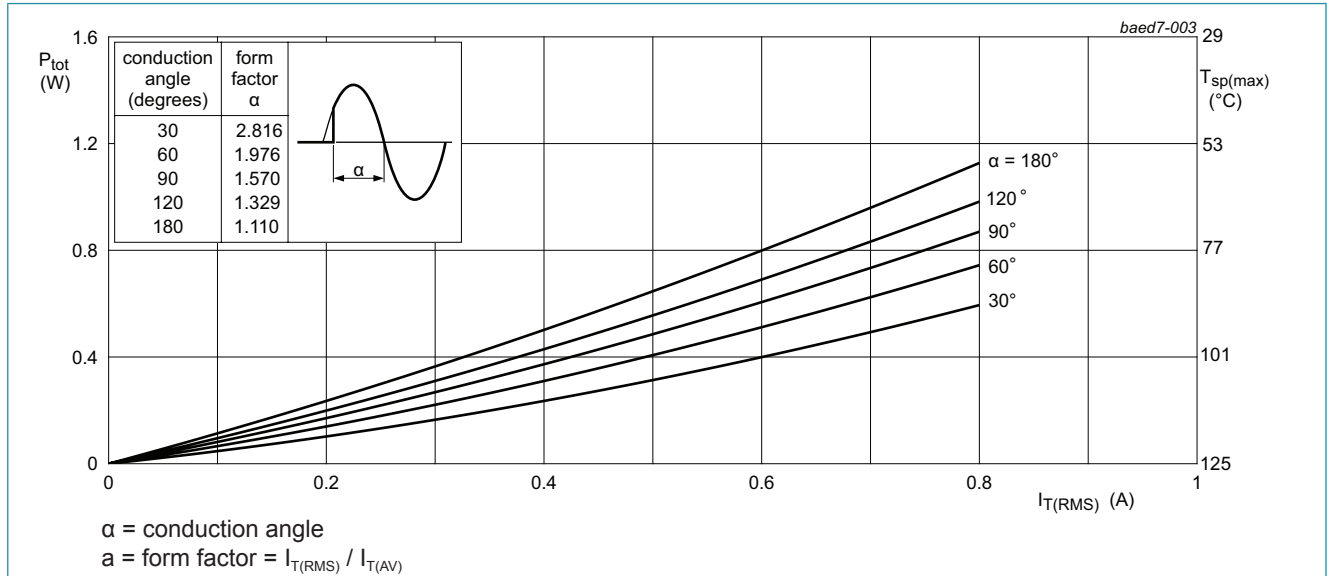


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

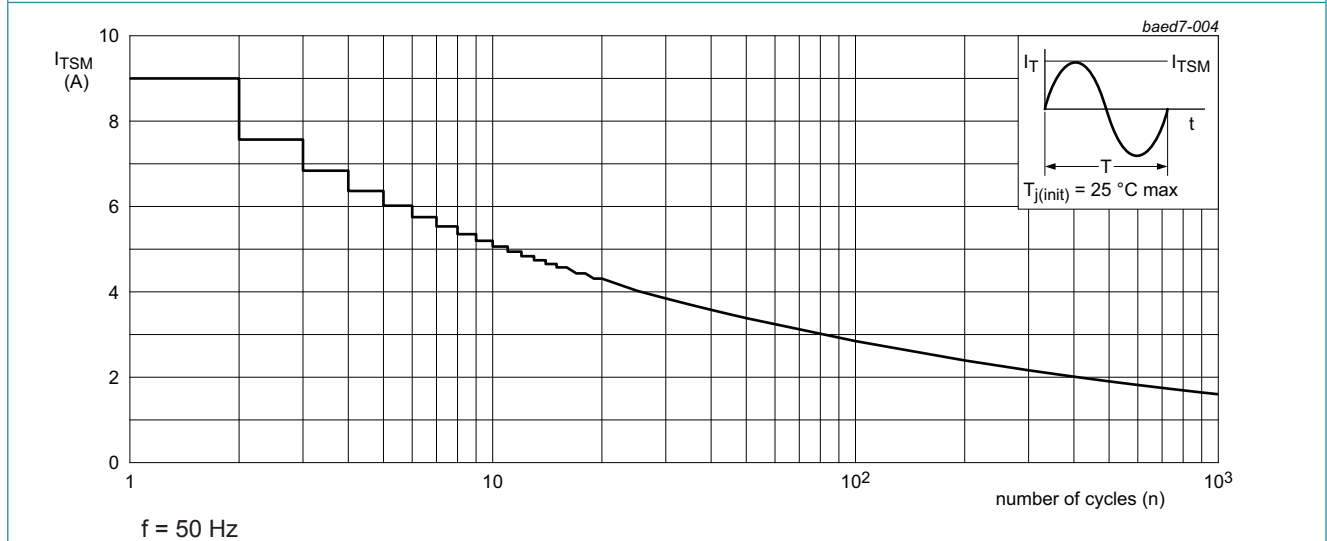


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

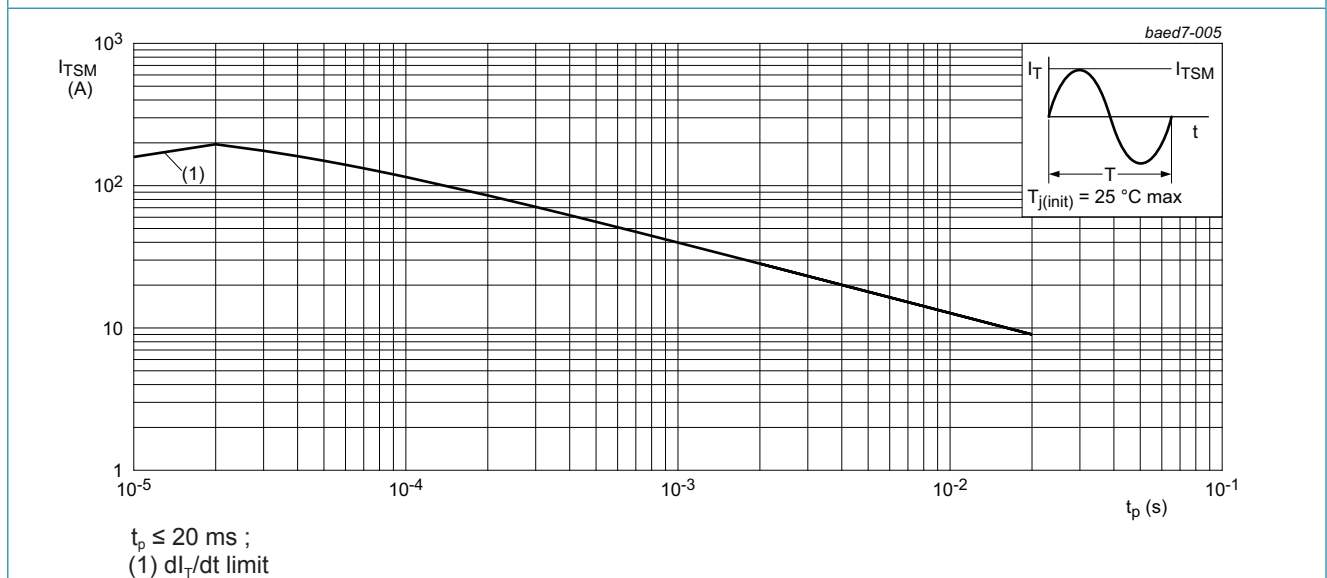


Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

9. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|------------------------|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead | Fig. 6 | - | - | 60 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air | - | 150 | - | K/W |

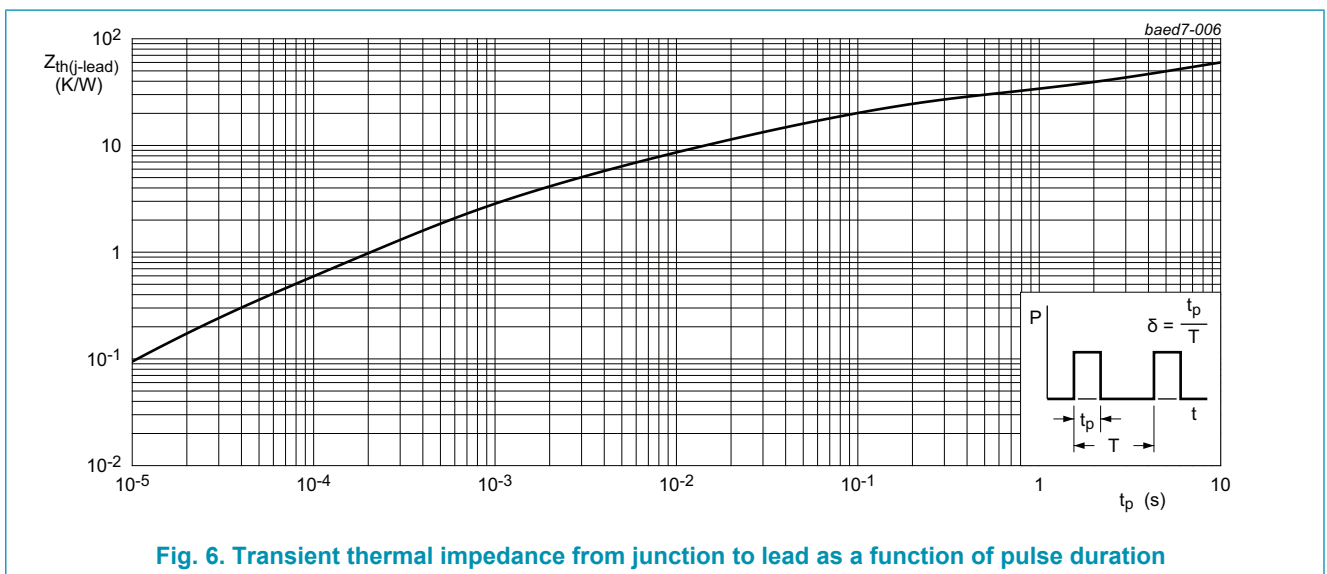
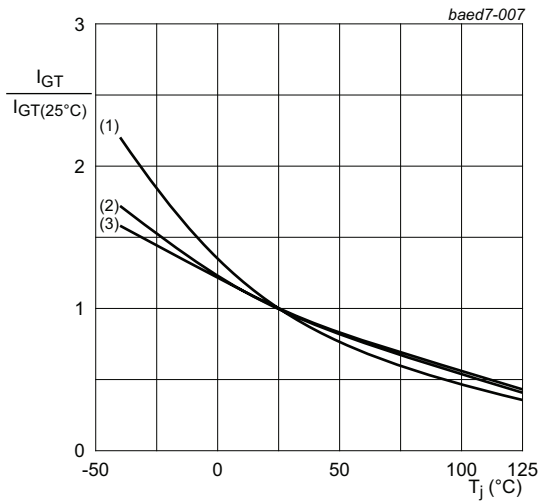


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse duration

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 7 | 0.25 | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 7 | 0.25 | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_J = 25\text{ °C}$; Fig. 8 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_J = 25\text{ °C}$; Fig. 8 | - | - | 20 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_J = 25\text{ °C}$; Fig. 8 | - | - | 10 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_J = 25\text{ °C}$; Fig. 9 | - | - | 10 | mA |
| V_T | on-state voltage | $I_T = 0.85\text{ A}$; $T_J = 25\text{ °C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 25\text{ °C}$; Fig. 11 | - | 0.85 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_J = 125\text{ °C}$; Fig. 11 | 0.2 | 0.3 | - | V |
| I_D | off-state current | $V_D = 1000\text{ V}$; $T_J = 25\text{ °C}$ | - | - | 10 | μA |
| | | $V_D = 1000\text{ V}$; $T_J = 125\text{ °C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 670\text{ V}$; $T_J = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | - | 150 | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_J = 125\text{ °C}$; $I_{T(RMS)} = 0.85\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 0.5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_J = 125\text{ °C}$; $I_{T(RMS)} = 0.85\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 1 | - | - | A/ms |



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

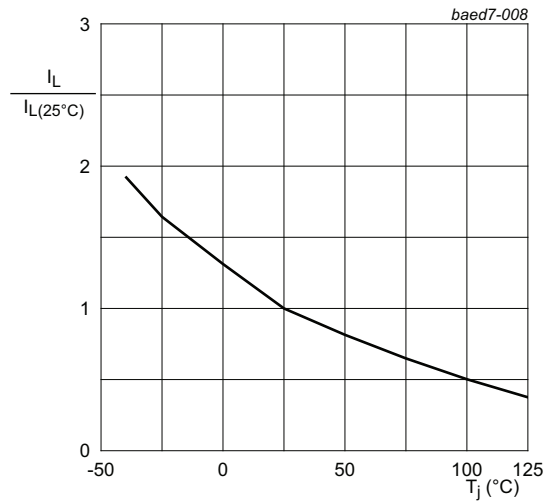


Fig. 8. Normalized latching current as a function of junction temperature

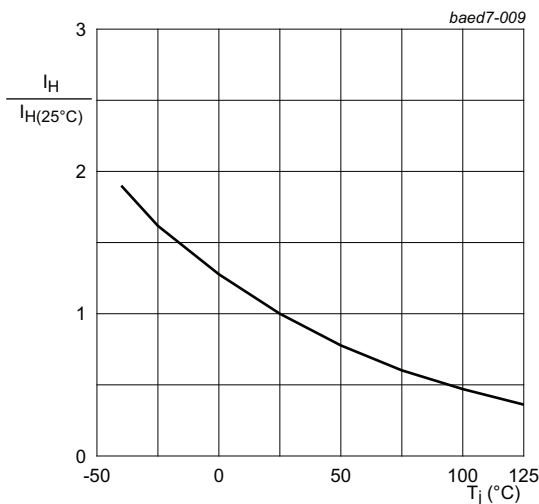
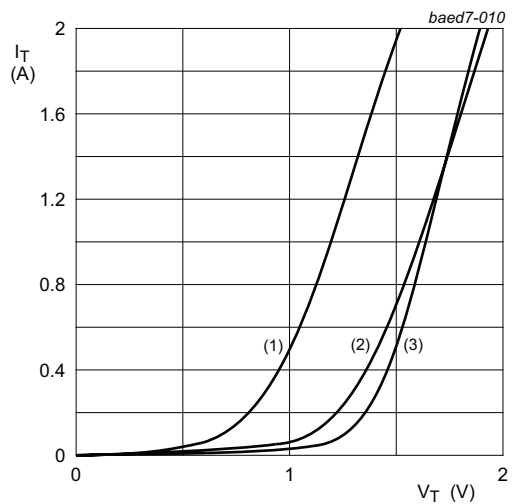


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.220\text{ V}$; $R_s = 0.3875\ \Omega$

- (1) $T_j = 125^\circ\text{C}$; typical values
- (2) $T_j = 125^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

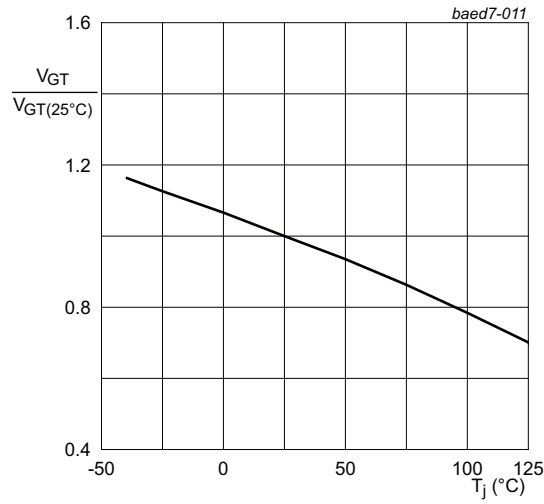
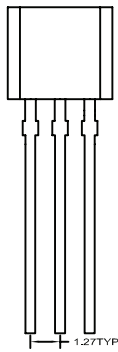


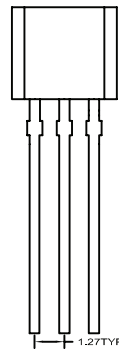
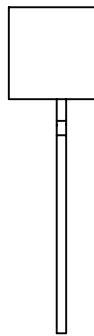
Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

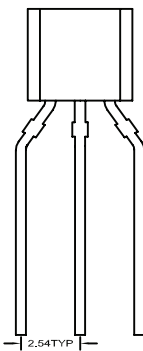
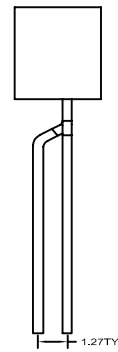
SOT54 PACKAGE OUTLINE



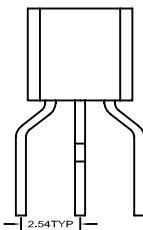
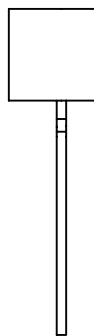
SOT54
Bulk Pack - 412



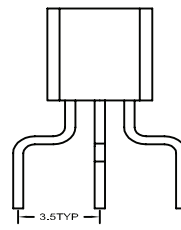
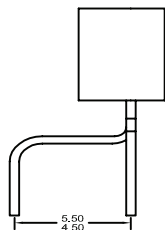
SOT54 LEADS ON CIRCLE
Bulk Pack - 112



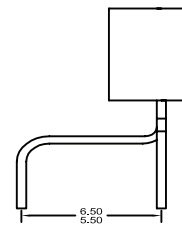
SOT54 WIDE PITCH
Tape/ Reel Pack - 116
Ammo Pack - 126



SOT54 LEAD BEND L01
Bulk Pack - 412



SOT54 LEAD BEND L02
Bulk Pack - 412



Remark: Detailed dimensions refer to POD drawing.

12. Legal information

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|--------------------------------|--------------------|---|
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13. Contents

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Date of release: 24 July 2017

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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