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Kind regards,

Team Nexperia

PEMD9; PUMD9

NPN/PNP resistor-equipped transistors;
R1 = 10 k Ω , R2 = 47 k Ω

Rev. 6 — 22 November 2011

Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/NPN complement	Package configuration
	NXP	JEITA			
PEMD9	SOT666	-	PEMB9	PEMH9	ultra small and flat lead
PUMD9	SOT363	SC-88	PUMB9	PUMH9	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

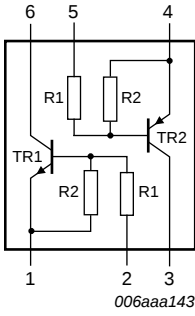
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		3.7	4.7	5.7	



2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMD9	-	plastic surface-mounted package; 6 leads	SOT666
PUMD9	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PEMD9	D9
PUMD9	D*9

[1] * = placeholder for manufacturing site code

5. Limiting values

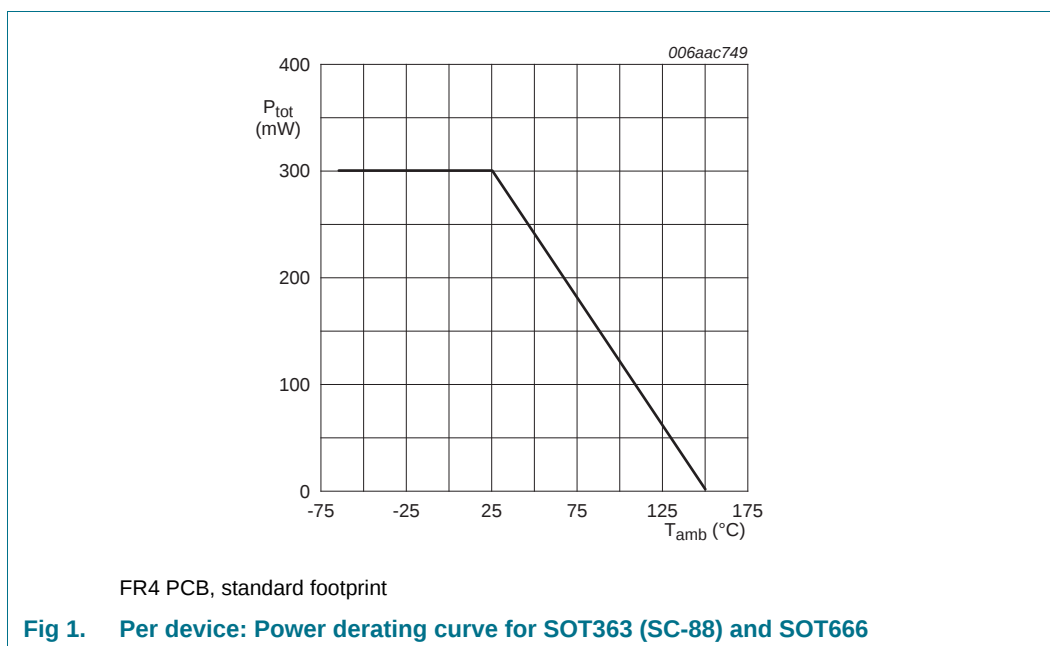
Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity					
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	50	V
V _{EBO}	emitter-base voltage	open collector	-	6	V
V _I	input voltage TR1				
	positive		-	+40	V
	negative		-	-6	V
	input voltage TR2				
	positive		-	+6	V
	negative		-	-40	V
I _O	output current		-	100	mA
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	PEMD9 (SOT666)		[1][2] -	200	mW
	PUMD9 (SOT363)		[1] -	200	mW
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	PEMD9 (SOT666)		[1][2] -	300	mW
	PUMD9 (SOT363)		[1] -	300	mW
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	PEMD9 (SOT666)		[1][2]	-	625	K/W
	PUMD9 (SOT363)		[1]	-	625	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	PEMD9 (SOT666)		[1][2]	-	417	K/W
	PUMD9 (SOT363)		[1]	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD9 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMD9 (SOT363); typical values

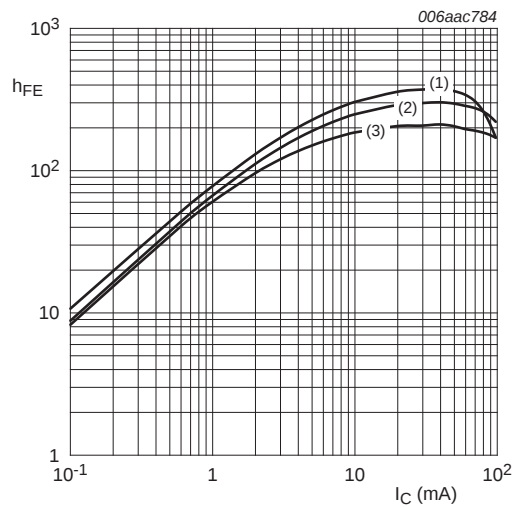
7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

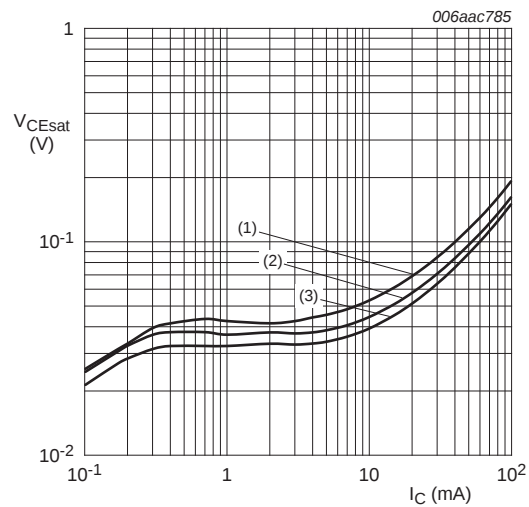
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	150	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}$	-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	0.7	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 1\text{ mA}$	1.4	0.8	-	V
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		3.7	4.7	5.7	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$				
	TR1 (NPN)		-	-	2.5	pF
	TR2 (PNP)		-	-	3	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}$ [1]				
	TR1 (NPN)		-	230	-	MHz
	TR2 (PNP)		-	180	-	MHz

[1] Characteristics of built-in transistor



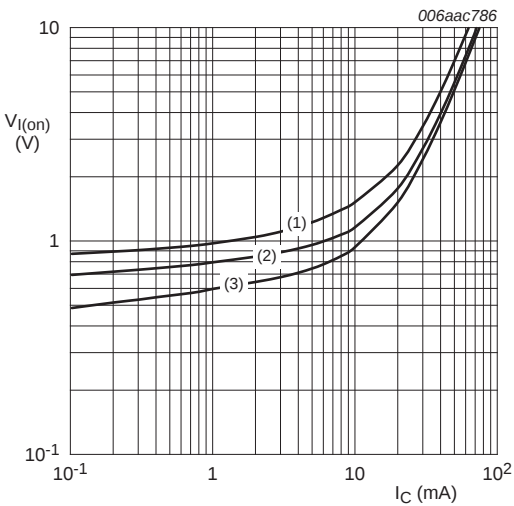
$V_{CE} = 5$ V
(1) $T_{amb} = 100$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = -40$ °C

Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values



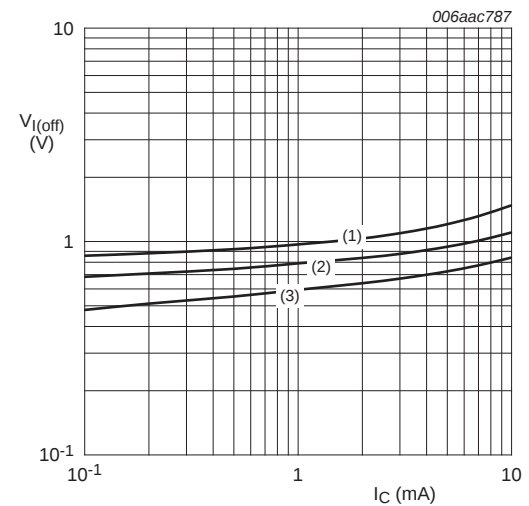
$I_C/I_B = 20$
(1) $T_{amb} = 100$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = -40$ °C

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



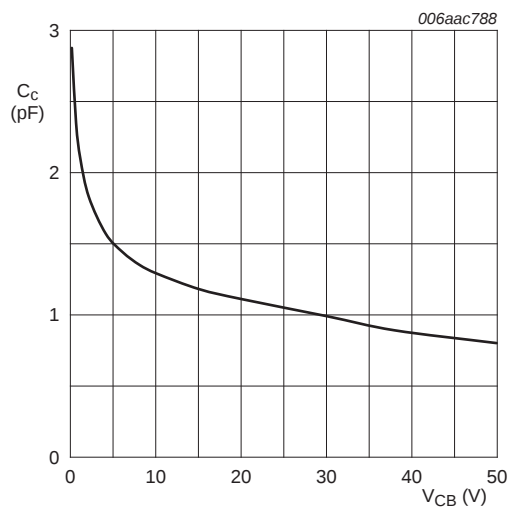
$V_{CE} = 0.3$ V
(1) $T_{amb} = -40$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 100$ °C

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



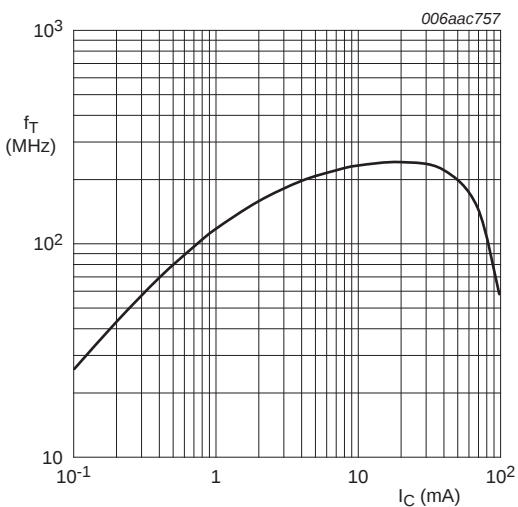
$V_{CE} = 5$ V
(1) $T_{amb} = -40$ °C
(2) $T_{amb} = 25$ °C
(3) $T_{amb} = 100$ °C

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



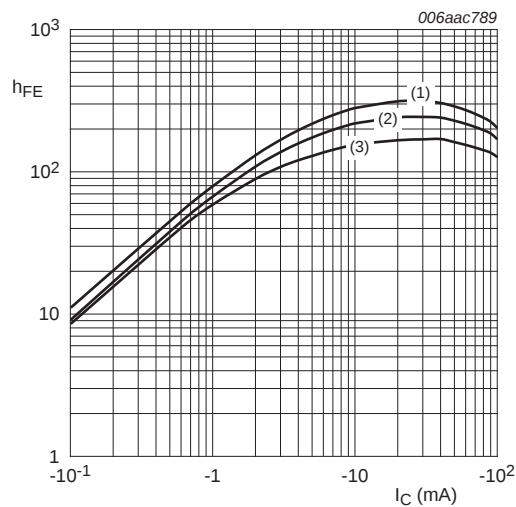
$f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

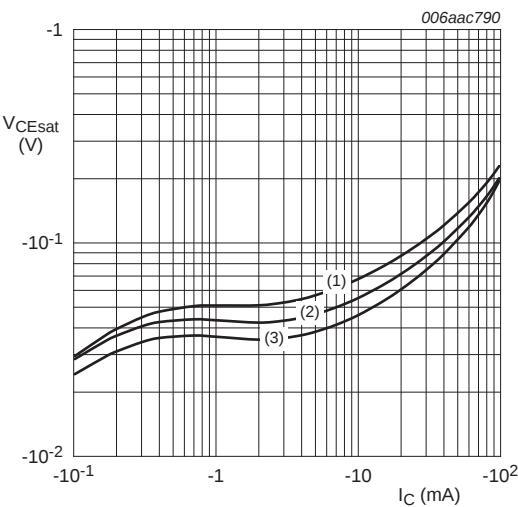
Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



$V_{CE} = -5 \text{ V}$

- (1) $T_{\text{amb}} = 100 \text{ }^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
- (3) $T_{\text{amb}} = -40 \text{ }^\circ\text{C}$

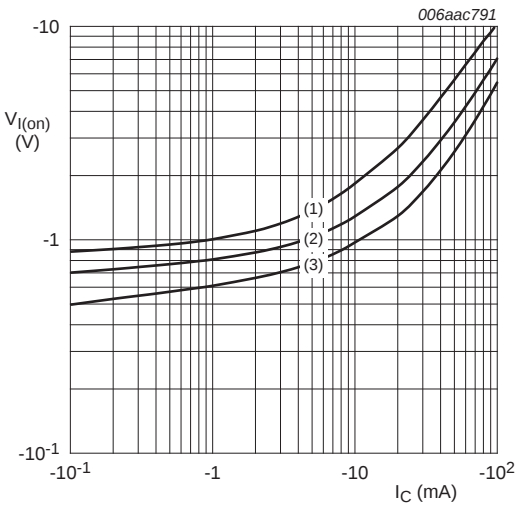
Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values



$I_C/I_B = 20$

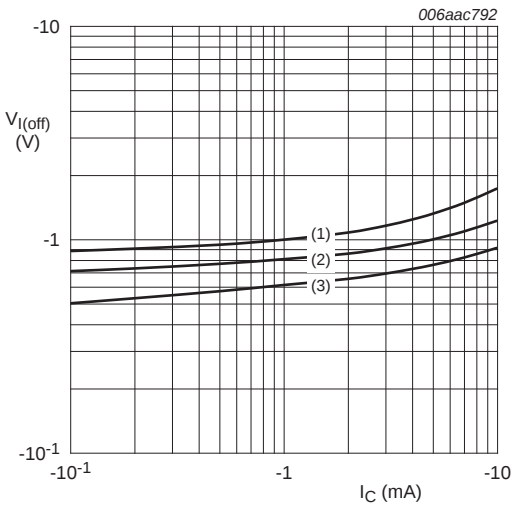
- (1) $T_{\text{amb}} = 100 \text{ }^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$
- (3) $T_{\text{amb}} = -40 \text{ }^\circ\text{C}$

Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



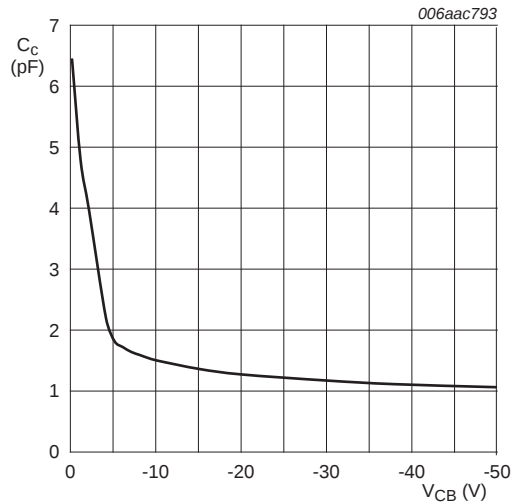
- $V_{CE} = -0.3\text{ V}$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values



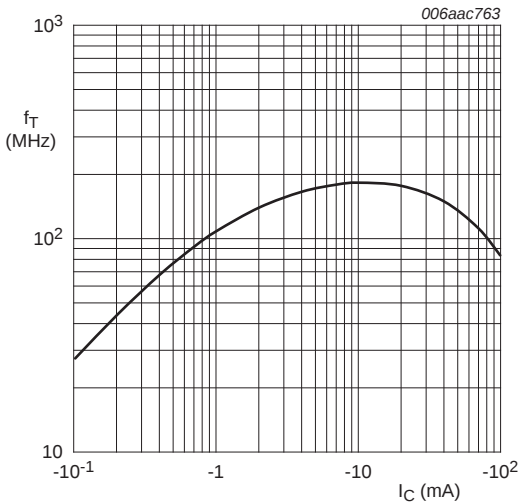
- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



$f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

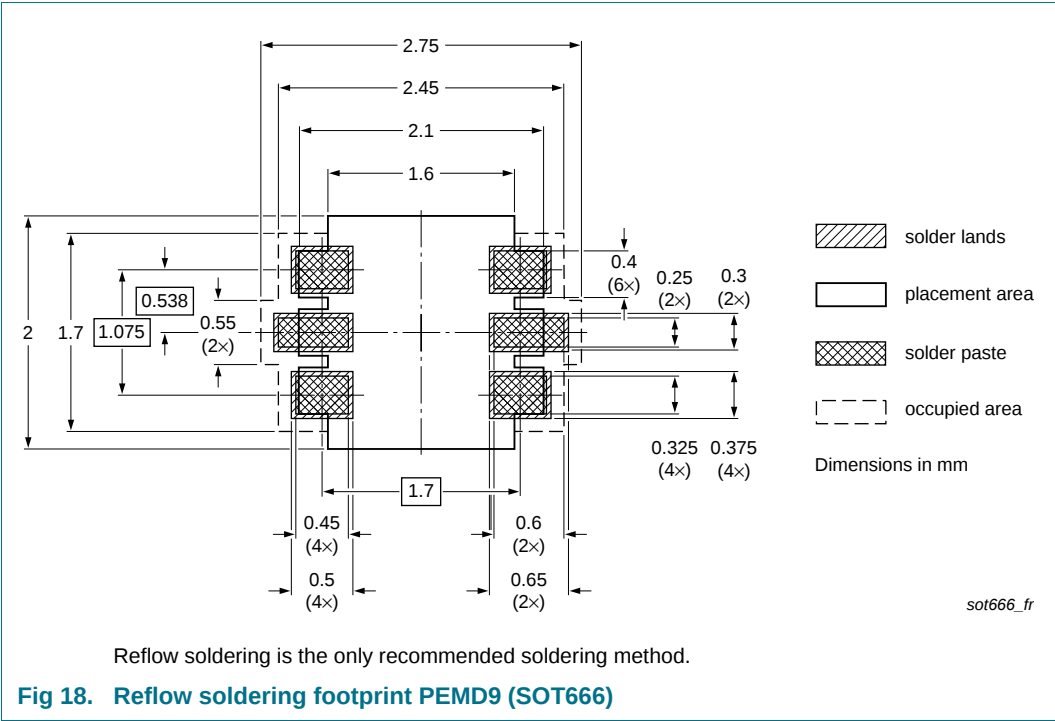
Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = -5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Soldering



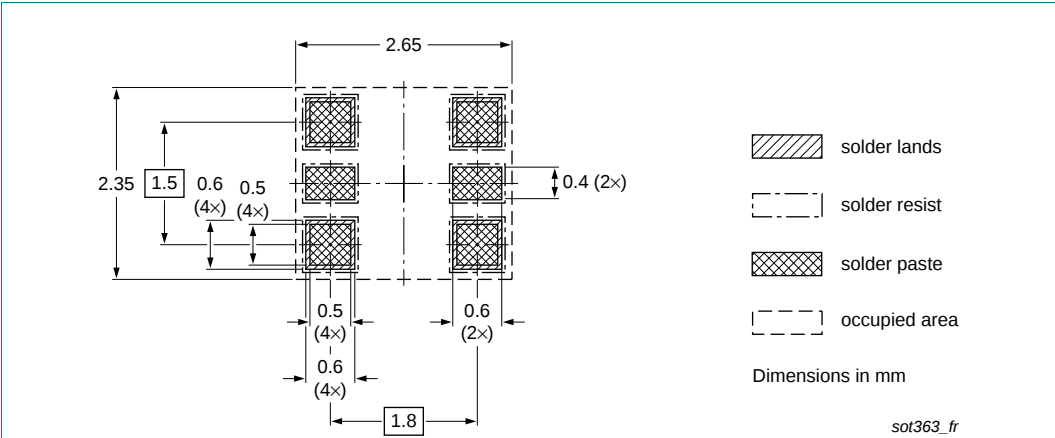


Fig 19. Reflow soldering footprint PUMD9 (SOT363)

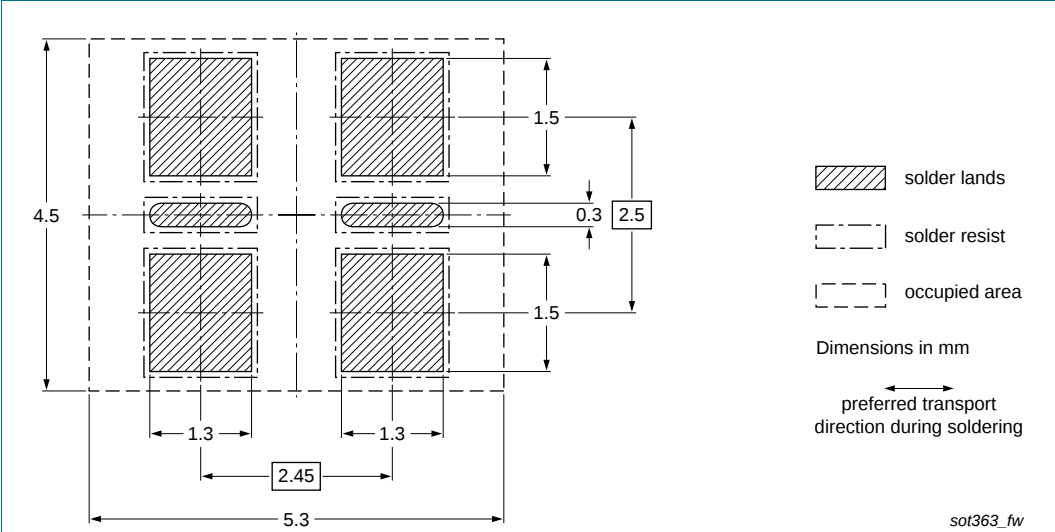


Fig 20. Wave soldering footprint PUMD9 (SOT363)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD9_PUMD9 v.6	20111122	Product data sheet	-	PEMD9_PUMD9 v.5
Modifications:	- The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Section 1 "Product profile": updated Section 4 "Marking": updated Figure 1 to 15: added Section 5 "Limiting values": updated Section 6 "Thermal characteristics": updated Table 8 "Characteristics": $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated, f_T added Section 8 "Test information": added Section 9 "Package outline": superseded by minimized package outline drawings Section 10 "Packing information": added Section 11 "Soldering": added Section 13 "Legal information": updated			
PEMD9_PUMD9 v.5	20040415	Product data sheet	-	PEMD9_PUMD9 v.4
PEMD9_PUMD9 v.4	20031104	Product specification	-	PEMD9 v.2 PUMD9 v.3
PEMD9 v.2	20020905	Product specification	-	PEMD9 v.1
PEMD9 v.1	20011022	Preliminary specification	-	-
PUMD9 v.3	20010216	Product specification	-	PUMD9 v.2
PUMD9 v.2	19990520	Product specification	-	PUMD9 v.1
PUMD9 v.1	19990107	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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