

# USB Power Delivery Alternate Mode Controller on Type-C

## General Description

The CYPD1120 device belongs to Cypress's CCG1 product family, which provides a complete USB Type-C and USB Power Delivery port control solution. The scalable and reconfigurable core architecture of CCG1 enables a base Type-C solution that can scale to a complete 100-W USB Power Delivery with Alternate Mode mux support. CCG1 is also a Type-C cable ID IC for active and passive cables. The ARM® Cortex®-M0 CPU based core can use common open source firmware or custom solutions developed with common libraries and APIs. CCG1 is the CC controller that detects connector insert, plug orientation, and  $V_{CONN}$  switching signals. CCG1 makes it easier to add USB Power Delivery to any architecture because it provides the control signals to manage external VBUS and  $V_{CONN}$  power management solutions as well as external mux controls for most single cable-docking solutions. CCG1's packaging options, and programmability, enables any USB Type-C and USB Power Delivery solution.

## Applications

- Dongles, docking stations
- Type-C to DisplayPort
- Type-C to HDMI
- Type-C to DVI
- Type-C to VGA

## Features

### 32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU with 32-KB flash and 4-KB SRAM

### Integrated analog blocks

- 12-bit, 1-Msps ADC for VBUS voltage and current monitoring

### Integrated digital blocks

- Two configurable 16-bit TCPWM blocks
- One I<sup>2</sup>C master or slave

### Type-C Support

- Integrated transceiver (BB PHY)

### PD Support

- Supports VESA DisplayPort Alternate Mode on USB Type-C Standard Version 1.0

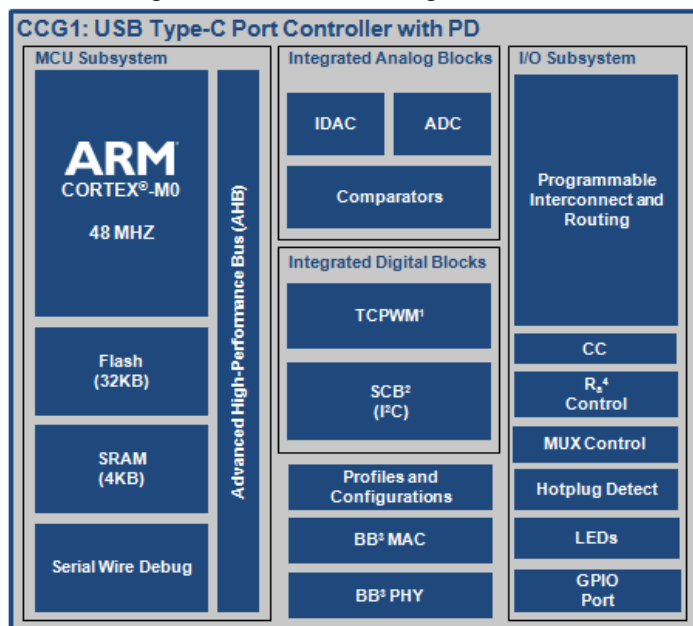
### Low-power operation

- 1.8-V to 5.5-V operation
- Sleep 1.3 mA, Deep Sleep 1.3  $\mu$ A<sup>[2]</sup>

### Packages

- 40-pin QFN
- 35-ball wafer-level CSP (WLCSP)

Figure 1. CCG1 Block Diagram<sup>[2, 3, 4, 5]</sup>



## Notes

1. Values measured for CCG1 silicon only. Application specific power numbers may be higher.
2. Timer, counter, pulse-width modulation block.
3. Serial communication block configurable as I<sup>2</sup>C.
4. Base band.
5. Termination resistor denoting an Alternate Mode Adaptor.

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## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

#### SRAM

A supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section [Power on page 7](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 1.8 to 5.5 V and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

#### Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I<sup>2</sup>C interface. The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I<sup>2</sup>C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.
- Fast-mode Plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8 mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I<sup>2</sup>C Master, it interposes an IDLE state between NACK and Repeated Start; the I<sup>2</sup>C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I<sup>2</sup>C Slave mode, and Address Match on External Clock is enabled (EC\_AM = 1) along with operation in the internally clocked mode (EC\_OP = 0), then its I<sup>2</sup>C address must be even.

### GPIO

The CCG1 has up to 10 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

## Pin Definitions

Table 1 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 20 on page 18 for pin numbers to package mapping.

**Table 1. Pin Definition for 40-Pin QFN and 35-Ball WLCSP**

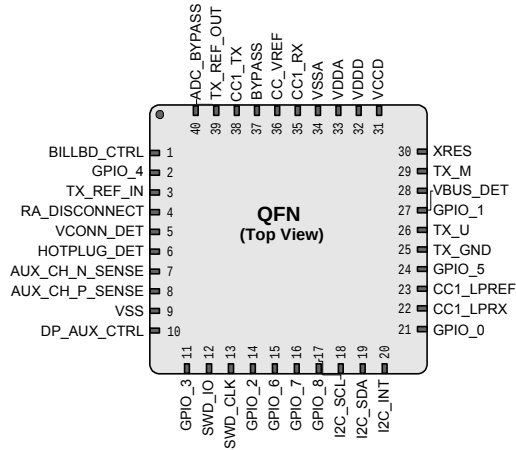
| Functional Pin Name | CYPD1120-35FNXIT | CYPD1120-40LQXI | Type  | Description                                                                                            |
|---------------------|------------------|-----------------|-------|--------------------------------------------------------------------------------------------------------|
| CC1_RX              | C4               | 35              | I     | CC1 control<br>0: TX enabled<br>z: RX sense                                                            |
| CC1_TX              | D7               | 38              | O     | Configuration Channel 1                                                                                |
| SWD_IO              | D1               | 12              | I/O   | SWD IO                                                                                                 |
| SWD_CLK             | C1               | 13              | I     | SWD Clock                                                                                              |
| I2C_SCL             | B1               | 18              | I     | I <sup>2</sup> C Slave Clock signal                                                                    |
| I2C_SDA             | B2               | 19              | I/O   | I <sup>2</sup> C Slave Data signal                                                                     |
| I2C_INT             | A2               | 20              | O     | I <sup>2</sup> C INT                                                                                   |
| XRES                | B6               | 30              | I     | Active Low Reset                                                                                       |
| VCCD                | A7               | 31              | POWER | Connect 1-μF capacitor between VCCD and Ground                                                         |
| VDDD                | C7               | 32              | POWER | VCONN Supply                                                                                           |
| VDDA                | C7               | 33              | POWER |                                                                                                        |
| VSSA                | B7               | 34              | GND   | Ground                                                                                                 |
| VSS                 | –                | 9               | GND   | Ground                                                                                                 |
| CC_VREF             | C5               | 36              | I     | Data reference signal for CC lines                                                                     |
| ADC_BYPASS          | E7               | 40              | I     | No Connect                                                                                             |
| TX_U                | B3               | 26              | O     | Signals for internal use only. The TX_U output signal should be connected to the TX_M signal           |
| TX_M                | B5               | 29              | I     |                                                                                                        |
| TX_REF_IN           | D3               | 3               | I     | Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor                     |
| TX_GND              | A3               | 25              | I     | Connect to GND via 2K 1% resistor                                                                      |
| TX_REF_OUT          | D4               | 39              | O     | Reference signal generated by connecting internal current source to two 1K external resistors          |
| RA_DISCONNECT       | E4               | 4               | O     | Optional control signal to remove RA after assertion of VCONN<br>0: RA disconnected<br>1: RA connected |
| CC1_LPREF           | A5               | 23              | I     | Reference signal for internal use. Connect to the output of resistor divider from VDDD.                |
| VCONN_DET           | E5               | 5               | O     | Detects presence of VCONN before responding to CC communication                                        |
| BYPASS              | D5               | –               | I     | Bypass capacitor for internal analog circuits                                                          |
|                     | –                | 37              |       |                                                                                                        |
| CC1_LPRX            | C3               | 22              | I     | Configuration Channel 1 RX signal for Low Power States                                                 |
| VBUS_DET            | B4               | 28              | I     | Detects presence of VBUS before enabling Billboard device                                              |

**Table 1. Pin Definition for 40-Pin QFN and 35-Ball WLCSP (continued)**

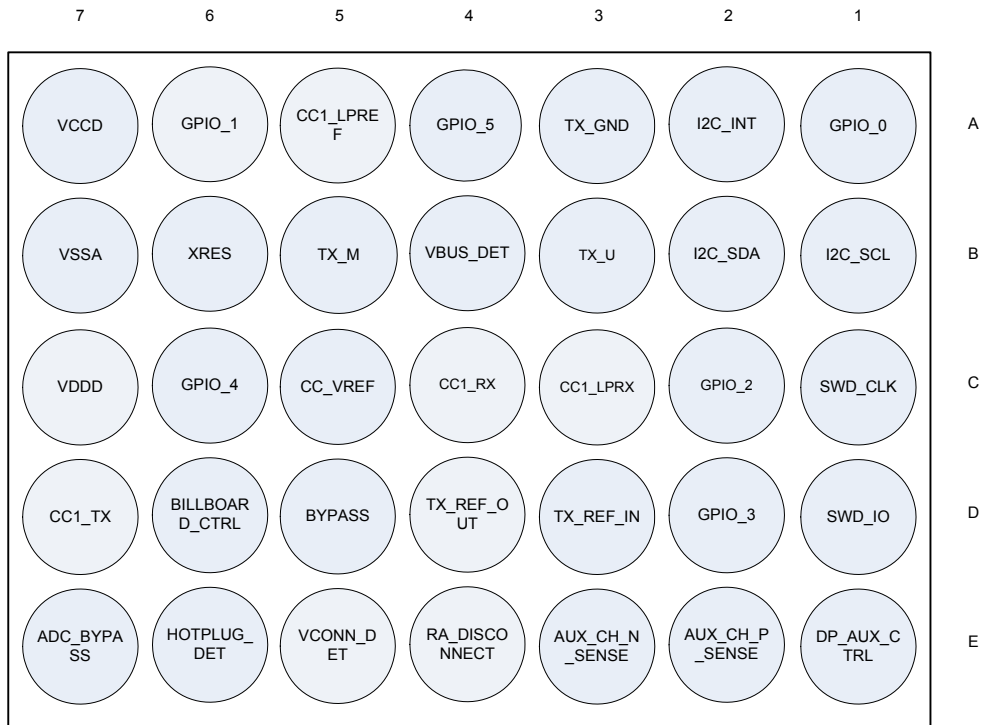
| Functional Pin Name | CYPD1120-35FNXIT | CYPD1120-40LQXI | Type | Description                                                 |
|---------------------|------------------|-----------------|------|-------------------------------------------------------------|
| BILLBOARD_CTRL      | D6               | –               | O    | Enables Billboard Device                                    |
|                     | –                | 1               |      |                                                             |
| DP_AUX_CTRL         | E1               | 10              | O    | Closes AUX_P/N switch after successful Alternate Mode entry |
| AUX_CH_P_SENSE      | E2               | 8               | I    | Senses presence of DisplayPort on UFP_D                     |
| AUX_CH_N_SENSE      | E3               | 7               | I    | Senses presence of DisplayPort on DFP_D                     |
| HOTPLUG_DET         | E6               | 6               | I/O  | HotPlug Detection/Driver for DisplayPort Alternate Mode     |
| GPIO_0              | A1               | 21              | I/O  | GPIO                                                        |
| GPIO_1              | A6               | 27              | I/O  | GPIO                                                        |
| GPIO_2              | C2               | 14              | I/O  | GPIO                                                        |
| GPIO_3              | D2               | 11              | I/O  | GPIO                                                        |
| GPIO_4              | C6               | –               | I/O  | GPIO                                                        |
|                     | –                | 2               |      |                                                             |
| GPIO_5              | A4               | 24              | I/O  | GPIO                                                        |
| GPIO_6              | –                | 15              | I/O  | GPIO                                                        |
| GPIO_7              | –                | 16              | I/O  | GPIO                                                        |
| GPIO_8              | –                | 17              | I/O  | GPIO                                                        |

## Pinouts

**Figure 2. 40-pin QFN Pinout**



**Figure 3. 35-Ball WLCSP Pinout**



## Power

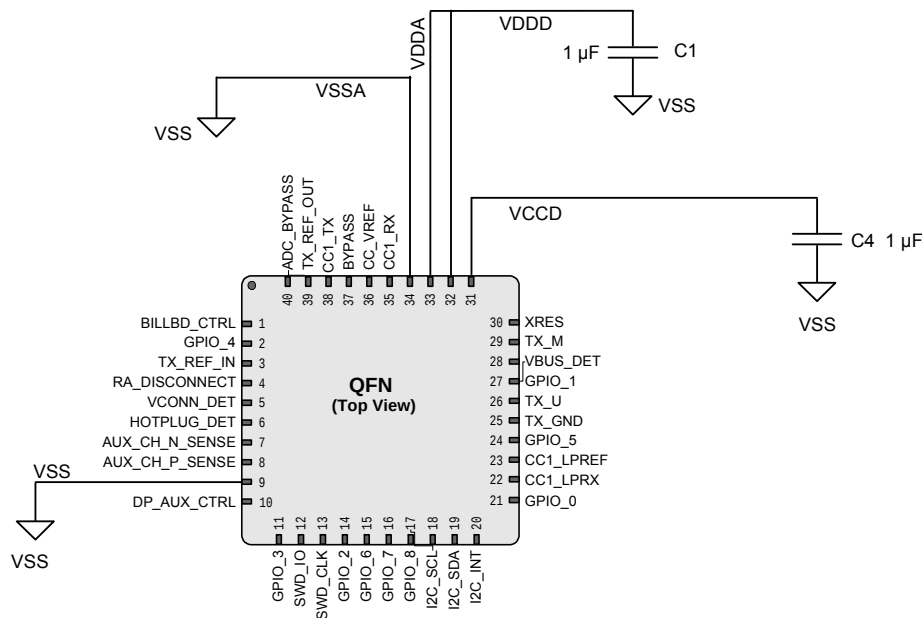
The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.8 V to 5.5 V with all functions and circuits operating over that range.

The CCG1 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the CCG1 supplies the internal logic and the VCCD output of the CCG1 must be bypassed to ground via an external capacitor (in the range of 1  $\mu$ F to 1.6  $\mu$ F; X5R ceramic or better). No voltage source should be applied to this pin.

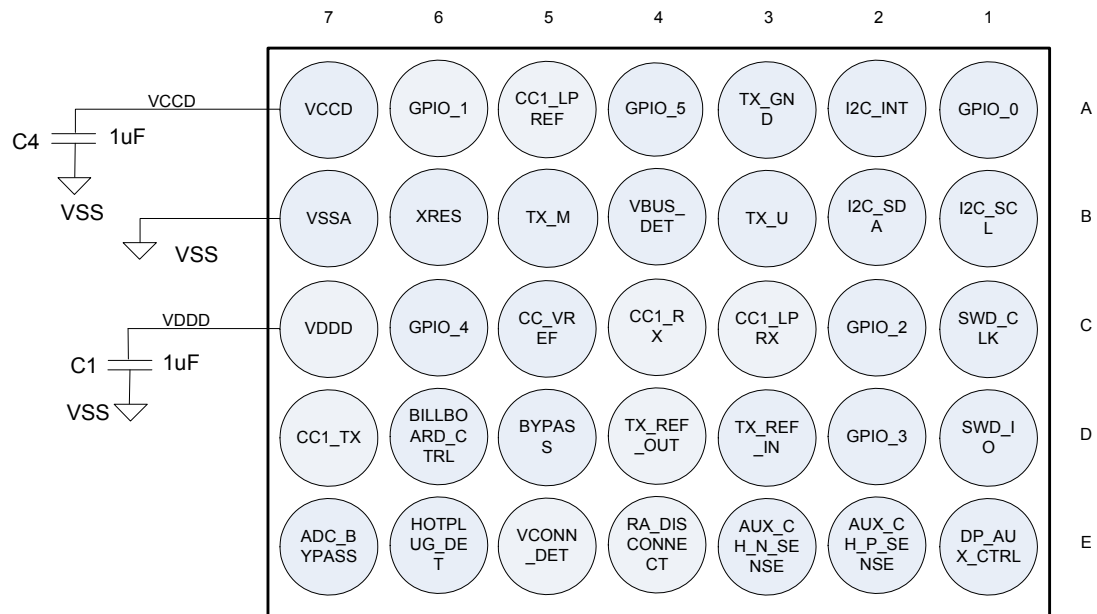
VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu$ F range in parallel with a smaller capacitor (0.1  $\mu$ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Examples of bypass schemes follow.

**Figure 4. 40-pin QFN Example**



**Figure 5. 35-ball WLCSP Example**





## Electrical Specifications

### Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings<sup>[6]</sup>

| Spec ID# | Parameter                   | Description                                                                                                        | Min   | Typ | Max                   | Units | Details/<br>Conditions                 |
|----------|-----------------------------|--------------------------------------------------------------------------------------------------------------------|-------|-----|-----------------------|-------|----------------------------------------|
| SID1     | V <sub>DDD_ABS</sub>        | Digital supply relative to V <sub>SSD</sub>                                                                        | −0.5  | –   | 6.0                   | V     | Absolute max                           |
| SID2     | V <sub>CCD_ABS</sub>        | Direct digital core voltage input relative to V <sub>SSD</sub>                                                     | −0.5  | –   | 1.95                  | V     | Absolute max                           |
| SID3     | V <sub>GPIO_ABS</sub>       | GPIO voltage                                                                                                       | −0.5  | –   | V <sub>DDD</sub> +0.5 | V     | Absolute max                           |
| SID4     | I <sub>GPIO_ABS</sub>       | Maximum current per GPIO                                                                                           | −25.0 | –   | 25.0                  | mA    | Absolute max                           |
| SID5     | I <sub>GPIO_injection</sub> | GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub> | −0.50 | –   | 0.5                   | mA    | Absolute max, current injected per pin |
| BID44    | ESD_HBM                     | Electrostatic discharge human body model                                                                           | 2200  | –   | –                     | V     | –                                      |
| BID45    | ESD_CDM                     | Electrostatic discharge charged device model                                                                       | 500   | –   | –                     | V     | –                                      |
| BID46    | LU                          | Pin current for latch-up                                                                                           | −200  | –   | 200                   | mA    | –                                      |

### Device Level Specifications

All specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 100^{\circ}\text{C}$  for 35-CSP and 40-QFN package options. Specifications are valid for 1.8 V to 5.5 V, except where noted.

Table 3. DC Specifications

| Spec ID#                                                                                               | Parameter          | Description                                | Min | Typ  | Max  | Units | Details/<br>Conditions |
|--------------------------------------------------------------------------------------------------------|--------------------|--------------------------------------------|-----|------|------|-------|------------------------|
| SID53                                                                                                  | V <sub>DDD</sub>   | Power supply input voltage                 | 1.8 | –    | 5.5  | V     | With regulator enabled |
| SID54                                                                                                  | V <sub>CCD</sub>   | Output voltage (for core logic)            | –   | 1.8  | –    | V     | –                      |
| SID55                                                                                                  | C <sub>EFC</sub>   | External regulator voltage bypass          | 1.0 | 1.3  | 1.6  | μF    | X5R ceramic or better  |
| SID56                                                                                                  | C <sub>EXC</sub>   | Power supply decoupling capacitor          | –   | 1.0  | –    | μF    | X5R ceramic or better  |
| <b>Active Mode, V<sub>DDD</sub> = 1.8 to 5.5 V. Typical values measured at V<sub>DD</sub> = 3.3 V.</b> |                    |                                            |     |      |      |       |                        |
| SID19                                                                                                  | I <sub>DD14</sub>  | Execute from flash; CPU at 48 MHz          | –   | 12.8 | –    | mA    | T = 25 °C              |
| SID20                                                                                                  | I <sub>DD15</sub>  | Execute from flash; CPU at 48 MHz          | –   | –    | 13.8 | mA    | –                      |
| <b>Sleep Mode, V<sub>DDD</sub> = 1.8 to 5.5 V</b>                                                      |                    |                                            |     |      |      |       |                        |
| SID25A                                                                                                 | I <sub>DD20A</sub> | I <sup>2</sup> C wakeup and comparators on | –   | 1.7  | 2.2  | mA    | –                      |
| <b>Deep Sleep Mode, V<sub>DDD</sub> = 1.8 to 3.6 V (Regulator on)</b>                                  |                    |                                            |     |      |      |       |                        |
| SID31                                                                                                  | I <sub>DD26</sub>  | I <sup>2</sup> C wakeup on                 | –   | 1.3  | –    | μA    | T = 25 °C, 3.6 V       |
| SID32                                                                                                  | I <sub>DD27</sub>  | I <sup>2</sup> C wakeup on                 | –   | –    | 50.0 | μA    | T = 85 °C              |
| <b>Deep Sleep Mode, V<sub>DDD</sub> = 3.6 to 5.5 V</b>                                                 |                    |                                            |     |      |      |       |                        |
| SID34                                                                                                  | I <sub>DD29</sub>  | I <sup>2</sup> C wakeup                    | –   | 15.0 | –    | μA    | T = 25 °C, 5.5 V       |
| <b>XRES Current</b>                                                                                    |                    |                                            |     |      |      |       |                        |
| SID307                                                                                                 | I <sub>DD_XR</sub> | Supply current while XRES asserted         | –   | 2.0  | 5.0  | mA    | –                      |

#### Note

6. Usage above the absolute maximum conditions listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 4. AC Specifications**

| Spec ID# | Parameter               | Description                 | Min | Typ | Max  | Units | Details/<br>Conditions                     |
|----------|-------------------------|-----------------------------|-----|-----|------|-------|--------------------------------------------|
| SID48    | F <sub>CPU</sub>        | CPU frequency               | DC  | –   | 48.0 | MHz   | 1.8 ≤ V <sub>DD</sub> ≤ 5.5                |
| SID49    | T <sub>SLEEP</sub>      | Wakeup from sleep mode      | –   | 0   | –    | μs    | Guaranteed by characterization             |
| SID50    | T <sub>DEEPSLEEP</sub>  | Wakeup from Deep Sleep mode | –   | –   | 25.0 | μs    | 24-MHz IMO. Guaranteed by characterization |
| SID52    | T <sub>RESETWIDTH</sub> | External reset pulse width  | 1.0 | –   | –    | μs    | Guaranteed by characterization             |

**I/O**
**Table 5. I/O DC Specifications**

| Spec ID# | Parameter                      | Description                                                          | Min                   | Typ  | Max                   | Units | Details/<br>Conditions                                  |
|----------|--------------------------------|----------------------------------------------------------------------|-----------------------|------|-----------------------|-------|---------------------------------------------------------|
| SID57    | V <sub>IH</sub> <sup>[7]</sup> | Input voltage high threshold                                         | 0.7 × V <sub>DD</sub> | –    | –                     | V     | CMOS Input                                              |
| SID58    | V <sub>IL</sub>                | Input voltage low threshold                                          | –                     | –    | 0.3 × V <sub>DD</sub> | V     | CMOS Input                                              |
| SID241   | V <sub>IH</sub> <sup>[7]</sup> | LVTTL input, V <sub>DD</sub> < 2.7 V                                 | 0.7 × V <sub>DD</sub> | –    | –                     | V     | –                                                       |
| SID242   | V <sub>IL</sub>                | LVTTL input, V <sub>DD</sub> < 2.7 V                                 | –                     | –    | 0.3 × V <sub>DD</sub> | V     | –                                                       |
| SID243   | V <sub>IH</sub> <sup>[7]</sup> | LVTTL input, V <sub>DD</sub> ≥ 2.7 V                                 | 2.0                   | –    | –                     | V     | –                                                       |
| SID244   | V <sub>IL</sub>                | LVTTL input, V <sub>DD</sub> ≥ 2.7 V                                 | –                     | –    | 0.8                   | V     | –                                                       |
| SID59    | V <sub>OH</sub>                | Output voltage high level                                            | V <sub>DD</sub> – 0.6 | –    | –                     | V     | I <sub>OH</sub> = 4 mA at 3-V V <sub>DD</sub>           |
| SID60    | V <sub>OH</sub>                | Output voltage high level                                            | V <sub>DD</sub> – 0.5 | –    | –                     | V     | I <sub>OH</sub> = 1 mA at 1.8-V V <sub>DD</sub>         |
| SID61    | V <sub>OL</sub>                | Output voltage low level                                             | –                     | –    | 0.6                   | V     | I <sub>OL</sub> = 4 mA at 1.8-V V <sub>DD</sub>         |
| SID62    | V <sub>OL</sub>                | Output voltage low level                                             | –                     | –    | 0.6                   | V     | I <sub>OL</sub> = 8 mA at 3-V V <sub>DD</sub>           |
| SID62A   | V <sub>OL</sub>                | Output voltage low level                                             | –                     | –    | 0.4                   | V     | I <sub>OL</sub> = 3 mA at 3-V V <sub>DD</sub>           |
| SID63    | R <sub>PULLUP</sub>            | Pull-up resistor                                                     | 3.5                   | 5.6  | 8.5                   | kΩ    | –                                                       |
| SID64    | R <sub>PULLDOWN</sub>          | Pull-down resistor                                                   | 3.5                   | 5.6  | 8.5                   | kΩ    | –                                                       |
| SID65    | I <sub>IL</sub>                | Input leakage current (absolute value)                               | –                     | –    | 2.0                   | nA    | 25 °C, V <sub>DD</sub> = 3.0 V                          |
| SID65A   | I <sub>IL_CTBM</sub>           | Input leakage current (absolute value) for analog pins               | –                     | –    | 4.0                   | nA    | –                                                       |
| SID66    | C <sub>IN</sub>                | Input capacitance                                                    | –                     | –    | 7.0                   | pF    | –                                                       |
| SID67    | V <sub>HYSTTL</sub>            | Input hysteresis LVTTL                                               | 15.0                  | 40.0 | –                     | mV    | V <sub>DD</sub> ≥ 2.7 V. Guaranteed by characterization |
| SID68    | V <sub>HYSCMOS</sub>           | Input hysteresis CMOS                                                | 200.0                 | –    | –                     | mV    | V <sub>DD</sub> ≥ 4.5 V. Guaranteed by characterization |
| SID69    | I <sub>DIODE</sub>             | Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub> | –                     | –    | 100.0                 | μA    | Guaranteed by characterization                          |
| SID69A   | I <sub>TOT_GPIO</sub>          | Maximum Total Source or Sink Chip Current                            | –                     | –    | 200.0                 | mA    | Guaranteed by characterization                          |

**Note**

 7. V<sub>IH</sub> must not exceed V<sub>DD</sub> + 0.2 V.

**Table 6. I/O AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter          | Description | Min | Typ | Max  | Units | Details/<br>Conditions                |
|----------|--------------------|-------------|-----|-----|------|-------|---------------------------------------|
| SID70    | T <sub>RISEF</sub> | Rise time   | 2.0 | –   | 12.0 | ns    | 3.3-V V <sub>DD</sub> , Cload = 25 pF |
| SID71    | T <sub>FALLF</sub> | Fall time   | 2.0 | –   | 12.0 | ns    | 3.3-V V <sub>DD</sub> , Cload = 25 pF |

XRES

**Table 7. XRES DC Specifications**

| Spec ID# | Parameter            | Description                                                          | Min                   | Typ   | Max                   | Units | Details/<br>Conditions         |
|----------|----------------------|----------------------------------------------------------------------|-----------------------|-------|-----------------------|-------|--------------------------------|
| SID77    | V <sub>IH</sub>      | Input voltage high threshold                                         | 0.7 × V <sub>DD</sub> | –     | –                     | V     | CMOS input                     |
| SID78    | V <sub>IL</sub>      | Input voltage low threshold                                          | –                     | –     | 0.3 × V <sub>DD</sub> | V     | CMOS input                     |
| SID79    | R <sub>PULLUP</sub>  | Pull-up resistor                                                     | 3.5                   | 5.6   | 8.5                   | kΩ    | –                              |
| SID80    | C <sub>IN</sub>      | Input capacitance                                                    | –                     | 3.0   | –                     | pF    | –                              |
| SID81    | V <sub>HYSXRES</sub> | Input voltage hysteresis                                             | –                     | 100.0 | –                     | mV    | Guaranteed by characterization |
| SID82    | I <sub>DIODE</sub>   | Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub> | –                     | –     | 100.0                 | μA    | Guaranteed by characterization |

## Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

*Pulse Width Modulation (PWM) for VSEL and CUR\_LIM Pins*
**Table 8. PWM AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter               | Description                   | Min  | Typ | Max  | Units | Details/Conditions |
|----------|-------------------------|-------------------------------|------|-----|------|-------|--------------------|
| SID140   | T <sub>PWMFREQ</sub>    | Operating frequency           | –    | –   | 48.0 | MHz   | –                  |
| SID141   | T <sub>PWMPWINT</sub>   | Pulse width (internal)        | 42.0 | –   | –    | ns    | –                  |
| SID142   | T <sub>PWMEXT</sub>     | Pulse width (external)        | 42.0 | –   | –    | ns    | –                  |
| SID143   | T <sub>PWMKILLINT</sub> | Kill pulse width (internal)   | 42.0 | –   | –    | ns    | –                  |
| SID144   | T <sub>PWMKILLEXT</sub> | Kill pulse width (external)   | 42.0 | –   | –    | ns    | –                  |
| SID145   | T <sub>PWMEINT</sub>    | Enable pulse width (internal) | 42.0 | –   | –    | ns    | –                  |
| SID146   | T <sub>PWMENEXT</sub>   | Enable pulse width (external) | 42.0 | –   | –    | ns    | –                  |
| SID147   | T <sub>PWMRESWINT</sub> | Reset pulse width (internal)  | 42.0 | –   | –    | ns    | –                  |
| SID148   | T <sub>PWMRESWEXT</sub> | Reset pulse width (external)  | 42.0 | –   | –    | ns    | –                  |

 I<sup>2</sup>C

**Table 9. Fixed I<sup>2</sup>C DC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter         | Description                                 | Min | Typ | Max   | Units | Details/Conditions |
|----------|-------------------|---------------------------------------------|-----|-----|-------|-------|--------------------|
| SID149   | I <sub>I2C1</sub> | Block current consumption at 100 kHz        | –   | –   | 10.5  | μA    | –                  |
| SID150   | I <sub>I2C2</sub> | Block current consumption at 400 kHz        | –   | –   | 135.0 | μA    | –                  |
| SID151   | I <sub>I2C3</sub> | Block current consumption at 1 Mbps         | –   | –   | 310.0 | μA    | –                  |
| SID152   | I <sub>I2C4</sub> | I <sup>2</sup> C enabled in Deep Sleep mode | –   | –   | 1.4   | μA    | –                  |

**Table 10. Fixed I<sup>2</sup>C AC Specifications**

(Guaranteed by Characterization)

| Spec ID# | Parameter         | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153   | F <sub>I2C1</sub> | Bit rate    | –   | –   | 1.0 | Mbps  | –                  |

**Memory**
**Table 11. Flash DC Specifications**

| Spec ID# | Parameter       | Description               | Min | Typ | Max | Units | Details/Conditions |
|----------|-----------------|---------------------------|-----|-----|-----|-------|--------------------|
| SID173   | V <sub>PE</sub> | Erase and program voltage | 1.8 | –   | 5.5 | V     | –                  |

**Table 12. Flash AC Specifications**

| Spec ID# | Parameter                              | Description                                                      | Min   | Typ | Max  | Units   | Details/Conditions             |
|----------|----------------------------------------|------------------------------------------------------------------|-------|-----|------|---------|--------------------------------|
| SID174   | T <sub>ROWWRITE</sub> <sup>[8]</sup>   | Row (block) write time (erase and program)                       | –     | –   | 20.0 | ms      | Row (block) = 128 bytes        |
| SID175   | T <sub>ROWERASE</sub> <sup>[8]</sup>   | Row erase time                                                   | –     | –   | 13.0 | ms      | –                              |
| SID176   | T <sub>ROWPROGRAM</sub> <sup>[8]</sup> | Row program time after erase                                     | –     | –   | 7.0  | ms      | –                              |
| SID178   | T <sub>BULKERASE</sub> <sup>[8]</sup>  | Bulk erase time (32 KB)                                          | –     | –   | 35   | ms      | –                              |
| SID180   | T <sub>DEVPROG</sub> <sup>[8]</sup>    | Total device program time                                        | –     | –   | 7.0  | seconds | Guaranteed by characterization |
| SID181   | F <sub>END</sub>                       | Flash endurance                                                  | 100 K | –   | –    | cycles  | Guaranteed by characterization |
| SID182   | F <sub>RET</sub> <sup>[9]</sup>        | Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles        | 20    | –   | –    | years   | Guaranteed by characterization |
| SID182A  | –                                      | Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles         | 10    | –   | –    | years   | Guaranteed by characterization |
| SID182B  | –                                      | Flash retention. 85 °C < T <sub>A</sub> ≤ 105 °C, 10K P/E cycles | 3     | –   | –    | years   | Guaranteed by characterization |

**System Resources**

Power-on-Reset (POR) with Brown Out

**Table 13. Imprecise Power On Reset (PRES)**

| Spec ID# | Parameter             | Description          | Min  | Typ | Max   | Units | Details/Conditions             |
|----------|-----------------------|----------------------|------|-----|-------|-------|--------------------------------|
| SID185   | V <sub>RISEIPOR</sub> | Rising trip voltage  | 0.80 | –   | 1.45  | V     | Guaranteed by characterization |
| SID186   | V <sub>FALLIPOR</sub> | Falling trip voltage | 0.75 | –   | 1.40  | V     | Guaranteed by characterization |
| SID187   | V <sub>IPORHYST</sub> | Hysteresis           | 15.0 | –   | 200.0 | mV    | Guaranteed by characterization |

**Table 14. Precise Power On Reset (POR)**

| Spec ID# | Parameter              | Description                                | Min  | Typ | Max | Units | Details/Conditions             |
|----------|------------------------|--------------------------------------------|------|-----|-----|-------|--------------------------------|
| SID190   | V <sub>FALLPPOR</sub>  | BOD trip voltage in active and sleep modes | 1.64 | –   | –   | V     | Guaranteed by characterization |
| SID192   | V <sub>FALLDPSLP</sub> | BOD trip voltage in Deep Sleep             | 1.40 | –   | –   | V     | Guaranteed by characterization |

**Note**

8. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
9. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact [customer care@cypress.com](mailto:customer care@cypress.com).

### SWD Interface

**Table 15. SWD Interface Specifications**

| Spec ID | Parameter    | Description                                  | Min            | Typ | Max           | Units | Details/Conditions                    |
|---------|--------------|----------------------------------------------|----------------|-----|---------------|-------|---------------------------------------|
| SID213  | F_SWDCCLK1   | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | –              | –   | 14.0          | MHz   | SWDCLK $\leq$ 1/3 CPU clock frequency |
| SID214  | F_SWDCCLK2   | $1.8\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | –              | –   | 7.0           | MHz   | SWDCLK $\leq$ 1/3 CPU clock frequency |
| SID215  | T_SWDI_SETUP | $T = 1/f\text{ SWDCLK}$                      | $0.25 \cdot T$ | –   | –             | ns    | Guaranteed by characterization        |
| SID216  | T_SWDI_HOLD  | $T = 1/f\text{ SWDCLK}$                      | $0.25 \cdot T$ | –   | –             | ns    | Guaranteed by characterization        |
| SID217  | T_SWDO_VALID | $T = 1/f\text{ SWDCLK}$                      | –              | –   | $0.5 \cdot T$ | ns    | Guaranteed by characterization        |
| SID217A | T_SWDO_HOLD  | $T = 1/f\text{ SWDCLK}$                      | 1              | –   | –             | ns    | Guaranteed by characterization        |

### Internal Main Oscillator

**Table 16. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description                     | Min | Typ | Max    | Units         | Details/Conditions |
|---------|-----------|---------------------------------|-----|-----|--------|---------------|--------------------|
| SID218  | I_IMO1    | IMO operating current at 48 MHz | –   | –   | 1000.0 | $\mu\text{A}$ | –                  |

**Table 17. IMO AC Specifications**

| Spec ID | Parameter    | Description          | Min | Typ   | Max       | Units         | Details/Conditions          |
|---------|--------------|----------------------|-----|-------|-----------|---------------|-----------------------------|
| SID223  | F_IMOTOL1    | Frequency variation  | –   | –     | $\pm 2.0$ | %             | With API-called calibration |
| SID226  | T_STARTIMO   | IMO startup time     | –   | –     | 12.0      | $\mu\text{s}$ | –                           |
| SID229  | T_JITRMSIMO3 | RMS Jitter at 48 MHz | –   | 139.0 | –         | ps            | –                           |

### Internal Low-Speed Oscillator

**Table 18. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description                     | Min | Typ  | Max  | Units         | Details/Conditions             |
|---------|-----------|---------------------------------|-----|------|------|---------------|--------------------------------|
| SID231  | I_ILO1    | ILO operating current at 32 kHz | –   | 0.30 | 1.05 | $\mu\text{A}$ | Guaranteed by characterization |
| SID233  | I_ILOLEAK | ILO leakage current             | –   | 2.0  | 15.0 | nA            | Guaranteed by design           |

**Table 19. ILO AC Specifications**

| Spec ID | Parameter   | Description              | Min  | Typ  | Max  | Units | Details/Conditions             |
|---------|-------------|--------------------------|------|------|------|-------|--------------------------------|
| SID234  | T_STARTILO1 | ILO startup time         | –    | –    | 2.0  | ms    | Guaranteed by characterization |
| SID236  | T_ILODUTY   | ILO duty cycle           | 40.0 | 50.0 | 60.0 | %     | Guaranteed by characterization |
| SID237  | F_ILOTRIM1  | 32-kHz trimmed frequency | 15.0 | 32.0 | 50.0 | kHz   | $\pm 60\%$ with trim           |

## Applications in Detail

Figure 6. Type-C to DisplayPort/Mini-DisplayPort Application Using 35-CSP Package

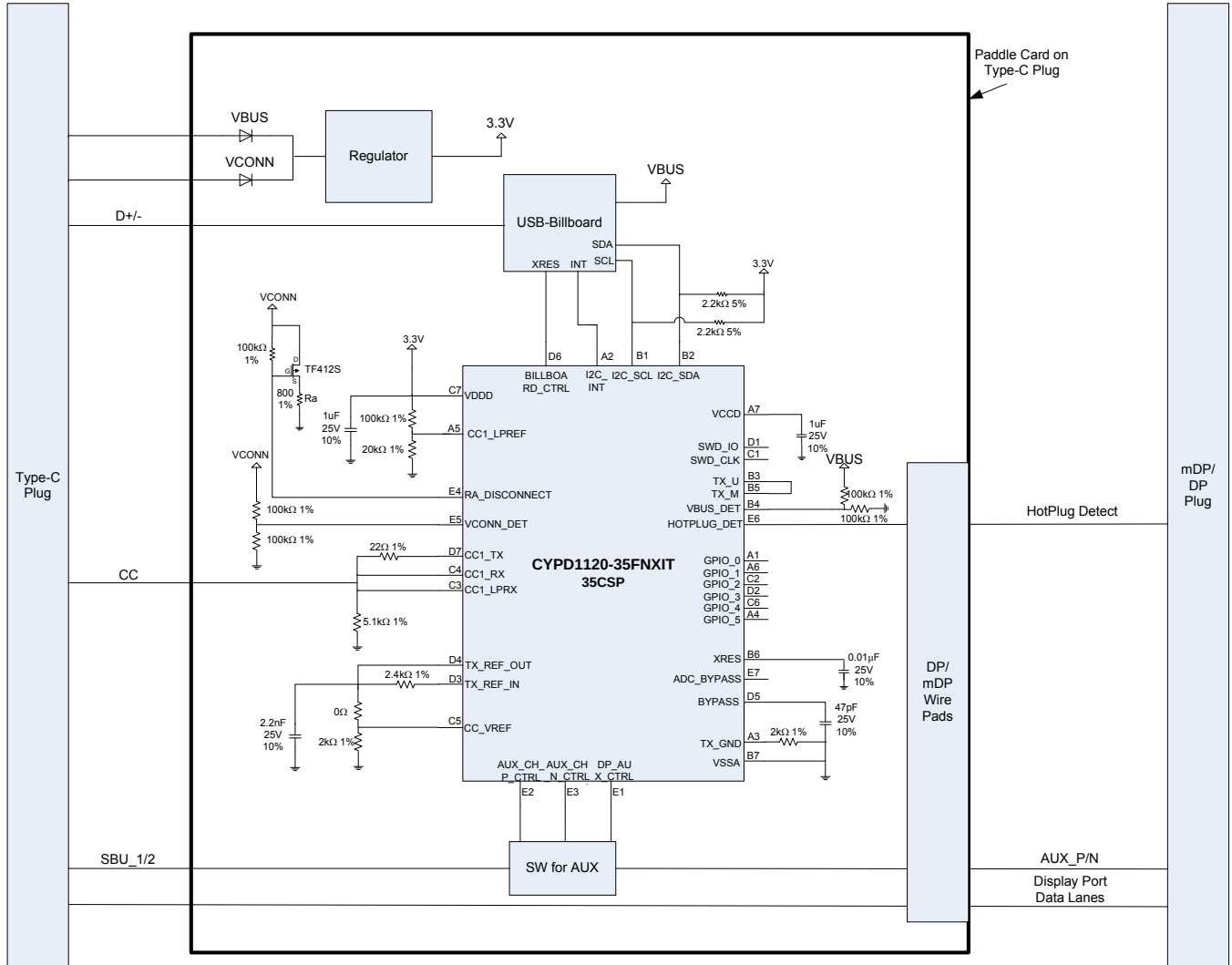
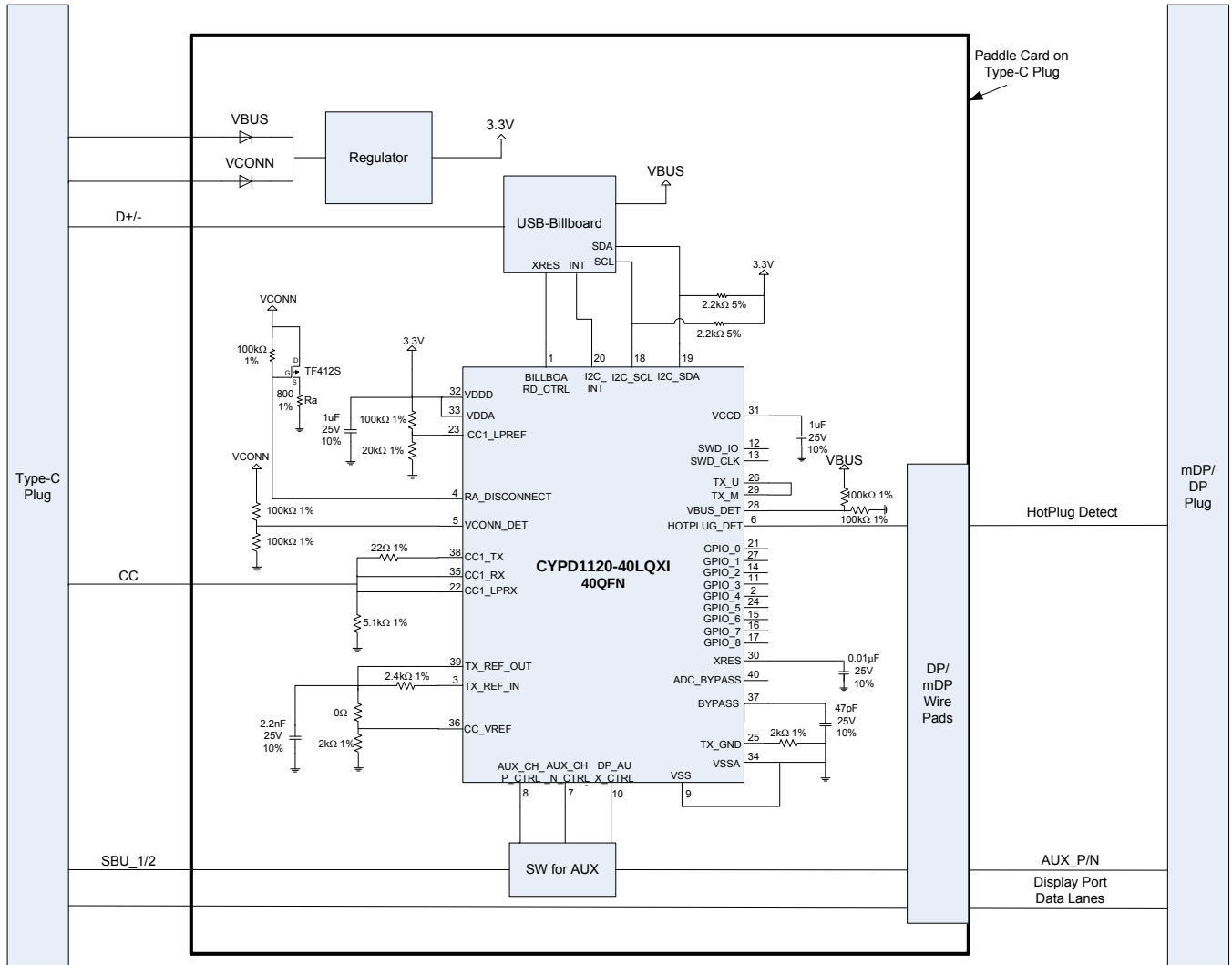
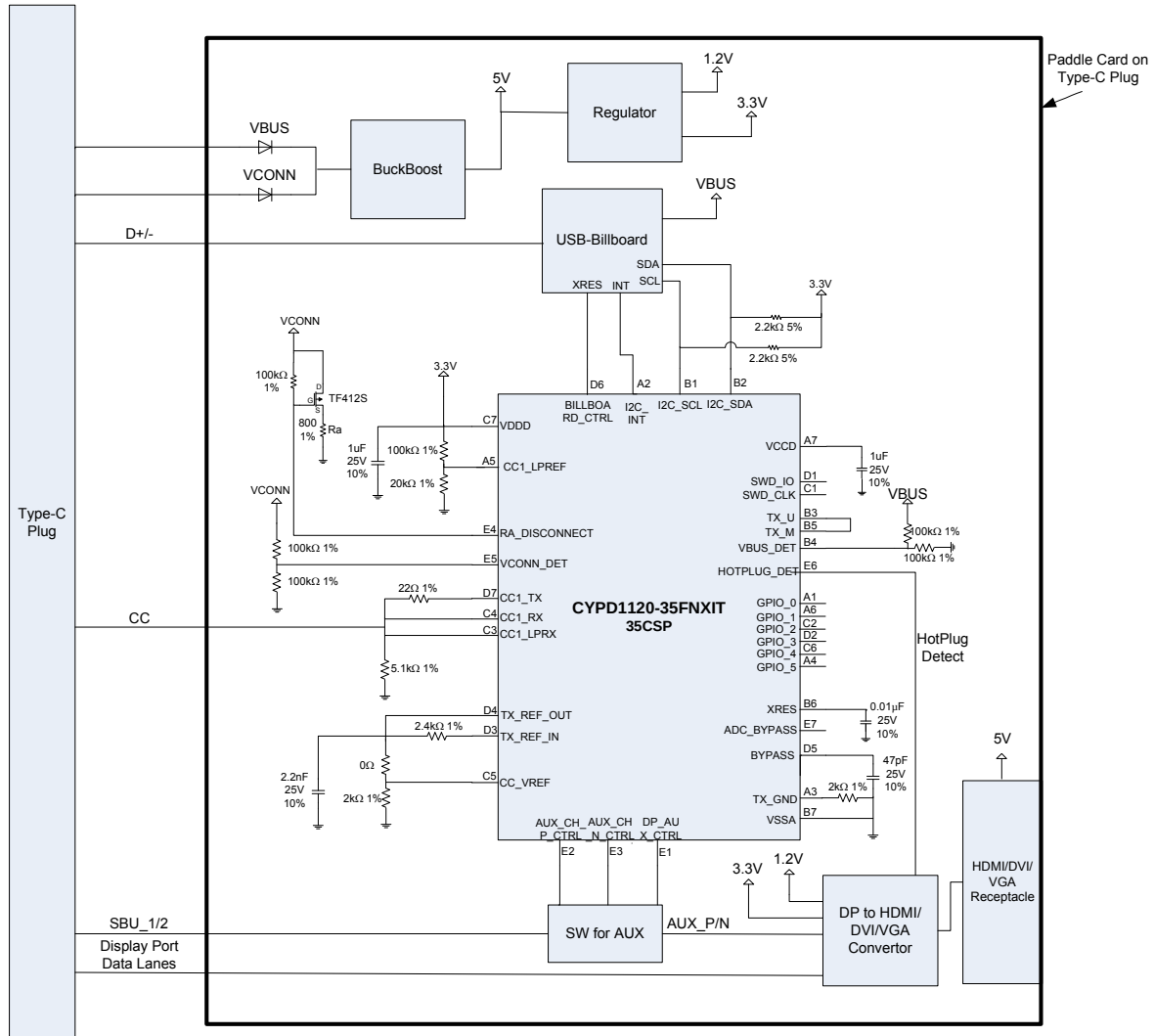


Figure 7. Type-C to DisplayPort/mini-DisplayPort Application Using 40-QFN Package

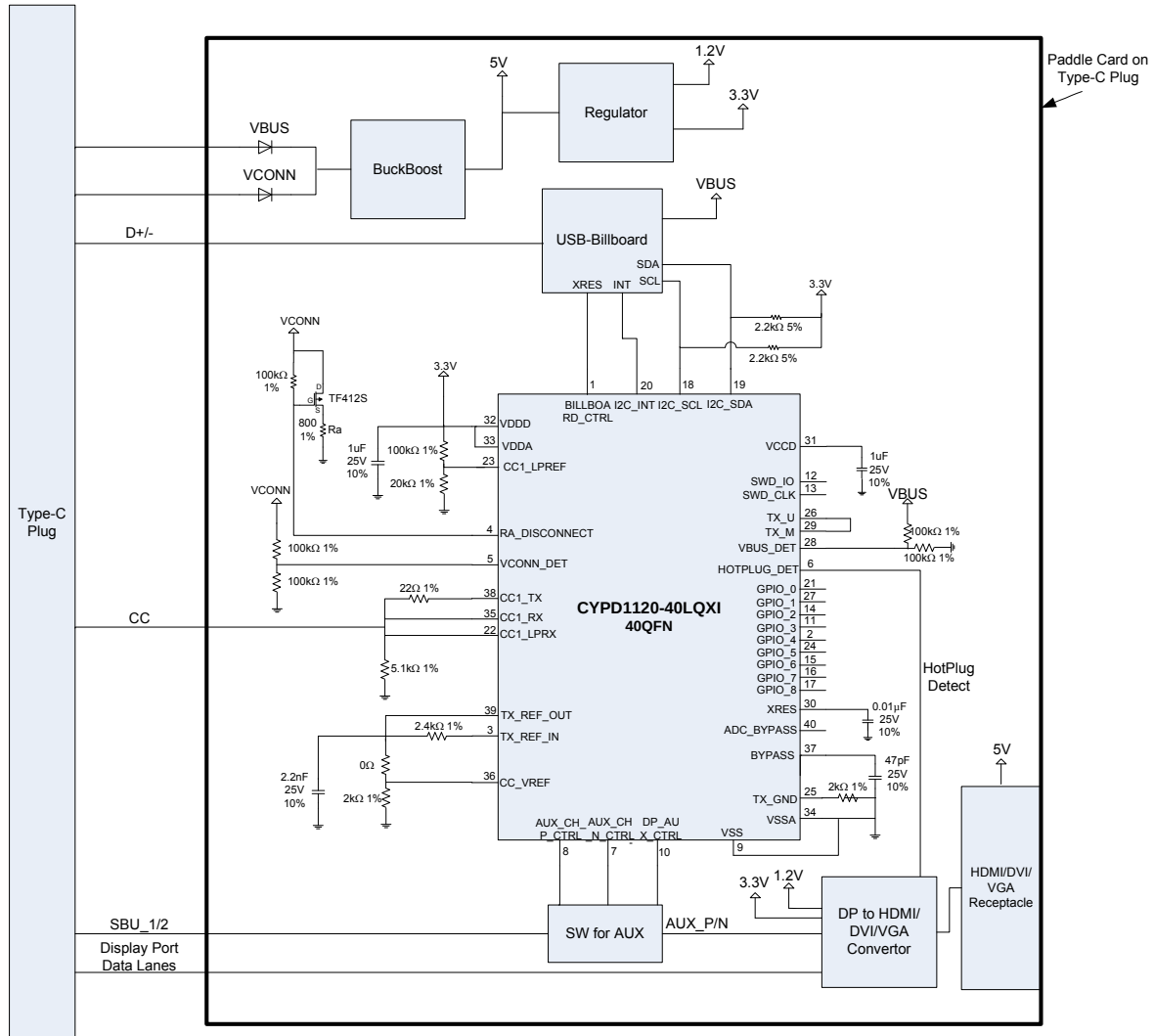


**Figure 8. Type-C to HDMI Application Using 35-CSP Package**





**Figure 9. Type-C to HDMI Application Using 40-QFN Package**



## Ordering Information

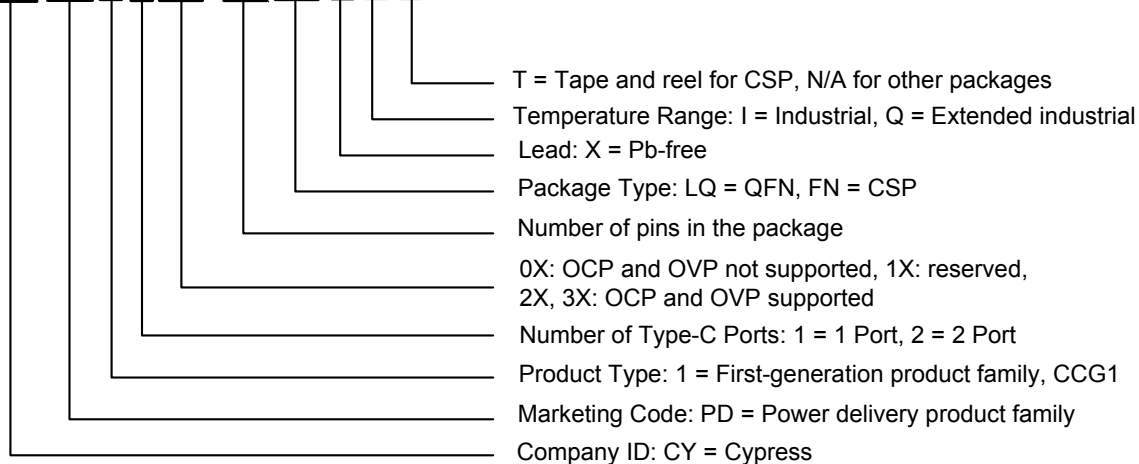
The CCG1 part numbers and features are listed in the following table.

**Table 20. CCG1 Ordering Information**

| Part Number <sup>[10]</sup> | Application                  | Type-C Ports <sup>[11]</sup> | Overcurrent Protection | Overvoltage Protection | Termination Resistor <sup>[12]</sup> | Role <sup>[13]</sup> | Package                  | Si ID |
|-----------------------------|------------------------------|------------------------------|------------------------|------------------------|--------------------------------------|----------------------|--------------------------|-------|
| CYPD1120-35FNXIT            | Type-C to DP, Type-C to HDMI | 1                            | No                     | No                     | R <sub>a</sub> <sup>[14]</sup>       | Cable                | 35-WLCSP <sup>[15]</sup> | 0492  |
| CYPD1120-40LQXI             | Type-C to DP, Type-C to HDMI | 1                            | Yes                    | Yes                    | R <sub>a</sub>                       | DFP <sup>[17]</sup>  | 40-QFN <sup>[16]</sup>   | 0488  |
| CYPD1120-40LQXIT            | Type-C to DP, Type-C to HDMI | 1                            | Yes                    | Yes                    | R <sub>a</sub>                       | DFP <sup>[17]</sup>  | 40-QFN <sup>[16]</sup>   | 0488  |

## Ordering Code Definitions

**CY PD X X XX- XX XX X X X**



### Notes

10. All part numbers support: Input voltage range from 1.8 to 5.5 V. Industrial parts support -40 °C to +85 °C, Extended Industrial parts support -40 °C to 105 °C.
11. Number of USB Type-C Ports Supported .
12. Default V<sub>CONN</sub> Termination.
13. PD Role.
14. Type-C Cable Termination.
15. 35-WLCSP#1 pinout.
16. 40-QFN#3 pinout.
17. Downstream Facing Port.

## Packaging

**Table 21. Package Characteristics**

| Parameter              | Description                        | Conditions | Min | Typ   | Max | Units   |
|------------------------|------------------------------------|------------|-----|-------|-----|---------|
| $T_A$ (40-QFN, 35-CSP) | Operating ambient temperature      | –          | –40 | 25.00 | 85  | °C      |
| $T_J$ (40-QFN, 35-CSP) | Operating junction temperature     | –          | –40 | –     | 100 | °C      |
| $T_{JA}$               | Package $\theta_{JA}$ (40-pin QFN) | –          | –   | 15.34 | –   | °C/Watt |
| $T_{JA}$               | Package $\theta_{JA}$ (35-CSP)     | –          | –   | 28.00 | –   | °C/Watt |
| $T_{JC}$               | Package $\theta_{JC}$ (40-pin QFN) | –          | –   | 02.50 | –   | °C/Watt |

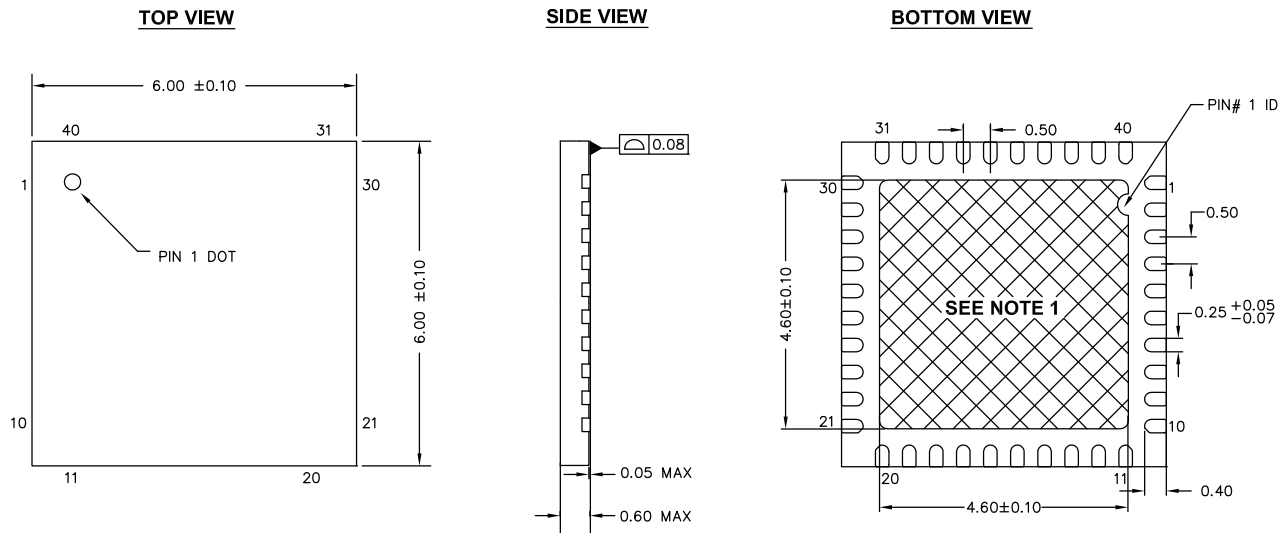
**Table 22. Solder Reflow Peak Temperature**

| Package       | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------------|--------------------------|----------------------------------|
| 40-pin QFN    | 260 °C                   | 30 seconds                       |
| 35-ball WLCSP | 260 °C                   | 30 seconds                       |

**Table 23. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package       | MSL   |
|---------------|-------|
| 40-pin QFN    | MSL 3 |
| 35-ball WLCSP | MSL 1 |

Figure 10. 40-pin QFN Package Outline, 001-80659



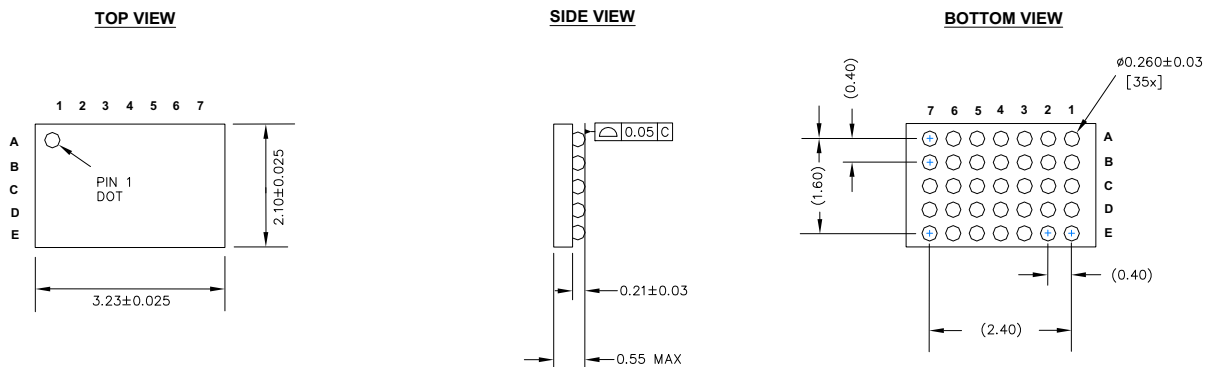
**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 \*A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 11. 35-Ball WLCSP Package Outline, 001-93741



**NOTES:**

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 \*\*

## Acronyms

Table 24. Acronyms Used in this Document

| Acronym                  | Description                                                                     |
|--------------------------|---------------------------------------------------------------------------------|
| ADC                      | analog-to-digital converter                                                     |
| API                      | application programming interface                                               |
| ARM®                     | advanced RISC machine, a CPU architecture                                       |
| CC                       | Configuration Channel                                                           |
| CPU                      | central processing unit                                                         |
| CRC                      | cyclic redundancy check, an error-checking protocol                             |
| CS                       | Current Sense                                                                   |
| DFP                      | Downstream Facing Port                                                          |
| DIO                      | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DP                       | DisplayPort                                                                     |
| EEPROM                   | electrically erasable programmable read-only memory                             |
| EMI                      | electromagnetic interference                                                    |
| ESD                      | electrostatic discharge                                                         |
| FPB                      | flash patch and breakpoint                                                      |
| FS                       | full-speed                                                                      |
| GPIO                     | general-purpose input/output, applies to a PSoC pin                             |
| IC                       | integrated circuit                                                              |
| IDE                      | integrated development environment                                              |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol                             |
| ILO                      | internal low-speed oscillator, see also IMO                                     |
| IMO                      | internal main oscillator, see also ILO                                          |
| I/O                      | input/output, see also GPIO, DIO, SIO, USBIO                                    |
| LVD                      | low-voltage detect                                                              |
| LVTTL                    | low-voltage transistor-transistor logic                                         |
| MCU                      | microcontroller unit                                                            |
| NC                       | no connect                                                                      |
| NMI                      | nonmaskable interrupt                                                           |
| NVIC                     | nested vectored interrupt controller                                            |

Table 24. Acronyms Used in this Document (continued)

| Acronym | Description                                                            |
|---------|------------------------------------------------------------------------|
| opamp   | operational amplifier                                                  |
| OCP     | Overcurrent protection                                                 |
| OVP     | Overvoltage protection                                                 |
| PCB     | printed circuit board                                                  |
| PGA     | programmable gain amplifier                                            |
| PHY     | physical layer                                                         |
| POR     | power-on reset                                                         |
| PRES    | precise power-on reset                                                 |
| PSoC®   | Programmable System-on-Chip™                                           |
| PWM     | pulse-width modulator                                                  |
| RAM     | random-access memory                                                   |
| RISC    | reduced-instruction-set computing                                      |
| RMS     | root-mean-square                                                       |
| RTC     | real-time clock                                                        |
| RX      | receive                                                                |
| SAR     | successive approximation register                                      |
| SCL     | I <sup>2</sup> C serial clock                                          |
| SDA     | I <sup>2</sup> C serial data                                           |
| S/H     | sample and hold                                                        |
| SPI     | Serial Peripheral Interface, a communications protocol                 |
| SRAM    | static random access memory                                            |
| SWD     | serial wire debug, a test protocol                                     |
| TX      | transmit                                                               |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UFP     | Upstream Facing Port                                                   |
| USB     | Universal Serial Bus                                                   |
| USBIO   | USB input/output, PSoC pins used to connect to a USB port              |
| VESA    | Video Electronics Standards Association                                |
| XRES    | external reset I/O pin                                                 |

## Document Conventions

### Units of Measure

Table 25. Units of Measure

| Symbol | Unit of Measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msps   | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |
| μs     | microsecond            |
| μV     | microvolt              |
| μW     | microwatt              |
| mA     | milliampere            |
| ms     | millisecond            |
| mV     | millivolt              |
| nA     | nanoampere             |
| ns     | nanosecond             |
| Ω      | ohm                    |
| pF     | picofarad              |
| ppm    | parts per million      |
| ps     | picosecond             |
| s      | second                 |
| sps    | samples per second     |
| V      | volt                   |

**Revision History**

| Description Title: CYPD1120 Datasheet USB Power Delivery Alternate Mode Controller on Type-C<br>Document Number: 001-96786 |         |                 |                 |                                                                  |
|----------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|------------------------------------------------------------------|
| Revision                                                                                                                   | ECN     | Orig. of Change | Submission Date | Description of Change                                            |
| **                                                                                                                         | 4686071 | VGT             | 05/13/2015      | New datasheet                                                    |
| *A                                                                                                                         | 4829889 | VGT             | 07/20/2015      | Added CYPD1120-40LQXIT in <a href="#">Ordering Information</a> . |

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С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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