ATA5780N

UHF ASK/FSK Receiver

SUMMARY DATASHEET

Features

- Atmel® ATA5780N UHF receiver is compatible with Atmel ATA5830N transceiver
- Supported frequency ranges
  - Low-band 310MHz to 318MHz, 418MHz to 477MHz
  - High-band 836MHz to 928MHz
  - 315.00MHz/433.92MHz/868.30MHz and 915.00MHz with one 24.305MHz crystal
- Low current consumption
  - 9.3mA for RXMode (low-band) 480µA for 50ms cycle 3 channel polling
- Max OFFMode current of 5µA at Vs = 5.5V and T = 105°C)
- Input 1dB compression point
  - –35dBm (Full Sensitivity Level)
  - –20dBm (15dB reduced Sensitivity)
- Programmable channel frequency with fractional-N PLL
  - 93Hz resolution for low-band
  - 185Hz resolution for high-band
- FSK deviation ±0.375kHz to ±93kHz
- FSK sensitivity (Manchester coded) at 433.92MHz
  - –106dBm at 20Kbit/s, Δf = ±20kHz, BW_{IF} = 165kHz
  - –109dBm at 10Kbit/s, Δf = ±10kHz, BW_{IF} = 165kHz
  - –112dBm at 5Kbit/s, Δf = ±5kHz, BW_{IF} = 165kHz
  - –121dBm at 0.75Kbit/s, Δf = ±0.75kHz, BW_{IF} = 25kHz
- ASK Sensitivity (Manchester Coded) at 433.92MHz
  - –107dBm at 20Kbit/s, BW_{IF} = 366kHz
  - –117dBm at 1Kbit/s, BW_{IF} = 366kHz
- Programmable RX-IF bandwidth 25kHz to 366kHz (approximately 10% steps)
- Blocking (BW_{IF} = 165kHz): 64dBC at frequency offset = 1MHz and 48dBC at 225kHz
- High image rejection 55dB (315MHz/433.92MHz) 47dB (868.3MHz/915MHz) without calibration
- Supported buffered data rate 0.5Kbit/s to 20Kbit/s (higher data rates up to 80Kbit/s Manchester coded and 160Kbit/s NRZ with transparent output)
- Supports pattern based wake-up and start of frame identification
- Digital RSSI with very high relative accuracy of ±1dB due to digitized IF processing

This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

- Programmable clock output derived from crystal frequency
- 512 byte EEPROM data memory for receiver configuration
- SPI interface for data access and receiver configuration
- Configurable EVENT signal indicates the status of the IC
- Automatic low power channel polling (three RKE channels, TPMS, RS)
- ID scanning up to 18 different IDs with 1..4 byte
- Supply voltage ranges 1.9V to 3.6V and 4.5V to 5.5V
- Temperature range –40°C to +105°C
- ESD protection at all pins (±4kV HBM, ±200V MM, ±750V FCDM)
- Small 5mm × 5mm QFN32 package/pitch 0.5mm
- Suitable for applications governed by EN 300 220 and FCC part 15, title 47

1. General Product Description

1.1 Overview

The Atmel® ATA5780N is a highly integrated, low power UHF ASK/FSK receiver fully compatible with the Atmel ATA5830N transceiver, except that it provides no transmit path and no Flash for the AVR® controller. The Atmel ATA5780N is partitioned into several sections; an RF frontend, a digital baseband, and a low power 8-bit AVR microcontroller with Atmel ATA5830N compatible ROM firmware for control. The product is designed for the ISM frequency bands in the ranges of 310MHz to 318MHz, 418MHz to 477MHz and 836MHz to 928MHz. External part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. It uses a low-IF architecture with an integrated double quadrature receiver and digitized IF processing. This results in high image rejection and excellent blocking performance. In addition, the highly flexible and configurable baseband signal processing allows the receiver to operate in several scanning, wake-up and automatic self polling scenarios. For example, during polling the IC can seek certain message content (IDs) and save valid telegram data in the FIFO buffer for later retrieval. The device possess two receive paths that enable parallel search for two telegrams with different modulations, data rates, wake-up conditions, etc. The highly configurable and autonomous scanning capability enables polling of up to five application channels such as 3-channel RKE, TPMS, PEG. The configuration of the receiver is stored in a 512 byte EEPROM. The SPI allows for external control and reconfiguration of the devices.

1.2 Target Applications

The receiver is designed to be used in the following application areas:

- Remote Keyless Entry System (RKE)
- Passive Entry Go System (PEG)
- Tire Pressure Monitoring System (TPM, TPMS)
- Remote Start System (RS)
- Remote Control System, e.g., garage door open
- Smart RF applications
- Telemetering Systems

Three applications with a total of five channels are supported by the Atmel firmware for autonomous self polling.

1.3 Main Extended Features of the Atmel ATA5780N

1.3.1 RF Performance

The Atmel ATA5780N provides high sensitivity, high image rejection and outstanding blocking performance enable a robust application against interferer with a low cost design. In addition, the programmable channel filter bandwidth provides flexibility to adapt to various system requirements.

1.3.2 Automatic Self Polling and Multi Channel Capability

The autonomous self polling supports the automatic scanning for three different applications such as Remote Keyless Entry (RKE), Tire Pressure Monitoring System (TPMS) and Remote Start (RS) using one IC. Additionally multi channel systems with up to three frequencies can be scanned. This means five frequencies can be scanned in the autonomous polling scheme; three for RKE, one for TPMS and one for RS. The configuration of each application is independent of the others. This is possible because of the flexibility in the digital baseband and two different baseband receiving paths. The IC can immediately scan all applications upon power-up without the need for any initial configuration by an external microcontroller.

1.3.3 Wake-up Scenario and ID Scanning

The powerful baseband signal processing is designed to offload these time consuming tasks from the host controller. This allows the transceiver to discard unwanted telegrams and limit external microcontroller wake-up to valid telegrams only. Up to seven criteria can be used to determine the telegram validity from carrier check on the lowest level to start of frame ID pattern match at the highest level.

1.3.4 Two Parallel Receiving Paths

The receiver's baseband contains two data paths. The parameters of both paths can be set differently, e.g., the modulation type or data rate. Generally both paths are working simultaneously but only the first path detecting a valid telegram will be used for further data reception and filling of the 32 byte buffer. The 32 byte receive data buffer can be accessed using SPI commands from the external host microcontroller.

1.3.5 ROM Firmware

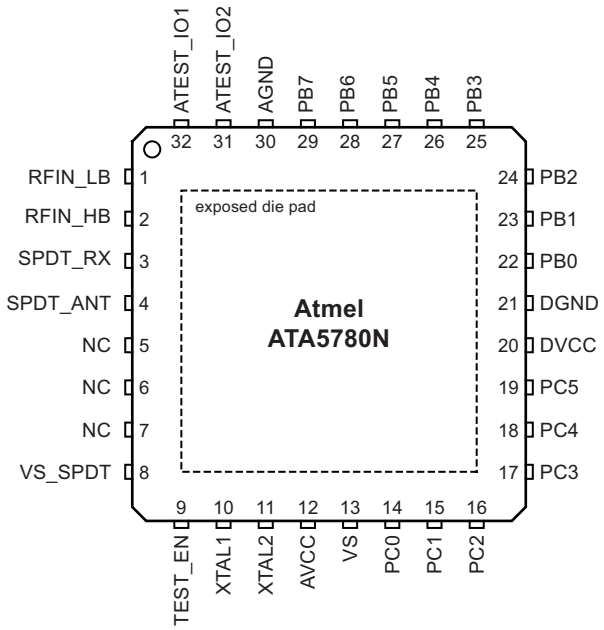
All the functionality is implemented with 24KB ROM firmware and controlled by SPI commands.

1.3.6 EEPROM Configuration

The configuration of the device e.g., RF-frequency, modulation type, data rate, etc. is stored in 512byte of EEPROM that is integrated within the Atmel® ATA5780N. This improves the efficiency of the SPI control since most of the configuration comes from the EEPROM. In most applications, only the received data and short SPI commands are required. The device is delivered with a standard configuration; only deviations from that need to be configured. Device configuration uses only a part of the 512byte of EEPROM leaving free space available for additional customer data storage. A modification of the EEPROM content is only allowed during IDLEMode.

1.4 Pin Diagram and Configuration of Atmel ATA5780N

Figure 1-1. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 1-1. Pin Configuration

Pin No.	Pin Name	Type	Description
1	RFIN_LB	Analog	RXMode, LNA input for Low-Band frequency range (< 500MHz)
2	RFIN_HB	Analog	RXMode, LNA input for High-Band frequency range (> 500MHz)
3	SPDT_RX	Analog	RXMode output of the SPDT switch (Damped signal output)
4	SPDT_ANT	Analog	Antenna input (RXMode) of the SPDT switch
5-7	NC	-	Open in application
8	VS_SPDT	Analog	SPDT supply 3V application supply voltage input
9	TEST_EN	-	Test enable, connected to GND in application
10	XTAL1	Analog	Crystal oscillator pin1 (Input)
11	XTAL2	Analog	Crystal oscillator pin2 (output)
12	AVCC	Analog	RF frontend supply regulator output
13	VS	Analog	Main supply voltage input
14	PC0	Digital	Main: AVR Port C0 Alternate: PCINT8/NRESET/Debug Wire
15	PC1	Digital	Main: AVR Port C1 Alternate: NPWRON1/PCINT9
16	PC2	Digital	Main: AVR Port C2 Alternate: NPWRON2/PCINT10/TRPA
17	PC3	Digital	Main: AVR Port C3 Alternate: NPWRON3/PCINT11/TMDO/TxD

Table 1-1. Pin Configuration (Continued)

Pin No.	Pin Name	Type	Description
18	PC4	Digital	Main: AVR Port C4 Alternate: NPWRON4/PCINT12/INT0/ TMDI/RxD
19	PC5	Digital	Main: AVR Port C5 Alternate: NPWRON5/PCINT13/TRPB/ TMDO_CLK
20	DVCC	-	Digital supply voltage regulator output
21	DGND	-	Digital ground
22	PB0	Digital	Main: AVR Port B0 Alternate: PCINT0/CLK_OUT
23	PB1	Digital	Main: AVR Port B1 Alternate: PCINT1 / SCK
24	PB2	Digital	Main: AVR Port B2 Alternate: PCINT2/MOSI (Master Out Slave In)
25	PB3	Digital	Main: AVR Port B3 Alternate: PCINT3/MISO (Master In Slave Out)
26	PB4	Digital	Main: AVR Port B4 Alternate: PWRON/PCINT4/LED1 (strong high side driver)
27	PB5	Digital	Main: AVR Port B5 Alternate: PCINT5/NSS
28	PB6	Digital	Main: AVR Port B6 Alternate: PCINT6/EVENT (firmware controlled external microcontroller event flag)
29	PB7	Digital	Main: AVR Port B7 Alternate: NPWRON6/PCINT7/ RX_ACTIVE (strong high side driver)/ LED0 (strong low side driver)
30	AGND	-	Analog ground
31	ATEST_IO2	-	RF frontend test input/output 2, connected to GND in application
32	ATEST_IO1	-	RF frontend test input/output 1, connected to GND in application
	GND	-	Ground/Backplane on exposed die pad

1.5 Typical Application Circuits

Figure 1-2. Typical 5V Application Circuit

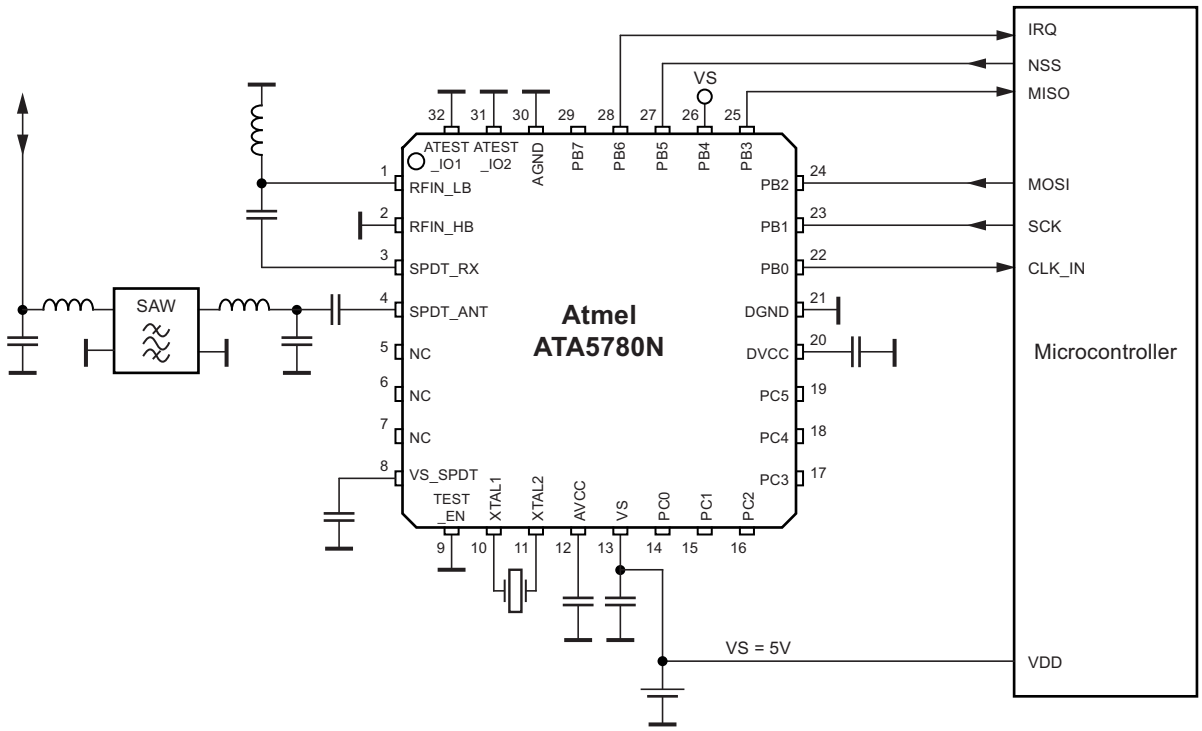


Figure 1-2 shows the typical application circuit with an external host microcontroller running from a 5V supply. For a 3V application VS and VS_SDPT have to be shorted. The pin PB4 (PWRON) is directly connected to VS and the Atmel® ATA5780N enters the IDLEMode after power-on. The Atmel ATA5780N can work autonomously while the microcontroller stays powered down to achieve low current consumption while being sensitive to RF telegrams.

To achieve low current in IDLEMode the Atmel ATA5780N can be configured in the EEPROM to work with the 125kHz RC oscillator (this mode is named IDLEMode(RC)). The Atmel ATA5780N can also be configured for autonomous multi channel and multi application PollingMode(RC). The external microcontroller is notified with IRQ if an appropriate RF message is received. Until that takes place, the Atmel ATA5780N periodically switches to RXMode, checks the different channels and applications configured in the EEPROM and returns to the IDLEMode(RC) all the while with the external host AVR® microcontroller in a deep sleep mode to achieve a low average current while being polling for valid RF messages. Once a valid RF message is detected, it can be buffered within the Atmel ATA5780N to allow the microcontroller time to wake-up and retrieve the buffered data.

RF_IN is matched to SPDT_RX by absorbing the parasitics of the SPDT switch into the matching network, hence the SPDT_ANT is a 50Ω port. The impedance of the SAW filter is transformed with LC matching circuits to the SPDT_ANT port and also to the antenna to the SAW. An external crystal, together with the fractional-N PLL within the Atmel® ATA5780N is used to fix the RX frequency. Accurate load capacitors for this crystal are integrated, to reduce system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS_SPDT and VS of the Atmel ATA5780N. The exposed die pad is the RF and analog ground of the Atmel ATA5780N. It is directly connected to AGND via a fused lead. For applications operating in the 868.3MHz or 915MHz frequency bands, a High-Band RF input is supplied, RFIN_HB, and must be used instead of RFIN_LB.

The Atmel ATA5780N is controlled using specific SPI commands via the SPI interface and an internal EEPROM for application specific configuration.

This application is compatible to the Atmel ATA5830N, therefore, the same application board can be used for both devices, just the population of the TX path is not populated for Atmel ATA5780N.

1.6 System Overview

Figure 1-3. Circuit Overview

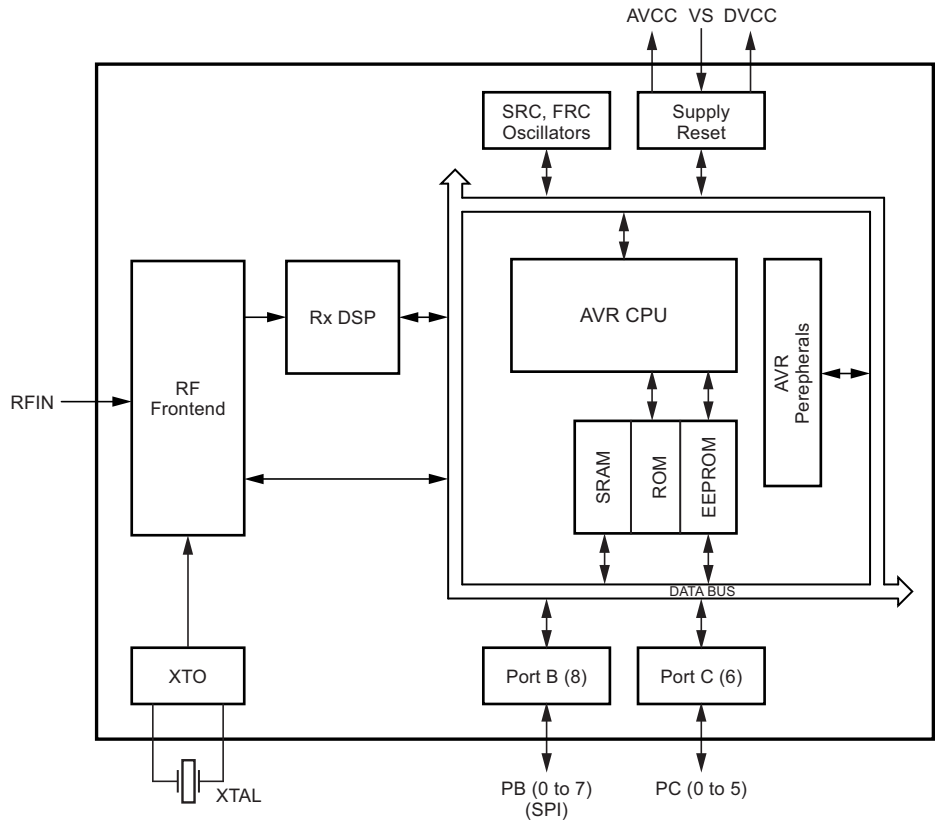


Figure 1-3 on page 8 shows an overview of the main functional blocks of the Atmel® ATA5780N. The control of the Atmel ATA5780N is performed through the SPI pins SCK, MOSI, MISO and NSS found on port B. The configuration of the Atmel ATA5780N is stored in the EEPROM and a large part of the functionality is defined with the firmware located in the ROM and processed using the AVR®. A SPI command like “Start RXMode” uses the information located in the EEPROM, configures all hardware registers of the different blocks according to this information, starts then the RXMode and directs the received data to the Rx Buffer located in the SRAM. An EVENT on port PB6 is signaled to the external microcontroller when the expected number of bytes is received.

Part of the EEPROM content is copied to the SRAM during start-up of the Atmel ATA5780N for faster access. Care should be taken to limit EEPROM R/W cycles so that the device’s maximum rating is not exceeded. Alternatively, the user should consider modifying the parameters in the SRAM. It is important to note that PWRON and NPWRON pins are active in OFFMode. This means that even if the ATA5780N is in OFFMode and the DVCC voltage is switched off, power management circuitry within the Atmel ATA5780N will bias these pins with VS.

AVR ports can be used as external LNA supply voltage (RX_ACTIVE), LED driver, event pins, switching control for additional SPDT switches, general purpose digital inputs and outputs, wake-up inputs etc. Some functionality of these ports is already implemented in the firmware and can be activated with EEPROM configuration. Other functionality is possible through the “Write/Read SRAM/Registers” SPI command.

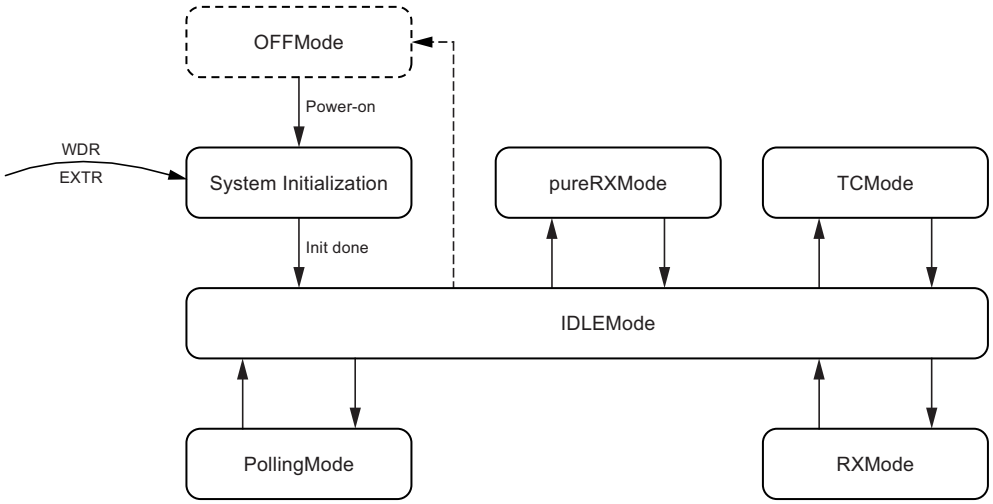
1.7 Compatibility to the Atmel UHF Transceiver ATA5830N

The Atmel® receiver ATA5780N is pin compatible to the Atmel transceiver ATA5830N. The receiver has the identical RX performance of the transceivers RX path. The difference exists in the digital block only. While extremely flexible, the receiver operates as a ROM programmed statemachine. Its functionality is limited to user selectable EEPROM configuration options. As a result, the receiver is fully compatible with the transceiver, but without the flexibility of 6KB Flash program space for custom applications.

2. System Operation Modes

The scope of this section is to give an overview of the Atmel® ATA5780N supported operation modes, shown in Figure 2-1.

Figure 2-1. Operation Modes Overview



After connecting the supply voltage to the VS pin, the Atmel ATA5780N always starts in OFFMode. All internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. The Atmel ATA5780N can be woken up by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After firmware initialization the Atmel ATA5780N reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operation modes. There are two options of the IDLEMode to be configured in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the Fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high accuracy clock output or timing measurements

The receive mode (RXMode) provides data reception on one of the preconfigured channels. The precondition for data reception is a valid preamble. The receiver is continuously searching for a valid telegram and receives the data if all preconfigured checks are successfully passed. The RXMode is usually enabled by SPI command, or directly after power-on, when selected in the EEPROM setting.

In PollingMode the receiver is activated for a short period of time to check for a valid telegram on the selected channels. The receiver will be deactivated if no valid telegram is found and a sleep period with very low power consumption elapses. This process is repeated periodically according to the EEPROM configuration. Up to five channels and a wide range of sleep times are supported by the Atmel firmware. This mode is activated via an SPI command, or directly after power-on, when selected in the EEPROM setting.

The tune and check mode (TCMode) offers a calibration and self-checking functionality for the VCO and FRC oscillators as well as for the polling cycle accuracy. This mode is activated via an SPI command. When selected in the EEPROM settings the TCMode is used during system initialization after power-on. Furthermore, the TCMode can be activated periodically during PollingMode.

Table 2-1 shows the relations between the operation modes and its corresponding power supplies, clock sources and sleep mode settings.

Table 2-1. Operation Modes versus Supplies and Oscillators

Operation Mode	AVR Sleep Mode	DVCC	AVCC	VS_SPDT	XTO	SRC	FRC
OFFMode	-	off	off	off	off	off	off
IDLEMode(RC)	Active mode	on	off	off	off	on	on
	Power-down(1)		off	off	off	on	off
IDLEMode(XTO)	Active mode		on	off	on	on	off
	Power-down(1)		on	off	on	on	off
RXMode	Active mode		on	off	on	on	off
PollingMode(RC)							
- Active Period	Active mode		on	off	on	on	on
- Sleep Period	Power-down(1)		off	off	off	on	off
PollingMode(XTO)							
- Active Period	Active mode		on	off	on	on	off
- Sleep Period	Power-down(1)		on	off	on	on	off

Notes:
1. During IDLEMode(RC) and IDLEMode(XTO) the AVR microcontroller will enter a sleep mode to reduce the current consumption. The sleep mode of the microcontroller section can be defined in the EEPROM. To achieve the optimum current consumption the power-down mode is recommended.
2. Only activated at 5V applications. This is selectable in the EEPROM setting.

3. Hardware Description

3.1 Overview

Figure 3-1. System Block Diagram

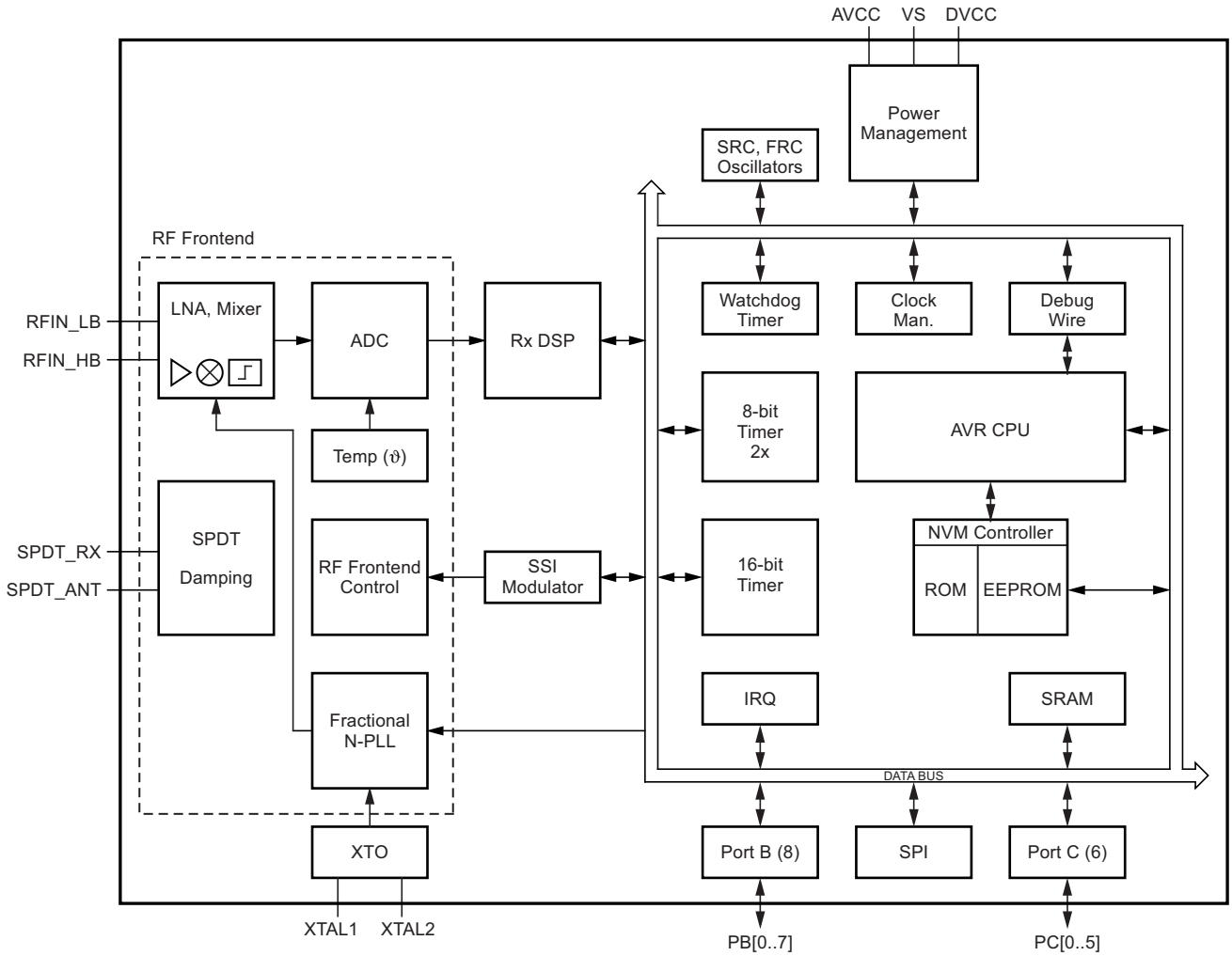


Figure 3-1 shows the system block diagram of Atmel® ATA5780N.

In RXMode the crystal oscillator (XTO) together with the fractional-N PLL generates the local oscillator (LO) signal. The RF signal coming either from the Low-Band input (RFIN_LB) or High Band input (RFIN_HB) is amplified by the Low Noise Amplifier (LNA) and down converted by the mixer to the Intermediate Frequency (IF) using the LO signal. Afterwards the IF signal is sampled using a high resolution a Analog to Digital Converter (ADC).

Within the RX Digital Signal Processing (RxDSP) the received signal from the ADC is filtered by a digital channel filter and demodulated. Two data receive paths are included into the RxDSP after the digital channel filter. The receive path can also be configured to provide the digital output of an internal temperature sensor (Temp( )).

The Single Pole Double Throw (SPDT) switch is used together with Atmel ATA5780N to have a ATA5830N compatible PCB layout and to use the integrated damping in the case of strong blockers.

The system is controlled by an AVR® CPU with 24KB ROM, 512 byte EEPROM, 768 byte SRAM and other peripherals supporting the receiver handling. Two ports PB[0..7] and PC[0..5] are available for external digital connections, e.g., the SPI interface is connected to port B. The Atmel® ATA5780N is controlled by EEPROM configuration and SPI commands. The functional behavior is mainly determined by the firmware in the ROM. It can be configured to a high degree by modifying the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality of the Atmel ATA5780N. The RXDSP registers are directly accessible from the AVR since these DSP's are directly connected to the AVR data bus. The RF frontend registers are programmed with an on chip serial interface (SSI) accessing the RF frontend control.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages VS, AVCC and DVCC of the Atmel ATA5780N. In OFFMode all the supply voltages AVCC and DVCC are switched off to achieve a very low current consumption. The Atmel ATA5780N can be powered up by activating the PWRON pin or one of the NPWRON1..6 pins since they are still active in OFFMode.

The RF frontend circuits and the XTO are connected to AVCC, the AVCC domain can be switched on and off independently from DVCC.

The Atmel ATA5780N provides two idle modes. In IDLEMode(RC) only the DVCC voltage regulator, the FRC- and SRC-oscillators are active and the AVR uses a power down mode to achieve a low current consumption. The same power-down mode can be used during the inactive phases of the PollingMode. In IDLEMode(XTO) the AVCC voltage domain as well as the XTO are activated additionally.

An integrated watchdog timer is available to restart the Atmel ATA5780N.

3.2 Receive Path

3.2.1 Overview

The receive path consists of a Low Noise Amplifier (LNA), mixer, Analog-to-Digital Converter (ADC) and a Rx Digital Signal Processor (DSP) as shown in Figure 3-1 on page 11. The fractional-N phase locked loop (PLL) and the quartz oscillator (XTO) described above delivers the local oscillator frequency f_{LO} in RXMode. The receive path is controlled wit the RF frontend registers.

Two separate LNA inputs, one for Low-Band and one for High-Band, are provided to obtain optimum performance matching for each frequency range and to allow multi band applications. A Radio Frequency (RF) level detector at the LNA output and a switchable damping included into Single-Pole Double-Trough (SPDT) switch is used in the presence of large blockers to achieve better system blocking performance.

The mixer converts the received RF signal to a low Intermediate Frequency (IF) of about 250kHz. A double quadrature architecture is used for the mixer to achieve high image rejection. Additionally, the 3rd order suppression of Local Oscillator (LO) harmonic receiving will make receiving without a frontend SAW filter, for example in a car keyfob application, less critical.

The ADC converts the IF signal into the digital domain. Due to the high effective resolution (14 bit) of the used ADC the channel filter and RSSI can be realized in the digital signal domain and no Analog Gain Control (AGC) which can lead to critical timing issues or analog filtering is required in front of the ADC. This leads to a receiver frontend with good blocking performance up to the 1dB compression point of the LNA and mixer, and a steep digital channel filter can be used.

The Rx DSP performs channel filtering and converts the digital output signals of the ADC to the baseband for demodulation. Due to the digital realization of these functions the Rx DSP can be adapted to the needs of many different applications since channel bandwidth, data rate, modulation type, wake-up criteria, signal checks, clock recovery and many other properties are configurable. See Rx DSP description in Section 3.2.2 "RX Digital Signal Processing (Rx DSP)" on page 13.

A Received Signal Strength Indicator (RSSI) value is built within the Rx DSP completely in the digital signal domain allowing for a high relative RSSI accuracy and a good absolute accuracy, which is only deteriorated by the gain errors of LNA, mixer and ADC.

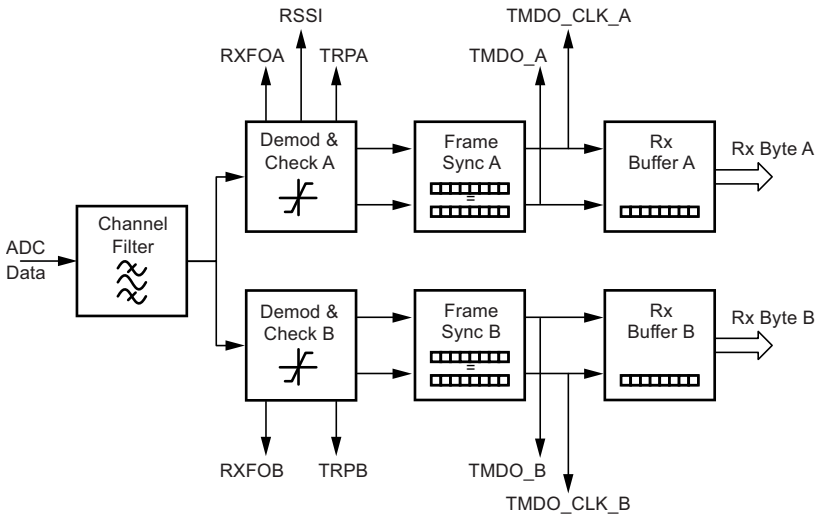
Two independent receive paths A and B are integrated in the Rx DSP after the channel filter see Section 3.2.2 "RX Digital Signal Processing (Rx DSP)" on page 13 and allow the use of different data rate, modulation type and protocol without the need to power-up the receive path more than once to decide which signal should be received. This allows a much lower polling current in several applications.

The integration of Remote Keyless Entry (RKE), Passive Entry Go (PEG) and Tire Pressure Monitoring systems (TPM) into one module is simplified since completely different protocols can be supported and a low polling current is achieved. It is even possible using different receive RF bands for different applications by using the two LNA inputs. For example a TPM receiver can be realized at 433.92MHz while a PEG system uses the 868MHz ISM band.

3.2.2 RX Digital Signal Processing (Rx DSP)

The Rx DSP block performs the digital signal processing, decoding and checking of the Rx samples from the ADC. It delivers the raw data at the TRPA/B pins, the decoded data at the TMDO output and the buffered data bytes (Rx byte A/B) from the Rx buffer. It also provides auxiliary information about the signal like the Received Signal Strength Indication (RSSI) and the frequency offset of the received signal versus the selected center frequency (RXFOA/B).

Figure 3-2. Rx DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B. Therefore, it has to be configured to be suitable for both. The receiving paths A and B are identical and consist of an ASK/FSK demodulator with attached signal checks, a frame synchronizer supporting pattern based search for the telegram start and a 1 byte hardware buffer for received data.

The receiver architecture with parallel receiving paths A and B allows for a simultaneous search for two different transmitters. The simultaneous search is supported only when the flexible telegram support is enabled (see EEPROM description).

E.g., path A can be configured for an ASK telegram with high data rate and path B can be configured for an FSK telegram with low data rate. During PollingMode both settings are applied and the check occurs simultaneously. This results in a shorter active time during polling.

3.3 Power Management

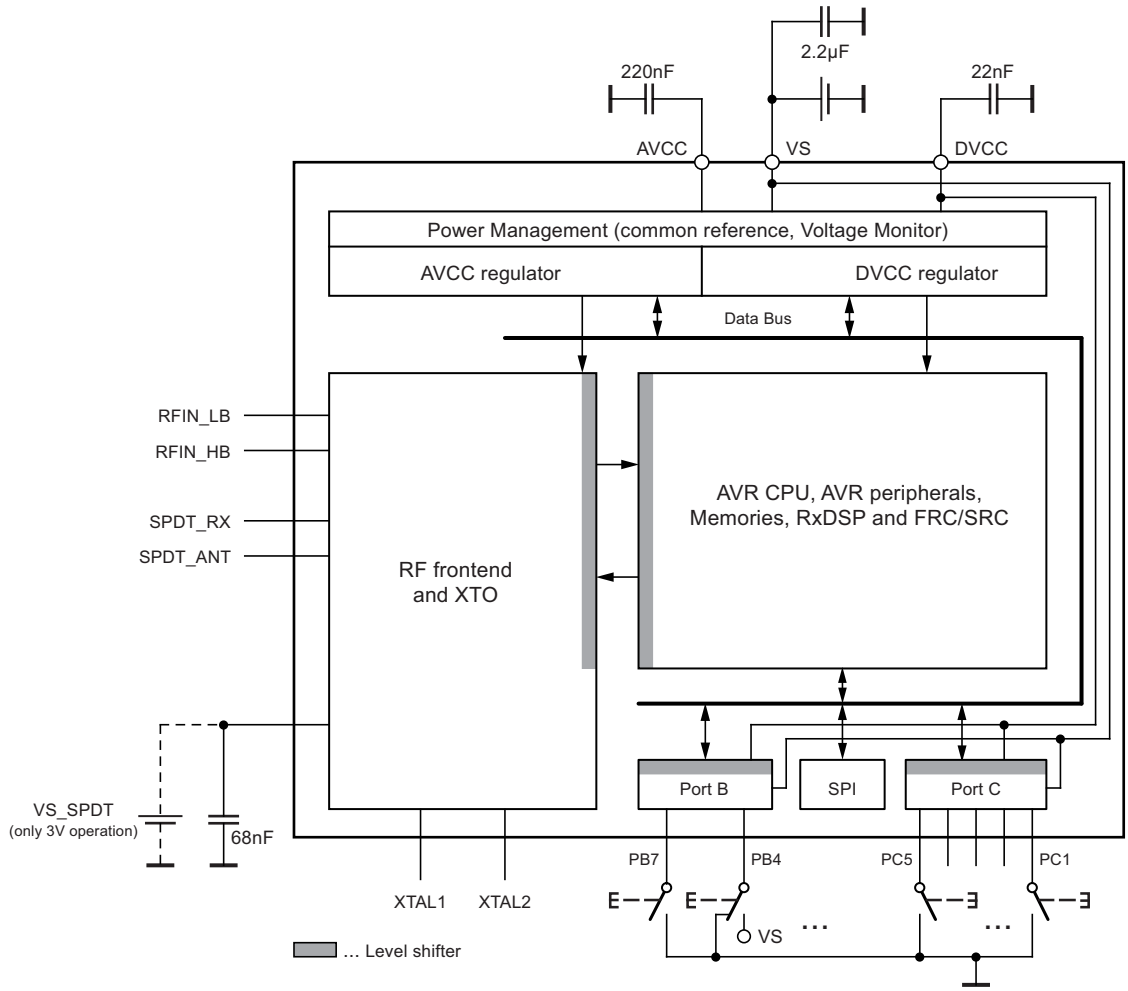
3.3.1 Overview

The IC has three power domains:

- VS – The unregulated battery voltage input.
- DVCC – The internally regulated digital supply voltage. Typical value is 1.35V.
- AVCC – The internally regulated RF frontend and XTO supply. Typical value is 1.85V.
- VS_SPDT – This is used to achieve full PCB and RF application compatibility with ATA5830N, in ATA5780N this supply is always switched off and connected externally to the battery in 3V applications.

The ATA5780N can be operated from V_S = 1.9V to 3.6V (3V application) and from V_S= 4.5V to 5.5V (5V application).

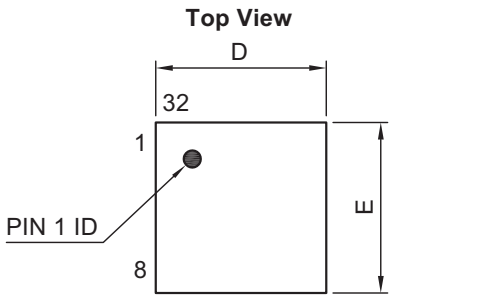
Figure 3-3. Power Supply Management

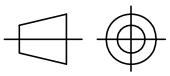


4. Ordering Information

Extended Type Number	Package	Remarks
ATA5780N-WNQW	QFN32	5mm × 5mm PB free

5. Package Information

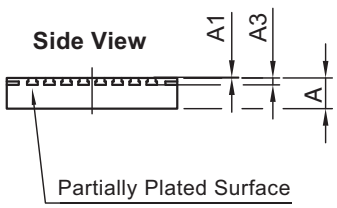


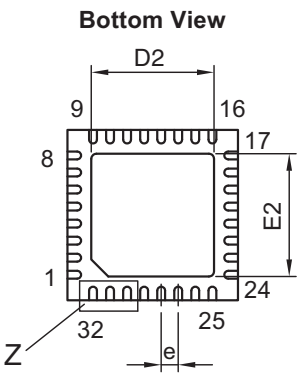


technical drawings
according to DIN
specifications

Dimensions in mm

Two Step Singulation process

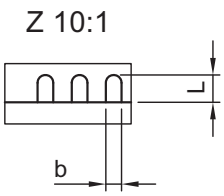




COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.8	0.9	1	
A1	0.0	0.02	0.05	
A3	0.15	0.2	0.25	
D	4.9	5	5.1	
D2	3.45	3.6	3.75	
E	4.9	5	5.1	
E2	3.45	3.6	3.75	
L	0.35	0.4	0.45	
b	0.16	0.23	0.3	
e		0.5 BSC		



11/30/11

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VQFN_5x5_32L** Exposed pad 3.6x3.6		6.543-5124.02-4	2

6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9207ES-RKE-06/13	• Section 4 “Ordering Information” on page 15 updated
9207DS-RKE-09/12	• Section 1.3.6 “EEPROM Configuration” on page 4 updated
9207CS-RKE-09/11	• Document completely redesigned

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