12-Channel Gamma Buffers with V_{COM} and Regulator

ADD8707

FEATURES

12 precision gamma reference outputs
Mask-programmable gamma resistors:
0.2% resolution and 0.1% accuracy
Mask programmable voltage regulator: 0.4% accuracy
Upper 6 buffers swing to V_{DD}
Lower 6 buffers swing to GND
Single-supply operation: 7.5 V to 16 V
Gamma current drive: 15 mA per channel
V_{COM} peak output current: 250 mA
Outputs stable under load conditions
48-lead, Pb-free LFCSP package

APPLICATIONS

LCD TV panels
LCD monitor panels

PRODUCT OVERVIEW

The ADD8707 is a 12-channel integrated gamma reference with VCOM for use in LCD TV and monitor panels. The output buffers feature high current drive and low offset voltage to provide an accurate and stable gamma curve. The top six channels swing to VDD and the lower six channels swing to GND.

Integrating the gamma setup resistors drastically reduces the external component count while increasing the gamma curve accuracy. To accommodate multiple column drivers and panel architectures, the ADD8707 is mask-programmable to a 0.2% resolution using the on-chip 500 resistor string. An on-board voltage regulator provides a fixed input for the resistor string, isolating the gamma curve from supply ripple.

The ADD8707 is specified over the temperature range of –40°C to +105°C and comes in a 48-lead, Pb-free, lead frame chip-scale package.

FUNCTIONAL BLOCK DIAGRAM

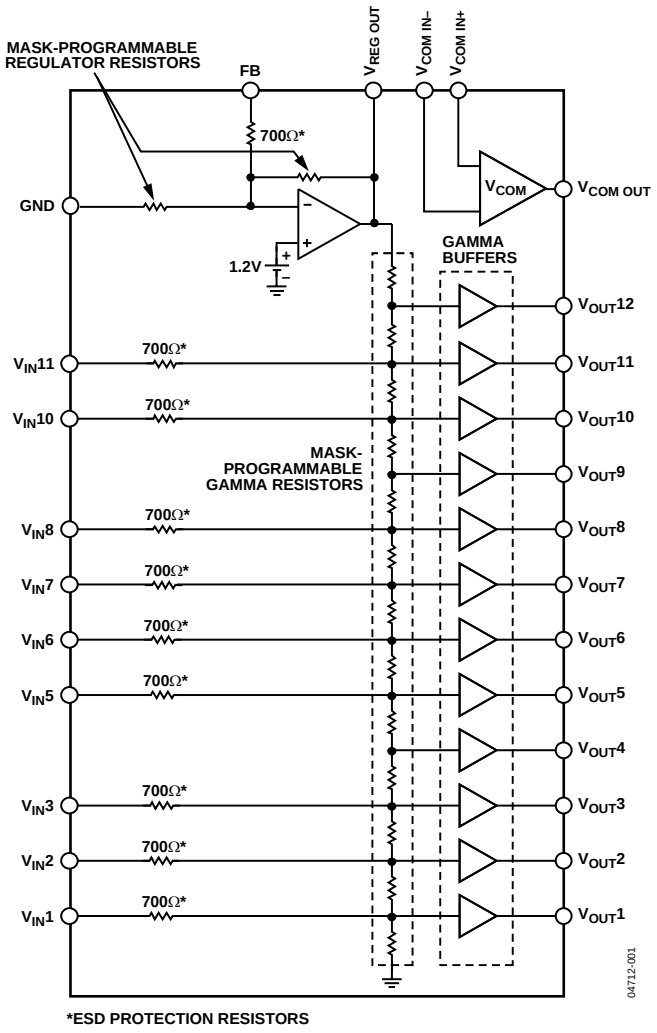


Figure 1. 48-Lead LFCSP

Rev. A

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TABLE OF CONTENTS

Electrical Characteristics 3
Absolute Maximum Ratings 5
Pin Configuration and Function Description 6
Typical Performance Characteristics 8
Application Notes 12
Tap Point Selection 12
Voltage Regulator 13
Maximum Power Dissipation 13
Land Pattern 13
Operating Temperature Range 14
Typical Applications Circuit 16
Development Circuit 17
Tap Point and Regulator Voltage Request Form 19
Regulator Section—$V_{REG\ OUT}$ 19
Tap Point Section 19
Outline Dimensions 20
Ordering Guide 20

REVISION HISTORY

10/04—Data Sheet Changed from Rev. 0 to Rev. A

Changes to Product Overview Section 1
Changes to Figure 1 1
Changes to Electrical Characteristics Section 3
Changes to Absolute Maximum Ratings Section 5
Changes to Pin Configuration and Function Description 6
Changes to Typical Performance Characteristics Section 8
Changes to Applications Notes Section 12
Changes to Figure 28, Typical Applications Circuit 16
Added Development Circuit Section 17
Added Tap Point and Regulator Voltage Request Form 19
Changes to Ordering Guide 20

7/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

V_{DD} = 16 V, T_A @ +25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
GAMMA CURVE CHARACTERISTICS						
Accuracy	R_{ACC}[1]			0.1	0.4	%
Programming Resolution	R_{RES}	500 segments		0.2		%
Total Resistor String Value	R_{TOTAL}			15		kΩ
BUFFER CHARACTERISTICS						
OUTPUTS						
Output Voltage Range (Ch12 to Ch7)	V_{OUT}	I_L = 100 μA	1.4		V_{DD}	V
Output Voltage Range (Ch6 to Ch1)	V_{OUT}	I_L = 100 μA	0		V_{DD} − 1.4	V
Output vs. Load (Ch12, Ch11, Ch2, Ch1)	ΔV_{OUT}[2]	I_L = 20 mA		15		mV
Output vs. Load (Ch10 to Ch3)	ΔV_{OUT}[2]	I_L = 5 mA		5		mV
INPUTS						
Offset Voltage	V_{OS}			5	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +105°C		20		μV/°C
Input Bias Current	I_B	−40°C ≤ T_A ≤ +105°C		0.5	1.5	μA
Input Voltage Range (Ch12 to Ch7)	V_{IN}		1.4		V_{DD}	V
Input Voltage Range (Ch6 to Ch1)	V_{IN}		0		V_{DD} − 1.4	V
V_{COM} CHARACTERISTICS						
Offset Voltage	V_{OS}			5	15	mV
Input Range	V_{IN}		1.4		V_{DD} − 1.4	V
Peak Output Current	I_{PK}			250		mA
Continuous Output Current	I_{OUT}			50		mA
Output vs. Load	ΔV_{COM}[2]	I_L = 30 mA		10		mV
BUFFER AND V_{COM} DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, CL = 200 pF	4	6		V/μs
Bandwidth	BW	−3dB, R_L = 10 kΩ, CL = 200 pF		4.5		MHz
Settling Time to 0.1%	t_S	1V step, R_L = 10 kΩ, CL = 200 pF		1.1		μs
Phase Margin	ϕ_o	R_L = 10 kΩ, CL = 200 pF		55		Degrees
Power Supply Rejection Ratio	PSRR	V_{DD} = 7 V to 17 V, −40°C ≤ T_A ≤ +105°C	68	90		dB
VOLTAGE REGULATOR						
Programmable Range	$V_{REG\ OUT}$		5		V_{DD} − 0.6	V
Initial Regulator Accuracy	V_{ACC}	No Load. $V_{REG\ OUT}$ = 14.4V		0.4	1.5	%
Dropout Voltage	V_{DO}	I_L = 100 μA		100	150	mV
		I_L = 5 mA		310	350	mV
Line Regulation	REG_{LINE}	V_{IN} = 8.5 V to 16.5 V, V_{OUT} = 8V		0.01	0.20	%/V
Load Regulation	REG_{LOAD}	I_O = 100 μA to 5 mA		0.02	0.10	%/mA
Maximum Load Current	I_O	−40°C ≤ T_A ≤ +105°C	5			mA
Feedback Reference Voltage	V_{REF}			1.2		V
Feedback Input Bias Current	$I_{B\ FB}$	−40°C ≤ T_A ≤ +105°C	−150	10	150	nA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SYSTEM ACCURACY				10		
Total Error[3, 4]	$V_{TOTAL\ ERROR}$	–40°C ≤ T_A ≤ +105°C		0.5	3	%
POWER SUPPLY						
Supply Voltage	V_{DD}		7.5		16	V
Supply Current	I_{SY}	No load, –40°C ≤ T_A ≤ +105°C		8.3	15	mA

[1] Gamma curve accuracy includes resistor matching and buffer errors, but excludes the regulator error.
[2] ΔV_{COM} is the shift from the desired output voltage under the specified current load.
[3] Total error is defined as the difference between the designed and actual output voltage divided by the actual regulator output voltage or full-scale voltage.
[4] Total error includes regulator error, resistor string error, bias current effects, and buffer offset voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	18 V
Input Voltage	−0.5 V to V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +105°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C
ESD Tolerance (HBM)	±3000 V
ESD Tolerance (MM)	±100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}[2]	θ_{JA}[3]	Unit
48-Lead LFCSP (CP)	28.3	47.7	°C/W

[1] See the Applications Information section.
[2] θ_{JA} for exposed pad soldered to JEDEC 4-layer board.
[3] θ_{JA} for exposed pad not soldered down.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTION

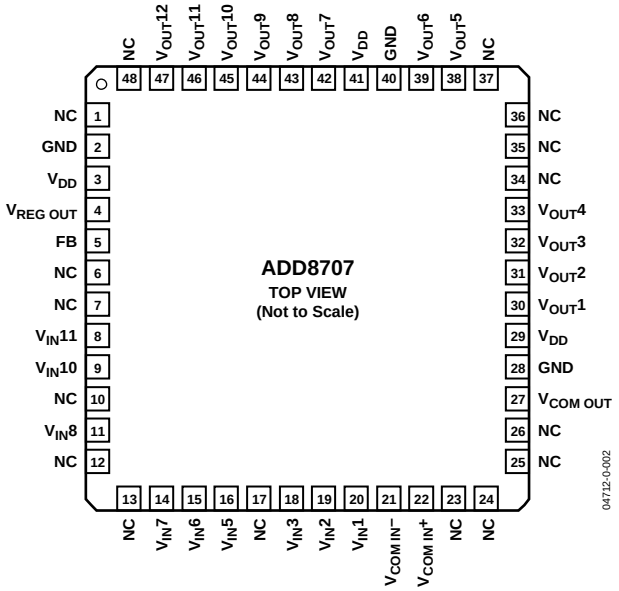


Figure 2. 48-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	NC	
2	GND	Ground. Normally 0 V.
3	V_{DD}	Supply voltage. Normally 16 V.
4	$V_{REG\ OUT}$	Regulator output voltage. Provides reference voltage to resistor string and is internally connected to the top of the resistor string.
5	FB	Regulator feedback pin. Compares a percentage of the regulator output to the internal 1.2V voltage reference. Internal resistors are used to program the desired regulator output voltage.
6	NC	
7	NC	
8	$V_{IN}11$	Buffer inputs. Normally floating.[1]
9	$V_{IN}10$	
10	NC	
11	$V_{IN}8$	Buffer inputs. Normally floating.[1]
12	NC	
13	NC	
14	$V_{IN}7$	
15	$V_{IN}6$	Buffer inputs. Normally floating.[1]
16	$V_{IN}5$	
17	NC	
18	$V_{IN}3$	
19	$V_{IN}2$	Buffer inputs. Normally floating.[1]
20	$V_{IN}1$	
21	$V_{COM\ IN}$-	V_{COM} amplifier inverting input.
22	$V_{COM\ IN}$+	V_{COM} amplifier non-inverting input.
23	NC	
24	NC	

[1] External resistors can be added to modify the internal resistor string to change the gamma voltage. An external resistor calculator is available upon request.

Pin No.	Name	Description
25	NC	
26	NC	
27	$V_{COM\ OUT}$	V_{COM} amplifier output.
28	GND	Ground. Normally 0 V.
29	V_{DD}	Supply voltage. Normally 16 V.
30	$V_{OUT}1$	Buffer outputs. These buffers can swing to ground.
31	$V_{OUT}2$	
32	$V_{OUT}3$	
33	$V_{OUT}4$	
34	NC	
35	NC	
36	NC	
37	NC	
38	$V_{OUT}5$	Buffer outputs. These buffers can swing to ground.
39	$V_{OUT}6$	
40	GND	Ground. Normally 0 V.
41	V_{DD}	Supply voltage. Normally 16 V.
42	$V_{OUT}7$	Buffer outputs. These buffers can swing to V_{DD}.
43	$V_{OUT}8$	
44	$V_{OUT}9$	
45	$V_{OUT}10$	
46	$V_{OUT}11$	
47	$V_{OUT}12$	
48	NC	

TYPICAL PERFORMANCE CHARACTERISTICS

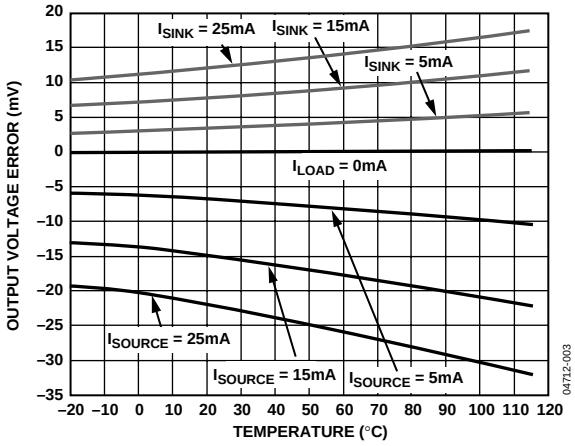


Figure 3. Output Voltage Error vs. Temperature

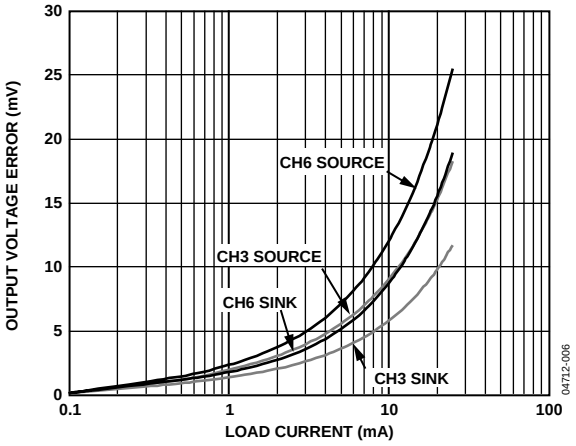


Figure 6. Output Voltage Error vs. Load Current (Channels 3 and 6)

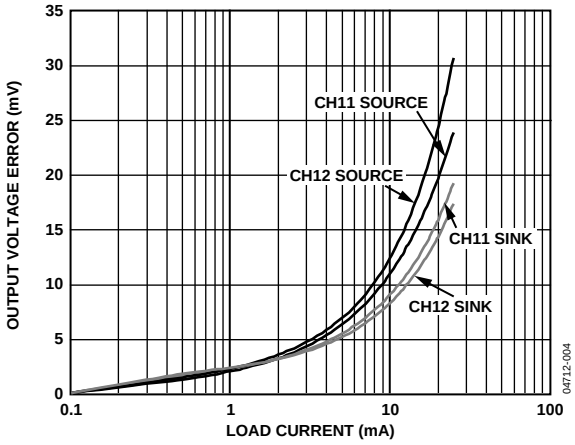


Figure 4. Output Voltage Error vs. Load Current (Channels 11 and 12)

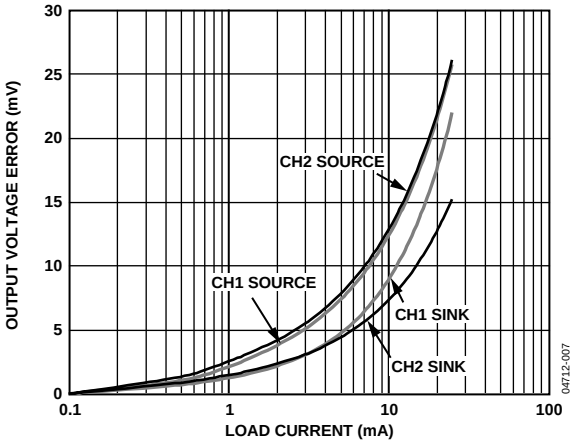


Figure 7. Output Voltage Error vs. Load Current (Channels 1 and 2)

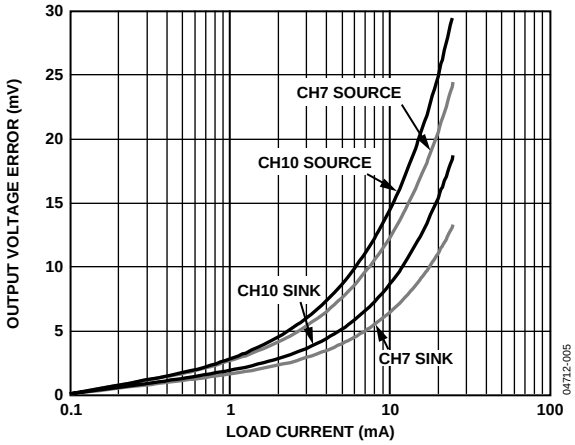


Figure 5. Output Voltage Error vs. Load Current (Channels 7 and 10)

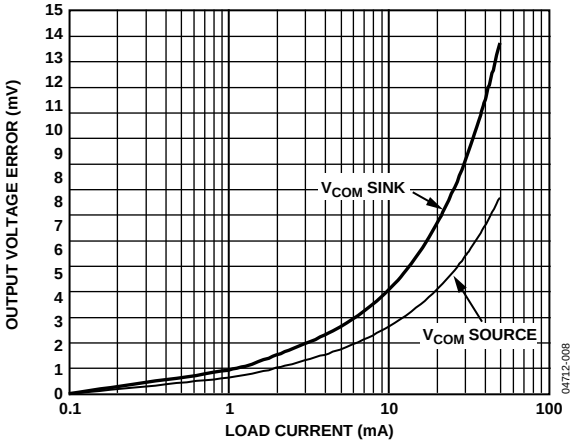


Figure 8. Output Voltage Error vs. Load Current (V_{COM})

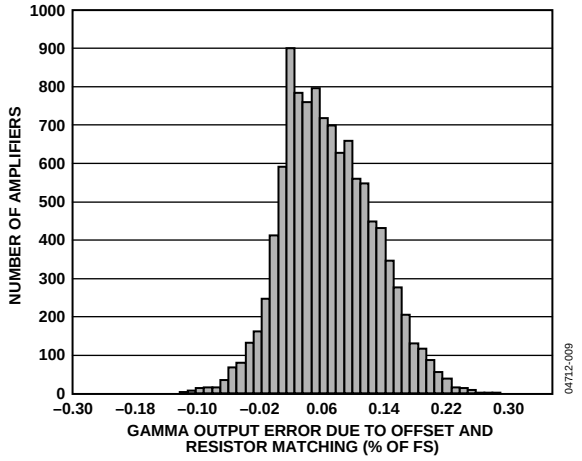


Figure 9. Gamma Output Voltage Error

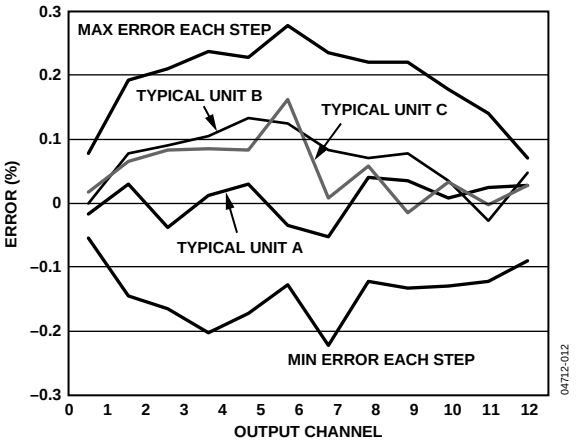


Figure 12. Gamma Output Error per Channel (920 Parts)

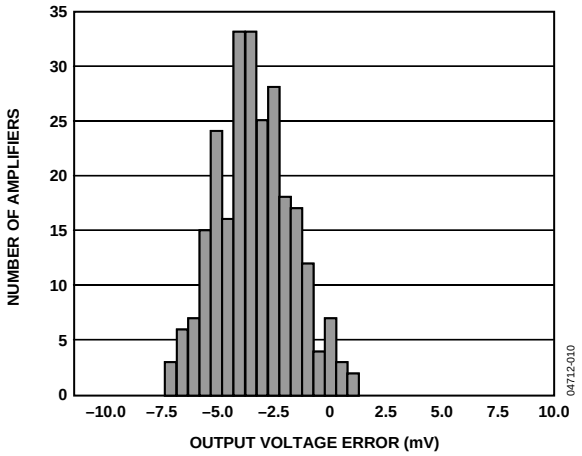


Figure 10. V_{COM} Offset Voltage

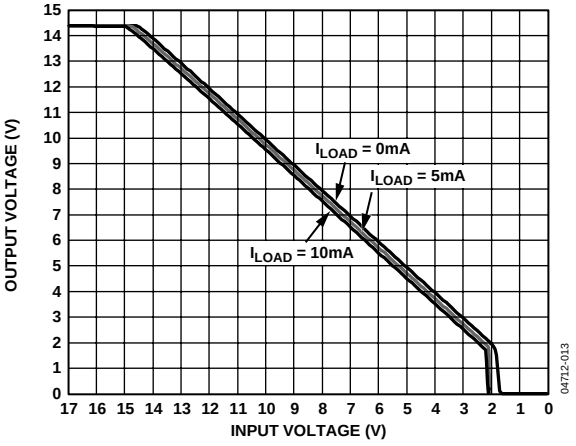


Figure 13. Dropout Characteristics

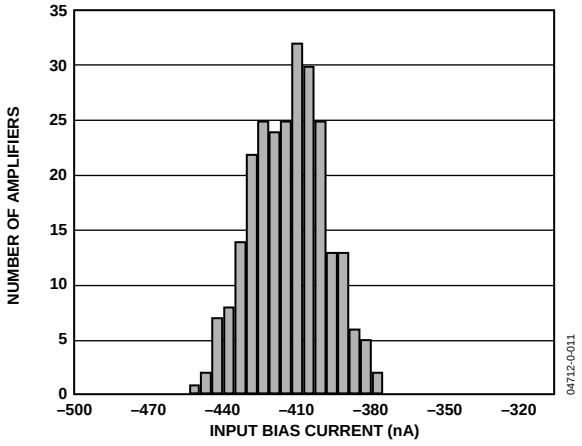


Figure 11. V_{COM} Input Bias Current Distribution

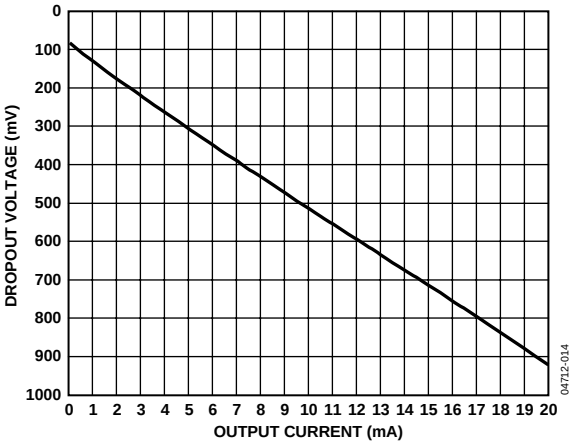


Figure 14. Dropout Voltage vs. Output Current

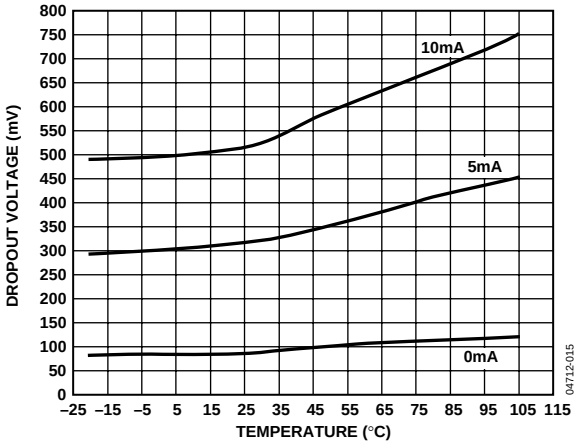


Figure 15. Dropout Voltage vs. Temperature

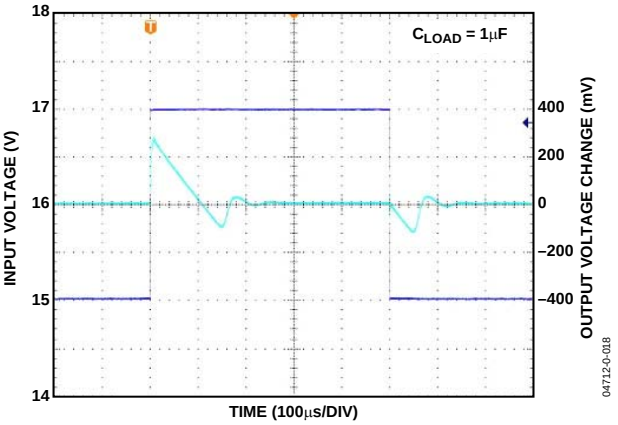


Figure 18. Regulator Line Transient Response

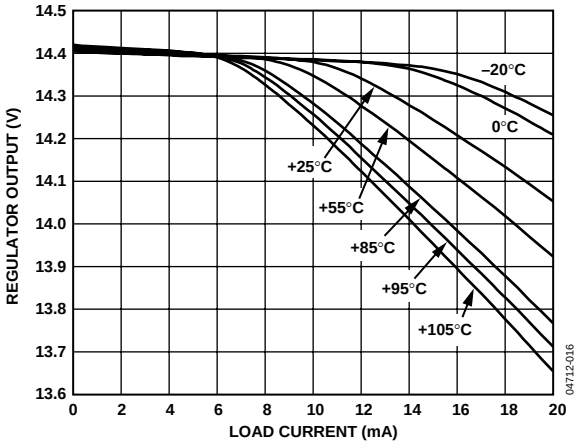


Figure 16. Regulator Output vs. I_{LOAD} over Temperature

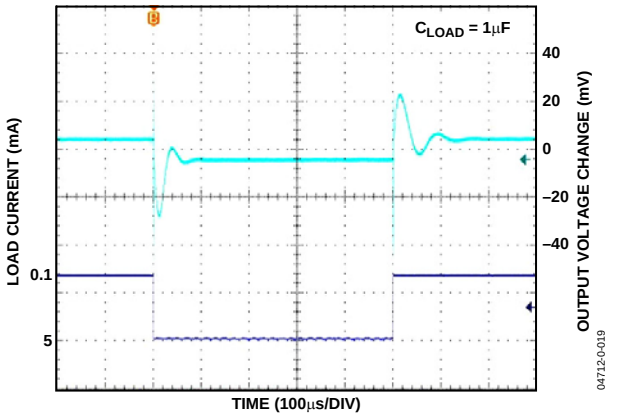


Figure 19. Regulator Load Transient Response

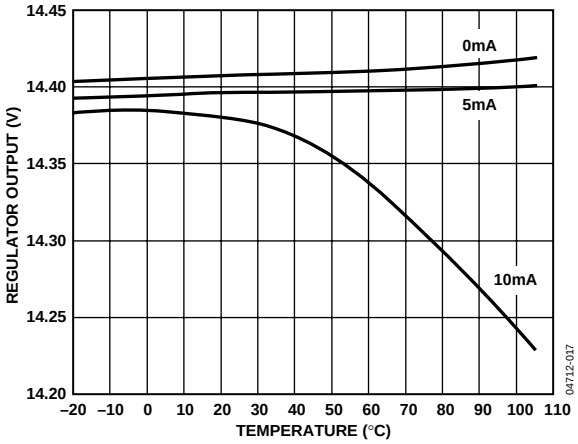


Figure 17. Regulator Output vs. Temperature

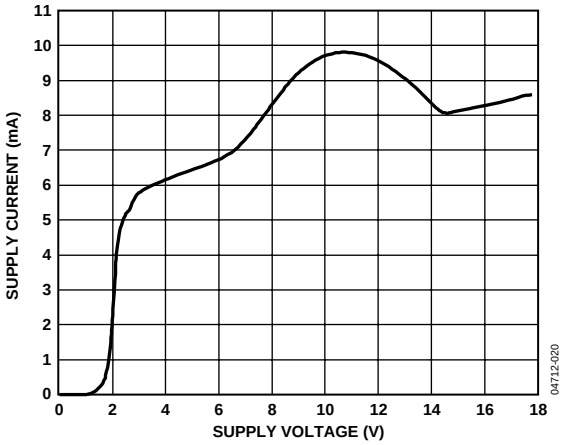


Figure 20. Supply Current vs. Supply Voltage

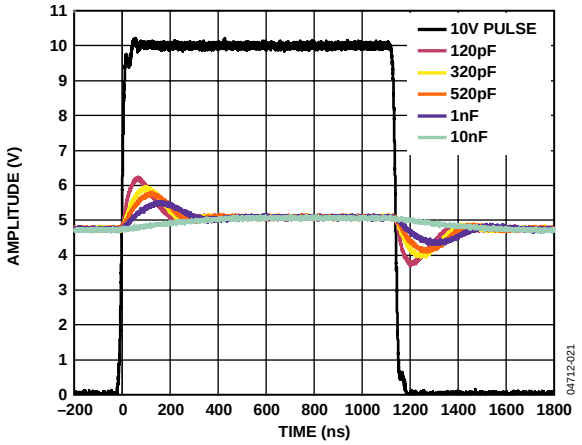


Figure 21. Gamma Buffers Transient Load Response vs. Capacitive Loading

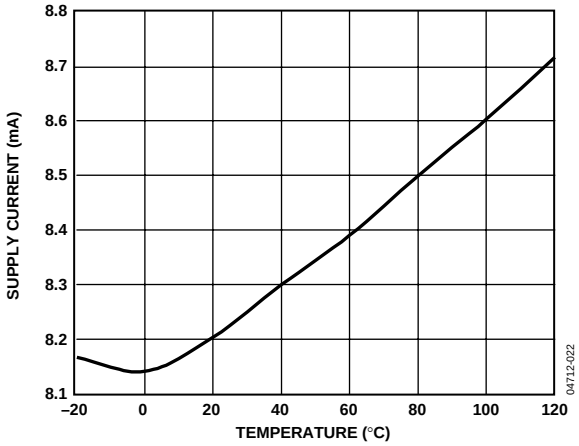


Figure 22. Supply Current vs. Temperature

APPLICATION NOTES

The ADD8707 is a mask-programmable gamma reference generator that allows source drivers to be optimized for the different combinations of liquid crystals, glass sizes, etc. in large LCD panels. It generates 12 gamma reference outputs that can be mask-programmed in 0.2% increments using the 500 matched internal resistors (Figure 23), so that every point on the curve can be targeted within 0.1% of the desired value.

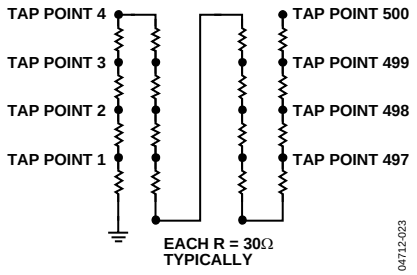


Figure 23. 500 Mask-Programmable Resistor String

In a typical panel application, the selected source drivers have an internal gamma curve that is not ideal for the specific panel (Figure 24). The ADD8707 allows the gamma curve in the source drivers to be adjusted appropriately, and also insures that all the source drivers have the same gamma curve.

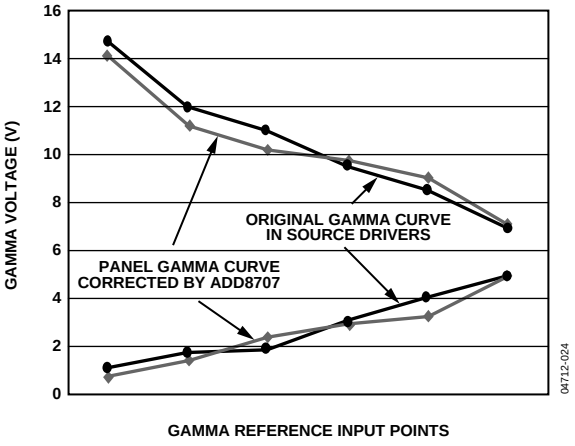


Figure 24. Original and Corrected Gamma Curves

The matching and tracking accuracy of the internal resistors is typically 0.1% with worst-case deviation from the desired curve within 0.4% of the ideal gamma curve, over temperature.

The ADD8707 also includes a low dropout linear regulator to provide a stable reference level for the gamma curve for optimum panel performance.

TAP POINT SELECTION

The ADD8707 uses a single resistor string consisting of 500 individual elements. The tap points are mask programmable and completely independent of each other. Refer to the Tap Point and Regulator Voltage Request Form in this data sheet.

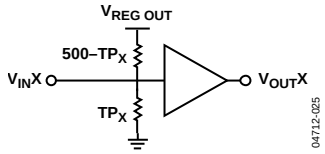


Figure 25. Gamma Buffers Tap Point Circuit.

Tap point voltages can be derived from the following equation:

$$V_{OUT\ X} = \frac{TP_X}{500} \times V_{REG\ OUT}$$

where TP_X is the desired tap point for the X^{th} channel.

Table 5. Typical Mask Implementation

V_{DD} = 16 V, $V_{REG\ OUT}$ = 14.4 V, 0 ≤ X ≤ 500

	Tap Point (X)	Voltage	Units
$V_{OUT}12$	500	14.400	V
$V_{OUT}11$	419	12.067	V
$V_{OUT}10$	365	10.512	V
$V_{OUT}9$	349	10.051	V
$V_{OUT}8$	343	9.878	V
$V_{OUT}7$	297	8.554	V
$V_{OUT}6$	213	6.134	V
$V_{OUT}5$	173	4.982	V
$V_{OUT}4$	163	4.694	V
$V_{OUT}3$	146	4.205	V
$V_{OUT}2$	95	2.736	V
$V_{OUT}1$	7	0.202	V

VOLTAGE REGULATOR

The on-board voltage regulator provides a regulated voltage to the resistor chain to provide stable gamma voltages.

The output of the regulator is set by the two mask programmable internal resistors R1 and R2, and a reference voltage. In the ADD8707, the typical values of these parts are shown in Figure 26. To request a different regulator voltage, please refer to the Tap Point and Regulator Voltage Request Form in this data sheet.

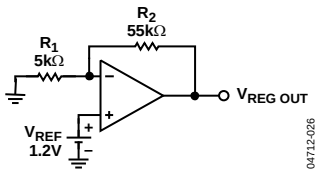


Figure 26. Voltage Regulator

The internal resistors have a typical accuracy of 0.1%. External resistors can be used to adjust the regulator voltage, though it is not recommended. Contact a sales office for further details.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADD8707 package is limited by the associated rise in junction temperature (TJ) on the die. At approximately 150°C, the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADD8707. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

LAND PATTERN

The LFCSP package comes with a thermal pad. Soldering down this thermal pad dramatically improves the heat dissipation of the package. It is necessary to attach vias that connect the soldered thermal pad to another layer on the board. This provides an avenue to dissipate the heat away from the part. Without vias, the heat is isolated directly under the part.

Subdivide the solder paste, or stencil layer, for the thermal pad. This reduces solder balling and splatter. It is not critical how the subdivisions are arranged, as long as the total coverage of the solder paste for the thermal pad is greater than 50%. The land pattern is critical to heat dissipation. A suggested land pattern is shown in Figure 27.

The thermal pad is attached to the substrate. In the ADD8707, the substrate is connected to V_{DD}. To be electrically safe, the thermal pad should be soldered to an area on the board that is electrically isolated or connected to V_{DD}. Attaching the thermal pad to ground adversely affects the performance of the part.

OPERATING TEMPERATURE RANGE

The junction temperature is as follows:

$$T_J = T_{AMB} + \theta_{JA} \times P_{DIS}$$

where:
T_{AMB} = ambient temperature specified on the data sheet.
θ_{JA} = junction-to-ambient thermal resistance, in °C/watt.
P_{DIS} = power dissipated in the device, in watts.

For the ADD8707, P_{DIS} can be calculated by

$$P_{DIS} = V_{DD} \times I_{DQ} + \Sigma(I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})) + \Sigma(-I_{OUT\,X(-)} \times V_{OUTX}) + (V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$$

where:

$V_{DD} \times I_{DQ}$ = nominal system power requirements.
$I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})$ = positive-current amplifier load power dissipation (current comes from V_{DD}).
$-I_{OU\,XT(-)} \times V_{OUT\,X}$ = negative-current amplifier load power dissipation (current goes to GND).
$(V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$ = regulator load power dissipation.

In this example, T_{AMB} = 95°C. To calculate P_{DIS}, assume the values in Table 6.

Table 6.

	$V_{OUT\,X}$ (V)	$I_{OUT\,X}$ (mA)	P (W)
$V_{OUT}12$	14.400	8.3	0.0133
$V_{OUT}11$	12.067	7.9	0.0311
$V_{OUT}10$	10.512	−4.5	0.0473
$V_{OUT}9$	10.051	−4.2	0.0422
$V_{OUT}8$	9.878	5.6	0.0343
$V_{OUT}7$	8.554	−3.3	0.0282
$V_{OUT}6$	6.134	−6.9	0.0423
$V_{OUT}5$	4.982	5.7	0.0628
$V_{OUT}4$	4.694	3.5	0.0396
$V_{OUT}3$	4.205	9.6	0.113
$V_{OUT}2$	2.736	9.5	0.126
$V_{OUT}1$	0.202	−7.2	0.00145
$\Sigma(I_{OUT\,X(+)} \times (V_{DD} - V_{OUT\,X})) + \Sigma(-I_{OUT\,X(-)} \times V_{OUT\,X})$			0.582

$V_{DD} \times I_{DQ}$ = 16 V × 15 mA = 0.240 W.
$(V_{DD} - V_{REG\,OUT}) \times I_{LOAD}$ = (16 V − 14.4 V) × 5 mA = 0.008 W.
P_{DIS} = 0.240W + 0.582W + 0.008W = 0.830W.

Example 1

Exposed pad soldered down with via θ_{JA} = 28.3°C/W:

$$T_J = 95°C + (28.3°C/W) \times (0.830\ W) = 118.5°C$$

The maximum junction temperature that is guaranteed before the part breaks down is 150°C. is The maximum process limit is 125°C. Because T_J is < 150°C and < 125°C, this example demonstrates a condition where the part should perform within process limits.

Example 2

Exposed pad not soldered down θ_{JA} = 47.7°C/W:

$$T_J = 95°C + (47.7°C/W) \times (0.830\ W) = 134.6°C$$

In this example, T_J is < 150°C but > 125°C. Although the part should not exhibit any damage here, the process limits have been exceeded. The part may no longer operate as intended.

These examples show that soldering down the exposed pad is important for proper heat dissipation. Under the same power-up and loading conditions, the unsoldered part has a higher temperature than the soldered part. Therefore, it is strongly advised that the exposed pad be soldered down.

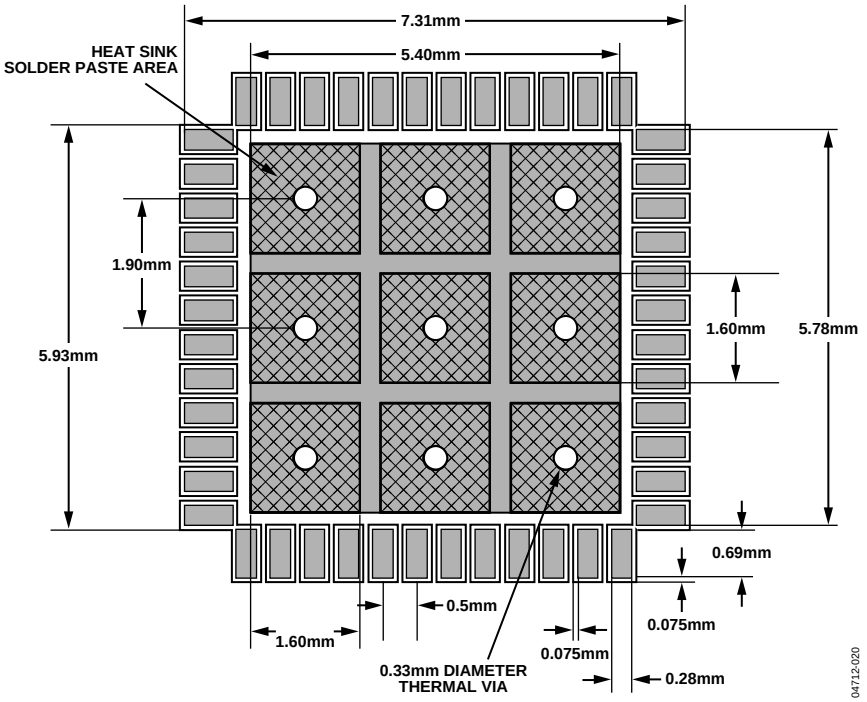


Figure 27. 48-Lead LFCSP (CP-48) Land Pattern—Dimensions shown in millimeters

Notes:

1. Gray area represents the board metallization.
2. White area represents the solder mask and vias.
3. Hatched area is for the heat sink solder paste.
4. The thermal pad is electrically active. The solder mask opening should be 0.150 mm larger than the pad size, resulting in 0.075 mm of clearance between the copper pad and solder mask.

TYPICAL APPLICATIONS CIRCUIT

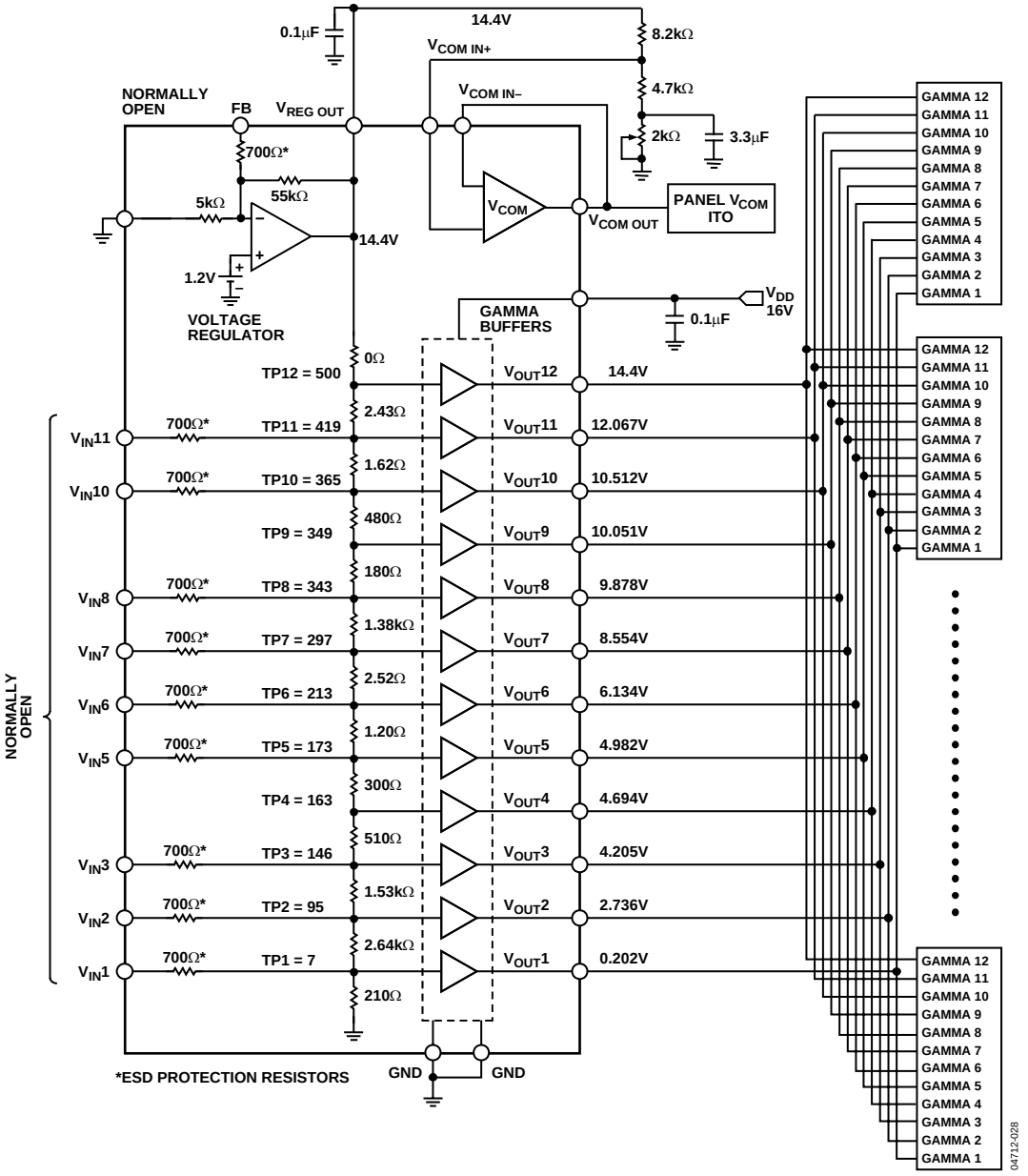


Figure 28. Typical Applications Circuit

DEVELOPMENT CIRCUIT

For development purposes, the ADD8707 is available in a generic form without the tap points (see Figure 29). The typical applications circuit for this part is shown in Figure 30. To order this version, refer to the Ordering Guide. The model listed is the development version.

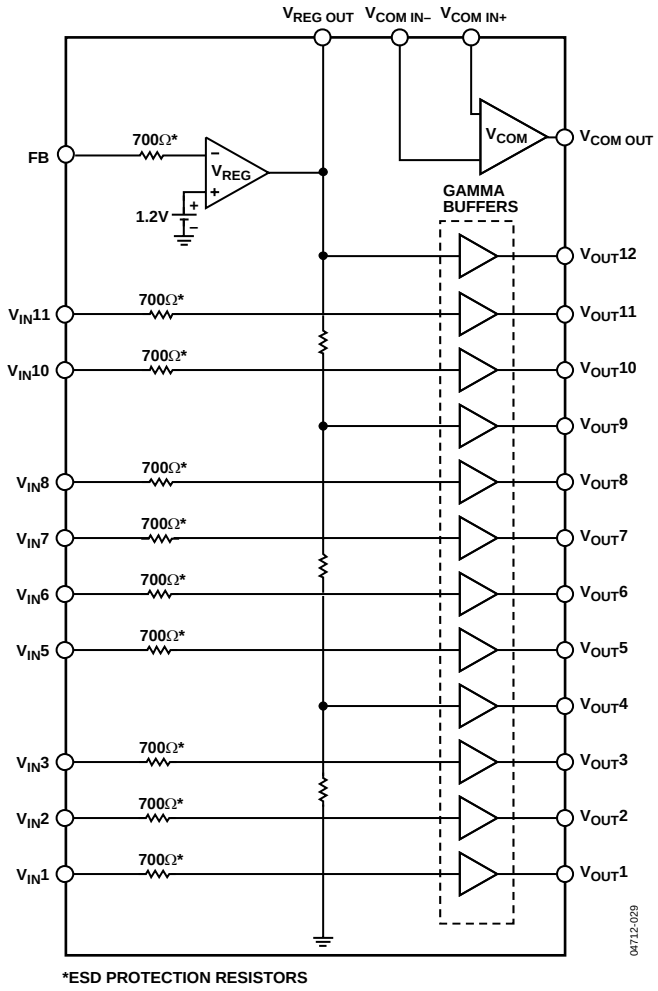


Figure 29. Block Diagram for ADD8707 Development Version (with No Tap Points)

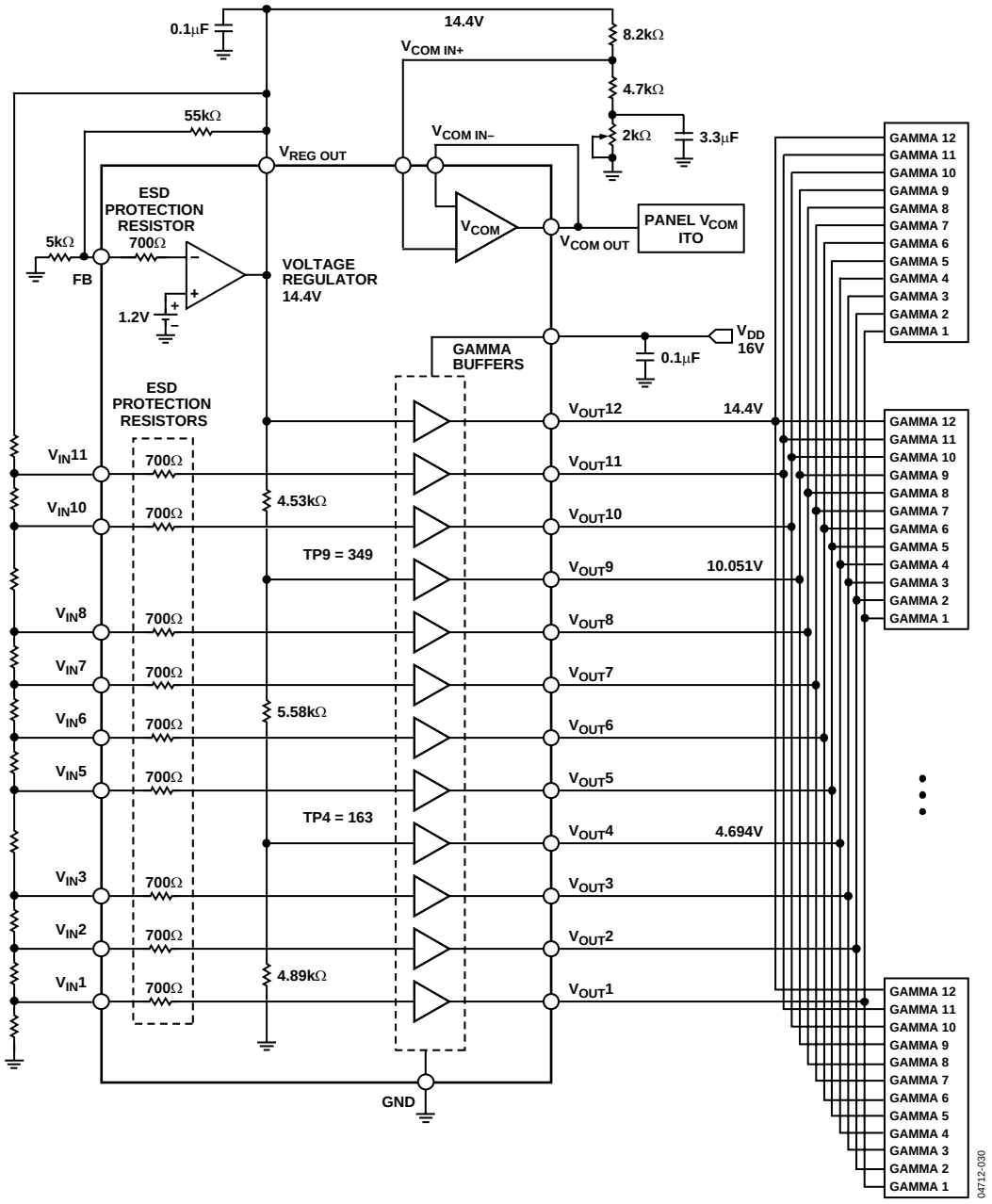


Figure 30. Typical Applications Circuit for ADD8707 Development Version (with No Tap Points)

TAP POINT AND REGULATOR VOLTAGE REQUEST FORM

REGULATOR SECTION—$V_{REG\ OUT}$

To ensure correct regulator operation V_{DD} must exceed V_{REG} by 600 mV minimum—that is, a V_{REG} = 14.4 V requires a minimum V_{DD} = 15.0 V.

Parameter	Value (6.9 V – 15.4 V)
$V_{REG\ OUT}$	

TAP POINT SECTION

Gamma output voltages are calculated using the following formula:

$$V_{OUT} = \frac{TP \times V_{REG\ OUT}}{500}$$

A Microsoft® Excel spreadsheet is available which automatically calculates the best tap point based on $V_{REG\ OUT}$ and the desired output voltages for each gamma output.

Output	Tap Point
$V_{OUT}18$	
$V_{OUT}17$	
$V_{OUT}16$	
$V_{OUT}15$	
$V_{OUT}14$	
$V_{OUT}13$	
$V_{OUT}12$	
$V_{OUT}11$	
$V_{OUT}10$	
$V_{OUT}9$	
$V_{OUT}8$	
$V_{OUT}7$	
$V_{OUT}6$	
$V_{OUT}5$	
$V_{OUT}4$	
$V_{OUT}3$	
$V_{OUT}2$	
$V_{OUT}1$	

CUSTOMER INFORMATION

Name: _____

Company: _____

Address: _____

_____

Date: _____

Please return this form to your local sales office.

OUTLINE DIMENSIONS

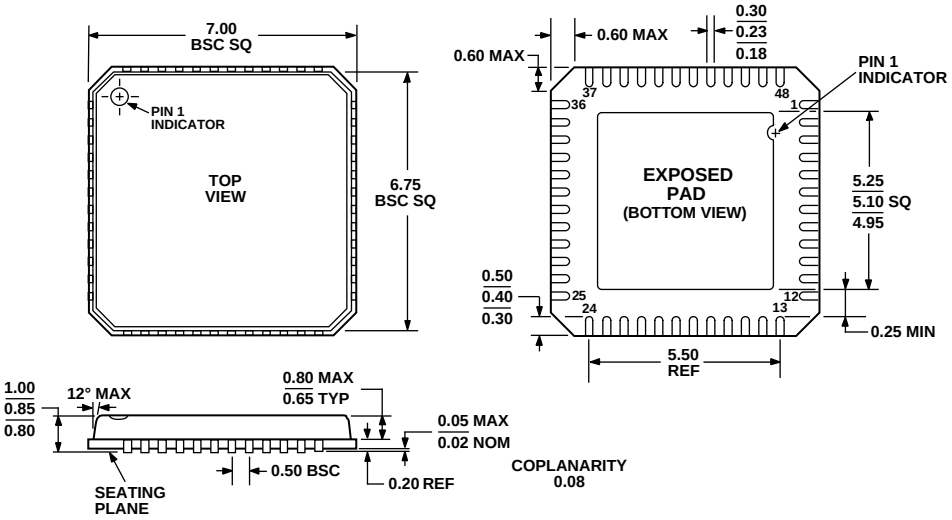


Figure 31. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body
(CP-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Outline
ADD8707WCPZ-REEL7[2, 3]	–40°C to +105°C	48-Lead Lead Frame Chip Scale Package	CP-48

[1] Available in reels only.
[2] Z = Pb-free part.
[3] Development version.

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