RENESAS

DATASHEET

X9271

Single Supply/Low Power/256-Tap/SPI Bus Single, Digitally Controlled (XDCP™) Potentiometer

FN8174 Rev 5.00 October 15, 2015

The X9271 integrates a single, digitally controlled potentiometer (XDCP[™]) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented by using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile data registers that can be directly written to and read by the user. The contents of the WCR control the position of the wiper on the resistor array though the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 256 Resistor Taps
- SPI Serial Interface for Write, Read, and Transfer Operations of Potentiometer
- Wiper Resistance, 100Ω typical at V_{CC} = 5V
- 16 Nonvolatile Data Registers
- · Nonvolatile Storage of Multiple Wiper Positions
- Power-on Recall; Loads Saved Wiper Position on Power-up
- Standby Current <3µA Max
- V_{CC} = 2.7V to 5.5V Operation
- 50kΩ End-to-End Resistance
- 100-yr Data Retention
- Endurance: 100,000 Data Changes per Bit per Register
- 14-Lead TSSOP
- Low-power CMOS
- · Pb-Free Plus Anneal Available (RoHS Compliant)

Functional Diagram





Ordering Information

PART NUMBER (<u>Notes 2, 3</u>)	PART MARKING	V _{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP. RANGE (°C)	PACKAGE Pb-Free	PKG. DWG. #
X9271UV14IZ (<u>Note 1</u>)	X9271 UVZI	5 ±10%	50	-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9271UV14Z (<u>Note 1</u>)	X9271 UVZ	5 ±10%	50	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9271UV14IZ-2.7	X9271 UVZG	2.7 to 5.5	50	-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9271UV14IZ-2.7T1	X9271 UVZG	2.7 to 5.5	50	-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9271UV14Z-2.7 (No longer available, recommended replacement: X9271UV14IZ-2.7T1)	X9271 UVZF	2.7 to 5.5	50	0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9271UV14Z-2.7T1 (No longer available, recommended replacement: X9271UV14IZ-2.7T1)	X9271 UVZF	2.7 to 5.5	50	0 to +70	14 Ld TSSOP (4.4mm)	M14.173

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

 These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see device information page for X9271. For more information on MSL please see Tech Brief TB363.

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	SO	Serial Data Output
2	A0	Device Address
3	NC	No Connect
4	CS	Chip Select
5	SCK	Serial Clock
6	SI	Serial Data Input
7	V _{SS}	System Ground
8	WP	Hardware Write Protect
9	A1	Device Address
10	HOLD	Device Select. Pause the serial bus.
11	R _W	Wiper Terminal of Potentiometer
12	R _H	High Terminal of Potentiometer
13	RL	Low Terminal of Potentiometer
14	V _{CC}	System Supply Voltage



Detailed Functional Diagram



Circuit-Level Applications

- · Vary the gain of a voltage amplifier.
- Provide programmable DC reference voltages for comparators and detectors.
- · Control the volume in audio circuits.
- Trim out the offset voltage error in a voltage amplifier circuit.
- Set the output voltage of a voltage regulator.
- Trim the resistance in Wheatstone bridge circuits.
- Control the gain, characteristic frequency, and Q-factor in filter circuits.
- Set the scale factor and zero point in sensor signal conditioning circuits.
- · Vary the frequency and duty cycle of timer ICs.
- Vary the DC biasing of a pin diode attenuator in RF circuits.
- Provide a control variable (I, V, or R) in feedback circuits.

System-Level Applications

- · Adjust the contrast in LCD displays.
- Control the power level of LED transmitters in communication systems.
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems.
- · Control the gain in audio and home entertainment systems.
- Provide the variable DC bias for tuners in RF wireless systems.
- Set the operating points in temperature control systems.
- · Control the operating point for sensors in industrial systems.
- Trim offset and gain errors in artificial intelligence systems.



Pin Descriptions

Bus Interface Pins

SERIAL OUTPUT (SO)

The Serial Output (SO) is the serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT (SI)

The Serial Input (SI) is the serial data input pin. All operational codes, byte addresses, and data to be written to the potentiometers and potentiometer registers are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The Serial Clock (SCK) input is used to clock data into and out of the X9271.

HOLD (HOLD)

 $\overline{\text{HOLD}}$ is used in conjunction with the $\overline{\text{CS}}$ pin to select the device. Once the part is selected and a serial sequence is under way, $\overline{\text{HOLD}}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{\text{HOLD}}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{\text{HOLD}}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{\text{HOLD}}$ should be held HIGH at all times. CMOS level input.

DEVICE ADDRESS (A1 - A0)

The Device Address (A1 - A0) inputs are used to set the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9271.

CHIP SELECT (CS)

When Chip Select (\overline{CS}) is HIGH, the X9271 is deselected, the SO pin is at high impedance and (unless an internal write cycle is under way) the device is in standby state. \overline{CS} LOW enables the X9271, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on \overline{CS} is required prior to the start of any operation.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

RW

The wiper pin $(\ensuremath{\mathsf{R}}_W)$ is equivalent to the wiper terminal of a mechanical potentiometer.

Supply Pins

SYSTEM SUPPLY VOLTAGE (V_CC) AND SUPPLY GROUND (V_SS)

The System Supply Voltage (V_{CC}) pin is the system supply voltage. The Supply Ground (V_{SS}) pin is the system ground.

Other Pins

HARDWARE WRITE PROTECT INPUT (WP)

The Hardware Write Protect Input (\overline{WP}) pin, when LOW, prevents nonvolatile writes to the data registers.

NO CONNECT

No Connect pins should be left floating. These pins are used for Intersil manufacturing and testing purposes.

Principles of Operation

Device Description

SERIAL INTERFACE

The X9271 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. \overline{CS} must be LOW and the \overline{HOLD} and \overline{WP} pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three-state outputs. This can help to reduce system pin count.

ARRAY DESCRIPTION

The X9271 is composed of a resistor array (Figure 1). The array contains the equivalent of 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array, only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The eight bits of the WCR (WCR[7:0]) are decoded to select, and enable, one of 256 switches (<u>Table 1</u>).

POWER-UP AND POWER-DOWN RECOMMENDATIONS

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins, provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W; i.e., V_{CC} \ge V_H, V_L, V_W. The V_{CC} ramp rate specification is always in effect.





FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

Device Description

Wiper Counter Register (WCR)

The X9271 contains a Wiper Counter Register (WCR) for the DCP potentiometer. The WCR can be envisioned as an 8-bit parallel and serial load counter, with its outputs decoded to select one of 256 switches along its resistor array (<u>Table 1</u>). The contents of the WCR can be altered in four ways:

- 1. It can be written directly by the host via the Write Wiper Counter Register instruction (serial load).
- It can be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load).
- 3. It can be modified one step at a time by the Increment/ Decrement instruction.
- 4. It is loaded with the contents of its Data Register zero (DR0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9271 is powered down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Powerup guidelines are recommended to ensure proper loading of the R0 value into the WCR. The DR0 value of Bank 0 is the default value.

Data Registers (DR3–DR0)

The potentiometer has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host (<u>Table 2</u>). Data can also be transferred between any of the four Data Registers and the associated WCR. All operations changing data in one of the Data Registers are nonvolatile operations and take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0 \sim 255).

Status Register (SR)

The 1-bit Status Register is used to store the system status (<u>Table 3</u>).

WIP: Write In Progress status bit; read only.

- WIP = 1 indicates that a high-voltage write cycle is in progress.
- WIP = 0 indicates that no high-voltage write cycle is in progress

TABLE 1.	WIPER COUNTER REGISTER, WCR (8-bit), WCR[7:0]:
	Used to store current wiper position (Volatile, V)

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V
(MSB)							(LSB)



BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV							
MSB							LSB

TABLE 2. DATA REGISTER, DR (8-BIT), DR[7:0]: Used to store wiper positions or data (Nonvolatile, NV)

TABLE 3. STATUS REGISTER, SR (WIP is 1-bit)

WIP	
(LSB)	

Device Description

Instructions

IDENTIFICATION BYTE (ID AND A)

The first byte sent to the X9271 from the host, following a CS going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bit is the device ID for the X9271; this is fixed as 0101[B] (Table 4).

The A1 - A0 bits in the ID byte are the internal slave address. The physical device address is defined by the state of the A1 - A0 input pins. The slave address is externally specified by the user. The X9271 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9271 to successfully continue the command sequence. Only the device for which slave address matches the incoming device address sent by the master executes the instruction. The A1 - A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS} .

INSTRUCTION BYTE (I[3:0])

The next byte sent to the X9271 contains the instruction and register pointer information. The three most significant bits are used to provide the instruction operation code (I[3:0]). The RB and RA bits point to one of the four Data Registers. P0 is the POT selection; since the X9271 is single POT, P0 = 0. The format is shown in Table 7.

REGISTER BANK SELECTION (R1, R0, P1, P0)

There are 16 registers organized into four banks. Bank 0 is the default bank of registers. Only Bank 0 registers can be used for the data register to Wiper Counter Register operations.

Banks 1, 2, and 3 are additional banks of registers (12 total) that can be used for SPI write and read operations. The data registers in Banks 1, 2, and 3 cannot be used for direct read/write operations to the Wiper Counter Register (Tables 5 and $\underline{6}$).

DEVI	CE TYPE	EIDENT	IFIER	SET TO PRO OPER	0 FOR PER ATION	INTEI SLA ADDI	RNAL AVE RESS
ID3	ID2	ID1	ID0	0	0	A1	A0
0	1	0	1				
(MSB)							(LSB)

TABLE 5. REGISTER SELECTION (DR0 TO DR3)

RB	RA	REGISTER SELECTION	OPERATIONS
0	0	0	Data Register Read and Write; Wiper Counter Register Operations
0	1	1	Data Register Read and Write; Wiper Counter Register Operations
1	0	2	Data Register Read and Write; Wiper Counter Register Operations
1	1	3	Data Register Read and Write; Wiper Counter Register Operations

TABLE 6. REGISTER BANK SELECTION (BANK 0 TO BANK 3)

P1	P0	BANK SELECTION	OPERATIONS
0	0	0	Data Register Read and Write; Wiper Counter Register Operations
0	1	1	Data Register Read and Write Only
1	0	2	Data Register Read and Write Only
1	1	3	Data Register Read and Write Only

TABLE 7. INSTRUCTION BYTE FORMAT

						SP1	REGISTER BANK SELECTION FOR REGISTER WRITE AND READ OPERATIONS)
I	NSTRUCTIO	ON OPCOD	E	REGI SELE	STER CTION		POTENTIOMETER SELECTION (WCR SELECTION) (<u>Note 4</u>)
13	12	l1	P0	RB	RA	P1	P0
(MSB)							(LSB)

NOTE:

4. Set to P0 = 0 for potentiometer operations.

Device Description

Instructions

Five of the eight instructions are three bytes in length. These instructions are:

- Read Wiper Counter Register: Read the current wiper position of the potentiometer.
- Write Wiper Counter Register: Change current wiper position of the potentiometer.
- **Read Data Register**: Read the contents of the selected Data Register.
- Write Data Register: Write a new value to the selected Data Register.
- **Read Status**: This command returns the contents of the WIP bit, which indicates if the internal write cycle is in progress.

See <u>Table 8</u> for details of the instruction set.

The basic sequence of the 3-byte instruction is shown in Figure 2. These 3-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action is delayed by t_{WRL} . A transfer from the WCR (current wiper position) to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers, or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (Figure 3).

Two instructions require a 2-byte sequence to complete (Figure 4). These instructions transfer data between the host and the X9271; either between the host and one of the data registers, or directly between the host and the Wiper Counter Register. These instructions are:

- XFR Data Register to Wiper Counter Register: Transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- XFR Wiper Counter Register to Data Register: Transfers the contents of the specified Wiper Counter Register to the associated Data Register.

The final command is Increment/Decrement (Figures 5 and 6). It is different from the other commands, because its length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment step, thereby providing a fine-tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper moves one resistor segment towards the R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper moves one resistor segment towards the R_L terminal.

Write-in-Process (WIP) Bit

The contents of the Data Registers are saved to nonvolatile memory when the \overline{CS} pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by the Write-in-Process bit (WIP). The WIP bit is read with a Read Status command.



FIGURE 2. THREE-BYTE INSTRUCTION SEQUENCE (WRITE)





These commands only valid when P1 = P0 = 0





FIGURE 5. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

SI



FIGURE 6. INCREMENT/DECREMENT TIMING LIMITS

|--|

		(1	IN /0 = D	STRU ATA IS		SET OR ZEF	RO)		
INSTRUCTION	13	12	11	10	RB	RA	P ₁	P ₀	OPERATION
Read Wiper Counter Register	1	0	0	1	0	0	0	1/0	Read contents of Wiper Counter Register.
Write Wiper Counter Register	1	0	1	0	0	0	0	1/0	Write new value to Wiper Counter Register.
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read contents of Data Register pointed to by P1 - P0 and RB - RA.
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to Data Register pointed to by P1 - P0 and RB - RA.
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	0	Transfer contents of Data Register pointed to by RB - RA (Bank 0 only) to Wiper Counter Register.
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	0	Transfer contents of Wiper Counter Register to Register pointed to by RB-RA (Bank 0 only).
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	0	Enable increment/decrement of the Wiper Counter Register.
Read Status (WIP Bit)	0	1	0	1	0	0	0	1	Read status of internal write cycle by checking WIP bit.

Instruction Format

Read Wiper Counter Register (WCR)

CS Falling	D	evice Iden	e Typ tifier	be		De Add	evice resse	s	I	nstru Opc	uctio code	n	A	DR/I	Bank esse	S		(Se	Wip nt by	oer F y X9	Posil 271	ion on :	SO)		CS Rising
Edge	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	0	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0	Eage

Write Wiper Counter Register (WCR)

CS Falling	D	evice Iden	e Typ tifier	be		De Add	evice resse	s	I	nstru Opc	uctio code	n	ŀ	DR/I \ddre	3ank esse	s S		(S	E ent)ata by ⊦	Byte lost	e on S	SI)		CS Rising
Edge	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	0	W C R 7	W C R 6	W C R 5	W C R 4	W C R 3	W C R 2	W C R 1	W C R 0	Edge



Read Data Register (DR)

CS Falling	D	evic Ider	e Typ ntifier	be		De Add	evice resse	es	Ir	nstru Opo	uctio code	n		DR/I Addre	Bank esses			(Sent	Data by X9	Byte 271 d	on SC))		CS Rising
Edge	0	1	0	1	0	0	A1	A0	1	0	1	1	RB	RA	P1	P0	D7	D 6	D5	D4	D3	D2	D1	D0	Edge

Write Data Register (DR)

CS Falling	D	evice Iden	e Tyj itifier	pe		De Add	evice resse	es	Ir	nstru Opc	uctio code	n		DR/I Addre	Bank esses				(Sen	Data t by ⊦	Byte lost c	on SI)			CS Rising	-TAGE YCLE
Edge	0	1	0	1	0	0	A1	A0	1	1	0	0	RB	RA	P1	P0	D7	D 6	D5	D4	D3	D2	D1	D0	Edge	HIGH-VOI WRITE C

Transfer Wiper Counter Register (WCR) to Data Register (DR)

CS Falling	D	evic Ider	e Typ ntifier	be		D Ado	evice dresse	es	h	nstru Opc	uctio code	on e	ŀ	DR/Ba \ddres	nk ses		CS Rising	HIGH-VOLTAGE WRITE CYCLE
Edge	0	1	0	1	0	0	A1	A0	1	1	1	0	RB	RA	0	0	Edge	

Transfer Data Register (DR) to Wiper Counter Register (WCR) (Notes 5, 6)

CS Falling	D	evice Iden	e Typ tifier	be		۲ Ad	Device dresse	s	Ir	nstru Opc	ictio ode:	n	/	DR/Ba Addres	ank ses		CS Rising
Edge	0	1	0	1	0	0	A1	A0	1	1	0	1	RB	RA	0	0	Edge

Increment/Decrement Wiper Counter Register (WCR) (Notes 5, 6, 7, 8, 9)

CS Falling	D	evice Iden	e Typ tifier	e		D Ado	evice dresse	s	l	nstru Opc	ictio ode	n	I A	DR/E	3ank esse	(S		In (Sei	crem nt by	ent/l Mas	Decr ster (reme on S	ent SDA)		CS Rising
Edge	0	1	0	1	0	0	A1	A0	0	0	1	0	Х	Х	0	0	I/D	I/D	-	·			I/D	I/D	Edge

Read Status Register (SR) (Note 5)

CS Falling	D	evice Iden	e Typ tifier	be		۲ Ad)evice dresse	s	Ir	nstru Opo	uctio code	n	I A	DR/E	Bank esse	(IS			(Ser	D nt by)ata / X9	Byte 271	e on S	SO)	CS Rising
Edge	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	Edge

NOTES:

5. "A1 ~ A0": stands for the device addresses sent by the master.

6. WCRx refers to wiper position data in the Wiper Counter Register.

7. "I": stands for the increment operation. SI held HIGH during active SCK phase (high).

8. "D": stands for the decrement operation. SI held LOW during active SCK phase (high).

9. "X:": Don't Care.

Absolute Maximum Ratings

Temperature Under Bias	65°C to +135°C
Voltage on SCK, any Address Input,	
with Respect to VSS	1V to +7V
$\Delta V = (VH - VL) \dots \dots$	5.5V
I _W (10 seconds)	±6mA
Supply Voltage (V _{CC}) Limits:	
X9271	
X9271-2.7	2.7V to 5.5V

Recommended Operating Conditions

Temperature Range (Commercial)	0°C to +70°C
Temperature Range (Industrial)	40°C to +85°C

Thermal Information

Maximum Storage Temperature Range	65°C to +150°C
Maximum Lead Temperature (Soldering 10s)	+300°C
Pb-Free Reflow Profile	see <u>TB493</u>

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

		LIMITS					
SYMBOL	PARAMETER	MIN (<u>Note 17</u>)	ТҮР	MAX (<u>Note 17</u>)	UNITS	TEST CONDITIONS	
R _{TOTAL}	End to End Resistance		50		kΩ	U version	
	End to End Resistance Tolerance			±20	%		
	Power Rating			50	mW	+25°C, each pot	
IW	Wiper Current			±3	mA		
R _W	Wiper Resistance			300	W	$I_W = \pm 3$ mA at $V_{CC} = 3V$	
R _W	Wiper Resistance			150	W	$I_W = \pm 3$ mA at V _{CC} = 5V	
V _{TERM}	Voltage on any R_H or R_L Pin	V _{SS}		v _{cc}	V	V _{SS} = 0V	
	Noise		-120		dBV/√Hz	Ref: 1V	
	Resolution		0.4		%		
	Absolute Linearity (<u>Note 10</u>)			±1	MI (<u>Note 12</u>)	R _{w(n)(actual) -} R _{w(n)(expected)} (<u>Note 14</u>)	
	Relative Linearity (<u>Note 11</u>)			±0.2	MI (<u>Note 12</u>)	$R_{w(n + 1)} - [R_{w(n) + MI}] (Note 14)$	
	Temperature Coefficient of RTOTAL		±300		ppm/°C		
	Ratiometric Temp. Coefficient			20	ppm/°C		
C _H /C _L /C _W	Potentiometer Capacitance		10/10/25		pF	See macro model	

Analog Characteristics Across recommended industrial operating conditions unless otherwise specified.

NOTES:

10. Absolute linearity is used to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

- 11. Relative linearity is used to determine actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
- 12. MI = RTOT / 255 or (R_H R_L) / 255, single pot.
- 13. During power-up, $V_{CC} > V_H$, V_L , and V_W .
- 14. n = 0, 1, 2, ..., 255; m = 0, 1, 2, ..., 254.



		LIMITS				
SYMBOL	PARAMETER	MIN (<u>Note 17</u>)	ТҮР	MAX (<u>Note 17</u>)	UNITS	TEST CONDITIONS
I _{CC1}	V _{CC} Supply Current (Active)			400	μA	f_{SCK} = 2.5MHz, SO = Open, V _{CC} = 6V Other Inputs = V _{SS}
I _{CC2}	V _{CC} Supply Current (Nonvolatile Write)		1	5	mA	f_{SCK} = 2.5MHz, SO = Open, V _{CC} = 6V Other Inputs = V _{SS}
I _{SB}	V _{CC} Current (Standby)			3	μA	$\frac{SCK = SI = V_{SS}, Addr. = V_{SS},}{CS} = V_{CC} = 6V$
I _{LI}	Input Leakage Current			10	μA	$V_{IN} = V_{SS}$ to V_{CC}
I _{LO}	Output Leakage Current			10	μA	$V_{OUT} = V_{SS}$ to V_{CC}
V _{IH}	Input HIGH Voltage	V _{CC} x 0.7		V _{CC} + 1	V	
VIL	Input LOW Voltage	-1		V _{CC} x 0.3	V	
V _{OL}	Output LOW Voltage			0.4	V	I _{OL} = 3mA
V _{OH}	Output HIGH Voltage	V _{CC} - 0.8			V	I_{OH} = -1mA, $V_{CC} \ge +3V$
V _{OH}	Output HIGH Voltage	V _{CC} - 0.4			V	I_{OH} = -0.4mA, $V_{CC} \le +3V$

D.C. Operating Characteristics Across the recommended operating conditions unless otherwise specified.

Endurance and Data Retention

PARAMETER	MIN. (<u>Note 17</u>)	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	Years

Capacitance

SYMBOL	TEST	MAX. (<u>Note 17</u>)	UNITS	TEST CONDITIONS
C _{IN/OUT} (<u>Note 15</u>)	Input / Output Capacitance (SI)	8	pF	V _{OUT} = 0V
C _{OUT} (<u>Note 15</u>)	Output Capacitance (SO)	8	pF	V _{OUT} = 0V
C _{IN} (<u>Note 15</u>)	Input Capacitance (A0, CS, WP, HOLD, and SCK)	6	pF	V _{IN} = 0V

Power-Up Timing

SYMBOL	PARAMETER	MIN. (<u>Note 17</u>)	MAX. (<u>Note 17</u>)	UNITS
t _r V _{CC} (<u>Note 15</u>)	V _{CC} Power-up Rate	0.2	50	V/ms
t _{PUR} (<u>Note 16</u>)	Power-up to Initiation of Read Operation		1	ms
t _{PUW} (<u>Note 16</u>)	Power-up to Initiation of Write Operation		50	ms

A.C. Test Conditions

INPUT PULSE LEVELS	V _{CC} x 0.1 to V _{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V _{CC} x 0.5

NOTES:

15. This parameter is not 100% tested.

16. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and are not 100% tested.

17. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



Equivalent A.C. Load Circuit



AC Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
f _{SCK}	SSI/SPI Clock Frequency		2.5	MHz
tCYC	SSI/SPI Clock Cycle Time	500		ns
t _{WH}	SSI/SPI Clock High Time	200		ns
t _{WL}	SSI/SPI Clock Low Time	200		ns
t _{LEAD}	Lead Time	250		ns
t _{LAG}	Lag Time	250		ns
t _{SU}	SI, SCK, HOLD and CS Input Setup Time	50		ns
t _H	SI, SCK, HOLD and CS Input Hold Time	50		ns
t _{RI}	SI, SCK, HOLD and CS Input Rise Time		2	μs
t _{FI}	SI, SCK, HOLD and CS Input Fall Time		2	μs
t _{DIS}	SO Output Disable Time	0	250	ns
t _V	SO Output Valid Time		200	ns
t _{HO}	SO Output Hold Time	0		ns
t _{RO}	SO Output Rise Time		100	ns
t _{FO}	SO Output Fall Time		100	ns
t _{HOLD}	HOLD Time	400		ns
t _{HSU}	HOLD Setup Time	100		ns
t _{НН}	HOLD Hold Time	100		ns
t _{HZ}	HOLD Low to Output in High Z		100	ns
t _{LZ}	HOLD High to Output in Low Z		100	ns
Τ _Ι	Noise Suppression Time Constant at SI, SCK, HOLD and CS Inputs		10	ns
t _{CS}	CS Deselect Time	2		μs
t _{WPASU}	WP, A0 Setup Time	0		ns
t _{WPAH}	WP, A0 Hold Time	0		ns

High-voltage Write Cycle Timing

SYMBOL	PARAMETER	ТҮР	MAX	UNITS
t _{WR}	High-voltage Write Cycle Time (Store Instructions)	5	10	ms



XDCP Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t _{WRPO}	Wiper Response Time After Third (Last) Power Supply is Stable	5	10	μs
t _{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)	5	10	μs

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Timing Diagrams

Input Timing



Output Timing





Hold Timing



XDCP Timing (for All Load Instructions)







Applications information

Basic Configurations of Electronic Potentiometers



3-terminal Potentiometer; Variable Voltage Divider



2-terminal Variable Resistor; Variable Current

Application Circuits



FIGURE 7. NONINVERTING AMPLIFIER



FIGURE 9. OFFSET VOLTAGE ADJUSTMENT



FIGURE 8. VOLTAGE REGULATOR



FIGURE 10. COMPARATOR WITH HYSTERESIS



Application Circuits (Continued)



 $v_0 = G v_S$ -1/2 $\leq G \leq +1/2$





FIGURE 13. INVERTING AMPLIFIER



FIGURE 12. FILTER



$$\begin{split} \mathsf{Z}_{\mathsf{IN}} = \mathsf{R}_2 + \mathsf{s} \; \mathsf{R}_2 \; (\mathsf{R}_1 + \mathsf{R}_3) \; \mathsf{C}_1 = \mathsf{R}_2 + \mathsf{s} \; \mathsf{Leq} \\ (\mathsf{R}_1 + \mathsf{R}_3) >> \mathsf{R}_2 \end{split}$$

FIGURE 14. EQUIVALENT L-R CIRCUIT



 $\label{eq:requency} \begin{array}{l} \mbox{Frequency} \propto R_1, \, R_2, \, C \\ \mbox{Amplitude} \propto R_A, \, R_B \end{array}$

FIGURE 15. FUNCTION GENERATOR



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 15, 2015	FN8174.5	 Updated Ordering Information Table on page 2. Added Revision History. Added About Intersil Verbiage.

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FN8174 Rev 5.00 October 15, 2015



Package Outline Drawing

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP) Rev 3, 10/09









NOTES:

- 1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
- 2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
- 3. Dimensions are measured at datum plane H.

SEE DETAIL "X"

0.09-0.20

0.90 +0.15/-0.10

0.05 MIN

0.15 MAX

END VIEW

DETAIL "X"

-1.00 REF-

GAUGE

PLANE

0°-8

0.60 ±0.15

0.25

- 4. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
 6. Dimension in () are for reference only.
- 7. Conforms to JEDEC MO-153, variation AB-1.





ООО "ЛайфЭлектроникс"

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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