VIDEO SWITCH FOR DVD RECORDER

■ GENERAL DESCRIPTION

The NJW1340 is a video switch for DVD recorders corresponding to the composite signal and Y/C signal.

It contains synchronous separation circuit and synchronous signal detection circuit, which are operating constantly. Therefore, It can detect a signal at the state of power save mode.

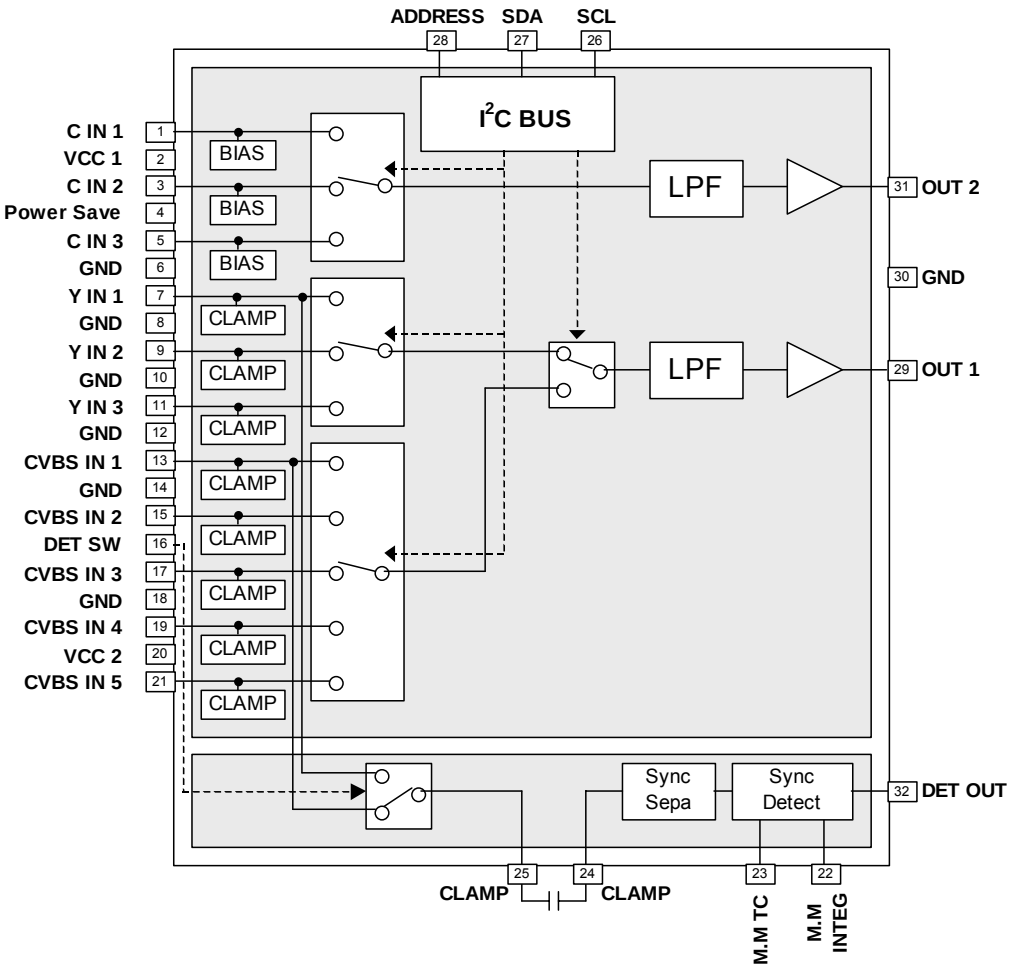
■ PACKAGE OUTLINE

NJW1340V

■ FEATURES

- Operating Voltage 4.5 to 5.5V
- I^2C BUS Interface
- 5-input 1-output video switch
- 3-input 1-output 2-circuit video switch
- 6th order Low Pass Filter
- Internal synchronous separation circuit
- Internal synchronous signal detection circuit
- Power Save Circuit
- Bi-CMOS Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	7.0	V
Power Dissipation	P_D	800(note1)	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(Note1) At on a board of EIA/JEDEC specification. (76.2 × 114.3 × 1.6mm Two layers, FR-4)

■ **RECOMMENDED OPEARATING CONDITION**(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr		4.5	5.0	5.5	V

■ **ELECTRICAL CHARACTERISTICS** (V^+=5.0V, R_L=10KΩ, Ta=25°C)

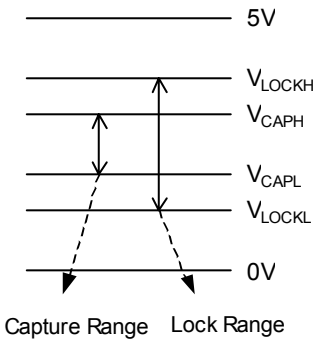
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	Icc	No signal	-	13.0	17.0	mA
Operating Current at Power Save	Isave	Power Save	-	5.0	6.5	mA
Maximum Output Voltage 1	Vom1	CLAMP Channel Vin=100kHz, 1.0Vp-p Sin signal, THD=1%	1.6	2.6	-	Vp-p
Maximum Output Voltage 2	Vom2	BIAS Channel Vin=100kHz, 1.0Vp-p Sin signal, THD=1%	1.6	2.9	-	Vp-p
Voltage Gain	Gv	Vin=1MHz, 1.0Vp-p Sin signal	-0.5	0.0	0.5	dB
Frequency Characteristic 1	Gf1	Vin=6MHz / 100kHz, 1.0Vp-p Sin signal	-0.5	0.0	0.5	dB
Frequency Characteristic 2	Gf2	Vin=27MHz / 100kHz, 1.0Vp-p Sin signal	-	-40	-24	dB
Cross talk 1	CTI	Vin=4.43MHz,1.0Vp-p Sin signal	-	-70	-	dB
Cross talk 2	CTB	Vin=4.43MHz,1.0Vp-p Sin signal	-	-70	-	dB
Differential Gain	DG	Vin=1.0Vp-p 10step Video signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p 10step Video signal	-	0.5	-	deg
S/N	SNv	Vin=1.0Vp-p,100% White Video Signal	-	65	-	dB
Sync Detection Level	V_{SYNC}	Vin=10step Video signal	-	80	-	mVp-p
Capture Voltage H	V_{CAPH}	(Note2)	2.07	2.22	2.37	V
Capture Voltage L	V_{CAPL}	(Note2)	1.57	1.72	1.87	V
Lock Voltage H	V_{LOCKH}	(Note2)	2.53	2.68	2.83	V
Lock Voltage L	V_{LOCKL}	(Note2)	1.25	1.40	1.55	V
DET OUT Output Voltage H	DetH		4.9	5.0	-	V
DET OUT Output Voltage L	DetL		-	0.1	0.3	V
Switch Change Voltage H	VthH		2.0	-	V^+	V
Switch Change Voltage L	VthL		0	-	0.6	V
ADR Voltage H	V_{ADRH}		3.5	-	5.0	V
ADR Voltage L	V_{ADRL}		0	-	1.0	V
Power Save SW Inflow Current H	I_{SWPH}	V=5V	150	220	300	μA
Power Save SW Inflow Current L	I_{SWPL}	V=0.3V	4.0	7.0	11.0	μA
DET SW Inflow Current H	I_{DETH}	V=5V	80	110	150	μA
DET SW Inflow Current L	I_{DETL}	V=0.3V	0.2	2.0	6.0	μA

■ **MODE SWITCH FUNCTON**

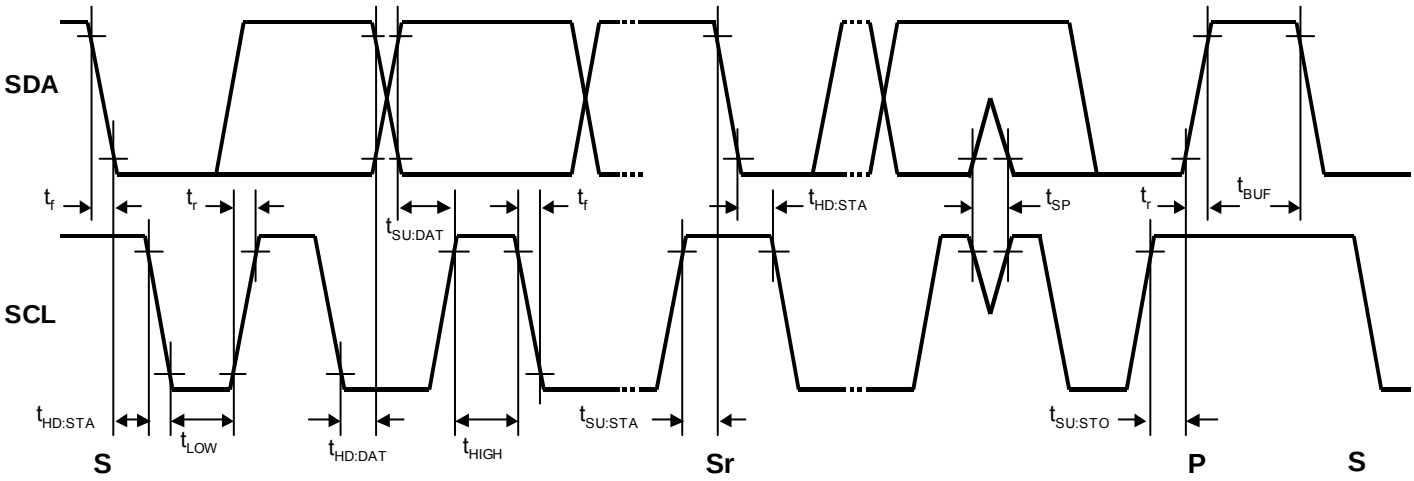
Power Save	Mode
H	Video switch block Power Save OFF (Active)
L	Video switch block Power Save ON (Mute)
OPEN	Video switch block Power Save ON (Mute)

DET SW	Mode
H	Y IN 1Select
L	CVBS IN 1 Select
OPEN	CVBS IN 1 Select

(Note2)



■TIMING ON THE I²C BUS (SDA,SCL)



■CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA,SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

PARAMETER	SYMBOL	Standard mode			UNIT
		MIN.	TYP.	MAX.	
Low Level Input Voltage	V_{IL}	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	3.0	-	5.0	V
Low level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	-10	-	10	μA

■CHARACTERISTICS OF BUS LINES (SDA,SCL) FOR I²C-BUS DEVICES

PARAMETER	SYMBOL	Standard mode			UNIT
		MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	kHz
Hold time (repeated) START condition.	$t_{HD:STA}$	4.0	-	-	μs
Low period of the SCL clock	t_{LOW}	4.7	-	-	μs
High period of the SCL clock	t_{HIGH}	4.0	-	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	μs
Data hold time NOTE)	$t_{HD:DAT}$	0	-	-	μs
Data set-up time	$t_{SU:DAT}$	250	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	μs
Capacitive load for each bus line	C_b	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	V

C_b ; total capacitance of one bus line in pF.

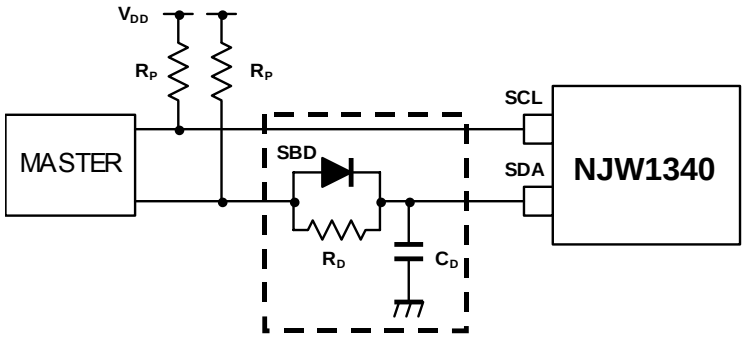
NOTE). Data hold time : $t_{HD:DAT}$

Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

The SDA block in the NJW1340 does not hold data. Add external data-delay-circuit of the SDA terminal, in case of not providing a hold time of at least 300nsec for the SDA in the master device.
The time-consists of the data-delay-circuit of the SDA terminal are as follows.

(a) Low level → High level: $T_{LH} \approx R_P * C_D$
(b) High level → Low level: $T_{HL} \approx R_D * C_D$

In addition, Schottky barrier diode (SBD) influences a Low level at the Acknowledge. Therefore choose the low forward voltage (Vf) as much as possible.



■I²C BUS FORMAT

	MSB	LSB		MSB	LSB		MSB	LSB		
S	Slave Address		A	Data		A	Data		A	P
1bit	8bit		1bit	8bit		1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

♦SLAVE ADDRESS

R/$\overline{W}$: Set the Write Mode or Read Mode.
ADR : Set the Slave Address by "ADR" terminal.

Slave Address								**Hex**
MSB							**LSB**	**-**
1	0	0	0	0	0	ADR	R/$\overline{W}$	-
◆ R/$\overline{W}$ = 0 : Write Mode, ADR = 0/1								**-**
1	0	0	1	0	1	0	0	94(h)
1	0	0	1	0	1	1	0	96(h)
◆ R/$\overline{W}$ = 1 : Read Mode, ADR = 0/1								**-**
1	0	0	1	0	1	0	1	95(h)
1	0	0	1	0	1	1	1	97(h)

♦CONTROL REGISTER TABLE

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	SEL SW1	SEL SW2	SEL SW3	✳	✳	✳	✳	✳

✳ : Don't Care

♦CONTROL REGISTER DEFAULT VALUE

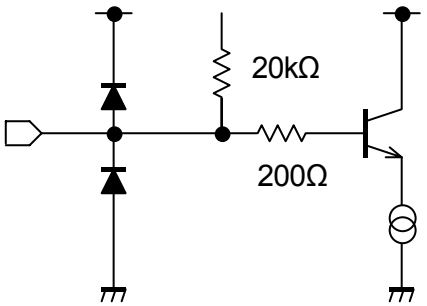
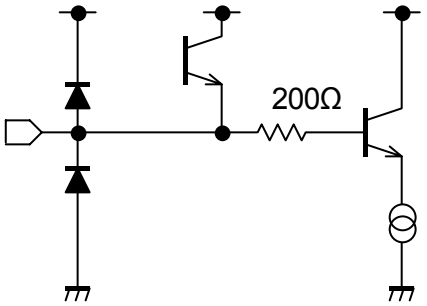
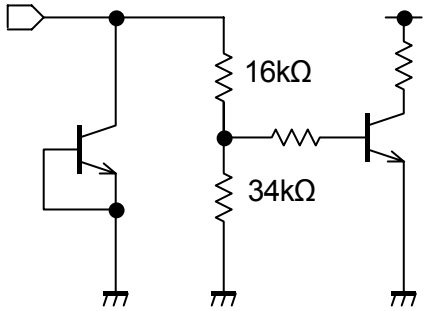
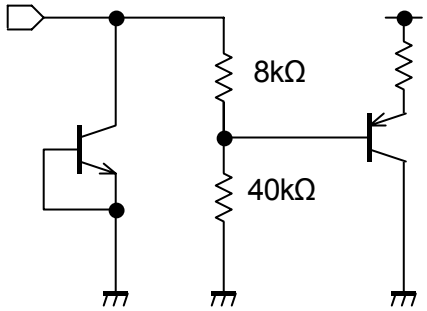
Control register default value is all "0".

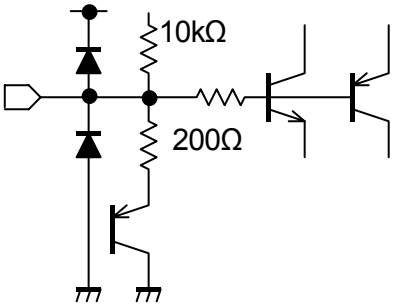
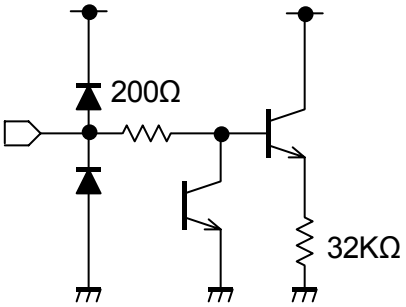
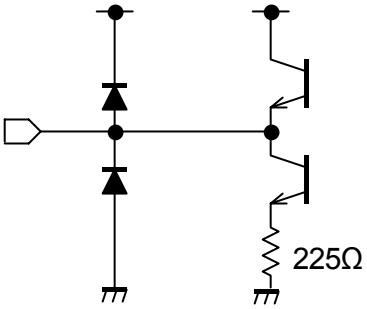
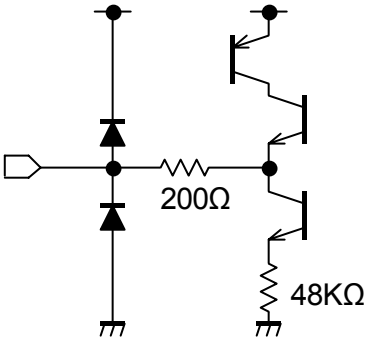
No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	0	0	0	0	0	0	0	0

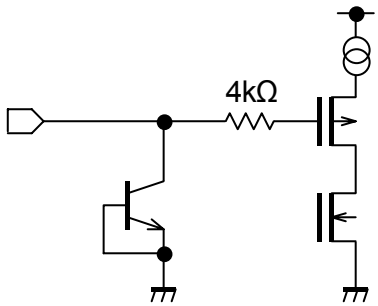
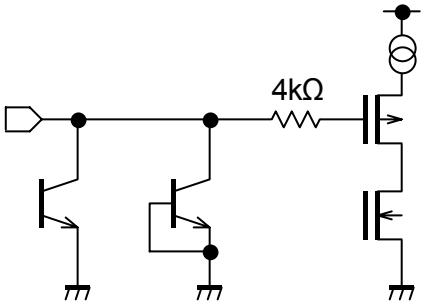
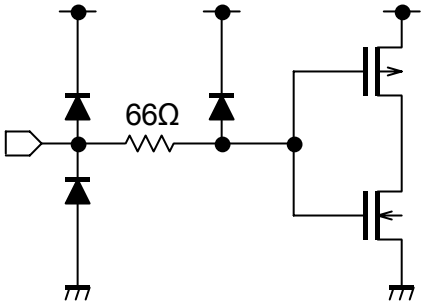
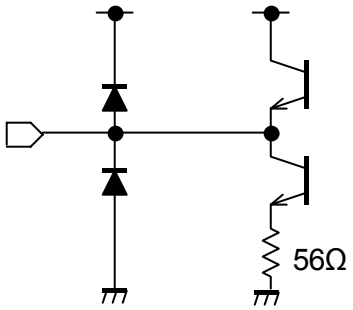
■INSTRUCTION CODE

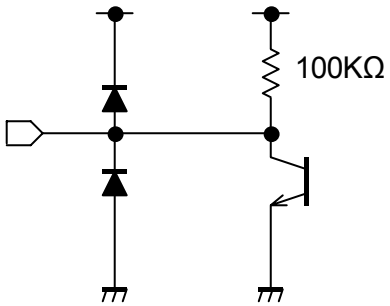
SEL SW1	SEL SW2	SEL SW3	OUT1	OUT2
0	0	0	CVBS IN1	C IN 1
0	0	1	CVBS IN2	C IN 1
0	1	0	CVBS IN3	C IN 1
0	1	1	CVBS IN4	C IN 1
1	0	0	CVBS IN5	C IN 1
1	0	1	Y IN 1	C IN 1
1	1	0	Y IN 2	C IN 2
1	1	1	Y IN 3	C IN 3

■**EQUIVALENT CIRCUIT**

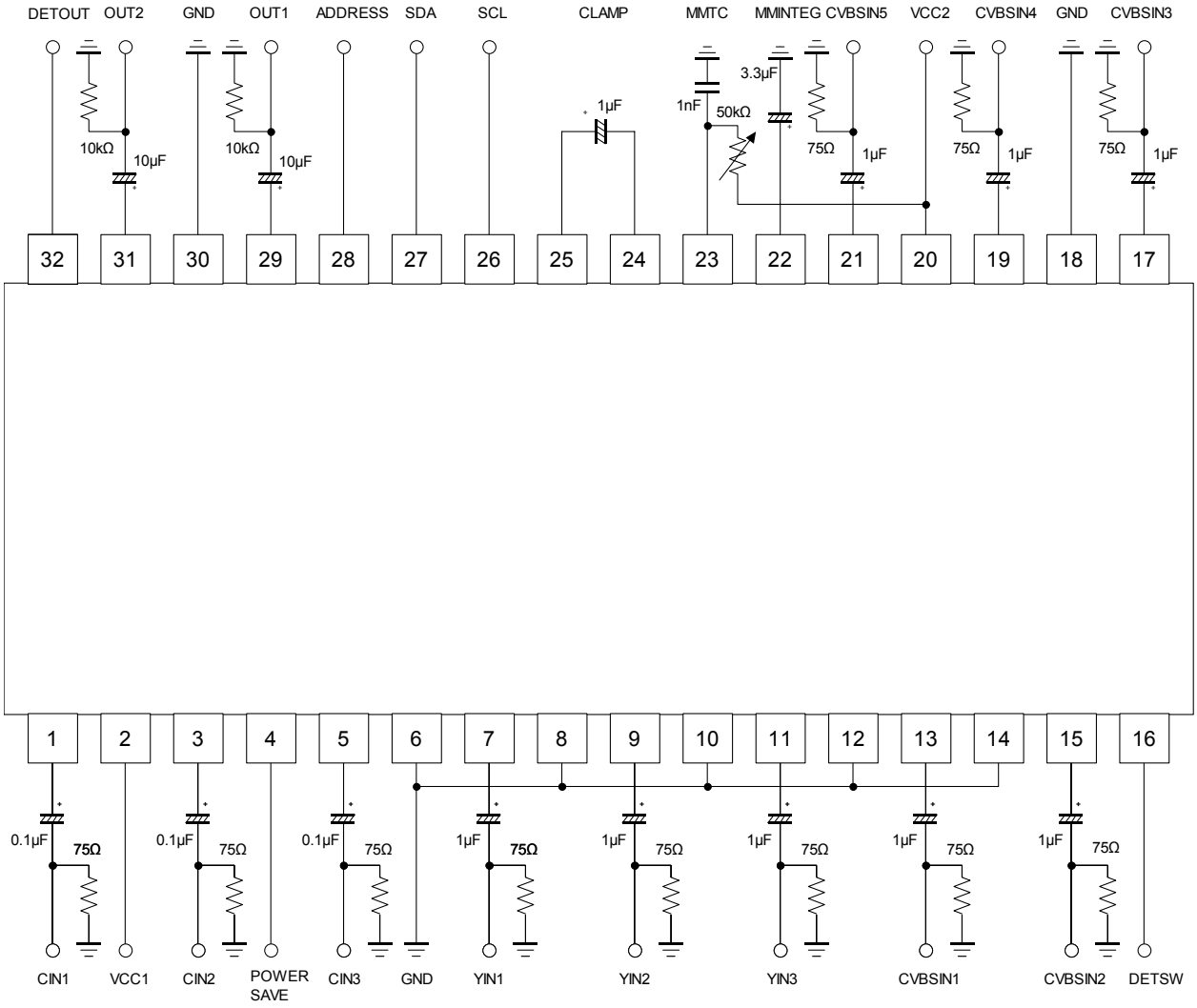
No.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
1 3 5	CIN1 CIN2 CIN3	Chroma signal input		2.8V
7 9 11 13 15 17 19 21	YIN1 YIN2 YIN3 CVBSIN1 CVBSIN2 CVBSIN3 CVBSIN4 CVBSIN5	Y signal input, YIN1 correspond to the synchronous detection at the power saving mode. Composite video signal input, CVBSIN1 correspond to the synchronous detection at the power saving mode.		2.5V
4	POWER SAVE	Power Save control		
16	DETSW	Signal detection control, Y IN1 or CVBS IN1		

No.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
22	MMINTEG	Capacitor connection for smoothing mono multi.		
23	MMTC	Capacitor and resistance connection for mono multi time constant. The accuracy of external resistance recommends within ±5%.		
24	CLAMP	Capacitor connection for CLAMP		0.9V
25	CLAMP	Capacitor connection for CLAMP		1.3V

No.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
26	SCL	I^2C clock		
27	SDA	I^2C data		
28	ADDRESS	Slave address setting		
29 31	OUT1 OUT2	Composite video signal, Y signal output Chroma signal output		0.9V 2.0V

No.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
29	DETOUT	Detection signal output. The synchronous detection result output at the power saving mode.		
6 8 10 12 14 18 30	GND	GND		
20	VCC1 VCC2	Vcc		

■TEST CIRCUIT

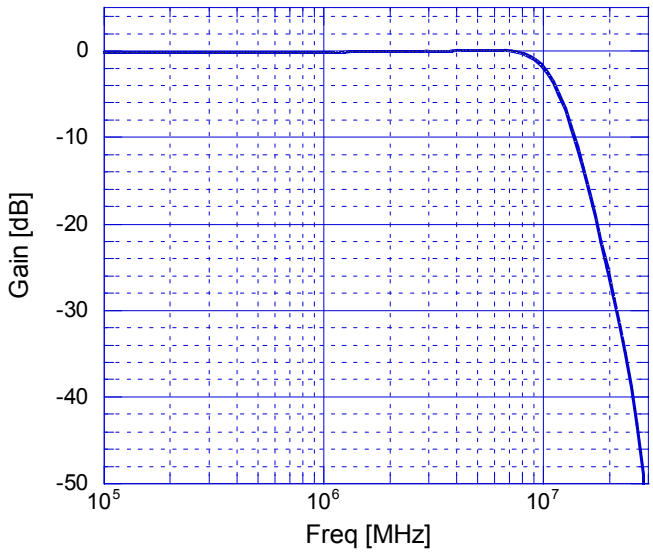


(Note) It the following refers when the synchronous signal detection unused.

16pin DETSW	OPEN
22pin MMINTEG	OPEN
23pin MMTC	OPEN
24pin CLAMP	OPEN
25pin CLAMP	OPEN
32pin DETOUT	OPEN

■TYPICAL CHARACTERISTICS

Voltage Gain vs Frequency



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