AUTOMOTIVE GRADE

CS3706

Dual Output Driver

Description

The CS3706 integrated circuit provides an interface between low-level TTL inputs and high-power switching devices such as power MOSFETs. A typical application is single-ended PWM control to push-pull power control conversion.

The primary function of this device is to convert a bipolar single-ended low current digital input to a pair of totem pole outputs which can source or sink up to 1.5A. An internal flip-flop, driven by double-pulse suppression logic, can be enabled to provide single-ended to push-pull conversion. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control and thermal shutdown.

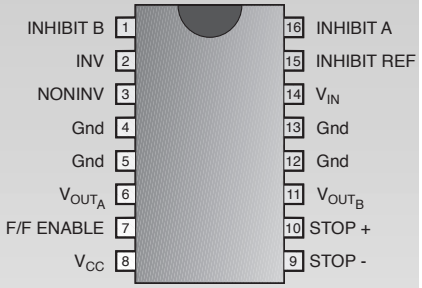
Features

- **Dual 1.5A Totem Pole Outputs**
- **40nsec Rise and Fall into 1000pF**
- **Parallel or Push-Pull Operation**
- **Single-Ended to Push-Pull Conversion**
- **High-Speed Power MOSFET Compatible**
- **Low Cross-Conduction Current Spike**
- **Analog Latched Shutdown**
- **Internal Deadband Inhibit Circuit**
- **Low Quiescent Current**
- **5V to 40V Operation**
- **Thermal Shutdown Protection**

Package Options

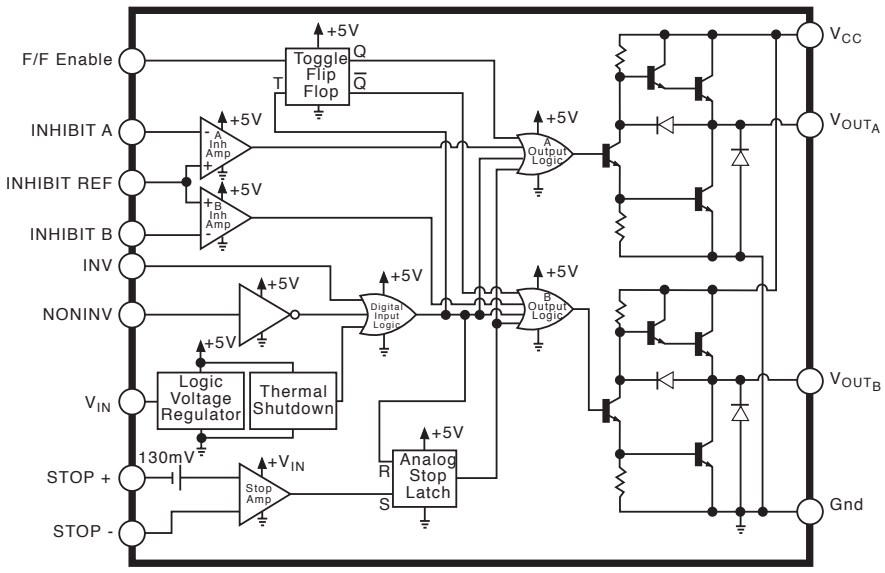
16 Lead PDIP

(Internally Fused Leads)



Note: All Four Ground Pins must be Connected to Common Ground.

Block Diagram



Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

Logic Supply Voltage (V_{IN}) 40.0V
Output Supply Voltage (V_{CC}) 40.0V
Output Current (each output, source, or sink)
- Steady State ..... ±500mA
- Peak Transient for Less Than 100μs ..... ±1.5A
- Capacitive Discharge Energy 20.0μJ

Digital Inputs (INV, NONINV) 5.5V
Analog Inputs (STOP +, STOP -) ..... V_{IN}
Inhibit Inputs (INHIBIT A, INHIBIT B, INHIBIT REF) 5.5V
Operating Temperature Range ..... 0 to 70˚C
Storage Temperature Range ..... -65 to 150˚C
Lead Temperature Soldering
- Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak

Notes: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.

Electrical Characteristics: These specifications apply over the operating temperature range of the IC. ($V_{IN} = V_{CC} = 20V$, Pins 4, 5, 12 &13 = 0V; unless otherwise stated.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Supply Current	V_{IN} = 40V, V_{CC} = 20V, INV = 0V, Unused pins = open.		8	12	mA
V_{CC} Supply Current	V_{IN} = 20V, V_{CC} = 40V, Outputs low		3	5	mA
V_{CC} Leakage Current	V_{IN} = 0V, V_{CC} = 40V		0.05	0.10	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Digital Input Current	V_I = 0V		-0.6	-1.0	mA
Digital Input Leakage	V_I = 5V		0.05	0.10	mA
Output High Sat., V_C-V_{OUT}	I_{OUT} = -50mA			2.0	V
Output High Sat., V_C-V_{OUT}	I_{OUT} = -500mA			2.5	V
Output Low Sat., V_{OUT}	I_{OUT} = 50mA			0.4	V
Output Low Sat., V_{OUT}	I_{OUT} = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
Inhibit Threshold	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0V		-10	-20	μA
Analog Threshold	V_{CM} = 0V to 15 V	100	130	150	mV
Analog Input Bias Current	V_I = 0V, V_{CM} = 15V		-10	-20	μA
Thermal Shutdown	Turn on		155		˚C
Thermal Shutdown	Turn off		125		˚C

Typical Switching Characteristics: (V_{IN} = V_{CC} = 20V, T_A = 25°C. Delays measured 50% in to 50% out.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction	Output Rise	25			ns
Current Spike Duration	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (-) Input = 0 to 0.5V	180			ns

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L PDIP *(Internally Fused Leads)*		
1	INHIBIT B	Control pin for deadband control on Channel B.
2	INV	Inverting input for output drivers.
3	NONINV	Noninverting input for output drivers.
4	Gnd	Ground.
5	Gnd	Ground.
6	$V_{OUT(A)}$	Channel A output.
7	F/F ENABLE	Controls the phase of the two outputs. F/F ENABLE = Gnd Out of phase. F/F ENABLE = floating In phase.
8	V_{CC}	Supply voltage (5V to 40V) for output drivers.
9	STOP -	Inverting input for stop latch comparator.
10	STOP +	Noninverting input for stop latch comparator.
11	$V_{OUT(B)}$	Channel B output.
12	Gnd	Ground.
13	Gnd	Ground.
14	V_{IN}	Supply voltage (5V to 40V) for IC (except output driver).
15	INHIBIT REF	Reference input for deadband control.
16	INHIBIT A	Control pin for deadband control on channel A.

Circuit Description

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_{CC} pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding F/F Enable activates the internal flip-flop to alternate the two outputs. With pin open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec. must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs–the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning on until the other has turned-off. The threshold is determined by the voltage on INHIBIT REF which can be set from 0.5 to 3.5 V. When this circuit is not used, ground INHIBIT REF and leave INHIBIT A&B open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} - 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply, however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_{CC}. When combined with a CS384X PWM, the Driver Bias switch can be used to supply V_{IN} to the CS3706. V_{IN} switching should be fast as undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

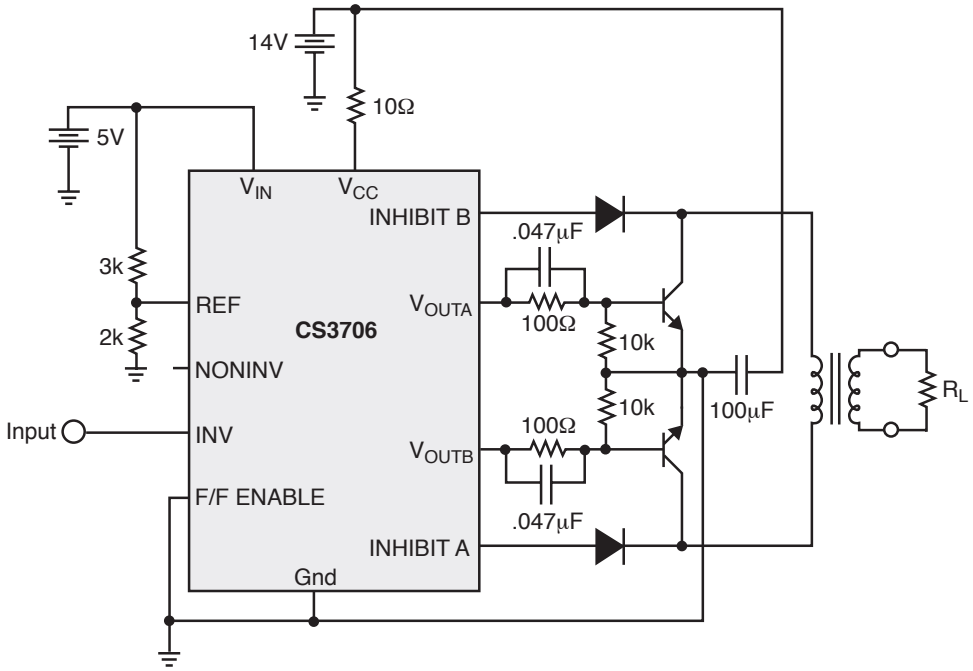
Should the chip temperature reach approximately 155˚C, a parallel, non-inverting input is activated driving both outputs to the low state.

Truth Table

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.
$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

Application Diagram



Package Specification

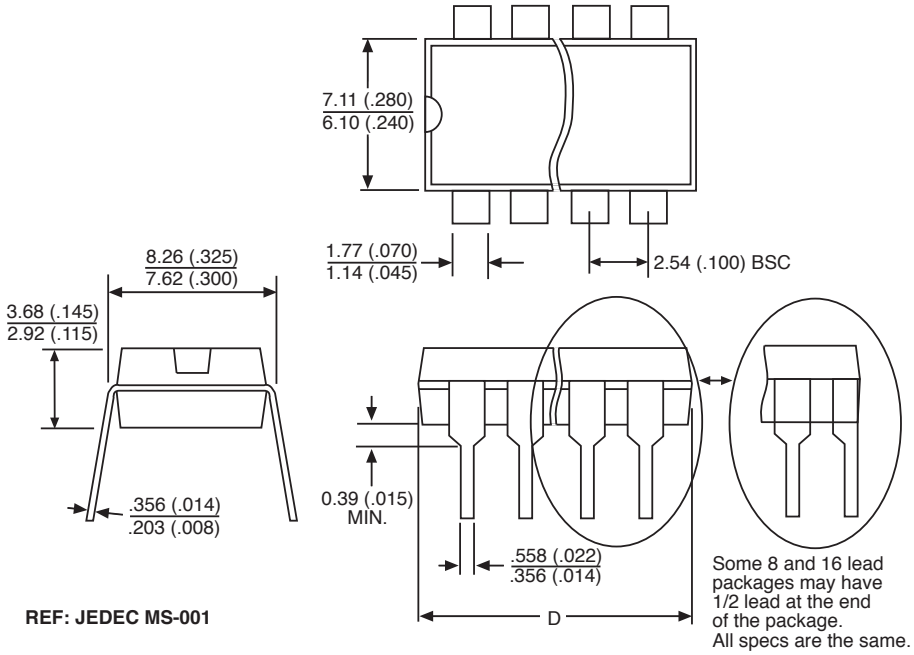
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP *(Internally Fused Leads)*	19.69	18.67	.775	.735

PACKAGE THERMAL DATA

Thermal Data		16 Lead PDIP *(Internally Fused Leads)*	
$R_{\Theta JC}$	typ	15	°C/W
$R_{\Theta JA}$	typ	50	°C/W

Plastic DIP (N); 300 mil wide



Ordering Information

Part Number	Description
CS3706GNF16	16 Lead PDIP *(Internally Fused Leads)*

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru