

General Description

The 8S89200 is a high speed 1-to-8 Differential-to-LVDS Clock Divider and is part of the high performance clock solutions from IDT. The 8S89200 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential inputs and V_{REF_AC} pins allow other differential signal families such as LVPECL, LVDS and CML to be easily interfaced to the input with minimal use of external components.

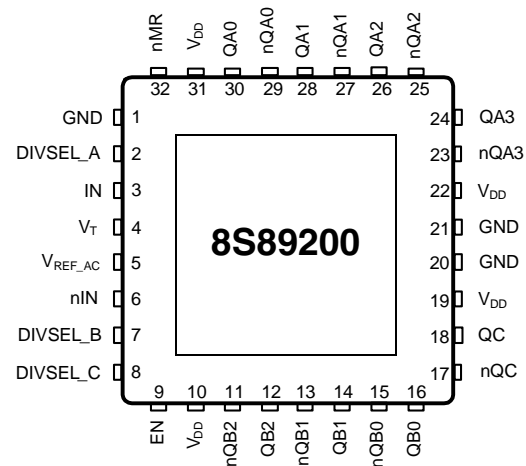
The device also has a selectable $\div 1$, $\div 2$, $\div 4$ output divider, which can allow the part to support multiple output frequencies from the same reference clock.

The 8S89200 is packaged in a small 5mm x 5mm 32-pin VFQFN package which makes it ideal for use in space-constrained applications.

Features

- Three output banks, consisting of eight LVDS output pairs total
- INx, nINx inputs can accept the following differential input levels: LVPECL, LVDS, CML
- Selectable output divider values of $\div 1$, $\div 2$ and $\div 4$
- Maximum output frequency: 1.5GHz
- Maximum input frequency: 3GHz
- Bank Skew: 10ps (typical)
- Part-to-part skew: 100ps (typical)
- Additive phase jitter, RMS: 0.170ps (typical)
- Propagation delay: 802ps (typical)
- Output rise time: 150ps (typical)
- $2.5V \pm 5\%$ operating supply voltage
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



32-Lead 5mm x 5mm VFQFN

Block Diagram

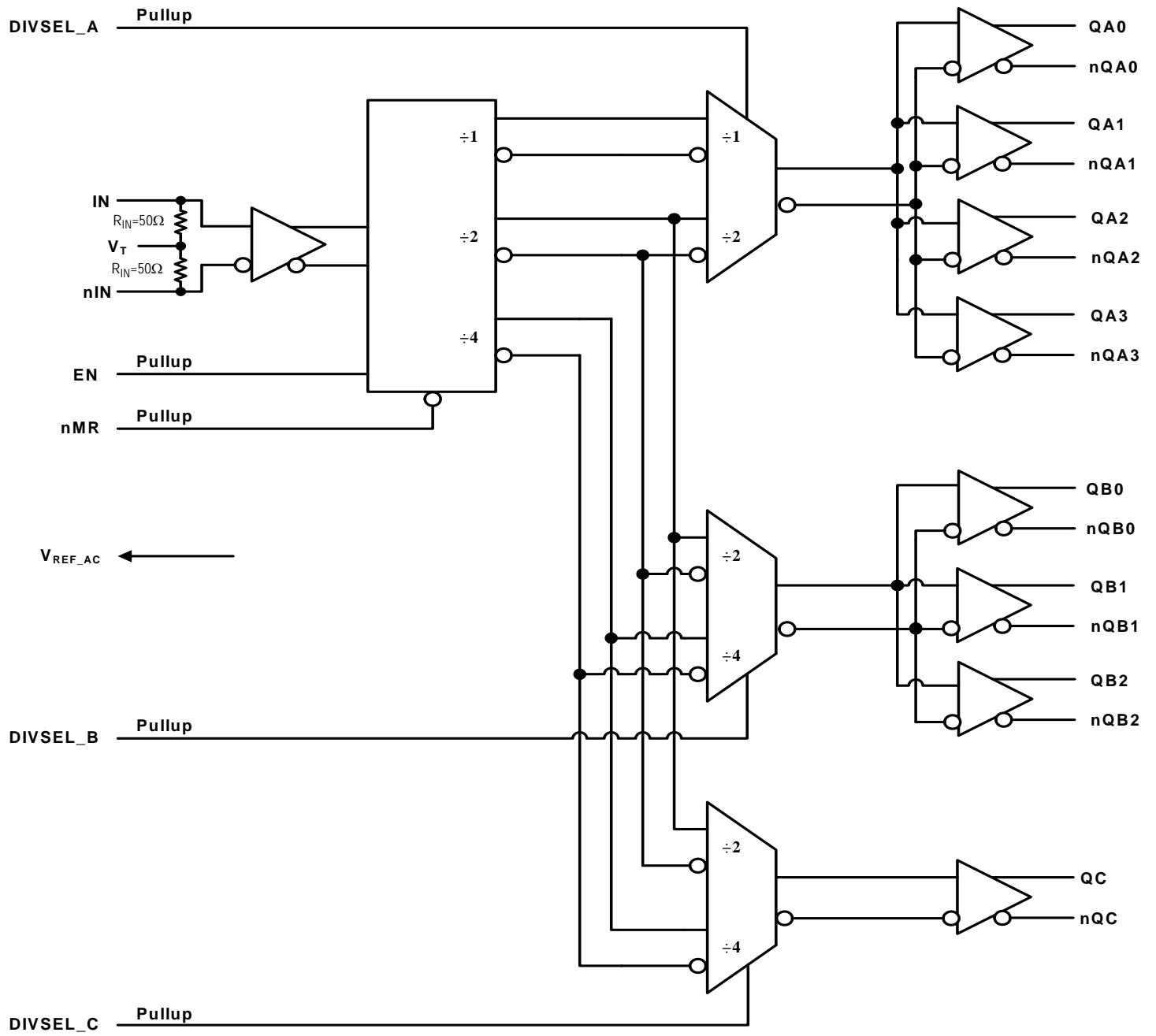


Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------------|---------------|--------|--------|--|
| 1, 20, 21 | GND | Power | | Ground supply pins. |
| 2 | DIVSEL_A | Input | Pullup | Output divider select pin. Controls output divider settings for Bank A. See Table 3 for additional information. LVCMOS/LVTTL interface levels. |
| 3 | IN | Input | | Non-inverting differential LVPECL clock input. $R_{IN} = 50\Omega$ termination to V_T . |
| 4 | V_T | Input | | Termination center-tap input. |
| 5 | V_{REF_AC} | Output | | Reference voltage for AC-coupled applications. |
| 6 | nIN | Input | | Inverting differential LVPECL clock input. $R_{IN} = 50\Omega$ termination to V_T . |
| 7 | DIVSEL_B | Input | Pullup | Output divider select pin. Controls output divider settings for Bank B. See Table 3 for additional information. LVCMOS/LVTTL interface levels. |
| 8 | DIVSEL_C | Input | Pullup | Output divider select pin. Controls output divider settings for Bank C. See Table 3 for additional information. LVCMOS/LVTTL interface levels. |
| 9 | EN | Input | Pullup | Output enable pin. See Table 3 for additional information. LVCMOS/LVTTL interface levels. |
| 10, 19, 22, 31 | V_{DD} | Power | | Positive supply pins. |
| 11, 12 | nQB2, QB2 | Output | | Differential output pair. LVDS interface levels. |
| 13, 14 | nQB1, QB1 | Output | | Differential output pair. LVDS interface levels. |
| 15, 16 | nQB0, QB0 | Output | | Differential output pair. LVDS interface levels. |
| 17, 18 | nQC, QC | Output | | Differential output pair. LVDS interface levels. |
| 23, 24 | nQA3, QA3 | Output | | Differential output pair. LVDS interface levels. |
| 25, 26 | nQA2, QA2 | Output | | Differential output pair. LVDS interface levels. |
| 27, 28 | nQA1, QA1 | Output | | Differential output pair. LVDS interface levels. |
| 29, 30 | nQA0, QA0 | Output | | Differential output pair. LVDS interface levels. |
| 32 | nMR | Input | Pullup | Master Reset. See Table 3 for additional information. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

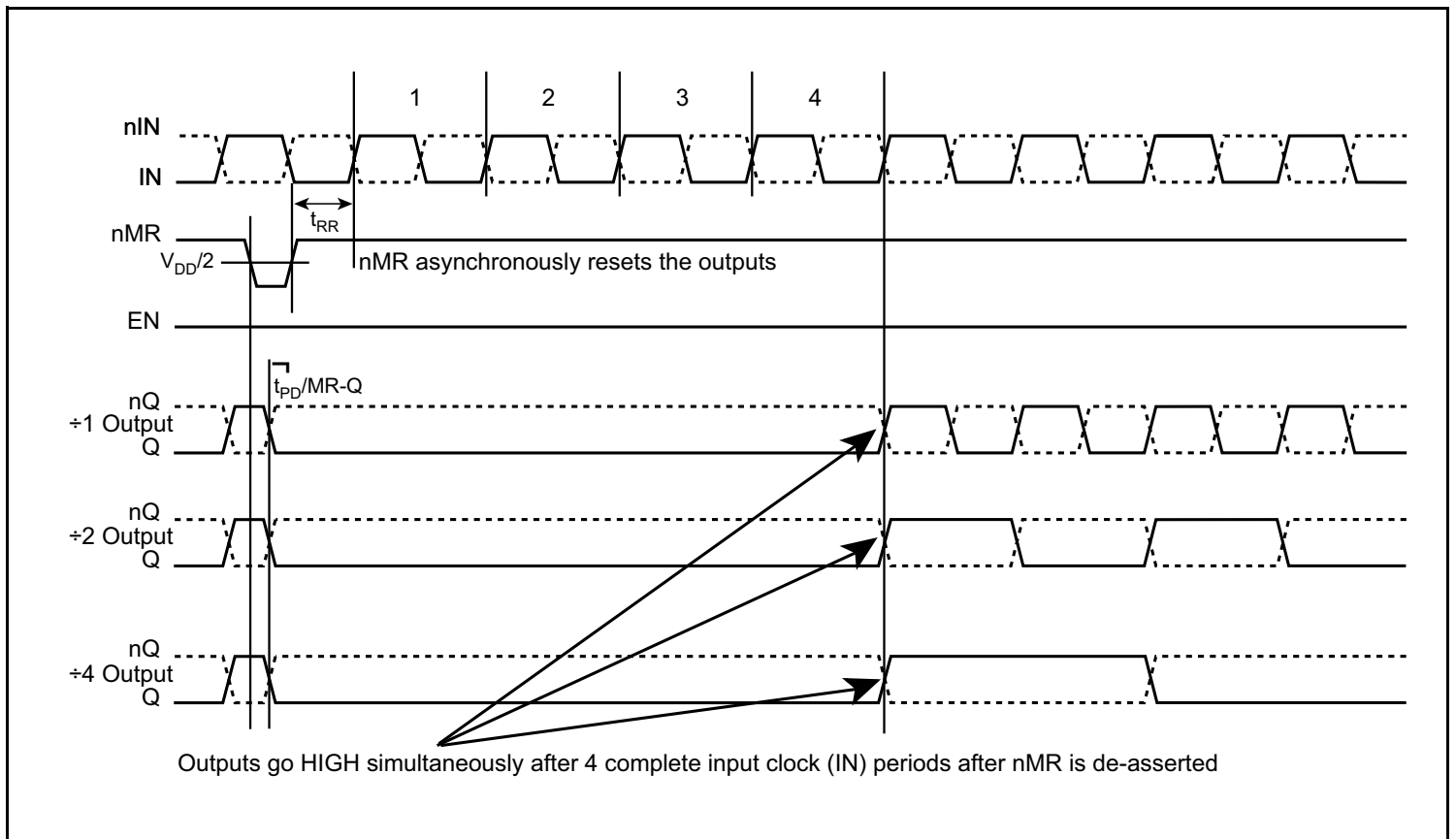
Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|-----------------------|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 2 | | pF |
| R_{PULLUP} | Input Pullup Resistor | | | 25 | | k Ω |

Function Tables

Table 3. SEL Function Table

| nMR | EN | DIVSEL_A | DIVSEL_B | DIVSEL_C | Output Bank A | Output Bank B | Output Bank C |
|-----|-----|----------|----------|----------|---------------|---------------|---------------|
| 0 | n/a | n/a | n/a | n/a | 0 | 0 | 0 |
| 1 | 0 | n/a | n/a | n/a | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | ÷1 | ÷2 | ÷2 |
| 1 | 1 | 1 | 1 | 1 | ÷2 | ÷4 | ÷4 |


Figure 1A. Reset with Output Enabled

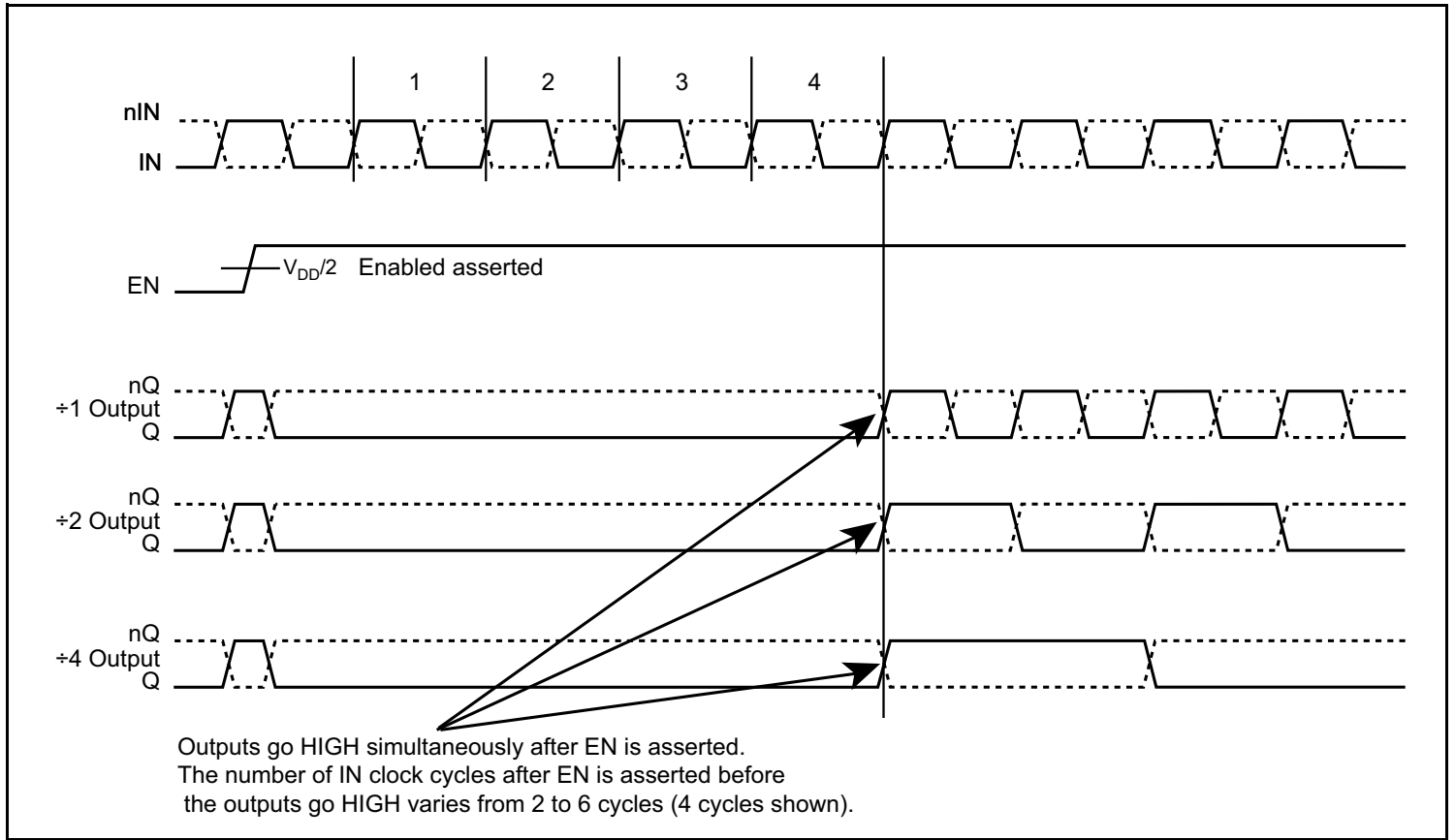


Figure 1B. Enabled Timing

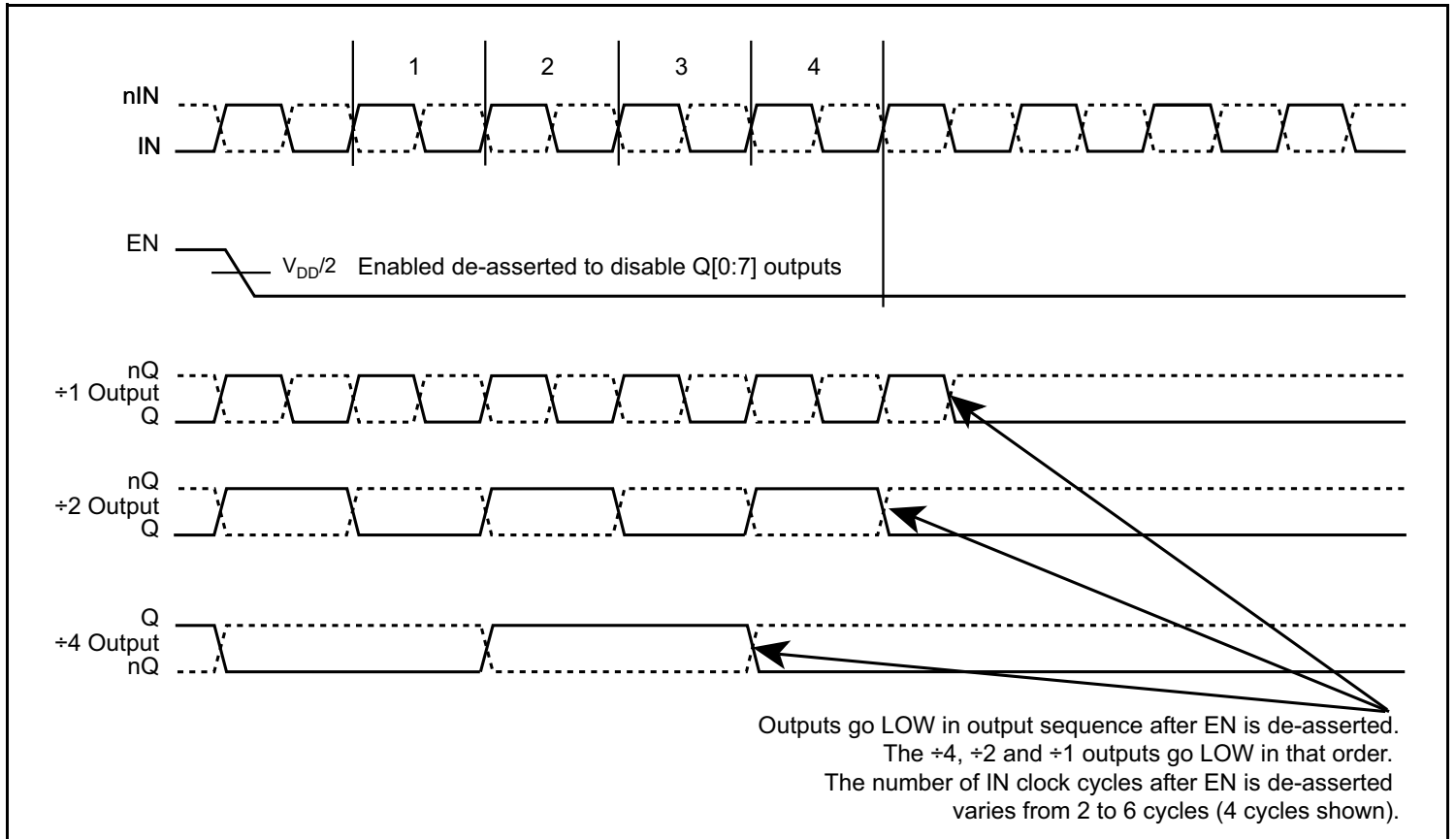


Figure 1C. Disabled Timing

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 10mA 15mA |
| Input Current, I_{IN} , nIN | $\pm 50mA$ |
| V_T Current, I_{VT} | $\pm 100mA$ |
| Input Sink/Source, I_{REF_AC} | $\pm 2mA$ |
| Package Thermal Impedance, θ_{JA} | 42.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | 280 | 311 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 2.625V$ | -125 | | 20 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 2.625V, V_{IN} = 0V$ | | | -300 | μA |

Table 4C. Differential DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|----------------------------------|-----------------|-----------------|----------------|-----------------|----------|
| R_{IN} | Input Resistance | I_{IN}, nIN | | 50 | | Ω |
| V_{IH} | Input High Voltage | I_{IN}, nIN | 0.15 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | I_{IN}, nIN | 0 | | $V_{DD} - 0.15$ | V |
| V_{IN} | Input Voltage Swing | | 0.15 | | 1.2 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing | | 0.3 | | 2.4 | V |
| V_{REF_AC} | Bias Voltage | | $V_{DD} - 1.34$ | $V_{DD} - 1.3$ | $V_{DD} - 1.18$ | V |

Table 4D. LVDS DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 312 | 375 | 483 | mV |
| ΔV_{OD} | VOD Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.14 | 1.25 | 1.40 | V |
| ΔV_{OS} | VOS Magnitude Change | | | | 50 | mV |

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---|--|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | | | 1.5 | GHz |
| f_{IN} | Input Frequency | | | | 3 | GHz |
| t_{PD} | Propagation Delay; NOTE 1 | IN to Qx | 650 | 802 | 935 | ps |
| | | nMR to Qx | 500 | 725 | 965 | ps |
| $tsk(b)$ | Bank to Bank Skew; NOTE 2, 3 | Same divide setting | | 10 | 55 | ps |
| $tsk(w)$ | Bank to Bank Skew; NOTE 2, 3 | Different divide setting | | 80 | 150 | ps |
| $tsk(o)$ | Within-Bank Skew; NOTE 2, 4 | Within same fanout bank | | 4 | 25 | ps |
| $tsk(pp)$ | Part-to-Part Skew; NOTE 2, 5 | | | | 250 | ps |
| τ_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section | 156.25MHz, Integration Range: 12kHz to 20MHz | | 0.170 | 0.214 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 80 | 150 | 210 | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

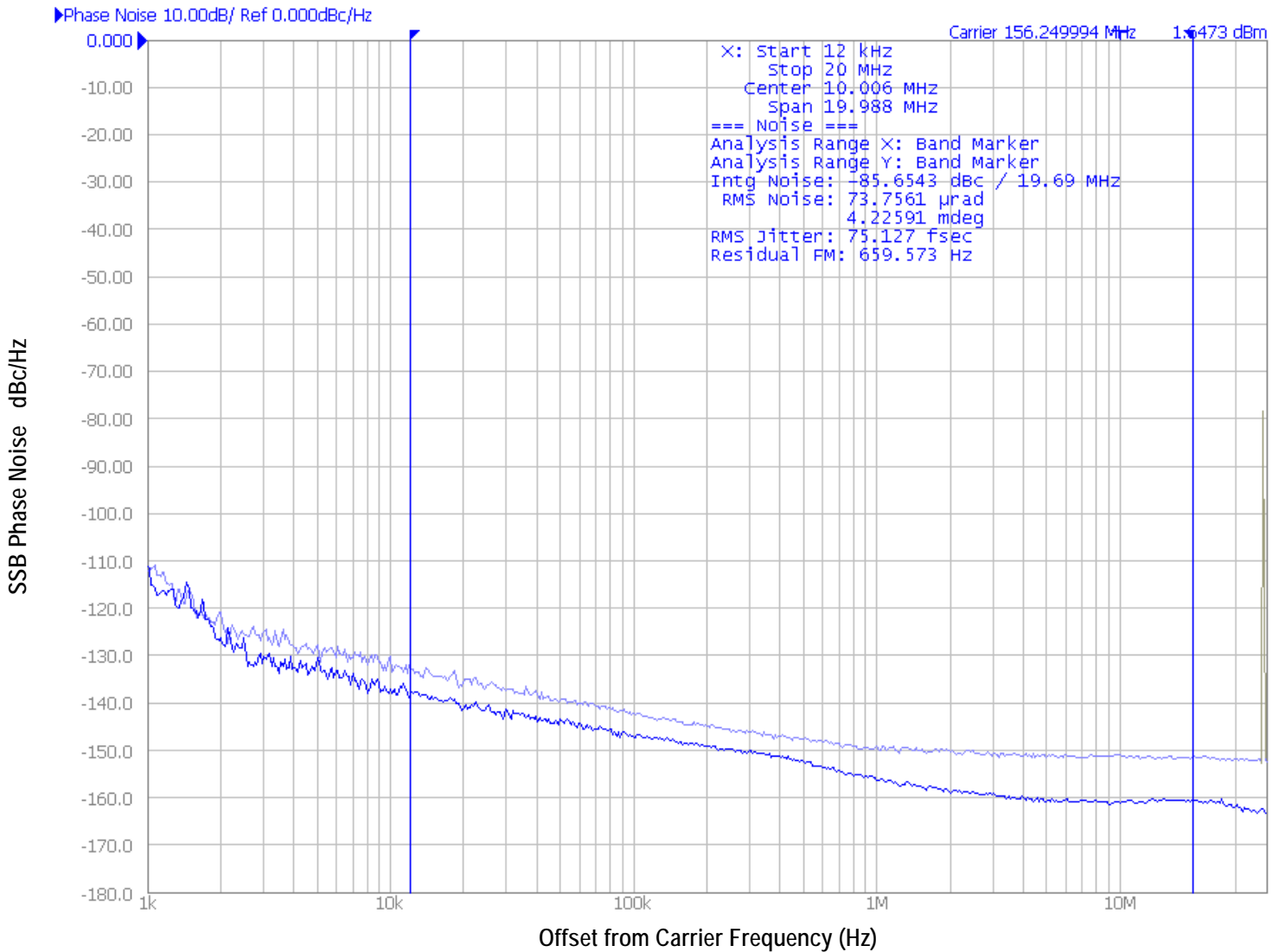
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

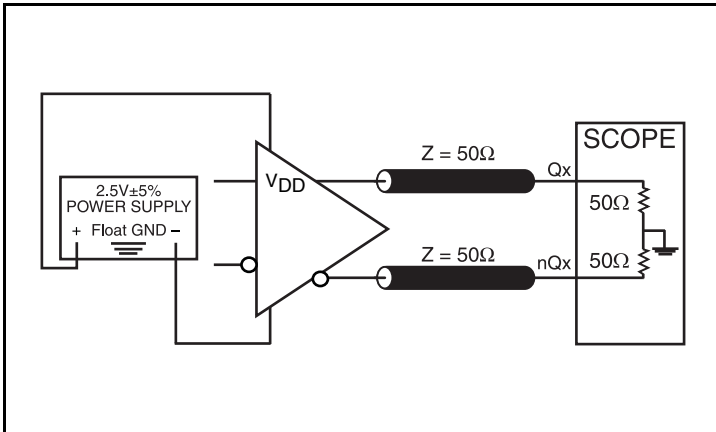
fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



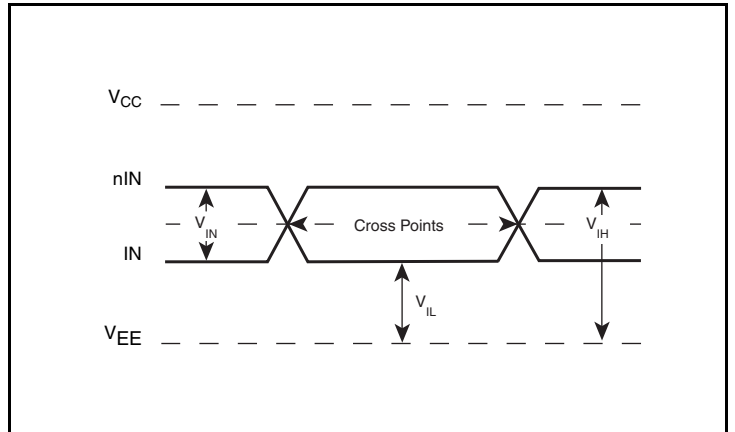
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.

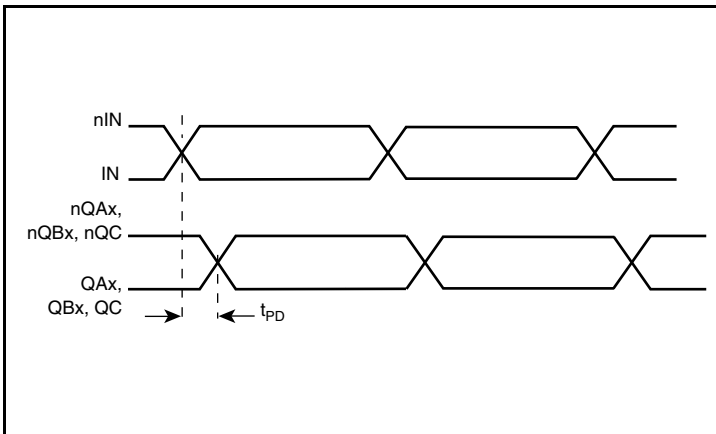
Parameter Measurement Information



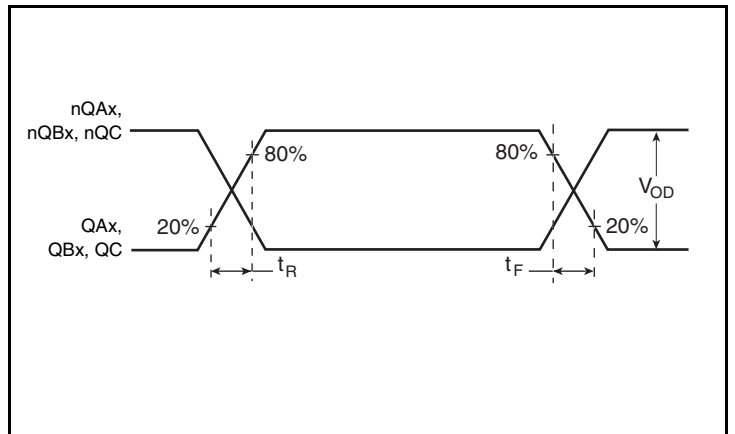
Output Load AC Test Circuit



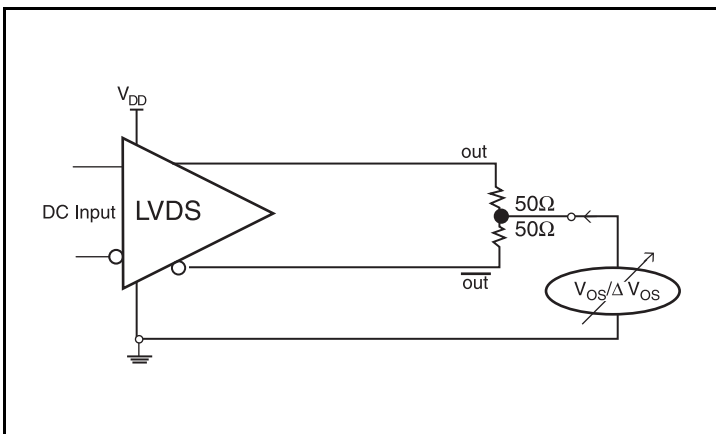
Input Levels



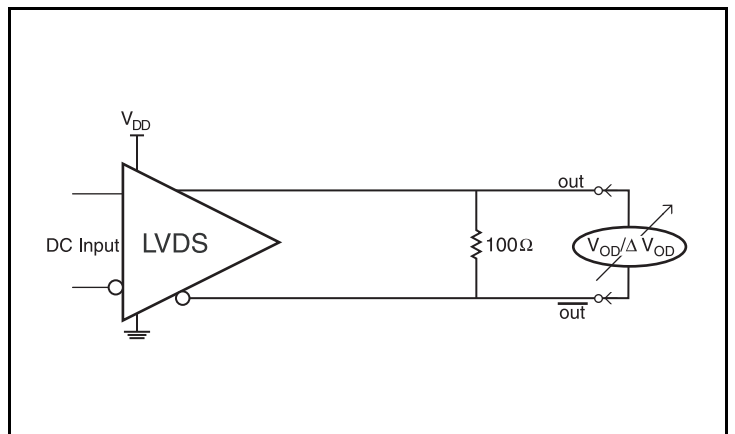
Propagation Delay



Output Rise/Fall Time

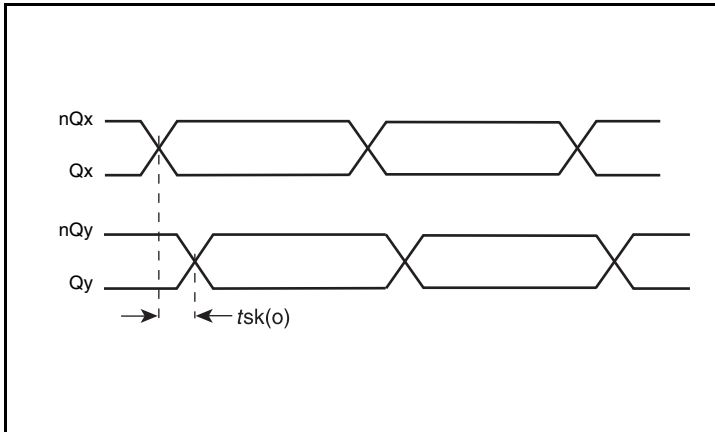


Offset Voltage Setup

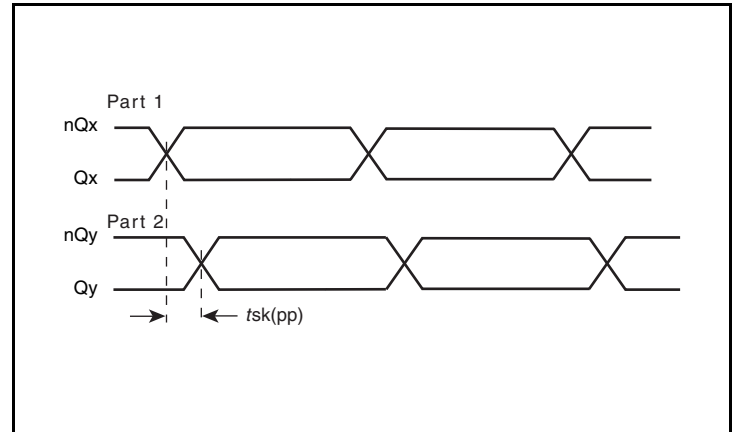


Differential Output Voltage Setup

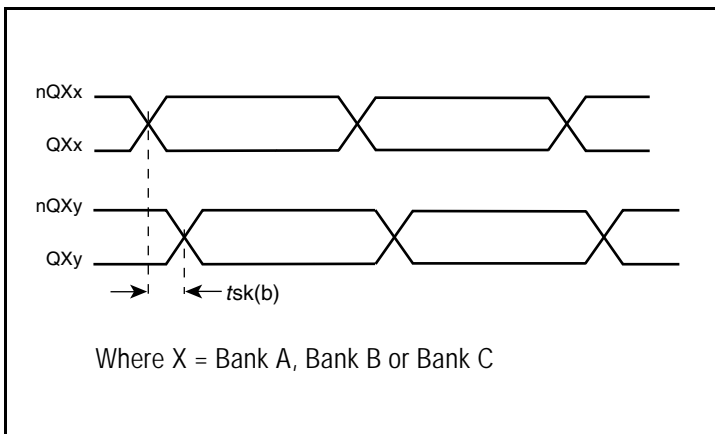
Parameter Measurement Information, continued



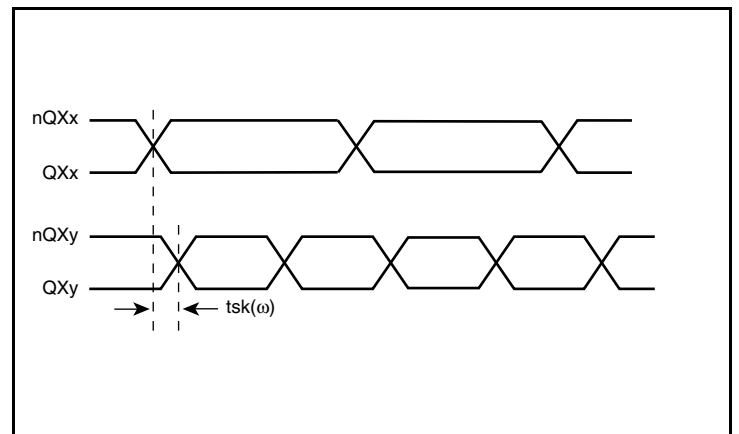
Within Bank Skew



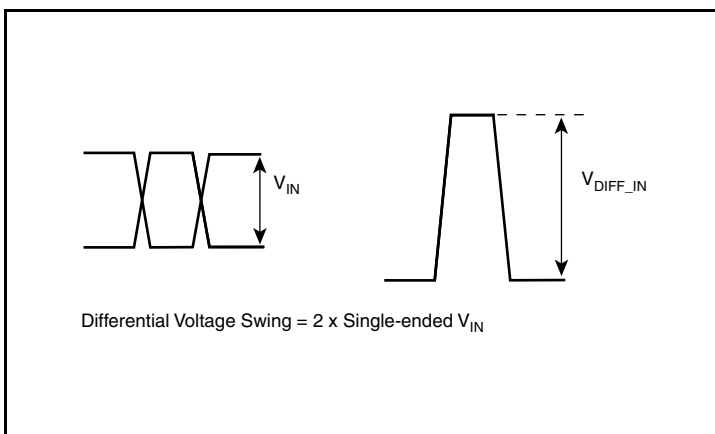
Part-to-Part Skew



Bank to Bank Skew (same divide setting)



Bank to Bank (different divide settings)



Single-Ended & Differential Input Swing

Applications Information

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by

the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

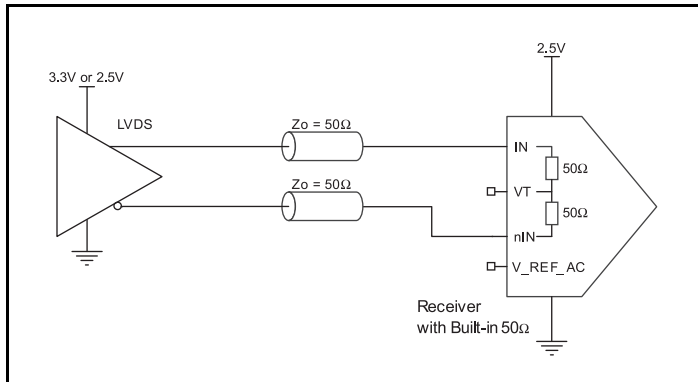


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

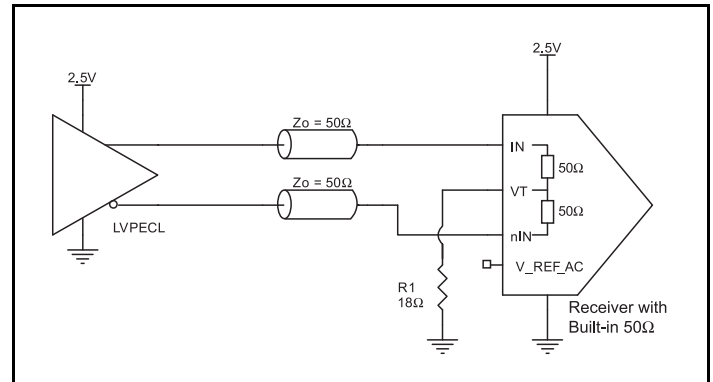


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

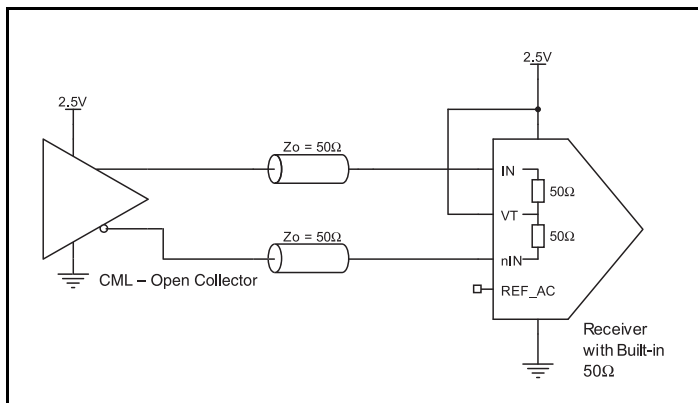


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

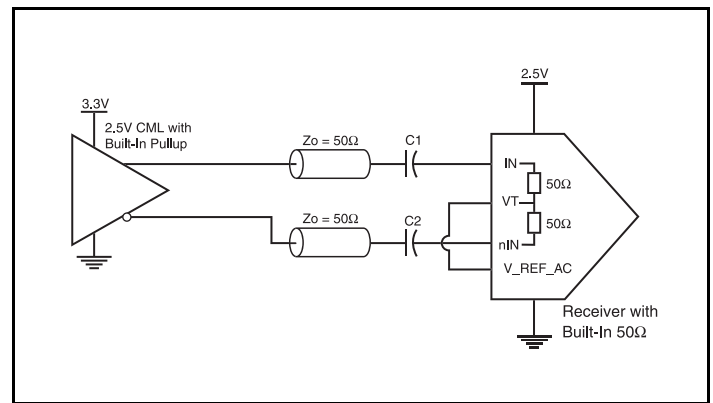
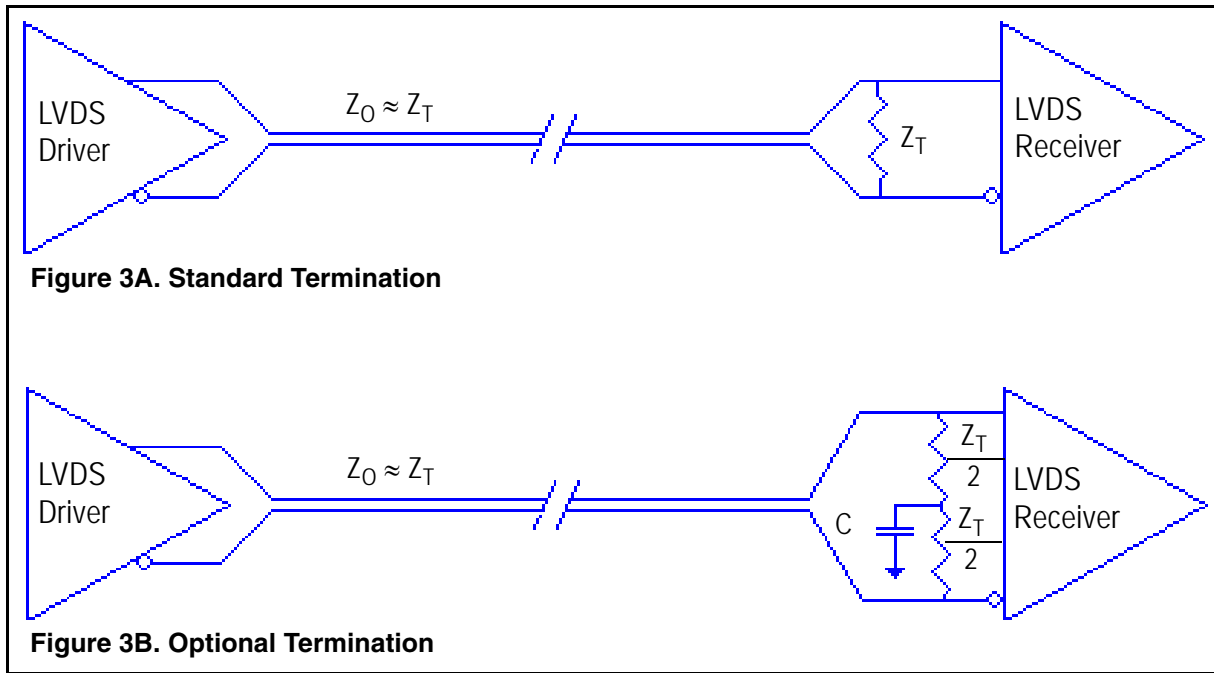


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



Recommendations for Unused Input and Output Pins

Inputs:

LVC MOS Select Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

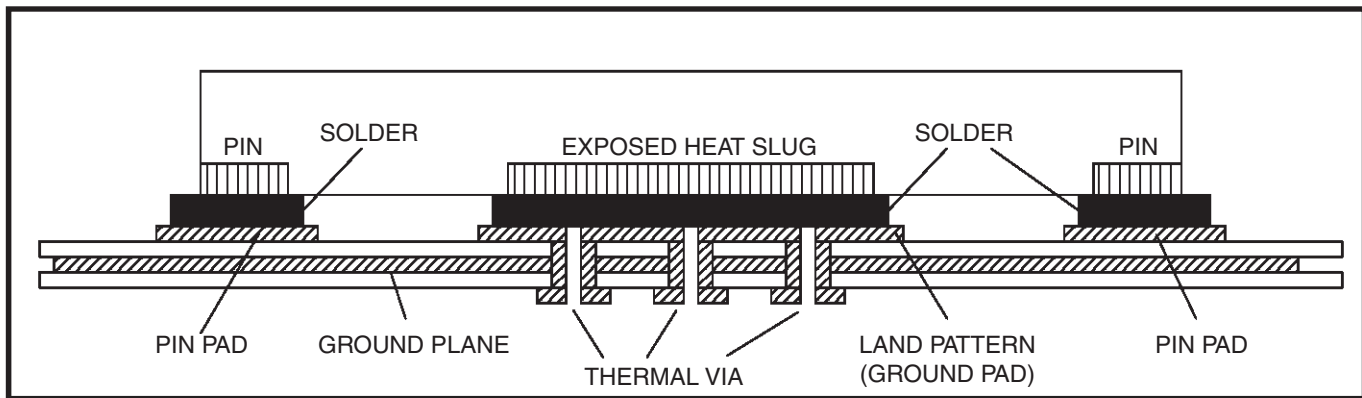


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89200. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89200 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 2.5V + 5\% = 2.625V$, which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD_MAX} = 281\text{mA}$$

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 2.625V * 311\text{mA} = \mathbf{816.375\text{mW}}$
- Power Dissipation for internal termination R_T
Power (R_T)_{MAX} = $(V_{IN_MAX})^2 / R_{T_MIN} = (1.2V)^2 / 80\Omega = \mathbf{18\text{mW}}$

$$\text{Total Power}_{MAX} = (2.625V, \text{ with all outputs switching}) = 816.375\text{mW} + 18\text{mW} = \mathbf{816.393\text{mW}}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_{total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.816\text{W} * 42.7^\circ\text{C/W} = 120^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.7°C/W | 37.3°C/W | 33.5°C/W |

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

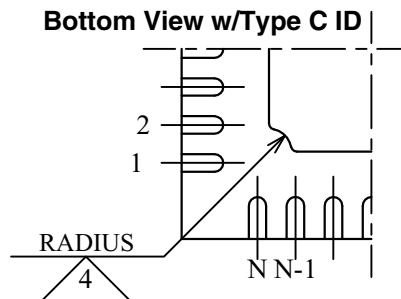
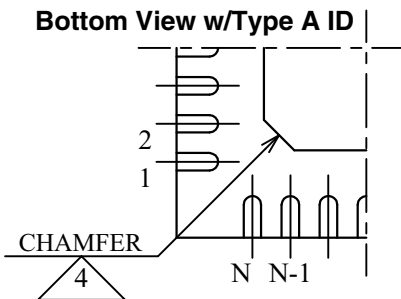
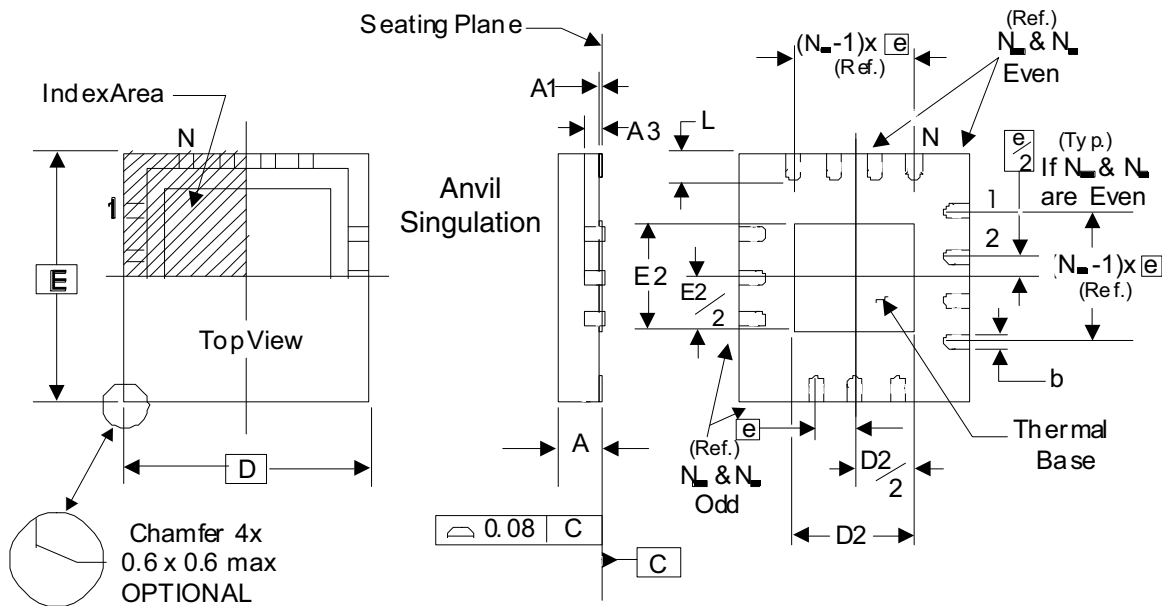
| θ_{JA} vs. Air Flow | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 42.7°C/W | 37.3°C/W | 33.5°C/W |

Transistor Count

The transistor count for 8S89200: 689

32 Lead VFQFN Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

| JEDEC Variation: VHHD-2/-4 | | | |
|---------------------------------|------------|---------|---------|
| All Dimensions in Millimeters | | | |
| Symbol | Minimum | Nominal | Maximum |
| N | 32 | | |
| A | 0.80 | | 1.00 |
| A1 | 0 | | 0.05 |
| A3 | 0.25 Ref. | | |
| b | 0.18 | 0.25 | 0.30 |
| N _D & N _E | | | 8 |
| D & E | 5.00 Basic | | |
| D2 & E2 | 3.0 | | 3.3 |
| e | 0.50 Basic | | |
| L | 0.30 | 0.40 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 8.

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|-------------|--------------------------|--|---------------|
| 8S89200BKILF | ICS89200BIL | 32 Lead VFQFN, Lead-Free | Tray | -40°C to 85°C |
| 8S89200BKILFT | ICS89200BIL | 32 Lead VFQFN, Lead-Free | Tape & Reel | -40°C to 85°C |
| 8S89200BKILF/W | ICS89200BIL | 32 Lead VFQFN, Lead-Free | Tape & Reel Pin 1 Orientation: EIA-481-D | -40°C to 85°C |

Table 10. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|---|
| LFT | Quadrant 1 (EIA-481-C) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |
| LF/W | Quadrant 2 (EIA-481-D) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-----------|----------|---|------------|
| B | T9 T10 | 18 18 | Ordering information Table - added additional row. Added Pin 1 Orientation in Tape & Reel Packaging Table. Updated header/footer throughout the data sheet. | 06/08/2015 |
| B | T9 | 18 | Ordering Information - removed LF note below table. Updated header and footer. | 2/8/16 |



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