

# 30 A VRPower® Integrated Power Stage

## **DESCRIPTION**

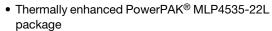
The SiC532 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 4.5 mm x 3.5 mm MLP package, SiC532 enables voltage regulator designs to deliver up to 30 A continuous current per phase.

The internal power MOSFETs utilize Vishay's state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC532 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD\_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

## **FEATURES**





- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers up to 30 A continuous current, 35 A at 10 ms peak current
- High efficiency performance
- High frequency operation up to 2 MHz
- Power ON reset
- 5 V PWM logic with tri-state and hold-off
- Supports PS4 mode light load requirement for IMVP8 with low shutdown supply current (5 V, 5 μA)
- Under voltage lockout for V<sub>CIN</sub>
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

#### **APPLICATIONS**

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8 VRPower delivery
  - -V<sub>CORE</sub>, V<sub>GRAPHICS</sub>, V<sub>SYSTEM</sub> AGENT Skylake, Kabylake platforms -V<sub>CCGI</sub> for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

## TYPICAL APPLICATION DIAGRAM

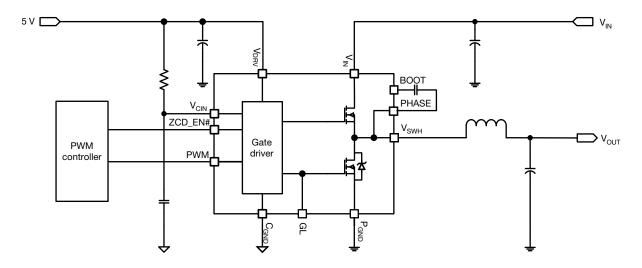


Fig. 1 - SiC532 Typical Application Diagram

## **PINOUT CONFIGURATION**

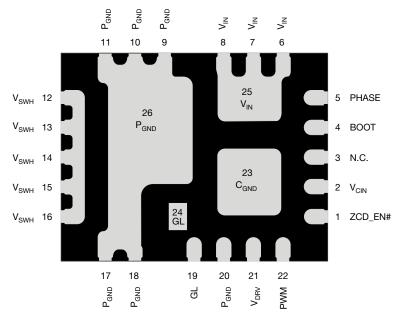


Fig. 2 - SiC532 Pin Configuration

PIN DESCRIPTION					
PIN NUMBER	NAME	FUNCTION			
1	ZCD_EN#	The ZCD_EN# pin enables or disables Diode Emulation. When ZCD_EN# is LOW, diode emulation is allowed. When ZCD_EN# is HIGH, continuous conduction mode is forced. ZCD_EN# can also be put in a high impedance mode by floating the pin. If both ZCD_EN# and PWM are floating, the device shuts down and consumes typically 3 μA (9 μA max.) current.			
2	$V_{CIN}$	Supply voltage for internal logic circuitry			
23	$C_{GND}$	Analog ground for the driver IC			
3	N.C.	No connection			
4	BOOT	High-side driver bootstrap voltage			
5	PHASE	Return path of high-side gate driver			
6 to 8, 25	V <sub>IN</sub>	Power stage input voltage. Drain of high-side MOSFET			
9 to 11, 17, 18, 20, 26	$P_{GND}$	Power ground			
12 to 16	$V_{SWH}$	Switch node of the power stage			
19, 24	GL	Low-side gate signal			
21	$V_{DRV}$	Supply voltage for internal gate driver			
22	PWM	PWM control input			

ORDERING INFORMATION						
PART NUMBER	PACKAGE MARKING CODE					
SiC532CD-T1-GE3	PowerPAK® MLP4535-22L SiC532 5 V PWM optimize					
SiC532DB	Reference board					



## PART MARKING INFORMATION

P/N
LL \( \triangle \)
FYWW

= pin 1 indicator

P/N = part number code

**=** Siliconix logo

 $\triangle$  = ESD symbol

F = assembly factory code

Y = year code

WW = week code

LL = lot code

ABSOLUTE MAXIMUM RATING				
ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT	
Input Voltage	V <sub>IN</sub>	-0.3 to +28		
Control Logic Supply Voltage	V <sub>CIN</sub>	-0.3 to +7		
Drive Supply Voltage	V <sub>DRV</sub>	-0.3 to +7		
Switch Node (DC voltage)	V	-0.3 to +28		
Switch Node (AC voltage) (1)	V <sub>SWH</sub>	-8 to +35	1	
BOOT Voltage (DC voltage)	\ <u>'</u>	33	V	
BOOT Voltage (AC voltage) (2)	V <sub>BOOT</sub>	40		
BOOT to PHASE (DC voltage)	V	-0.3 to +7		
BOOT to PHASE (AC voltage) (3)	VBOOT- PHASE	-0.3 to +8		
All Logic Inputs and Outputs (PWM and ZCD_EN#)		-0.3 to V <sub>CIN</sub> + 0.3		
Max. Operating Junction Temperature	T <sub>J</sub>	150		
Ambient Temperature	T <sub>A</sub>	-40 to +125		
Storage Temperature	T <sub>stg</sub>	-65 to +150		
Flacture static Dischause Dustaction	Human body model, JESD22-A114	2000		
Electrostatic Discharge Protection	Charged device model, JESD22-C101	1000	V	

#### Note

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings
  only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the
  specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- <sup>(1)</sup> The specification values indicated "AC" is  $V_{SWH}$  to  $P_{GND}$ , -8 V (< 20 ns, 10  $\mu$ J), min. and 35 V (< 50 ns), max.
- $^{(2)}$  The specification value indicates "AC voltage" is  $V_{BOOT}$  to  $P_{GND},\,40$  V (< 50 ns) max.
- $^{(3)}$  The specification value indicates "AC voltage" is  $V_{BOOT}$  to  $V_{PHASE}$ , 8 V (< 50 ns) max.

RECOMMENDED OPERATING RANGE							
ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT			
Input Voltage (V <sub>IN</sub> )	4.5	-	24				
Drive Supply Voltage (V <sub>DRV</sub> )	4.5	5	5.5	V			
Control Logic Supply Voltage (V <sub>CIN</sub> )	4.5	5	5.5	]			
BOOT to PHASE (V <sub>BOOT-PHASE</sub> , DC voltage)	4	4.5	5.5				
Thermal Resistance from Junction to PCB	-	5	-	°C/W			
Thermal Resistance from Junction to Case	-	2.5	-	C/VV			

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PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT		
PANAMETEN	STIVIBOL	TEST CONDITION	MIN.	TYP.	MAX.	Oitii		
POWER SUPPLY								
		$V_{PWM} = FLOAT$ - 80			-			
Control Logic Supply Current	I <sub>VCIN</sub>	$V_{PWM} = FLOAT, V_{ZCD\_EN\#} = 0 V$	-	120	-	μΑ		
		$f_S = 300 \text{ kHz}, D = 0.1$	-	300	-			
Drive Supply Current	h many	$f_S = 300 \text{ kHz}, D = 0.1$	-	10	15	mA		
Биче Зарріу Запені	I <sub>VDRV</sub>	$f_S = 1 \text{ MHz}, D = 0.1$	-	20	-			
PS4 Mode Supply Current	I <sub>VCIN</sub> + I <sub>VDRV</sub>	$V_{PWM} = V_{ZCD\_EN\#} = FLOAT,$ $T_A = -10 \degree C \text{ to } +100 \degree C$	-	3	9	μΑ		
BOOTSTRAP SUPPLY								
Bootstrap Diode Forward Voltage	V <sub>F</sub>	$I_F = 2 \text{ mA}$	-	-	0.65	V		
PWM CONTROL INPUT								
Rising Threshold	V <sub>TH_PWM_R</sub>		3.6	3.9	4.2			
Falling Threshold	V <sub>TH_PWM_F</sub>		0.72	1	1.3			
Tri-state Voltage	V <sub>TRI</sub>	$V_{PWM} = FLOAT$	-	2.5	-	V		
Tri-state Rising Threshold	V <sub>TRI_TH_R</sub>		1.1	1.35	1.6	]		
Tri-state Falling Threshold	V <sub>TRI_TH_F</sub>		3.4	3.7	4			
Tri-state Rising Threshold Hysteresis	V <sub>HYS_TRI_R</sub>		-	325	1	mV		
Tri-state Falling Threshold Hysteresis	V <sub>HYS_TRI_F</sub>		-	250	-	1110		
PWM Input Current	laun.	$V_{PWM} = 5 V$	-	-	350			
FWW Input Guirent	I <sub>PWM</sub>	$V_{PWM} = 0 V$	-	-	-350	μA		
ZCD_EN# CONTROL INPUT								
Rising Threshold	V <sub>TH_ZCD_EN#_R</sub>		3.3	3.6	3.9			
Falling Threshold	V <sub>TH_ZCD_EN#_F</sub>		1.1	1.4	1.7	V		
Tri-state Voltage	V <sub>TRI_ZCD_EN#</sub>	$V_{ZCD\_EN\#} = FLOAT$	-	2.5	-			
Tri-state Rising Threshold	V <sub>TRI_ZCD_EN#_R</sub>		1.5	1.8	2.1			
Tri-state Falling Threshold	V <sub>TRI_ZCD_EN#_F</sub>		2.9	3.15	3.4			
Tri-state Rising Threshold Hysteresis	V <sub>HYS_TRI_ZCD#_R</sub>		-	375	-	mV		
Tri-state Falling Threshold Hysteresis	V <sub>HYS_TRI_ZCD#_F</sub>		-	450	-	1110		
ZCD_EN# Input Current	I <sub>ZCD_EN#</sub>	$V_{ZCD\_EN\#} = 5 \text{ V}$	-	-	100	μΑ		
	'ZOD_EN#	$V_{ZCD\_EN\#} = 0 V$	-	-	-100	μ, ι		
PS4 Exit Latency	t <sub>PS4EXIT</sub>		-	-	5	μs		
TIMING SPECIFICATIONS								
Tri-State to GH/GL Rising Propagation Delay	t <sub>PD_TRI_R</sub>		-	20	-			
Tri-state Hold-Off Time	t <sub>TSHO</sub>		-	150	-			
GH - Turn Off Propagation Delay	t <sub>PD_OFF_GH</sub>		-	20	-			
GH - Turn On Propagation Delay (Dead time rising)	t <sub>PD_ON_GH</sub>	N_GH No load, see fig. 4	-	20	-	ns		
GL - Turn Off Propagation Delay	t <sub>PD_OFF_GL</sub>		-	20	-			
GL - Turn On Propagation Delay (Dead time falling)	t <sub>PD_ON_GL</sub>		-	20	-			
PWM Minimum On-Time T <sub>PWM_ON_1</sub>		MIN		-	-	1		
PROTECTION								
		V <sub>CIN</sub> rising, on threshold	-	3.4	3.9			
Under Voltage Lockout	V <sub>UVLO</sub>	V <sub>CIN</sub> falling, off threshold	2.4	2.9	-	V		
Under Voltage Lockout Hysteresis	V <sub>UVLO_HYST</sub>		_	500	_	mV		

## Notes

S15-2728-Rev. A, 23-Nov-15

<sup>(1)</sup> Typical limits are established by characterization and are not production tested.

<sup>(2)</sup> Guaranteed by design.



#### **DETAILED OPERATIONAL DESCRIPTION**

#### **PWM Input with Tri-state Function**

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above V<sub>PWM TH R</sub> the low-side is turned OFF and the high-side is turned  $\bar{ON}$ . When PWM input is driven below  $V_{PWM\ TH\ F}$  the high-side is turned OFF and the low-side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC532 to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, fig. 4). If the PWM input stays in this region for the tri-state hold-off period, t<sub>TSHO</sub>, both high-side and low-side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC532 incorporates PWM voltage thresholds that are compatible with 5 V logic.

#### Diode Emulation Mode and PS4 Mode (ZCD\_EN#)

The ZCD\_EN# pin enables or disables diode emulation mode. When ZCD\_EN# is driven below  $V_{TH\_ZCD\_EN#\_F}$ , diode emulation is allowed. When ZCD\_EN# is driven above  $V_{TH\_ZCD\_EN#\_R}$ , continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC532 will detect the zero current crossing of the output inductor and turn off the low-side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC532 will respond to the ZCD\_EN# input immediately after it changes state.

The ZCD\_EN# pin can be floated resulting in a high impedance state. High impedance on the input of ZCD\_EN# combined with a tri-stated PWM output will shut down the SiC532, reducing current consumption to typically 5  $\mu$ A. This is an important feature in achieving the low standby current requirements required in the PS4 state in ultrabooks and notebooks.

## Voltage Input (V<sub>IN</sub>)

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

#### Switch Node (V<sub>SWH</sub> and PHASE)

The switch node,  $V_{SWH}$ , is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node,  $V_{SWH}$ . This pin is to be used exclusively as the return pin for the BOOT capacitor.

#### Ground Connections (C<sub>GND</sub> and P<sub>GND</sub>)

 $P_{GND}$  (power ground) should be externally connected to  $C_{GND}$  (control signal ground). The layout of the printed circuit board should be such that the inductance separating  $C_{GND}$  and  $P_{GND}$  is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

## Control and Drive Supply Voltage Input (VDRV, VCIN)

 $V_{CIN}$  is the bias supply for the gate drive control IC.  $V_{DRV}$  is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

## **Bootstrap Circuit (BOOT)**

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

## **Shoot-Through Protection and Adaptive Dead Time**

The SiC532 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The high-side and low-side gate voltages are monitored to prevent the MOSFET turning ON from tuning ON until the other MOSFET's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOSFET is completely OFF, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

#### **Under Voltage Lockout (UVLO)**

During the start up cycle, the UVLO disables the gate drive, holding high-side and low-side MOSFET gates low, until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC532 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device.

## **FUNCTIONAL BLOCK DIAGRAM**

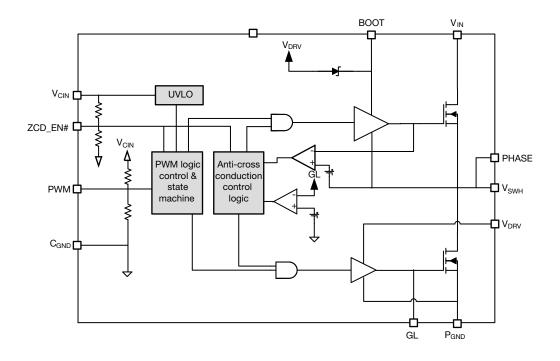


Fig. 3 - SiC532 Functional Block Diagram

DEVICE TRUTH TABLE						
ZCD_EN#	PWM	GH	GL			
Hi-Z (PS4 mode)	X	L	L			
L	L	L	H, I <sub>L</sub> > 0 A L, I <sub>L</sub> < 0 A			
L	Н	Н	L			
L	Hi-Z	L	L			
Н	L	L	Н			
Н	Н	Н	L			
Н	Hi-Z	L	L			

## **PWM TIMING DIAGRAM**

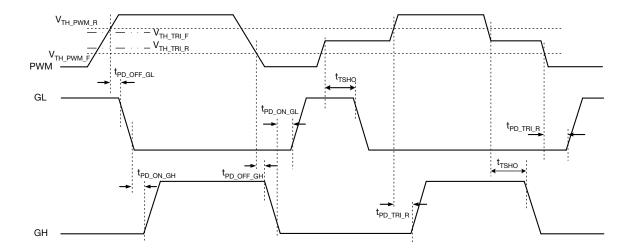


Fig. 4 - Definition of PWM Logic and Tri-State

## ZCD\_EN# - PS4 EXIT TIMING

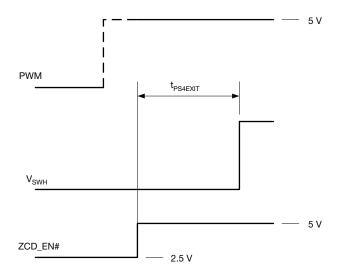


Fig. 5 - ZCD\_EN# - PS4 Exit Timing



## **ELECTRICAL CHARACTERISTICS**

Test condition:  $V_{IN} = 13 \text{ V}$ ,  $V_{DRV} = V_{CIN} = 5 \text{ V}$ ,  $ZCD\_EN\# = 5 \text{ V}$ ,  $V_{OUT} = 1 \text{ V}$ ,  $L_{OUT} = 250 \text{ nH}$ , (DCR = 0.32 m $\Omega$ ),  $T_A = 25 ^{\circ}$ C (All power loss and normalized power loss curves show SiC532 losses only unless otherwise stated)

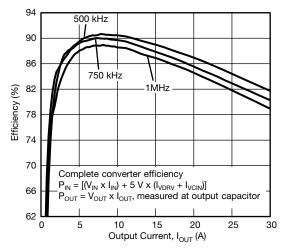


Fig. 6 - Efficiency vs. Output Current (V<sub>IN</sub> = 12.6 V)

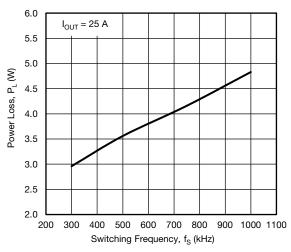


Fig. 7 - Power Loss vs. Switching Frequency (V<sub>IN</sub> = 12.6 V)

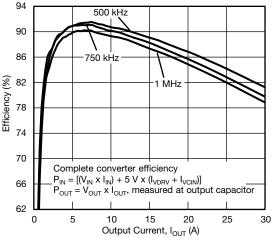


Fig. 8 - Efficiency vs. Output Current (9 V)

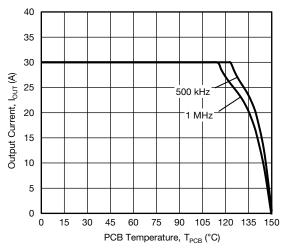


Fig. 9 - Safe Operating Area (V<sub>IN</sub> = 12.6 V)

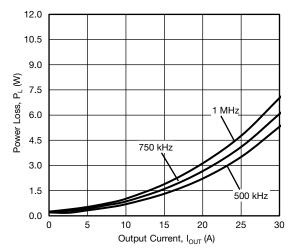


Fig. 10 - Power Loss vs. Output Current (V<sub>IN</sub> = 12.6 V)

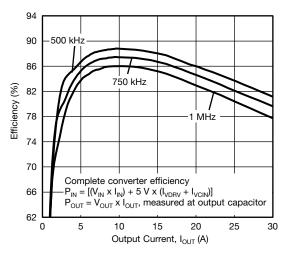


Fig. 11 - Efficiency vs. Output Current (V<sub>IN</sub> = 19 V)



## **ELECTRICAL CHARACTERISTICS**

Test condition:  $V_{IN} = 13 \text{ V}$ ,  $V_{DRV} = V_{CIN} = 5 \text{ V}$ ,  $ZCD\_EN\# = 5 \text{ V}$ ,  $V_{OUT} = 1 \text{ V}$ ,  $L_{OUT} = 250 \text{ nH}$ , (DCR = 0.32 m $\Omega$ ),  $T_A = 25 ^{\circ}$ C (All power loss and normalized power loss curves show SiC532 losses only unless otherwise stated)

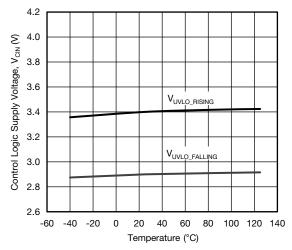


Fig. 12 - UVLO Threshold vs. Temperature

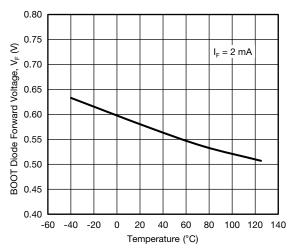


Fig. 13 - BOOT Diode Forward Voltage vs. Temperature

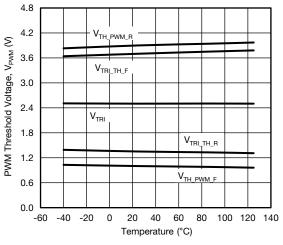


Fig. 14 - PWM Threshold vs. Temperature

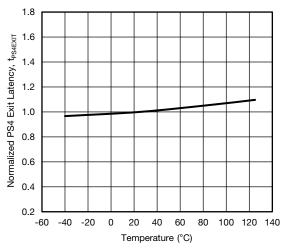


Fig. 15 - PS4 Exit Latency vs. Temperature

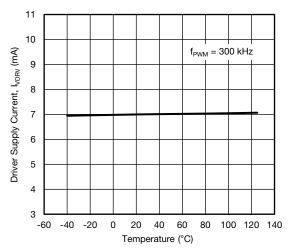


Fig. 16 - Driver Supply Current vs. Temperature

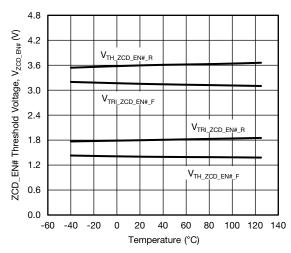
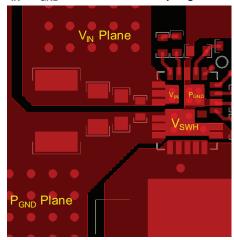


Fig. 17 - ZCD\_EN# Threshold vs. Temperature



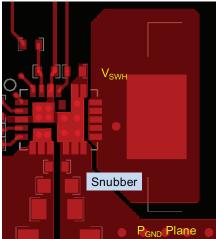
## **PCB LAYOUT RECOMMENDATIONS**

Step 1: VIN / PGND Planes and Decoupling



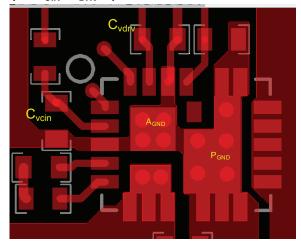
- 1. Layout V<sub>IN</sub> and P<sub>GND</sub> planes as shown above.
- 2. Ceramic capacitors should be placed directly between  $V_{\text{IN}}$  and  $P_{\text{GND}}$ , and close to the device for best decoupling effect.
- Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, 0402.
- 4. Smaller capacitance values, placed closer to the device's  $V_{\text{IN}}$  pin(s), results in better high frequency noise absorbing.

Step 2: V<sub>SWH</sub> Plane



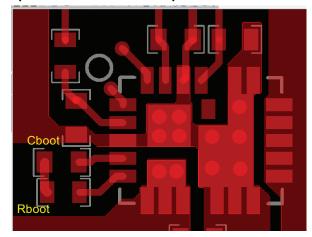
- Connect output inductor to IC with large plane to lower resistance.
- V<sub>SWH</sub> plane also serves as a heat-sink for low-side MOSFET. Make the plane wide and short to achieve the best thermal path.
- If a snubber network is required, place the components as shown above, the network can be placed at bottom.

Step 3: V<sub>CIN</sub> / V<sub>DRV</sub> Input Filter



- 1. The  $V_{\text{CIN}}$  /  $V_{\text{DRV}}$  input filter ceramic cap should be placed as close as possible to the IC. It is recommended to connect two capacitors separately.
- V<sub>CIN</sub> capacitor should be placed between pin 2 (V<sub>CIN</sub>) and pin 3 (A<sub>GND</sub> of driver IC) to achieve best noise filtering.
- V<sub>DRV</sub> capacitor should be placed between pin 20 (P<sub>GND</sub> of driver IC) and pin 21 (V<sub>DRV</sub>) to provide maximum instantaneous driver current for low side MOSFET during switching cycle.
- For connecting V<sub>CIN</sub> to A<sub>GND</sub>, it is recommended to use a large plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement

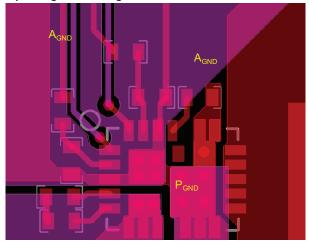


- 1. The components need to be placed as close as possible to IC, directly between PHASE (pin 5) and BOOT (pin 4).
- To reduce parasitic inductance, chip size 0402 can be used.

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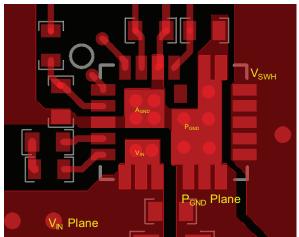
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Step 5: Signal Routing



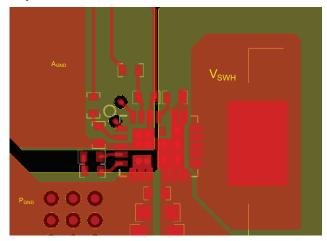
- 1. Route the PWM and ZCD\_EN# signal traces out of the top left corner next to pin 1.
- The PWM signal is an important signal, both signal and return traces should not cross any power nodes on any laver.
- 3. It is best to "shield" these traces from power switching nodes, e.g.  $V_{\rm SWH}$ , with a GND island to improve signal integrity.
- GL (pin 19) has been connected with GL pad (pin 24) internally.

Step 6: Adding Thermal Relief Vias



- 1. Thermal relief vias can be added on the  $V_{\text{IN}}$  and  $A_{\text{GND}}$  pads to utilize inner layers for high-current and thermal dissipation.
- 2. To achieve better thermal performance, additional vias can be placed on  $V_{\text{IN}}$  plane and  $P_{\text{GND}}$  plane.
- 3. V<sub>SWH</sub> pad is a noise source, it is not recommended to place vias on this pad.
- 4. 8 mil vias for pads and 10 mils vias for planes are the optimal via sizes. Vias on pad may drain solder during assembly and cause assembly issues. Consult with the assembly house for guidelines.

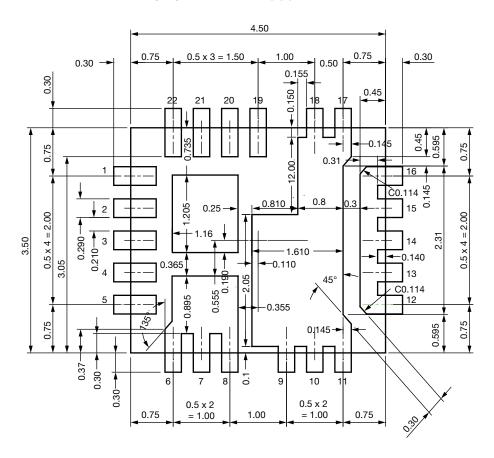
**Step 7: Ground Connection** 

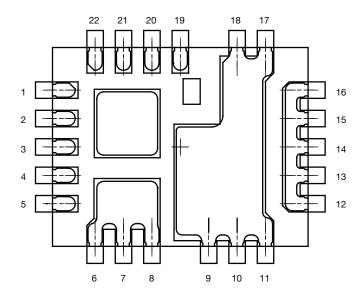


- 1. It is recommended to make a single connection between  $A_{GND}$  and  $P_{GND}$  which can be made on the top layer.
- 2. It is recommended to make the entire first inner layer (below top layer) the ground plane and separate them into  $A_{GND}$  and  $P_{GND}$  planes.
- 3. These ground planes provide shielding between noise sources on top layer and signal traces on bottom layer.



## RECOMMENDED LAND PATTERN PowerPAK® MLP4535-22L

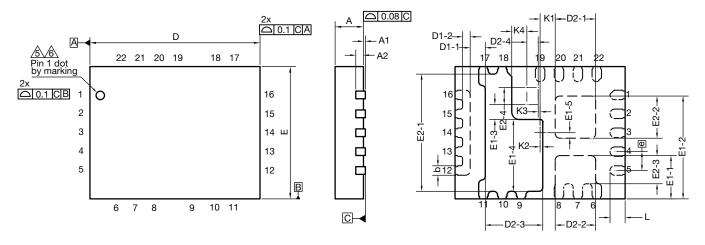




All dimensions in millimeters



## **PACKAGE OUTLINE DRAWING MLP4535-22L**

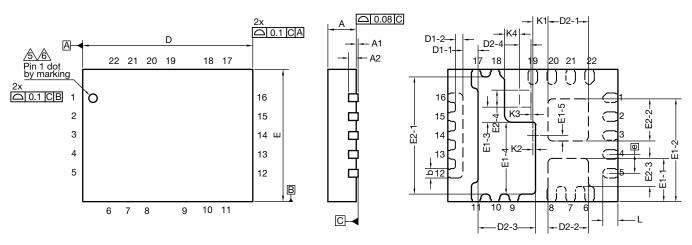


DIM	MILLIMETERS		INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A (8)	0.70	0.75	0.80	0.027	0.0029	0.031	
A1	0.00	-	0.05	0.000	-	0.002	
A2		0.20 ref.			0.008 ref.		
b <sup>(4)</sup>	0.20	0.25	0.30	0.0078	0.0098	0.0110	
D		4.50 BSC		0.177 BSC			
е		0.50 BSC			0.019 BSC		
E		3.50 BSC			0.137 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017	
N (3)		22			22		
Nd <sup>(3)</sup>		6			6		
Ne <sup>(3)</sup>		5			5		
D1-1	0.35	0.40	0.45	0.013	0.015	0.017	
D1-2	0.15	0.20	0.25	0.005	0.007	0.009	
D2-1	1.02	1.07	1.12	0.040	0.042	0.044	
D2-2	1.02	1.07	1.12	0.040	0.042	0.044	
D2-3	1.47	1.52	1.57	0.057	0.059	0.061	
D2-4	0.25	0.30	0.35	0.009	0.011	0.013	
E1-1	1.095	1.145	1.195	0.043	0.045	0.047	
E1-2	2.67	2.72	2.77	0.105	0.107	0.109	
E1-3	0.35	0.40	0.45	0.013	0.015	0.017	
E1-4	1.85	1.90	1.95	0.072	0.074	0.076	
E1-5	0.095	0.145	0.195	0.0037	0.0057	0.0076	
E2-1	3.05	3.10	3.15	0.120	0.122	0.124	
E2-2	1.065	1.115	1.165	0.0419	0.0438	0.0458	
E2-3	0.695	0.745	0.795	0.027	0.029	0.031	
E2-4	0.40	0.45	0.50	0.015	0.017	0.019	
K1		0.40 BSC			0.015 BSC		
K2	0.07 BSC			0.002 BSC			
K3		0.05 BSC			0.001 BSC		
K4		0.40 BSC			0.015 BSC		

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?74770">www.vishay.com/ppg?74770</a>

Vishay Siliconix

# MLP 4.5 x 3.5-22L BWL Case Outline



DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A <sup>(8)</sup>	0.70	0.75	0.80	0.027	0.0029	0.031	
A1	0.00	-	0.05	0.000	-	0.002	
A2		0.20 ref.			0.008 ref.		
b <sup>(4)</sup>	0.20	0.25	0.30	0.0078	0.0098	0.0110	
D		4.50 BSC			0.177 BSC		
е		0.50 BSC			0.019 BSC		
Е		3.50 BSC			0.137 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017	
N (3)		22			22		
Nd <sup>(3)</sup>		6			6		
Ne <sup>(3)</sup>		5			5		
D1-1	0.35	0.40	0.45	0.013	0.015	0.017	
D1-2	0.15	0.20	0.25	0.005	0.007	0.009	
D2-1	1.02	1.07	1.12	0.040	0.042	0.044	
D2-2	1.02	1.07	1.12	0.040	0.042	0.044	
D2-3	1.47	1.52	1.57	0.057	0.059	0.061	
D2-4	0.25	0.30	0.35	0.009	0.011	0.013	
E1-1	1.095	1.145	1.195	0.043	0.045	0.047	
E1-2	2.67	2.72	2.77	0.105	0.107	0.109	
E1-3	0.35	0.40	0.45	0.013	0.015	0.017	
E1-4	1.85	1.90	1.95	0.072	0.074	0.076	
E1-5	0.095	0.145	0.195	0.0037	0.0057	0.0076	
E2-1	3.05	3.10	3.15	0.120	0.122	0.124	
E2-2	1.065	1.115	1.165	0.0419	0.0438	0.0458	
E2-3	0.695	0.745	0.795	0.027	0.029	0.031	
E2-4	0.40	0.45	0.50	0.015	0.017	0.019	
K1	0.40 BSC		0.015 BSC				
K2		0.07 BSC		0.002 BSC			
K3		0.05 BSC			0.001 BSC		
K4		0.40 BSC			0.015 BSC		

Revision: 20-Oct-14 1 Document Number: 67234

# **Package Information**



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#### **Notes**

- 1. Use millimeters as the primary measurement
- 2. Dimensioning and tolerances conform to ASME Y14.5M. 1994
- 3. N is the number of terminals,

Nd is the number of terminals in X-direction and

Ne is the number of terminals in Y-direction.

- 4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- 5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- 6. Exact shape and size of this feature is optional
- 7. Package warpage max. 0.08 mm
- 8. Applied only for terminals

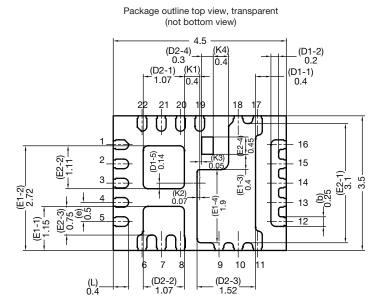
T14-0626-Rev. A, 20-Oct-14

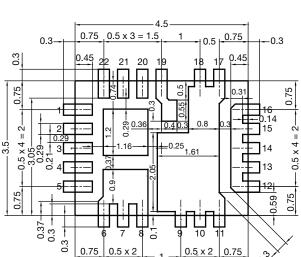
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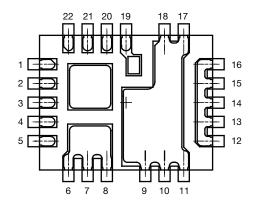
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# Recommended Land Pattern PowerPAK® MLP4535-22L





Land pattern



All dimensions in millimeters



# **Legal Disclaimer Notice**

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Revision: 02-Oct-12 Document Number: 91000



OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
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В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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