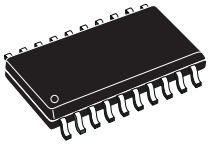
TDA7403

BASIC SIGNAL PROCESSOR

- DEVICE INCLUDES AUDIO PROCESSOR, STEREO DECODER AND NOISEBLANKER
- HIGH PERFORMANCE SIGNAL PROCESSOR WITH BASIC FUNCTIONS
- AM, FM, (MPX) AND CASSETTE INPUTS
- NO EXTERNAL COMPONENTS REQUIRED
- FULLY PROGRAMMABLE VIA I^2C BUS
- LOW DISTORTION AND NOISE



SO20

ORDERING NUMBER: TDA7403D

DESCRIPTION

The TDA7403 is a high performance signal processor specifically designed for car radio applications focused on the low-end market.

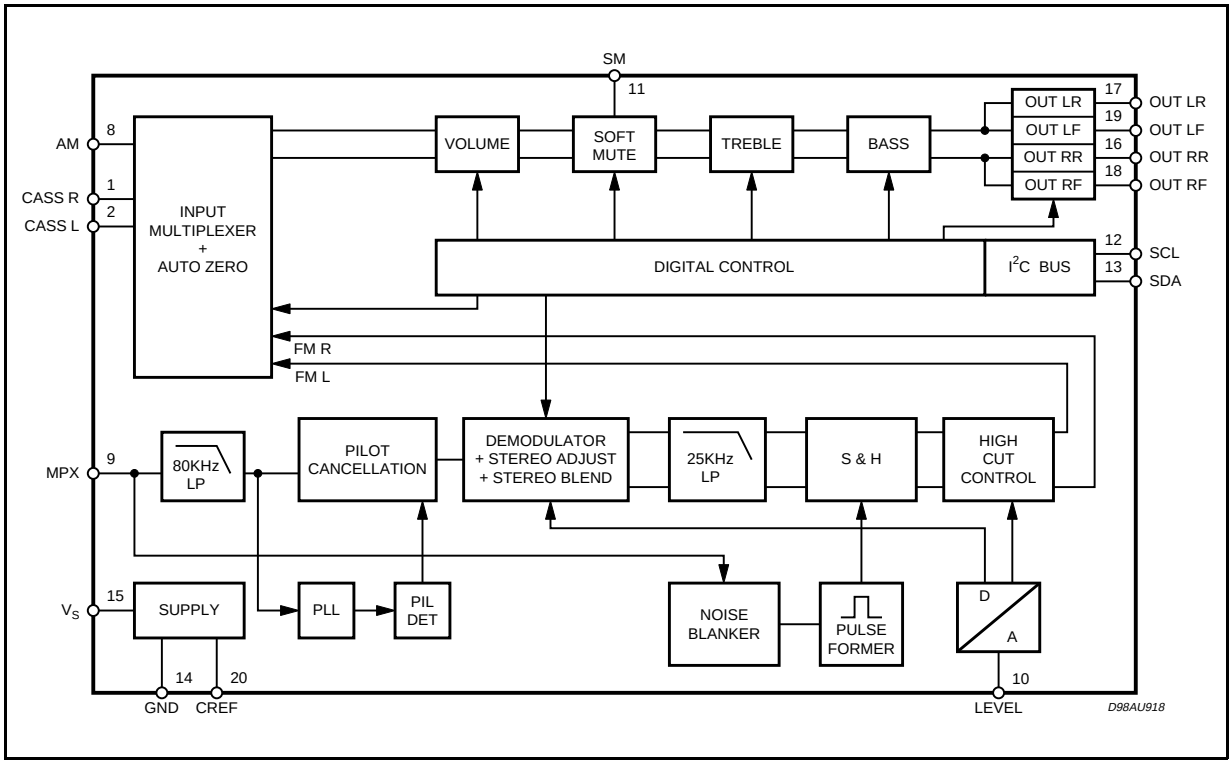
The device includes a complete audioprocessor and a stereo decoder with noiseblanker.

Switched-capacitors design technique allows to obtain all these features without external components or adjustments. Using TDA7403 results is in a very performant low-cost signal processing application

The device is fully programmable by I^2C bus interface allowing to customize key device parameters and especially filter characteristics.

The BICMOS process combined with the optimized signal processing assure low noise and low distortion performances.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature Range	-40 to 80	°C
T_{stg}	Operating Storage Temperature Range	-55 to 150	°C

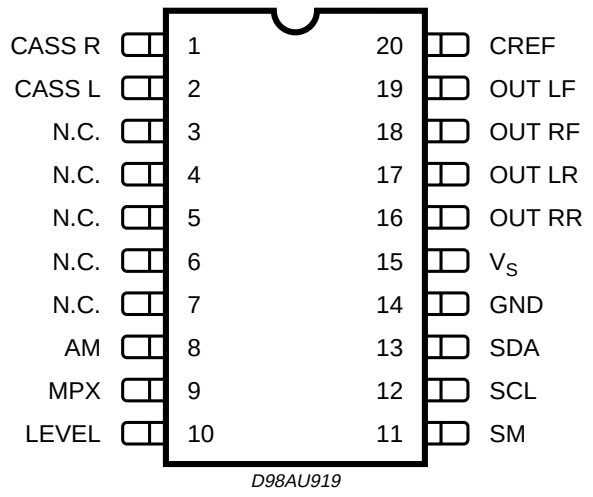
SUPPLY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		7.5	9	10	V
I_S	Supply Current	V_S = 9V	25	30	35	mA
SVRR	Ripple Rejection @ 1KHz	Audioprocessor (all filters flat)		60		dB
		Stereodecoder + Audioprocessor		55		dB

ESD

All pins are protected against ESD according to the MIL883 standard.

PIN CONNECTION



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\text{-}j\ pins}$	Thermal Resistance Junction-pins	Max	85	°C/W

PIN DESCRIPTION

N.	Name	Function	Type
1	CASSR	Cassette Input Right	I
2	CASSL	Cassette Input Left	I
3	n.c.	not connected	
4	n.c.	not connected	
5	n.c.	not connected	
6	n.c.	not connected	
7	n.c.	not connected	
8	AM	AM Input	I
9	MPX	FM Input (MPX)	I
10	LEVEL	Level Input Stereodecoder	I
11	SM	Soft Mute Drive	I
12	SCL	I^2C Clock Line	I/O
13	SDA	I^2C Data Line	I/O
14	GND	Supply Ground	S
15	VS	Supply Voltage	S
16	OUTRR	Right Rear Speaker Output	O
17	OUTLR	Left Rear Speaker Output	O
18	OUTRF	Right Front Spaeaker Output	O
19	OUTLF	Left Front Speaker Output	O
20	CREF	Reference Capacitor Pin	S

(1) See input configuration tree and databyte specification "configuration"

Pin type legenda:

I = Input

O = Output

I/O = Input/Output

S = Supply

AUDIO PROCESSOR PART

Input Multiplexer
- MPX input
- Cassette stereo input
- AM mono

Volume control
- 1dB attenuator
- Max. gain 20dB
- Max. attenuation 79dB

Soft-step gain control

Bass Control
- 2nd order frequency response
- Center frequency programmable in 4(5) steps
- DC gain programmable
- 7 x 2dB steps

Treble Control
- 2nd order frequency response
- Center frequency programmable in 4 steps
- 7 x 2dB steps

Speaker Control
- 4 independent speaker controls (1dB steps control range 50dB)

Mute Functions
- Direct mute driven by pin SM
- Digitally controlled softmute with 4 programmable time constants

ELECTRICAL CHARACTERISTICS (V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SELECTOR						
R_{in}	Input Resistance	all inputs except Phone	70	100	130	KΩ
V_{CL}	Clipping Level		2.2	2.6		V_{RMS}
S_{IN}	Input Separation		80	100		dB
$G_{IN\ MIN}$	Min. Input Gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. Input Gain			14		dB
G_{STEP}	Step Resolution			2		dB
V_{DC}	DC Steps	Adjacent Gain Step		0		mV
		G_{MIN} to G_{MAX}		1		mV
VOLUME CONTROL						
G_{MAX}	Max Gain			20		dB
A_{MAX}	Max Attenuation			79		dB
A_{STEP}	Step Resolution			1		dB
E_A	Attenuation Set Error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -60 to 20dB	-4	0	3	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV
		From 0dB to G_{MIN}		0.5	5	mV
SOFT MUTE						
A_{MUTE}	Mute Attenuation		70	100		dB
T_D	Delay Time	T1		0.48		ms
		T2		0.96		ms
		T3		40.4		ms
		T4		324		ms
V_{THlow}	Low Threshold for SM Pin (1)				1	V
V_{THhigh}	High Threshold for SM Pin		2.5			V
R_{PU}	Internal Pull-up Resistor		70	100	130	KΩ
V_{PU}	Pull-up Voltage			4.7		V

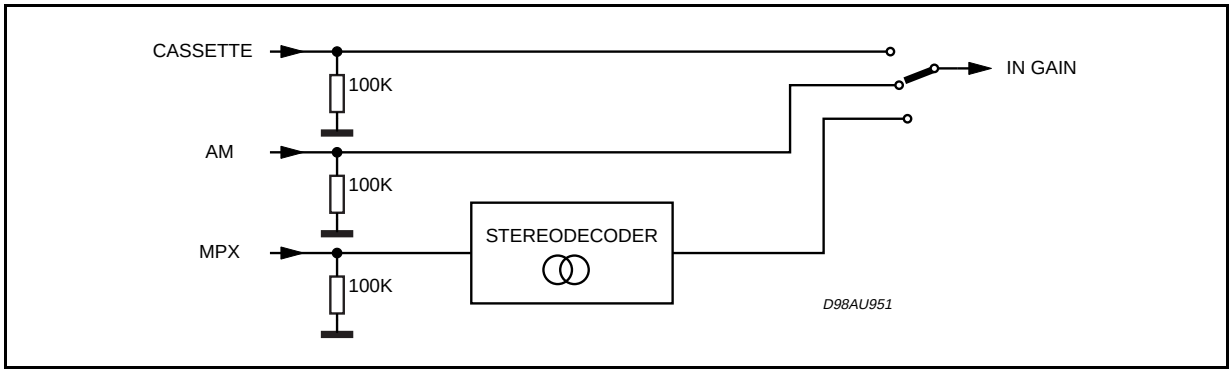
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SOFT STEP						
T_{SW}	Switch Time			10		ms
BASS CONTROL						
C_{RANGE}	Control Range			±14		dB
A_{STEP}	Step Resolution			2		dB
f_C	Center Frequency	f_{C1}		60		Hz
		f_{C2}		70		Hz
		f_{C3}		80		Hz
		f_{C4}		100(2)		Hz
Q_{BASS}	Quality Factor	Q_1		1		
		Q_2		1.25		
		Q_3		1.5		
		Q_4		2		
DC_{GAIN}	Bass-Dc-Gain	DC = off		0		dB
		DC = on		4.4		dB
TREBLE CONTROL						
C_{RANGE}	Control Range			±14		dB
A_{STEP}	Step Resolution			2		dB
f_C	Center Frequency	f_{C1}		10		KHz
		f_{C2}		12.5		KHz
		f_{C3}		15		KHz
		f_{C4}		17.5		KHz
SPEAKER ATTENUATORS						
C_{RANGE}	Control Range			50		dB
A_{STEP}	Step Resolution			1		dB
A_{MUTE}	Output Mute Attenuation			80		dB
E_E	Attenuation Set Error				3	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	10	mV
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	2.2	2.6		V_{RMS}
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				10	nF
R_{OUT}	Output Impedance			30	120	Ω
V_{DC}	DC Voltage Level			3.8		V
GENERAL						
e_{NO}	Output Noise	BW = 20 Hz to 20 KHz output muted		5		µV
		BW = 20 Hz to 20 KHz all gain = 0dB		10		µV
S/N	Signal to Noise Ratio	all gain = 0dB flat; $V_O = 2V_{RMS}$		106		dB
		bass treble at 12dB; V_O = $2.6V_{RMS}$		96		dB
d	Distortion	$V_{IN} = 1V_{RMS}$; all stages 0dB		0.002		%
		$V_{IN} = 1V_{RMS}$; Bass & Treble = 12dB		0.05		%
S_C	Channel separation Left/Right		80	100		dB
E_T	Total Tracking Error	A_V = 0 to -20dB		0	1	dB
		A_V = -20 to -60dB		0	2	dB

1) SM pin is active low (mute condition)
2) See description of Audioprocessor Part - Bass & Treble filter characteristics programming

DESCRIPTION OF THE AUDIOPROCESSOR

Figure 1. Input stages



Input stages

The input circuits are the same as in preceeding ST audioprocessors with exception of the CD inputs (see figure 1).
The typical input impedance is 100kΩ.

AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output.

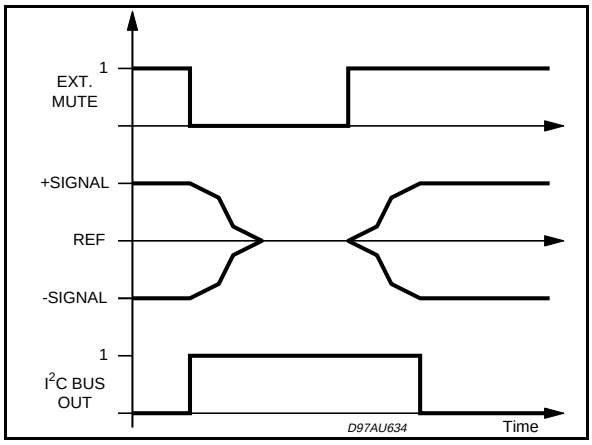
To avoid that effect a special offset cancellation stage called AutoZero is implemented.
To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the µP is executing a refresh cycle of the I^2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7403 could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^2C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see figure 2).

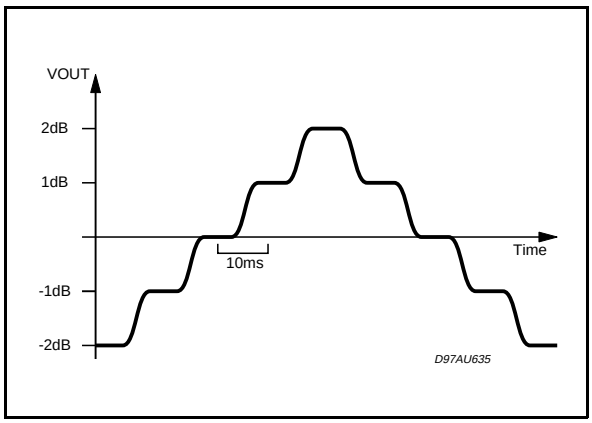
For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 2. Softmute Timing



Note: Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

Figure 3. Soft Step Timing



Note: For steps more than 1dB the softstep mode should be deactivated because it could generate a 1dB error during the blend-time

Softstep Volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Softstep feature both kinds of clicks could be reduced to a minimum and are no more audible (see figure 3).

Bass

There are three parameters programmable in the bass stage (see figs 4, 5, 6, 7):

- Attenuation
- Center Frequency (60, 70, 80 and 100Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

DC Mode

In this mode the DC gain is increased by 4.4dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.

Treble

There are two parameters programmable in the treble stage (see figs 8, 9):

- Attenuation
- Center Frequency (10, 12.5, 15 and 17.5kHz).

Speaker Attenuator

Due to practical aspects the steps in the speaker attenuators are not linear over the full range. At attenuations more than 24dB the steps increase from 1.5dB to 10dB (please see data byte specification).

Figure 4. Bass Control @ fc = 80Hz, Q = 1

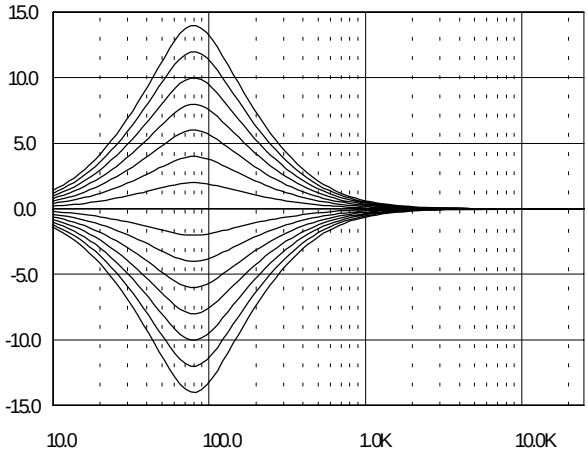


Figure 5. Bass Center @ Gain = 14dB, Q = 1

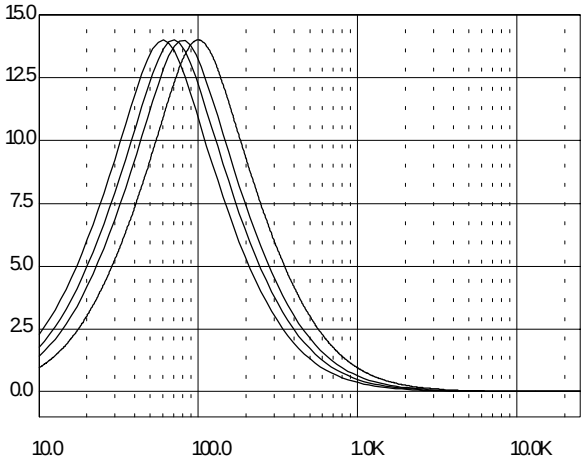


Figure 6. Bass Quality factors @ Gain = 14dB, fc = 80Hz

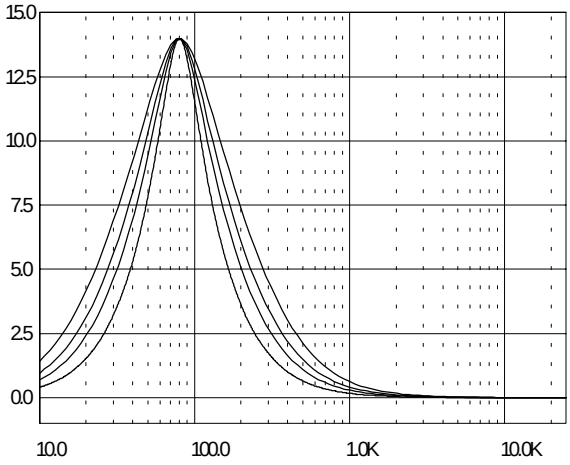
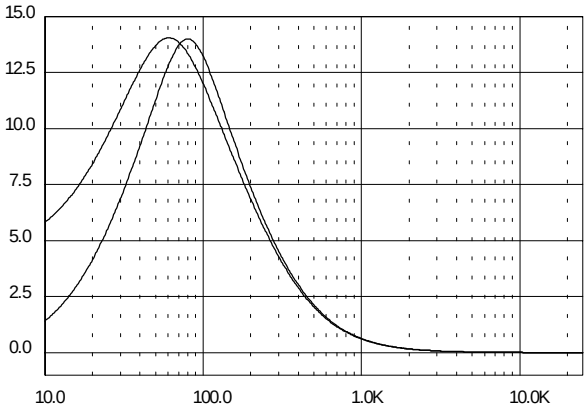


Figure 7. Bass normal and DC Mode @ Gain = 14dB, fc = 80Hz



Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100Hz.

Figure 8. Treble Control @ fc = 17.5KHz

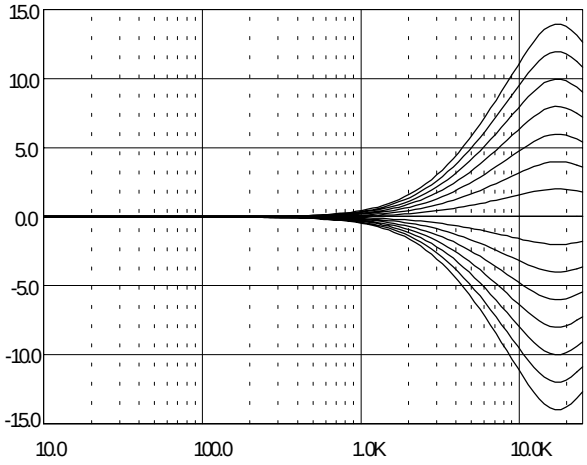
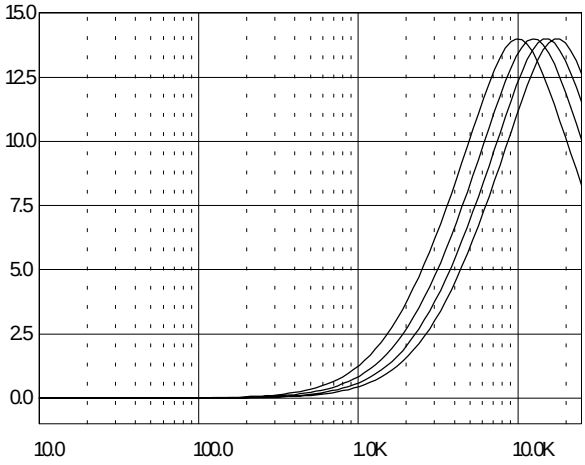


Figure 9. Treble Center Frequencies @ Gain = 14dB



STEREODECODER PART

- No external components necessary
- PLL with adjustment free fully integrated VCO
- Automatic pilot dependent MONO/STEREO switching
- Very high suppression of intermodulation and interference
- Programmable Roll-Off compensation
- Dedicated RDS Softmute
- Highcut and Stereoblend characterisctics programmable in a wide range
- Internal Noiseblanker with threshold controls
- Multipath detector with programmable internal/external influence
- I^2C bus control of all necessary functions

ELECTRICAL CHARACTERISTICS (V_S = 9V; deemphasis time constant = 50µs, V_{MPX} = 500mV, 75KHz deviation, f = 1KHz. G_I = 6dB, T_{amb} = 25°C; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX Input Level	Input Gain = 3.5dB		0.5	1.25	V_{RMS}
R_{in}	Input Resistance			100		KΩ
G_{min}	Minimum Input Gain			3.5		dB
G_{max}	Max Input Gain			11		dB
G_{STEP}	Step Resolution			2.5		dB
SVRR	Supply Voltage Ripple Rejection	V_{ripple} = 100mv, f = 1khz		60		dB
α	Max Channel Separation			50		dB
THD	Total Harmonic Distortion			0.05		%
$\frac{S+N}{N}$	Signal plus Noise to Noise Ratio	S = $2V_{rms}$		86		dB
MONO/STEREO SWITCH						
V_{PTHST1}	Pilot Threshold Voltage	for Stereo, PTH = 1		15		mV
V_{PTHST0}	Pilot Threshold Voltage	for Stereo, PTH = 0		25		mV
V_{PTHMO1}	Pilot Threshold Voltage	for Mono, PTH = 1		12		mV
V_{PTHMO0}	Pilot Threshold Voltage	for Stereo, PTH = 0		19		mV
PLL						
Δf/f	Capture Range		0.5			%
DEEMPHASIS and HIGHCUT						
τ_{HC50}	Deemphasis Time Constant	Bit = 7, Subadr. 10 = 0 V_{LEVEL} >> V_{HCH}		50		µs
τ_{HC75}	Deemphasis Time Constant	Bit = 7, Subadr. 10 = 1 VLEVEL >> V_{HCH}		75		µs
τ_{HC50}	Highcut Time Constant	Bit = 7, Subadr. 10 = 0 VLEVEL >> V_{HCL}		150		µs
τ_{HC75}	Highcut Time Constant	Bit = 7, Subadr. 10 = 1 VLEVEL >> V_{HCL}		225		µs
STEREOBLEND and HIGHCUT-CONTROL						
REF5V	Internal Reference Voltage			5		V
TC_{REF5V}	Temperature Coefficient			3300		ppm
L_{Gmin}	Min. LEVEL Gain			0		dB
L_{Gmax}	Max. LEVEL Gain			10		dB
L_{Gstep}	LEVEL Gain Step Resolution			0.67		dB
$VSBL_{min}$	Min.Voltage for Mono			33		%REF5V
$VSBL_{max}$	Max. Voltage for Mono			58		%REF5V
$VSBL_{step}$	Step Resolution			8.4		%REF5V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STEREOBLEND and HIGHCUT CONTROL						
$VHCH_{min}$	Min.Voltage for NO Highcut			42		%REF5V
$VHCH_{max}$	Max. Voltage for NO Highcut			66		%REF5V
$VHCH_{step}$	Step Resolution			8.4		%REF5V
$VHCL_{min}$	Min. Voltage for FULL High cut			17		%VHCH
$VHCL_{max}$	Max. Voltage for FULL High cut			33		%VHCH
Carrier and harmonic suppression at the output						
$\alpha 19$	Pilot Signal	f = 19KHz		50		dB
$\alpha 38$	Subcarrier	f = 38KHz		75		dB
$\alpha 57$	Subcarrier	f = 57KHz		62		dB
$\alpha 76$	Subcarrier	f = 76KHz		90		dB
Intermodulation (Note1)						
$\alpha 2$	Pilot Signal	f_{mod} = 10KHz; f_{spur} = 1KHz;		65		dB
$\alpha 3$		f_{mod} = 13KHz; f_{spur} = 1KHz;		75		dB
Traffic Radio (Note 2)						
$\alpha 57$	Signal	f = 57KHz		70		dB
SCA - Subsidiary Communications Authorization (Note 3)						
$\alpha 67$	Signal	f = 67KHz		75		dB
ACI - Adjacent Channel Interference (Note 4)						
$\alpha 114$	Signal	f = 114KHz		95		dB
$\alpha 190$	Signal	f = 190KHz		84		dB

Notes to the characteristics:

1. Intermodulation Suppression: measured with: 91% pilot signal; fm = 10kHz or 13kHz.

2. Traffic Radio (V.F.) Suppression: measured with: 91% stereo signal; 9% pilot signal; fm=1kHz; 5% subcarrier (f = 57kHz, fm = 23Hz AM, m = 60%)

3. SCA (Subsidiary Communications Authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1kHz; 10%SCA - subcarrier (fs = 67kHz, unmodulated).

4. ACI (Adjacent Channel Interference) measured with: 90% mono signal; 9% pilot signal; fm =1kHz; 1% spurious signal (fs = 110kHz or 186kHz, unmodulated).

NOISE BLANKER PART

- internal 2nd order 140kHz high pass filter
- programmable trigger threshold
- additional circuits for trigger adjustment (deviation, field-strenght)
- very low offset current during hold time
- four selectable pulse suppression times

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger Threshold [0) 1)]	meas. with V_{PEAK} = 0.9V	NBT = 111		30		mV_{OP}
			NBT = 110		35		mV_{OP}
			NBT = 101		40		mV_{OP}
			NBT = 100		45		mV_{OP}
			NBT = 011		50		mV_{OP}
			NBT = 010		55		mV_{OP}
			NBT = 001		60		mV_{OP}
			NBT = 000		65		mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger Threshold [2)]	meas. with V_{PEAK} = 1.5V	NCT = 00		260		mV_{OP}
			NCT = 01		220		mV_{OP}
			NCT = 10		180		mV_{OP}
			NCT = 11		140		mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV			0.9		V
		V_{MPX} = 50mV; f = 150KHz			1.7		V
		V_{MPX} = 100mV; f = 150KHz			2.5		V
$V_{RECT\ DEV}$	deviation dependent rectifier Voltage [3)]	means. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11		0.9(off)		V_{OP}
			OVD = 10		1.2		V_{OP}
			OVD = 01		2.0		V_{OP}
			OVD = 00		2.8		V_{OP}
$V_{RECT\ FS}$	Fieldstrength Controlled Rectifier Voltage [4)]	means. with V_{MPX} = 0mV V_{LEVEL} << V_{SBL} (fully mono)	FSC = 11		0.9(off)		V
			FSC = 10		1.3		V
			FSC = 01		1.8		V
			FSC = 00		2.3		V

0) All thresholds are measured using a pulse with T_R = 2 µs, T_{HIGH} = 2 µs and T_F = 10 µs.

1) NBT represents the Noiseblanker-Byte bits D2; D0 for the noise blanker trigger threshold

2) NAT represents the Noiseblanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment

3) OVD represents the Noiseblanker-Byte bit pair D7,D6 for the over deviation detector

4) FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control

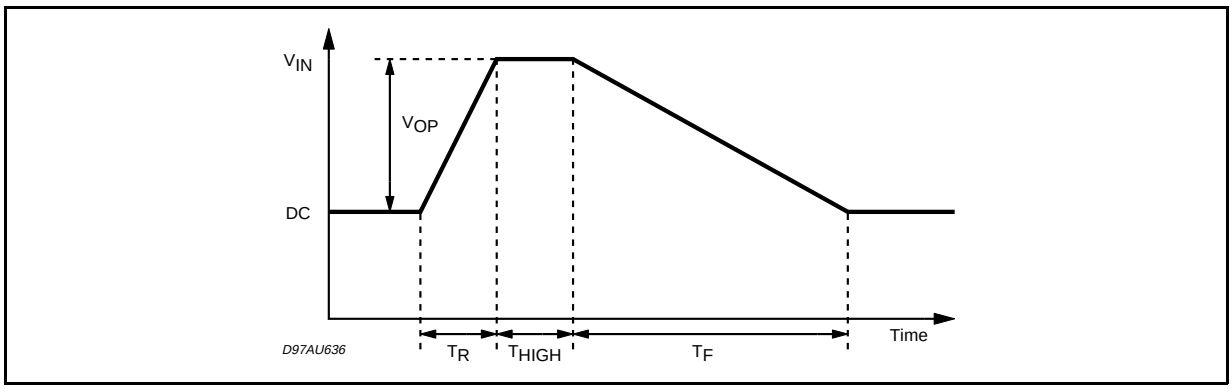


Figure 10. Trigger Threshold vs. V_{PEAK}

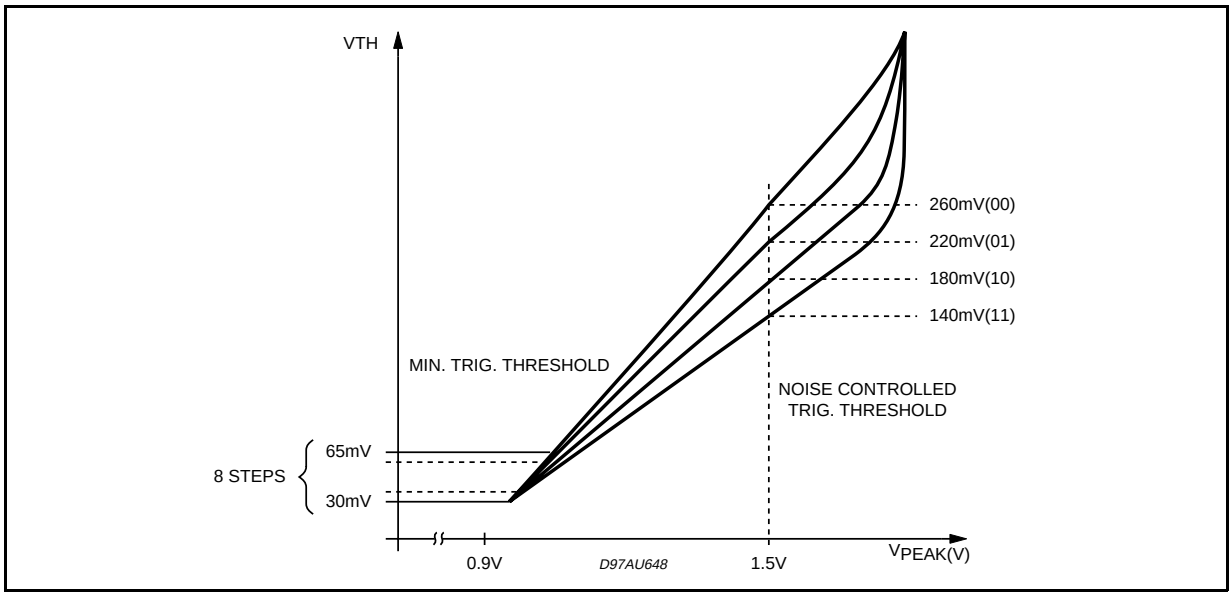


Figure 11. Deviation Controlled Trigger Adjustment

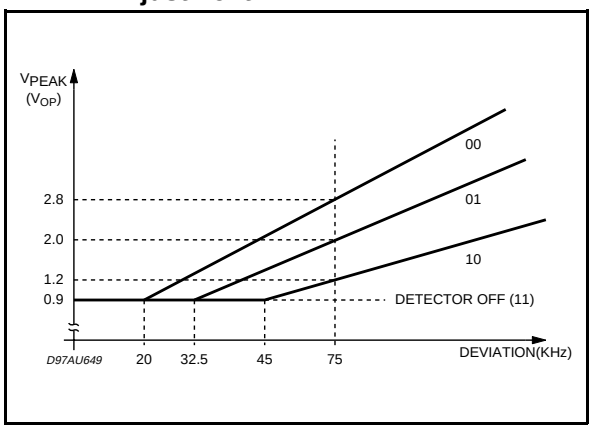


Figure 12. Fieldstrength Controlled Trigger Adjustment

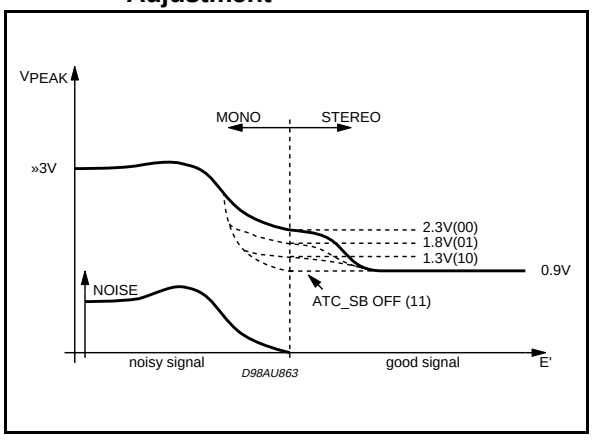
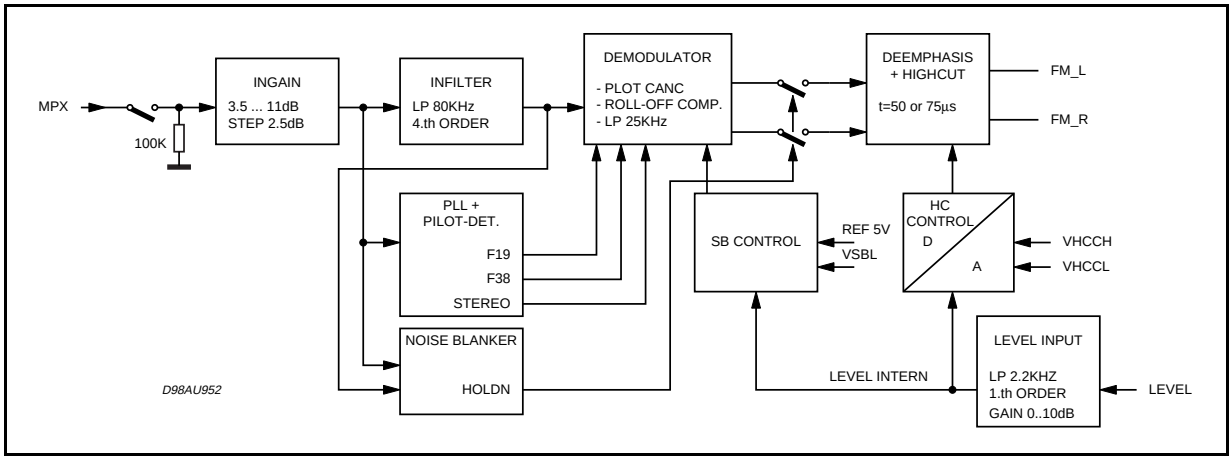


Figure 13. Block diagram of the stereo decoder



DESCRIPTION OF STEREODECODER

The stereodecoder part of the TDA7403 (see Fig. 16) contains all functions necessary to demodulate the MPX signal like pilot tone dependent MONO/STEREO switching as well as "stereoblend" and "highcut" functions.

Adaptations like programmable input gain, roll-off compensation, selectable deemphasis time constant and a programmable fieldstrength input allow to use different IF devices.

Stereodecoder Mute

The TDA7403 has a fast and easy to control RDS mute function which is a combination of the audioprocessor softmute and the high-ohmic mute of the stereodecoder. If the stereodecoder is selected and a softmute command is sent (or activated through the SM pin) the stereodecoder will be set automatically to the high-ohmic mute condition after the audio signal has been softmuted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereodecoder is unmuted immediately and the audioprocessor is softly unmuted. Fig. 14 shows the output signal V_O as well as the internal stereodecoder mute signal. This influence of Softmute on the stereodecoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereodecoder mute command (bit 0, stereodecoder byte set to "1") will set the stereodecoder in any case independently to the high-ohmic mute state.

If any other source than the stereodecoder is selected the decoder remains muted and the MPX pin is connected to Vref to avoid any discharge of the coupling capacitor through leakage currents.

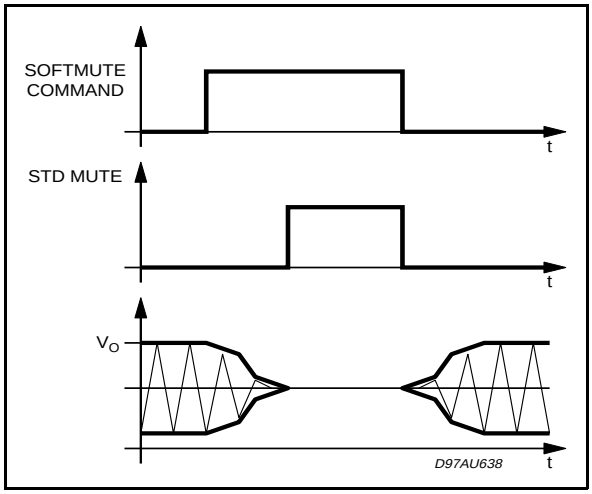
Input Stages

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4.th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and noise and acts as an antialiasing filter for the following switch capacitor filters.

Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7403 offers an I2C bus programmable roll-off adjustment which is able to compensate the low-

Figure 14. Signals during stereodecoder's softmute



pass behaviour of the tuner section. If the tuner attenuation at 38kHz is in a range from 20.2% to 31% the TDA7403 needs no external network before the MPX pin. Within this range an adjustment to obtain at least 40dB channel separation is possible.

The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation and the fieldstrength control are trimmed.

Deemphasis and Highcut

The lowpass filter for the deemphasis allows to choose between a time constant of 50µs and 75µs (bit D7, Stereodecoder byte).

The highcut control range will be in both cases $t_{HC} = 2 \cdot t_{Deemp}$. Inside the highcut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between $t_{Deemp}...3 \cdot t_{Deemp}$. There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values.

The highcut function can be switched off by I2C bus (bit D7, Fieldstrength byte set to "0").

PLL and Pilot Tone Detector

The PLL has the task to lock on the 19kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilottone threshold VPTHST. Two different thresholds are available. The detector output (signal STEREO, see block diagram) can be checked

by reading the status byte of the TDA7403 via I2C bus.

Fieldstrength Control

The fieldstrength input is used to control the high cut and the stereoblend function. In addition the signal can be also used to control the noise-blanker thresholds.

LEVEL Input and Gain

To suppress undesired high frequency modulation on the highcut and stereoblend function the LEVEL signal is lowpass filtered firstly. The filter is a combination of a 1st order RC lowpass at 53kHz (working as anti-aliasing filter) and a 1st-order switched capacitor lowpass at 2.2kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF.

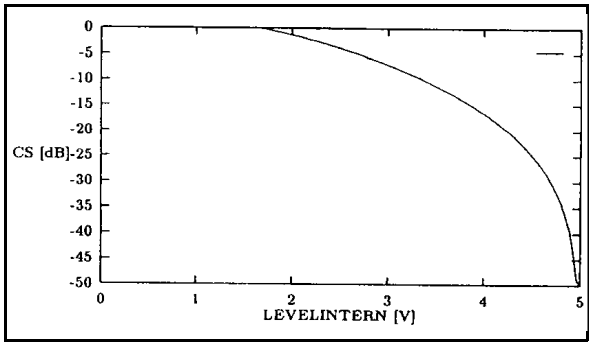
The gain is widely programmable in 16 steps from 0dB to 10dB (step = 0.67dB). These 4 bits are located together with the Roll-Off bits in the "Stereodecoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.

Stereoblend Control

The stereoblend control block converts the internal LEVEL voltage (LEVEL INTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed to be 33%, 42%, 50% or 58% of REF5V (see fig. 16).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL

Figure 15. Internal stereoblend characteristics



gain L_G and VSBL. To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain L_G has to be defined. The following equation can be used to estimate the gain:

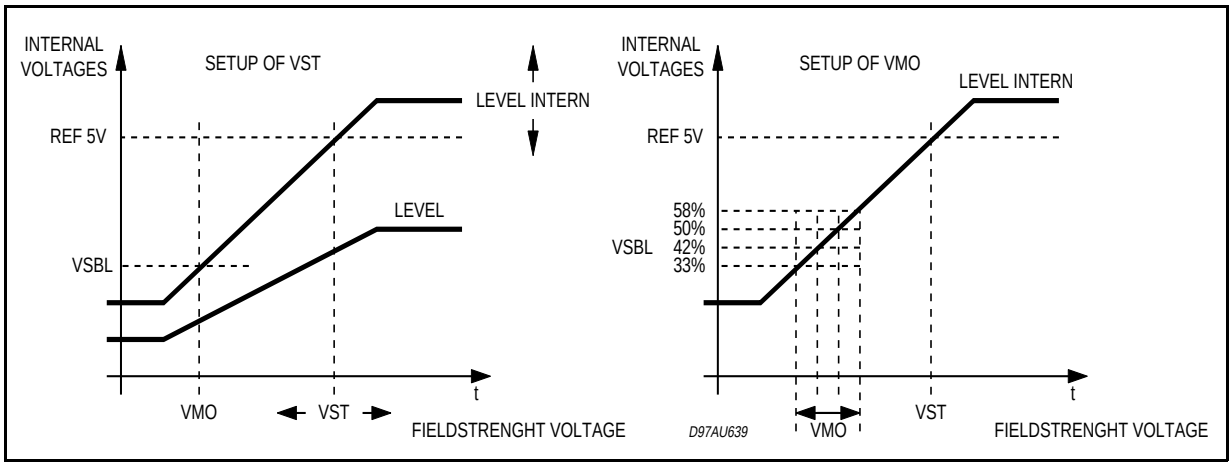
$$L_G = \frac{\text{REF5V}}{\text{Field strength voltage [STEREO]}}$$

The gain can be programmed through 4 bits in the "Stereodecoder-Adjustment" byte.

The MONO voltage VMO (0dB channel separation) can be choosen selecting 33, 42, 50 or 58% of REF5V.
All necessary internal reference voltages like REF5V are derived from a bandgap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most IF devices apply a LEVEL voltage with a TC of 3300ppm. The TDA7403 offers this TC for the reference voltages, too. The TC is selectable with bit D7 of the "stereodecoder adjustment" byte.

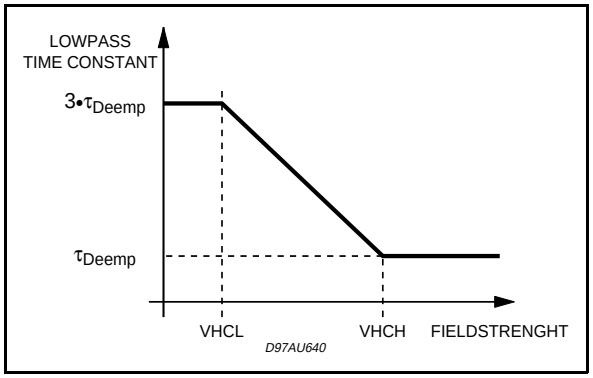
Figure 16. Relation between internal and external LEVEL voltage and setup of Stereoblend



Highcut Control

The highcut control setup is similar to the stereoblend control setup : the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17 or 33% of VHCH (see fig. 17).

Figure 17. Highcut characteristics



FUNCTIONAL DESCRIPTION OF THE NOISE-BLANKER

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noiseblanker part is to cancel the audible influence of the spikes. Therefore the output of the stereodecoder is held at the actual voltage for 40µs.

In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the triggerstage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signalpath the noiseblanker is supplied by his own biasing circuit.

Trigger Path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order high-pass-filter has a corner frequency of 140kHz. The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140kHz increases the PEAK voltage. The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signalpath for 40µs.

The block diagram of the noiseblanker is given in fig.18.

Automatic Noise Controlled Threshold Adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold:

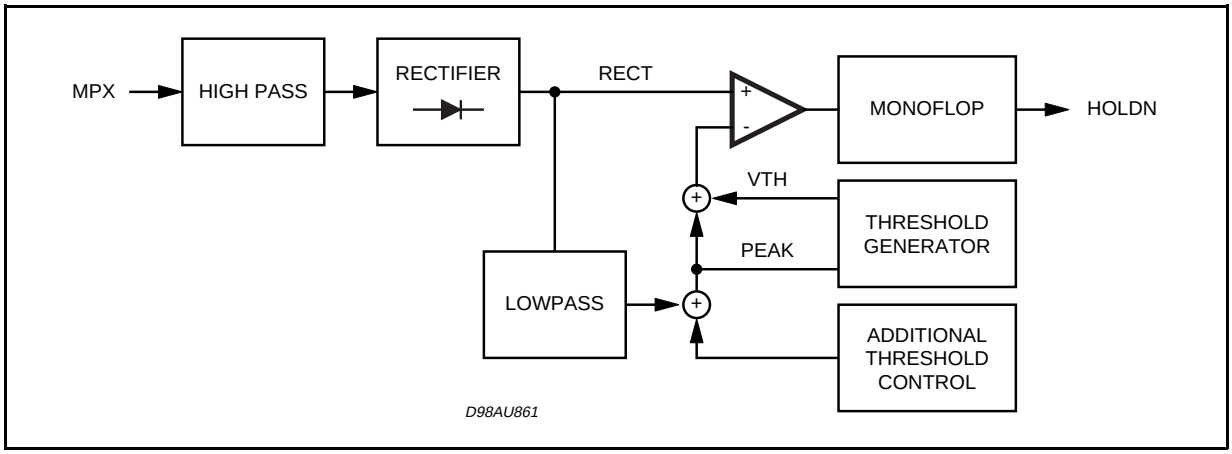
a the low threshold in 8 steps (bits D0 to D2 of the noiseblanker byte)

b the noise adjusted threshold in 4 steps (bits D3 and D4 of the noiseblanker byte, see fig. 13).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see fig. 10).

Figure 18. Block diagram of the noiseblanker



Automatic Threshold Control

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereoblend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (fig. 15). In some cases the behaviour of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occures for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.

Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereoblend. This threshold increase is programmable in 3 steps or switched off with bits D0 and D1 of the fieldstrength control byte.

Over Deviation Detector

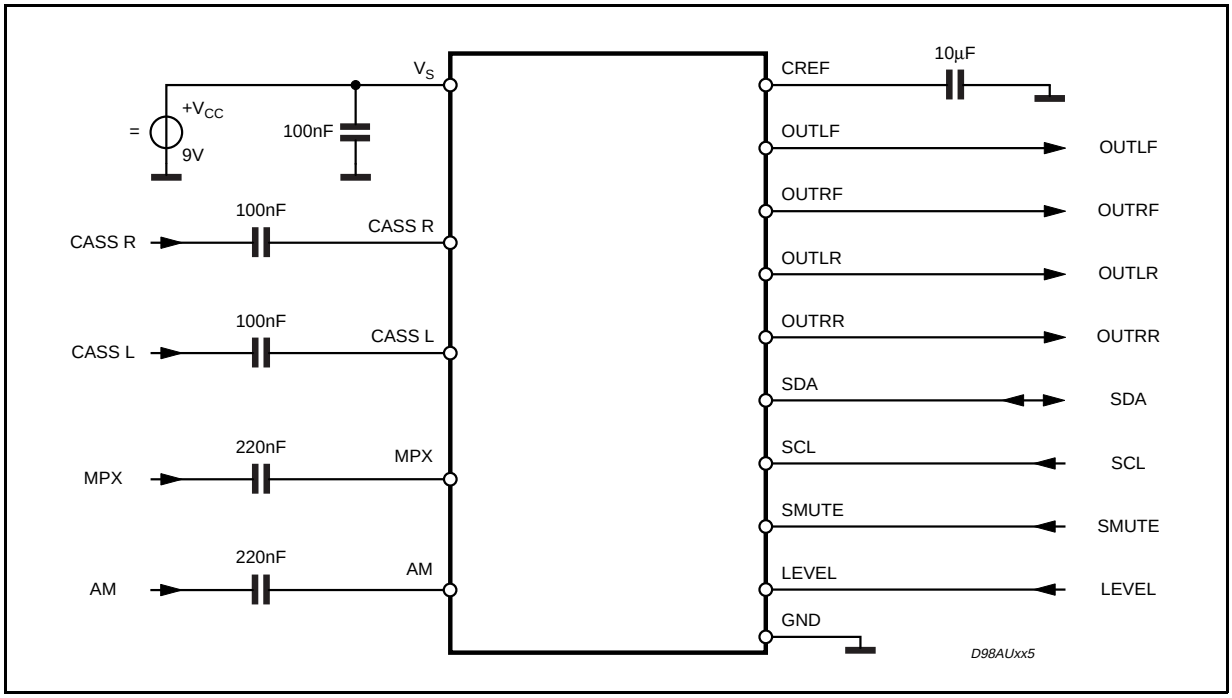
If the system is tuned to stations with a high deviation the noiseblanker can trigger on the higher frequencies of the modulation. To avoid this wrong behaviour, which causes noise in the output signal, the noiseblanker offers a deviation dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D6 and D7 of the stereodecoder byte (the first step turns off the detector, see fig. 15).

TEST MODE

During the test mode which can be activated by setting bit D0 of the testing byte and bit D5 of the subaddress byte to "1" several internal signals are available at the CASSR pin. During this mode the input resistance of 100kOhm is disconnected from the pin. The internal signals available are shown in the software specification.

Figure 19. Application Example.



I²C BUS INTERFACE DESCRIPTION

Interface Protocol

The interface protocol comprises:

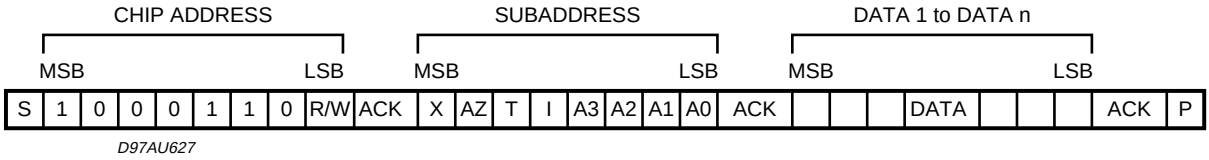
-a start condition (S)

-a chip address byte (the LSB bit determines read / write transmission)

-a subaddress byte

-a sequence of data (N-bytes + acknowledge)

-a stop condition (P)



S = Start

ACK = Acknowledge

AZ = AutoZero-Remain

T = Testing

I = Autoincrement

P = Stop

MAX CLOCK SPEED 500kbits/s

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

Auto increment

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled.

TRANSMITTED DATA (send mode)

MSB							**LSB**
X	X	X	X	ST	SM	X	X

SM = Soft mute activated

ST = Stereo

X = Not Used

SUBADDRESS (receive mode)

MSB							**LSB**	**FUNCTION**
X	AZ	T	I	A3	A2	A1	A0	
				0	0	0	0	Not allowed
				0	0	0	1	Auto-Zero
				0	0	1	0	Volume
				0	0	1	1	Softmute
				0	1	0	0	Bass / Treble Attenuator
				0	1	0	1	Bass / Treble Configuration
				0	1	1	0	Speaker attenuator LF
				0	1	1	1	Speaker attenuator LR
				1	0	0	0	Speaker attenuator RF
				1	0	0	1	Speaker attenuator RR / Blanktime adjust
				1	0	1	0	Stereodecoder
				1	0	1	1	Noiseblanker
				1	1	0	0	Fieldstrength Control
				1	1	0	1	Configuration
				1	1	1	0	Stereodecoder Adjustment
				1	1	1	1	Testing

T = Testmode

I = Autoincrement

AZ = Auto Zero Remain

X = not used

DATA BYTE SPECIFICATION

Input Selector

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Source Selector
					0	0	0	don't use
					0	0	1	Cassette
					0	1	0	don't use
					0	1	1	AM
					1	0	0	Stereo Decoder
					1	0	1	don't use
					1	1	0	Mute
					1	1	1	don't use
				X				**Don't Care**
								AM/FM Mode
			1		0	1	1	AM mono
			0		0	1	1	AM stereo
			0		1	0	0	AM through Stereo/Decoder
			1		1	0	0	FM- Stereo/Decoder
								In-Gain
0	0	0						14dB
0	0	1						12dB
:	:	:						:
1	1	0						2 dB
1	1	1						0 dB

For example to select the CD input in quasi-differential mode with gain of 8dB the Data Byte is: 0/01111000

Autozero

MSB							LSB	LOUDNESS
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	0	0	0	0	setting fix

Mute, Beep and Mixing

MSB							LSB	MUTE/BEEP/MIXING
D7	D6	D5	D4	D3	D2	D1	D0	
								Mute
							0	Enable Softmute
							1	Disable Softmute
					0	0		Mute time =0.48 ms
					0	1		Mute time =0.96 ms
					1	0		Mute time =40.4 ms
					1	1		Mute time =324 ms
				0				Stereo Decoder Softmute Influence = off
				1				Stereo Decoder Softmute Influence = on
1	1	1	1					Must be "1"

Note: for more information to the Stereodecoder-Softmute-Influence please refer to the stereodecoder description.

Volume

MSB							LSB	ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	+32dB
	0	0	0	0	0	0	1	+31dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	0	0	+20dB
	0	0	0	1	1	0	1	+19dB
	0	0	0	1	1	1	0	+18dB
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	+1dB
	0	1	0	0	0	0	0	0dB
	0	1	0	0	0	0	1	- 1dB
	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	0	-78dB
	1	1	0	1	1	1	1	-79dB
								Softstep
0								Softstep Volume = off
1								Softstep Volume = on

Note: It is not recommended to use a gain more than 20dB for system performance reason. In general, the max. gain should be limited by software to the maximum value, which is needed for the system.

Bass & Treble Attenuation

MSB							LSB	BASS & TREBLE ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble Steps
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				:	:	:	:	:
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	+2dB
				:	:	:	:	:
				1	0	0	1	+12dB
				1	0	0	0	+14dB
								Bass Steps
0	0	0	0					-14dB
0	0	0	1					-12dB
:	:	:	:					:
0	1	1	0					-2dB
0	1	1	1					0dB
1	1	1	1					0dB
1	1	1	0					+2dB
:	:	:	:					:
1	0	0	1					+12dB
1	0	0	0					+14dB

For example 12dB Treble and -8dB Bass give the following DATA BYTE : 0 0 1 1 1 0 0 1.

Bass & Treble Filter Characteristics

MSB							LSB	BASS & TREBLE FILTER
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble
						0	0	Center Frequency = 10 KHz
						0	1	Center Frequency = 12.5 KHz
						1	0	Center Frequency = 15 KHz
						1	1	Center Frequency = 17.5 KHz
								Bass
				0	0			Center Frequency = 60 Hz
				0	1			Center Frequency = 70 Hz
				1	0			Center Frequency = 80 Hz
				1	1			Center Frequency = 100Hz
				1	1			Center Frequency = 150Hz
		1	1					Quality factor = 1
		0	0					Quality factor = 1.25
		0	1					Quality factor = 1.5
		1	0					Quality factor = 2
		1	1					Quality factor = 2
	0							DC-Gain = 0dB
	1							DC-Gain = ±4.4dB
1								must be "1"

For example Treble center frequency = 15kHz, Bass center frequency = 100Hz, Bass Q = 1 and DC = 0dB give the following DATA BYTE: 1 0 0 0 1 1 1 0

Speaker Attenuation (LF, LR, RF, RR)

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
								Attenuation
		0	0	0	0	0	0	0dB
		0	0	0	0	0	1	-1dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	-23dB
		0	1	1	0	0	0	-24.5dB
		0	1	1	0	0	1	-26dB
		0	1	1	0	1	0	-28dB
		0	1	1	0	1	1	-30
		0	1	1	1	0	0	-32dB
		0	1	1	1	0	1	-35dB
		0	1	1	1	1	0	-40dB
		0	1	1	1	1	1	-50dB
		1						Speaker Mute
1	1							Must be "1" (except RR speaker; see below)
								Blank Time adj. (only at RR speaker)
0	0							38µs
0	1							25.5µs
1	0							32µs
1	1							22µs

Stereodecoder

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0	STD Unmuted
							1	STD Muted
					0	0		IN-Gain 11dB
					0	1		IN-Gain 8.5dB
					1	0		IN-Gain 6dB
					1	1		IN-Gain 3.5dB
				1				must be "1"
		1	0					Forced MONO
		1	1					MONO/STEREO switch automatically
	0							Pilot Threshold HIGH
	1							Pilot Threshold LOW
0								Deemphasis 50µs
1								Deemphasis 75µs

Noiseblanker

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	Low Threshold 65mV
					0	0	1	Low Threshold 60mV
					0	1	0	Low Threshold 55mV
					0	1	1	Low Threshold 50mV
					1	0	0	Low Threshold 45mV
					1	0	1	Low Threshold 40mV
					1	1	0	Low Threshold 35mV
					1	1	1	Low Threshold 30mV
			0	0				Noise Controlled Threshold 320mV
			0	1				Noise Controlled Threshold 260mV
			1	0				Noise Controlled Threshold 200mV
			1	1				Noise Controlled Threshold 140mV
		0						Noise blanker OFF
		1						Noise blanker ON
0	0							Over deviation Adjust 2.8V
0	1							Over deviation Adjust 2.0V
1	0							Over deviation Adjust 1.2V
1	1							Over deviation Detector OFF

Fieldstrength Control

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
						0	0	Noiseblanker Field strength Adj 2.3V
						0	1	Noiseblanker Field strength Adj 1.8V
						1	0	Noiseblanker Field strength Adj 1.3V
						1	1	Noiseblanker Field strength Adj OFF
				0	0			VSBL at 33% REF 5V
				0	1			VSBL at 42% REF 5V
				1	0			VSBL at 50% REF 5V
				1	1			VSBL at 58% REF 5V
		0	0					VHCH at 42% REF 5V
		0	1					VHCH at 50% REF 5V
		1	0					VHCH at 58% REF 5V
		1	1					VHCH at 66% REF 5V
	1							VHCL at 17% VHCH
	0							VHCL at 33% VHCH
0								High cut OFF
1								High cut ON

Configuration

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	setting fix

Stereodecoder Adjustment

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Roll-Off Compensation
					0	0	0	not allowed
					0	0	1	20.2%
					0	1	0	21.9%
					:	:	:	:
					1	0	0	25.5%
					:	:	:	:
					1	1	1	31.0%
								LEVEL Gain
	0	0	0	0				0dB
	0	0	0	1				0.66dB
	0	0	1	0				1.33dB
	:	:	:	:				:
	1	1	1	1				10dB
								Temperature compensation at LEVEL input
0								TC = 0
1								TC = 16.7mV/K (3300ppm)

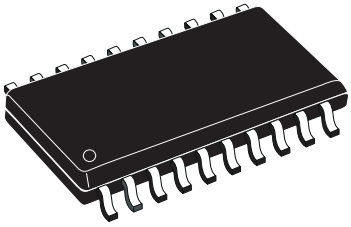
Testing

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Stereodecoder test signals
							0	OFF
							1	Test signals enabled if bit D5 of the subaddress (test mode bit) is set to "1", too
						0		External Clock
						1		Internal Clock
								Testsignals at CASS_R
		0	0	0	0			VHCCH
		0	0	0	1			Level intern
		0	0	1	0			Pilot magnitude
		0	0	1	1			VCOCON; VCO Control Voltage
		0	1	0	0			Pilot threshold
		0	1	0	1			HOLDN
		0	1	1	0			NB threshold
		0	1	1	1			F228
		1	0	0	0			VHCCL
		1	0	0	1			VSBL
		1	0	1	0			not used
		1	0	1	1			not used
		1	1	0	0			PEAK
		1	1	0	1			not used
		1	1	1	0			REF5V
		1	1	1	1			not used
								VCO
	0							OFF
	1							ON
								Audioprocessor test mode
0								only if bit D5 of the subaddress (test mode bit) is set to "1"
1								OFF

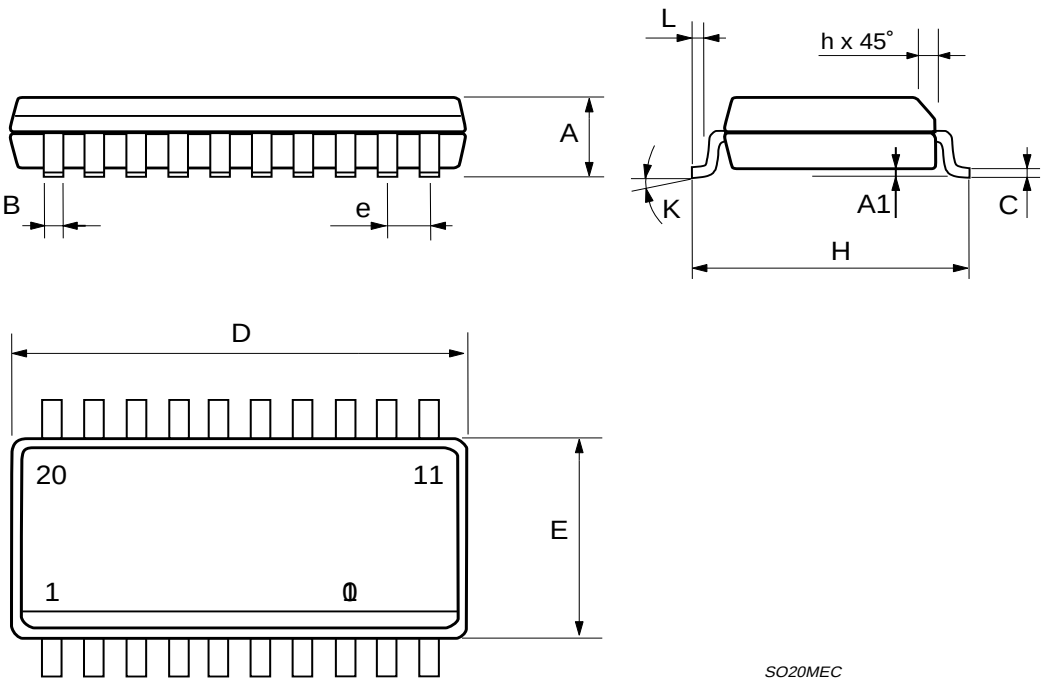
Note : This byte is used for testing or evaluation purposes only and must not be set to other values than the default "11111110" in the application!

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0˚ (min.)8˚ (max.)					

OUTLINE AND MECHANICAL DATA



SO20



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