8-/10-/12-Bit, High Bandwidth Multiplying DACs with Parallel Interface

Data Sheet

AD5424/AD5433/AD5445

FEATURES

- 2.5 V to 5.5 V supply operation
- Fast parallel interface (17 ns write cycle)
- Update rate of 20.4 MSPS
- INL of ±1 LSB for 12-bit DAC
- 10 MHz multiplying bandwidth
- ±10 V reference input
- Extended temperature range: –40°C to +125°C
- 20-lead TSSOP and chip scale (4 mm × 4 mm) packages
- 8-, 10-, and 12-bit current output DACs
- Upgrades to AD7524/AD7533/AD7545
- Pin-compatible 8-, 10-, and 12-bit DACs in chip scale
- Guaranteed monotonic
- 4-quadrant multiplication
- Power-on reset with brownout detection
- Readback function
- 0.4 µA typical power consumption

APPLICATIONS

- Portable battery-powered applications
- Waveform generators
- Analog processing
- Instrumentation applications
- Programmable amplifiers and attenuators
- Digitally controlled calibration
- Programmable filters and oscillators
- Composite video
- Ultrasound
- Gain, offset, and voltage trimming

GENERAL DESCRIPTION

The AD5424/AD5433/AD5445[1] are CMOS 8-, 10-, and 12-bit current output digital-to-analog converters (DACs), respectively. These devices operate from a 2.5 V to 5.5 V power supply, making them suitable for battery-powered applications and many other applications. These DACs utilize data readback, allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with 0s and the DAC outputs are at zero scale.

As a result of manufacturing with a CMOS submicron process, they offer excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier.

While these devices are upgrades of the AD5424/AD5433/AD5445 in multiplying bandwidth performance, they have a latched interface and cannot be used in transparent mode.

The AD5424 is available in small, 20-lead LFCSP and 16-lead TSSOP packages, while the AD5433/AD5445 DACs are available in small, 20-lead LFCSP and TSSOP packages.

The EVAL-AD5445SDZ evaluation board is available for evaluating DAC performance. For more information, see the UG-333 evaluation board user guide.

[1] U.S Patent No. 5,689,257.

FUNCTIONAL BLOCK DIAGRAM

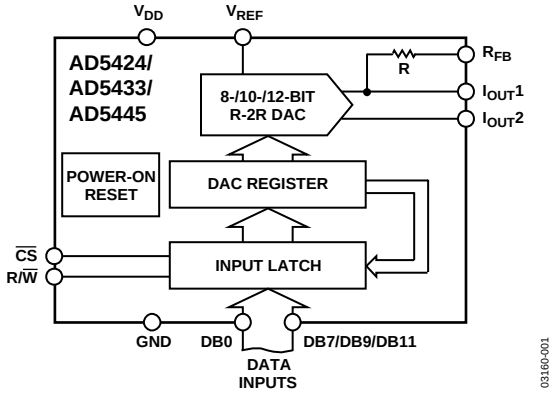

Figure 1.

Document Feedback

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SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. Temperature range for Y version: −40°C to +125°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP177 and ac performance measured with AD8038, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
AD5424					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
AD5433					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5445					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			−1/+2	LSB	Guaranteed monotonic
Gain Error			±10	mV	
Gain Error Temperature Coefficient[1]		±5		ppm FSR/°C	
Output Leakage Current[1]			±10	nA	Data = 0×0000, T_A = 25°C, $I_{OUT}1$
			±20	nA	Data = 0×0000, T = −40°C to +125°C, $I_{OUT}1$
REFERENCE INPUT[1]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
R_{FB} Resistance	8	10	12	kΩ	Input resistance TC = −50 ppm/°C
Input Capacitance					
Code Zero Scale		3	6	pF	
Code Full Scale		5	8	pF	
DIGITAL INPUTS/OUTPUT[1]					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.6	V	
Output High Voltage, V_{OH}	V_{DD} − 1			V	V_{DD} = 4.5 V to 5 V, I_{SOURCE} = 200 µA
	V_{DD} − 0.5			V	V_{DD} = 2.5 V to 3.6 V, I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	V_{DD} = 4.5 V to 5 V, I_{SINK} = 200 µA
			0.4	V	V_{DD} = 2.5 V to 3.6 V, I_{SINK} = 200 µA
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance		4	10	pF	
DYNAMIC PERFORMANCE[1]					
Reference Multiplying Bandwidth		10		MHz	V_{REF} = ±3.5 V; DAC loaded all 1s
Output Voltage Settling Time					V_{REF} = ±3.5 V, R_{LOAD} = 100 Ω, DAC latch alternately loaded with 0s and 1s
Measured to ±16 mV of full scale		30	60	ns	
Measured to ±4 mV of full scale		35	70	ns	
Measured to ±1 mV of full scale		80	120	ns	
Digital Delay		20	40	ns	Interface delay time
10% to 90% Settling Time		15	30	ns	Rise and fall time, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital-to-Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error					DAC latch loaded with all 0s, V_{REF} = ±3.5 V
		70		dB	Reference = 1 MHz
		48		dB	Reference = 10 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions
Output Capacitance					
$I_{OUT}1$		12	17	pF	All 0s loaded
		25	30	pF	All 1s loaded
$I_{OUT}2$		22	25	pF	All 0s loaded
		10	12	pF	All 1s loaded
Digital Feedthrough		1		nV-s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Analog THD		81		dB	V_{REF} = 3.5 V p-p, all 1s loaded, f = 100 kHz
Digital THD					Clock = 10 MHz, V_{REF} = 3.5 V
50 kHz f_{OUT}		65		dB	
Output Noise Spectral Density[2]		25		nV√Hz	@ 1 kHz
SFDR Performance (Wide Band)					AD5445, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					AD5445, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50 kHz f_{OUT}		82		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					AD5445, V_{REF} = 3.5 V
Clock = 10 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		65		dB	
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	
Clock = 25 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		51		dB	
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.6	µA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.4	5	µA	Logic inputs = 0 V or V_{DD}, T= −40°C to +125°C
Power Supply Sensitivity			0.001	%/%	ΔV_{DD} = ±5%

[1] Guaranteed by design, not subject to production test.
[2] Specification measured with OP27.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V; temperature range for Y version: −40°C to +125°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	V_{DD} = 2.5 V to 5.5 V	V_{DD} = 4.5 V to 5.5 V	Unit	Test Conditions/Comments
t_1	0	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	0	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_3	10	10	ns min	$\overline{CS}$ low time (write cycle)
t_4	6	6	ns min	Data setup time
t_5	0	0	ns min	Data hold time
t_6	5	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_7	9	7	ns min	$\overline{CS}$ min high time
t_8	20	10	ns typ	Data access time
	40	20	ns max	
t_9	5	5	ns typ	Bus relinquish time
	10	10	ns max	

[1] Guaranteed by design, not subject to production test.

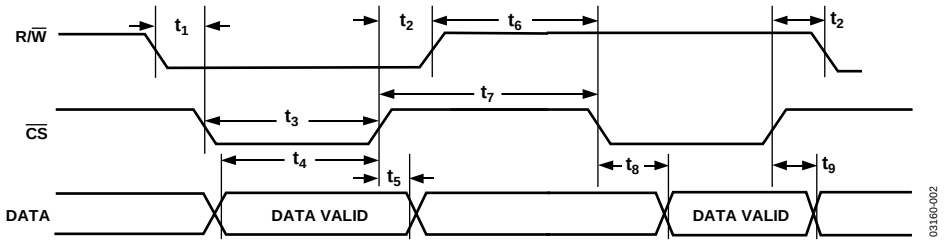


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{REF}, R_{FB} to GND	−12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	−0.3 V to +7 V
Logic Inputs and Output[1]	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Extended Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP θ_{JA} Thermal Impedance	150°C/W
20-Lead TSSOP θ_{JA} Thermal Impedance	143°C/W
20-Lead LFCSP θ_{JA} Thermal Impedance	135°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at DBx, $\overline{CS}$, and R/$\overline{W}$, are clamped by internal diodes.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

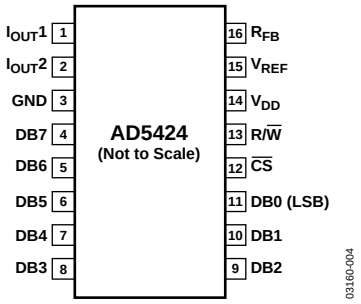


Figure 3. AD5424 Pin Configuration (TSSOP)

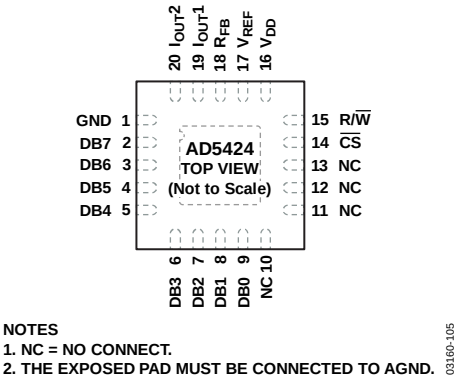


Figure 4. AD5424 Pin Configuration (LFCSP)

Table 4. AD5424 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground.
4 to 11	2 to 9	DB7 to DB0	Parallel Data Bits 7 to 0.
	10 to 13	NC	No Internal Connection.
12	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
13	15	R/$\overline{W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
14	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
15	17	V_{REF}	DAC Reference Voltage Input Terminal.
16	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

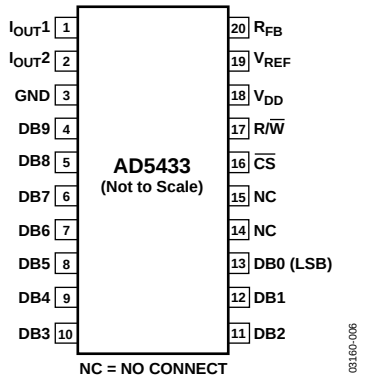


Figure 5. AD5433 Pin Configuration (TSSOP)

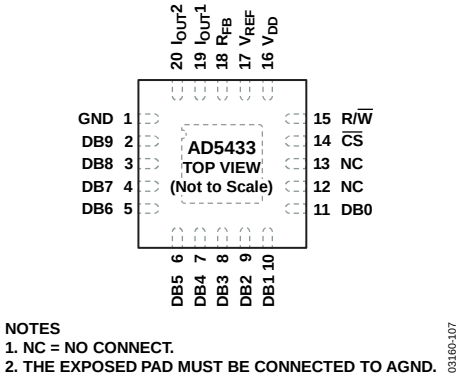


Figure 6. AD5433 Pin Configuration (LFCSP)

Table 5. AD5433 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground.
4 to 13	2 to 11	DB9 to DB0	Parallel Data Bits 9 to 0.
14, 15	12, 13	NC	Not Internally Connected.
16	14	$\overline{CS}$	Chip Select Input. Active low. Use in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V_{REF}	DAC Reference Voltage Input Terminal.
20	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

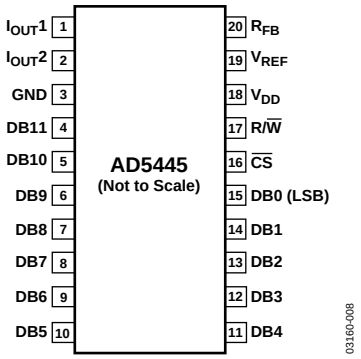


Figure 7. AD5445 Pin Configuration (TSSOP)

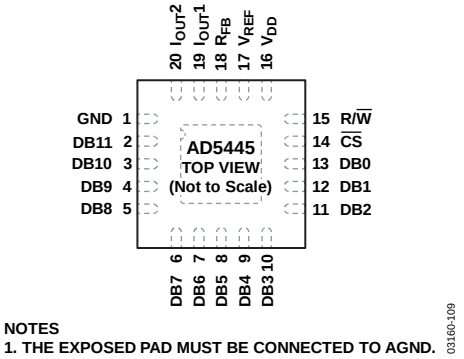


Figure 8. AD5445 Pin Configuration (LFCSP)

Table 6. AD5445 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4 to 15	2 to 13	DB11 to DB0	Parallel Data Bits 11 to 0.
16	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	R/$\overline{W}$	Read/Write. When low, use in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to read back contents of DAC register.
18	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V_{REF}	DAC Reference Voltage Input Terminal.
20	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

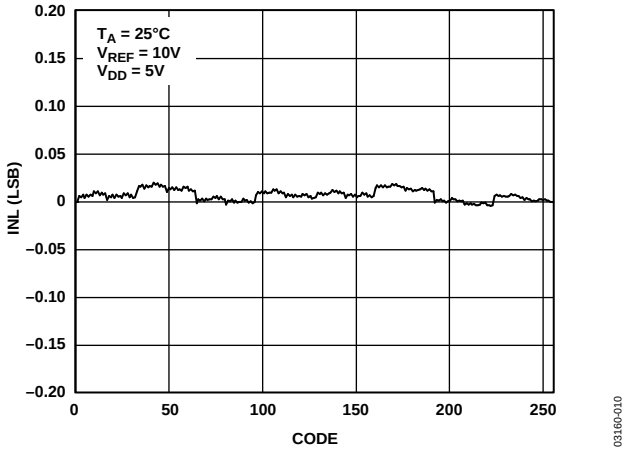


Figure 9. INL vs. Code (8-Bit DAC)

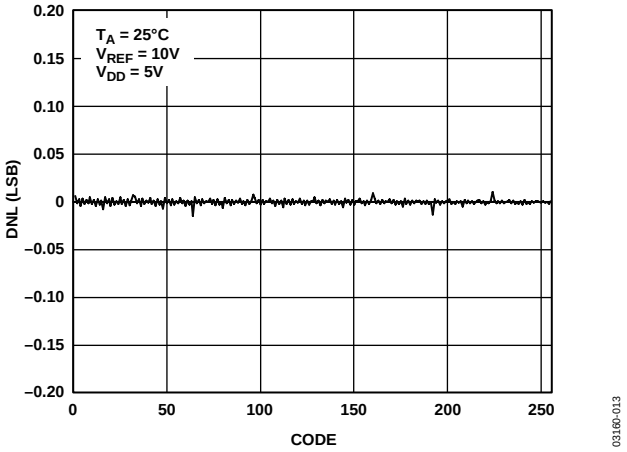


Figure 12. DNL vs. Code (8-Bit DAC)

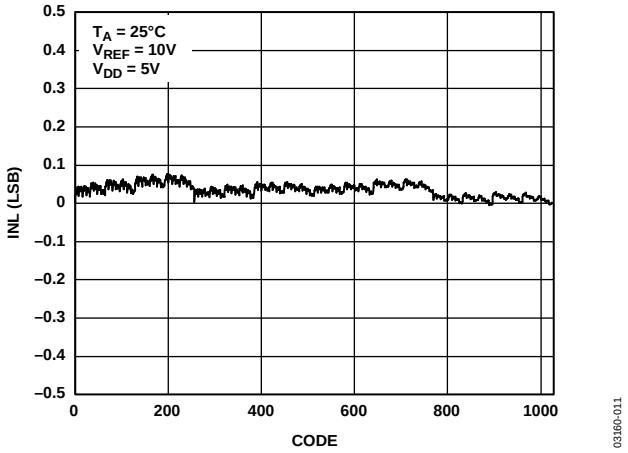


Figure 10. INL vs. Code (10-Bit DAC)

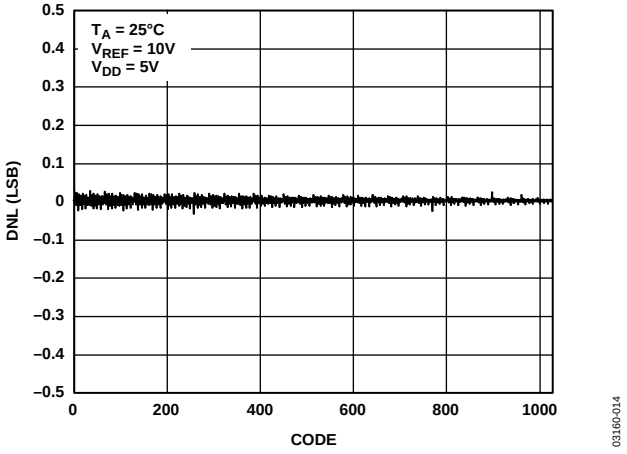


Figure 13. DNL vs. Code (10-Bit DAC)

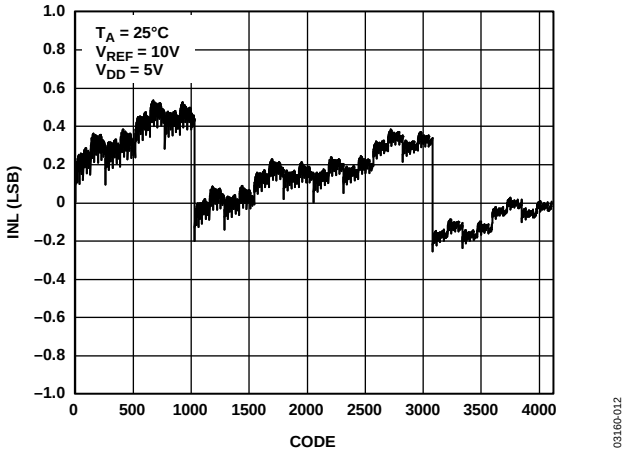


Figure 11. INL vs. Code (12-Bit DAC)

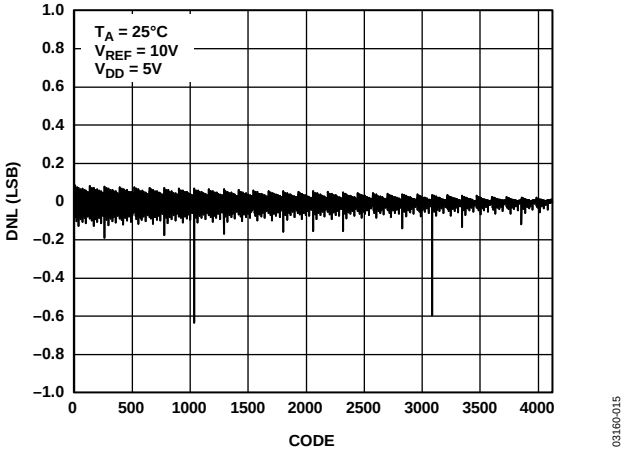


Figure 14. DNL vs. Code (12-Bit DAC)

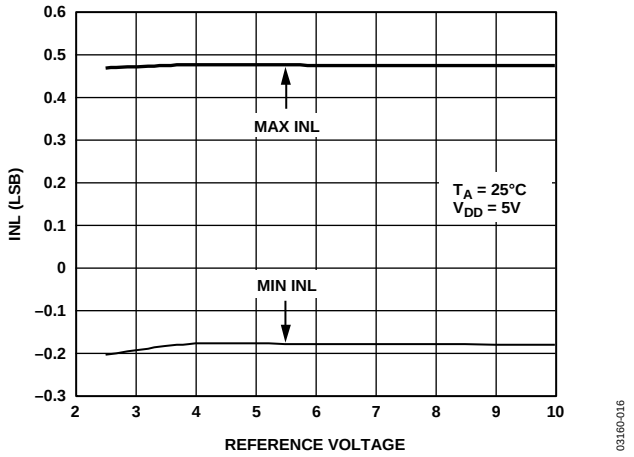


Figure 15. INL vs. Reference Voltage, AD5445

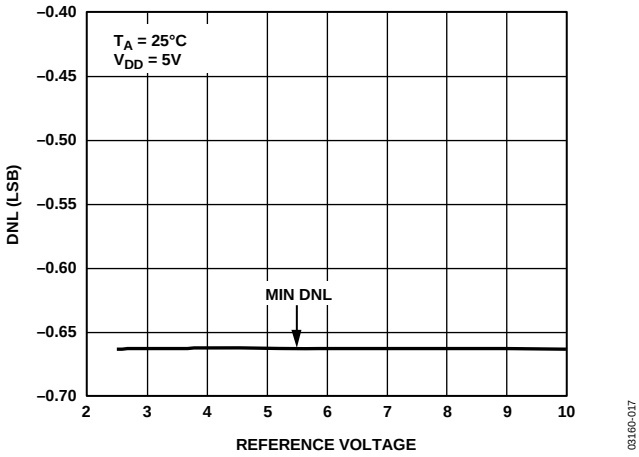


Figure 16. DNL vs. Reference Voltage, AD5445

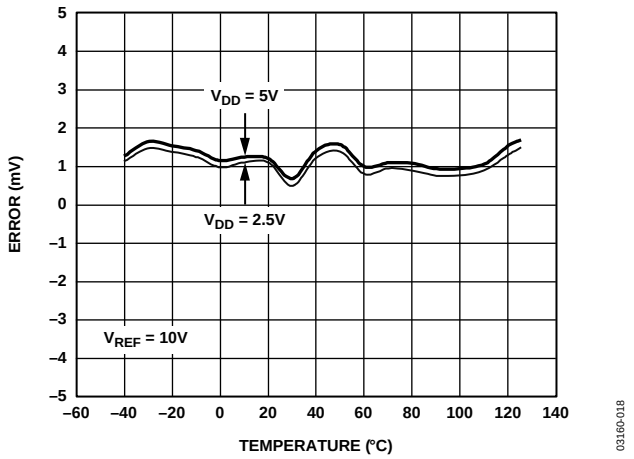


Figure 17. Gain Error vs. Temperature

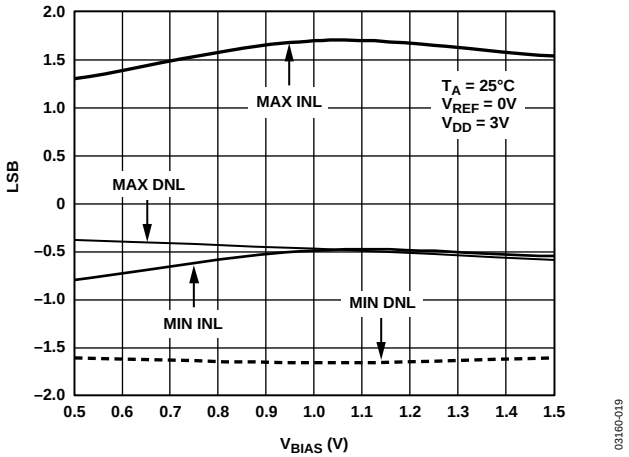


Figure 18. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445

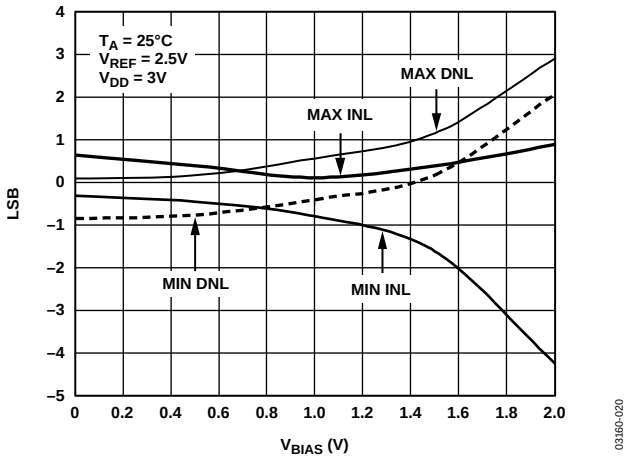


Figure 19. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445

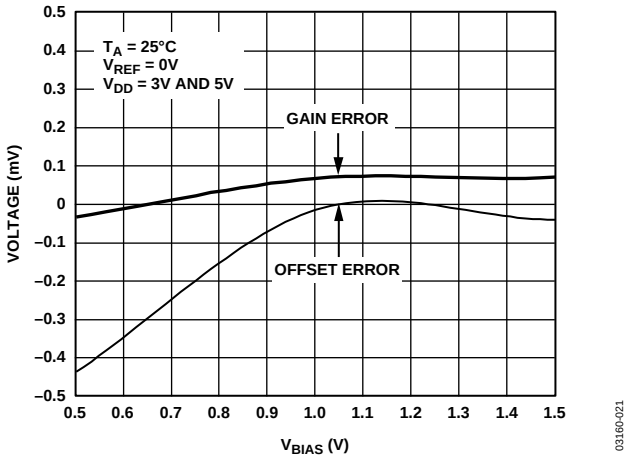


Figure 20. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

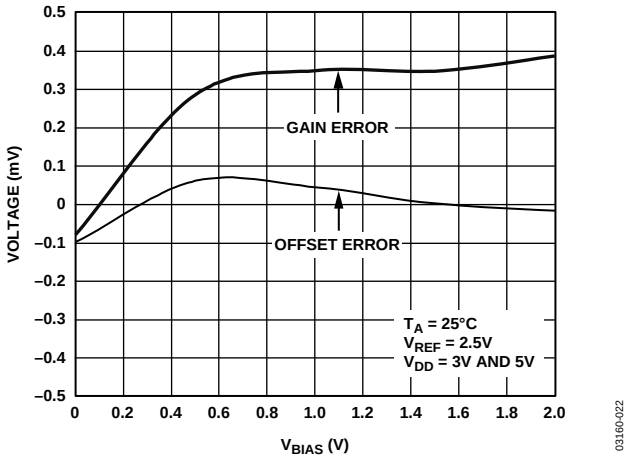


Figure 21. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$

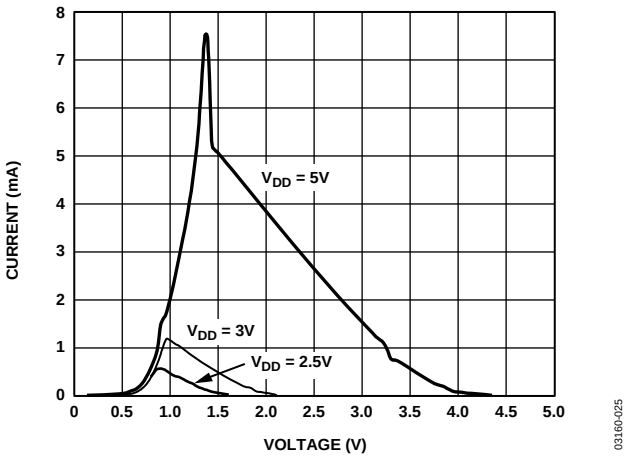


Figure 24. Supply Current vs. Logic Input Voltage (Driving DB0 to DB11, All Other Digital Inputs qt Supplies)

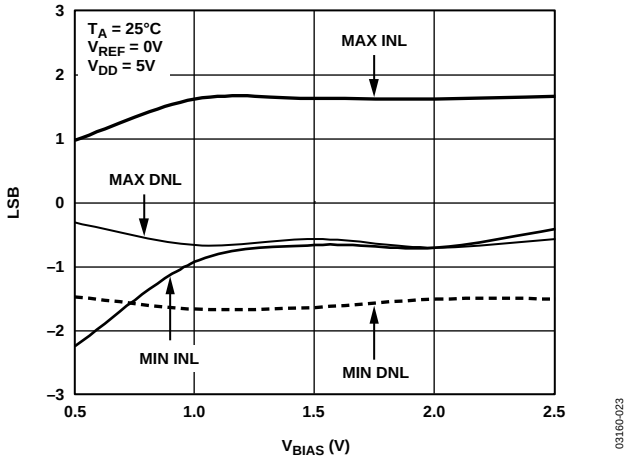


Figure 22. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445

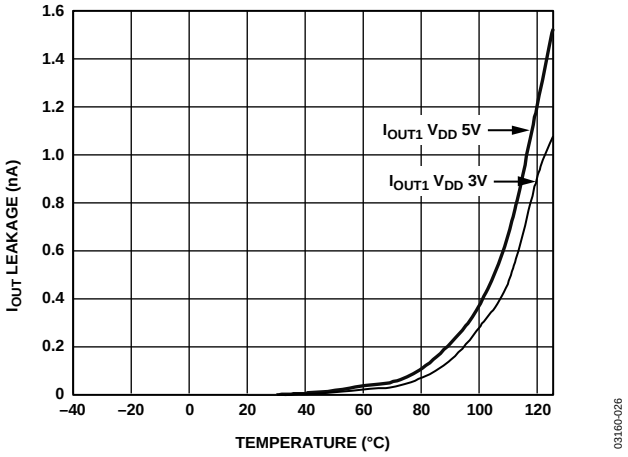


Figure 25. $I_{OUT}1$ Leakage Current vs. Temperature

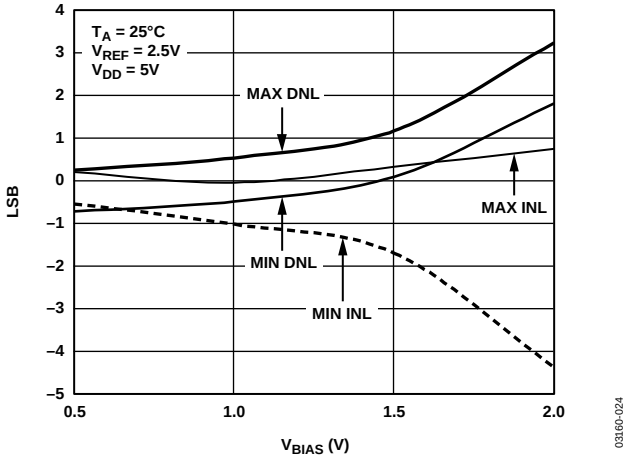


Figure 23. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445

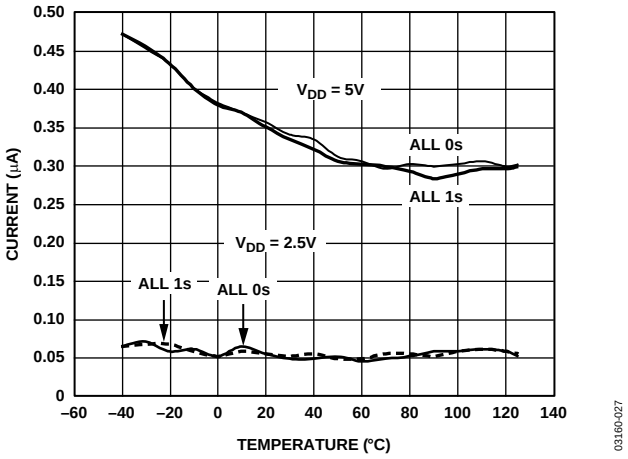


Figure 26. Supply Current vs. Temperature

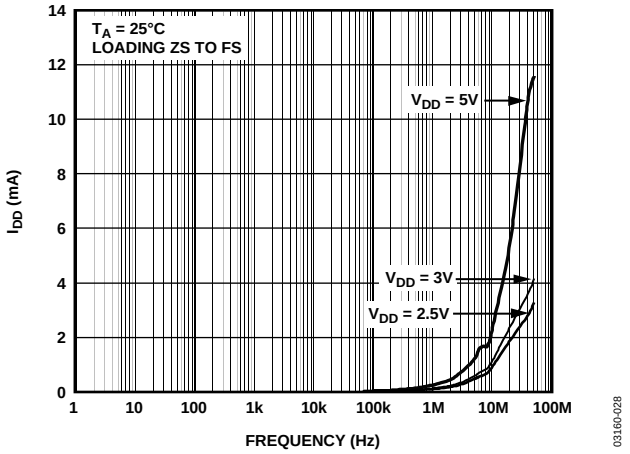


Figure 27. Supply Current vs. Update Rate

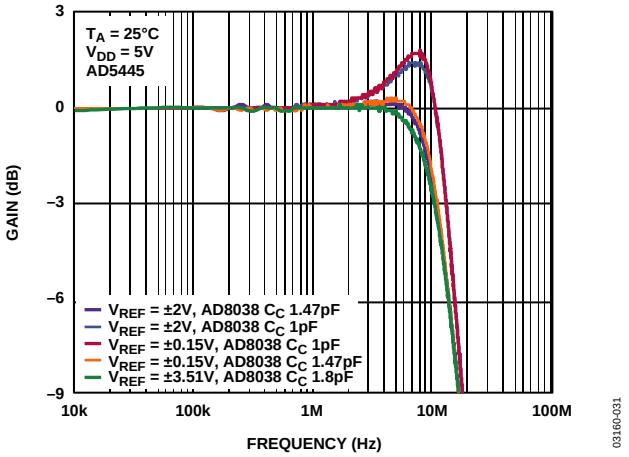


Figure 30. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor

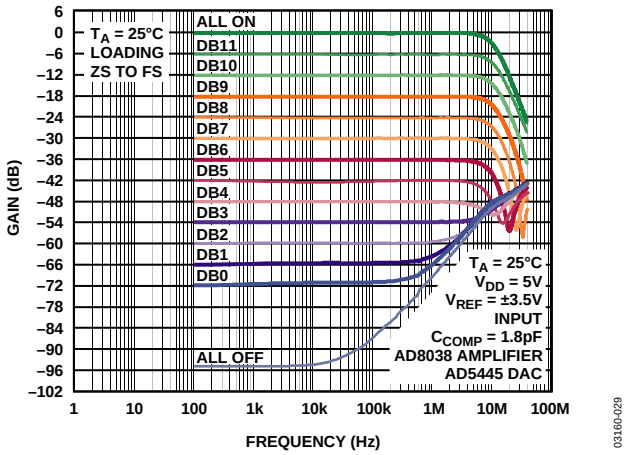


Figure 28. Reference Multiplying Bandwidth vs. Frequency and Code

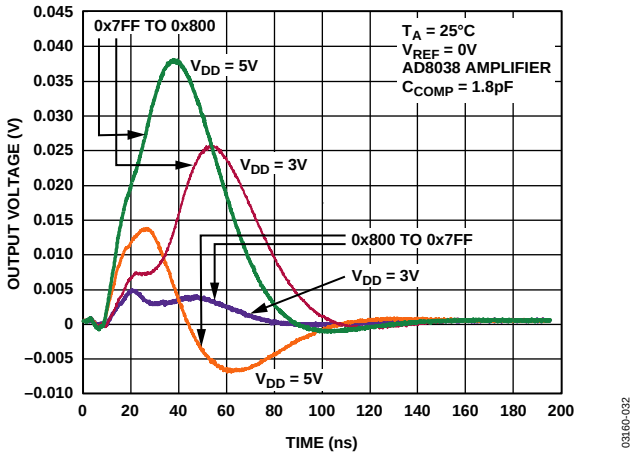


Figure 31. Midscale Transition, V_{REF} = 0 V

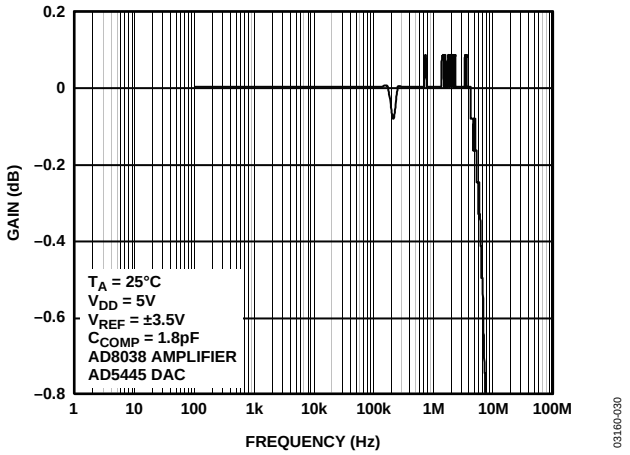


Figure 29. Reference Multiplying Bandwidth—All 1s Loaded

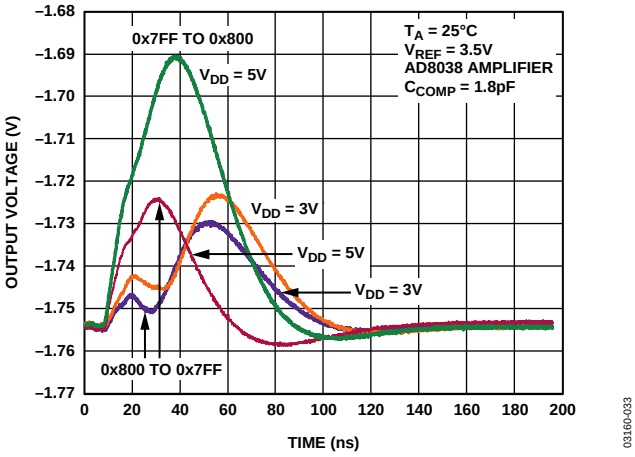


Figure 32. Midscale Transition, V_{REF} = 3.5 V

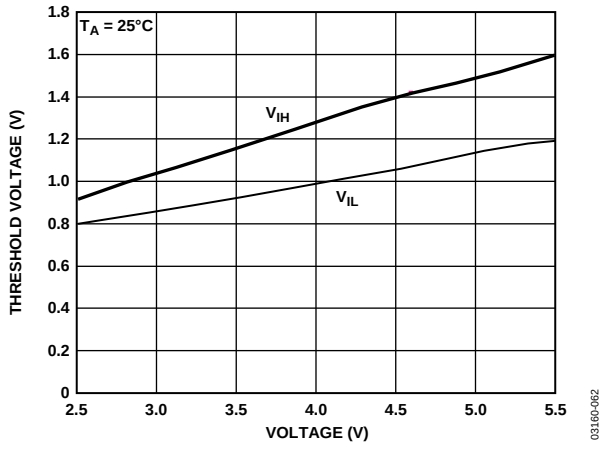


Figure 33. Threshold Voltages vs. Supply Voltage

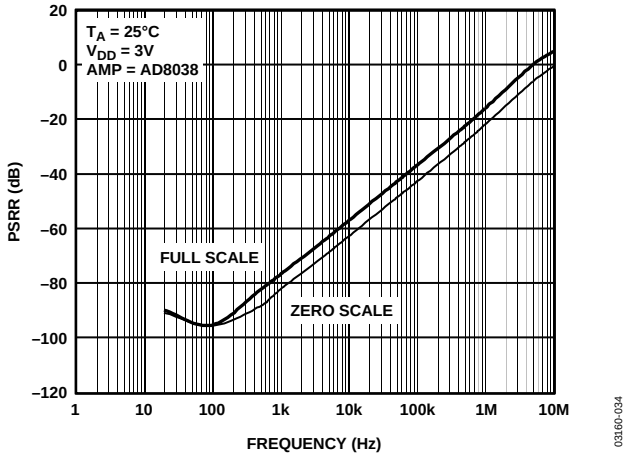


Figure 34. Power Supply Rejection vs. Frequency

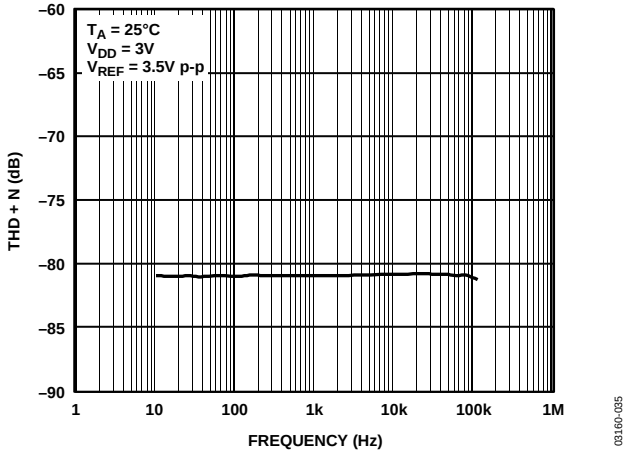


Figure 35. THD and Noise vs. Frequency

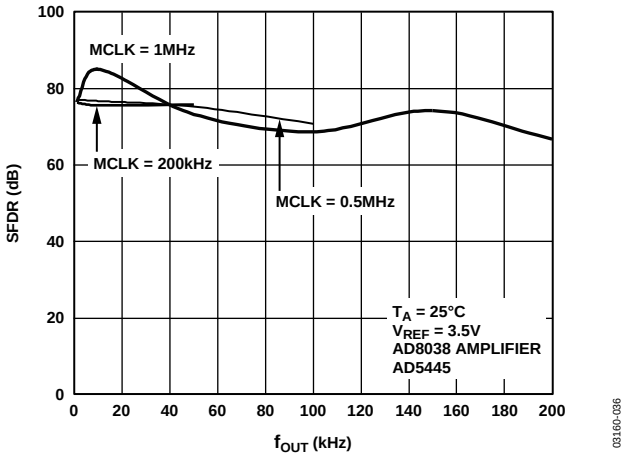


Figure 36. Wideband SFDR vs. f_{OUT} Frequency

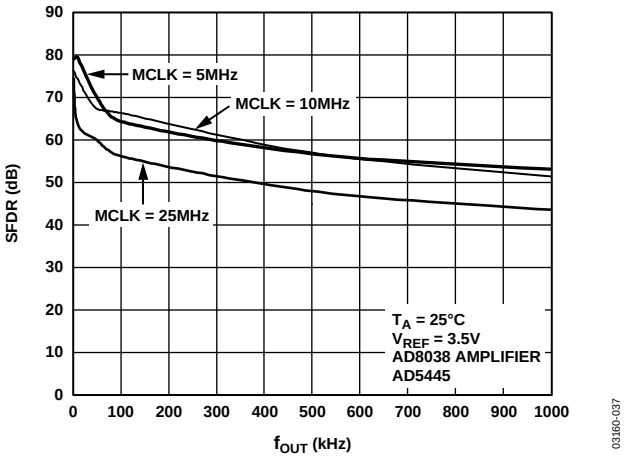


Figure 37. Wideband SFDR vs. f_{OUT} Frequency

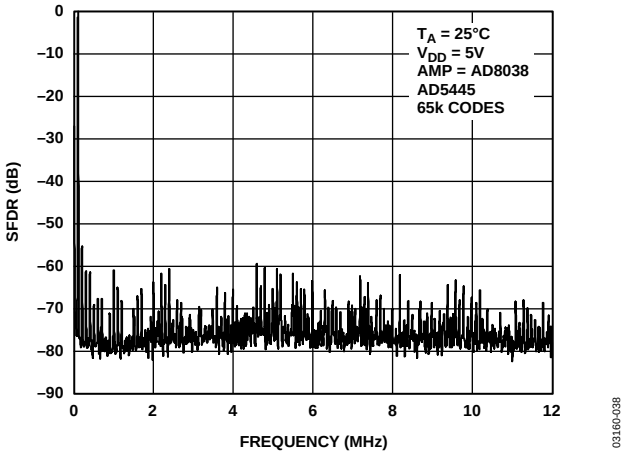


Figure 38. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz

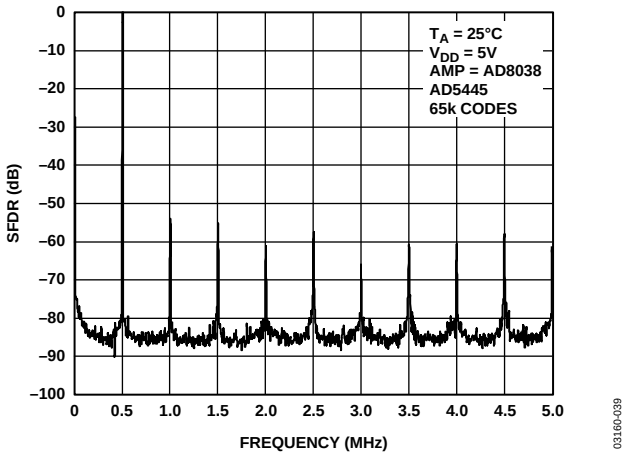


Figure 39. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz

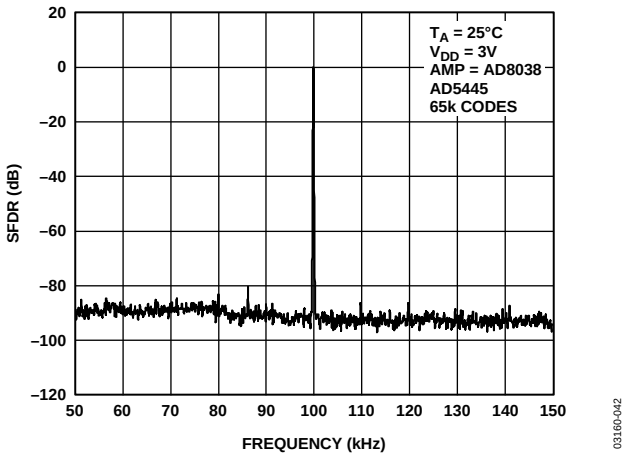


Figure 42. Narrow-Band SFDR, f_{OUT} = 100 kHz, MCLK = 25 MHz

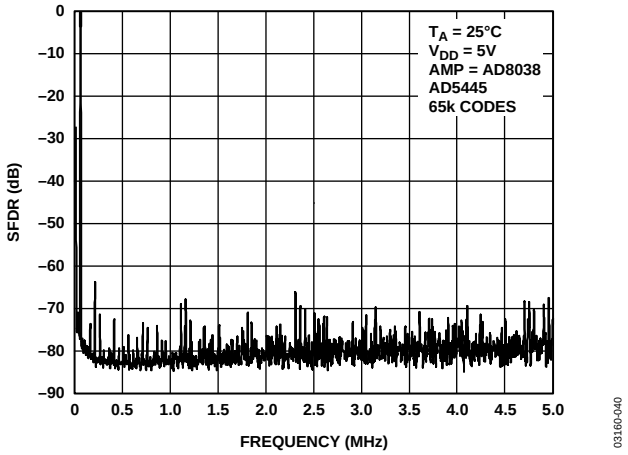


Figure 40. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz

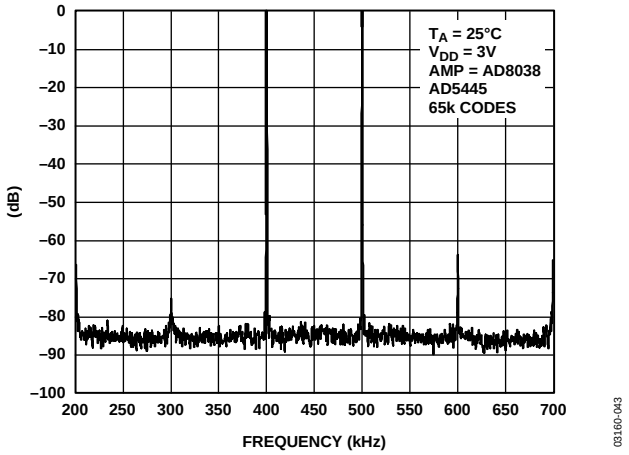


Figure 43. Narrow-Band IMD, f_{OUT} = 400 kHz, 500 kHz, Clock = 10 MHz

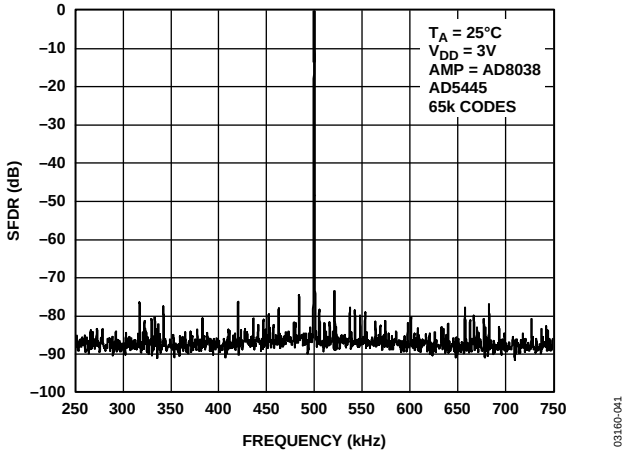


Figure 41. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz

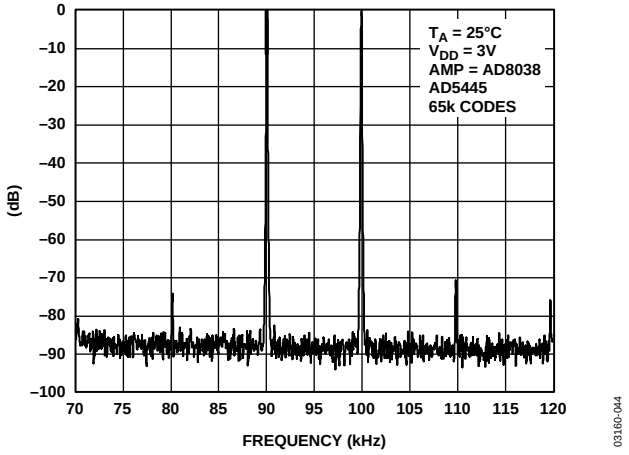


Figure 44. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz

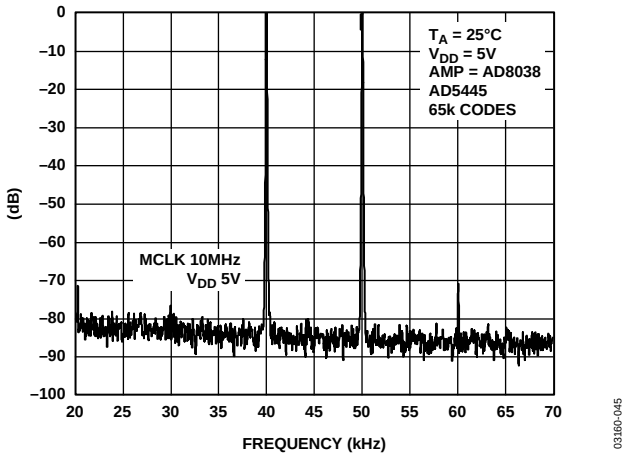


Figure 45. Narrow-Band IMD, f_{OUT} = 40 kHz, 50 kHz, Clock = 10 MHz

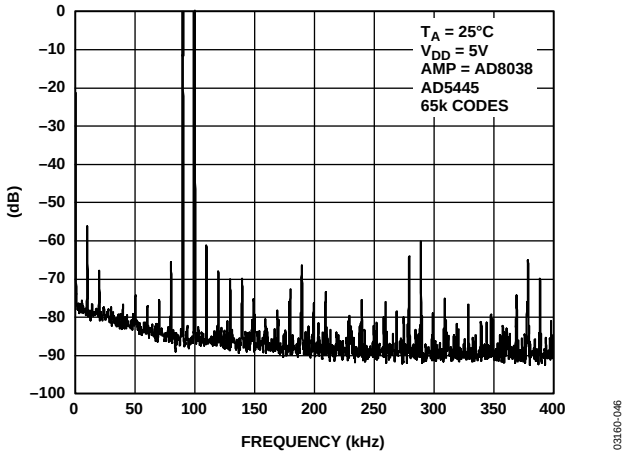


Figure 46. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz

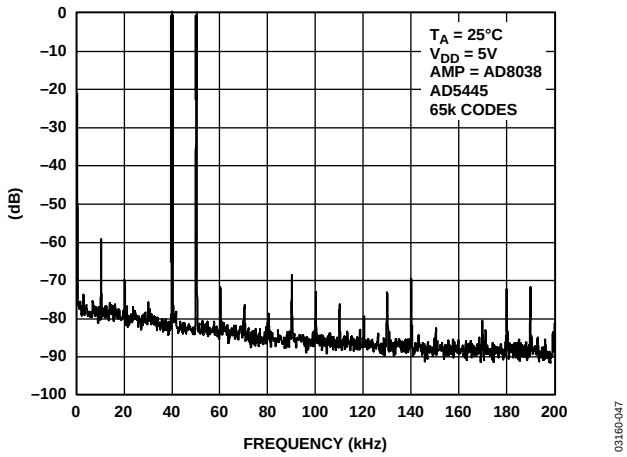


Figure 47. Wideband IMD, f_{OUT} = 60 kHz, 50 kHz, Clock = 10 MHz

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting zero scale and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of –1 LSB maximum over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} – 1 LSB. Gain error of the DACs is adjustable to 0 with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current flows in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$, or $I_{OUT}2$, to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

The settling time specification includes the digital delay from the $\overline{CS}$ rising edge to the full-scale output change.

Digital-to-Analog Glitch lmpulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA seconds or nV seconds, depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs may be capacitively coupled through the device to show up as noise on the I_{OUT} pins and subsequently in the following circuitry. This noise is called digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second to fifth.

$$THD = 20 \log \frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}$$

Digital Intermodulation Distortion
Second-order intermodulation distortion (IMD) measurements are the relative magnitude of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa − fb and 2fb − fa.

Spurious-Free Dynamic Range (SFDR)
SFDR is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. It is measured by the difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). Narrow-band SFDR is a measure of SFDR over an arbitrary window size, in this case, 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is a digitally generated sine wave.

THEORY OF OPERATION

The AD5424, AD5433, and AD5445 are 8-, 10-, and 12-bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-bit AD5424 is shown in Figure 48. The matching feedback resistor R_{FB} has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of resistance value R. The DAC output (I_{OUT}) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

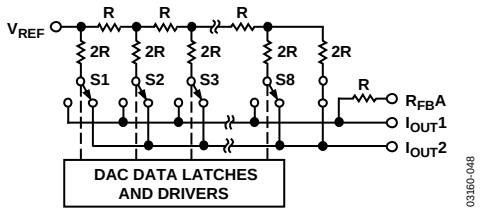


Figure 48. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$, and $I_{OUT}2$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, 4-quadrant multiplication in bipolar mode or in single-supply modes of operation. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing, as shown in Figure 49.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times \frac{D}{2^n}$$

where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

D = 0 to 255 (8-bit AD5424)
= 0 to 1023 (10-bit AD5433)
= 0 to 4095 (12-bit AD5445)

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal digital logic to drive the DAC switches' on and off states.

These DACs are also designed to accommodate ac reference input signals in the range of –10 V to +10 V.

With a fixed 10 V reference, the circuit shown in Figure 49 gives a unipolar 0 V to –10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table 7 shows the relationship between digital code and expected output voltage for unipolar operation (AD5424, 8-bit device).

Table 7. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	V_{REF} (1/256)
0000 0000	V_{REF} (0/256) = 0

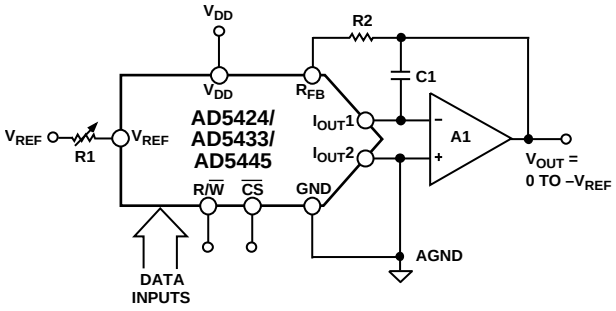


Figure 49. Unipolar Operation

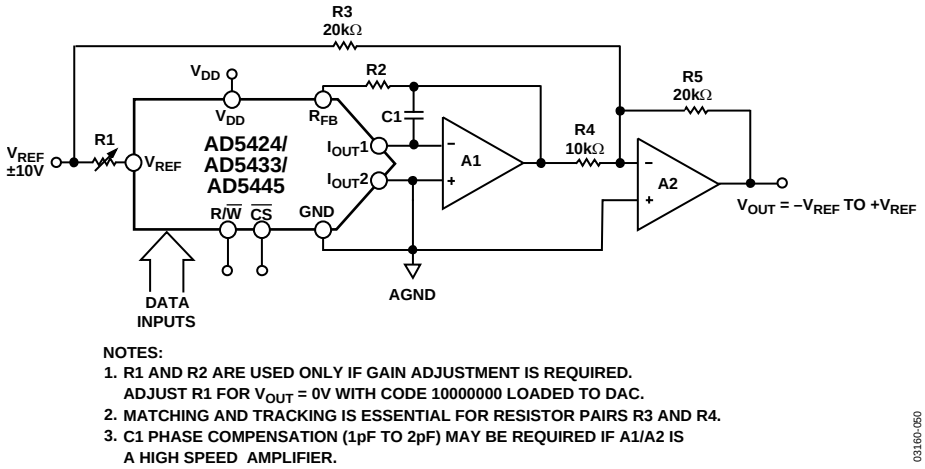


Figure 50. Bipolar Operation (4-Quadrant Multiplication)

BIPOLAR OPERATION

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors, as shown in Figure 50. In this circuit, the second amplifier, A2, provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage, results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ($V_{OUT} = -V_{REF}$) to midscale (V_{OUT} = 0 V) to full scale ($V_{OUT} = +V_{REF}$).

$$V_{OUT} = \left(V_{REF} \times D / 2^{n-1}\right) - V_{REF}$$

where D is the fractional representation of the digital word loaded to the DAC and n is the resolution of the DAC.

D = 0 to 255 (8-bit AD5424)
= 0 to 1023 (10-bit AD5433)
= 0 to 4095 (12-bit AD5445)

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table 8 shows the relationship between digital code and the expected output voltage for bipolar operation (AD5424, 8-bit device).

Table 8. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as closely as possible and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in closed-loop applications.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability, as shown in Figure 49 and Figure 50. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically, but 1 pF to 2 pF is generally adequate for compensation.

SINGLE-SUPPLY APPLICATIONS

Current Mode Operation

The current mode circuit in Figure 51 shows a typical circuit for operation with a single 2.5 V to 5 V supply. $I_{OUT}2$ and therefore $I_{OUT}1$ is biased positive by the amount applied to V_{BIAS}. In this configuration, the output voltage is given by

$$V_{OUT} = [D \times (R_{FB}/R_{DAC}) \times (V_{BIAS} - V_{IN})] + V_{BIAS}$$

As D varies from 0 to 255 (AD5424), 0 to 1023 (AD5433), or 0 to 4095 (AD5445), the output voltage varies from

$$V_{OUT} = V_{BIAS} \text{ to } V_{OUT} = 2V_{BIAS} - V_{IN}$$

V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the $I_{OUT}2$ terminal.

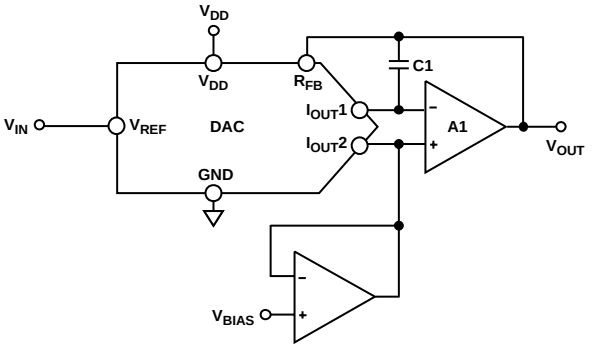


Figure 51. Single-Supply Current Mode Operation

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, there on resistance differs and the linearity of the DAC degrades.

Voltage Switching Mode of Operation

Figure 52 shows these DACs operating in the voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin, $I_{OUT}2$ is connected to AGND, and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage, making single-supply operation possible. The output from the DAC is a voltage at a constant impedance (the DAC ladder resistance), thus an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. Therefore, the voltage input should be driven from a low impedance source.

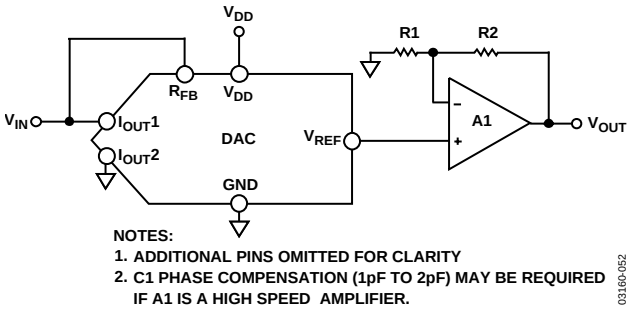


Figure 52. Single-Supply Voltage-Switching Mode Operation

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, there on resistance differs, which degrades the linearity of the DAC. See Figure 18 to Figure 23. Also, V_{IN} must not go negative by more than 0.3 V; otherwise, an internal diode turns on, exceeding the maximum ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

POSITIVE OUTPUT VOLTAGE

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. To achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor tolerance errors. To generate a negative reference, the reference can be level-shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and –2.5 V respectively, as shown in Figure 53.

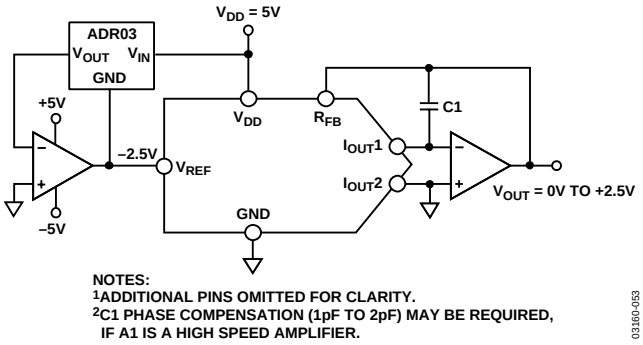


Figure 53. Positive Voltage Output with Minimum of Components

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can be achieved in a single stage. It is important to consider the effect of the temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the R_{FB} resistor causes mismatches in the temperature coefficients and results in larger gain temperature coefficient errors. Instead, the circuit shown in Figure 54 is a recommended method of increasing the gain of the circuit. R1, R2, and R3 should have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains greater than 1 are required.

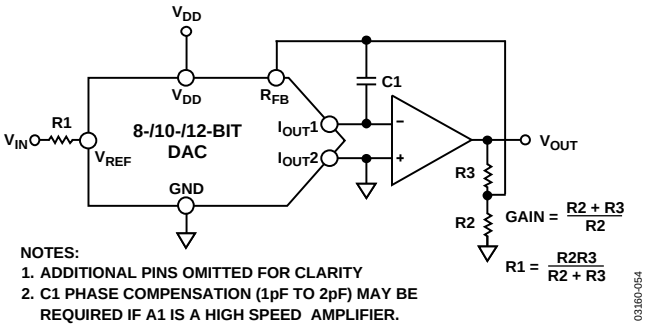


Figure 54. Increasing the Gain of the Current Output DAC

DACS USED AS A DIVIDER OR PROGRAMMABLE GAIN ELEMENT

Current steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor, as shown in Figure 55, then the output voltage is inversely proportional to the digital input fraction, D.

For $D = 1 - 2^{-n}$ the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/(1 - 2^{-n})$$

As D is reduced, the output voltage increases. For small values of D, it is important to ensure that the amplifier does not saturate and that the required accuracy is met.

For example, in the circuit shown in Figure 55, an 8-bit DAC driven with the binary code 0x10 (00010000), that is, 16 decimal, should cause the output voltage to be 16 × V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB, then D can in fact have a weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage falls in the range 15.5 V_{IN} to 16.5 V_{IN}—an error of 3% even though the DAC itself has a maximum error of 0.2%.

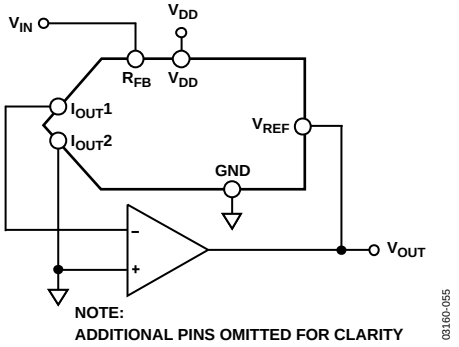


Figure 55. Current-Steering DAC Used as a Divider or Programmable Gain Element

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction, D, of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage has to change as follows:

Output Error Voltage due to DAC Leakage = (*Leakage* × *R*)/*D*

where R is the DAC resistance at the V_{REF} terminal.

For a DAC leakage current of 10 nA, R = 10 kΩ, and a gain (that is, 1/D) of 16, the error voltage is 1.6 mV.

Table 9. Suitable ADI Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Temp Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Package
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-23, SC70
ADR02	5	0.06	3	1	10	SOIC-8
ADR02	5	0.06	9	1	10	TSOT-23, SC70
ADR03	2.5	0.10	3	1	6	SOIC-8
ADR03	2.5	0.10	9	1	6	TSOT-23, SC70
ADR06	3	0.10	3	1	10	SOIC-8
ADR06	3	0.10	9	1	10	TSOT-23, SC70
ADR431	2.5	0.04	3	0.8	3.5	SOIC-8
ADR435	5	0.04	3	0.8	8	SOIC-8
ADR391	2.5	0.16	9	0.12	5	TSOT-23
ADR395	5	0.10	9	0.12	8	TSOT-23

Table 10. Suitable ADI Precision Op Amps

Part No.	Supply Voltage (V)	V_{OS} (Max) (µV)	I_B (Max) (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Package
OP97	±2 to ±20	25	0.1	0.5	600	SOIC-8
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP, SOIC-8
AD8551	2.7 to 5	5	0.05	1	975	MSOP, SOIC-8
AD8603	1.8 to 6	50	0.001	2.3	50	TSOT
AD8628	2.7 to 6	5	0.1	0.5	850	TSOT, SOIC-8

Table 11. Suitable ADI High Speed Op Amps

Part No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package
AD8065	5 to 24	145	180	1500	6000	SOIC-8, SOT-23, MSOP
AD8021	±2.5 to ±12	490	120	1000	10500	SOIC-8, MSOP
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
AD9631	±3 to ±6	320	1300	10000	7000	SOIC-8

REFERENCE SELECTION

When selecting a reference for use with the AD5424/AD5433/AD5445 family of current output DACs, pay attention to the reference's output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum system drift with temperature should be less than 78 ppm/°C.

A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized. Table 9 suggests some references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code dependent output resistance of the DAC) of the circuit. A change in the noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, could cause the DAC to be non-monotonic. In general, the input offset voltage should be <1/4 LSB to ensure monotonic behavior when stepping through codes.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing into the feedback resistor, R_{FB}. Most op amps have input bias currents low enough to prevent significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage-switching circuits, since it produces a code dependent error at the voltage output of the circuit. Most op amps have adequate common mode rejection for use at 8-, 10-, and 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low inputs capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turns requires an amplifier that can handle rail-to-rail signals. There is a large range of single-supply amplifiers available from Analog Devices.

PARALLEL INTERFACE

Data is loaded to the AD5424/AD5433/AD5445 in the format of an 8-, 10-, or 12-bit parallel word. Control lines $\overline{CS}$ and R/$\overline{W}$ allow data to be written to or read from the DAC register. A write event takes place when $\overline{CS}$ and R/$\overline{W}$ are brought low, data available on the data lines fills the shift register, and the rising edge of $\overline{CS}$ latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent, thus a write sequence must consist of a falling and rising edge on $\overline{CS}$ to ensure that data is loaded to the DAC register and its analog equivalent is reflected on the DAC output.

A read event takes place when R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. New data is loaded from the DAC register back to the input register and out onto the data line where it can be read back to the controller for verification or diagnostic purposes.

MICROPROCESSOR INTERFACING

ADSP-21xx-to-AD5424/AD5433/AD5445 Interface

Figure 56 shows the AD5424/AD5433/AD5445 interfaced to the ADSP-21xx series of DSPs as a memory-mapped device. A single wait state may be necessary to interface the AD5424/AD5433/AD5445 to the ADSP-21xx, depending on the clock speed of the DSP. The wait state can be programmed via the data memory wait state control register of the ADSP-21xx (see the ADSP-21xx family user's manual for details).

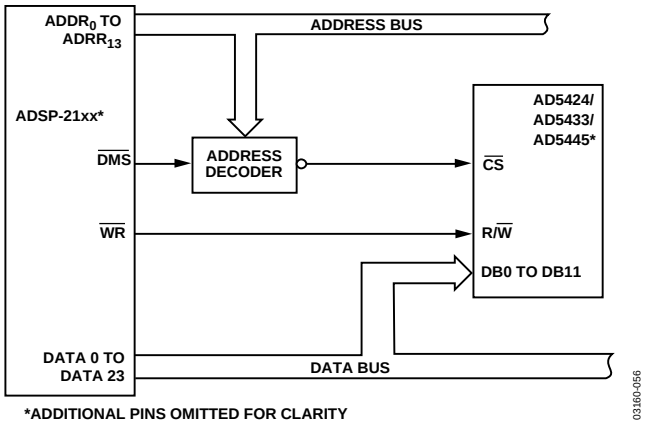


Figure 56. ADSP21xx-to-AD5424/AD5433/AD5445 Interface

8xC51-to-AD5424/AD5433/AD5445 Interface

Figure 57 shows the interface between the AD5424/AD5433/AD5445 and the 8xC51 family of DSPs. To facilitate external data memory access, the address latch enable (ALE) mode is enabled. The low byte of the address is latched with this output pulse during access to external memory. AD0 to AD7 are the multiplexed low order addresses and data bus and require strong internal pull-ups when emitting 1s. During access to external memory, A8 to A15 are the high order address bytes. Since these ports are open drained, they also require strong internal pull-ups when emitting 1s.

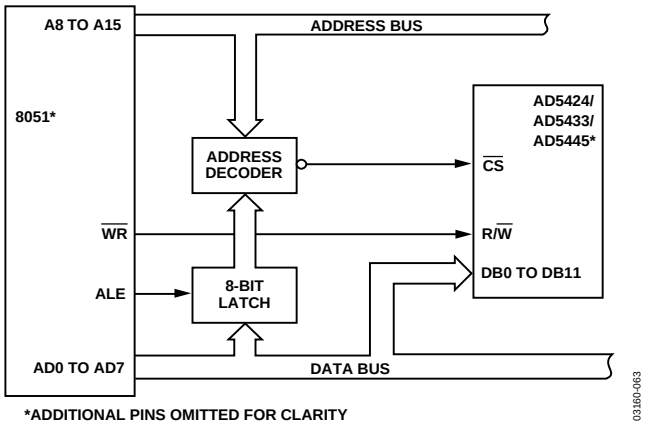


Figure 57. 8xC51-to-AD5424/AD5433/AD5445 Interface

ADSP-BF5xx-to-AD5424/AD5433/AD5445 Interface

Figure 58 shows a typical interface between the AD5424/AD5433/AD5445 and the ADSP-BF5xx family of DSPs. The asynchronous memory write cycle of the processor drives the digital inputs of the DAC. The $\overline{AMS}$x line is actually four memory select lines. Internal ADDR lines are decoded into $\overline{AMS}_{3-0}$, these lines are then inserted as chip selects. The rest of the interface is a standard handshaking operation.

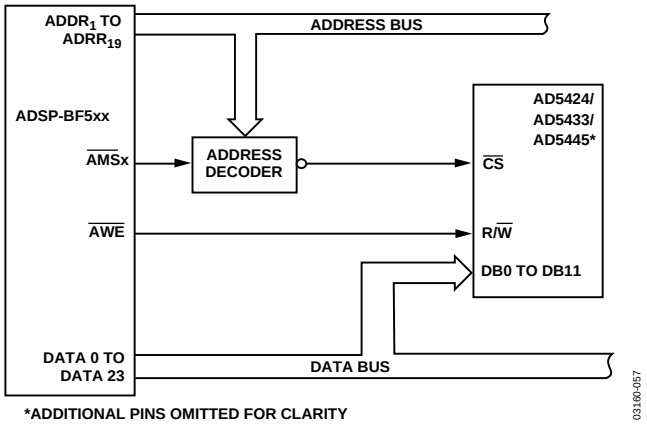


Figure 58. ADSP-BF5xx-to-AD5424/AD5433/AD5445 Interface

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5424/AD5433/AD5445 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply, located as close to the package as possible and ideally right up against the device. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, while signal traces are placed on the solder side.

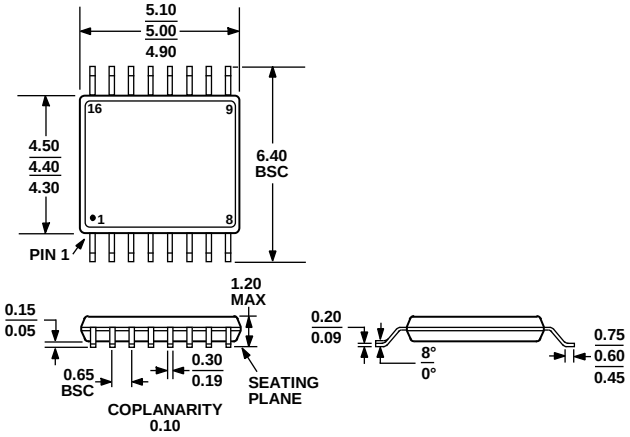
It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

Table 12. Overview of AD54xx and AD55xx Devices

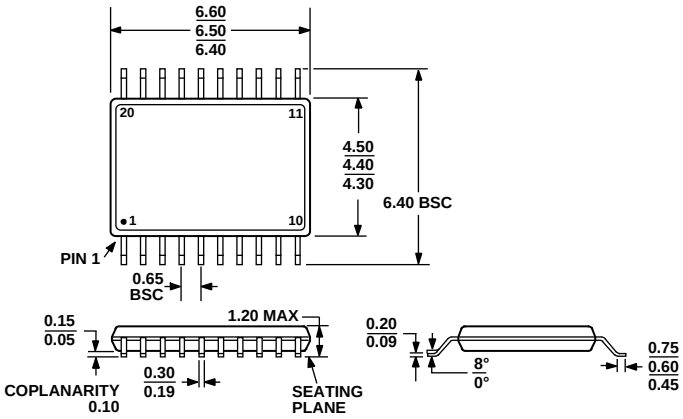
Part No.	Resolution	No. DACs	INL(LSB)	Interface	Package	Features
AD5424	8	1	±0.25	Parallel	RU-16, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5426	8	1	±0.25	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5428	8	2	±0.25	Parallel	RU-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5429	8	2	±0.25	Serial	RU-10	10 MHz BW, 50 MHz serial
AD5450	8	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5432	10	1	±0.5	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5433	10	1	±0.5	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5439	10	2	±0.5	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5440	10	2	±0.5	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5451	10	1	±0.25	Serial	RJ-8	10 MHz BW, 50 MHz serial
AD5443	12	1	±1	Serial	RM-10	10 MHz BW, 50 MHz serial
AD5444	12	1	±0.5	Serial	RM-8	50 MHz serial interface
AD5415	12	2	±1	Serial	RU-24	10 MHz BW, 50 MHz serial
AD5405	12	2	±1	Parallel	CP-40	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5445	12	2	±1	Parallel	RU-20, CP-20	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5447	12	2	±1	Parallel	RU-24	10 MHz BW, 17 ns $\overline{CS}$ pulse width
AD5449	12	2	±1	Serial	RU-16	10 MHz BW, 50 MHz serial
AD5452	12	1	±0.5	Serial	RJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5446	14	1	±1	Serial	RM-8	10 MHz BW, 50 MHz serial
AD5453	14	1	±2	Serial	UJ-8, RM-8	10 MHz BW, 50 MHz serial
AD5553	14	1	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5556	14	1	±1	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5555	14	2	±1	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5557	14	2	±1	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5543	16	1	±2	Serial	RM-8	4 MHz BW, 50 MHz serial clock
AD5546	16	1	±2	Parallel	RU-28	4 MHz BW, 20 ns $\overline{WR}$ pulse width
AD5545	16	2	±2	Serial	RU-16	4 MHz BW, 50 MHz serial clock
AD5547	16	2	±2	Parallel	RU-38	4 MHz BW, 20 ns $\overline{WR}$ pulse width

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 59. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 60. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

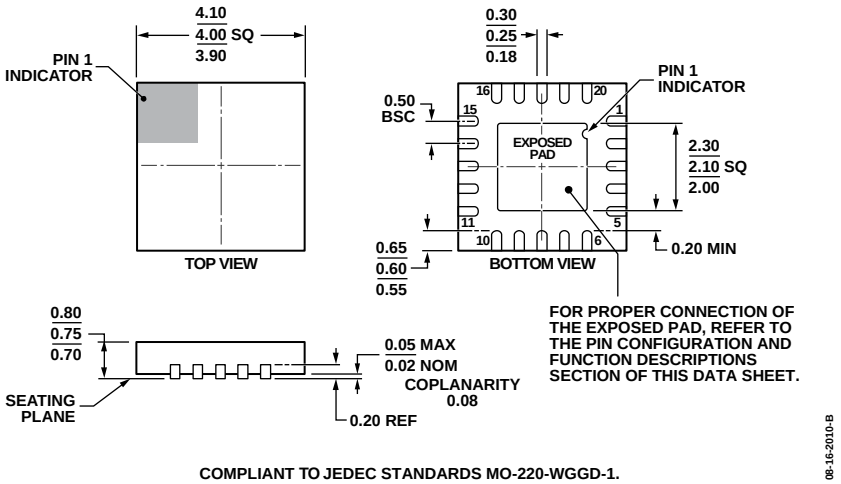


Figure 61. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution (Bits)	INL (LSB)	Temperature Range	Package Description	Package Option
AD5424YRU	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRU-REEL	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRU-REEL7	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ-REEL	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YRUZ-REEL7	8	±0.25	−40°C to +125°C	16-Lead TSSOP	RU-16
AD5424YCPZ	8	±0.25	−40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5424YCPZ-REEL7	8	±0.25	−40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5433YRU	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRU-REEL	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRU-REEL7	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ-REEL	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YRUZ-REEL7	10	±0.5	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5433YCPZ	10	±0.5	−40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
AD5445YRU	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRU-REEL	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRU-REEL7	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ-REEL	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YRUZ-REEL7	12	±1	−40°C to +125°C	20-Lead TSSOP	RU-20
AD5445YCPZ	12	±1	−40°C to +125°C	20-Lead LFCSP_WQ	CP-20-6
EVAL-AD5445SDZ				Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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