PFS7523-7529/7533-7539
HiperPFS-3 Family

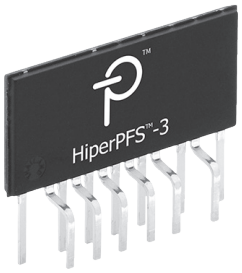
PFC Controller with Integrated High-Voltage MOSFET and Qspeed Diode Optimized for High PF and Efficiency Across Load Range

Key Benefits

- High efficiency and power factor across load range
  - >95% efficiency from 10% load to full load
  - <60 mW no-load consumption at 230 VAC
  - PF >0.92 easily achievable at 20% load
  - EN61000-3-2 Class C and D compliant
- Highly integrated for smallest boost PFC form factor
  - Integrated controller, MOSFET and ultra-low reverse recovery loss diode (Qspeed)
- Packaging optimized for high volume production
  - Eliminates insulating pad/heat-spreader
- Enhanced features
  - Programmable Power Good (PG) signal
  - User selectable power limit: Enables different HiperPFS-3 family members to be tested in the same design for optimum device selection
  - Integrated non-linear amplifier for fast output OV and UV protection and transient response
  - Digital line peak detection that provides robust performance even with distorted input voltage from UPS or generators
  - Digital power factor enhancer compensates for EMI filter and bridge distortion, providing high-line PF >0.92 @ 20% load
- Frequency adjusted over line voltage and each line cycle
  - Spread-spectrum across >60 kHz window simplifies EMI filtering requirements
  - Lower boost inductance
- Provides up to 450 W peak output power for universal applications, 1 kW for high-line only applications
- Protection features include: UVLO, UV, OV, OTP, brown-in/out, cycle-by-cycle current limit and power limiting for overload protection
- Halogen free and RoHS compliant

Applications

- PC
- Printer
- LCD TV
- Video game consoles
- 80 Plus™ Platinum designs
- High-power adaptors
- High-power LED lighting
- Industrial and appliance
- Generic PFC converters



eSIP-16D (H Package)

eSIP-16G (L Package)

Figure 2. Package Options.

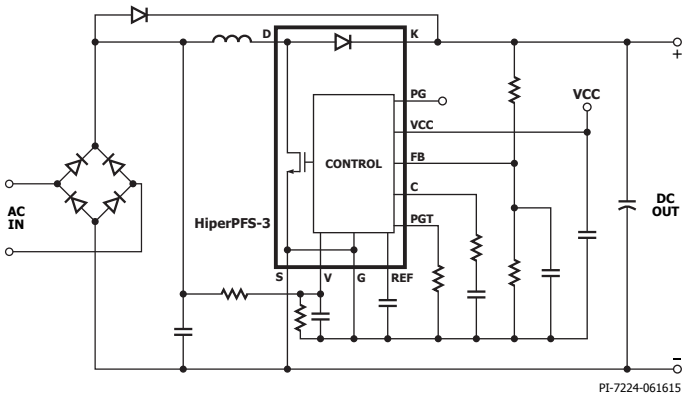


Figure 1. Typical Application Schematic.

Output Power Table

Universal Input Devices		
Product	**Maximum Continuous Output Power Rating at 90 VAC (Full Power Mode)**	**Peak Output Power (Full Power Mode)**
PFS7523L/H	110 W	120 W
PFS7524L/H	130 W	150 W
PFS7525L/H	185 W	205 W
PFS7526H	230 W	260 W
PFS7527H	290 W	320 W
PFS7528H	350 W	385 W
PFS7529H	405 W	450 W
High-Line Only Input Devices		
Product	**Maximum Continuous Output Power Rating at 180 VAC (Full Power Mode)**	**Peak Output Power (Full Power Mode)**
PFS7533H	255 W	280 W
PFS7534H	315 W	350 W
PFS7535H	435 W	480 W
PFS7536H	550 W	610 W
PFS7537H	675 W	750 W
PFS7538H	810 W	900 W
PFS7539H	900 W	1000 W

Table 1. Output Power Table (See Table 2 on page 11 for Maximum Continuous Output Power Ratings.)

This Product is Covered by Patents and/or Pending Patent Applications.

Description

The HiperPFS™-3 devices incorporate a continuous conduction mode (CCM) boost PFC controller, gate driver, ultra-low reverse recovery (Qspeed™) diode and high-voltage power MOSFET in a single, low-profile (GROUND pin connected) power package. HiperPFS-3 devices eliminate the PFC converter's need for external current sense resistors and the associated power loss, and use an innovative control technique that adjusts the switching frequency over output load, input line voltage, and even input line cycle.

This control technique maximizes efficiency over the entire load range of the converter, particularly at light loads. Additionally, it significantly minimizes the EMI filtering requirements due to its wide bandwidth spread spectrum effect. The HiperPFS-3 uses advanced digital techniques for line monitoring functions, line feed-forward scaling, and power factor enhancement, while using analog techniques for the core controller in order to maintain extremely low no-load power consumption. The HiperPFS-3 also features an integrated non-linear error amplifier for enhanced load transient response, a user programmable Power Good (PG) signal as well as user selectable power limit functionality. HiperPFS-3 includes Power Integrations' standard set of comprehensive protection features, such as integrated UV, OV, brown-in/out, and hysteretic thermal shutdown. HiperPFS-3 also provides cycle-by-cycle current limit and Safe Operating Area (SOA) protection of the power MOSFET, power limiting of the output for overload protection, and pin-to-pin short-circuit protection.

HiperPFS-3's innovative variable frequency continuous conduction mode operation (VF-CCM) minimizes switching losses by maintaining a low average switching frequency, while modulating the switching frequency in order to suppress EMI, the traditional challenge with continuous conduction mode solutions. Systems using HiperPFS-3 typically reduce the total X and Y capacitance requirements of the converter, the inductance of both the boost choke and EMI noise suppression chokes, thereby reducing overall system size and cost. Additionally, HiperPFS-3 devices dramatically reduce component count and board footprint while simplifying system design and enhancing reliability, when compared with designs that use discrete MOSFETs and controllers. The innovative variable frequency, continuous conduction mode controller enables the HiperPFS-3 to realize all of the benefits of continuous conduction mode operation while leveraging low-cost, small, simple EMI filters.

Many regions mandate high power factor for many electronic products with high power requirements. These rules are combined with numerous application-specific standards that require high power supply efficiency across the entire load range, from full load to as low as 10% load. High efficiency at light load is a challenge for traditional PFC solutions in which fixed MOSFET switching frequencies cause fixed switching losses on each cycle, even at light loads. In addition to featuring relatively flat efficiency across the load range, HiperPFS-3 also enables high power factor of >0.92 at 20% load. HiperPFS-3 simplifies compliance with new and emerging energy-efficiency standards over a broad market space in applications such as PCs, LCD TVs, notebooks, appliances, pumps, motors, fans, printers and LED lighting.

HiperPFS-3's advanced power packaging technology and high efficiency simplify the complexity of mounting the IC and thermal management, while providing very high power capabilities in a single compact package; these devices are suitable for PFC applications from 75 W to 900 W.

Product Highlights

Protected Power Factor Correction Solution

- Incorporates high-voltage power MOSFET, ultra-low reverse recovery loss Qspeed diode, controller and gate driver.
- EN61000-3-2 Class C and Class D compliance.
- Integrated protection features reduce external component count.
  - Accurate built-in brown-in/out protection.
  - Accurate built-in undervoltage (UV) protection.
  - Accurate built-in overvoltage (OV) protection.
  - Hysteretic thermal shutdown (OTP).
  - Internal power limiting function for overload protection.
  - Cycle-by-cycle power switch current limit.
  - Internal non-linear error amplifier for enhanced load transient response.
- No external current sense resistor required.
  - Provides 'lossless' internal sensing via sense-FET.
  - Reduces component count and system losses.
  - Minimizes high current gate drive loop area.
- Minimizes output overshoot and stresses during start-up
  - Integrated power limit.
- Improved dynamic response.
  - Digitally controlled input line feed-forward gain adjustment for flattened loop gain across entire input voltage range.
- Eliminates up to 40 discrete components for higher reliability and lower cost.

Solution for High Efficiency, Low EMI and High PF

- Continuous conduction mode PFC uses novel constant amp-second [on-time] volt-second [off-time] control engine.
  - High efficiency across load.
  - High power factor across load.
  - Low cost EMI filter.
- Frequency sliding technique for light load efficiency improvements.
  - >95% efficiency from 10% load to full load achievable at nominal input voltages.
- Variable switching frequency to simplify EMI filter design.
  - Varies over line input voltage to maximize efficiency and minimize EMI filter requirements.
  - Varies with input line cycle voltage by >60 kHz to maximize spread spectrum effect.

Advanced Package for High Power Applications

- Up to 450 W [universal], 1 kW [high-line only] peak output power capability in a highly compact package.
- Simple adhesive or clip mounting to heat sink.
  - No insulation pad required and can be directly connected to heat sink.
- Staggered pin arrangement for simple routing of board traces and high-voltage creepage requirements.
- Single package solution for PFC converter reduces assembly costs and layout size.

Pin Functional Description

BIAS POWER (VCC) Pin:
This is a 10.2-15 VDC [operating, 12 V typical] bias supply used to power the IC. The bias voltage must be externally clamped to prevent the BIAS POWER pin from exceeding 15 VDC to ensure long-term reliability.

REFERENCE (REF) Pin:
This pin is connected to an external bypass capacitor and is used to program the IC for either FULL or EFFICIENCY power mode. The external capacitor is connected between the REFERENCE and SIGNAL GROUND [G] pins. Note: the return trace to G must not be shared with other return traces with a potential for large return currents during surge events. The REFERENCE pin has two valid capacitor values to select 'Full' (1.0 μF ±20%) and 'Efficiency' (0.1 μF ±20%) power modes.

SIGNAL GROUND (G) Pin:
Discrete components used in the feedback circuit, including loop compensation, decoupling capacitors for the BIAS POWER (VCC), REFERENCE (REF) and VOLTAGE MONITOR (V) must be referenced to the SIGNAL GROUND (G) pin. The SIGNAL GROUND pin is also connected to the tab of the device. The SIGNAL GROUND pin should not be tied directly to the SOURCE pin external to the IC.

VOLTAGE MONITOR (V) Pin:
The VOLTAGE MONITOR pin is tied to the rectified high-voltage DC rail through a 100:1, 1% high-impedance resistor divider to minimize power dissipation and standby power consumption. The recommended resistance value is between 8 MΩ and 16 MΩ. Modifying this divider ratio affects peak power limit, brown-in/out thresholds and will degrade input current quality (reduce power factor and increase THD). A small ceramic capacitor forming an 80 μs nominal time-constant is required from the VOLTAGE MONITOR pin to the SIGNAL GROUND pin to bypass any switching noise present on the rectified DC bus.

This pin also features brown-in/out detection thresholds and incorporates a weak current source into the IC in order to act as a pull-down in the event of an open circuit condition.

COMPENSATION (C) Pin:
This pin is used for loop pole/zero compensation of the OTA error amplifier via the connection of a network of capacitors and a resistor between the COMPENSATION pin and SIGNAL GROUND pin. The COMPENSATION pin connects internally to the output of the OTA error amplifier and the input to the on-time and off-time controllers.

FEEDBACK (FB) Pin:
This pin is connected to the main voltage regulation feedback resistor divider network and is also used for fast over and undervoltage protection. This pin also detects the presence of the feedback voltage divider network at start-up and during operation. The divider ratio should be the same as the VOLTAGE MONITOR pin for proper and optimized power limit and power factor. A large upper resistor between 8 MΩ and 16 MΩ ±1% is recommended. A small ceramic capacitor between FEEDBACK and SIGNAL GROUND, forming a nominal 80 μs time-constant with the bottom resistor, is required.

POWER GOOD (PG) Pin:
Use of the PG function is optional. The POWER GOOD pin is an active low, open-drain connection which sinks current when the output voltage is in regulation. At start-up, once the FEEDBACK pin voltage has risen to ~95% of the internal reference voltage, the POWER GOOD pin is asserted low.

After start-up, the output voltage threshold at which the PG signal becomes high-impedance depends on the threshold programmed by the POWER GOOD THRESHOLD pin resistor. When not in use, the POWER GOOD pin is left unconnected.

POWER GOOD THRESHOLD (PGT) Pin:
This pin is used to program the output voltage threshold at which the PG signal becomes high-impedance representing the PFC stage falling out of regulation. The low threshold for the PG signal is programmed with a resistor between the POWER GOOD THRESHOLD and SIGNAL GROUND pins. Tying POWER GOOD THRESHOLD to the REFERENCE pin disables the power good function (i.e. POWER GOOD pin remains high impedance).

SOURCE (S) Pins:
These pins are the source connection of the power switch as well as the negative bulk capacitor terminal connection.

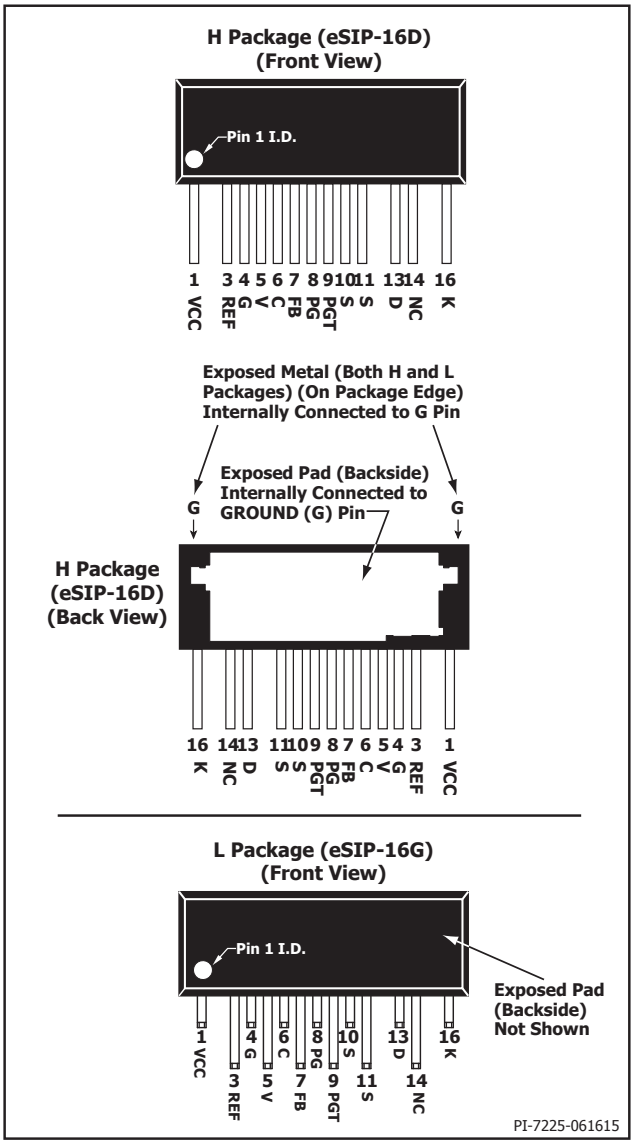


Figure 3. Pin Configuration.

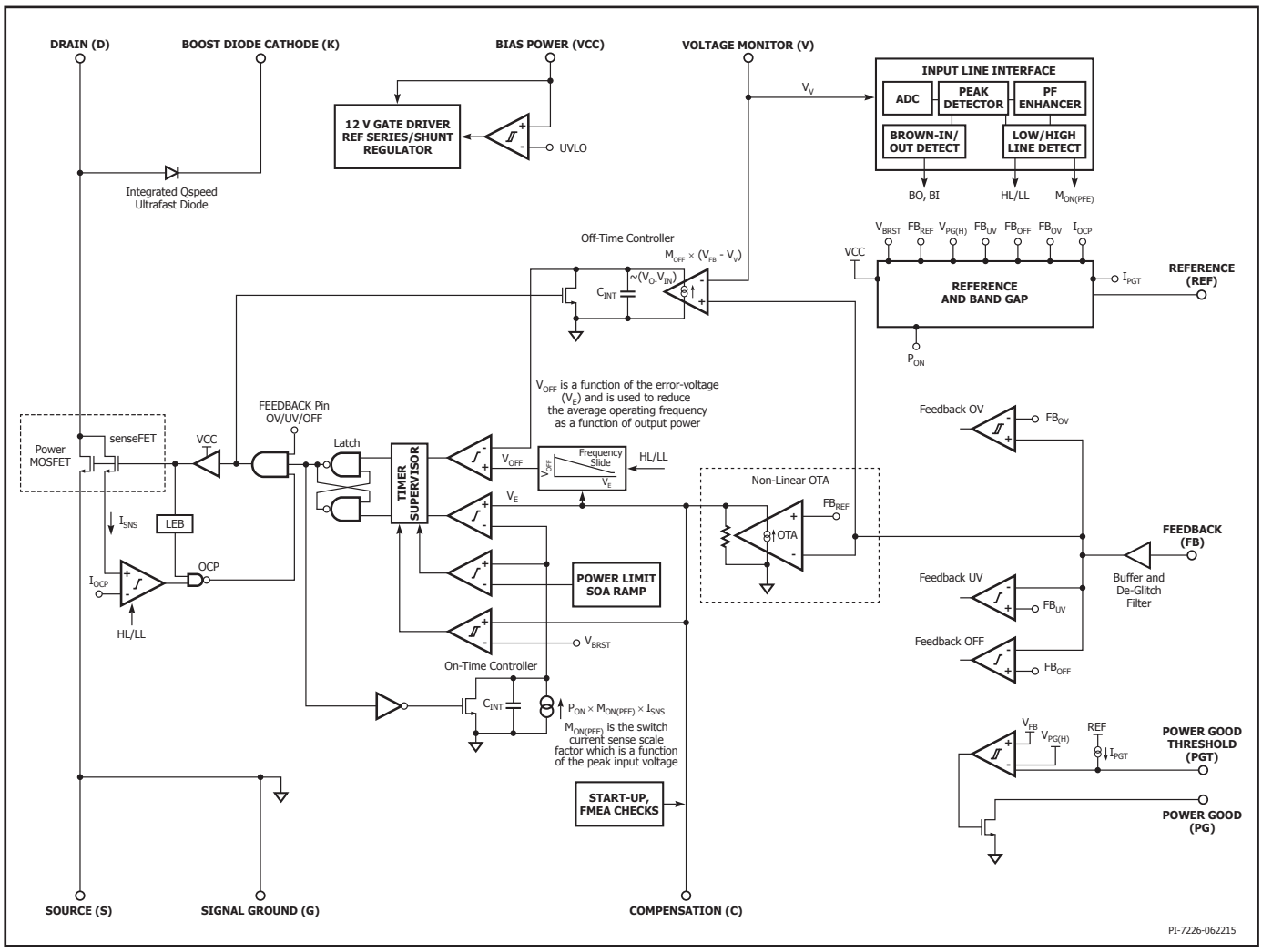


Figure 4. Functional Block Diagram.

DRAIN (D) Pin:
This is the drain connection of the internal power switch.

BOOST DIODE CATHODE (K) Pin:
This is the cathode connection of the internal Qspeed Diode.

Functional Description

The HiperPFS-3 is a variable switching frequency boost PFC solution. More specifically, it employs a constant amp-second on-time and constant volt-second off-time control algorithm. This algorithm is used to regulate the output voltage and shape the input current to comply with regulatory harmonic current limits (high power factor). Integrating the switch current and controlling it to have a constant amp-sec product over the on-time of the switch allows the average input current to follow the input voltage. Integrating the difference between the output and input voltage maintains a constant volt-second balance dictated by the electro-magnetic properties of the boost inductor and thus regulates the output voltage and power.

More specifically, the control technique sets constant volt-seconds for the off-time (t_{OFF}). The off-time is controlled such that:

$$(V_O - V_{IN}) \times t_{OFF} = K_1 \quad (1)$$

Since the volt-seconds during the on-time must equal the volt-seconds during the off-time, to maintain flux equilibrium in the PFC choke, the on-time (t_{ON}) is controlled such that:

$$V_{IN} \times t_{ON} = K_1 \quad (2)$$

The controller also sets a constant value of charge during each on-cycle of the power MOSFET. The charge per cycle is varied gradually over many switching cycles in response to load changes so it can be regarded as substantially constant for a half line cycle. With this constant charge (or amp-second) control, the following relationship is therefore also true:

$$I_{IN} \times t_{ON} = K_2 \quad (3)$$

Substituting t_{ON} from (2) into (3) gives:

$$I_{IN} = V_{IN} \times \frac{K_2}{K_1} \quad (4)$$

The relationship of (4) demonstrates that by controlling a constant amp-second on-time and constant volt-second off-time, the input current I_{IN} is proportional to the input voltage V_{IN}, therefore providing the fundamental requirement of power factor correction.

This control produces a continuous mode power switch current waveform that varies both in frequency and peak current value across a line half-cycle to produce an input current proportional to the input voltage.

Control Engine

The controller features a low bandwidth, high gain OTA error-amplifier of which its non-inverting terminal is connected to an internal voltage reference of 3.85 V. The inverting terminal of the error-amplifier is available on the external FEEDBACK pin which connects to the output voltage divider network with a divider ratio of 1:100 to regulate the output voltage to 385 V nominally. The FEEDBACK pin connects directly to the divider network for fast transient load response.

The internally sensed FET switch current is scaled by the input voltage peak detector current sense gain (M_{ON}) then integrated and compared with the error-amplifier signal (V_E) to determine the cycle on-time. Internally the difference between the input and output voltage is derived and the resultant is scaled, integrated, and compared to a voltage reference (V_{OFF}) to determine the cycle off-time. Careful selection of the internal scaling factors produces input current waveforms with very low distortion and high power factor.

Line Feed-Forward Scaling Factor (M_{ON}) and PF Enhancer

The VOLTAGE MONITOR (V) pin voltage is sampled and converted by a Δ-Σ ADC to a quantized digital value. A digital line cycle peak detector, with dynamic time constants and multi-cycle filtering, derives and smooths the peak of the input line voltage. This peak is used internally to scale the gain of the current sense signal through the M_{ON} variable. This contribution is required to reduce the dynamic range of the control feedback signal as well as flatten the loop gain over the operating input line range. The line-sense feed-forward gain adjustment is proportional to the square of the peak rectified AC line voltage and is adjusted as a function of the VOLTAGE MONITOR pin voltage.

At high-line and light load, the feed-forward M_{ON} variable is dynamically adjusted throughout the line cycle in order to compensate for the line current distortion through the EMI filter and full bridge network, thereby improving power factor.

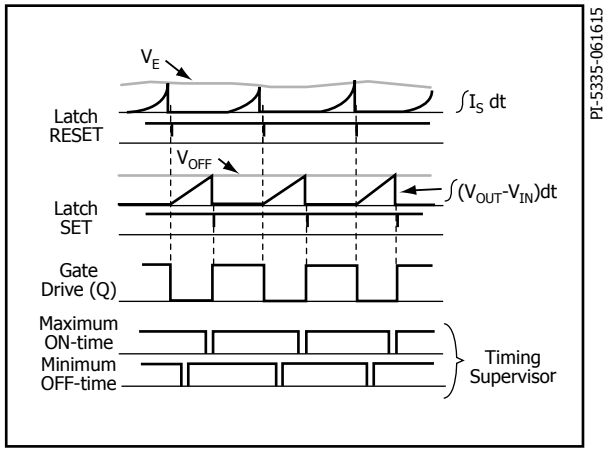


Figure 5. Idealized Converter Waveforms.

The line-sense feed-forward gain is also important in providing a switch power limit over the input line range.

This characteristic is optimized to maintain a relatively constant internal error-voltage level at full load from an input line of 90 to 230 VAC.

Beyond the specified peak power rating of the device, the internal power limit feature will regulate the output voltage below the set regulation threshold as a function of output overload to maintain a constant output power. Figure 6 illustrates the typical regulation characteristic as a function of load.

Below the brown-in threshold (V_{BR+}) the power limit is reduced when the device is operated in the 'Full' power mode as shown in Figure 7. As the input line voltage is reduced toward the brown-out threshold (V_{BR-}) and if the load exceeds the power limit derating, the boost output voltage will drop out of regulation in accordance with Figure 6.

The rated peak power shown in Table 1 is not derated for voltages below the brown-in threshold when the device is operated in the 'Efficiency' mode.

Start-Up with Pin-to-Pin Short-Circuit Protection

At start-up, the engine performs a sequence of operational checks and pin short/open evaluations, as illustrated in Figure 8, prior to the commencement of switching. When the input voltage peak is above brown-in, the engine enables switching.

The OTA error amplifier provides a non-linear amplifier (NLA) mechanism to overcome the inherently slow feedback loop response when the sensed output voltage on the FEEDBACK pin is outside its regulation window. This allows the error amplifier function to limit the maximum overshoot and undershoot during load transient events.

To reduce switch and output diode current stress at start-up, the HiperPFS-3 calculates off-time based upon output voltage (V_{OUT}) during start-up, resulting in a relatively soft controlled start-up.

Once the applied VCC is above the VCC_{UVLO+} threshold, and the output of the on-chip V_{REF} regulator is above REF_{UV+}, the value of the REFERENCE pin capacitor is detected and the full or efficiency power mode is latched. The pin open/short tests are performed, and if the FEEDBACK pin voltage is valid the over-temperature OTP is checked to be false. Once the preceding checks are satisfied the input voltage is monitored via the VOLTAGE MONITOR pin until it exceeds the V_{BR+} threshold [but the peak detector is not saturated]. It is at this point that switching is enabled.

Timing Supervisor and Operating Frequency Range

Since the controller is expected to operate with a variable switching frequency over the line frequency half-cycle, typically spanning a range of 22 – 123 kHz when operating in CCM, the controller also features a timing supervisor function which monitors and limits the maximum switch on-time and off-time as well as ensures a minimum cycle on-time. Figure 9(a) shows the typical half-line frequency profile of the device switching frequency as a function of input voltage at peak load conditions. Figure 9(b) shows for a given line condition of 115 VAC, the effect of EcoSmart™ on the switching frequency as a function of load. The switching frequency is not a function of boost choke inductance in CCM (continuous conduction mode) operation.

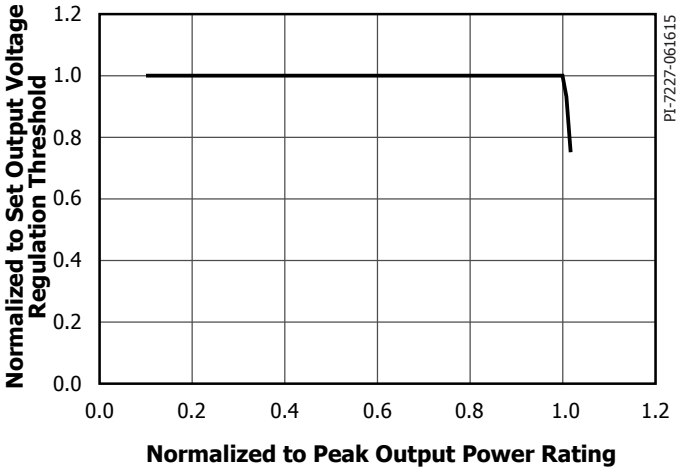


Figure 6. Typical Normalized Output Voltage Characteristics as Function of Normalized Peak Load Rating.

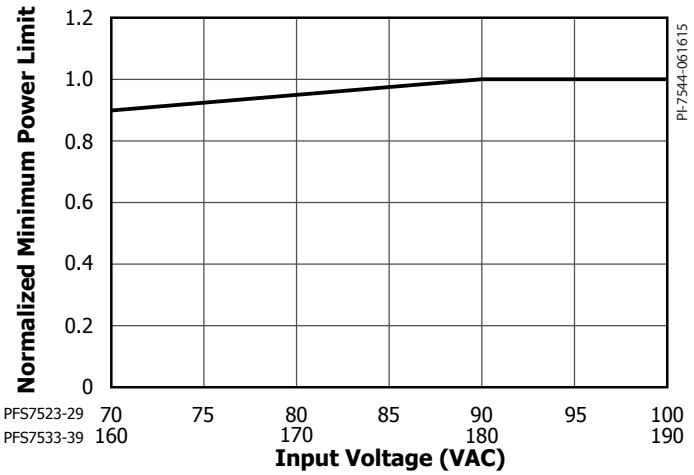


Figure 7. Normalized Minimum Power Limit as Function of Input Voltage.

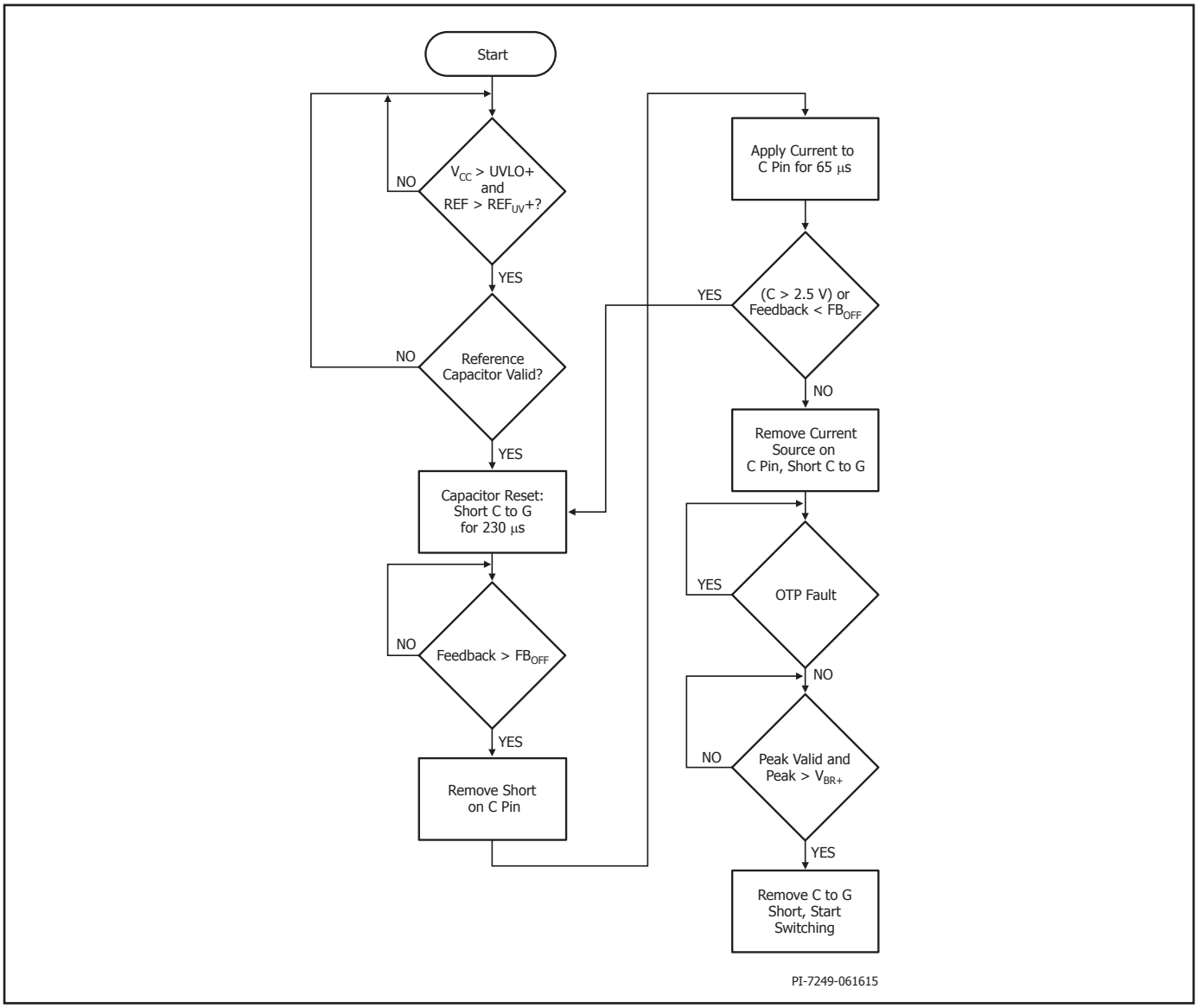


Figure 8. Start-Up Flow Chart.

EcoSmart

The HiperPFS-3 includes an EcoSmart function wherein the internal error signal (V_E) is used to detect the converter output power. Since the internal error-signal is related to the output power, this signal level is used to set the average switching frequency as a function of output power.

As shown in Figure 10, the off-time integrator control reference (V_{OFF}) is controlled with respect to the internal error-voltage level (output power) to allow the converter to maintain output voltage regulation and relatively flat conversion efficiency from 20% to 100% of rated load, which is essential to meet many efficiency directives. The degree of frequency slide is also controlled as a function of input line voltage. The lower V_{OFF} slope as a function of input voltage reduces the average frequency extremes for high input line operation.

Burst-Mode for No-Load Power Consumption Reduction

Under no-load conditions the HiperPFS-3 engine is architected to enter a burst mode which gates the power switch on and off between fixed error voltage levels. This ensures low power consumption by switching in bursts in order to maintain regulation when leakage currents constitute the majority of the load. Higher output voltage ripple at light load is an artifact of efficient burst mode operation.

Power Good Signal (PG)

The HiperPFS-3 features a 'power good' (PG) circuit which comprises an internal comparator that turns 'on' an open-drain switch during start-up when the sensed output voltage on the FEEDBACK pin rises to ~95% (V_{PG+}) of the set output voltage threshold. During start-up, prior to the output voltage reaching V_{PG+}, the PG signal is in a high-impedance state (internal switch is in 'off' state).

The power good signal transitions from 'on' to 'off' state when the sensed output voltage on the FEEDBACK pin falls to a user selected threshold, programmed with a resistor on the POWER GOOD THRESHOLD (PGT) pin. The POWER GOOD THRESHOLD pin sources a fixed current I_{PGT}. This current combined with the power good threshold resistor sets the threshold when the power good signal transitions from the 'on' state to the high-impedance 'off' state as the PFC output falls out of regulation.

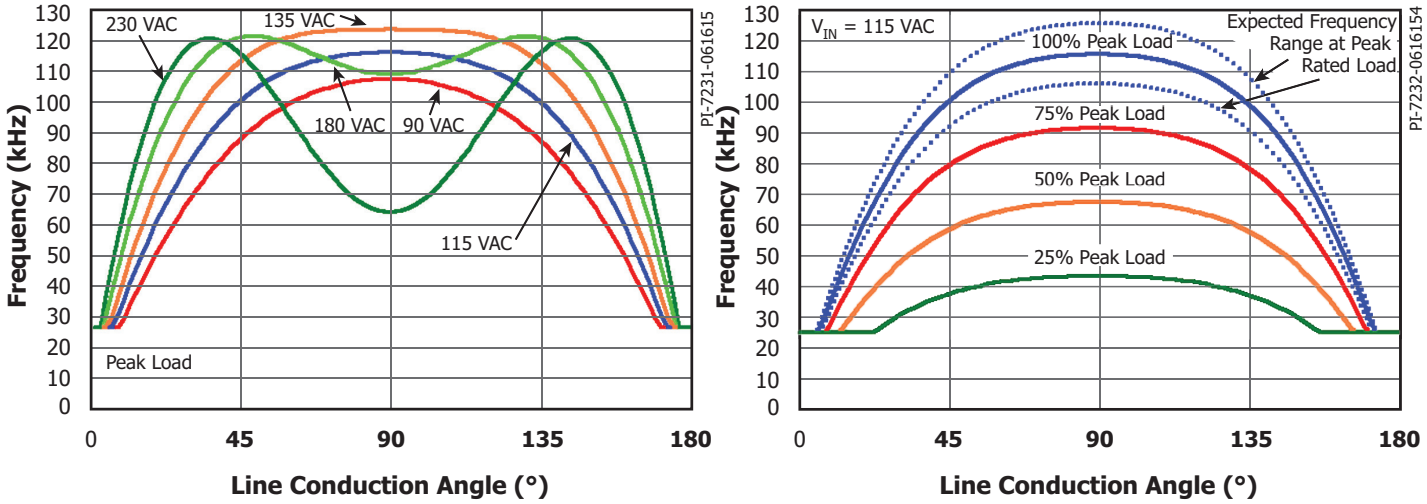


Figure 9. (a) Frequency Variation over Line Half-Cycle as a Function of Input Voltage (b) Frequency Variation over Line Half-Cycle as a Function of Load. Note: Frequency Profiles Shown were Analytically Derived and Reflect CCM Operation Across the Entire Line Cycle.

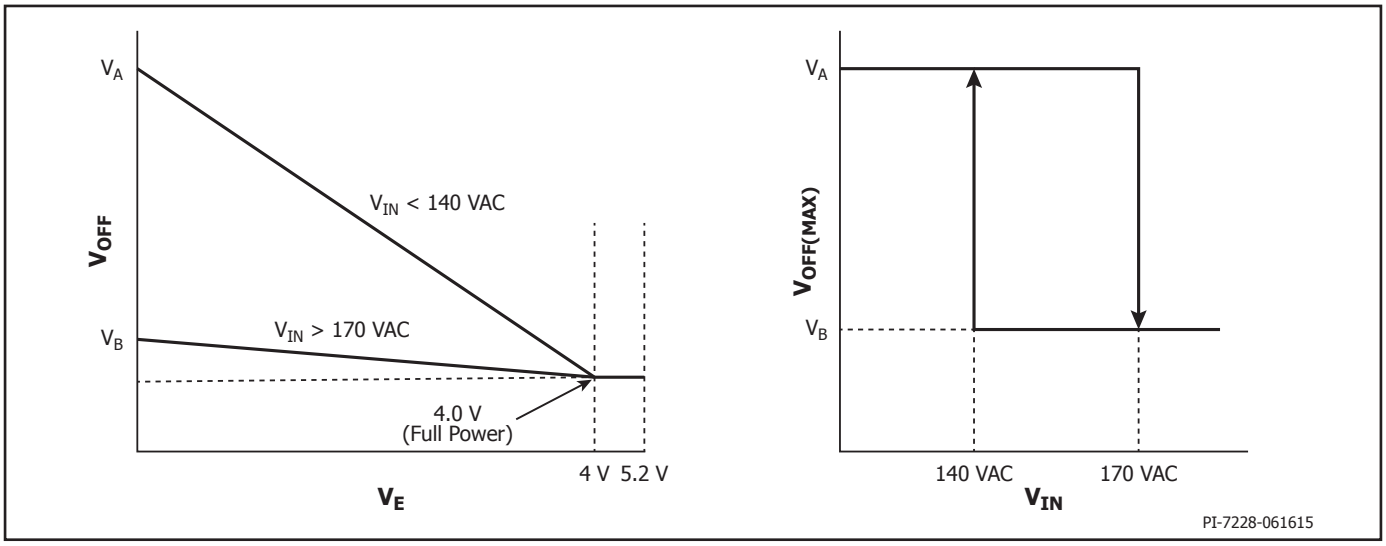


Figure 10. EcoSmart Frequency Slide V_{OFF} vs. V_E and $V_{OFF(MAX)}$ vs. Input Voltage.

The power good comparator has an internal 81 μs de-glitch filter (t_{PGD}) to prevent noise events from falsely triggering the programmed V_{PG-} threshold.

In the event a load fault prevents the boost from achieving regulation (above ~95% of the set output voltage threshold) the PG function will remain in the high-impedance state and will not indicate when an output voltage has fallen below the user programmed V_{PG-} threshold. The V_{PG-} user programmed threshold is enabled once the V_{PG+} threshold has been reached.

If the POWER GOOD THRESHOLD programming pin is tied to REFERENCE pin, the power good function is disabled and PG remains in the high-impedance ('off') state. This is the preferred configuration when PG is not in use. If the POWER GOOD THRESHOLD pin is shorted to the SIGNAL GROUND pin, the PG signal will transition to the 'on' state at V_{PG+} and remain low ('on') until the PFC output voltage has fallen below the V_{FB_UV} threshold for greater than t_{FB_UV} seconds.

Similar to the disable condition described above, if the value of the PGT resistor is such that the V_{PG-} threshold is greater than the V_{PG+} threshold, the PG signal will latch off and remain in the high-impedance off-state.

The Power Good function is not valid under the following conditions:

A. VCC or VREF are not in a valid range of operation. VCC below UVLO- or VREF below REF_{UV-} the power good function is not valid with the POWER GOOD pin in a high-impedance state.
B. Power Good will go to high-impedance state when a soft- shutdown is initiated by an over-temperature fault to provide early indication to secondary circuits of an OT fault.
C. PGT is outside the valid programming range of between 225 V and 360 V. PGT voltages above this range, including PGT floating, will prevent PG from transitioning to active pull-down. PGT voltages below this range result in PG deassertion at the output undervoltage (V_{FB_UV}) threshold.
D. Once the start-up sequence check has passed and the converter goes into start-up, if PGT is opened, then the PG signal will remain latched in the high-impedance state until the controller is reset.

Selectable Power Limit

The capacitor on the REFERENCE pin allows user selection between 'full' and 'efficiency' power limit for each device. The 'efficiency' power mode will permit user selection of a larger device for a given output power requirement for increased conversion efficiency.

In 'full' power mode the REFERENCE pin capacitor is 1.0 μF ±20% and the 'efficiency' power limit mode is selected with a 0.1 μF ±20% capacitor.

If the REFERENCE pin is accidentally shorted to ground, the IC will disable switching and remain disabled until all conditions for the start-up sequence are satisfied.

If the REFERENCE pin is open-circuit, the absence of a bypass capacitor will prevent start-up. During operation, an open-circuit may result in enough REFERENCE pin noise to result in a $VREF\ REF_{UV-}$ shut-down.

Protection Modes

Brown-In Protection (V_{BR+})

The VOLTAGE MONITOR pin features an input line under-voltage detection to limit the minimum start-up voltage. This detection threshold will inhibit the device from starting at input AC voltages below brown-in and above input peak voltages of 400 V_{PK}.

Brown-Out Protection (V_{BR-})

The VOLTAGE MONITOR pin features a brown-out protection mode wherein the HiperPFS-3 will turn-off when the VOLTAGE MONITOR pin voltage is below the line undervoltage threshold (V_{BR-}) for a period exceeding t_{BRWN_OUT} (brown-out debounce period). In the event a single half-line cycle is missing (normal operating line frequency is 47 Hz to 63 Hz) the brown-out detection will not be initiated. Once brown-out has been triggered, the HiperPFS-3 soft-shutdown gradually reduces the internal error-voltage to zero volts over a period of 1 ms to ramp the power MOSFET on-time to zero. The onset of this soft-shutdown is aligned to the next line cycle zero crossing to minimize reactive component di/dt transients and allow time for the energy stored within the boost choke as well as the input EMI filter to dissipate. This helps minimize voltage transients after the bridge rectifier, which helps to prevent false restarts. The device will

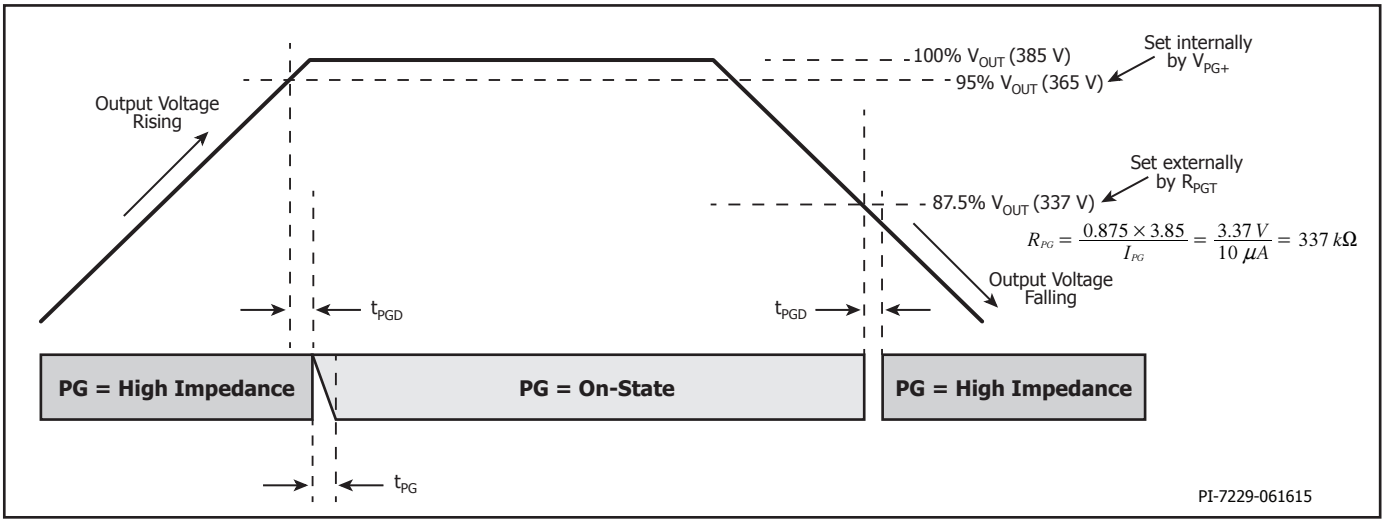


Figure 11. Power Good Function Description.

perform an auto-restart, including FMEA pin fault checks and other start-up qualifications prior to checking for the line voltage being above the brown-in voltage by virtue of the VOLTAGE MONITOR pin being above V_{BR+}.

After a brown-in event, until after the $t_{STARTUP}$ timer has expired, the line voltage brown-out threshold is reduced to V_{BR-NTC} and the brown-out timer is extended to $t_{BRWN_OUT_NTC}$ to allow for the detected drop in line voltage due to an in-rush limiting negative temperature coefficient (NTC) thermistor in series with the input line.

If the $t_{BRWN_OUT_NTC}$ debounce timer is triggered by the sensed line voltage dropping below the V_{BR-NTC} threshold but the line voltage recovers to above the V_{BR-NTC} threshold before the $t_{BRWN_OUT_NTC}$ expires, then the $t_{STARTUP}$ timer will be re-started. If the line does not recover above the V_{BR-NTC} threshold before the $t_{BRWN_OUT_NTC}$ debounce timer expires a shutdown will occur.

After the $t_{STARTUP}$ timer has expired, if the VOLTAGE MONITOR pin voltage is qualified above V_{BR-NTC}, the brown-out debounce timer will switch to normal period (t_{BRWN_OUT}) and the brown-out threshold will switch to V_{BR-}. If the VOLTAGE MONITOR pin voltage is not qualified above V_{BR-} after the subsequent t_{BRWN_OUT} timer has expired then a brown-out shutdown will occur.

HiperPFS-3 incorporates input waveform discrimination to determine if the line signal peak-to-average ratio is more representative of a sinewave or a high duty cycle square wave. The brown-out threshold is reduced to V_{BR_SQ} when a high duty cycle (UPS) square wave is detected.

VCC Undervoltage Protection (UVLO)

The BIAS POWER (VCC) pin has an undervoltage lock-out protection which inhibits the IC from starting unless the applied VCC voltage is above the VCC_{UVLO+} threshold. The IC initiates a start-up once the BIAS POWER pin voltage exceeds the VCC_{UVLO+} threshold. After start-up the IC will continue to operate until the BIAS POWER pin voltage has fallen below the VCC_{UVLO-} level. The absolute maximum voltage of the BIAS POWER pin is 17.5 V which must be externally limited to prevent long term damage to the IC.

Line Dependent Over Current Protection (OCP) limit

The device includes a cycle-by-cycle over-current protection mechanism which protects the device in the event of a fault. The intent of OCP protection in this device is protection of the internal power MOSFET and is not specifically intended to protect the converter from output short-circuit or overload fault conditions.

For universal line input parts, the OCP limit is set as a function of the input line voltage, one setting for low-line voltages and another setting for high-line voltages. This helps to bound power limit into short-circuits as well as helps to minimize the stress on the switch due to current overloads at higher input line conditions. Figure 12 illustrates the hysteretic adjustment of the OCP levels as a function of VOLTAGE MONITOR pin line-sensing. This equates to selecting the low-line OCP (the greater of the two settings) when the peak of the input line voltage drops below 140 VAC for 3 consecutive half-cycles and selecting the high-line OCP level (the lesser of the two settings) when the input line voltage rises above 170 VAC for 1 half-cycle, (except in follower mode, as described in the subsequent sections).

The HiperPFS-3 utilizes a high input line OCP after detecting the VOLTAGE MONITOR pin above the high-line threshold, V_{HIGH+}. The controller reverts back to low-line OCP (as well as low-line frequency slide) only after 3 consecutive half-line cycle peak values that are

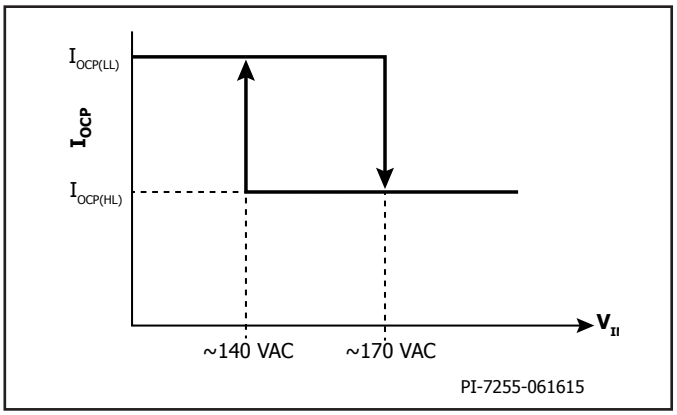


Figure 12. Line Dependent OCP.

below the low-line threshold V_{HIGH-}. In the event of a line drop-out, the controller may revert from high-line to low-line parameters if the drop-out exceeds 37 ms (nominal). High-line only input parts use a single fixed OCP threshold.

A follower-mode feature updates the controller to high-line status rapidly, as soon as the input voltage exceeds V_{HIGH+}. This feature has particular benefit for high-line hard-start conditions after a long AC line drop-out where the peak detector may initially indicate a low input line condition.

A leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time is set so that switch current spikes caused by drain capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction period.

Safe Operating Area (SOA) Mode

Since the cycle-by-cycle OCP mechanism described above does not prevent the possibility of inductor current 'stair-casing', an SOA mode is also featured. Rapid build-up of the switch current can occur in the event of inductor saturation or when the input and output voltage differential is small combined with too little inductor reset time.

The SOA mode is triggered whenever the switch current reaches current limit (I_{OCP}) and the on-time is less than t_{SOA}. The SOA mode forces an off-time equal to $t_{OFF(SOA)}$ and pulls the internal error-voltage (V_E) down by 1/2 of its maximum value in order to ensure the switch remains within its SOA.

Fast Output Voltage Overvoltage Protection (FB_{OV})

The HiperPFS-3 features a voltage feedback threshold comparator on the FEEDBACK pin which detects an output voltage overvoltage condition to allow rapid response, independent of the COMPENSATION pin response, to prevent hazardous voltage conditions from occurring. The overvoltage protection is hysteretic – the voltage on the FEEDBACK pin must drop by 0.1 V (equating to an output voltage drop of 10 V) before switching is re-started.

FEEDBACK to COMPENSATION Pin Short Detection Safeguard

The PFC controller continuously monitors the FEEDBACK and COMPENSATION pins to ensure that there are no potential short conditions between the adjacent FEEDBACK and COMPENSATION pins, which could result in output overvoltage conditions if not detected. In the event a potential short is detected, a rapid short check is performed and a shutdown is executed in the event that a suspected short is validated.

Open FEEDBACK Pin Protection

The FEEDBACK pin continuously sinks a static current of I_{FBPD} [VCC > VCC_{UVLO+}] to protect against a fault related to an open FEEDBACK pin or incomplete feedback divider network. The internal current sink introduces a small static offset to the output regulation which can be accounted for in selecting the output feedback regulation components (FEEDBACK pin divider).

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the controller die temperature which is well coupled to the heat sink through the exposed, grounded pad. The threshold is set at 117 °C typical with a 36 °C hysteresis. When the controller die temperature rises above this threshold (OTP), the controller initiates a soft-shutdown and remains disabled until the controller die temperature falls by ~36 °C, at which point the device will re-initiate the start-up sequence.

The maximum time delay for soft-shutdown to occur after an OTP event is detected is t_{OTP} beyond the next zero-crossing.

HiperPFS-3 Additional Features and Changes

Note: HiperPFS-3 is not a pin for pin drop-in replacement of HiperPFS-2 due to functional changes and optimizations.

- Improved operating supply voltage maximum: 15 V.
- Reduced external component count.
- Improved tolerance of key parameters over a wide temperature range.
- Modified architecture improving noise immunity and operational accuracy.
- Feedback network voltage divider is decoupled from the loop compensation components.
- High-line only family of parts added to HiperPFS-3 family.
- Peak-detector supports deglitch methodology for NTC in-rush current limiting at start-up.
- Digital Power Factor Enhancer algorithm improves high-line light load power factor.
- OTA error amplifier replaces voltage error amplifier of HiperPFS-2.
- NLA implemented via fixed current sources for quick transient response, replaces switched voltage gain in HiperPFS-2.
- Off-time controller senses actual feedback voltage to calculate off-time to prevent inductor saturation.
- VOLTAGE MONITOR pin uses voltage-mode sensing rather than current-mode sensing of HiperPFS-2, allowing flexibility in selection of magnitude of resistor divider.
- Reduced minimum line feed-forward gain supports higher power delivery during line sag events.
- Line feed-forward gain implemented with true squaring function, versus piece-wise linear approximation.
- Line voltage functions performed in the digital domain: peak detection, feed-forward, brown-in/brown-out and PF-enhancement.
- Peak detector incorporates filtering to smooth out cycle-to-cycle variation.
- Optimized brown-in/brown-out thresholds with tighter tolerances.
- Most timers are derived from an internal high-speed clock providing accurate timing.
- eSIP-16 package pinout has been modified for optimal operation and internal grounding.
- No-load/light-load power consumption optimized by re-engineered burst-mode operation.
- Reduced control-engine power consumption: standby current reduced by ~4~5× HiperPFS-2 nominal.
- HiperPFS-3 REFERENCE pin replaces HiperPFS-2 REFERENCE pin; external bypass capacitor replaces external 1% resistor.
- $V_{FB(REF)}$ reduced to 3.85 V nominal from 6.0 V nominal in HiperPFS-2.
- Peak detector optimized across maximum operational conditions when operating with distorted waveforms and line drop-outs.
- Square-wave detector feature for improved UPS operation.
- Power good function is independent of engine during operation except for OTP events.
- FB_{OFF} fault check is always enabled during operation.
- Maximum CCM peak switching frequency has been increased from ~100 kHz to 123 kHz.

Output Power Table

eSIP Package						
Product	**Efficiency Power Mode C_{REF} = 0.1 µF**			**Full Power Mode C_{REF} = 1.0 µF**		
	Maximum Continuous Output Power Rating at 90 VAC[2]		**Peak Output Power Rating at 90 VAC[4]**	**Maximum Continuous Output Power Rating at 90 VAC[2]**		**Peak Output Power Rating at 90 VAC[4]**
	Minimum[3]	Maximum		Minimum[3]	Maximum	
PFS7523L/H	65 W	90 W	100 W	85 W	110 W	120 W
PFS7524L/H	80 W	110 W	125 W	100 W	130 W	150 W
PFS7525L/H	110 W	150 W	170 W	140 W	185 W	205 W
PFS7526H	140 W	190 W	215 W	180 W	230 W	260 W
PFS7527H	175 W	235 W	265 W	220 W	290 W	320 W
PFS7528H	210 W	285 W	320 W	270 W	350 W	385 W
PFS7529H	245 W	335 W	375 W	300 W	405 W	450 W
Product	**Efficiency Power Mode C_{REF} = 0.1 µF**			**Full Power Mode C_{REF} = 1.0 µF**		
	Maximum Continuous Output Power Rating at 180 VAC[2]		**Peak Output Power Rating at 180 VAC[4]**	**Maximum Continuous Output Power Rating at 180 VAC[2]**		**Peak Output Power Rating at 180 VAC[4]**
	Minimum[3]	Maximum		Minimum[3]	Maximum	
PFS7533H	155 W	205 W	230 W	195 W	255 W	280 W
PFS7534H	200 W	260 W	290 W	240 W	315 W	350 W
PFS7535H	275 W	360 W	400 W	335 W	435 W	480 W
PFS7536H	350 W	460 W	510 W	415 W	550 W	610 W
PFS7537H	430 W	560 W	625 W	520 W	675 W	750 W
PFS7538H	520 W	675 W	750 W	625 W	810 W	900 W
PFS7539H	575 W	745 W	830 W	690 W	900 W	1000 W

Table 2. Output Power Table.

Notes:
1. *See Key Application considerations.*
2. *Maximum practical continuous power at 90 VAC in an open-frame design with adequate heat sinking, measured at 50 °C ambient.*
3. *Recommended lower range of maximum continuous power for **best light load efficiency**; HiperPFS-3 will operate and perform below this level.*
4. *Internal output power limit.*

Application Example

A High Efficiency, 275 W, 385 VDC Universal Input PFC

The circuit shown in Figure 13 is designed using a device from the HiperPFS- 3 family of integrated PFC controllers. This design is rated for a continuous output power of 275 W and provides a regulated output voltage of 385 VDC nominal, maintaining a high input power factor and overall efficiency from light load to full load.

Fuse F1 provides protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input voltage. Capacitors C1-C7 together with inductors L2 and L3 form the EMI filter which reduces the common mode and differential mode noise. Resistors R1, R2 and CAPZero, IC U2 are required to discharge the EMI filter capacitors once the circuit is disconnected. CAPZero eliminates static losses in R1 and R2 by only connecting these components across the input when AC is removed.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

The boost converter stage consists of inductor L1, and the Hiper-PFS-3 IC U1. This stage functions as a boost converter and controls the input current of the power supply while simultaneously regulating the output DC voltage. Diode D2 prevents a resonant buildup of output voltage at start-up by bypassing inductor L1 while simultaneously charging output capacitor C17.

Thermistor RT1 limits the inrush input current of the circuit at start-up and prevents saturation of L1. In most high-performance designs, a relay will be used to bypass the thermistor after start-up to improve power supply efficiency. Thermistor RT1 is bypassed by the electro-mechanical relay RL1 after the output voltage is in regulation and a power-good signal from U1 is asserted low. Resistor R3, R4, and Q1 drive relay RL1 and optocoupler U3. Diode D1 clamps the relay coil reverse voltage during de-assertion transitions. Resistor R5 limits the current to the diode in the optocoupler. IC U3 provides optocoupler isolation through connector J2 for a power-good output signal if required.

Capacitor C15 is used for reducing the loop length and area of the output circuit to reduce EMI and overshoot of voltage across the drain and source of the MOSFET inside U1 at each switching edge.

The PFS7527H IC requires a regulated supply of 12 V for operation and must not exceed 15 V. Resistors R6, R7, R8, Zener diode VR1, and transistor Q2 form a series pass regulator that prevents the supply voltage to IC U1 from exceeding 15 V. Capacitors C8, and C9 filter the supply voltage and provide bypassing and decoupling to ensure reliable operation of IC U1. Diode D3 provides reverse polarity protection.

Resistor R15 programs the output voltage level [via the power good threshold (PGT) pin] below which the power good [PG] pin will go into a high-impedance state. Capacitor C14 provides noise immunity on the POWER GOOD THRESHOLD pin.

IC U1 is configured in full power mode by capacitor C10 which is connected to the REFERENCE pin.

The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R10-R13. These resistors values are large to minimize power consumption. Capacitor C11 connected in parallel with the bottom resistor R13 filters noise coupled into the VOLTAGE MONITOR pin.

Output voltage divider network comprising of resistors R16 – R19 are used to scale the output voltage and provide feedback to the IC. Capacitor C16 in parallel with resistor R19 attenuates high frequency noise.

R14, C12 and C13 are required for shaping the loop response of the feedback network.

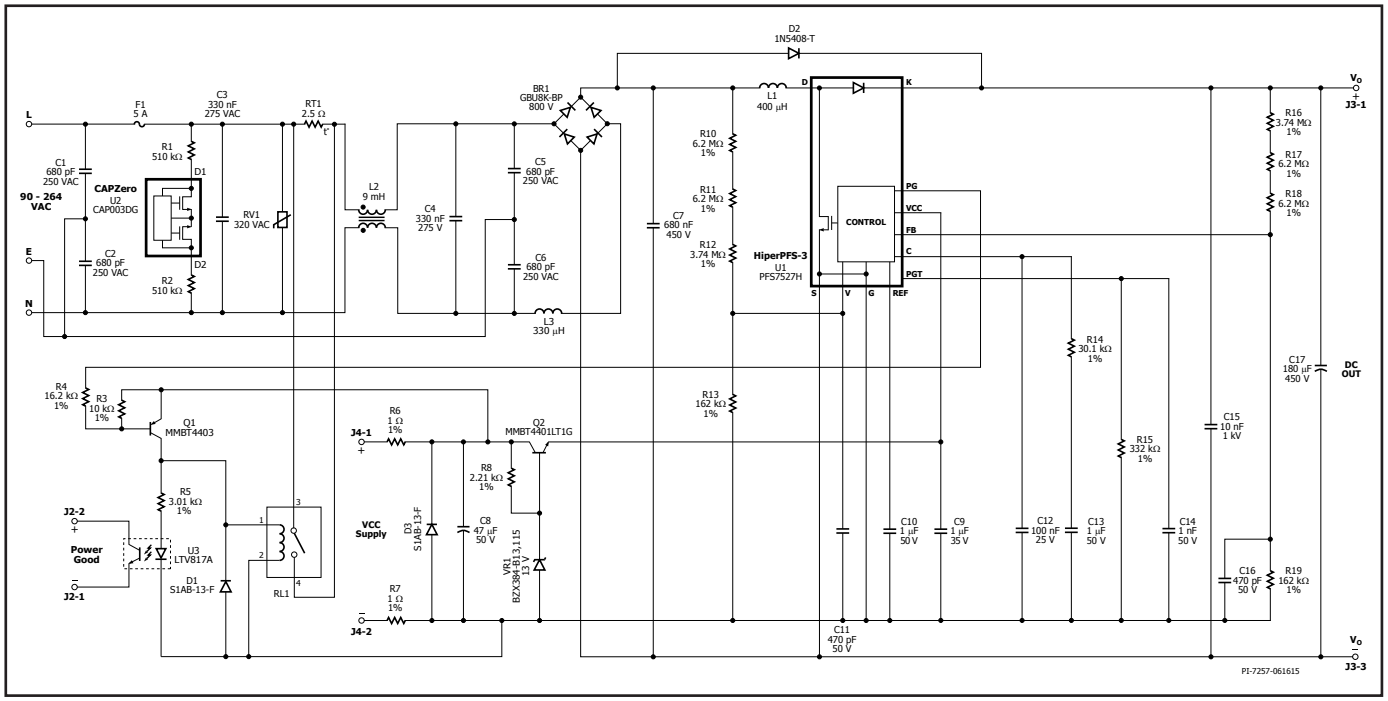


Figure 13. 275 W PFC using PFS7527H.

Design, Assembly, and Layout Considerations

Power Table

The data sheet power table as shown in Table 2 represents the maximum practical continuous output power based on the following conditions:

For the universal input devices (PFS7523L/H – PFS7529H):

1. An input voltage range of 90 VAC to 264 VAC.
2. Overall efficiency of at least 93% at the lowest operating voltage.
3. 385 V nominal output.
4. Sufficient heat sinking to keep device temperature ≤100 ºC.

Operation beyond the limits stated above will require derating. Operation at elevated temperatures could result in reduced MTBF and performance degradation, e.g. reduced efficiency, reduced power limit, PF, and potential of observing hysteretic brown-out, etc., and is not recommended. Use of a nominal output voltage higher than 395 V is not recommended for HiperPFS-3 based designs. Operation at voltages higher than 395 V can result in higher than expected drain-source voltage during line and load transients.

HiperPFS-3 Selection

Selection of the optimum HiperPFS-3 part depends on required maximum output power, PFC efficiency and overall system efficiency (when used with a second stage DC-DC converter), heat sinking constraints, system requirements and cost goals. The HiperPFS-3 part used in a design can be easily replaced with the next higher or lower part in the power table to optimize performance, improve efficiency or for applications where there are thermal design constraints. Minor adjustments to the inductance value and EMI filter components may be necessary in some designs when the next higher or the next lower HiperPFS-3 part is used in an existing design for performance optimization.

Every HiperPFS-3 family part has an optimal load level where it offers the most value. Operating frequency of a part will change depending on load level. Change of frequency will result in change in peak to peak current ripple in the inductance used. Change in current ripple will affect input PF and total harmonic distortion of input current.

Input Fuse and Protection Circuit

The input fuse should be rated for a continuous current above the input current at which the PFC turns-off due to input under- voltage. This voltage is referred to as the brown-out voltage.

The fuse should also have sufficient I^2t rating in order to avoid nuisance failures during start-up. At start-up a large current is drawn from the input as the output capacitor charges to the peak of the applied voltage. The charging current is only limited by any inrush limiting thermistors, impedance of the EMI filter inductors and the forward resistance of the input rectifier diodes. A MOV will typically be required to protect the PFC from line surges. Selection of the MOV rating will depend on the energy level (EN1000-4-5 Class level) which the PFC is required to withstand.

A suitable NTC thermistor should be used on the input side to provide inrush current limiting. Choice of this thermistor should depend on the inrush current specification for the power supply. NTC thermistors may not be placed in any other location in the circuit as they fail to limit the stress on the part in the event of line transients and also fail to limit the inrush current in a predictable manner. The example in Figure 13 shows the circuit configuration that has the inrush limiting NTC thermistor on the input side which is bypassed with a relay after PFC start-up. This arrangement ensures that a consistent inrush limiting performance is achieved by the circuit.

Input EMI Filter

The variable switching frequency of the HiperPFS-3 effectively modulates the switching frequency and reduces conducted EMI peaks associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for the average detection mode used in EMI measurements.

The PFC is a switching converter and will need an EMI filter at the input in order to meet the requirements of most safety agency standards for conducted and radiated EMI. Typically a common mode filter with X capacitors connected across the line will provide the required attenuation of high frequency components of input current to an acceptable level. The leakage reactance of the common mode filter inductor and the X capacitors form a low pass filter. In some designs, additional differential filter inductors may have to be used to supplement the differential mode inductance of the common-mode choke.

A filter capacitor with low ESR and high ripple current capability should be connected at the output of the input bridge rectifier. This capacitor reduces the generation of the switching frequency components of the input current ripple and simplifies EMI filter design. Typically, 0.33 μF per 100 W should be used for universal input designs and 0.15 μF per 100 W of output power should be used for 230 VAC only designs.

It is often possible to use a higher value of capacitance after the bridge rectifier and reduce the X capacitance in the EMI filter.

Regulatory requirements require use of a discharge resistor to be connected across the input X capacitance on the AC side of the bridge rectifier. This is to ensure that residual charge is dissipated after the input voltage is removed when the capacitance is higher than 0.1 μF. Use of CAPZero integrated circuits from Power Integrations, helps eliminate the steady- state losses associated with the use of discharge resistors connected permanently across the X capacitors.

Inductor Design

For ferrite inductors the optimal design has K_p of 0.3 to 0.45. (K_p is defined as the current peak-to-peak value divided by the peak value at minimum AC voltage and 90* phase angle, full load). K_p <0.3 (more continuous) tends towards excessive inductor size, while higher K_p >0.45 tends towards excessive winding AC resistance losses due to large high-frequency AC currents, especially since most ferrite inductor designs will require >3 winding layers. Flux density at maximum current limit should be <3900 gauss to prevent core saturation.

If Sendust core material is used, 90μ or 125μ material is recommended, because the higher μ materials tend to produce greater inductance at lower currents, and thus reduced peak- to-peak inductor currents at lower line phase angles (<45*) which reduces losses and improves PF at lighter loads and higher input voltages. The design target is for H at the peak current (low-line, full-load, 90* line phase angle) to be ~60 A-t/cm. Higher H tends towards excessive core loss, and lower than this increases AC copper losses.

The HiperPFS-3 design spreadsheet simplifies this process and automatically recommends a core size and design for either ferrite or Sendust.

For high performance designs, use of Litz wire is recommended to reduce copper loss due to skin effect and proximity effect. For toroidal inductors the numbers of layers should be less than 3 and for bobbin wound inductors, inter layer insulation should be used to minimize inter layer capacitance.

Output Capacitor

For a 385 V nominal PFC, use of an electrolytic capacitor with 450 V or higher continuous rating is recommended. The capacitance required is dependent on the acceptable level of output ripple and any hold up time requirements. The equations below provide an easy way to determine the required capacitance in order to meet the hold-up time requirement and also to meet the output ripple requirements. The higher of the two values would be required to be used:

calculated using the equation:

$$C_O = \frac{2 \times P_{OUT} \times t_{HOLD_UP}}{V_{OUT}^{\ 2} - V_{OUT(MIN)}^{\ 2}}$$

C_O	PFC output capacitance in F.
P_O	PFC output power in watts.
$t_{HOLD-UP}$	Hold-up time specification for the power supply in seconds.
V_{OUT}	Lowest nominal output voltage of the PFC in volts.
$V_{OUT(MIN)}$	Lowest permissible output voltage of the PFC at the end of hold-up time in volts.

Capacitance required for meeting the low frequency ripple specification is calculated using the equation:

$$C_O = \frac{I_{O(MAX)}}{2 \times \pi \times f_L \times \Delta V_O \times \eta_{PFC}}$$

f_L	Input frequency in Hz.
ΔV_O	Peak-peak output voltage ripple in volts.
η_{PFC}	PFC operating efficiency.
$I_{O(MAX)}$	Maximum output current in amps.

Capacitance calculated using the above method should be appropriately increased to account for ageing and tolerances.

Power Supply for the IC

A 12 V regulated supply should be used for the HiperPFS-3. If the VCC exceeds 15 V, the HiperPFS-3 may be damaged. In most applications a simple series pass linear regulator made using an NPN transistor and Zener diode is adequate since the HiperPFS-3 only requires approximately $I_{CC(ON)}$ maximum for its operation.

It is recommended that a 1 µF or larger, low ESR ceramic capacitor be used to decouple the VCC supply. This capacitor should be placed directly at the IC pin on the circuit board.

Line-Sense Network

The line-sense network connected to the VOLTAGE MONITOR pin provides input voltage information to the HiperPFS-3. A value of 16 MΩ is chosen in this example design to minimize power consumption in these resistors. Only 1% tolerance resistors are recommended.

A decoupling capacitor of 470 pF is required to be connected in parallel with the bottom resistor from the VOLTAGE MONITOR pin to the GROUND pin of the HiperPFS-3. This capacitor should be placed directly at the IC pin on the circuit board.

Feedback Network

A resistor divider network that provides 3.85 V at the FEEDBACK pin at the rated output voltage should be used for optimal performance. It should be scaled in direct proportion to the VOLTAGE MONITOR pin resistor divider network in order to ensure proper regulation and power delivery. The HiperPFS-3 controller has been optimized for operation with an output voltage of 385 VDC. Applications requiring voltages that deviate from this nominal parameter, thereby requiring a FEEDBACK pin divider ratio other than the recommended 100:1, need to be evaluated for trade-offs of the key target parameters of the specific design. E.g.: the VOLTAGE MONITOR pin divider ratio can be modified to be equivalent to that of the feedback divider in order to optimize power factor. However, this will have an impact on power limit, as well as brown-in/brown-out thresholds, etc. Modification of within ±10 V of nominal should not result in dramatically compromised performance, but should be thoroughly verified. Changes in excess of this are not recommended. Itemized trade-offs of this type are outside the scope of this data sheet.

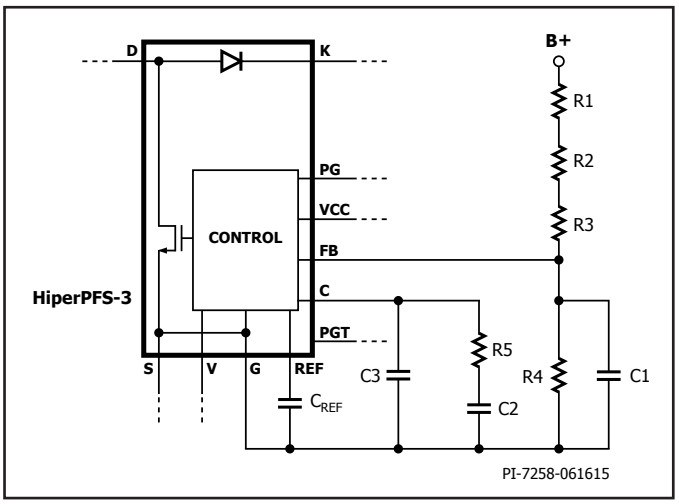


Figure 14. Recommended Feedback Circuit.

The recommended circuit and the associated component values are shown in Figure 14.

Resistors, R1 to R4 comprise of the main output voltage divider network. The sum of resistors R1, R2 and R3 is the upper divider resistor and the lower feedback resistor is R4. Capacitor C1 is to filter any switching noise from coupling into the FEEDBACK pin. Resistor R5, capacitor C2 and C3 is the loop compensation network required to tailor the loop response to ensure low cross-over frequency and sufficient phase margin. The recommended values for the components used are as follows:

R1 = 3.74 MΩ
R2 = 6.2 MΩ
R3 = 6.2 MΩ
R5 = 30.1 kΩ
C1 = 470 pF
C2 = 1 µF
C3 = 100 nF

When the above component values are used, the value of resistor R4 can be calculated using the equation below:

$$R_4 = \frac{(R_1 + R_2 + R_3)}{\left(\frac{V_O}{V_{FB(REF)}} - 1\right)}$$

V_O	Output voltage.
$V_{FB(REF)}$	FEEDBACK pin voltage, 3.85 V.

The value of resistor R5 will have to be adjusted in some designs and as a guideline the value from the following calculation can be used:

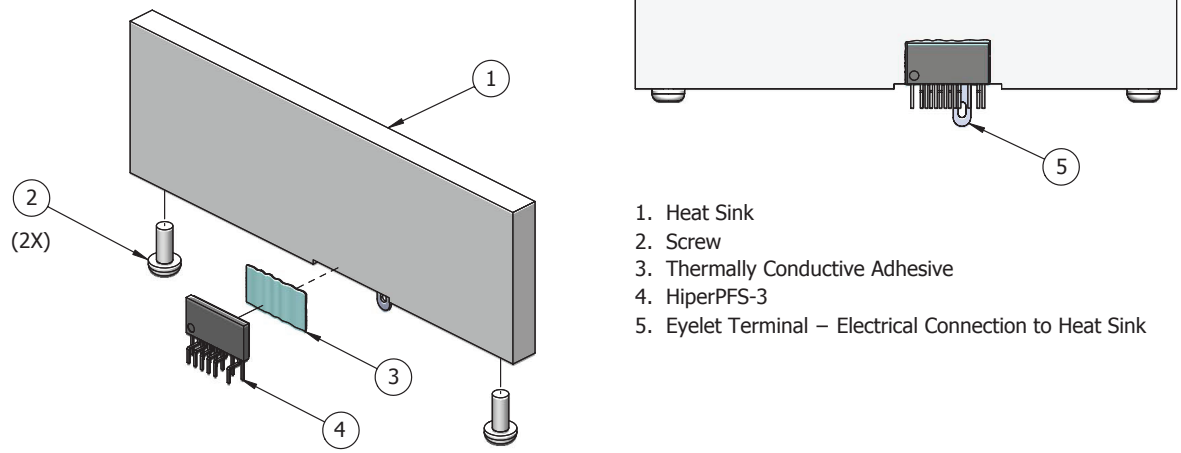
$$R_5 = R_Z = \frac{P_O}{0.3 \times V_O^2 \times C_O}(k\Omega)$$

P_O Maximum continuous output power in watts.
V_O Nominal PFC output voltage in volts.
C_O PFC output capacitance in farads.

Heat Sinking and Thermal Design

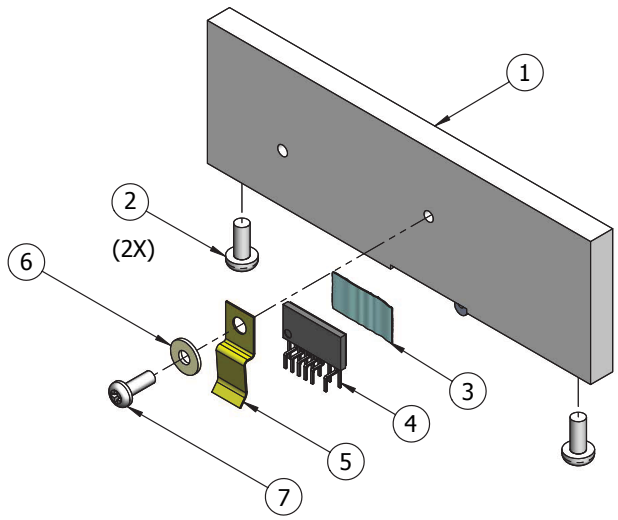
Figures 15, 16, 17 show an example of the recommended assembly for the HiperPFS-3. In this assembly, no insulation pad is required and HiperPFS-3 can be directly connected to the heat sink by mechanical clip or adhesive thermal compound.

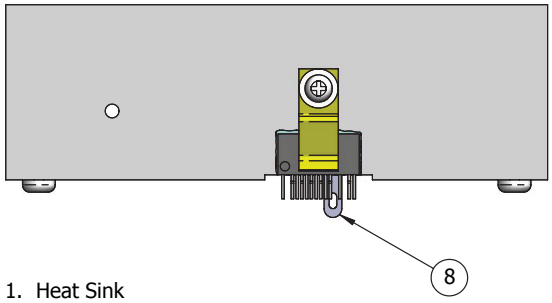
The HiperPFS-3 back metal is electrically connected to the heat sink and the heat sink is required to be connected to the HiperPFS-3 source terminal in order to reduce EMI.



1. Heat Sink
2. Screw
3. Thermally Conductive Adhesive
4. HiperPFS-3
5. Eyelet Terminal – Electrical Connection to Heat Sink

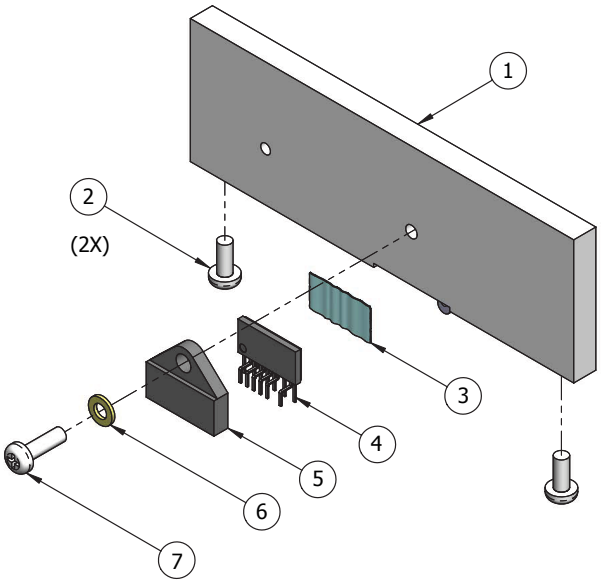
Figure 15. Heat Sink Assembly – using Thermally Conductive Adhesive.

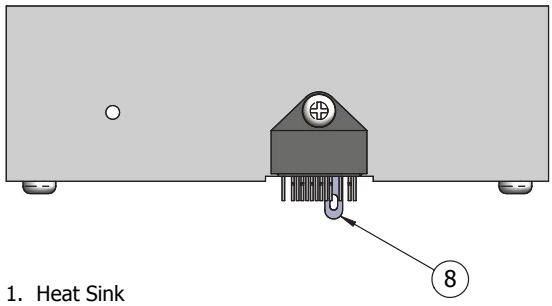




1. Heat Sink
2. Screw
3. Thermally Conductive Silicone Grease
4. HiperPFS-3
5. Metal Clip
6. Washer
7. Screw
8. Eyelet Terminal – Electrical Connection to Heat Sink

Figure 16. Heat Sink Assembly – with Metal Clip.





1. Heat Sink
2. Screw
3. Thermally Conductive Silicone Grease
4. HiperPFS-3
5. Plastic Clip
6. Washer
7. Screw
8. Eyelet Terminal – Electrical Connection to Heat Sink

Figure 17. Heat Sink Assembly – with Plastic Clip.

PCB Design Guidelines and Design Example

The line-sense network and the feedback circuit use large resistance values in order to minimize power dissipation in the feedback network and the line-sense network. Care should be taken to place the feedback circuit and the line-sense network components away from the high-voltage and high current nodes to minimize any interference. Any noise injected in the feedback network or the line-sense network will typically manifest as degradation of power factor. Excessive noise injection can lead to waveform instability or dissymmetry.

The EMI filter components should be clustered together to improve filter effectiveness. The placement of the EMI filter components on the circuit board should be such that the input circuit is located away from the drain node of the PFC inductor.

A filter or decoupling capacitor should be placed at the output of the bridge rectifier. This capacitor together with the X capacitance in the EMI filter and the differential inductance of the EMI filter section and the source impedance, works as a filter to reduce the switching frequency current ripple in the input current. This capacitor also helps to minimize the loop area of the switching frequency current loop thereby reducing EMI.

The connection between the HiperPFS-3 drain node, output diode drain terminal and the PFC inductor should be kept as short as possible.

A low loss ceramic dielectric capacitor should be connected between the cathode of the PFC output diode and the source terminal of the HiperPFS-3. This ensures that the loop area of the loop carrying high frequency currents at the transition of the MOSFET and helps to reduce radiated EMI due to the high frequency pulsating nature of the diode current traversing through the loop.

During placement of components on the board, it is best to place the voltage monitor, feedback, reference and bias power decoupling capacitors as close as possible to the pins before the other components are placed and routed. REFERENCE pin decoupling capacitor needs to have dedicated return path to GROUND pin. Failing to do so could reduce the noise immunity during surge and ESD test. Power supply return trace from the GROUND pin should be separate from the trace connecting the feedback circuit components to the GROUND pin.

To minimize the effects of trace impedance on regulation, output feedback should be taken directly from the output capacitor positive terminal. The upper end of the line-sense resistors should be connected to the high frequency filter capacitor connected at the output of the bridge rectifier.

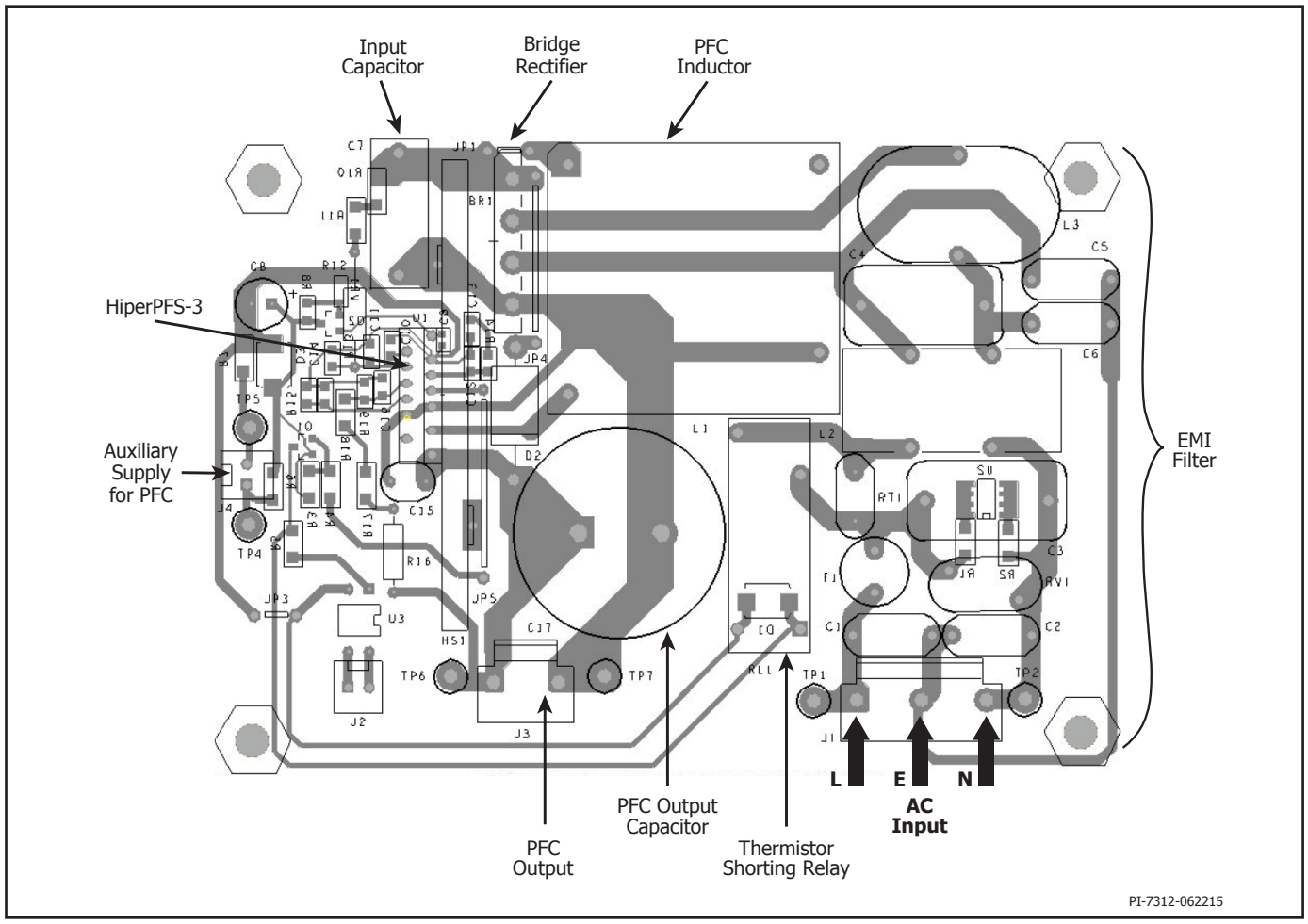


Figure 18. PCB Layout Example.

Quick Design Checklist

As with any power supply design, all HiperPFS-3 designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak VDS does not exceed 530 V at lowest input voltage and maximum overload output power. Maximum overload output power occurs when the output is overloaded to a level just above the highest rated load or before the power supply output voltage starts falling out of regulation. Additional external snubbers should be used if this voltage is exceeded. In most designs, addition of a ceramic capacitor in the range of 33 pF and 100 pF connected across the PFC output diode will reduce the maximum drain-source voltage to a level below the BV_{DSS} rating. When measuring drain-source voltage of the MOSFET, a high-voltage probe should be used. When the probe tip is removed, a silver ring in the vicinity of the probe tip can be seen. This ring is at ground potential and the best ground connection point for making noise free measurements. Wrapping stiff wire around the ground ring and then connecting that ground wire into the circuit with the shortest possible wire length, and connecting the probe tip to the point being measured, ensures error free measurement. Probe should be compensated according to probe manufacturer's guidelines to ensure error-free measurement.
2. Maximum drain current – Drain current can be measured indirectly by monitoring inductor current. A current probe should be inserted between the bridge rectifier and inductor connection. At maximum ambient temperature, minimum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of inductor saturation. When performing this measurement with Sendust inductor, it is typical to see inductor wave-forms that show exponential increase in current due to permeability drop. This should not be confused with hard saturation.
3. Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for the HiperPFS-3, PFC inductor, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of HiperPFS-3, as specified in the data sheet. A maximum package temperature of 100 °C is recommended to allow for these variations.
4. Input PF should improve with load, if performance is found to progressively deteriorate with loading, it is a sign of possible noise pick-up by the VOLTAGE MONITOR pin circuit or the feedback divider network and the compensation circuit.

Absolute Maximum Ratings[1,2]

DRAIN Pin Peak Current: PFS7523/PFS7533 .....7.5 A
PFS7524/PFS7534 ..... 9.0 A
PFS7525/PFS7535 .....11.3 A
PFS7526/PFS7536 .....13.5 A
PFS7527/PFS7537.....15.8 A
PFS7528/PFS7538 .....18.0 A
PFS7529/PFS7539 .....21.0 A
DRAIN Pin Voltage ..... -0.3 V to 530 V / 540 V[6]
VCC[3] Pin Voltage ..... -0.3 V to 17.5 V
PG ..... -0.3 V to 17.5 V
PG Pin Current.....10 mA
V, PGT, FB, C, REF Pin Voltage .....-0.3 V to 5.6 V
Storage Temperature .....-65 °C to 150 °C
Junction Temperature[4].....-40 °C to 150 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. The absolute maximum rating of the VCC is 17.5 V. This is an absolute maximum condition that must not be exceeded. Voltages between the max operating voltage (15 V) and this abs max rating should be very infrequent and short in duration (e.g. at start-up or temporary fault conditions). It is not intended as a guarantee of the reliability of the product up to the absolute maximum rating, but is a guideline as to the level of applied voltage above which there is a risk of immediate damage to the product.
4. Normally limited by internal circuitry. Applies to Controller $T_{J(C)}$, MOSFET $T_{J(M)}$ and Diode Junction Temperature $T_{J(D)}$.
5. 1/16" from case for 5 seconds.
6. Duration less than 15 ns and $I_{DS} \leq I_{OCP(TYP)}$.
7. $T_{C(D)}$ diode case temperature.

Qspeed Diode

		PFS7523-7529 PFS7533-7535	PFS7536-7539
Peak Repetitive Reverse Voltage (VRRM)		530 V	530 V
Average Forward Current IF(AV)	$T_{J(D)}$ = 150 °C	3 A	6 A
Non-Repetitive Peak Surge Current (IFSM)	60 Hz, ½ cycle, $T_{C(D)}$[7] = 25 °C	50 A	100 A
Non-Repetitive Peak Surge Current (IFSM)	t = 500 µs, $T_{C(D)}$[7] = 25 °C	130 A	260 A

Thermal Resistance

Thermal Resistance: H/L Package:
(θ_{JA})[1] ..... 103 °C/W
(θ_{JC}) .....(see Figure 21)

Notes:
1. Controller junction temperature ($T_{J(C)}$) may be less than the MOSFET Junction Temperature ($T_{J(M)}$) and Diode Junction Temperature ($T_{J(D)}$).

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)	Pin	Min	Typ	Max	Units
Currents							
Undervoltage Current Consumption After Power-Up of Core and Zeners	$I_{CC(UVLO)}$	VCC < UVLO+(min) V = 1 V, C = 0 V, FB = 3.85 V 0 °C < $T_{J(C)}$ < 100 °C	VCC		140		µA
Standby Current Consumption – No Switching Prior to Brown-In	$I_{CC(STBY)}$	V = 1 V, C = 0 V, FB = 3.85 V 0 °C < $T_{J(C)}$ < 100 °C	VCC		320		µA
Current Consumption – in Burst Mode, No Switching	$I_{CC(BURST)}$	FB = 3.85 V, C < V_{ERR_MIN}, V = 1.414 V (or 2.828 V for High-Line Only Parts) 0 °C < $T_{J(C)}$ < 100 °C	VCC		395	470	µA

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Currents (cont.)							
Operating Current	$I_{CC(ON)}$	No-load on REF Switching at F_{MIN} (T_{OFF} = $T_{OFF(MIN)}$, T_{ON} = $T_{ON(MAX)}$) 0 °C < $T_{J(C)}$ < 100 °C	PFS7523 PFS7533	0.64	0.75	0.90	mA
			PFS7524 PFS7534	0.67	0.79	0.95	
			PFS7525 PFS7535	0.74	0.88	1.05	
			PFS7526 PFS7536	0.79	0.93	1.12	
			PFS7527 PFS7537	0.85	1.00	1.20	
			PFS7528 PFS7538	0.91	1.07	1.28	
			PFS7529 PFS7539	0.98	1.15	1.38	
Leakage Current in UVLO State	I_{oz}	0 < Pin Voltage < REF 0 °C < $T_{J(C)}$ < 100 °C	V, FB, C, PGT		±10		nA
		V_{PG} = 12 V	PG		±0.1		µA
Pull-Down Current on Feedback	$I_{FB(PD)}$	Not Active When VCC < UVLO+ 0 °C < $T_{J(C)}$ < 100 °C	FB		100		nA
Pull-Down Current on Voltage	$I_{V(PD)}$	Not Active When VCC < UVLO+ 0 °C < $T_{J(C)}$ < 100 °C	V		100		nA
On-Time Controller							
Maximum Operating "On"-Time	$t_{ON(MAX)}$	0 °C < $T_{J(C)}$ < 100 °C		29	34	40	µs
Off-Time Controller							
Maximum Operating "Off"-Time	$t_{OFF(MAX)}$	0 °C < $T_{J(C)}$ < 100 °C		36	43	48	µs
Off-Time Accuracy	$t_{OFF(ACCURACY)}$	0 °C < $T_{J(C)}$ < 100 °C V = 1.414 V (or 2.828 V for High-Line Only) FB = 3.85 V C > = 4 V			±4.0		%
Feedback							
Feedback Voltage Reference	$V_{FB(REF)}$	$T_{J(C)}$ = 25 °C		3.82	3.85	3.88	V
		0 °C < $T_{J(C)}$ < 100 °C		3.75	3.85	3.95	
Feedback Error-Amplifier Transconductance Gain	G_M	3.75 V < V_{FB} < 3.95 V V_C = 4 V 0 °C < $T_{J(C)}$ < 100 °C		75	95	105	µA/V
Soft-Shutdown Time	$t_{SHUTDWN}$	See Note A		0.86	1.00	1.16	ms
FEEDBACK Pin Start-Up/Fault Threshold	$V_{FB(OFF)}$	0 °C < $T_{J(C)}$ < 100 °C		0.57	0.64	0.71	V

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)	Min	Typ	Max	Units
Feedback (cont.)						
FEEDBACK Pin Undervoltage Assertion Threshold	$V_{FB(UV)}$	0 °C < $T_{J(C)}$ < 100 °C	2.09	2.25	2.36	V
FEEDBACK Pin Overvoltage Assertion Threshold	$V_{FB(OV+)}$	0 °C < $T_{J(C)}$ < 100 °C	4.00	4.10	4.20	V
FEEDBACK Pin Overvoltage Assertion Relative Threshold	$V_{FB(OV+REL_FB)}$	0 °C < $T_{J(C)}$ < 100 °C	V_{FBREF} +0.19	V_{FBREF} +0.245	V_{FBREF} +0.30	
FEEDBACK Pin Overvoltage Deassertion Threshold	$V_{FB(OV-)}$	0 °C < $T_{J(C)}$ < 100 °C	3.90	4.00	4.10	V
FEEDBACK Pin Overvoltage Deassertion Relative Threshold	$V_{FB(OV-REL_FB)}$	0 °C < $T_{J(C)}$ < 100 °C	V_{FBREF} +0.11	V_{FBREF} +0.16	V_{FBREF} +0.21	
FEEDBACK Pin Overvoltage Hysteresis	$V_{FB(OVHYST)}$	0 °C < $T_{J(C)}$ < 100 °C	0.070	0.085	0.115	V
COMPENSATION Pin PF Enhancer Disable Threshold	$V_{LOW(LOAD+)}$	See Note A		1.1		V
COMPENSATION Pin PF Enhancer Enable Threshold	$V_{LOW(LOAD-)}$	See Note A		1.0		V
COMPENSATION Pin PF Enhancer Threshold Hysteresis	$V_{LOW(LOAD_HYST)}$	See Note A		0.1		V
COMPENSATION Pin Burst Disable Threshold	$V_{ERR(MIN+)}$	0 °C < $T_{J(C)}$ < 100 °C		0.19		V
COMPENSATION pin Burst Enable Threshold	$V_{ERR(MIN-)}$	0 °C < $T_{J(C)}$ < 100 °C		0.1		V
COMPENSATION Pin Burst Threshold Hysteresis	$V_{ERR(HYST)}$	0 °C < $T_{J(C)}$ < 100 °C		0.09		V
Line-Sense/Peak Detector						
Line-Sense Input Voltage Range	$V_{V(RANGE)}$	See Note A	0		4	V
Brown-In Threshold Voltage	V_{BR+}	Universal Input Devices (PFS7523-PFS7529) 0 °C < $T_{J(C)}$ < 100 °C	1.08	1.12	1.16	V
		High-Line Only Input Devices (PFS7533-PFS7539) 0 °C < $T_{J(C)}$ < 100 °C	2.30	2.35	2.42	

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)		Min	Typ	Max	Units
Line-Sense/Peak Detector (cont.)							
Brown-Out Threshold Voltage	V_{BR-}	Universal Input Devices (PFS7523-PFS7529) 0 °C < $T_{J(C)}$ < 100 °C		0.93	0.97	1.02	V
		High-Line Only Input Devices (PFS7533-PFS7539) 0 °C < $T_{J(C)}$ < 100 °C		2.15	2.21	2.27	
Brown-In/Out Hysteresis (After NTC Warm-Up Time)	$V_{BR(HYS)}$	0 °C < $T_{J(C)}$ < 100 °C		0.13	0.145	0.160	V
Brown-Out Threshold for High Duty Cycle Square Wave	$V_{BR(SQ)}$	Universal Input Devices (PFS7523-PFS7529)			0.86		V
		High-Line Only Input Devices (PFS7533-PFS7539)			1.93		
Start-Up Brown-Out Threshold Voltage (During NTC Warm-Up Time)	$V_{BR(NTC)}$	Universal Input Devices (PFS7523-PFS7529)			0.74		V
		High-Line Only Input Devices (PFS7533-PFS7539)			1.57		
Brown-Out NTC Debounce Timer	$t_{BRWNOUT(NTC)}$	See Note A		875	1000	1160	ms
Brown-Out Debounce Timer	$t_{BRWNOUT}$	See Note A		43	54	66	ms
Start-Up Timer for Using Lower brown-Out Threshold (V_{BR-NTC})	$t_{STARTUP}$	See Note A		875	1000	1160	ms
VOLTAGE Pin High-Line Assertion Threshold	$V_{V(HIGH+)}$	See Note A			2.42		V
VOLTAGE Pin High-Line Deassertion Threshold	$V_{V(HIGH-)}$	See Note A			2.00		V
VOLTAGE Pin Minimum Asserted Peak Value	$V_{PK(MIN)}$	See Note A			0.71		V
Current Limit/Circuit Protection							
Over-Current Protection		PFS7523L/H di/dt = 250 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	3.8	4.1	4.3	A
			V_V > 2.42 V	2.6	2.8	3.0	
		PFS7524L/H di/dt = 300 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	4.5	4.8	5.1	
			V_V > 2.42 V	3.0	3.3	3.5	

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specfied)		Min	Typ	Max	Units
Current Limit/Circuit Protection (cont.)							
Over-Current Protection	I_{OCP}	PFS7525L/H di/dt = 400 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	5.5	5.9	6.2	A
			V_V > 2.42 V	3.6	4.0	4.4	
		PFS7526H di/dt = 500 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	6.8	7.2	7.5	
			V_V > 2.42 V	4.6	4.9	5.25	
		PFS7527H di/dt = 650 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	8.0	8.4	8.8	
			V_V > 2.42 V	5.35	5.8	6.2	
		PFS7528H di/dt = 800 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	9.0	9.5	9.9	
			V_V > 2.42 V	6.0	6.5	7.1	
		PFS7529H di/dt = 920 mA/µs $T_{J(C)}$ = 25 °C	V_V < 2 V	10	10.5	11	
			V_V > 2.42 V	6.7	7.2	7.7	
		PFS7533H di/dt = 250 mA/µs $T_{J(C)}$ = 25 °C		3.8	4.1	4.3	
		PFS7534H di/dt = 300 mA/µs $T_{J(C)}$ = 25 °C		4.5	4.8	5.1	
		PFS7535H di/dt = 400 mA/µs $T_{J(C)}$ = 25 °C		5.5	5.9	6.2	
		PFS7536H di/dt = 500 mA/µs $T_{J(C)}$ = 25 °C		6.8	7.2	7.5	
		PFS7537H di/dt = 650 mA/µs $T_{J(C)}$ = 25 °C		8.0	8.4	8.8	
		PFS7538H di/dt = 800 mA/µs $T_{J(C)}$ = 25 °C		9.0	9.5	9.9	
		PFS7539H di/dt = 920 mA/µs $T_{J(C)}$ = 25 °C		10	10.5	11	

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)	Min	Typ	Max	Units
Current Limit/Circuit Protection (cont.)						
Normalized Frequency at Power Limit	F_{LIM}	C_{REF} = 1.0 µF $T_{J(C)}$ = 25 °C		±7		%
		0 °C < $T_{J(C)}$ < 100 °C		±10		
SOA Protection Fixed Off-Time	$t_{OFF(SOA)}$	$T_{J(C)}$ = 25 °C	200	250	300	µs
Leading Edge Blanking (LEB) Time Period	t_{LEB}	$T_{J(C)}$ = 25 °C See Note A		220		ns
Minimum On-Time in IOCP	$t_{ON_OCP(MIN)}$	$T_{J(C)}$ = 25 °C		400		ns
VCC Auxiliary Power Supply						
VCC Operating Range	VCC		UVLO+	12	15	V
Start-Up VCC (Rising Edge)	$VCC_{UV(LO+)}$	0 °C < $T_{J(C)}$ < 100 °C	9.6	9.85	10.1	V
Shutdown VCC (Falling Edge)	$VCC_{UV(LO-)}$	0 °C < $T_{J(C)}$ < 100 °C	9.05	9.3	9.55	V
VCC Hysteresis	$VCC_{(HYS)}$	0 °C < $T_{J(C)}$ < 100 °C	0.50	0.57	0.65	V
UVLO Shutdown Delay Timer	$t_{UV(LO-)}$	See Note A		500		ns
Time From VCC > VCC_{UVLO+} Until Device Commences Switching	t_{RESET}	V > V_{BR+} See Note A		60	75	ms
Series Regulator						
REFERENCE Pin Voltage	V_{REF}	0 °C < $T_{J(C)}$ < 100 °C	4.95	5.25	5.45	V
REFERENCE Pin Required Capacitance	C_{REF}	Full Power Mode	0.8	1.0		µF
		Efficiency Mode	0.08	0.1	0.2	
REFERENCE Pin UVLO Rising Edge	REF_{UV+}	0 °C < $T_{J(C)}$ < 100 °C See Note A			5.0	V
REFERENCE Pin UVLO Falling Edge	REF_{UV-}	0 °C < $T_{J(C)}$ < 100 °C See Note A	4.4			V
Power Good						
Power Good Deassertion Threshold Output Reference Current	$I_{PG(T)}$	0 °C < $T_{J(C)}$ < 100 °C; V_{PGT} = 3.0 V	-10.65	-10	-9.35	µA
Power Good Delay Time (From FB > V_{PG+} to PG < 1 V)	t_{PG}	0 °C < $T_{J(C)}$ < 100 °C; PG = 20 kΩ Pull-Up to VCC, See Note A		<15		µs
Power Good Deglitch Time	$t_{PG(D)}$	See Note A	57	81	108	µs

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)			Min	Typ	Max	Units
Power Good (cont.)								
Power Good Internal Assertion Threshold	$V_{PG(+)}$	0 °C < $T_{J(C)}$ < 100 °C			3.55	3.65	3.75	V
Power Good Relative Threshold	$V_{PG+REL(FB)}$	0 °C < $T_{J(C)}$ < 100 °C			V_{FBREF} -0.24	V_{FBREF} -0.20	V_{FBREF} -0.16	
Power Good Deassertion Threshold	$V_{PG(-)}$	V (PGT) = 3 V 0 °C < $T_{J(C)}$ < 100 °C			2.94	V (PGT) ±30 mV	3.06	V
POWER GOOD Pin Leakage Current in Off-State	$IOZH_{PG}$	FB < V_{PG-} 0 °C < $T_{J(C)}$ < 100 °C					500	nA
POWER GOOD Pin On-State Voltage	VOL_{PG}	0 °C < $T_{J(C)}$ < 100 °C I_{PG} = 2.0 mA; FB = 3.85 V					2	V
Thermal Protection (OTP)								
Controller Junction Temperature ($T_{J(C)}$) for Shutdown	T_{OTP+}	See Note A				117		°C
Controller Junction Temperature ($T_{J(C)}$) for Restart	T_{OTP-}	See Note A				81		°C
Over-Temperature Hysteresis	$T_{OTP(HYST)}$	V > V_{BR+} See Note A				36		°C
VTS MOSFET								
On-State Resistance	$R_{DS(ON)}$	I_D = 0.5 × I_{OCP}	PFS7523 PFS7533	$T_{J(M)}$ = 25 °C		0.61	0.76	Ω
				$T_{J(M)}$ =100 °C			1.10	
			PFS7524 PFS7534	$T_{J(M)}$ = 25 °C		0.51	0.63	
				$T_{J(M)}$ = 100 °C			0.92	
			PFS7525 PFS7535	$T_{J(M)}$ = 25 °C		0.41	0.51	
				$T_{J(M)}$ = 100 °C			0.73	
			PFS7526 PFS7536	$T_{J(M)}$ = 25 °C		0.34	0.42	
				$T_{J(M)}$ = 100 °C			0.62	
			PFS7527 PFS7537	$T_{J(M)}$ = 25 °C		0.30	0.36	
				$T_{J(M)}$ = 100 °C			0.52	
			PFS7528 PFS7538	$T_{J(M)}$ = 25 °C		0.26	0.32	
				$T_{J(M)}$ = 100 °C			0.46	
			PFS7529 PFS7539	$T_{J(M)}$ = 25 °C		0.22	0.27	
				$T_{J(M)}$= 100 °C			0.40	

Parameter	Symbol	Conditions SOURCE = 0 V; V_{CC} = 12 V, -40 °C < $T_{J(C)}$ < 125 °C (Note C) (Unless Otherwise Specified)			Min	Typ	Max	Units
VTS MOSFET								
Effective Output Capacitance	C_{oss}	$T_{J(M)}$ = 25 °C V_{GS} = 0 V, V_{DS} = 0 to 80% BV_{DSS} See Note A	PFS7523 PFS7533				176	pF
			PFS7524 PFS7534				210	
			PFS7525 PFS7535				265	
			PFS7526 PFS7536				312	
			PFS7527 PFS7537				369	
			PFS7528 PFS7538				420	
			PFS7529 PFS7539				487	
Breakdown Voltage	BV_{DSS}	$T_{J(M)}$ = 25 °C, VCC = 12 V I_D = 250 µA, V_{FB}= V_V = 0 V			530			V
Breakdown Voltage Temperature Coefficient	$BV_{DSS(TC)}$	See Note A				0.048		%/°C
Off-State Drain Current Leakage	I_{DSS}	V_{DS} = 80% BV_{DSS} VCC = 12 V V_{FB} = V_V = V_C = 0	PFS7523 PFS7533	$T_{J(M)}$ =100 °C			80	µA
			PFS7524 PFS7534	$T_{J(M)}$ =100 °C			100	
			PFS7525 PFS7535	$T_{J(M)}$ =100 °C			120	
			PFS7526 PFS7536	$T_{J(M)}$ =100 °C			150	
			PFS7527 PFS7537	$T_{J(M)}$ =100 °C			170	
			PFS7528 PFS7538	$T_{J(M)}$ =100 °C			200	
			PFS7529 PFS7539	$T_{J(M)}$ =100 °C			235	
Turn-Off Voltage Rise Time	t_R	See Notes A, B, C				50		ns
Turn-On Voltage Fall Time	t_F	See Notes A, B, C				100		ns

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Qspeed Diode (3A) PFS7523-7529/7533-7535							
DC Characteristics							
Reverse Current	I_R	V_R = 530 V	$T_{J(D)}$ = 25 °C		0.4		µA
			$T_{J(D)}$ = 100 °C		0.07		mA
Forward Voltage	V_F	I_F = 3 A	$T_{J(D)}$ = 25 °C		1.55		V
			$T_{J(D)}$ = 100 °C		1.47		
Junction Capacitance	C_J	V_R = 10 V, 1 MHz			18		pF
Dynamic Characteristics (Note: See Figures 19, 20 for dynamic characteristic definition)							
Reverse Recovery Time	t_{RR}	di/dt = 200 A/µs, V_R = 400 V I_F = 3 A	$T_{J(D)}$ = 25 °C		26.5		ns
			$T_{J(D)}$ = 100 °C		32		
Reverse Recovery Charge	Q_{RR}	di/dt = 200 A/µs, V_R = 400 V I_F = 3 A	$T_{J(D)}$ = 25 °C		40.6		nC
			$T_{J(D)}$ = 100 °C		65.7		
Maximum Reverse Recovery Current	I_{RRM}	di/dt = 200 A/µs, V_R = 400 V I_F = 3 A	$T_{J(D)}$ = 25 °C		2.1		A
			$T_{J(D)}$ = 100 °C		3.0		
Softness Factor = t_B/t_A	S	di/dt = 200 A/µs, V_R = 400 V I_F = 3 A	$T_{J(D)}$ = 25 °C		1		
			$T_{J(D)}$ = 100 °C		0.45		

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Qspeed Diode (6A) PFS7536-7539							
DC Characteristics							
Reverse Current	I_R	V_R = 530 V	$T_{J(D)}$ = 25 °C		0.8		µA
			$T_{J(D)}$ = 100 °C		0.15		mA
Forward Voltage	V_F	I_F = 6 A	$T_{J(D)}$ = 25 °C		1.51		V
			$T_{J(D)}$ = 100 °C		1.44		
Junction Capacitance	C_J	V_R = 10 V, 1 MHz			41		pF
Dynamic Characteristics (Note: See Figures 19, 20 for dynamic characteristic definition)							
Reverse Recovery Time	t_{RR}	di/dt = 200 A/µs, V_R = 400 V I_F = 6 A	$T_{J(D)}$ = 25 °C		28.5		ns
			$T_{J(D)}$ = 100 °C		37.3		
Reverse Recovery Charge	Q_{RR}	di/dt = 200 A/µs, V_R = 400 V I_F = 6 A	$T_{J(D)}$ = 25 °C		58		nC
			$T_{J(D)}$ = 100 °C		105.5		
Maximum Reverse Recovery Current	I_{RRM}	di/dt = 200 A/µs, V_R = 400 V I_F = 6 A	$T_{J(D)}$ = 25 °C		2.95		A
			$T_{J(D)}$ = 100 °C		4.05		
Softness Factor = t_B/t_A	S	di/dt = 200 A/µs, V_R = 400 V I_F = 6 A	$T_{J(D)}$ = 25 °C		0.53		
			$T_{J(D)}$ = 100 °C		0.31		

NOTES:
A. Not tested parameter. Guaranteed by design.
B. Tested in typical Boost PFC application circuit.
C. Normally limited by internal circuitry.
D. Test under this condition may require pulsed operation due to self-heat. Pulse parameters (duration, repetition) are TBD.
E. BV_{DSS} 540 V maximum for 10 ns.

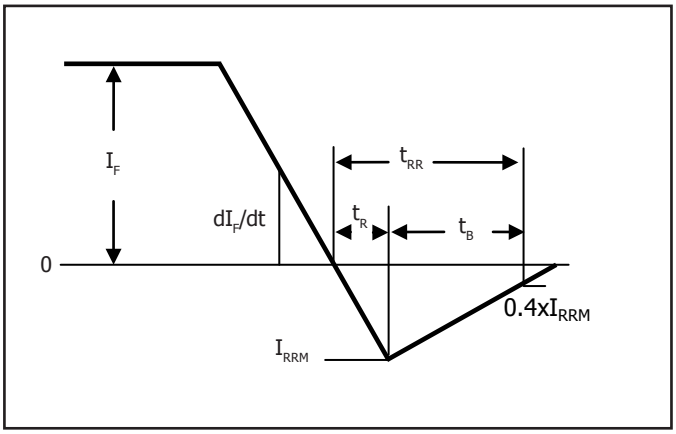


Figure 19. Reverse Recovery Definitions.

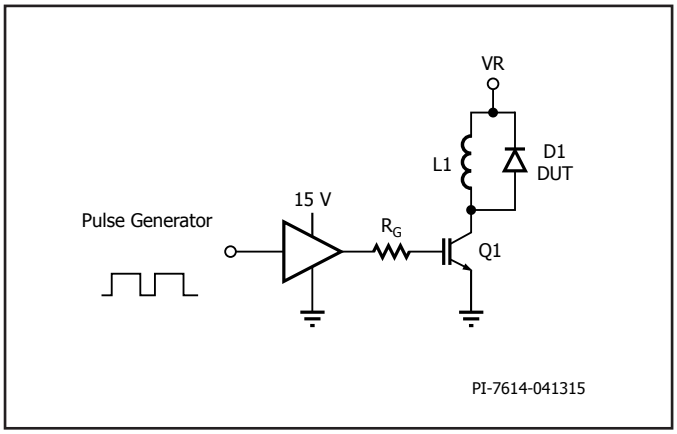


Figure 20. Reverse Recovery Test Circuit.

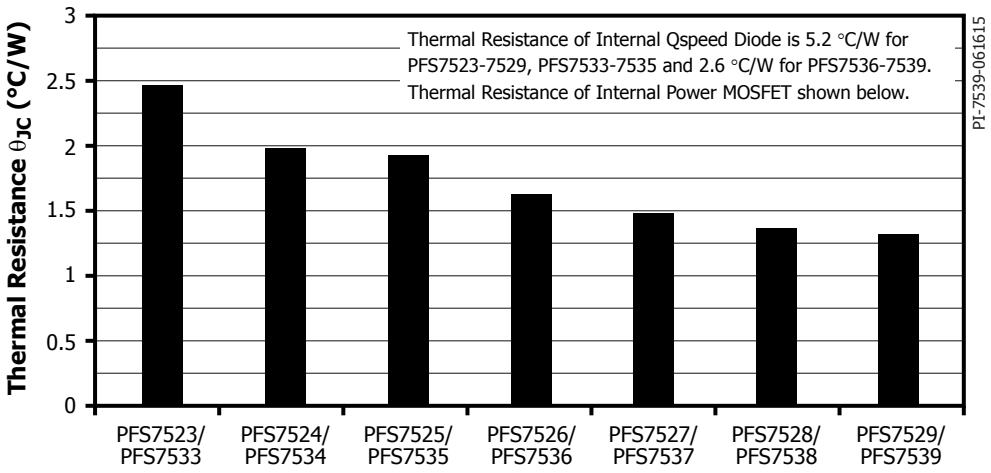


Figure 21. Thermal Resistance eSIP-16D / eSIP-16G Package (θ_{JC}).

Typical Performance Characteristics

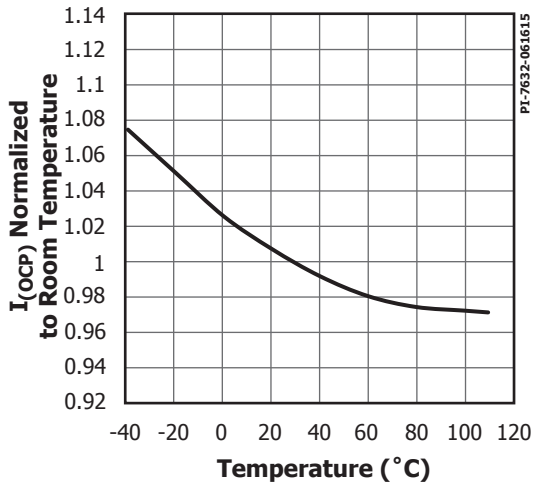


Figure 22. Normalized $I_{(OCP)}$ vs. Temperature.

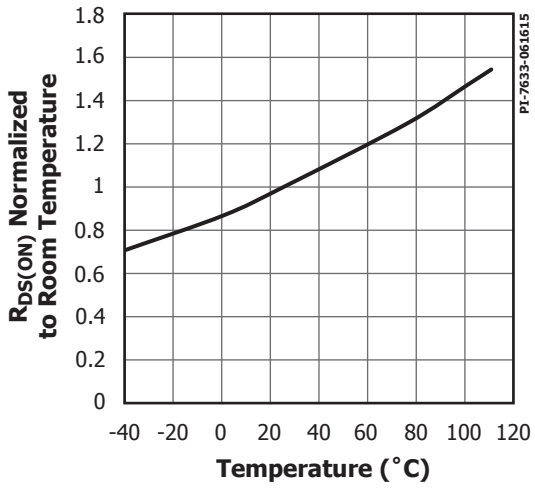


Figure 23. Normalized $R_{DS(ON)}$ vs. Temperature.

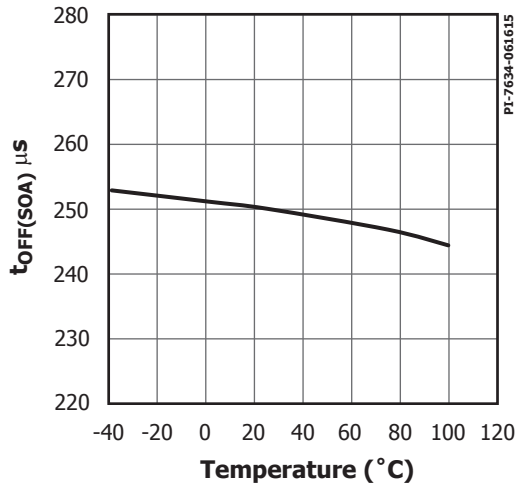


Figure 24. $t_{OFF(SOA)}$ vs. Temperature.

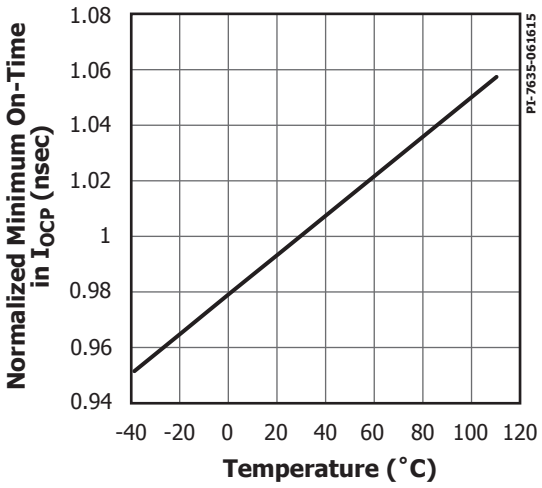


Figure 25. Normalized On-Time in IOCP vs. Temperature.

Typical Performance Characteristics

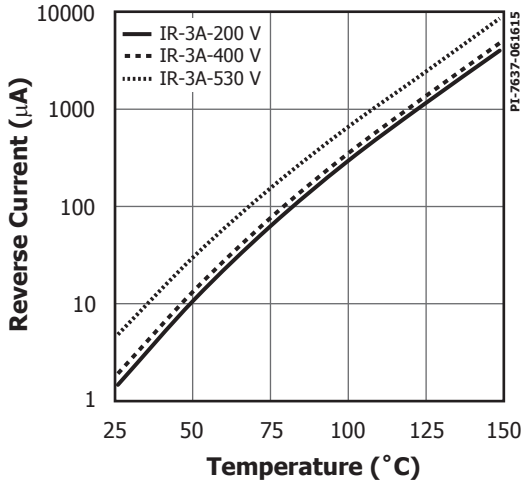


Figure 26. Temperature Dependence of 3 A Qspeed Diode Reverse Current.

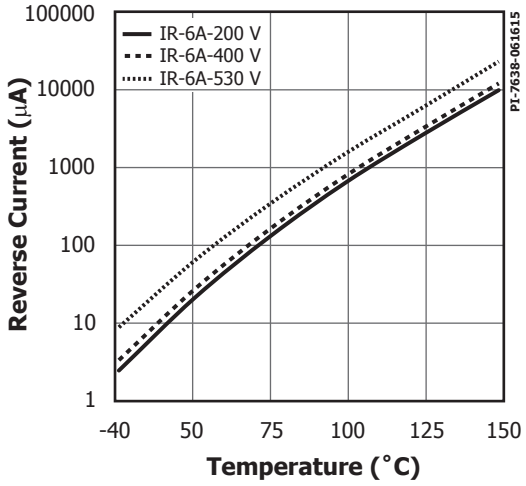


Figure 27. Temperature Dependence of 6 A Qspeed Diode Reverse Current

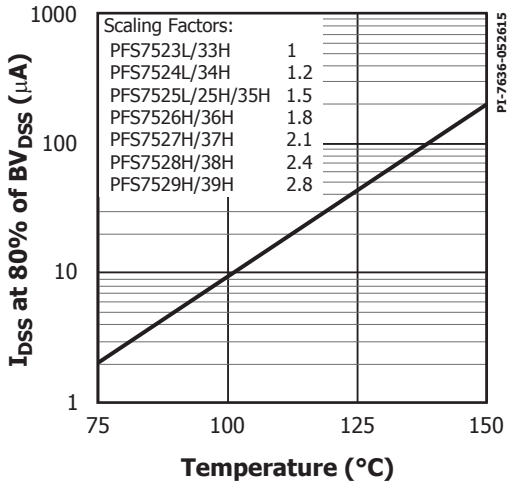
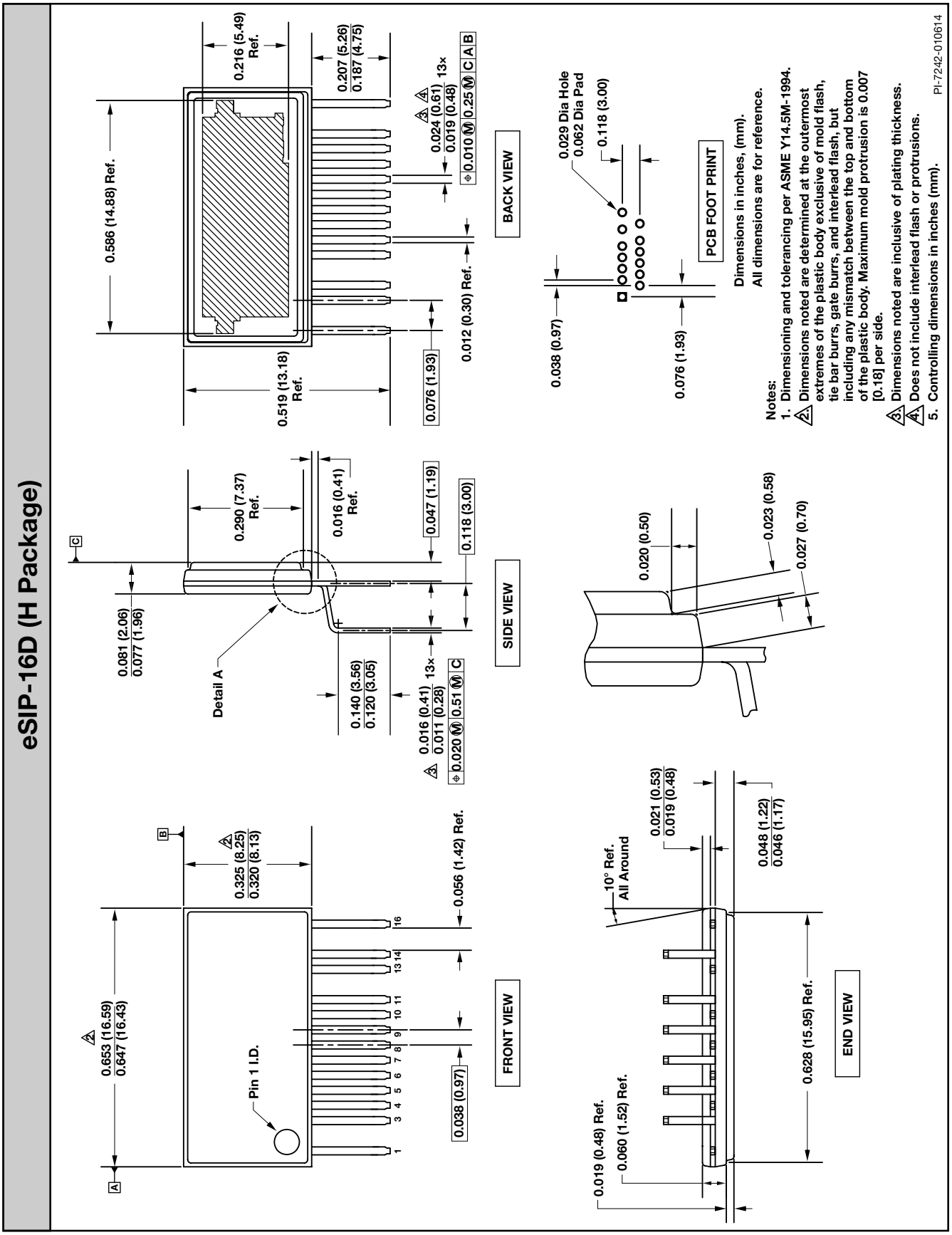


Figure 28. Typical Temperature Dependence of I_{DSS} at 80% of BV_{DSS}.

eSIP-16D (H Package)



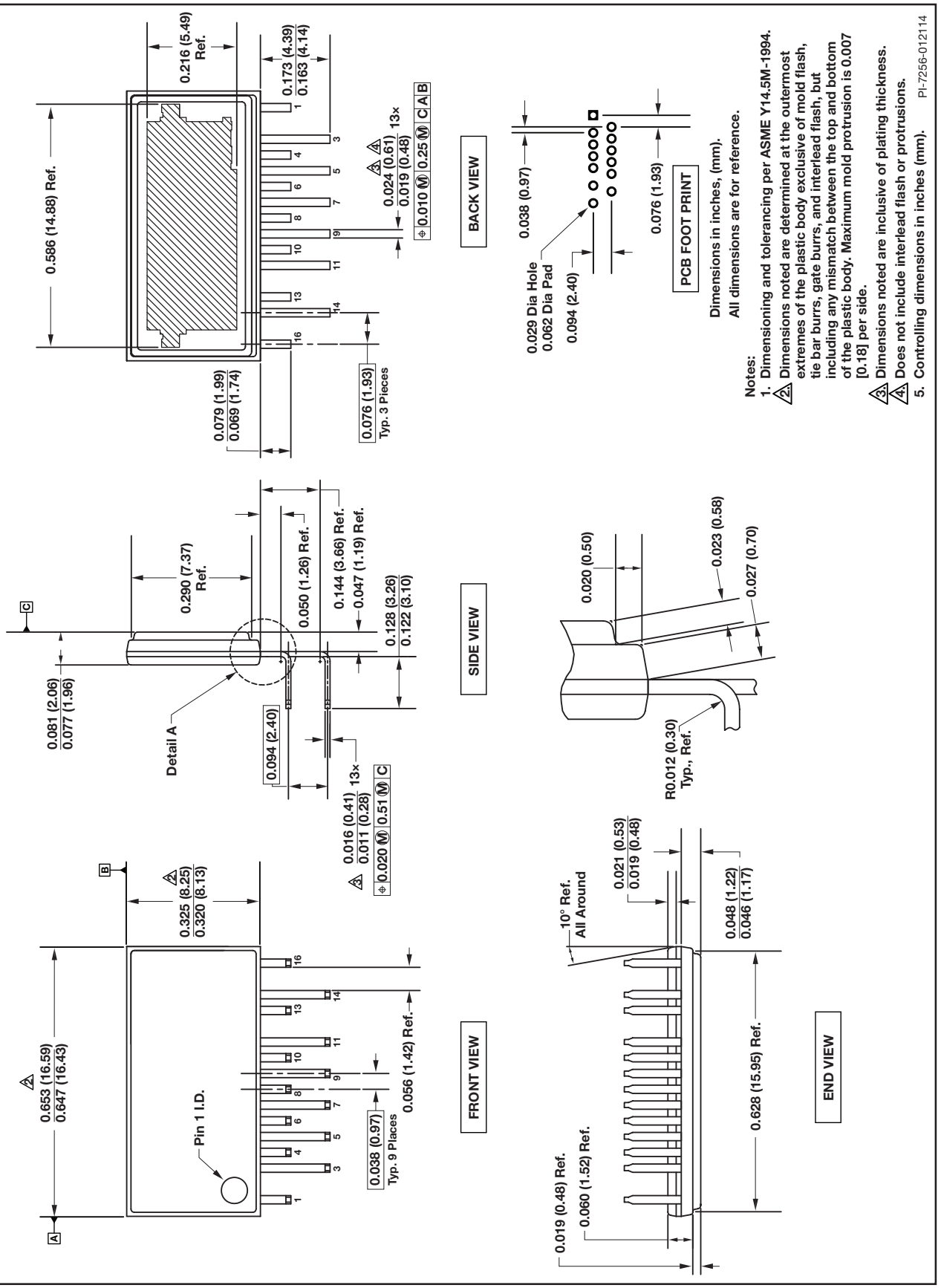
Dimensions in inches, (mm).
All dimensions are for reference.

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-7242-010614

eSIP-16G (L Package)



Dimensions in inches, (mm).
All dimensions are for reference.

Notes:

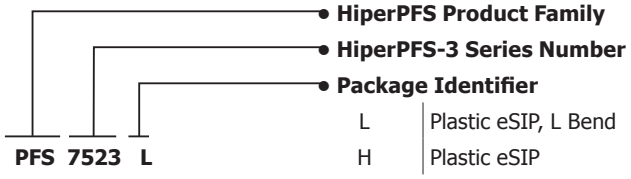
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-7256-012114

Part Ordering Information

Part Number	Option	Quantity
PFS7523L/H	Tube	30
PFS7524L/H	Tube	30
PFS7525L/H	Tube	30
PFS7526H	Tube	30
PFS7527H	Tube	30
PFS7528H	Tube	30
PFS7529H	Tube	30
PFS7533H	Tube	30
PFS7534H	Tube	30
PFS7535H	Tube	30
PFS7536H	Tube	30
PFS7537H	Tube	30
PFS7538H	Tube	30
PFS7539H	Tube	30

Part Marking Information



Notes

Revision	Notes	Date
A	Initial Release.	06/15

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