

Features

- 4 LVPECL outputs
- Up to 266MHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ)
- Two selectable inputs
- Low delay from input to output (Tpd typ. < 1.5ns)
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-20 package

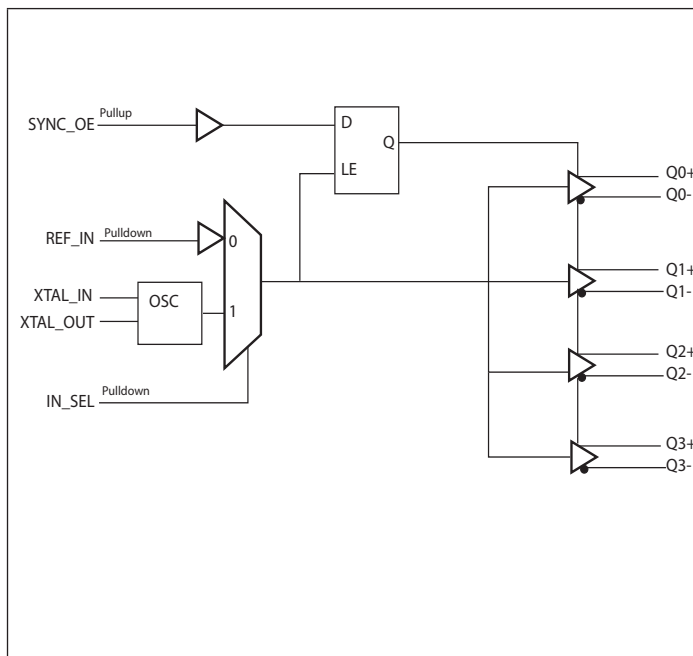
Description

The PI6C48535-11C is a fanout buffer device with embedded oscillator circuit which supports up to 266MHz frequency. This device is ideal for systems that need to generate and distribute low jitter clock signals to multiple destinations.

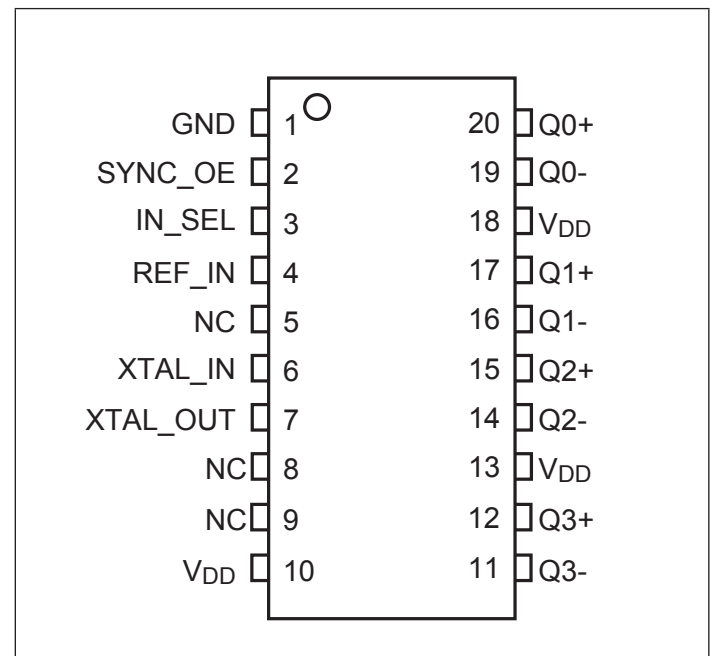
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (20-Pin TSSOP)



Pinout Table

Pin #	Pin Name	Type		Description
1	GND	Power		Ground
2	SYNC_OE	Input	Pullup	Synchronous clock enable. When High, clock outputs follow REF_IN. When low, Q+ outputs are forced low, Q- are forced high
3	IN_SEL	Input	Pulldown	Clock input source selection pin
4	REF_IN	Input	Pulldown	Clock input
5, 8, 9	NC	-		No connect
6, 7	XTAL_IN XTAL_OUT	Input		Crystal Oscillator connection
10, 13, 18	V _{DD}	Power		Power supply
11, 12	Q3+ Q3-	Output		LVPECL output clock 3
14, 15	Q2+ Q2-	Output		LVPECL output clock 2
16, 17	Q1+ Q1-	Output		LVPECL output clock 1
19, 20	Q0+ Q0-	Output		LVPECL output clock 0

Function Table

Table 1: Clock source input select function

IN_SEL	Function
0	REF_IN is the selected reference input
1	XTAL_IN is the selected reference input

Table 2: SYNC_OE select function

SYNC_OE	Function
0	All outputs disabled. Q+ disabled low, Q- disabled High.
1	All outputs enabled.

Pin Characteristics

Symbol	Parameter	Min	Typ	Max	Units
R _{PULLUP}	Input Pullup Resistor		51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor		51		kΩ

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential (V_{DD}).....	-0.5 to +4.65V
Inputs (Referenced to GND)	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up	200mA
ESD Protection (Input)	2000 V min (HBM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions ($T_A = -40$ to 85 °C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				85	mA

LVCMOS/ LVTTTL DC Characteristics ($T_A = -40$ to 85 °C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	$V_{DD} = V_{IN} = 3.465V$	2		$V_{DD}+0.3$	V
		$V_{DD} = V_{IN} = 2.625V$	1.6		$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = V_{IN} = 3.465V$	-0.3		0.8	V
		$V_{DD} = V_{IN} = 2.625V$	-0.3		0.6	V
I_{IH}	Input High Current	SYNC_OE	$V_{DD} = V_{IN} = 3.465V$		5	μA
			$V_{DD} = V_{IN} = 2.625V$		5	μA
		IN_SEL	$V_{DD} = V_{IN} = 3.465V$		150	μA
			$V_{DD} = V_{IN} = 2.625V$		150	μA
I_{IL}	Input Low Current	SYNC_OE	$V_{DD} = V_{IN} = 3.465V$	-150		μA
			$V_{DD} = V_{IN} = 2.625V$	-150		
		IN_SEL	$V_{DD} = V_{IN} = 3.465V$	-5		μA
			$V_{DD} = V_{IN} = 2.625V$	-5		

DC Electrical Specifications- LVPECL Outputs ($T_A = -40$ to 85 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		$V_{DD}-1.4$		$V_{DD}-0.9$	V
V_{OL}	Output Low voltage		$V_{DD}-2.0$		$V_{DD}-1.7$	V
V_{SWING}	Peak to Peak Output Voltage Swing		0.6		1.0	V

AC Electrical Specifications – Differential Outputs ($T_A = -40$ to 85 °C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL			266	MHz
T_r	Output rise time	From 20% to 80%	300		700	ps
T_f	Output fall time	From 80% to 20%	300		700	ps
T_{ODC}	Output duty cycle		48		52	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			
$T_{addjitter}$	Buffer additive jitter RMS			0.03		ps
T_{SK}	Output Skew	4 outputs devices, outputs in same tank, with same load, at DUT.			30	ps
T_{PD}	Propagation Delay		1450		1600	ps
T_{OD}	Valid to HiZ		200			ns
T_{OE}	HiZ to valid		200			ns
$T_{P2P\ Skew}$	Part to Part Skew ¹				TBD	ns

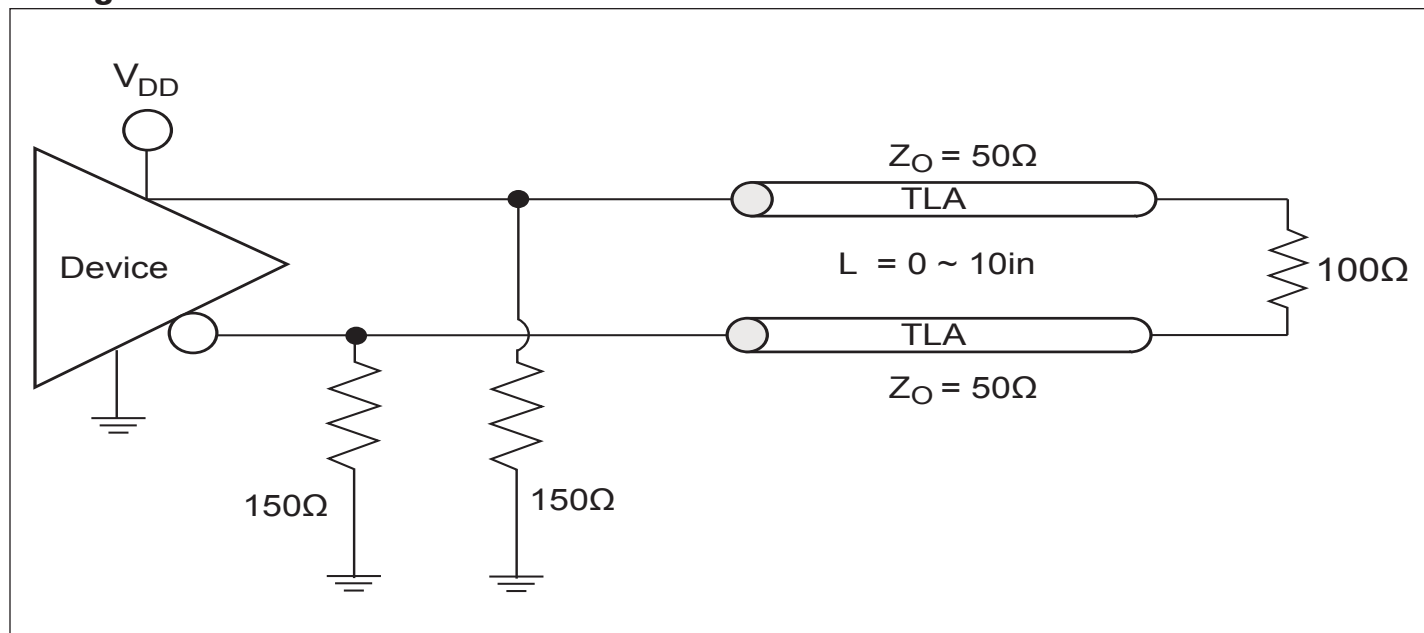
Notes:

1. This parameter is guaranteed by design

Crystal Characteristics

Parameter	Test Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency		12		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Configuration Test Load Board Termination for LVPECL



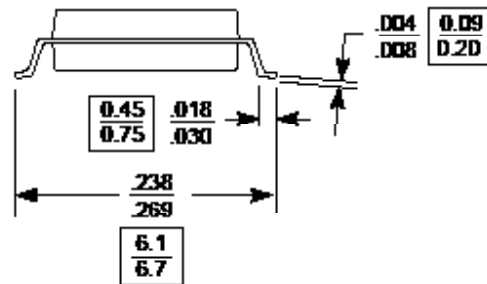
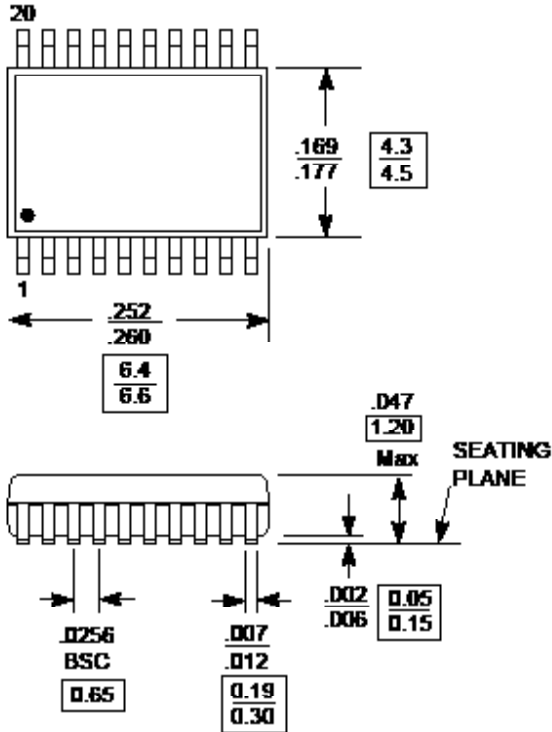
Thermal Information

Symbol	Description	
Θ_{JA}	Junction-to-ambient thermal resistance	84.0 °C/W
Θ_{JC}	Junction-to-case thermal resistance	17.0 °C/W

Packaging Mechanical: 20-Contact TSSOP (L)

DOCUMENT CONTROL NO.
PD - 1311

REVISION: E
DATE: 03/09/05



- Note:**
1. Package Outline Exclusive of Mold Flash and Metal Burr
 2. Controlling dimensions in millimeters
 3. Ref: JEDEC MO-153F1AG



Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2336 • www.pericom.com

DESCRIPTION: 20-Pin, 173-Mil Wide, TSSOP

PACKAGE CODE: L

Ordering Information

Ordering Number	Package Code	Package Description	Operating Temperature
PI6C48535-11CLIE	L	Pb-free & Green 20-Contact TSSOP	-40 to 85 °C
PI6C48535-11CLIEX	L	Pb-free & Green 20-Contact TSSOP, Tape and Reel	-40 to 85 °C

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

Mouser Electronics

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[PI6C48535-11CLIE](#) [PI6C48535-11CLIEX](#)

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- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
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- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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