

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A "full pack" plastic package. This triac is intended for use in motor control circuits where very high blocking voltage, high static and dynamic dV/dt as well as high dI_{com}/dt can occur. This "series C" triac will commutate the full rated RMS current at the maximum rated junction temperature without the aid of a snubber.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn on by dV/dt
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very high voltage capability

3. Applications

- Compressor starting controls
- General purpose motor controls
- Reversing induction motor control e.g. window shutters, blinds and sun shades

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	1000	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 92\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	25	A
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	2	6	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	2	8	35	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	2	20	35	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

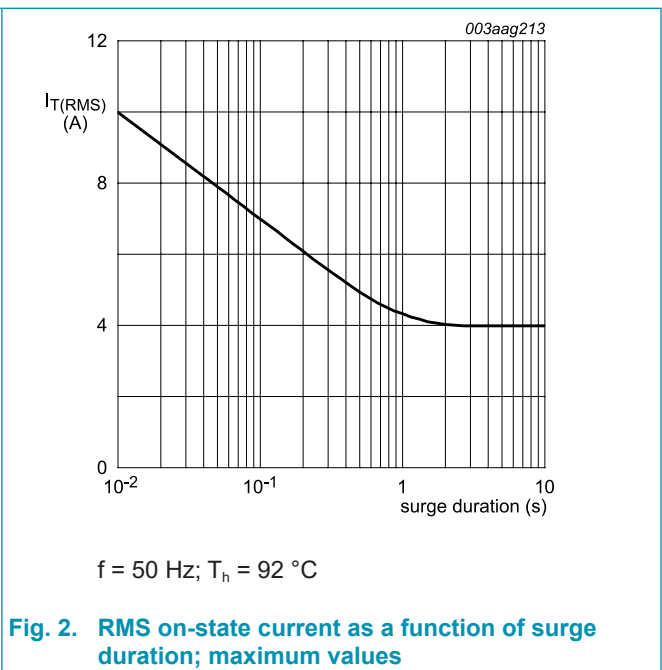
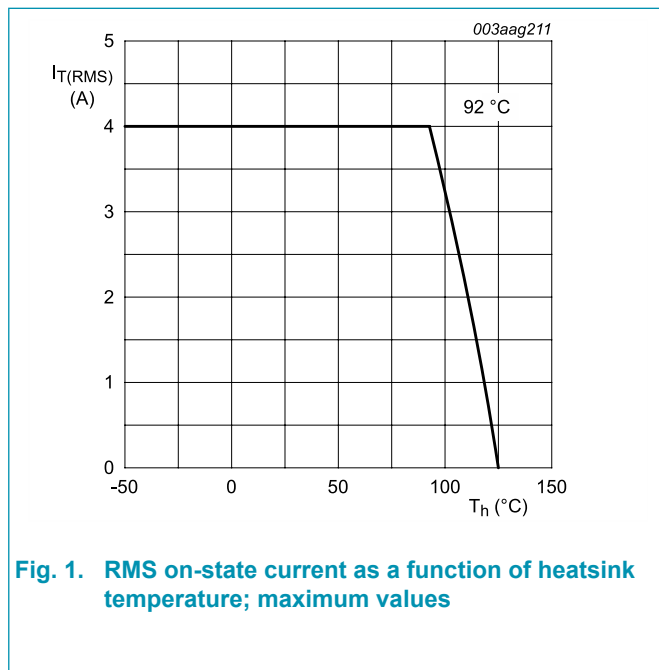
Type number	Package		
	Name	Description	Version
BTA204X-1000C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	1000	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 92\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig 4 ; Fig 5	-	25	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	27	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	3.1	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 70\text{ mA}$	-	100	A/ μ s
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_J	junction temperature		-	125	°C



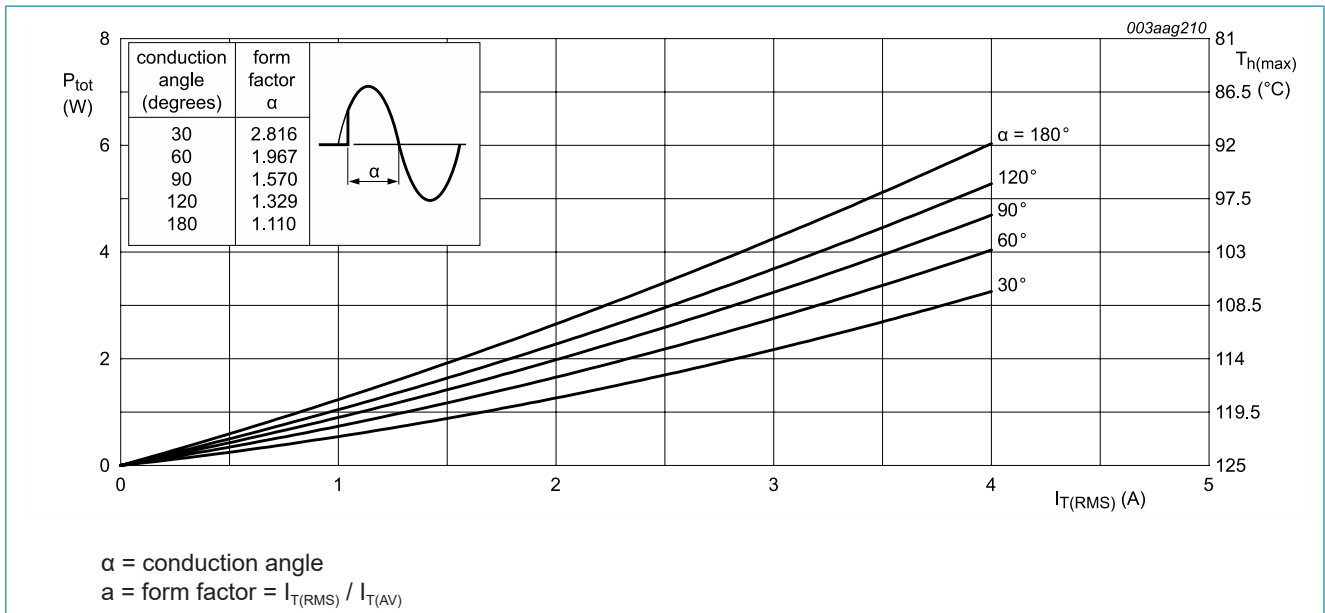


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

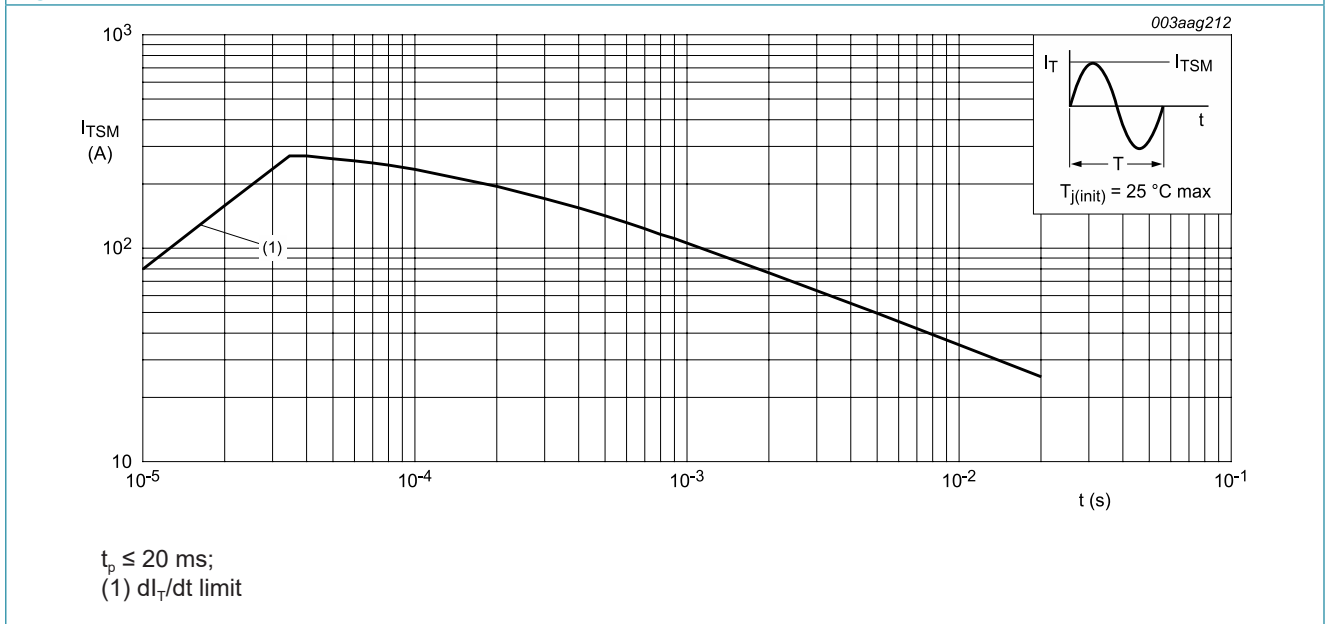
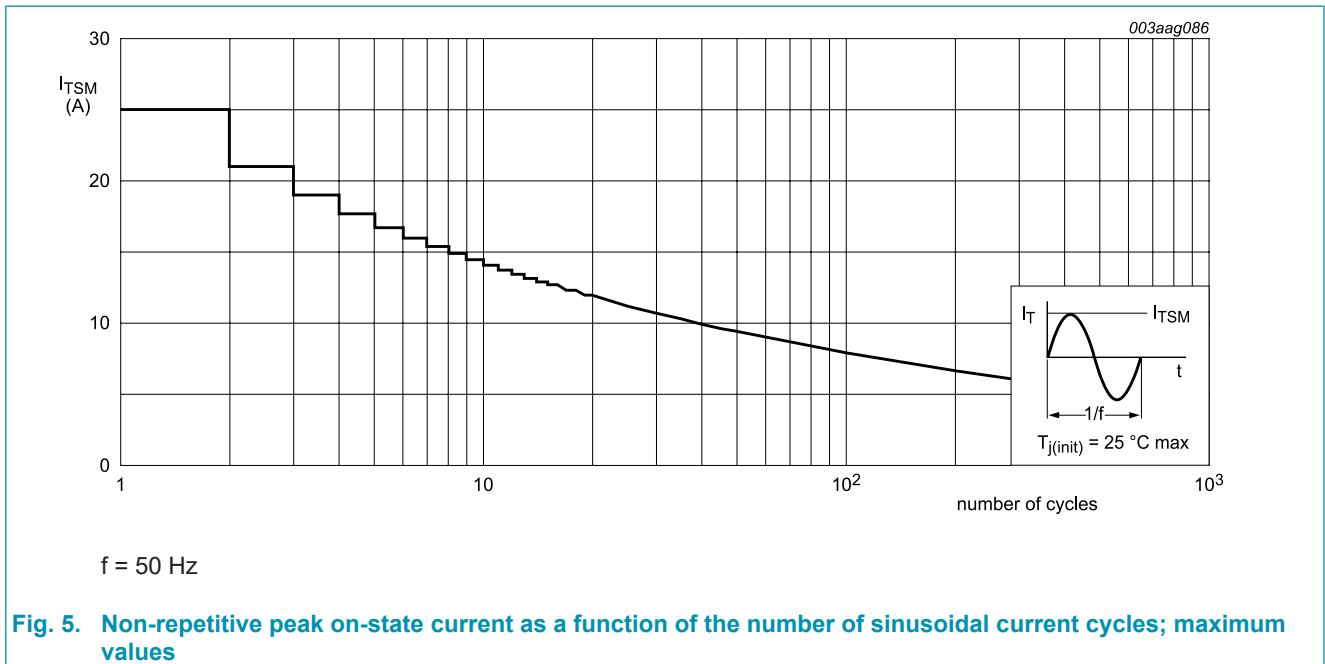


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig 6	-	-	5.5	K/W
		full cycle or half cycle; without heatsink compound; Fig 6	-	-	7.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W

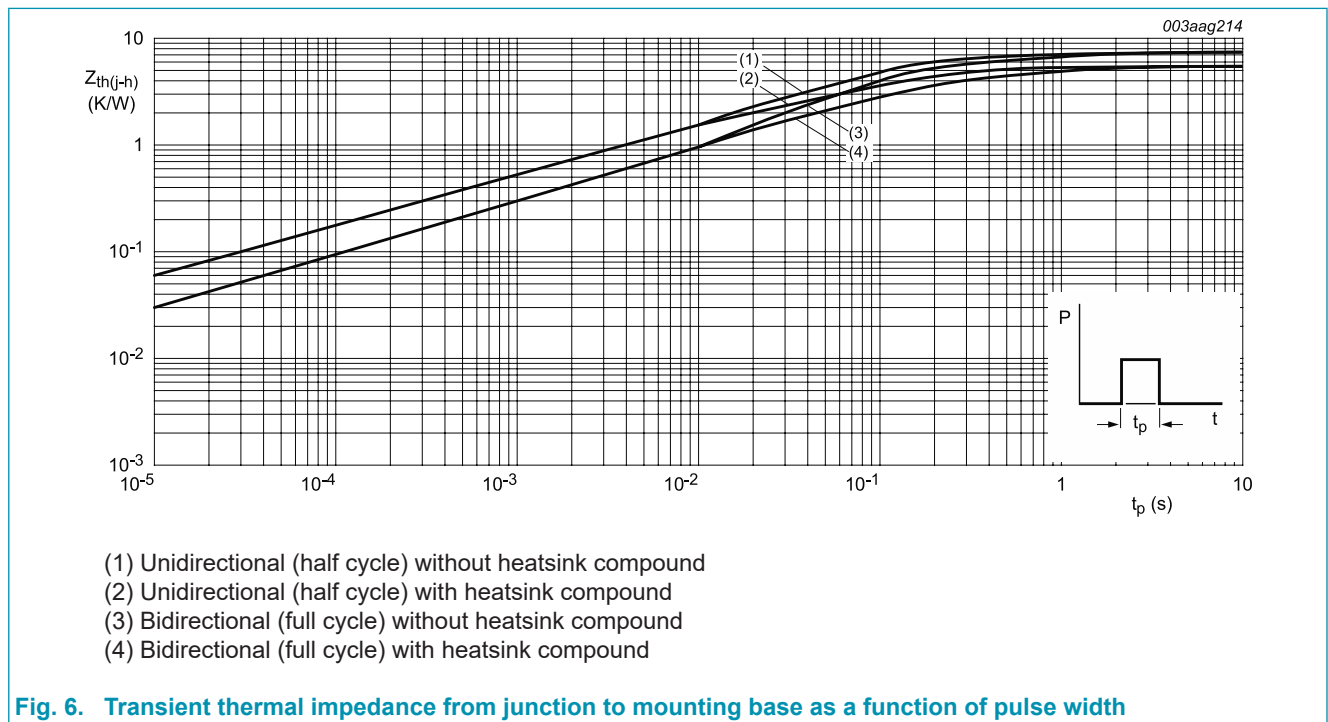


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Isolation Characteristics

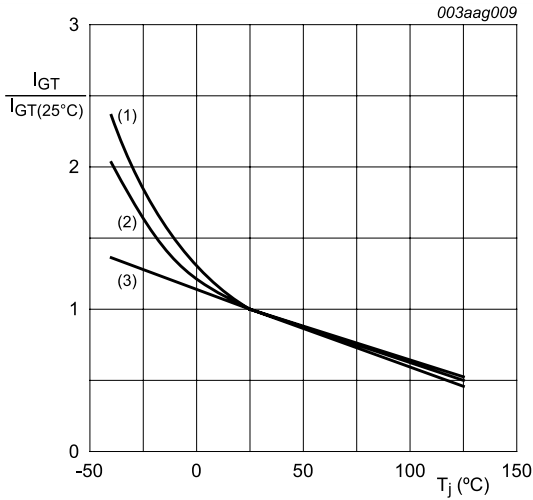
Table 6. Isolation Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_n = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_n = 25\text{ }^\circ\text{C}$	-	10	-	pF

10. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	2	6	35	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	2	8	35	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	2	20	35	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	20	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	30	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	20	mA
I_H	holding current	$V_D = 12\text{ V}; T_J = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	20	mA
V_T	on-state voltage	$I_T = 5\text{ A}; T_J = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.4	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_J = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.7	1.5	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_J = 125\text{ }^\circ\text{C};$	0.25	0.4	-	V
I_D	off-state current	$V_D = 1000\text{ V}; T_J = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 670\text{ V}; T_J = 125\text{ }^\circ\text{C};$ exponential waveform; gate open circuit	1000	500	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_J = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 4\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (without snubber condition); gate open circuit	3	30	-	A/ms
t_{gt}	gate-controlled turn-on time	$I_{TM} = 12\text{ A}; V_D = 1000\text{ V}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

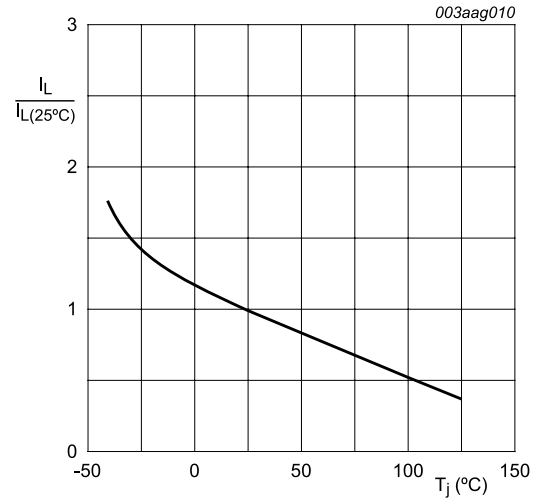


Fig. 8. Normalized latching current as a function of junction temperature

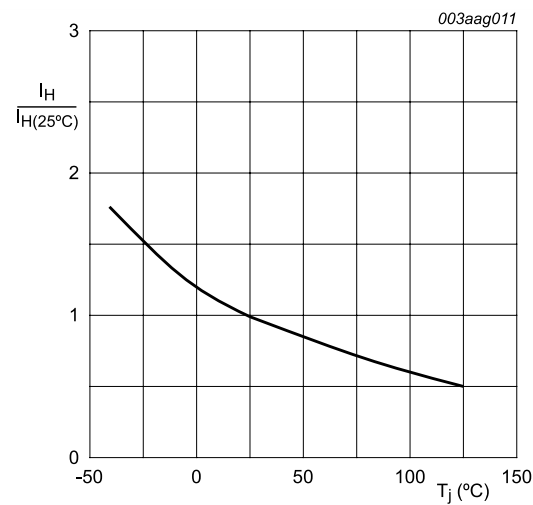
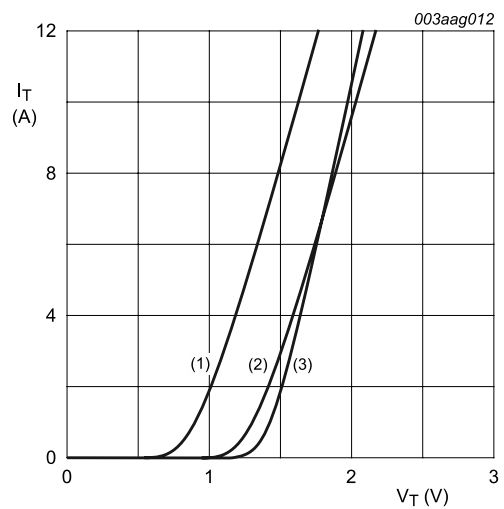


Fig. 9. Normalized holding current as a function of junction temperature



- $V_o = 1.22 \text{ V}; R_s = 0.04 \Omega$
- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
 - (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
 - (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

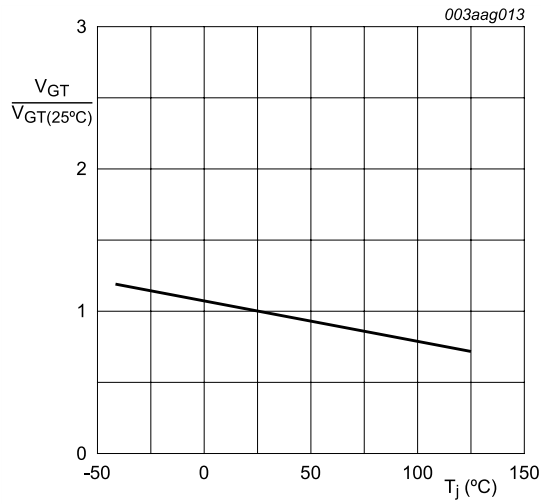
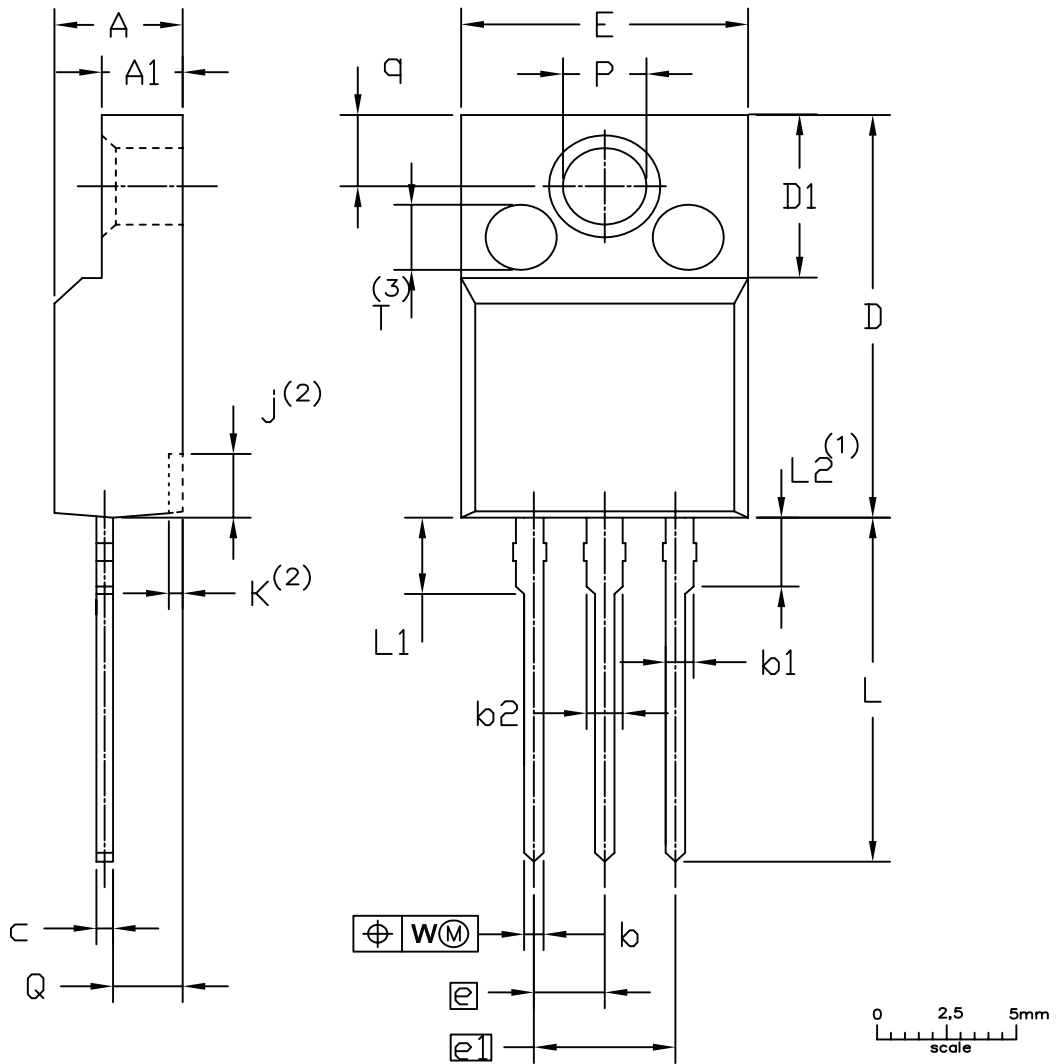


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"

SOT186A



UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j ⁽²⁾	k ⁽²⁾	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	W	T ⁽³⁾
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

- Notes
- Terminal dimensions within this zone are uncontrolled
 - Dot lines area designs may vary
 - Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3 LEADS TO220F			2013-11-14

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

1. General description.....	1
2. Features and benefits	1
3. Applications	1
4. Quick reference data	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Limiting values	3
8. Thermal characteristics	6
9. Isolation characteristics	6
10. Characteristics.....	7
11. Package outline	10
12. Legal information	11
13. Contents	13

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- Оценку стоимости проекта по компонентам.
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