74CBTLV3126

4-bit bus switch

Rev. 5 — 9 October 2018

Product data sheet

1. General description

The 74CBTLV3126 provides a 4-bit high-speed bus switch with separate output enable inputs (10E to 40E). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable (nOE) input is LOW.

To ensure the high-impedance OFF-state during power-up or power-down, nOE should be tied to the GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- Standard '126'-type pinout
- · High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- · Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



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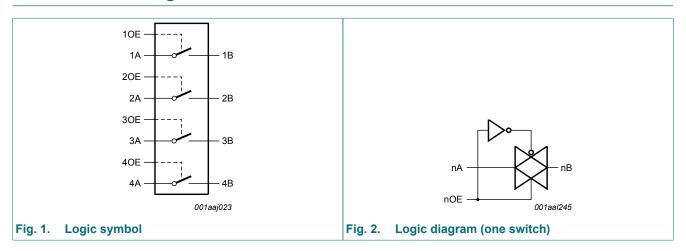
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3126DS	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3126PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74CBTLV3126BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

^[1] Also known as QSOP16.

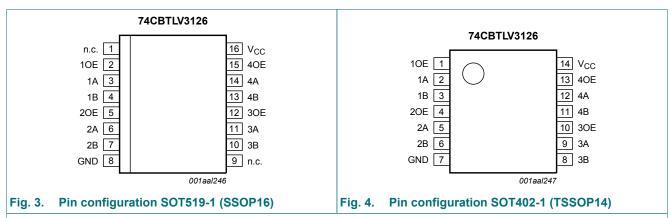
4. Functional diagram



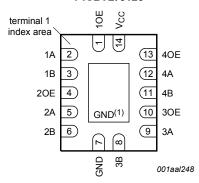
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5. Pinning information

5.1. Pinning







Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT519-1	SOT402-1 and SOT762-1	
10E, 20E, 30E, 40E	2, 5, 12, 15	1, 4, 10, 13	output enable input
1A, 2A, 3A, 4A	3, 6, 11, 14	2, 5, 9, 12	A input/output
1B, 2B, 3B, 4B	4, 7, 10, 13	3, 6, 8, 11	B output/input
GND	8	7	ground (0 V)
V _{CC}	16	14	supply voltage
n.c.	1, 9	-	not connected

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6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Output enable input nOE	Function switch
L	OFF-state
Н	ON-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	control inputs [1]	-0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode [2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	V _{SW} = 0 V to V _{CC}	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C to} + 125 ^{\circ}\text{C}$ [3]	-	500	mW

^[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
VI	input voltage	control inputs	0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	pin nOE; V _{CC} = 2.3 V to 3.6 V	0	200	ns/V

^[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

^[3] For SSOP16 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C. For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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9. Static characteristics

Table 6. Static characteristics

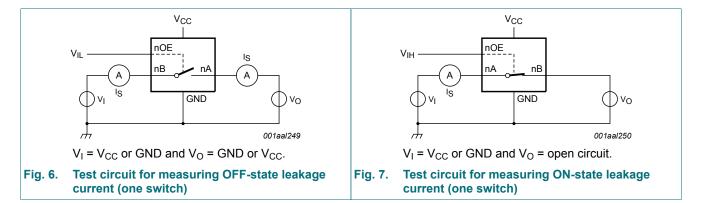
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb}	= -40 °C to ·	+85 °C	T _{ar} -40 °C to	_{nb} = o +125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
	voltage	V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
	voltage	V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
l _l	input leakage current	pin nOE; V_I = GND to V_{CC} ; V_{CC} = 3.6 V	-	-	±1.0	-	±20	μΑ
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see <u>Fig. 6</u>	-	-	±1	-	±20	μΑ
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see <u>Fig. 7</u>	-	-	±1	-	±20	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±10	-	±50	μΑ
I _{CC}	supply current	V_I = GND or V_{CC} ; I_O = 0 A; V_{SW} = GND or V_{CC} ; V_{CC} = 3.6 V	-	-	10	-	50	μA
ΔI _{CC}	additional supply current	pin nOE; $V_1 = V_{CC} - 0.6 \text{ V}$; [2] $V_{SW} = \text{GND or } V_{CC}$; $V_{CC} = 3.6 \text{ V}$	-	-	300	-	2000	μA
Cı	input capacitance	pin nOE; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	$V_{CC} = 3.3 \text{ V}; V_I = 0 \text{ V to } 3.3 \text{ V}$	-	14.3	-	-	-	pF

All typical values are measured at T_{amb} = 25 °C. One input at 3 V, other inputs at V_{CC} or GND.

4-bit bus switch

9.1. Test circuits



9.2. ON resistance

Table 7. Resistance Ron

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

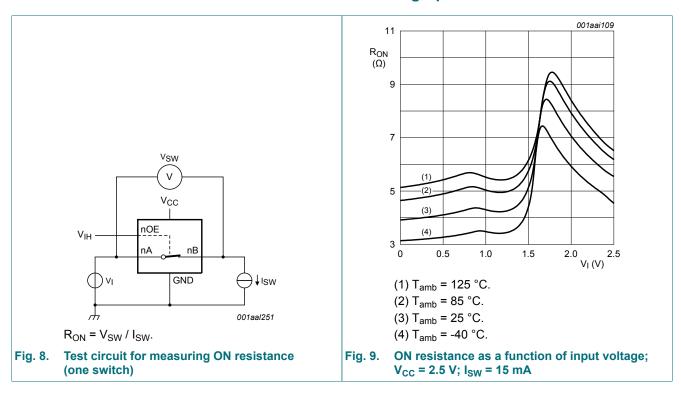
Symbol	Parameter	Conditions	T _{amb} =	-40 °C to	+85 °C		_{nb} =) +125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON}	ON resistance	V _{CC} = 2.3 V to 2.7 V; [2] see <u>Fig. 9</u> to <u>Fig. 11</u>						
		I _{SW} = 64 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 15 mA; V _I = 1.7 V	-	8.4	40.0	-	60.0	Ω
		V _{CC} = 3.0 V to 3.6 V; see <u>Fig. 12</u> to <u>Fig. 14</u>						
		I _{SW} = 64 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 15 mA; V _I = 2.4 V	-	6.2	15.0	-	25.5	Ω

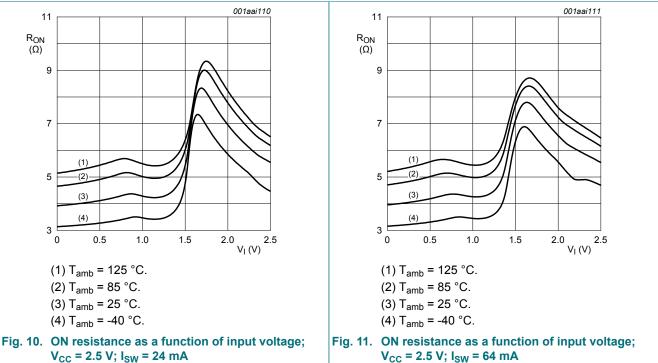
^[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC} .

^[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

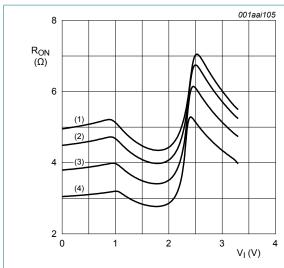
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9.3. ON resistance test circuit and graphs



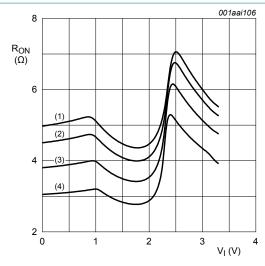


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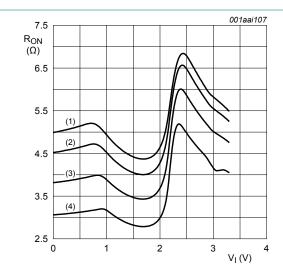
- (1) $T_{amb} = 125 \, ^{\circ}C$.
- (2) $T_{amb} = 85 \, ^{\circ}C$.
- (3) T_{amb} = 25 °C.
- (4) $T_{amb} = -40 \, ^{\circ}C$.

Fig. 12. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 15 mA



- (1) $T_{amb} = 125 \,^{\circ}C$.
- (2) $T_{amb} = 85 \, ^{\circ}C$.
- (3) $T_{amb} = 25 \, ^{\circ}C$.
- (4) T_{amb} = -40 °C.

Fig. 13. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 24 mA



- (1) $T_{amb} = 125 \, ^{\circ}C$.
- (2) T_{amb} = 85 °C.
- (3) $T_{amb} = 25 \, ^{\circ}C$.
- (4) $T_{amb} = -40 \, ^{\circ}C$.

Fig. 14. ON resistance as a function of input voltage; V_{CC} = 3.3 V; I_{SW} = 64 mA

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10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 18

Symbol	Parameter	Conditions	T _{amb} =	-40 °C to	+85 °C	T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation	nA to nB or nB to nA; see Fig. 16 [2][3]						
	delay	V _{CC} = 2.3 V to 2.7 V	-	-	0.13	-	0.20	ns
		V _{CC} = 3.0 V to 3.6 V	-	-	0.20	-	0.31	ns
t _{en}	enable time	nOE to nA or nB; see Fig. 17 [4]						
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	4.5	1.0	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.2	4.2	1.0	6.0	ns
t _{dis}	disable time	nOE to nA or nB; see Fig. 17 [5]						
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	4.7	1.0	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.4	4.8	1.0	6.5	ns

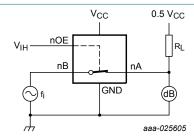
- All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC} . The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- t_{pd} is the same as t_{PLH} and t_{PHL} .
- t_{en} is the same as t_{PZH} and t_{PZL}.
- t_{dis} is the same as t_{PHZ} and t_{PLZ} .

10.1. Additional dynamic characteristics

Table 9. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);

Symbol	Parameter	Conditions	T,	T _{amb} = 25 °C		Unit
			Min	Тур	Max	
f _(-3dB)	-3 dB frequency response	V_I = GND or V_{CC} ; t_r = $t_f \le 2.5$ ns; V_{CC} = 3.3 V; R_L = 50 Ω ; see Fig. 15	-	406	-	MHz



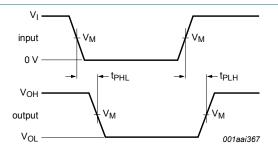
nOE connected to V_{CC} ; f_i is biased at $0.5V_{CC}$. Adjust f_i voltage to obtain 0 dBm level at output. Increase fi frequency until dB meter reads -3 dB.

Fig. 15. Test circuit for measuring the frequency response when channel is in ON-state

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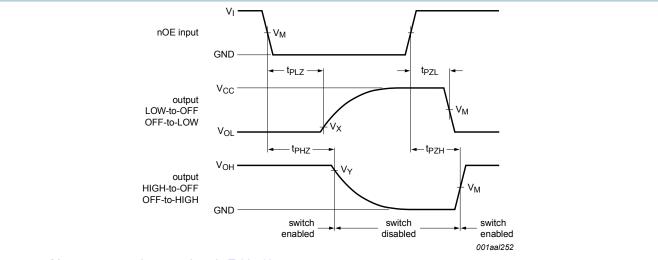
10.2. Waveforms and test circuit



Measurement points are given in <u>Table 10</u>.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 16. The data input (nA or nB) to output (nB or nA) propagation delays



Measurement points are given in <u>Table 10</u>.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

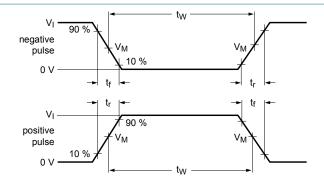
Fig. 17. Enable and disable times

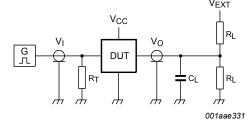
Table 10. Measurement points

Supply voltage	Input		Output			
V _{CC}	V _M	VI	V _M	V _X	V _Y	
2.3 V to 2.7 V	0.5V _{CC}	V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V	
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V	

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Test data is given in Table 11.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	-oad			V _{EXT}		
V _{CC}	CL	R _L	$t_r = t_f$	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	≤ 2.0 ns	open	GND	2V _{CC}
3.0 V to 3.6 V	50 pF	500 Ω	≤ 2.0 ns	open	GND	2V _{CC}

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11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

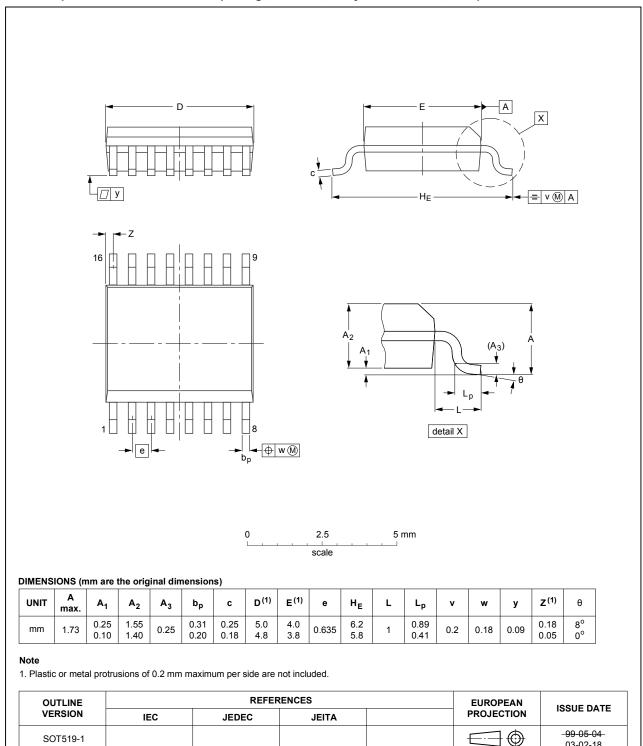


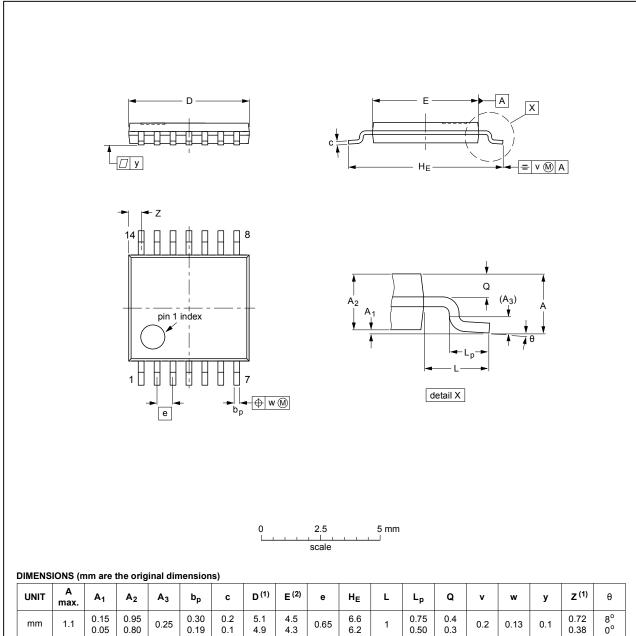
Fig. 19. Package outline SOT519-1 (SSOP16)

03-02-18

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT402-1		MO-153			-99-12-27- 03-02-18

Fig. 20. Package outline SOT402-1 (TSSOP14)

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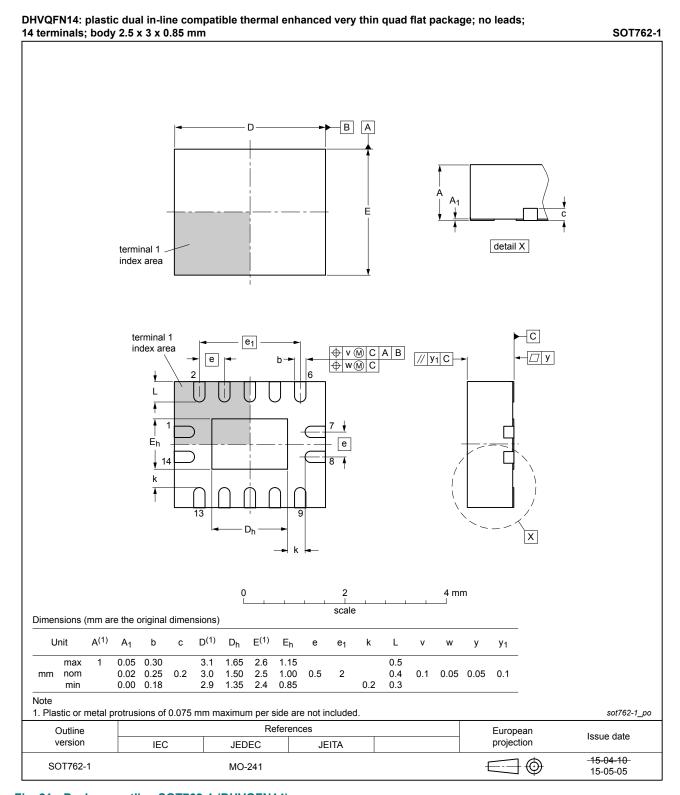


Fig. 21. Package outline SOT762-1 (DHVQFN14)

4-bit bus switch

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

13. Revision history

Table 13. Revision history

Release date	Data sheet status	Change notice	Supersedes		
20181009	Product data sheet	-	74CBTLV3126 v.4		
 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 					
20161108	Product data sheet	-	74CBTLV3126 v.3		
Section 10.1 added.					
20111215	Product data sheet	-	74CBTLV3126 v.2		
Legal pages updated.					
20110104	Product data sheet	-	74CBTLV3126 v.1		
20100105	Product data sheet	-	-		
	20181009 The format of of Nexperia. Legal texts has 20161108 Section 10.1 20111215 Legal pages 20110104	20181009 Product data sheet The format of this data sheet has been rof Nexperia. Legal texts have been adapted to the necessary and the second sheet Product data sheet Section 10.1 added. 20111215 Product data sheet Legal pages updated. 20110104 Product data sheet	20181009 Product data sheet - The format of this data sheet has been redesigned to con of Nexperia. Legal texts have been adapted to the new company name 20161108 Product data sheet - Section 10.1 added. 20111215 Product data sheet - Legal pages updated. 20110104 Product data sheet -		

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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4-bit bus switch

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OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
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- Работу по проектам и поставку образцов.
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- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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