ZILOG

*ADVAANCE INFORMATION SPECIFICATION*

# Z86E03/E06

## CMOS Z8® 8-BIT OTP CCP™ CONSUMER CONTROLLER PROCESSORS

2

### FEATURES

- The Z86E03/E06 Devices Have the Following General Characteristics:

| Part | ROM | RAM | Speed |
|---|---|---|---|
| Z86E03 | 512 bytes | 60 | 8 MHz |
| Z86E06 | 1 Kbyte | 124 | 12 MHz |

- 18-Pin Package (DIP, SOIC)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: –40°C to +105°C
- Clock Speeds up to 8 MHz (E03) and 12 MHz (E06)
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (E03); 1.0 µs @ 12 MHz (E06)
- Multiple Expanded Register File Control Registers and Two SPI Registers (Z86E06 only)
- One/Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Permanent Watch-Dog Timer Option
- Power-On Reset Timer
- Programmable Auto Latches
- Two Standby Modes: STOP and HALT
- Two Comparators with Programmable Interrupt Polarity
- 14 Input/Output Lines (Two with Comparator Inputs)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Serial Peripheral Interface (SPI) (Z86E06 Only)
- Software Programmable Low EMI Mode
- EPROM Protect Option

### GENERAL DESCRIPTION

Zilog's Z86E03/E06 OTP (One-Time Programmable) CCP™ (Consumer Controller Processors) are members of the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 512 and 1K bytes of EPROM and 60 and 124 bytes of general-purpose RAM, respectively. These low cost, low power consumption 18-pin CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86E03/E06 architecture is characterized by Zilog's 8-bit microcontroller core with the addition of an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The Z86E03/E06 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86E03/E06 provides 14 pins dedicated to input and output. These lines are grouped into two ports and are configurable under software control to provide timing, status signals, or parallel I/O.

## GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (Figure 1). The Register File is composed of 60/124 bytes of General-Purpose Registers, two I/O Port registers, and thirteen/fifteen Control and Status registers. The Expanded Register File consists of three control registers in the Z86E03, and four control registers, a SPI Receive Buffer, and a SPI compare register in the Z86E06.

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), and serial peripheral interface (E06 only), the Z86E03/E06 meets the needs of a variety of sophisticated controlle applications.

**Notes:**
All Signals with a preceding front slash, "/", are active Low, e.g. B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

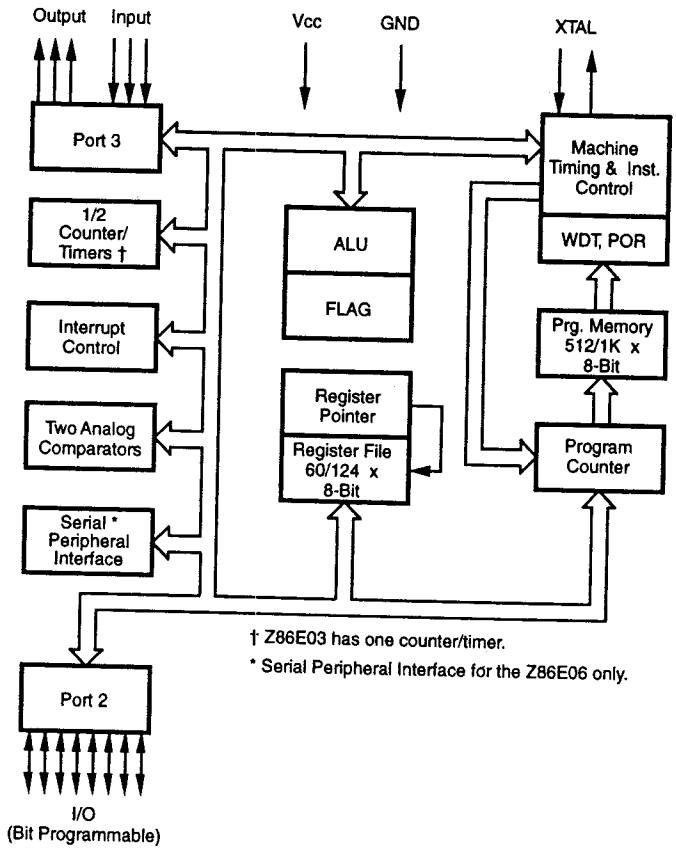



**Figure 1. Z86E03/E06 Functional Block Diagram**

## PIN DESCRIPTION

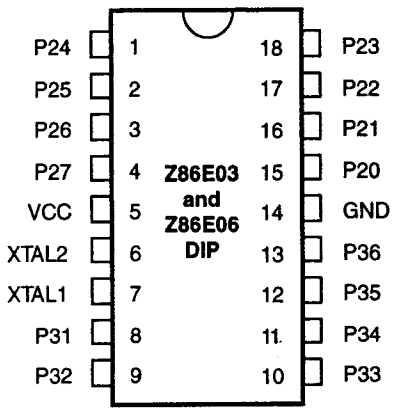



**Figure 2. 18-Pin DIP Pin Configuration**

**Table 1. 18-Pin DIP and SOIC Pin Identification**

| No | Symbol | Function | Direction |
|---|---|---|---|
| 1-4 | P24-27 | Port 2, pins 4, 5, 6, 7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | XTAL2 | Crystal Oscillator Clock | Output |
| 7 | XTAL1 | Crystal Oscillator Clock | Input |
| 8-10 | P31-33 | Port 3, pins 1, 2, 3 | Fixed Input |
| 11-13 | P34-36 | Port 3, pins 4, 5, 6 | Fixed Output |
| 14 | GND | Ground | |
| 15-18 | P20-23 | Port 2, pins 0, 1, 2, 3 | In/Output |



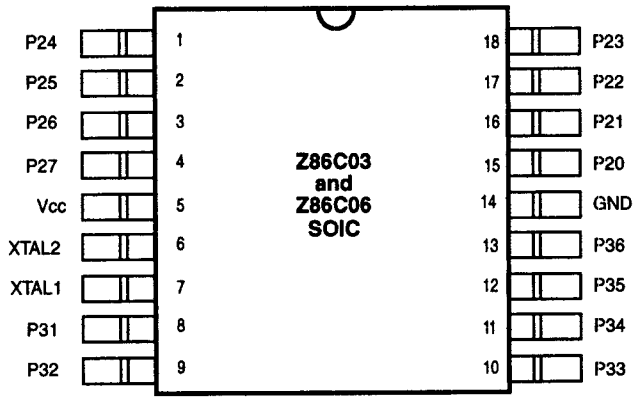



**Figure 3. 18-Pin SOIC Pin Configuration**

## PIN FUNCTIONS

**XTAL1.** *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or an external single-phase clock to the on-chip oscillator input.

**XTAL2.** *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

**Port 2 (P27-P20).** Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered and contain Auto Latches. Bits programmed as outputs may be globally programmed as either push-pull or open-drain (Figure 4a., 4b., and 4c.). Low EMI output buffers can be globally programmed by the software. In addition, when the SPI is enabled, P20 functions as data-in (DI), and P27 functions as data-out (DO) for the SPI (SPI on the Z86E06 only).

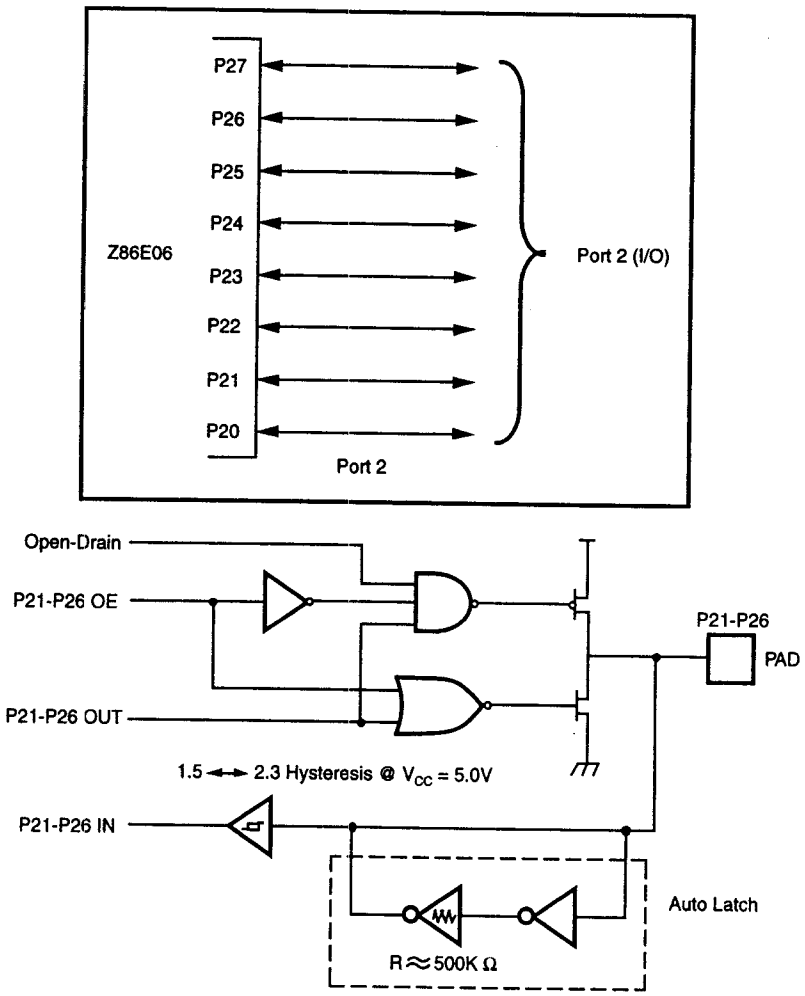



**Figure 4a. Port 2 Configuration (Z86E06)**



PS021001-0603

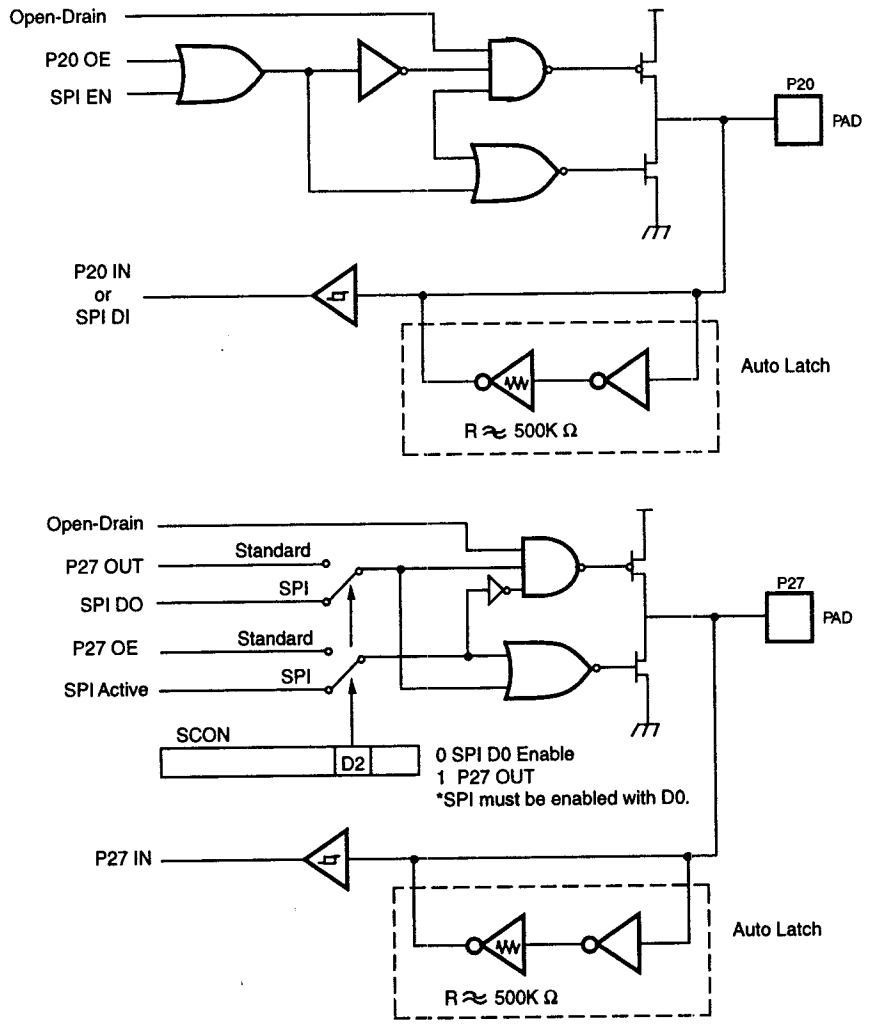



**Figure 4b. Port 2 Configuration (Z86E06)**

**PIN FUNCTIONS** (Continued)

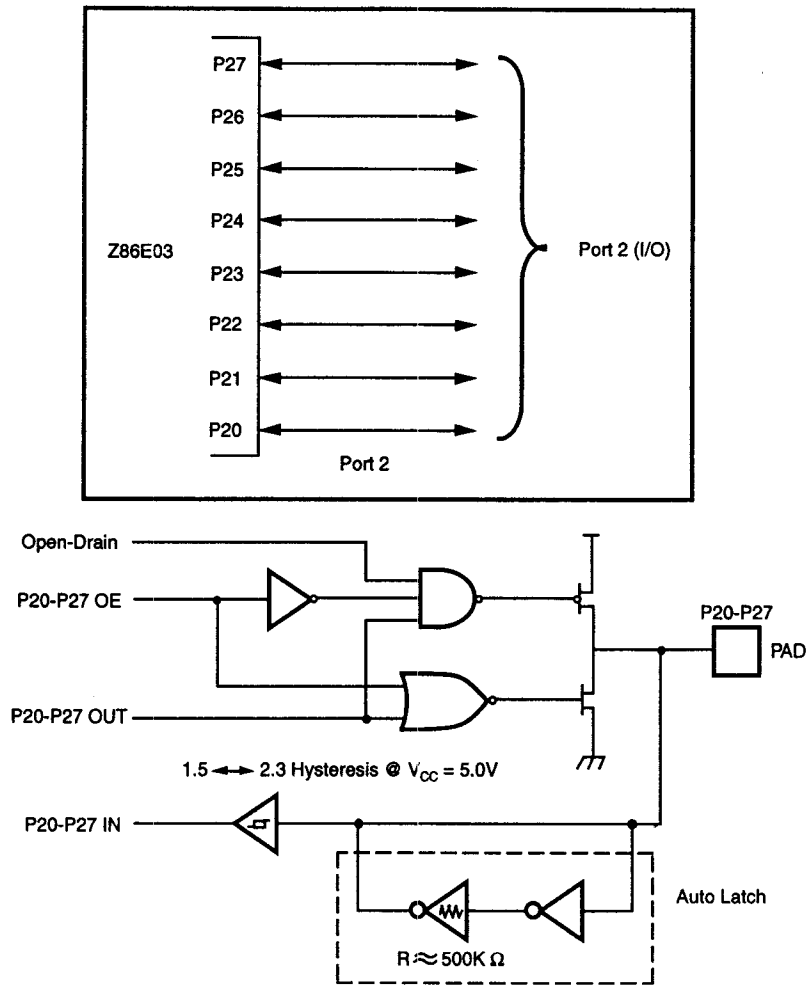



**Figure 4c. Port 2 Configuration (Z86E03)**

**Auto Latch.** The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

**Port 3 (P36-P31).** Port 3 is a 6-bit, CMOS compatible port. These six lines consist of three fixed inputs (P31-P33) and three fixed outputs (P34-P36). Pins P31, P32, and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, and P36 are push-pull outputs. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming Port 3 Mode Register (P3M-bit D1). Pins P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input when the analog mode is selected. P33 is a falling edge interrupt input only.

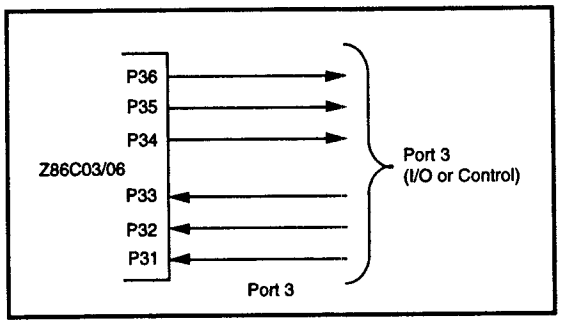
**Note:** P33 is available as an interrupt input only in the digital mode. P31 and P32 are valid interrupt inputs and P31 is the $T_{IN}$ input when the analog or digital input mode is selected.

The outputs from the analog comparator can be globally programmed to output from P34 and P35 by setting PCON (F) 00 bit D0 = 1.

Access to Counter/Timer 1 is made through P31 ($T_{IN}$) and P36 ($T_{OUT}$).

In the Z86E06, pin P34 can also be configured as SPI clock (SK), input and output, and pin P35 can be configured as Slave Select (SS) in slave mode only, when the SPI is enabled (Figures 5a and 5b).

2



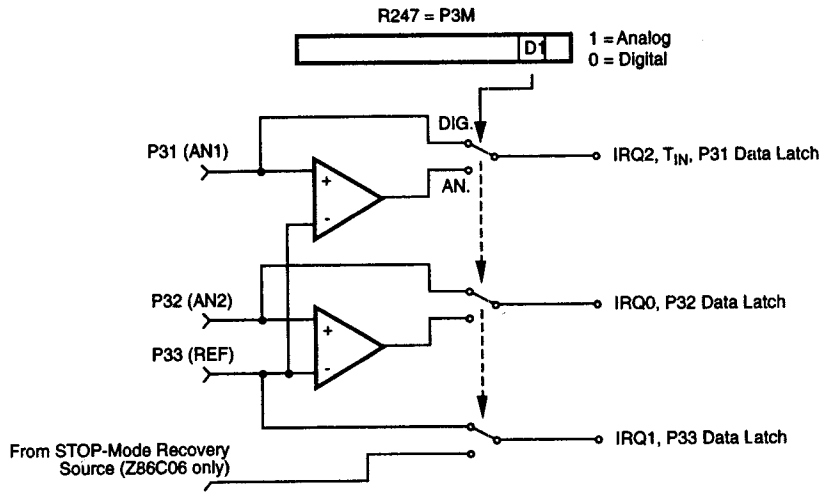




**Figure 5a. Port 3 Configuration**

**PIN FUNCTIONS** (Continued)

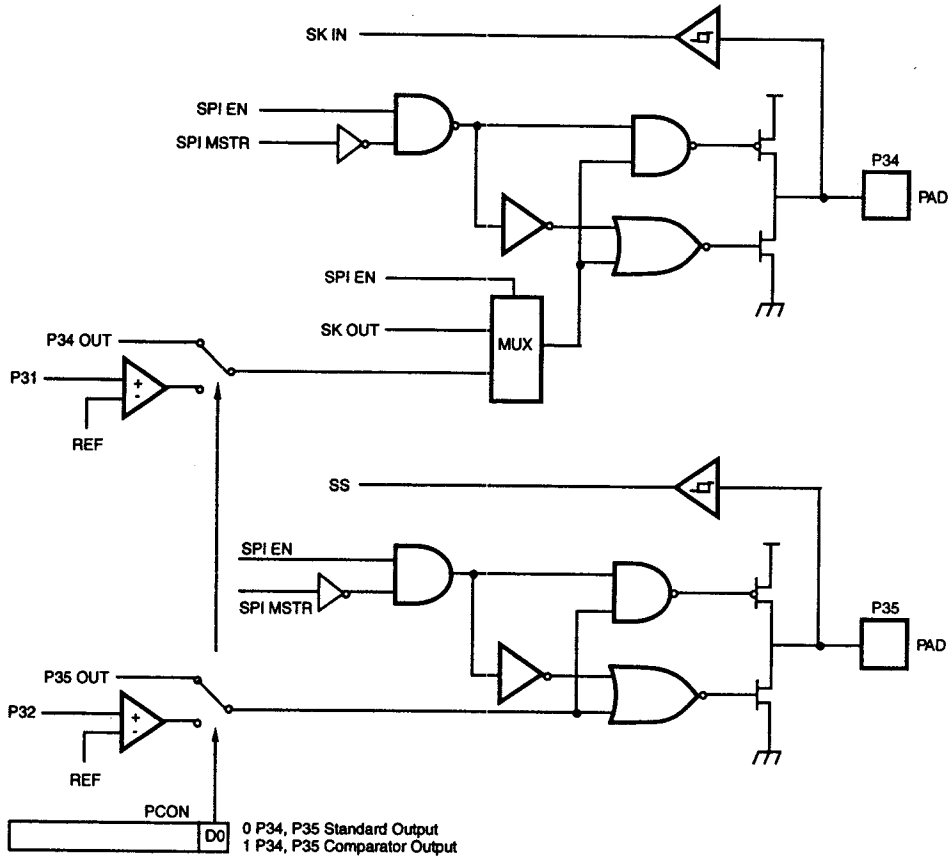



**Figure 5b. Port 3 Configuration (Z86E06)**

**Low EMI Emission.** The Z86E03/E06 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns (typical).
- Low EMI output drivers resistance of 200 ohms (typical).
- Low EMI oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz (250 ns cycle time) when the low EMI oscillator is selected and SCLK = External (SMR Register Bit D1=1).

**Comparator Inputs.** Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, Pin P33 can be used as a P33 register input or IRQ1 source.

## FUNCTIONAL DESCRIPTION

**RESET.** The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source
- Low Voltage Protection

Having the Auto Power-On Reset circuitry built-in, the Z86E03/E06 does not require an external reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles.

The device does not re-initialize the WDTMR, SMR, P2M, or P3M registers to their reset values on a STOP-Mode Recovery operation.

**Program Memory.** Z86E03/E06 can address up to 512/1K bytes of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 511/1023 consists of on-chip, user program mask ROM.

**EPROM Protect.** The 512/1K bytes of Program Memory is mask programmable. A EPROM protect feature will prevent "dumping" of the EPROM contents by inhibiting execution of the LDC and LDCI instructions to program memory in all modes.

EPROM protect is EPROM-programmable. It is selected by the customer when the ROM code is submitted. **Selecting ROM protect disables the LDC and LDCI instructions in all modes. ROM lookup tables are not supported in this mode.**

**Expanded Register File (ERF).** The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of the RP register select the working register group (Figure 7). For the Z86E03, three system configuration registers reside in the ERF address space Bank F. For the Z86E06, three system configuration registers reside in the ERF address space Bank F, while three SPI registers reside in Bank C. The rest of the ERF address space is not physically implemented and is open for future expansion.

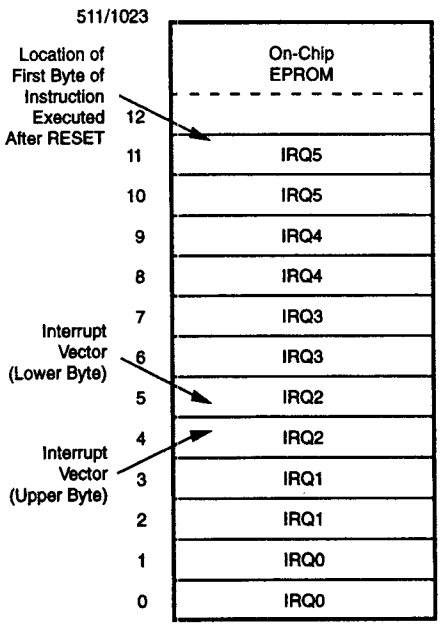



**Figure 6. Program Memory Map**

## FUNCTIONAL DESCRIPTION (Continued)

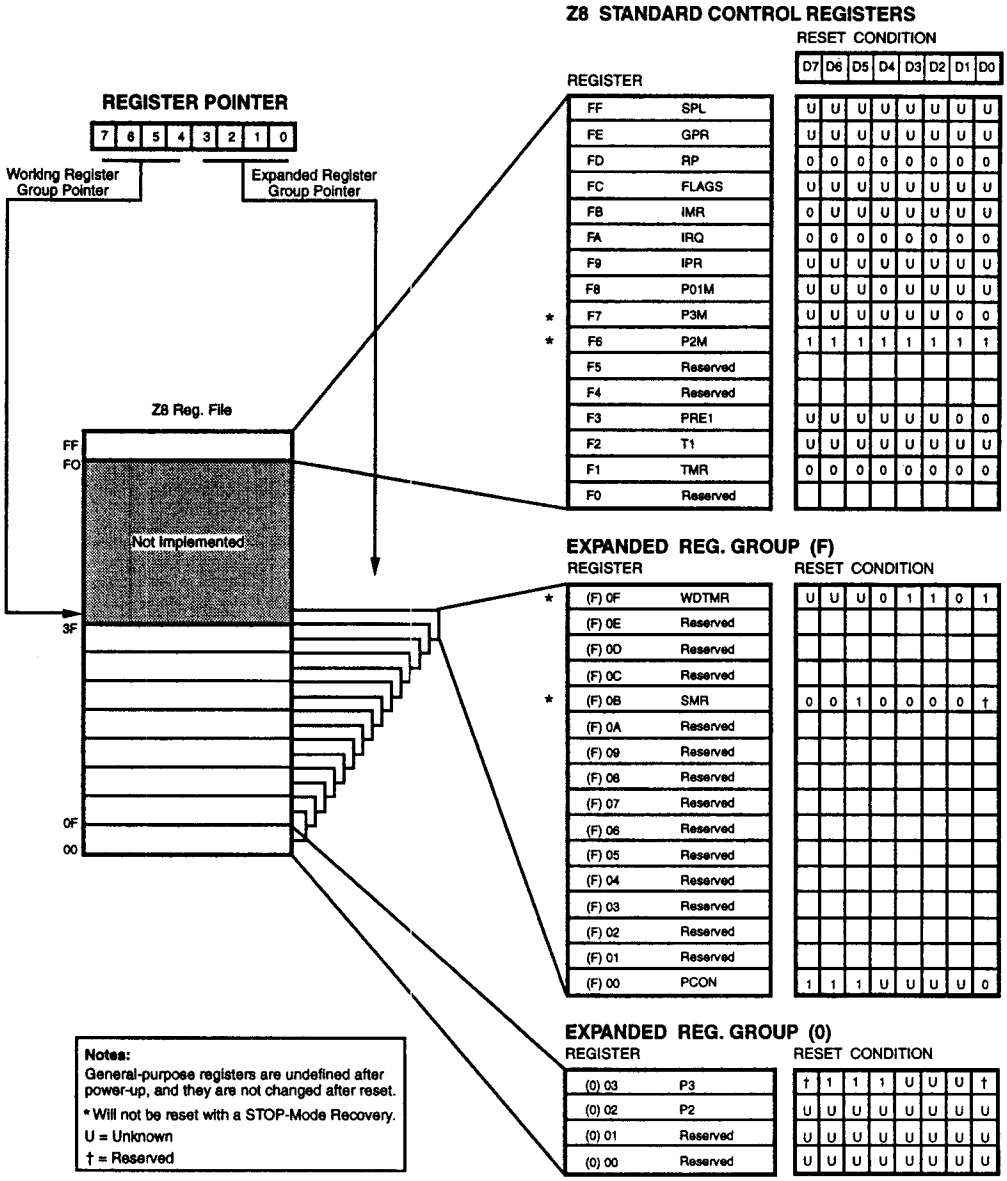



**Figure 7a. Expanded Register File Architecture (Z86E03)**

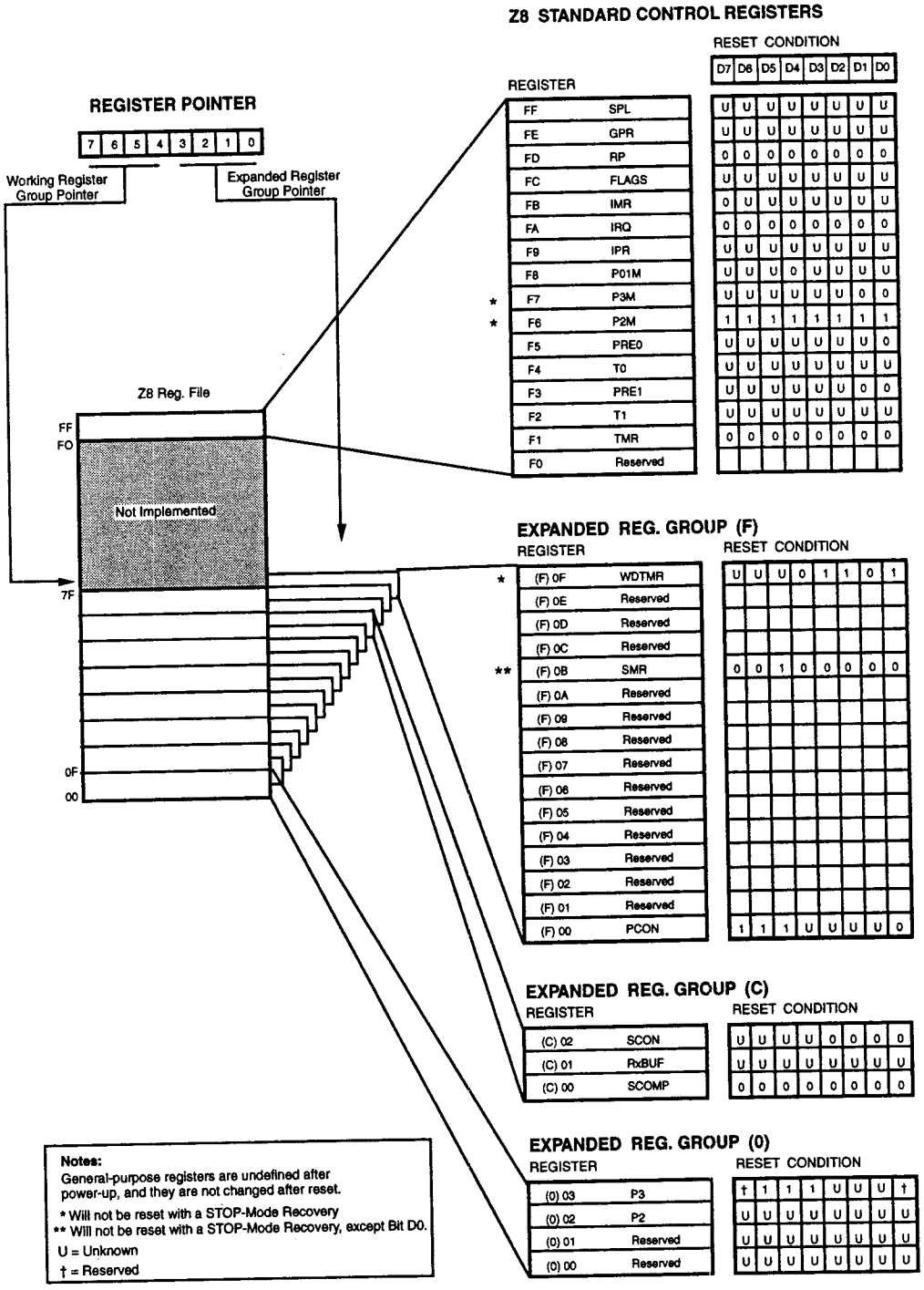



**Figure 7b. Expanded Register File Architecture (Z86E06)**

## FUNCTIONAL DESCRIPTION (Continued)

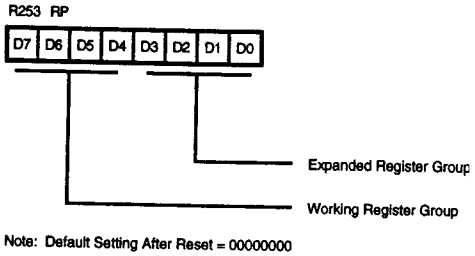



**Figure 8. Register Pointer Register**

**Register File.** The Register File consists of two I/O port registers, 60/124 general-purpose registers, and 13/15 control and status registers. The Z86E03 General-Purpose Register file ranges from address 00 to 3F while the Z86E06 General-Purpose Register file ranges from address 00 to 7F (see Figure 9). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

**General-Purpose Registers (GPR).** These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the $V_{CC}$ voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register.

**Stack.** An 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60/124 general-purpose registers.

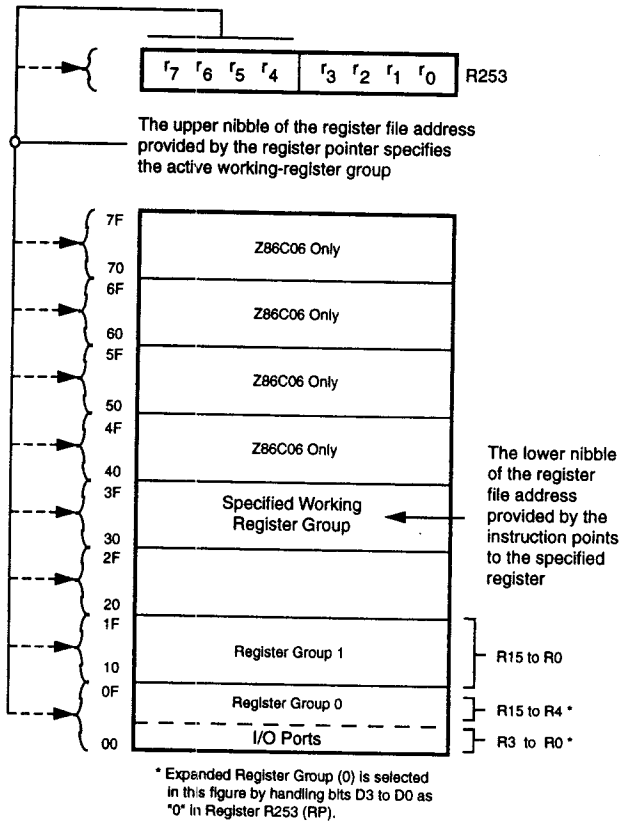



**Figure 9. Register Pointer**

**Counter/Timers.** There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler (Z86E03 only has T1). The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 10).

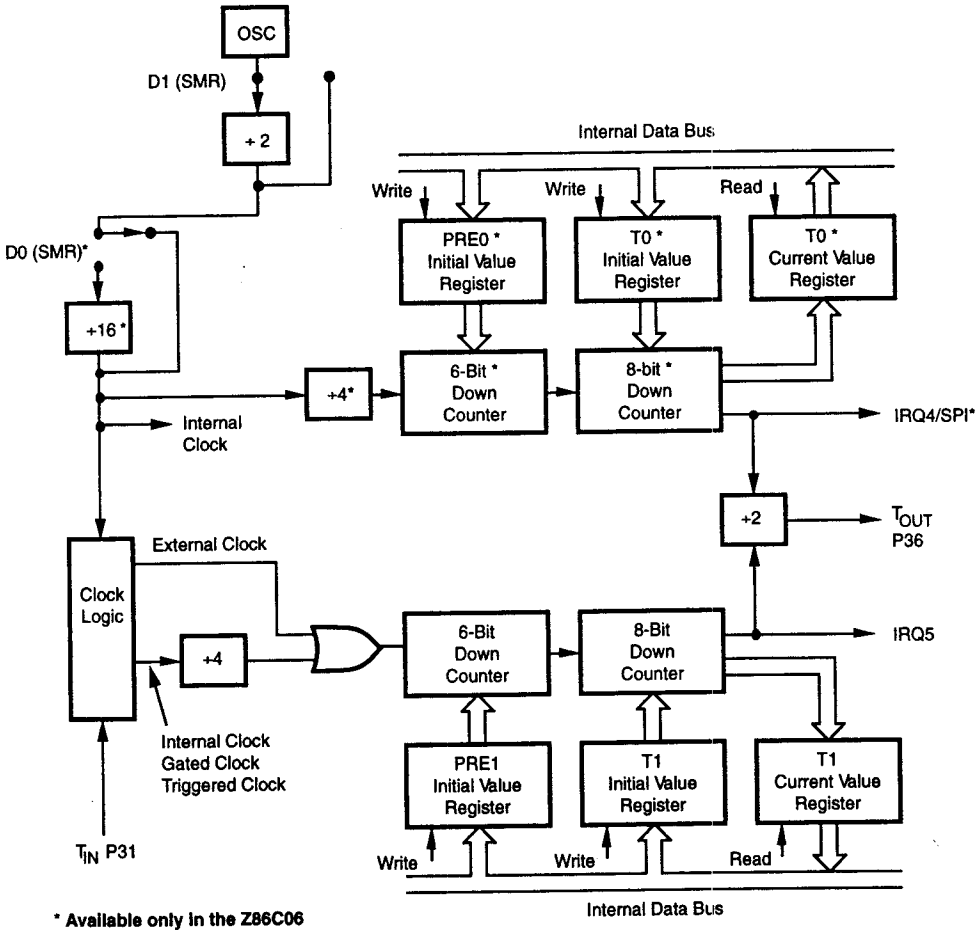



**Figure 10. Counter/Timer Block Diagram**

## FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, RQ4 (T0) or IRQ5 (T1), is generated. Note that IRQ4 is software-generated in the Z86E03.

The counters are programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36 serves as a timer output ($T_{OUT}$) through which T0 (E06 only), T1, or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1 (E06 only). The $T_{IN}$ mode is enabled by setting PRE1 bit D1 (R243) to 0.

**Interrupts.** The Z86E03/E06 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; three sources are claimed by Port 3 lines P31-P33, two sources in the counter/timers, and one source for the SPI. The Interrupt Mask Register globally or singularly enables or disables the six interrupt requests (Table 2).

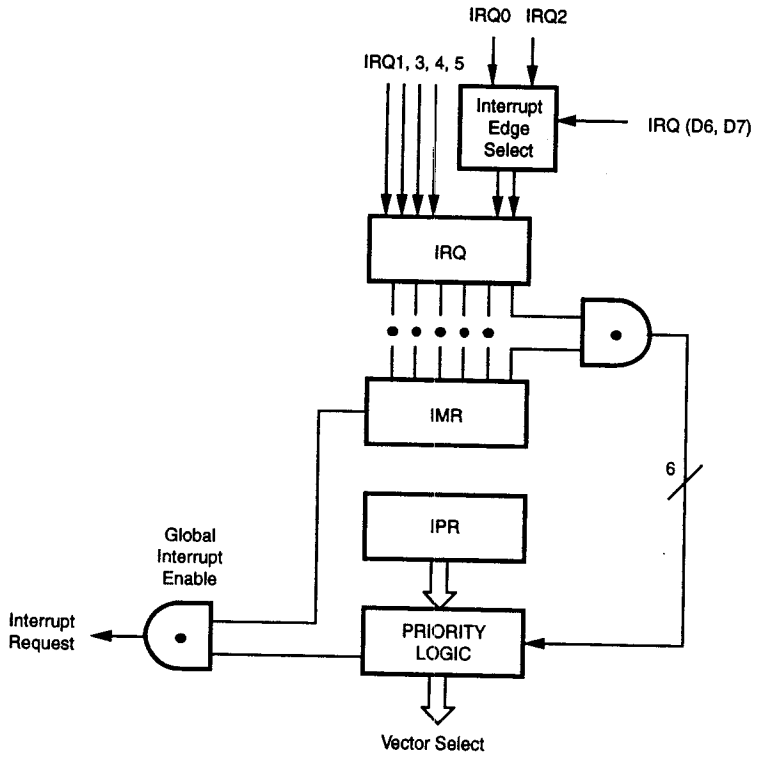



**Figure 11. Interrupt Block Diagram**

**Table 2. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ 0 | IRQ 0 | 0, 1 | External (P32), Rising/Falling Edge Triggered |
| IRQ 1 | IRQ 1 | 2, 3 | External (P33), Falling Edge Triggered |
| IRQ 2 | IRQ 2, $T_{IN}$ | 4,5 | External (P31), Rising/Falling Edge Triggered |
| IRQ 3 | IRQ 3 | 6, 7 | Software Generated, SPI Receive |
| IRQ 4 | T0/IRQ 4 | 8, 9 | Internal for E06 and Software Generated for E03 |
| IRQ 5 | TI | 10, 11 | Internal |

**Note:**
When enabled, the SPI receive interrupt is mapped to IRQ3 in the Z86E06.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E03/E06 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service. In the Z86E06, when the SPI is disabled, IRQ3 has no hardware source but can be invoked by software (write to IRQ3 Register). When the SPI is enabled, an interrupt will be mapped to IRQ3 after a byte of data has been received by the SPI Shift Register.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

The programming bits for the INTERRUPT EDGE SELECT are located in the IRQ register (R250), bits D7 and D6. The configuration is shown in Table 3.

**Table 3. IRQ Register**

| IRQ | | Interrupt Edge | |
|---|---|---|---|
| D7 | D6 | P31 | P32 |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

**Notes:**
F = Falling Edge
R = Rising Edge

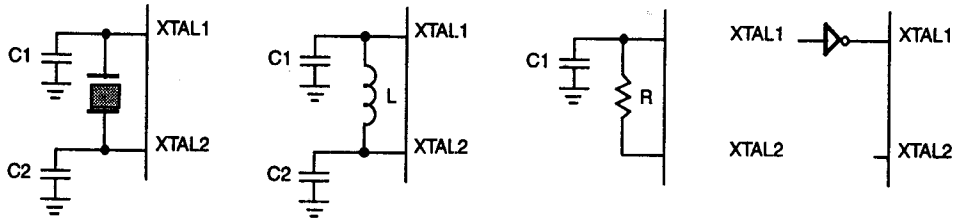
## FUNCTIONAL DESCRIPTION (Continued)

**Clock.** The Z86E03/E06 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 8 MHz/12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values (capacitance between 10 pF to 300 pF) from each pin directly to the device ground (pin 14). The layout is important to reduce ground noise injection.

The RC oscillator option is EPROM-programmable, to be selected by the customer at the time the Z8 is EPROM programmed. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12).

In addition, a special feature has been incorporated into the Z86E03/E06; in low EMI noise mode (bit 7 of PCON register=0) with the RC option selected, the oscillator is targeted to consume considerately less $I_{cc}$ current at frequencies of 10 kHz or less.




Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
F = 8 MHz

LC
C1, C2 = 22 pF
L = 130 µH *
F = 3 MHz

RC
@ 5V Vcc (TYP)
C1 = 33pF*
R = 1kΩ*
F = 9.5 MHz

External Clock

* Preliminary Value Including Pin Parasitics

**Figure 12. Oscillator Configuration**

**Power-On Reset.** A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows $V_{cc}$ and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the three conditions:

- Power-Fail to Power-OK Status
- STOP-Mode Recovery (If D5 of SMR=1)
- WDT Time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

**HALT.** Will turn off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device may be recovered by interrupts either externally or internally generated.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR, SPI compare; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). Note, the crystal remains active in STOP mode if bits 3 and 4 of the WDTMR are enabled. In this mode, only the Watch-Dog Timer runs in STOP mode.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF    NOP   ; clear the pipeline
6F    STOP  ; enter STOP mode
or
FF    NOP   ; clear the pipeline
7F    HALT  ; enter HALT mode
```

**Serial Peripheral Interface (SPI)—Z86E06 Only.** The Z86E06 incorporates a serial peripheral interface for communication with other microcontrollers and peripherals. **The SPI does not exist on the Z86E03.** The SPI includes features such as STOP-Mode Recovery, Master/Slave selection, and Compare mode. Table 4 contains the pin configuration for the SPI feature when it is enabled. The SPI consists of four registers: SPI Control Register (SCON), SPI Compare Register (SCOMP), SPI Receive/Buffer Register (RxBUF), and SPI Shift Register. SCON is located in bank (C) of the Expanded Register Group at address 02.

**Table 4. SPI Pin Configuration**

| Name | Function | Pin Location |
|---|---|---|
| DI | Data-In | P20 |
| DO | Data-Out | P27 |
| SS | Slave Select | P35 |
| SK | SPI Clock | P34 |

The SPI Control Register (SCON) (Figure 13) is a read/write register that controls; Master/Slave selection, interrupts, clock source and phase selection, and error flag. Bit 0 enables/disables the SPI with the default being SPI disabled. A 1 in this location will enable the SPI, and a 0 will disable the SPI. Bits 1 and 2 of the SCON register in Master mode select the clock rate. The user may choose whether internal clock is divide-by-2, -4, -8, or -16. In slave mode, Bit 1 of this register flags the user if an overrun of the RxBUF Register has occurred. The RxCharOverrun flag is only reset by writing a 0 to this bit. In slave mode, bit 2 of the Control Register disables the data-out I/O function. If a 1 is written to this bit, the data-out pin is released to its original port configuration. If a 0 is written to this bit, the SPI shifts out one bit for each bit received. Bit 3 of the SCON Register enables the compare feature of the SPI, with the default being disabled. When the compare feature is enabled, a comparison of the value in the SCOMP Register is made with the value in the RxBUF Register. Bit 4 signals that a receive character is available in the RxBUF Register.

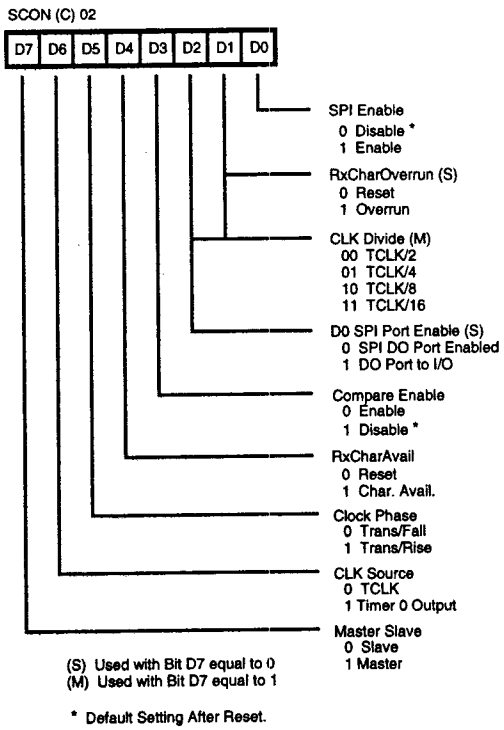



**Figure 13. SPI Control Register (SCON) (Z86E06 Only)**

If the associated IRQ3 is enabled, an interrupt is generated. Bit 5 controls the clock phase of the SPI. A 1 in Bit 5 allows for receiving data on the clock's falling edge and transmitting data on the clock's rising edge. A 0 allows receiving data on the clock's rising edge and transmitting on the clock's falling edge. The SPI clock source is defined in bit 6. A 1 uses Timer0 output for the SPI clock, and a 0 uses TCLK for clocking the SPI. Finally, bit 7 determines whether the SPI is used as a Master or a Slave. A 1 puts the SPI into Master mode and a 0 puts the SPI into Slave mode.

## FUNCTIONAL DESCRIPTION (Continued)

**SPI Operation (Z86E06 only).** The SPI is used in one of two modes: either as system slave, or as system master. Several of the possible system configurations are shown in Figure 14. In the slave mode, data transfer starts when the slave select (SS) pin goes active. Data is transferred into the slave's SPI Shift Register through the DI pin, which has the same address as the RxBUF Register. After a byte of data has been received by the SPI Shift Register, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. The next byte of data will be received at this time. The RxBUF Register must be cleared, or a Receive Character Overrun (RxCharOverrun) flag will be set in the SCON Register, and the data in the RxBUF Register will be overwritten. When the communication between the master and slave is complete, the SS goes inactive.

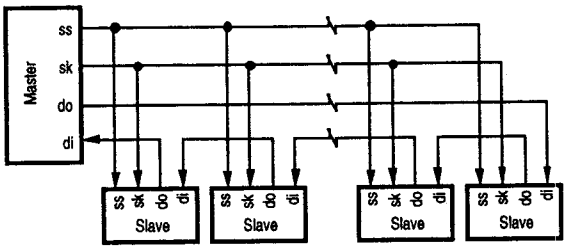
Unless disconnected, for every bit that is transferred into the slave through the DI pin, a bit is transferred out through the DO pin on the opposite clock edge. During slave operation, the SPI clock pin (SK) is an input. In master mode, the CPU must first activate a SS through one of it's I/O ports. Next, data is transferred through the master's DO pin one bit per master clock cycle. Loading data into the shift register initiates the transfer. In master mode, the master's clock will drive the slave's clock. At the conclusion of a transfer, a Receive Character Available (RCA/IRQ3) flag and interrupt is generated. Before data is transferred via the DO pin, the SPI Enable bit in the SCON Register must be enabled.

**SPI Compare (Z86E06 only).** When the SPI Compare Enable bit, D3 of the SCON Register is set to 1, the SPI Compare feature is enabled. The compare feature is only valid for slave mode. A compare transaction begins when the (SS) line goes active. Data is received as if it were a normal transaction, but there is no data transmitted to avoid bus contention with other slave devices. When the compare byte is received, IRQ3 is not generated. Instead, the data is compared with the contents of the SCOMP Register. If the data does not match, DO remains inactive and the slave ignores all data until the (SS) signal is reset. If the data received matches the data in the SCOMP register, then a SMR signal is generated. DO is activated if it is not tri-stated by D2 in the SCON Register, and data is received the same as any other SPI slave transaction.

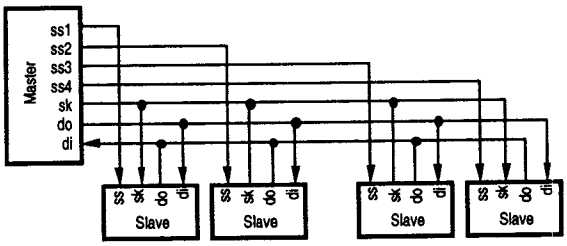
When the SPI is activated as a slave, it operates in all system modes; STOP, HALT, and RUN. Slaves' not comparing remain in their current mode, whereas slaves' comparing wake from a STOP or HALT mode by means of an SMR.

**SPI Clock (Z86E06 only).** The SPI clock maybe driven by three sources: Timer0, a division of the internal system clock, or the external master when in slave mode. Bit D6 of the SCON Register controls what source drives the SPI clock. A 0 in bit D6 of the SCON Register determines the division of the internal system clock if this is used as the SPI clock source. Divide by 2, 4, 8, or 16 is chosen as the scaler.

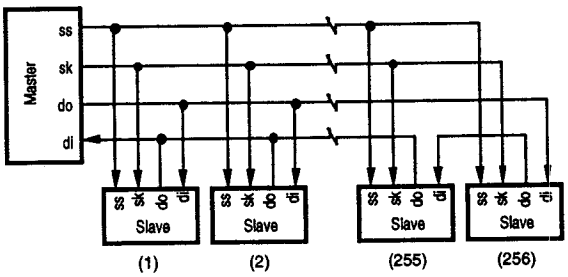
**Standard Serial Setup**




**Standard Parallel Setup**

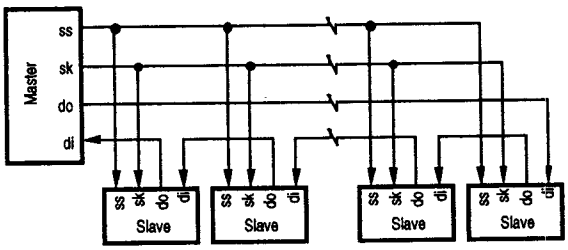



**Setup For Compare**




Up to 256 slaves per SS line

**Three Wire Compare Setup**




Multiple slaves may have the same address.

**Figure 14. SPI System Configuration (Z86E06 Only)**

## FUNCTIONAL DESCRIPTION (Continued)

**Receive Character Available and Overrun (Z86E06 Only).** When a complete data stream is received, an interrupt is generated and the RxCharAvail bit in the SCON Register is set. Bit 4 in the SCON Register is for enabling or disabling the RxCharAvail interrupt. The RxCharAvail bit is available for interrupt polling purposes and is reset when the RxBUF Register is read. RxCharAvail is generated in both master and slave modes. While in slave mode, if the RxBUF is not read before the next data stream is received and loaded into the RxBUF Register, Receive Character Overrun (RxCharOverrun) occurs. Since there is no need for clock control in slave mode, bit D1 in the SPI Contro Register is used to log any RxCharOverrun (Figure 15 and Figure 16).

| No | Parameter | Min | Units |
|---|---|---|---|
| 1 | DI to SK Setup | 10 | ns |
| 2 | SK to D0 Valid | 15 | ns |
| 3 | SS to SK Setup | .5 Tsk | ns |
| 4 | SS to D0 Valid | 15 | ns |
| 5 | SK to DI Hold Time | 10 | ns |

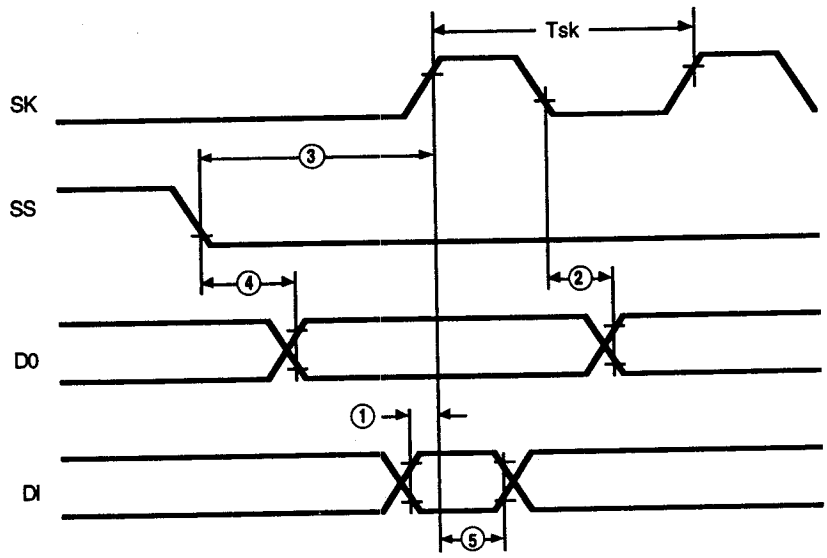



**Figure 15. SPI Timing (Z86E06 Only)**

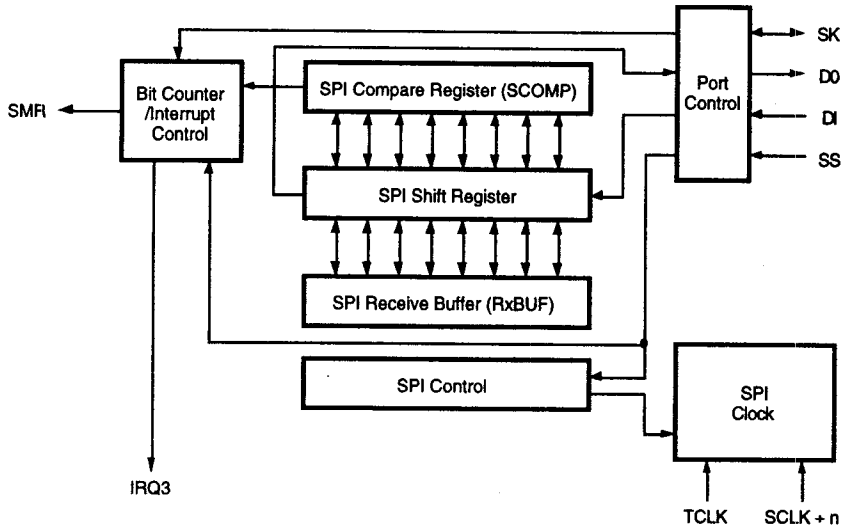



**Figure 16. SPI Logic (Z86E06 Only)**

**PORT Configuration Register (PCON).** The PCON configures the ports individually for comparator output on Port 3, low EMI noise on Ports 2 and 3, and low EMI noise oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 17).

**Comparator Output Port 3 (D0).** Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34, and P35 and a 0 releases the Port to its standard I/O configuration.

**Bits D4-D1.** These bits are reserved and must be 1.

**Low EMI Port 2 (D5).** Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) or configured as a Standard Port by setting D5=1. The default value is 1.

**Low EMI Port 3 (D6).** Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting D6=1. The default value is 1.

**Low EMI OSC (D7).** This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL.

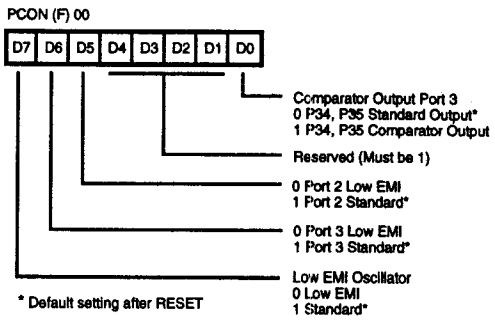



**Figure 17. Port Configuration Register (PCON) (Write Only)**

## FUNCTIONAL DESCRIPTION (Continued)

**STOP-Mode Recovery Register (SMR).** This register selects the clock divide value and determines the mode of STOP-Mode Recovery (Figure 18). All bits are Write Only except bit 7, which is Read Only. Bit 7 is a flag bit that is hardware set on the condition of a STOP recovery and reset on a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. The recovery level must be active Low to work with SPI. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR specify the source of the STOP-Mode Recovery signal. Bit 1 determines whether the XTAL is divided by 1 or 2. A 0 in this location uses XTAL divide-by-two, and a 1 uses XTAL. The default for this bit is XTAL divide-by-two. Bit 0 controls the divide-by-16 prescaler of SCLK/TCLK. The SMR is located in bank F of the Expanded Register Group at address 0BH.

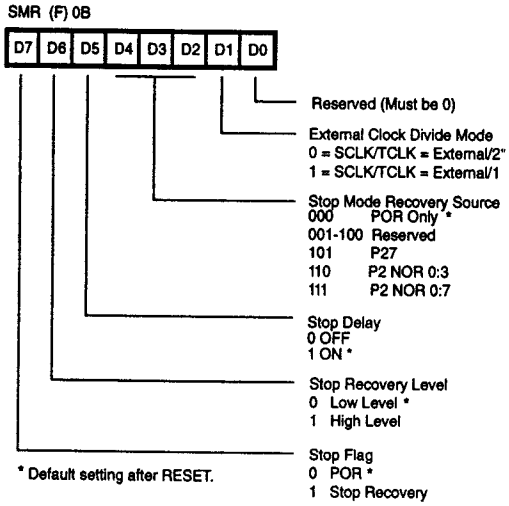



**Figure 18a. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E03)**

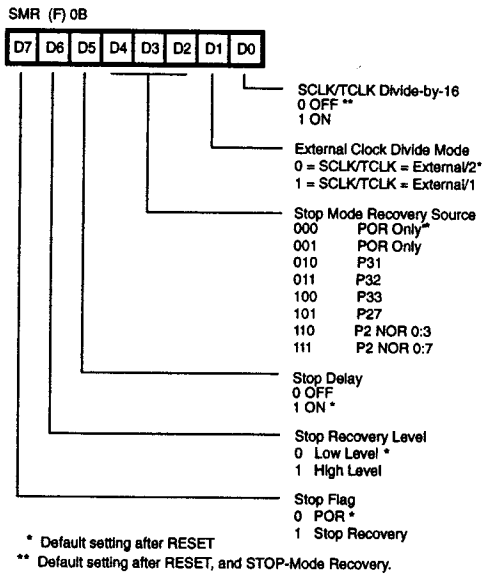



**Figure 18b. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only.) (Z86E06)**

**SCLK/TCLK Divide-by-16 Select (D0)—Z86E06 Only.** D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources the counter/timers and interrupt logic).

**External Clock Divide Mode (D1).** This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit, together with D7 of PCON, helps further lower EMI [i.e., D7 (PCON)=0, D1 (SMR=1]. The default setting is 0.

**STOP-Mode Recovery Source (D2,D3,D4).** These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 19 and Table 5).

**Table 5. STOP-Mode Recovery Source**

| SMR D4 | SMR D3 | SMR D2 | Operation Description of Action |
|---|---|---|---|
| 0 | 0 | 0 | POR recovery only |
| 0 | 0 | 1 | POR recovery only (E03 = Reserved) |
| 0 | 1 | 0 | P31 transition (E03 = Reserved) |
| 0 | 1 | 1 | P32 transition (E03 = Reserved) |
| 1 | 0 | 0 | P33 transition (E03 = Reserved) |
| 1 | 0 | 1 | P27 transition |
| 1 | 1 | 0 | Logical NOR of Port 2 bits 0:3 |
| 1 | 1 | 1 | Logical NOR of Port 2 bits 0:7 |

P31-P33 cannot wake up from STOP Mode if the input lines are configured as analog inputs. In the Z86E06, when the SPI is enabled and the Compare feature is active, a SMR is generated upon a comparison in the SPI Shift Register and SCOMP Register, regardless of the above SMR Register settings. If SPI Compare is used to wake up the part from STOP Mode, it is still possible to have one of the other STOP-Mode Recovery sources active. **Note:** These other STOP- Mode Recovery sources must be active level Low (bit D6 in SMR set to 0 if P31, P32, P33, and P27 selected, or bit D6 in SMR set to 1 if logical NOR of Port 2 is selected).

**STOP-Mode Recovery Delay Select (D5).** This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

**STOP-Mode Recovery Level Select (D6).** A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the device from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 19).

**Cold or Warm Start (D7).** This bit is set by the device upon entering STOP Mode. It is active High, and is 0 (cold) on POR/WDT RESET. This bit is Read Only. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

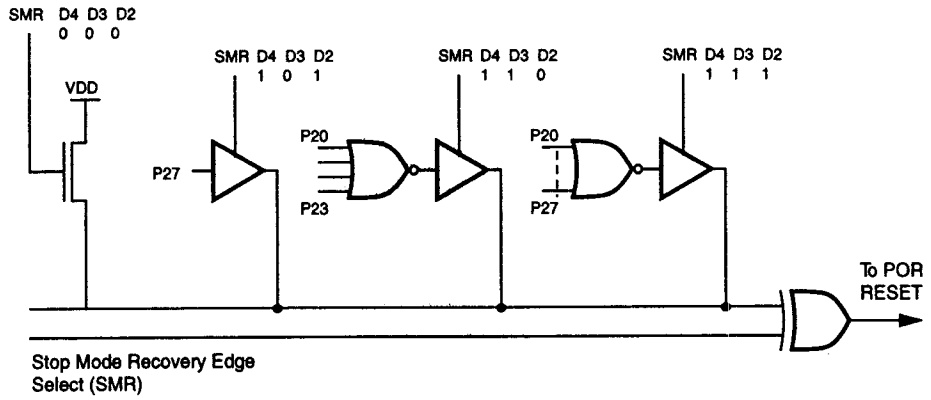
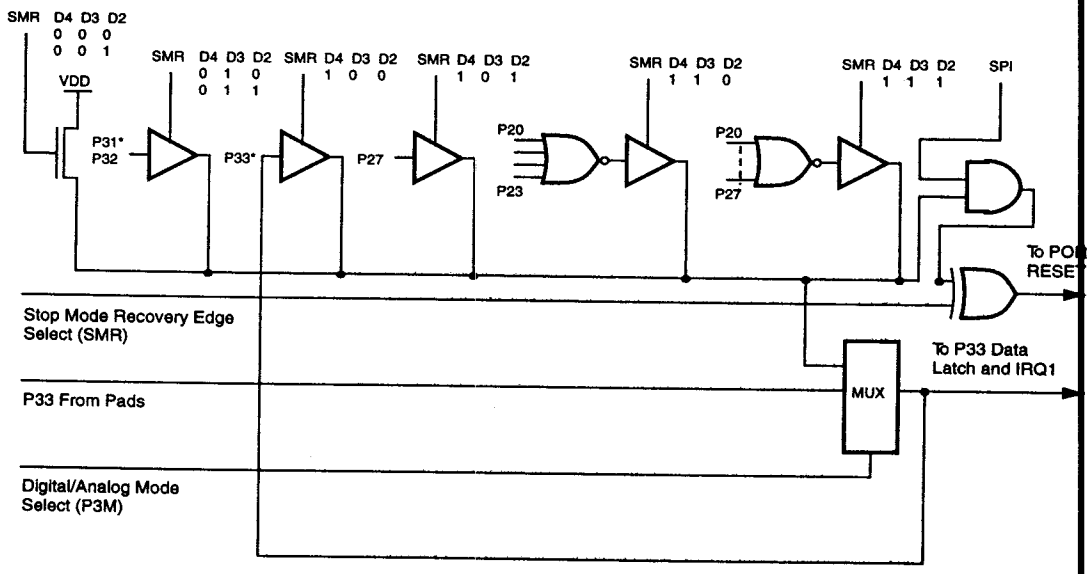



**Figure 19a. STOP Mode Recovery Source (Z86E03)**

## FUNCTIONAL DESCRIPTION (Continued)



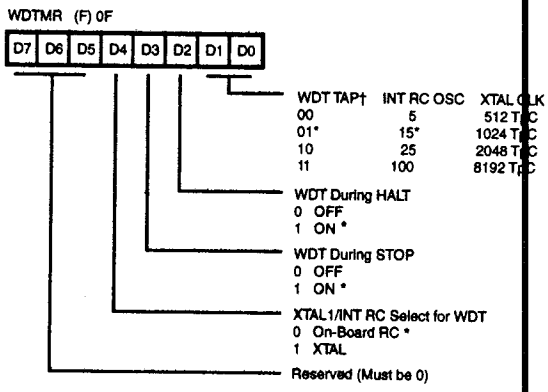

*Note: P31, P32 and P33 are not in Analog Mode.

**Figure 19b. STOP-Mode Recovery Source (Z86E06)**

**Watch-Dog Timer Mode Register (WDTMR).** The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDTMR register.

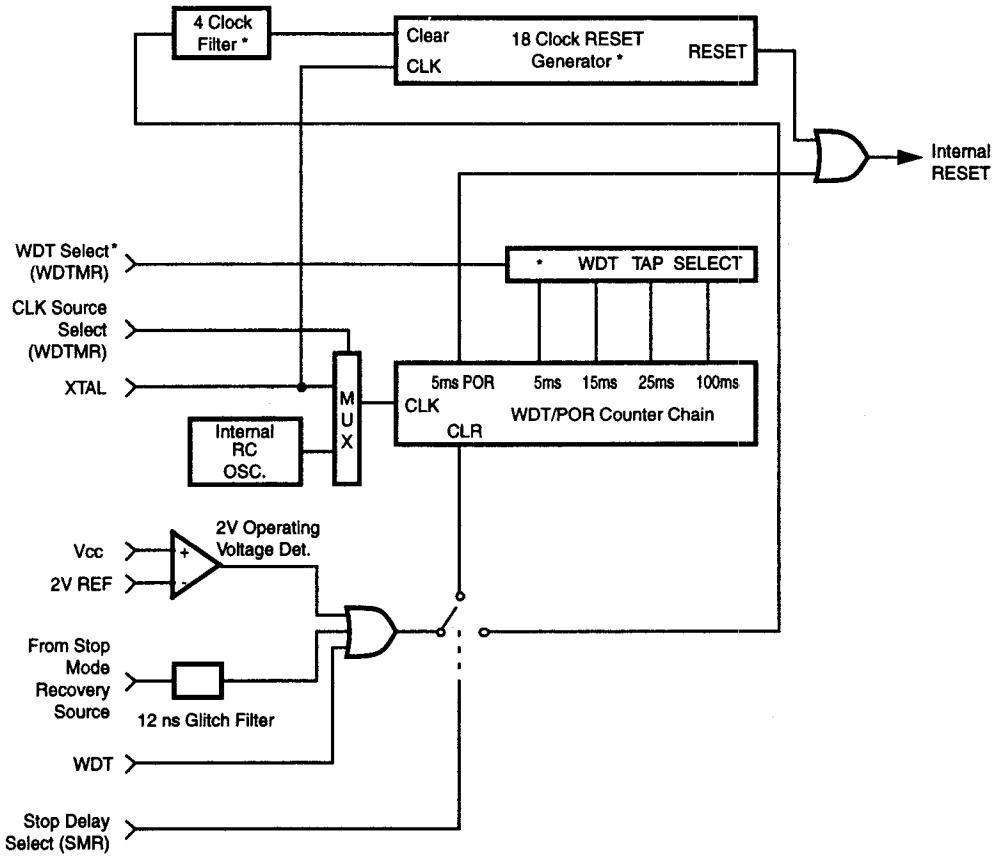
**Note:** Execution of the WDT instruction affects the Z (zero), S (sign), and V (overflow) flags.

Bits 0 and 1 control a tap circuit that determines the timeout period (on Z86E06 only). Bit 2 determines whether the WDT is active during HALT and bit 3 determines WDT activity during STOP. If bits 3 and 4 of this register are both set to 1, the WDT is only driven by the external clock during STOP mode. This feature makes it possible to wake up from STOP mode from an internal source. Bits 5 through 7 of the WDTMR are reserved (Figure 20). ***This register is accessible only during the first 64 internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Reset or a STOP Mode Recovery (Figure 21). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH.***




* Default setting after RESET
† Must be 01 for Z86E03

**Figure 20. Watch-Dog Timer Mode Register (Write Only)**




* Not available on the Z86E03, WDT fixed at 15 ms/1024TpC in the Z86E03.

**Figure 21. Resets and WDT**

## FUNCTIONAL DESCRIPTION (Continued)

**WDT Time Select (D1,D0).** Bits 0 and 1 control a tap circuit that determines the time-out period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively. These select bits are present in the Z86E06 only.

**Table 6. Time-Out Period of the WDT (Z86E06 Only)**

| D1 | D0 | Time-Out of Internal RC OSC | Time-Out of XTAL Clock |
|---|---|---|---|
| 0 | 0 | 5 ms min | 256TpC |
| 0 | 1 | 15 ms min | 512TpC |
| 1 | 0 | 25 ms min | 1024TpC |
| 1 | 1 | 100 ms min | 4096TpC |

**Notes:**
TpC = XTAL clock cycle
The default on reset is 15 ms, D0 = 1 and D1 = 0.
The values given are for $V_{CC}$ = 5.0V

For the Z86E03, the WDT time-out value is fixed at 1024 TpC (depending on WDTMR bit D4) period. When writing to the WDTMR in the Z86E03, bit D0 must be 1 and D1 must be 0.

**WDT During HALT (D2).** This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

**WDT During STOP (D3).** This bit determines whether or not the WDT is active during STOP mode. Since XTAL clock is stopped during STOP Mode, unless as specified below, the on-board RC must be selected as the clock source to the POR counter. A 1 indicates active during STOP. The default is 1. If bits D3 and D4 are both set to 1, the WDT only, is driven by the external clock during STOP mode.

**Clock Source for WDT (D4).** This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the internal RC oscillator.

**Bits 5, 6 and 7.** These bits are reserved.

**$V_{CC}$ Voltage Comparator.** An on-board Voltage Comparator checks that $V_{CC}$ is at the required level to ensure correct operation of the device. Reset is globally driven if $V_{CC}$ is below the specified voltage (typically 2.6V).

**Low Voltage Protection ($V_{LV}$).** The Low Voltage Protection trip point ($V_{LV}$) will be less than 3 volts and above 1.8 volts under the following conditions.

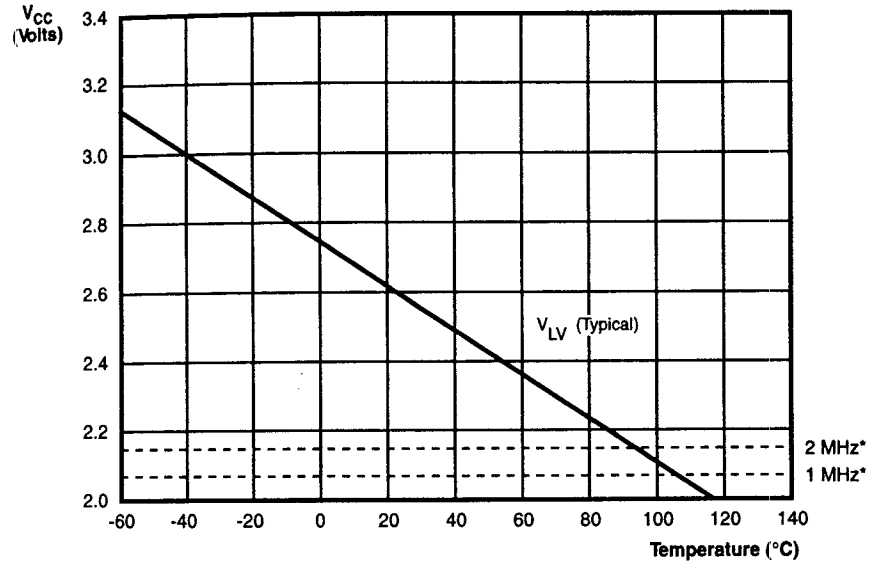
Maximum ($V_{LV}$) Conditions:

**Case 1:** $T_A$ = –40° to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz

**Case 2:** $T_A$ = –40° to +85°C, Internal Clock (SCLK) Frequency equal or less than 2 MHz

**Note:** The internal clock frequency (SCLK) is determined by SMR (F) 0BH bit D1.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device is guaranteed to function normally until the Low Voltage Protection trip point ($V_{LV}$) is reached, for the temperatures and operating frequencies in cases 1 and 2 above. The actual low voltage trip point is a function of temperature and process parameters (Figure 22).




Note: * The typical minimum operating Vcc voltage at that frequency.

**Figure 22. Typical Z86E03/E06 $V_{LV}$ Voltage vs Temperature**

## SPECIAL FUNCTIONS
### EPROM Mode

Besides $V_{DD}$ and GND ($V_{SS}$), the Z86E03/E06 changes all its pin functions in the EPROM mode. XTAL2 has no function, XTAL1 functions as /CE, P31 functions as /OE, P32 functions as EPM, P33 functions as $V_{PP}$, and P02 functions as /PGM.

**EPROM Protect.** ROM protect is EPROM-programmable. It is selected by the customer at the time the ROM code is EPROM programmed. The selection of ROM Protect disables the LDC and LDCI instructions in all modes. A ROM look-up table cannot be used in this mode.

### Application Caution

Please note that when using the device in a noisy enviro ment, it is suggested that the voltages on the EP /CE, /OE pins be clamped to $V_{CC}$ through a diode to $V_{CC}$ prevent accidentally entering the OTP mode. The requires both a diode and a 100 pF capacitor.

**User Modes.** Table 7 shows the programming voltage each mode of Z86E06.

**Table 7. OTP Programming Table**

| Programming Modes | $V_{PP}$ | EPM | /CE | /OE | /PGM | ADDR | DATA | $V_{CC}$* |
|---|---|---|---|---|---|---|---|---|
| EPROM READ1 | X | $V_H$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADDR | Out | 4.5V |
| EPROM READ2 | X | $V_H$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADDR | Out | 5.5V |
| PROGRAM | $V_H$ | X | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | ADDR | In | 6.0V |
| PROGRAM VERIFY | $V_H$ | X | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | ADDR | Out | 6.0V |
| EPROM PROTECT | $V_H$ | $V_H$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.0V |
| PERMANENT WDT ENABLED | $V_H$ | $V_{IH}$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.0V |
| GLOBAL AUTO LATCH DISABLED | $V_H$ | $V_{IH}$ | $V_H$ | $V_{IL}$ | $V_{IL}$ | NU | NU | 6.0V |
| RC OSCILLATOR | $V_H$ | $V_{IL}$ | $V_H$ | $V_{IH}$ | $V_{IL}$ | NU | NU | 6.0V |

**Notes:**
In EPROM Mode, all Z8 inputs are TTL inputs.
$V_H$ = 12.5V ±0.5V
$V_{IH}$ = As per specific Z8 DC specification.
$V_{IL}$ = As per specific Z8 DC specification.
X = Not used, but must be set to $V_H$, $V_{IH}$, or $V_{IL}$ level.
NU = Not used, but must be set to either $V_{IH}$ or $V_{IL}$ level.
$I_{PP}$ during programming = 40 mA maximum.
$I_{CC}$ during programming, verify, or read = 40 mA maximum.
* $V_{CC}$ has a tolerance of ±0.25V.



PS0201001-0603

**Internal Address Counter.** The address of Z86E03/E06 is generated internally with a counter clocked through pin P01 (Clock). Each clock signal increases the address by one and the high level of pin P00 (Clear) will reset the address to zero. Figure 16 shows the setup time of the serial address input.

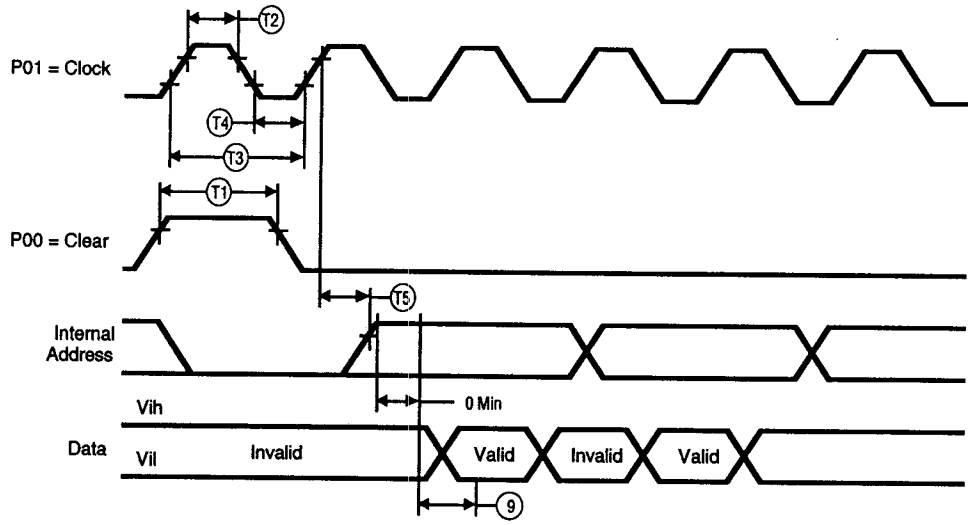
**Programming Waveform.** Figures 24, 25 and 26 show the programming waveforms of each mode. Table 7 shows the timing of programming waveforms.

**Programming Algorithm.** Figure 27 shows the flow chart of the Z86E03/E06 programming algorithm.

**Table 8. Timing of Programming Waveforms**

| Parameters | Name | Min | Max | Units |
|---|---|---|---|---|
| 1 | Address Setup Time | 2 | | µs |
| 2 | Data Setup Time | 2 | | µs |
| 3 | $V_{PP}$ Setup | 2 | | µs |
| 4 | $V_{CC}$ Setup Time | 2 | | µs |
| 5 | Chip Enable Setup Time | 2 | | µs |
| 6 | Program Pulse Width | 0.95 | | ms |
| 7 | Data Hold Time | 2 | | µs |
| 8 | /OE Setup Time | 2 | | µs |
| 9 | Data Access Time | | 200 | ns |
| 10 | Data Output Float Time | | 100 | ns |
| 11 | Overprogram Pulse Width | 2.85 | | ms |
| 12 | EPM Setup Time | 2 | | µs |
| 13 | /PGM Setup Time | 2 | | µs |
| 14 | Address to /OE Setup Time | 2 | | µs |
| 15 | Option Program Pulse Width | 78 | | ms |

## SPECIAL FUNCTIONS (Continued)
### EPROM Mode




| Legend: | |
|---|---|
| T1 Reset Clock Width | 30 ns Min |
| T2 Input Clock High | 30 ns Min |
| T3 Input Clock Period | 70 ns Min |
| T4 Input Clock Low | 30 ns Min |
| T5 Clock to Address Counter Out Delay | 15 ns Max |

**Figure 23. Z86E03/E06 Address Counter Waveform**

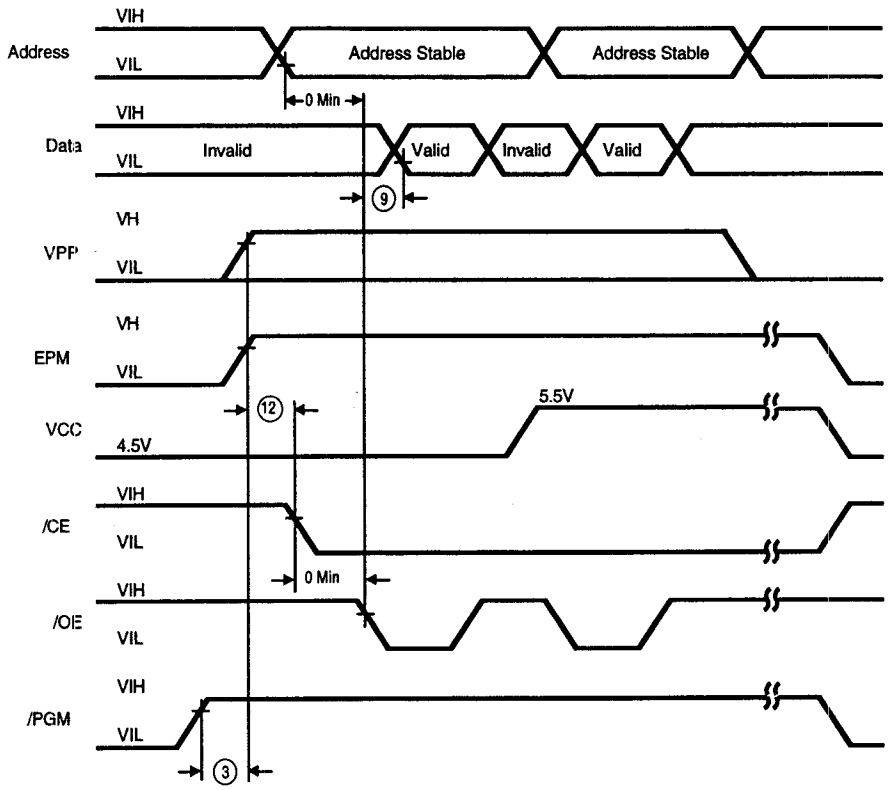



**Figure 24. Z86E03/E07 Programming Waveform (EPROM Read)**

## SPECIAL FUNCTIONS (Continued)
### EPROM Mode

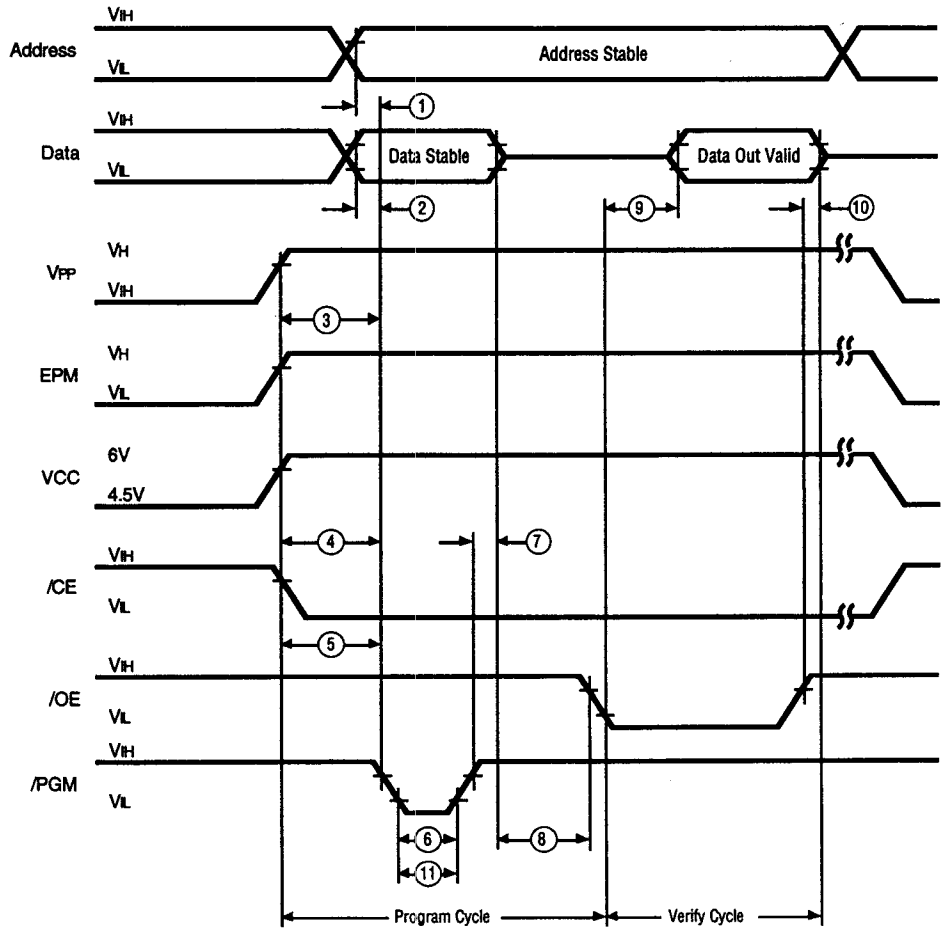



**Figure 25. Z86E03/E06 Programming Waveform (Program and Verify)**

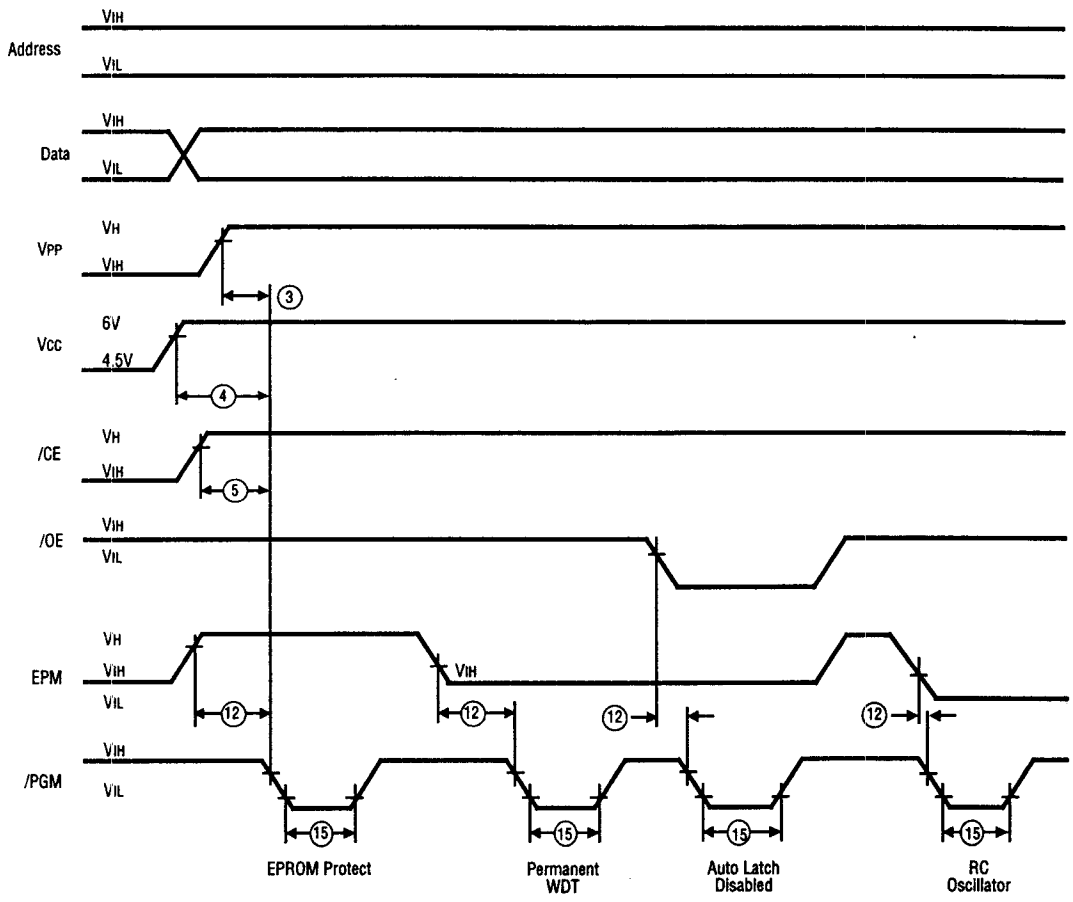



**Figure 26. Z86E03/E06 Programming Waveform (EPROM Protect and Low EMI Program)**

**SPECIAL FUNCTIONS** (Continued)
**EPROM Mode**

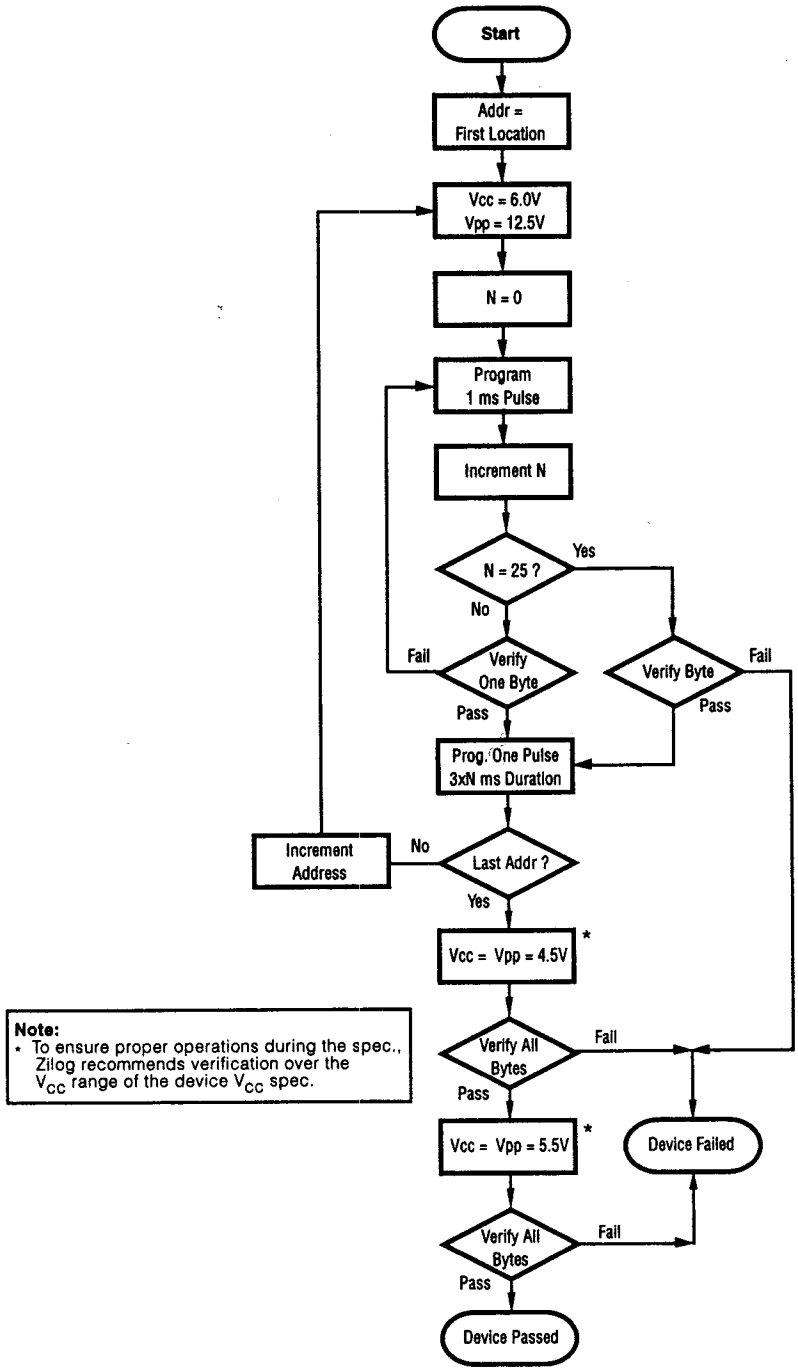



**Figure 27. Z86E03/E06 Programming Algorithm**

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage* | –0.3 | +7.0 | V |
| $V_{IHM}$ | Max Input Voltage** | | 12 | V |
| $T_{STG}$ | Storage Temp | –65 | +150 | °C |
| $T_A$ | Oper Ambient Temp | † | | °C |

**Notes:**
* Voltage on all pins with respect to GND.
** Applies to Port pins only and must limit current going into or out of Port pins to 250 µA maximum.
† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 28).

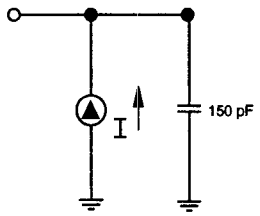



**Figure 28. Test Load Configuration**

## CAPACITANCE

$T_A$ = 25° C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

| Parameter | Min | Max |
|---|---|---|
| Input Capacitance | 0 | 12 pF |
| Output Capacitance | 0 | 20 pF |
| I/O Capacitance | 0 | 25 pF |

## $V_{CC}$ SPECIFICATION

$V_{CC}$ = 3.0V to 5.5V

## DC ELECTRICAL CHARACTERISTICS
Z86E03/E06

| Symbol | Parameter | $V_{CC}$ Note [3] | $T_A$ = 0°C to +70°C Min | Max | $T_A$ = −40°C to +105°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CH}$ | Clock Input High Voltage | 3.3V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | 2.4 | V | Driven by External Clock Generator | |
| | | 5.0V | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | 0.9 $V_{CC}$ | $V_{CC}$+0.3 | 3.9 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 3.3V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.6 | V | Driven by External Clock Generator | |
| | | 5.0V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 2.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 3.3V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | | |
| | | 5.0V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 3.3V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.0 | V | | |
| | | 5.0V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 3.3V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 3.1 | V | $I_{OH}$ = -2.0 mA | [10] |
| | | 5.0V | $V_{CC}$–0.4 | | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = -2.0 mA | [10] |
| $V_{OL1}$ | Output Low Voltage | 3.3V | | 0.8 | | 0.8 | 0.2 | V | $I_{OL}$ = +4.0 mA | [10] |
| | | 5.0V | | 0.4 | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | [10] |
| $V_{OL2}$ | Output Low Voltage | 3.3V | | 1.0 | | 1.0 | 0.4 | V | $I_{OL}$ = + 6 mA, 3 Pin Max | [10] |
| | | 5.0V | | 1.0 | | 1.0 | 0.5 | V | $I_{OL}$ = +12 mA, 3 Pin Max | [10] |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 3.3V | | ±10 | | ±10 | ±5 | mV | | |
| | | 5.0V | | ±10 | | ±10 | ±5 | mV | | |
| $V_{ICR}$ | Input Common Mode Voltage Range | 3.3V | 0V | $V_{CC}$–1.0v | 0V | $V_{CC}$–1.5v | | | | [7] |
| | | 5.0V | 0V | $V_{CC}$–1.0v | 0V | $V_{CC}$–1.5v | | | | [7] |
| $I_{IL}$ | Input Leakage | 3.3V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.0V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 3.3V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.0V | –1.0 | 1.0 | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{CC}$ | Supply Current | 3.3V | | 6 | | 6 | 3.0 | mA | @ 8 MHz | [4,5,12] |
| | | 5.0V | | 11.0 | | 11.0 | 6.0 | mA | @ 8 MHz | [4,5,12] |
| | | 3.3V | | 8.0 | | 8.0 | 4.5 | mA | @ 12 MHz | [4,5,10,13] |
| | | 5.0V | | 15 | | 15 | 9.0 | mA | @ 12 MHz | [4,5,10,13] |
| $I_{OB}$ | Input Bias Current | 3.3V | | 300 | | 300 | | nA | | [7] |
| | | 5.0V | | 300 | | 300 | | nA | | [7] |
| $I_{IO}$ | Input Offset Current | 3.3V | | +150 | | +150 | | nA | | [7] |
| | | 5.0V | | +150 | | +150 | | nA | | [7] |

| Symbol | Parameter | $V_{CC}$ Note [3] | $T_A$ = 0°C to +70°C Min | Max | $T_A$ = −40°C to +105°C Min | Max | Typical @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OL3}$ | P36 | 5.0V | | 1.0 | | 1.0 | | V | $I_{OL}$ = 24 mA | |
| $I_{CC1}$ | Standby Current | 3.3V | | 3.0 | | 3.0 | 1.3 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | [4, 5,12] |
| | | 5.0V | | 5 | | 5 | 3.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | [4, 5,12] |
| | | 3.3V | | 4.5 | | 4.5 | 2.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | [4,5,13] |
| | | 5.0V | | 7.0 | | 7.0 | 4.0 | mA | HALT Mode $V_{IN}$ = 0V, $V_{CC}$ @ 12 MHz | [4,5,13] |
| | | 3.3V | | 1.4 | | 1.4 | 0.7 | mA | Clock Divide-by-16 @ 8 MHz | [4, 5,12] |
| | | 5.0V | | 3.5 | | 3.5 | 2.0 | mA | Clock Divide-by-16 @ 8 MHz | [4, 5,12] |
| | | 3.3V | | 2.0 | | 2.0 | 1.0 | mA | Clock Divide-by-16 @ 12 MHz | [4, 5,13] |
| | | 5.0V | | 4.5 | | 4.5 | 2.5 | mA | Clock Divide-by-16 @ 12 MHz | [4, 5,13] |
| | | 5.0V | | 1.0 | | 1.0 | | mA | HALT Mode @ 12 kHz | [4,5,11,13] |
| $I_{CC2}$ | Standby Current | 3.0V | | 10 | | 20 | 1.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | [6, 9] |
| | | 5.0V | | 10 | | 20 | 3.0 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | [6, 9] |
| | | 3.3V | | 600 | | 600 | 400 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is Running | [6, 9,12] |
| | | 5.0V | | 1000 | | 1000 | 800 | µA | STOP Mode $V_{IN}$ = 0V, $V_{CC}$ WDT is Running | [6, 9,12] |
| $I_{ALL}$ | Auto Latch Low Current | 3.3V | | 7.0 | | 14.0 | 4.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.0V | | 20.0 | | 30.0 | 10 | µA | $0V < V_{IN} < V_{CC}$ | |
| $I_{ALH}$ | Auto Latch High Current | 3.3V | | −4.0 | | −8.0 | −2.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| | | 5.0V | | −9.0 | | −16.0 | −5.0 | µA | $0V < V_{IN} < V_{CC}$ | |
| $T_{POR}$ | Power-On Reset | 3.3V | 7 | 24 | 6 | 25 | 13 | ms | | |
| | | 5.0V | 3 | 13 | 2 | 14 | 7 | ms | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Protection Voltage | | 2.2 | 2.8 | 1.7 | 3.0 | 2.6 | V | 6 MHz max Int. CLK Freq. | [3] |

**Notes:**

[1] $I_{CC1}$

| | Typ | Max | Unit | Freq |
|---|---|---|---|---|
| Clock Driven on XTAL | 0.3 | 5.0 | mA | 8 MHz |
| Crystal or Ceramic Resonator | 3.0 | 5.0 | mA | 8 MHz |

[2] $V_{SS}$ = 0V = GND

[3] $V_{CC}$ = 3.0V to 5.5V. The $V_{LV}$ increases as the temperature decreases. Typical values measured at 3.3V and 5.0V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] $C_{L1} = C_{L2}$ = 100 pF

[6] Same as note [4] except inputs at $V_{CC}$.

[7] For analog comparator inputs when analog comparators are enabled.

[8] Excludes clock pins.

[9] Clock must be forced Low when XTAL1 is clock-driven and XTAL2 is floating.

[10] STD mode (not low EMI mode).

[11] Low EMI Oscillator enabled.

[12] Z86E03 only.

[13] Z86E06 only.

## AC ELECTRICAL CHARACTERISTICS
Z86E03/E06

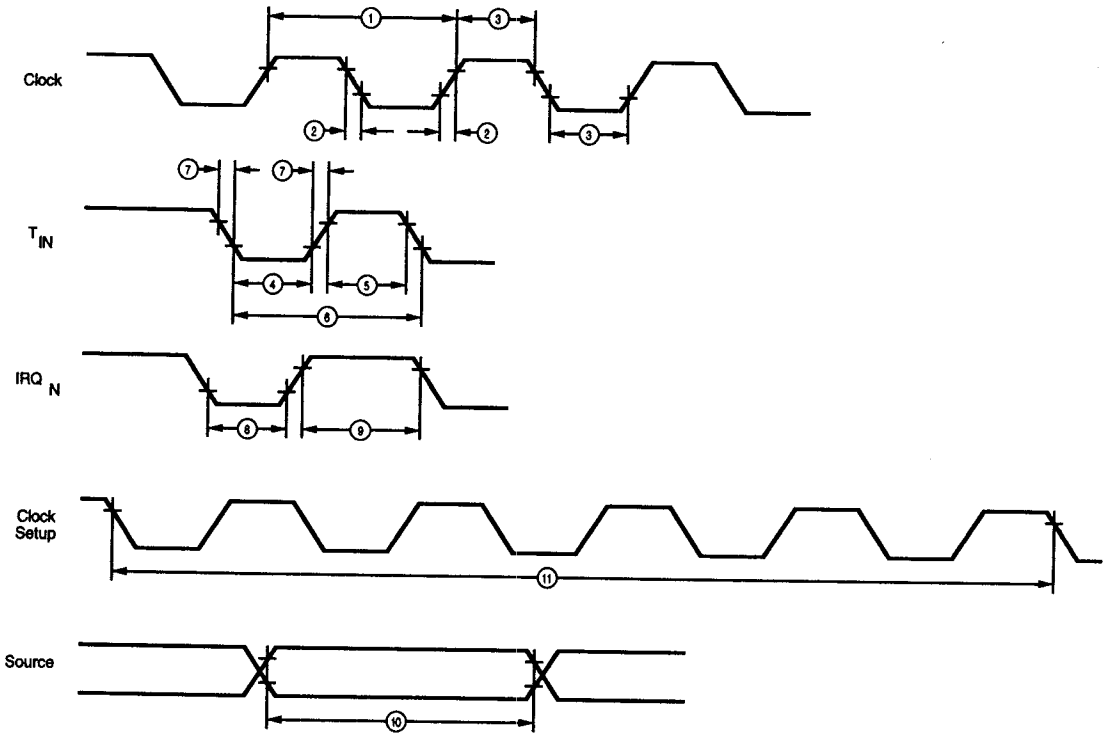



**Figure 29. Additional Timing**

## AC ELECTRICAL CHARACTERISTICS
(SCLK/TCLK = EXTERNAL/2)

| | | | | $T_A$ = 0°C To +70°C | | | | $T_A$ = −40°C To +105°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ | 8 MHz [11] | | 12 MHz [11] | | 8 MHz [11] | | 12 MHz [11] | | | |
| No | Symbol | Parameter | Note[3] | Min | Max | Min | Max | Min | Max | Min | Max | Units | Notes |
| 1 | TpC | Input Clock Period | 3.0V | 125 | DC | 83 | DC | 125 | DC | 83 | DC | ns | [1,7,8] |
| | | | 5.5V | 125 | DC | 83 | DC | 125 | DC | 83 | DC | ns | [1,7,8] |
| 2 | TrC,TfC | Clock Input Rise | 3.0V | | 25 | | 15 | | 25 | | 15 | ns | [1,7,8] |
| | | and Fall Times | 5.5V | | 25 | | 15 | | 25 | | 15 | ns | [1,7,8] |
| 3 | TwC | Input Clock Width | 3.0V | 62 | | 41 | | 62 | | 41 | | ns | [1,7,8] |
| | | | 5.5V | 62 | | 41 | | 62 | | 41 | | ns | [1,7,8] |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | [1,7,8] |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | [1,7,8] |
| 5 | TwTinH | Timer Input High Width | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,7,8] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,7,8] |

## AC ELECTRICAL CHARACTERISTICS (Continued)
(SCLK/TCLK = EXTERNAL/2)

| No | Symbol | Parameter | $V_{CC}$ Note [3] | $T_A$ = 0°C TO +70°C 8 MHz[11] Min | Max | 12 MHz[11] Min | Max | $T_A$ = –40°C TO +105°C 8 MHz[11] Min | Max | 12 MHz[11] Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | TpTin | Timer Input Period | 3.0V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | [1,7,8] |
| | | | 5.5V | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | [1,7,8] |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Timer | 3.0V | | 100 | | 100 | | 100 | | 100 | ns | [1,7,8] |
| | | | 5.5V | | 100 | | 100 | | 100 | | 100 | ns | [1,7,8] |
| 8 | TwIL | Int. Request Input Low Time | 3.0V | 100 | | 100 | | 100 | | 100 | | ns | [1,2,7,8] |
| | | | 5.5V | 70 | | 70 | | 70 | | 70 | | ns | [1,2,7,8] |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,2,7,8] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [1,2,7,8] |
| 10 | Twsm | STOP Mode Recovery Width Spec | 3.0V | 12 | | 12 | | 12 | | 12 | | | [1,8,10] |
| | | | 5.5V | 12 | | 12 | | 12 | | 12 | | | [1,8,10] |
| 11 | Tost | Oscillator Startup Time | 3.0V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | ns | [1,3,4,9] |
| | | | 5.5V | 5TpC | | 5TpC | | 5TpC | | 5TpC | | ns | [1,3,4,9] |
| 12 | Twdt | Watch-Dog Timer Refresh Time | 3.0V | 15 | | 15 | | 12 | | 12 | | ms | D0 = 0 [5,6] |
| | | | 5.5V | 5 | | 5 | | 3 | | 3 | | ms | D1 = 0 [5,6] |
| | | | 3.0V | 30 | | 30 | | 25 | | 25 | | ms | D0 = 1 [5,6] |
| | | | 5.5V | 16 | | 16 | | 12 | | 12 | | ms | D1 = 0 [5,6] |
| | | | 3.0V | 60 | | 60 | | 50 | | 50 | | ms | D0 = 0 [5,6] |
| | | | 5.5V | 25 | | 25 | | 30 | | 30 | | ms | D1 = 1 [5,6] |
| | | | 3.0V | 250 | | 250 | | 200 | | 200 | | ms | D0 = 1 [5,6] |
| | | | 5.5V | 120 | | 120 | | 100 | | 100 | | ms | D1 = 1 [5,6] |

**Notes:**
[1] Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
[2] Interrupt request via Port 3 (P31-P33).
[3] $V_{CC}$ = 3.0V to 5.5V.
[4] SMR-D5 = 0, POR delay is off.
[5] WDTMR Register
[6] Internal RC Oscillator only.
[7] SMR D1 = 0, SCLK = External/2
[8] Maximum frequency for internal system clock is 4 MHz when using SCLK = EXTERNAL clock mode.
[9] For RC and LC oscillator and for clock-driven oscillator.
[10] SMR-D5 = 1, STOP-Mode Recovery delay is on.
[11] Z86E03 = 8 MHz; Z86E06 = 12 MHz.

## AC ELECTRICAL CHARACTERISTICS

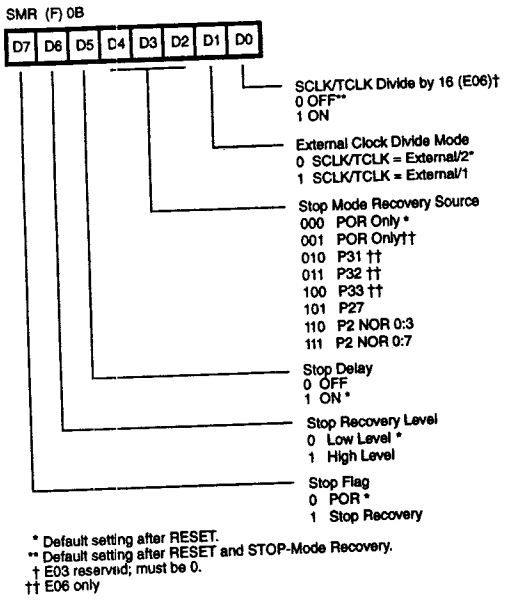
Additional Timing Table (Divide-By-One Mode, SCLK/TCLK = EXTERNAL)

| No | Symbol | Parameter | $V_{CC}$ Note [6] | $T_A$ = 0°C to +70°C 4 MHz Min | Max | $T_A$ = −40°C to +105°C 4 MHz Min | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TpC | Input Clock Period | 3.0V | 250 | DC | 250 | DC | ns | [1,7,8] |
| | | | 5.5V | 250 | DC | 250 | DC | ns | [1,7,8] |
| 2 | TrC,TfC | Clock Input Rise & Fall Times | 3.0V | | 25 | | 25 | ns | [1,7,8] |
| | | | 5.5V | | 25 | | 25 | ns | [1,7,8] |
| 3 | TwC | Input Clock Width | 3.0V | 125 | | 125 | | ns | [1,7,8] |
| | | | 5.5V | 125 | | 125 | | ns | [1,7,8] |
| 4 | TwTinL | Timer Input Low Width | 3.0V | 100 | | 100 | | ns | [1,7,8] |
| | | | 5.5V | 70 | | 70 | | ns | [1,7,8] |
| 5 | TwTinH | Timer Input High Width | 3.0V | 3TpC | | 3TpC | | | [1,7,8] |
| | | | 5.5V | 3TpC | | 3TpC | | | [1,7,8] |
| 6 | TpTin | Timer Input Period | 3.0V | 4TpC | | 4TpC | | | [1,7,8] |
| | | | 5.5V | 4TpC | | 4TpC | | | [1,7,8] |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Timer | 3.0V | | 100 | | 100 | ns | [1,7,8] |
| | | | 5.5V | | 100 | | 100 | ns | [1,7,8] |
| 8 | TwIL | Int. Request Low Time | 3.0V | 100 | | 100 | | ns | [1,2,7,8] |
| | | | 5.5V | 70 | | 70 | | ns | [1,7,8] |
| 9 | TwIH | Int. Request Input High Time | 3.0V | 3TpC | | 3TpC | | | [1,2,7,8] |
| | | | 5.5V | 3TpC | | 3TpC | | | [1,2,7,8] |
| 10 | Twsm | Stop-Mode Recovery Width Spec | 3.0V | 12 | | 12 | | ns | [1,4,] |
| | | | 5.5V | 12 | | 12 | | ns | [1,4] |
| 11 | Tost | Oscillator Startup Time | 3.0V | | 5TpC | | 5TpC | | [1,3,8,9] |
| | | | 5.5V | | 5TpC | | 5TpC | | [1,3,8,9] |

**Notes:**

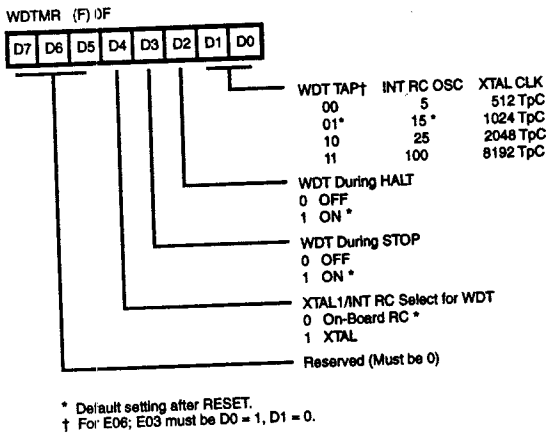
[1] Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
[2] Interrupt request via Port 3 (P33-P31).
[3] SMR-D5 = 0.
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] $V_{CC}$ = 3.0V to 5.5V.
[7] SMR D1 = 1.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-one mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.

## EXPANDED REGISTER FILE CONTROL REGISTERS



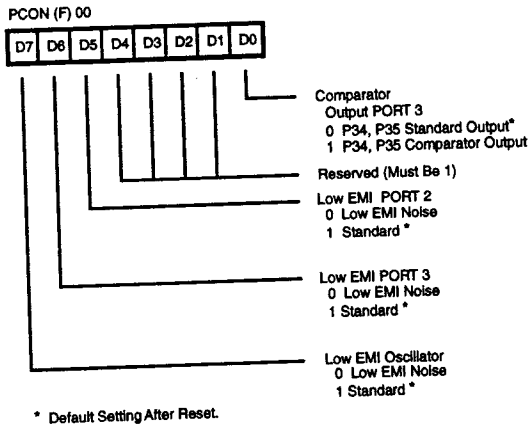

* Default setting after RESET.
** Default setting after RESET and STOP-Mode Recovery.
† E03 reserved; must be 0.
†† E06 only

**Figure 30. STOP-Mode Recovery Register (Write Only except bit D7, which is Read Only)**



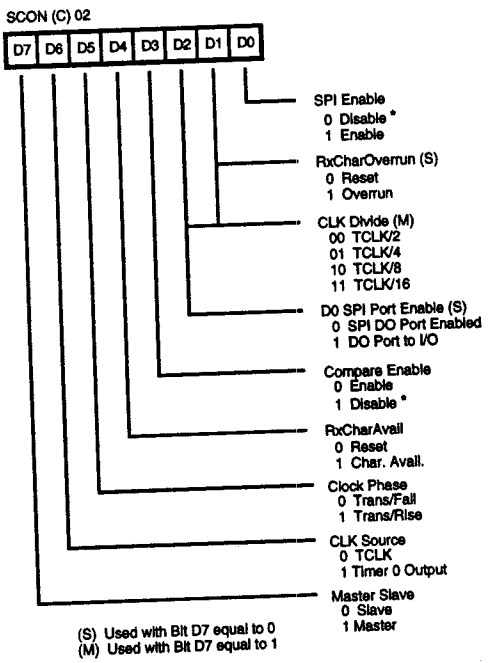

* Default setting after RESET.
† For E06; E03 must be D0 = 1, D1 = 0.

**Figure 31. Watch-Dog Timer Mode Register (Write Only)**




* Default Setting After Reset.

**Figure 32. PORT Control Register (Write Only)**




(S) Used with Bit D7 equal to 0
(M) Used with Bit D7 equal to 1

* Default Setting After Reset.

**Figure 33. SPI Control Register (Z86E06 Only)**

## EXPANDED REGISTER FILE CONTROL REGISTERS (Continued)

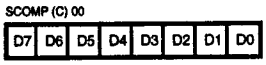



**Figure 34. SPI Compare Register (Z86E06 Only)**

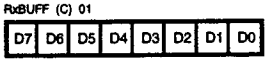



**Figure 35. SPI Receive Buffer (Z86E06 Only)**

## Z8 CONTROL REGISTER DIAGRAMS

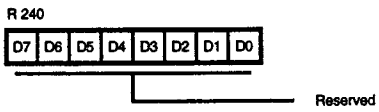



**Figure 36. Reserved**

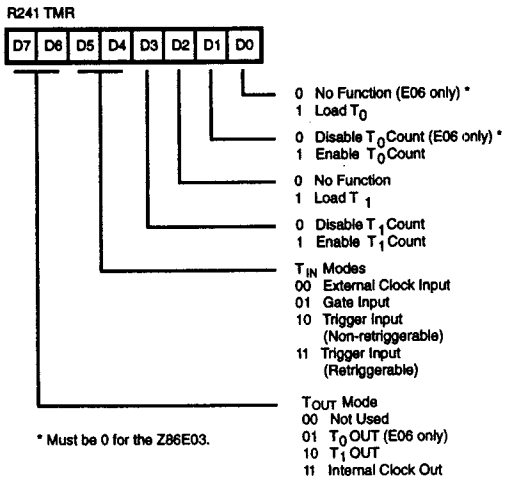



**Figure 37. Timer Mode Register ($F1_H$: Read/Write)**

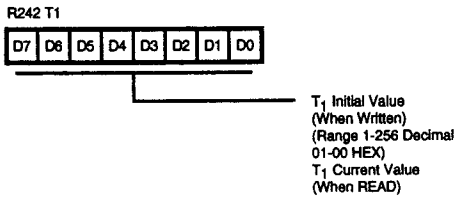



**Figure 38. Counter Timer 1 Register ($F2_H$: Read/Write)**

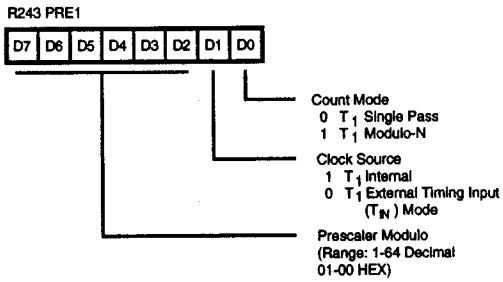



**Figure 39. Prescaler 1 Register ($F3_H$: Write Only)**

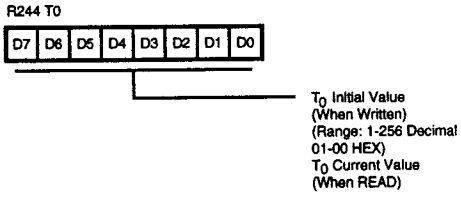



**Figure 40. Counter/Timer 0 Register ($F4_H$: Read/Write; Z86E06 Only)**

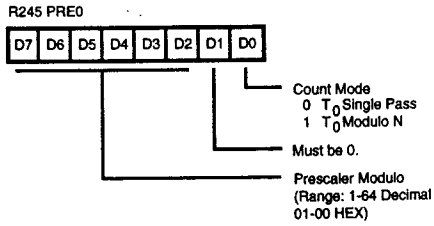



**Figure 41. Prescaler 0 Register ($F5_H$: Write Only; Z86E06 Only)**

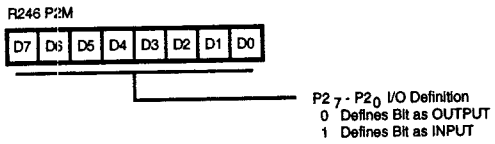



**Figure 42. Port 2 Mode Register ($F6_H$: Write Only)**

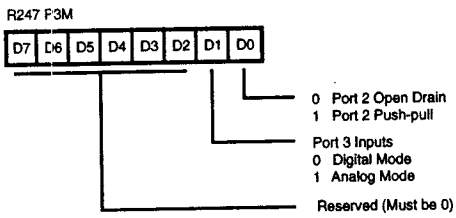



**Figure 43. Port 3 Mode Register ($F7_H$: Write Only)**

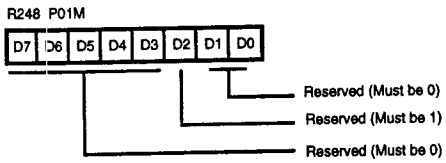



**Figure 44. Port 0 and 1 Mode Register ($F8_H$: Write Only)**

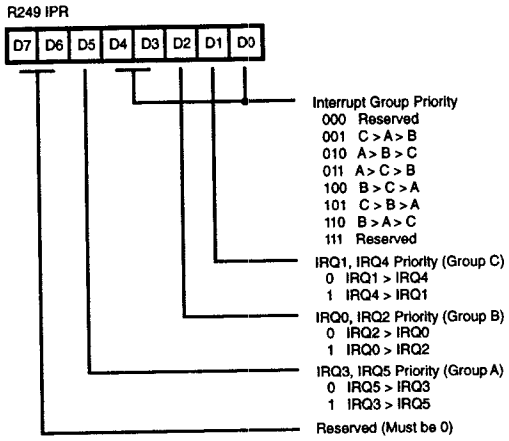



**Figure 45. Interrupt Priority Register ($F9_H$: Write Only)**

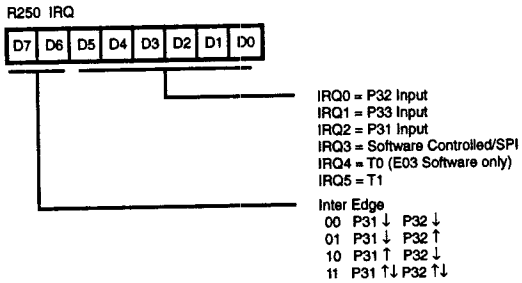



**Figure 46. Interrupt Request Register ($FA_H$: Read/Write)**

2

## Z8 CONTROL REGISTER DIAGRAMS (Continued)

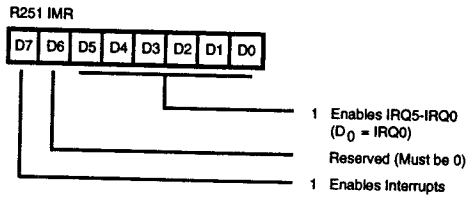



**Figure 47. Interrupt Mask Register ($FB_H$: Read/Write)**

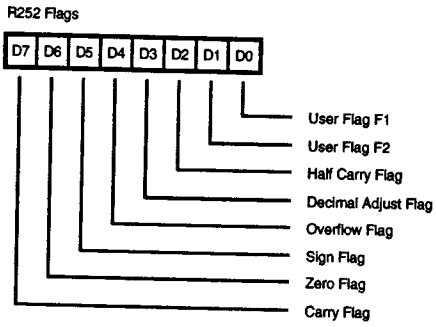



**Figure 48. Flag Register ($FC_H$: Read/Write)**

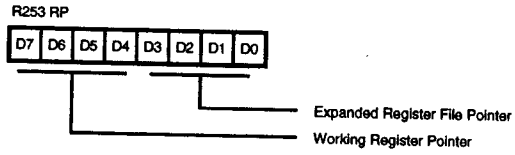



**Figure 49. Register Pointer ($FD_H$: Read/Write)**

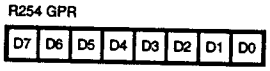



**Figure 50. General Purpose Register ($FE_H$: Read/Write)**

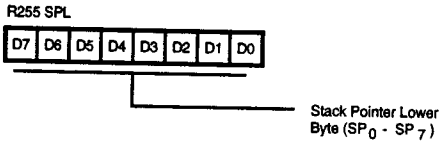



**Figure 51. Stack Pointer ($FF_H$: Read/Write)**

## INSTRUCTION SET NOTATION

**Addressing Modes.** The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

| Symbol | Meaning |
|---|---|
| IRR | Indirect register pair or indirect working-register pair address |
| Irr | Indirect working-register pair only |
| X | Indexed address |
| DA | Direct address |
| RA | Relative address |
| IM | Immediate |
| R | Register or working-register address |
| r | Working-register address only |
| IR | Indirect-register or indirect working-register address |
| Ir | Indirect working-register address only |
| RR | Register pair or working register pair address |

**Symbols.** The following symbols are used in describing the instruction set.

| Symbol | Meaning |
|---|---|
| dst | Destination location or contents |
| src | Source location or contents |
| cc | Condition code |
| @ | Indirect address prefix |
| SP | Stack Pointer |
| PC | Program Counter |
| FLAGS | Flag register (Control Register 252) |
| RP | Register Pointer (R253) |
| IMR | Interrupt mask register (R251) |

**Flags.** Control register (R252) contains the following six flags:

| Symbol | Meaning |
|---|---|
| C | Carry flag |
| Z | Zero flag |
| S | Sign flag |
| V | Overflow flag |
| D | Decimal-adjust flag |
| H | Half-carry flag |

Affected flags are indicated by:

| | |
|---|---|
| 0 | Clear to zero |
| 1 | Set to one |
| * | Set to clear according to operation |
| - | Unaffected |
| x | Undefined |

2

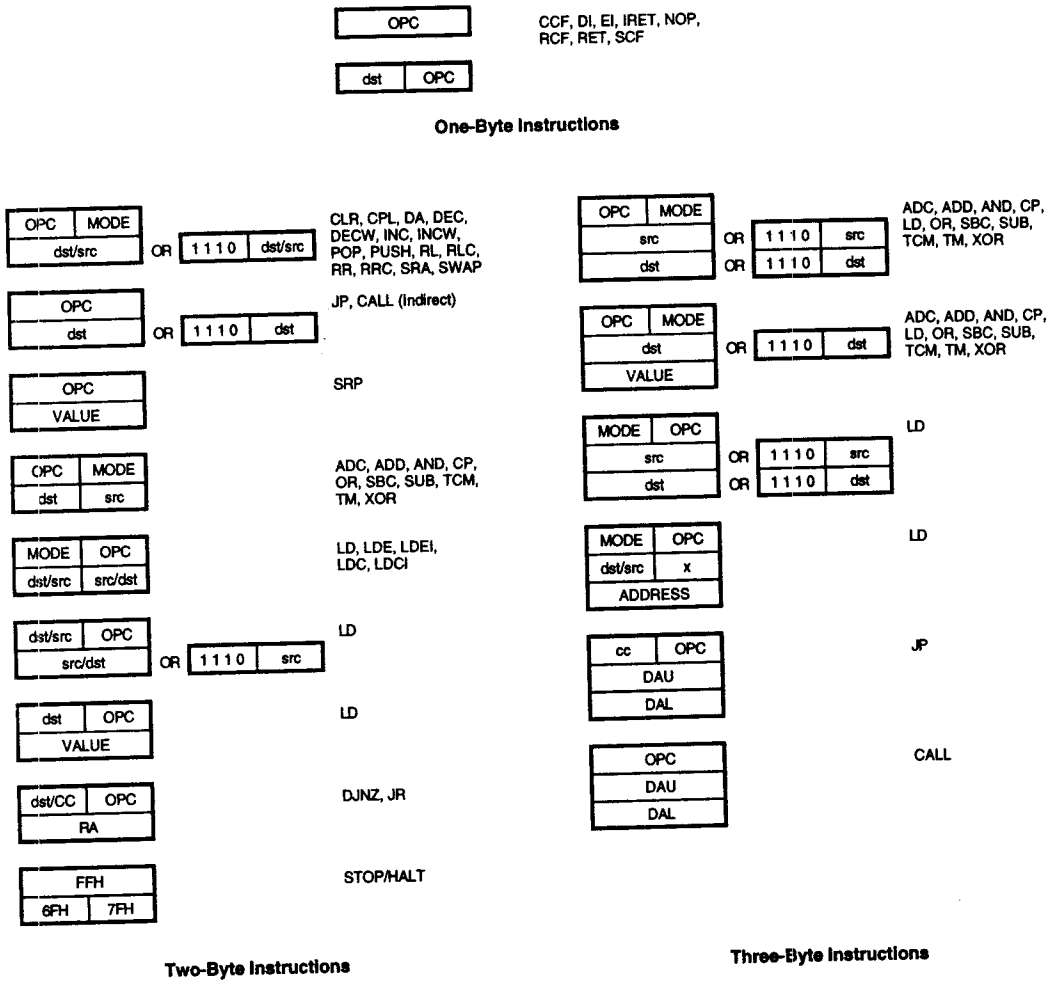
## CONDITION CODES

| Value | Mnemonic | Meaning | Flags Set |
|---|---|---|---|
| 1000 | | Always True | |
| 0111 | C | Carry | C = 1 |
| 1111 | NC | No Carry | C = 0 |
| 0110 | Z | Zero | Z = 1 |
| 1110 | NZ | Not Zero | Z = 0 |
| 1101 | PL | Plus | S = 0 |
| 0101 | MI | Minus | S = 1 |
| 0100 | OV | Overflow | V = 1 |
| 1100 | NOV | No Overflow | V = 0 |
| 0110 | EQ | Equal | Z = 1 |
| 1110 | NE | Not Equal | Z = 0 |
| 1001 | GE | Greater Than or Equal | (S XOR V) = 0 |
| 0001 | LT | Less than | (S XOR V) = 1 |
| 1010 | GT | Greater Than | [Z OR (S XOR V)] = 0 |
| 0010 | LE | Less Than or Equal | [Z OR (S XOR V)] = 1 |
| 1111 | UGE | Unsigned Greater Than or Equal | C = 0 |
| 0111 | ULT | Unsigned Less Than | C = 1 |
| 1011 | UGT | Unsigned Greater Than | (C = 0 AND Z = 0) = 1 |
| 0011 | ULE | Unsigned Less Than or Equal | (C OR Z) = 1 |
| 0000 | F | Never True (Always False) | — |



PS0201001-0603

## INSTRUCTION FORMATS




## INSTRUCTION SUMMARY

**Note:** Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

## INSTRUCTION SUMMARY (Continued)

| Instruction and Operation | Address Mode dst | src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **ADC** dst, src<br>dst←dst + src +C | † | | 1[ ] | * | * | * | * | 0 | * |
| **ADD** dst, src<br>dst←dst + src | † | | 0[ ] | * | * | * | * | 0 | * |
| **AND** dst, src<br>dst←dst AND src | † | | 5[ ] | - | * | * | 0 | - | - |
| **CALL** dst<br>SP←SP - 2<br>@SP←PC,<br>PC←dst | DA<br>IRR | | D6<br>D4 | - | - | - | - | - | - |
| **CCF**<br>C←NOT C | | | EF | * | - | - | - | - | - |
| **CLR** dst<br>dst←0 | R<br>IR | | B0<br>B1 | - | - | - | - | - | - |
| **COM** dst<br>dst←NOT dst | R<br>IR | | 60<br>61 | - | * | * | 0 | - | - |
| **CP** dst, src<br>dst - src | † | | A[ ] | * | * | * | * | - | - |
| **DA** dst<br>dst←DA dst | R<br>IR | | 40<br>41 | * | * | * | X | - | - |
| **DEC** dst<br>dst←dst - 1 | R<br>IR | | 00<br>01 | - | * | * | * | - | - |
| **DECW** dst<br>dst←dst - 1 | RR<br>IR | | 80<br>81 | - | * | * | * | - | - |
| **DI**<br>IMR(7)←0 | | | 8F | - | - | - | - | - | - |
| **DJNZ**r, dst<br>r←r - 1<br>if r ≠ 0<br>PC←PC + dst<br>Range: +127, 128 | RA | | rA<br>r = 0 - F | - | - | - | - | - | - |
| **EI**<br>IMR(7)←1 | | | 9F | - | - | - | - | - | - |
| **HALT** | | | 7F | - | - | - | - | - | - |

| Instruction and Operation | Address Mode dst | src | Opcode Byte (Hex) | Flags Affected C | Z | S | V | D | H |
|---|---|---|---|---|---|---|---|---|---|
| **INC** dst<br>dst←dst + 1 | r<br><br>R<br>IR | | rE<br>r = 0 - F<br>20<br>21 | - | * | * | * | - | - |
| **INCW** dst<br>dst←dst + 1 | RR<br>IR | | A0<br>A1 | - | * | * | * | - | - |
| **IRET**<br>FLAGS←@SP;<br>SP←SP + 1<br>PC←@SP;<br>SP←SP + 2;<br>IMR(7)←1 | | | BF | * | * | * | * | * | * |
| **JP** cc, dst<br>if cc is true,<br>PC←dst | DA<br><br>IRR | | cD<br>c = 0 - F<br>30 | - | - | - | - | - | - |
| **JR** cc, dst<br>if cc is true,<br>PC←PC + dst<br>Range: +127, -128 | RA | | cB<br>c = 0 - F | - | - | - | - | - | - |
| **LD** dst, src<br>dst←src | r<br>r<br>R<br><br>r<br>X<br>r<br>r<br>R<br>R<br>R<br>R<br>IR<br>IR | Im<br>R<br>r<br><br>X<br>r<br>Ir<br>r<br>R<br>IR<br>IM<br>IM<br>R | rC<br>r8<br>r9<br>r = 0 - F<br>C7<br>D7<br>E3<br>F3<br>E4<br>E5<br>E6<br>E7<br>F5 | - | - | - | - | - | - |
| **LDC** dst, src<br>dst←src | r | Irr | C2 | - | - | - | - | - | - |
| **LDCI** dst, src<br>dst←src<br>r←r + 1;rr←rr + 1 | Ir | Irr | C3 | - | - | - | - | - | - |
| **NOP** | | | FF | - | - | - | - | - | - |

| Instruction and Operation | Address Mode dst src | Opcode Byte (Hex) | Flags Affected C Z S V D H |
|---|---|---|---|
| **OR** dst, src<br>dst←dst OR src | † | 4[ ] | - * * 0 - - |
| **POP** dst<br>dst←@SP;<br>SP←SP + 1 | R<br>IR | 50<br>51 | - - - - - - |
| **PUSH** src<br>SP←SP - 1;<br>@SP←src | R<br>IR | 70<br>71 | - - - - - - |
| **RCF**<br>C←0 | | CF | 0 - - - - - |
| **RET**<br>PC←@SP;<br>SP←SP + 2 | | AF | - - - - - - |
| **RL** dst | R<br>IR | 90<br>91 | * * * * - - |
| **RLC** dst | R<br>IR | 10<br>11 | * * * * - - |
| **RR** dst | R<br>IR | E0<br>E1 | * * * * - - |
| **RRC** dst | R<br>IR | C0<br>C1 | * * * * - - |
| **SBC** dst, src<br>dst←dst–src–C | † | 3[ ] | * * * * 1 * |
| **SCF**<br>C←1 | | DF | 1 - - - - - |
| **SRA** dst | R<br>IR | D0<br>D1 | * * * 0 - - |
| **SRP** dst<br>RP←src | Im | 31 | - - - - - - |
| **STOP** | | 6F | 1 - - - - - |

| Instruction and Operation | Address Mode dst src | Opcode Byte (Hex) | Flags Affected C Z S V D H |
|---|---|---|---|
| **SUB** dst, src<br>dst←dst - src | † | 2[ ] | * * * * 1 * |
| **SWAP** dst | R<br>IR | F0<br>F1 | X * * X - - |
| **TCM** dst, src<br>(NOT dst) AND src | † | 6[ ] | - * * 0 - - |
| **TM** dst, src<br>dst AND src | † | 7[ ] | - * * 0 - - |
| **WDT** | | 5F | - X X X - - |
| **XOR** dst, src<br>dst←dst XOR src | † | B[ ] | - * * 0 - - |

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

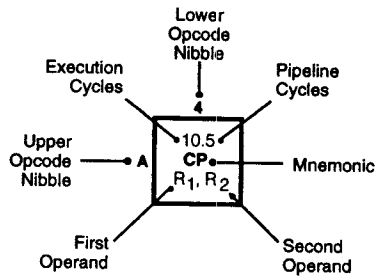
| Address Mode dst | Address Mode src | Lower Opcode Nibble |
|---|---|---|
| r | r | [2] |
| r | Ir | [3] |
| R | R | [4] |
| R | IR | [5] |
| R | IM | [6] |
| IR | IM | [7] |

2

## OPCODE MAP

Lower Nibble (Hex)

| Upper Nibble (Hex) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 6.5 **DEC** R1 | 6.5 **DEC** IR1 | 6.5 **ADD** r1, r2 | 6.5 **ADD** r1, Ir2 | 10.5 **ADD** R2, R1 | 10.5 **ADD** IR2, R1 | 10.5 **ADD** R1, IM | 10.5 **ADD** IR1, IM | 6.5 **LD** r1, R2 | 6.5 **LD** r2, R1 | 12/10.5 **DJNZ** r1, RA | 12/10.0 **JR** cc, RA | 6.5 **LD** r1, IM | 12.10.0 **JP** cc, DA | 6.5 **INC** r1 | |
| 1 | 6.5 **RLC** R1 | 6.5 **RLC** IR1 | 6.5 **ADC** r1, r2 | 6.5 **ADC** r1, Ir2 | 10.5 **ADC** R2, R1 | 10.5 **ADC** IR2, R1 | 10.5 **ADC** R1, IM | 10.5 **ADC** IR1, IM | | | | | | | | |
| 2 | 6.5 **INC** R1 | 6.5 **INC** IR1 | 6.5 **SUB** r1, r2 | 6.5 **SUB** r1, Ir2 | 10.5 **SUB** R2, R1 | 10.5 **SUB** IR2, R1 | 10.5 **SUB** R1, IM | 10.5 **SUB** IR1, IM | | | | | | | | |
| 3 | 8.0 **JP** IRR1 | 6.1 **SRP** IM | 6.5 **SBC** r1, r2 | 6.5 **SBC** r1, Ir2 | 10.5 **SBC** R2, R1 | 10.5 **SBC** IR2, R1 | 10.5 **SBC** R1, IM | 10.5 **SBC** IR1, IM | | | | | | | | |
| 4 | 8.5 **DA** R1 | 8.5 **DA** IR1 | 6.5 **OR** r1, r2 | 6.5 **OR** r1, Ir2 | 10.5 **OR** R2, R1 | 10.5 **OR** IR2, R1 | 10.5 **OR** R1, IM | 10.5 **OR** IR1, IM | | | | | | | | |
| 5 | 10.5 **POP** R1 | 10.5 **POP** IR1 | 6.5 **AND** r1, r2 | 6.5 **AND** r1, Ir2 | 10.5 **AND** R2, R1 | 10.5 **AND** IR2, R1 | 10.5 **AND** R1, IM | 10.5 **AND** IR1, IM | | | | | | | | 6.0 **WDT** |
| 6 | 6.5 **COM** R1 | 6.5 **COM** IR1 | 6.5 **TCM** r1, r2 | 6.5 **TCM** r1, Ir2 | 10.5 **TCM** R2, R1 | 10.5 **TCM** IR2, R1 | 10.5 **TCM** R1, IM | 10.5 **TCM** IR1, IM | | | | | | | | 6.0 **STOP** |
| 7 | 10/12.1 **PUSH** R2 | 12/14.1 **PUSH** IR2 | 6.5 **TM** r1, r2 | 6.5 **TM** r1, Ir2 | 10.5 **TM** R2, R1 | 10.5 **TM** IR2, R1 | 10.5 **TM** R1, IM | 10.5 **TM** IR1, IM | | | | | | | | 7.0 **HALT** |
| 8 | 10.5 **DECW** RR1 | 10.5 **DECW** IR1 | | | | | | | | | | | | | | 6.1 **DI** |
| 9 | 6.5 **RL** R1 | 6.5 **RL** IR1 | | | | | | | | | | | | | | 6.1 **EI** |
| A | 10.5 **INCW** RR1 | 10.5 **INCW** IR1 | 6.5 **CP** r1, r2 | 6.5 **CP** r1, Ir2 | 10.5 **CP** R2, R1 | 10.5 **CP** IR2, R1 | 10.5 **CP** R1, IM | 10.5 **CP** IR1, IM | | | | | | | | 14.0 **RET** |
| B | 6.5 **CLR** R1 | 6.5 **CLR** IR1 | 6.5 **XOR** r1, r2 | 6.5 **XOR** r1, Ir2 | 10.5 **XOR** R2, R1 | 10.5 **XOR** IR2, R1 | 10.5 **XOR** R1, IM | 10.5 **XOR** IR1, IM | | | | | | | | 16.0 **IRET** |
| C | 6.5 **RRC** R1 | 6.5 **RRC** IR1 | 12.0 **LDC** r1, Irr2 | 18.0 **LDCI** Ir1, Irr2 | | | | 10.5 **LD** r1,x,R2 | | | | | | | | 6.5 **RCF** |
| D | 6.5 **SRA** R1 | 6.5 **SRA** IR1 | | | 20.0 **CALL*** IRR1 | | 20.0 **CALL** DA | 10.5 **LD** r2,x,R1 | | | | | | | | 6.5 **SCF** |
| E | 6.5 **RR** R1 | 6.5 **RR** IR1 | | 6.5 **LD** r1, IR2 | 10.5 **LD** R2, R1 | 10.5 **LD** IR2, R1 | 10.5 **LD** R1, IM | 10.5 **LD** IR1, IM | | | | | | | | 6.5 **CCF** |
| F | 8.5 **SWAP** R1 | 8.5 **SWAP** IR1 | | 6.5 **LD** Ir1, r2 | | 10.5 **LD** R2, IR1 | | | | | | | | | | 6.0 **NOP** |
| Bytes per Instruction | 2 | | | 3 | | | | | 2 | | | | | 3 | 1 | |



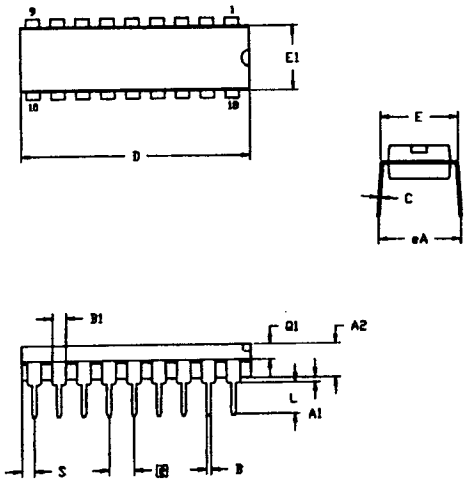

**Legend:**
R = 8-bit address
r = 4-bit address
$R_1$ or $r_1$ = Dst address
$R_2$ or $r_2$ = Src address

**Sequence:**
Opcode, First Operand, Second Operand

**Note:** The blank areas are reserved.

* 2-byte instruction appears as a 3-byte instruction

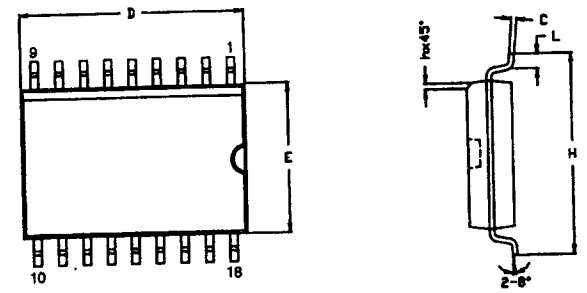
## PACKAGE INFORMATION




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | .020 | .032 |
| A2 | 3.25 | 3.43 | .128 | .135 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.14 | 1.65 | .045 | .065 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 22.35 | 23.37 | .880 | .920 |
| E | 7.62 | 8.13 | .300 | .320 |
| E1 | 6.22 | 6.48 | .245 | .255 |
| eB | 2.54 TYP | | .100 TYP | |
| eA | 7.87 | 8.89 | .310 | .350 |
| L | 3.18 | 3.81 | .125 | .150 |
| Q1 | 1.52 | 1.65 | .060 | .065 |
| S | 0.89 | 1.65 | .035 | .065 |

CONTROLLING DIMENSIONS : INCH

**18-Pin DIP Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 11.40 | 11.75 | .449 | .463 |
| E | 7.40 | 7.60 | .291 | .299 |
| eB | 1.27 TYP | | .050 TYP | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.40 | .012 | .016 |
| L | 0.60 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.07 | .038 | .042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**18-Pin SOIC Package Diagram**



PS0201001-0603

## ORDERING INFORMATION

### Z86E03 (8 MHz)

| Standard Temperature | | Extended Temperature | |
|---|---|---|---|
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86E0308PSC | Z86E0308SSC | Z86E0308PEC | Z86E0308SEC |

### Z86E06 (12 MHz)

| Standard Temperature | | Extended Temperature | |
|---|---|---|---|
| 18-Pin DIP | 18-Pin SOIC | 18-Pin DIP | 18-Pin SOIC |
| Z86E0612PSC | Z86E0612SSC | Z86E0612PEC | Z86E0612SEC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

## CODES

**Preferred Package**
P = Plastic DIP

**Longer Lead Time**
S = Plastic SOIC

**Preferred Temperature**
S = 0°C to +70°C

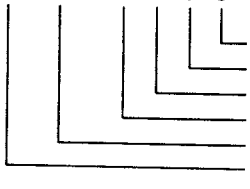
**Longer Lead Time**
E = –40°C to +105°C

**Speeds**
08 = 8 MHz
12 = 12 MHz

**Environmental**
C = Plastic Standard

**Example:**

**Z 86E03 08 P S C** is a Z86E03, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



LifeElectronics
Живое партнерство

**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

*ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703*

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***