EiceDRIVER™

1ED020I12-B2

Single IGBT Driver IC

Final Data Sheet

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Industrial Power Control

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Revision History

Page or Item	Subjects (major changes since previous revision)
Rev. 2.1, 2017-09-28	
All	Corrected typos and clarified description
Page 17, Table 3	Upgrade common mode transient immunity rating to 100 kV/µs, change typo $\|DV_{ISO}/dt\|$ to $\|dV_{ISO}/dt\|$

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1 Overview

Main Features

- Single channel isolated IGBT Driver
- For 600V/1200 V IGBTs
- 2 A rail-to-rail output
- Vcesat-detection
- Active Miller Clamp

Product Highlights

- Coreless transformer isolated driver
- Basic insulation according to DIN EN 60747-5-2
- Integrated protection features
- Suitable for operation at high ambient temperature

Potential Applications

- AC and Brushless DC Motor Drives
- High Voltage DC/DC-Converter
- UPS-Systems
- Welding

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

The 1ED020I12-B2 is a galvanic isolated single channel IGBT driver in PG-DSO-16-15 package that provides an output current capability of typically 2A.

All logic pins are 5V CMOS compatible and could be directly connected to a microcontroller.

The data transfer across galvanic isolation is realized by the integrated Coreless Transformer Technology.

The 1ED020I12-B2 provides several protection features like IGBT desaturation protection, active Miller clamping and active shut down.

Product Name	Gate Drive Current	Package
1ED020I12-B2	±2 A	PG-DSO-16-15

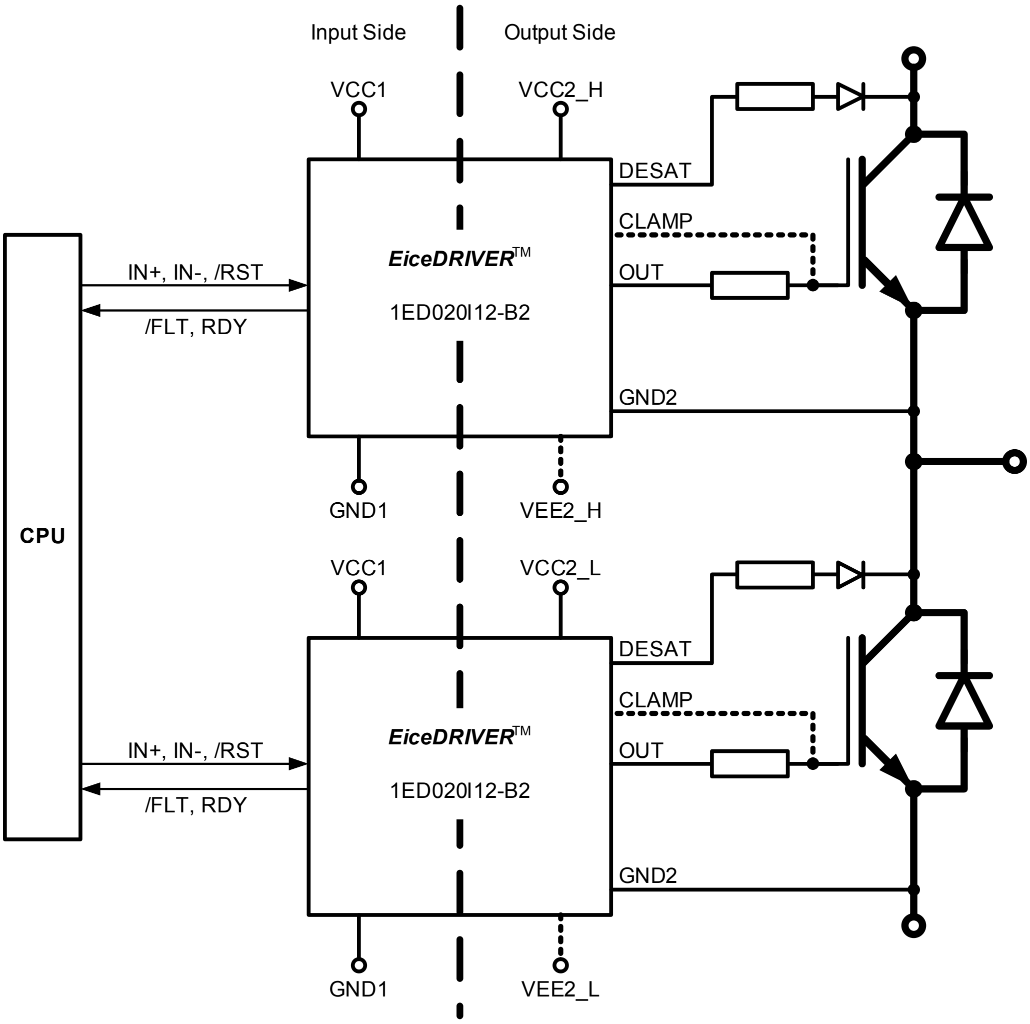


Figure 1 Typical Application

2 Block Diagram

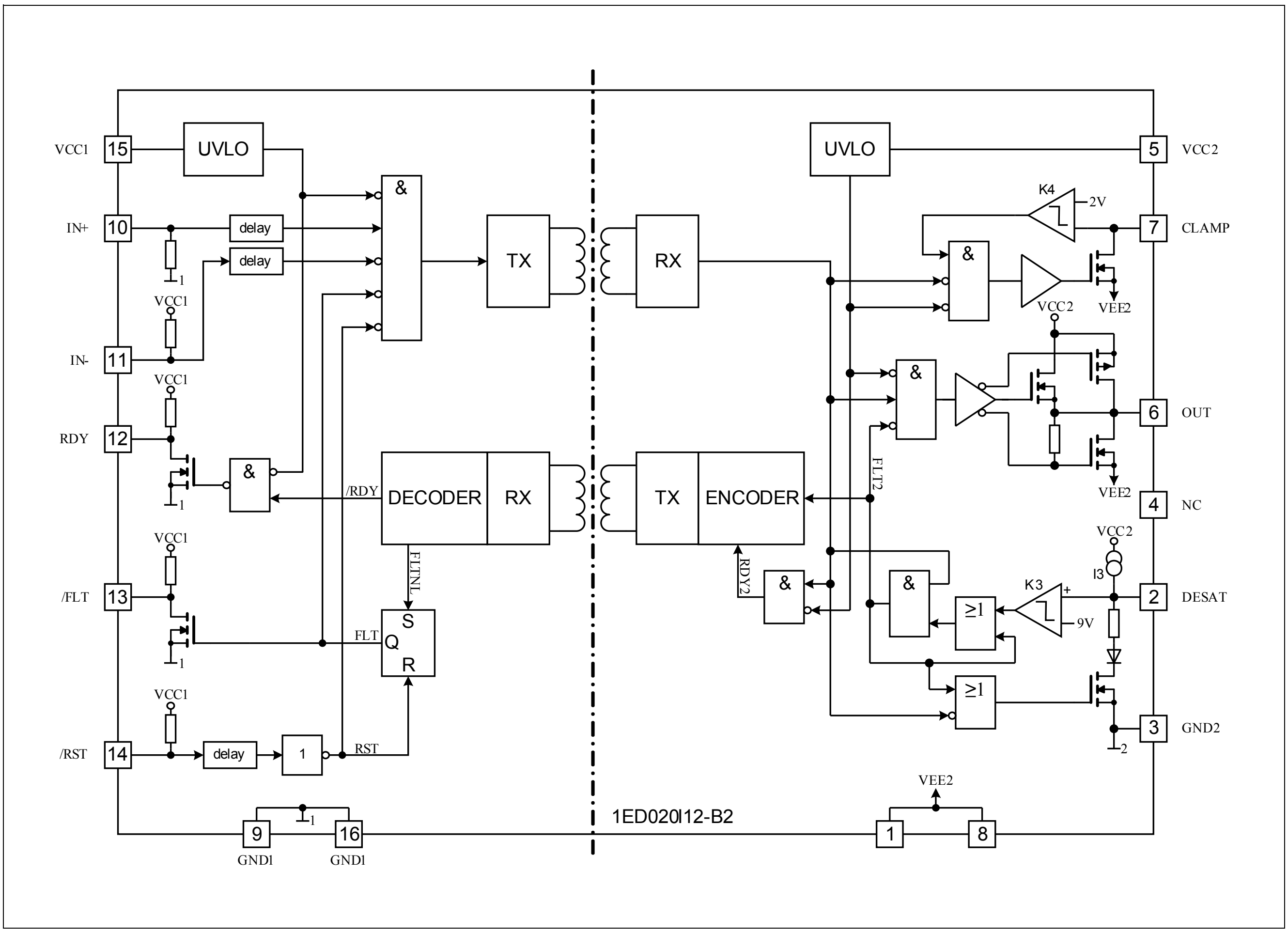


Figure 2 Block Diagram 1ED020I12-B2

3 Pin Configuration and Functionality

3.1 Pin Configuration

Table 1 Pin Configuration

Pin No.	Name	Function
1	VEE2	Negative power supply output side
2	DESAT	Desaturation protection
3	GND2	Signal ground output side
4	NC	Not connected
5	VCC2	Positive power supply output side
6	OUT	Driver output
7	CLAMP	Miller clamping
8	VEE2	Negative power supply output side
9	GND1	Ground input side
10	IN+	Non inverted driver input
11	IN-	Inverted driver input
12	RDY	Ready output
13	/FLT	Fault output, low active
14	/RST	Reset input, low active
15	VCC1	Positive power supply input side
16	GND1	Ground input side

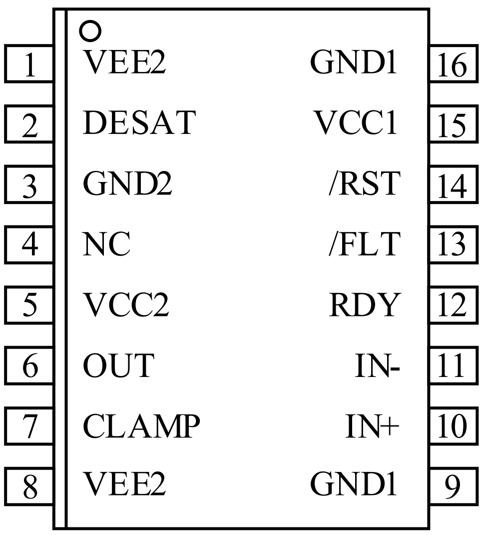


Figure 3 PG-DSO-16-15 (top view)

3.2 Pin Functionality

GND1

Ground connection of the input side.

IN+ Non Inverting Driver Input

IN+ control signal for the driver output if IN- is set to low. (The IGBT is on if IN+ = high and IN- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

IN- Inverting Driver Input

IN- control signal for driver output if IN+ is set to high. (IGBT is on if IN- = low and IN+ = high)

A minimum pulse width is defined to make the IC robust against glitches at IN-. An internal Pull-Up-Resistor ensures IGBT Off-State.

/RST Reset Input

Function 1: Enable/shutdown of the input chip. (The IGBT is off if /RST = low). A minimum pulse width is defined to make the IC robust against glitches at /RST.

Function 2: Resets the DESAT-FAULT-state of the chip if /RST is low for a time T_{RST}. An internal Pull-Up-Resistor is used to ensure /FLT status output.

/FLT Fault Output

Open-drain output to report a desaturation error of the IGBT (/FLT is low if desaturation occurs)

RDY Ready Status

Open-drain output to report the correct operation of the device (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless).

VCC1

5 V power supply of the input chip

VEE2

Negative power supply pins of the output chip. If no negative supply voltage is available, all VEE2 pins have to be connected to GND2.

DESAT Desaturation Detection Input

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMP Miller Clamping

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2 V (related to VEE2). The clamp is designed for a Miller current up to 2 A.

GND2 Reference Ground

Reference ground of the output chip.

OUT Driver Output

Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode Vout is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) Vout is set to VEE2 independent of the input control signals.

VCC2

Positive power supply pin of the output side.

4 Functional Description

4.1 Introduction

The 1ED020I12-B2 is an advanced IGBT gate driver that can be also used for driving power MOS devices. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5 V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

The rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes IGBT desaturation protection with /FLT status output.

The READY status output reports if the device is supplied and operates correctly.

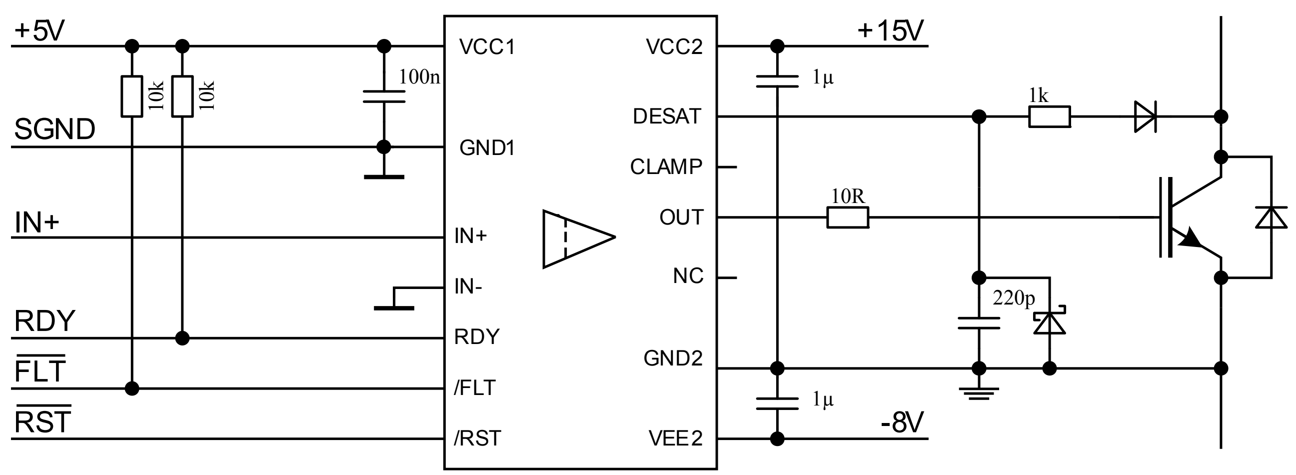


Figure 4 Application Example Bipolar Supply

4.2 Supply

The driver 1ED020I12-B2 is designed to support two different supply configurations, bipolar supply and unipolar supply.

In bipolar supply the driver is typically supplied with a positive voltage of 15V at VCC2 and a negative voltage of -8V at VEE2, please refer to **Figure 4**. Negative supply prevents a dynamic turn on due to the additional charge which is generated from IGBT input capacitance times negative supply voltage. If an appropriate negative supply voltage is used, connecting CLAMP to IGBT gate is redundant and therefore typically not necessary.

For unipolar supply configuration the driver is typically supplied with a positive voltage of 15V at VCC2. Erratically dynamic turn on of the IGBT could be prevented with active Miller clamp function, so CLAMP output is directly connected to IGBT gate, please refer to **Figure 5**.

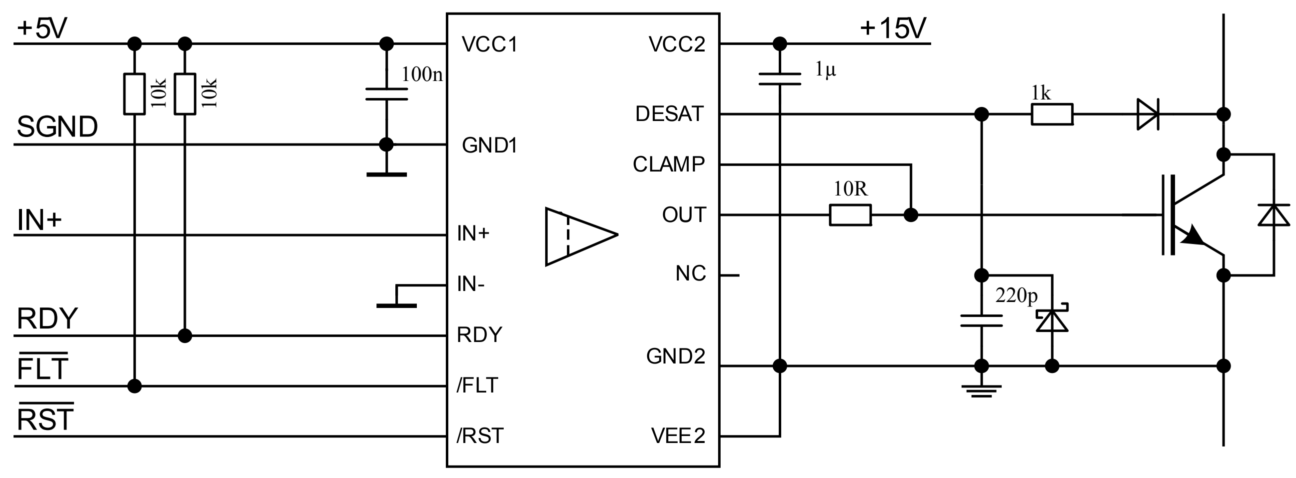


Figure 5 Application Example Unipolar Supply

4.3 Internal Protection Features

4.3.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips, refer to **Figure 9**.

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored as long as V_{VCC1} reaches the power-up voltage V_{UVLOH1}.

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored as long as V_{VCC2} reaches the power-up voltage V_{UVLOH2}. VEE2 is not monitored, otherwise negative supply voltage range from 0 V to -12 V would not be possible.

4.3.2 READY Status Output

The READY output shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission after a short delay

It is not necessary to reset the READY signal since its state only depends on the status of the former mentioned protection signals.

4.3.3 Watchdog Timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

4.3.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply, IGBT gate is clamped at OUT to VEE2.

4.4 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high, please see **Figure 7**. A minimum input pulse width is defined to filter occasional glitches.

4.5 Driver Output

The output driver sections uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

4.6 External Protection Features

4.6.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches 9 V, the output is driven low. Further, the /FLT output is activated after DESAT to FAULT off delay, please refer to **Figure 8**. An off command at IN during DESAT to FAULT off delay is erasing the fault status. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

4.6.2 Active Miller Clamp

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore in many applications, the use of a negative supply voltage can be avoided.

During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below typical 2 V (related to VEE2). The clamp is designed for a Miller current up to 2 A.

4.6.3 Short Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10 µs may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

4.7 RESET

The reset inputs have two functions.

Firstly, /RST is in charge of setting back the /FLT output. If /RST is low longer than a given time, /FLT will be cleared at the rising edge of /RST, refer to **Figure 8**; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic, refer to **Figure 7**.

5 Electrical Parameters

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Positive power supply output side	V_{VCC2}	-0.3	20	V	[1]
Negative power supply output side	V_{VEE2}	-12	0.3	V	[1]
Maximum power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	28	V	–
Gate driver output	V_{OUT}	V_{VEE2}-0.3	V_{VCC2}+0.3	V	–
Gate driver high output maximum current	I_{OUT}	–	2.4	A	t = 2 µs
Gate & Clamp driver low output maximum current	I_{OUT}	–	2.4	A	t = 2 µs
Maximum short circuit clamping time	t_{CLP}	–	10	µs	$I_{CLAMP/OUT}$ = 500 mA
Positive power supply input side	V_{VCC1}	-0.3	6.5	V	–
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	6.5	V	–
Opendrain Logic output voltage ($\overline{FLT}$)	$V_{FLT\#}$	-0.3	6.5	V	–
Opendrain Logic output voltage (RDY)	V_{RDY}	-0.3	6.5	V	–
Opendrain Logic output current ($\overline{FLT}$)	$I_{FLT\#}$	–	10	mA	–
Opendrain Logic output current (RDY)	I_{RDY}	–	10	mA	–
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3	V	[1]
Pin CLAMP voltage	V_{CLAMP}	-0.3	V_{VCC2} +0.3[2]	V	[3]
Input to output isolation voltage (GND2)	V_{ISO}	-1200	1200	V	
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_S	-55	150	°C	–
Power dissipation, per input part	$P_{D, IN}$	–	100	mW	[4]@T_A = 25°C
Power dissipation, per output part	$P_{D, OUT}$	–	700	mW	[4] @T_A = 25°C
Thermal resistance (Input part)	$R_{THJA,IN}$	–	160	K/W	[4] @T_A = 25°C
Thermal resistance (Output chip active)	$R_{THJA,OUT}$	–	125	K/W	[4] @T_A = 25°C
ESD Capability	V_{ESD}	–	1	kV	Human Body Model[5]

1) With respect to GND2.

2) May be exceeded during short circuit clamping.
3) With respect to VEE2.
4)Output IC power dissipation is derated linearly at 10 mW/°C above 62°C. Input IC power dissipation does not require derating. See **Figure 11** for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.
5) According to EIA/JESD22-A114-B (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).

5.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Table 3 Operating Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Positive power supply output side	V_{VCC2}	13	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0	V	1)
Maximum power supply voltage output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	28	V	–
Positive power supply input side	V_{VCC1}	4.5	5.5	V	–
Logic input voltages (IN+,IN-,RST)	$V_{LogicIN}$	-0.3	5.5	V	–
Pin CLAMP voltage	V_{CLAMP}	V_{VEE2}-0.3	V_{VCC2} 2)	V	–
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2}	V	1)
Pin TLSET voltage	V_{TLSET}	-0.3	V_{VCC2}	V	1)
Ambient temperature	T_A	-40	105	°C	–
Common mode transient immunity 3)	$\|dV_{ISO}/dt\|$	–	100	kV/µs	@ 1200 V

1) With respect to GND2.
2) May be exceeded during short circuit clamping.
3) The parameter is not subject to production test - verified by design/characterization

5.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1.

Table 4 Recommended Operating Parameters

Parameter	Symbol	Value	Unit	Note / Test Condition
Positive power supply output side	V_{VCC2}	15	V	1)
Negative power supply output side	V_{VEE2}	-8	V	1)
Positive power supply input side	V_{VCC1}	5	V	–

1) With respect to GND2.

5.4 Electrical Characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 9 to 16, GND2 for pins 1 to 8).

5.4.1 Voltage Supply

Table 5 Voltage Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO Threshold Input Chip	V_{UVLOH1}	–	4.1	4.3	V	–
	V_{UVLOL1}	3.5	3.8	–	V	–
UVLO Hysteresis Input Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.15	–	–	V	–
UVLO Threshold Output Chip	V_{UVLOH2}	–	12.0	12.6	V	–
	V_{UVLOL2}	10.4	11.0	–	V	–
UVLO Hysteresis Output Chip (V_{UVLOH2} - V_{UVLOL2})	V_{HYS2}	0.7	0.9	–	V	–
Quiescent Current Input Chip	I_{Q1}	–	7	9	mA	V_{VCC1} = 5 V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	I_{Q2}	–	4	6	mA	V_{VCC2} = 15 V V_{VEE2} = -8 V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

5.4.2 Logic Input and Output

Table 6 Logic Input and Output

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IN+,IN-, $\overline{RST}$ Low Input Voltage	V_{IN+L}, V_{IN-L}, $V_{RSTL\#}$	–	–	1.5	V	–
IN+,IN-, $\overline{RST}$ High Input Voltage	V_{IN+H}, V_{IN-H}, $V_{RSTH\#}$	3.5	–	–	V	–
IN-, $\overline{RST}$ Input Current	I_{IN-}, $I_{RST\#}$	-400	-100	–	µA	V_{IN-} = GND1 $V_{RST\#}$ = GND1
IN+ Input Current	I_{IN+},	–	100	400	µA	V_{IN+} = VCC1
RDY,$\overline{FLT}$ Pull Up Current	I_{PRDY}, $I_{PFLT\#}$	-400	-100	–	µA	V_{RDY} = GND1 $V_{FLT\#}$ = GND1
Input Pulse Suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	–	ns	–
Input Pulse Suppression $\overline{RST}$ for ENABLE/SHUTDOWN	T_{MINRST}	30	40	–	ns	–
Pulse Width $\overline{RST}$ for Reseting $\overline{FLT}$	T_{RST}	800	–	–	ns	–
$\overline{FLT}$ Low Voltage	V_{FLTL}	–	–	300	mV	$I_{SINK(FLT\#)}$ = 5 mA
RDY Low Voltage	V_{RDYL}	–	–	300	mV	$I_{SINK(RDY)}$ = 5 mA

5.4.3 Gate Driver

Table 7 Gate Driver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High Level Output Voltage	V_{OUTH1}	V_{CC2} -1.2	V_{CC2} -0.8	–	V	I_{OUTH} = -20 mA
	V_{OUTH2}	V_{CC2} -2.5	V_{CC2} -2.0	–	V	I_{OUTH} = -200 mA
	V_{OUTH3}	V_{CC2} -9	V_{CC2} -5	–	V	I_{OUTH} = -1 A
	V_{OUTH4}		V_{CC2} -10	–	V	I_{OUTH} = -2 A
High Level Output Peak Current	I_{OUTH}	-1.5	-2.0	–	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V_{OUTL1}	–	V_{VEE2} +0.04	V_{VEE2}+0.09	V	I_{OUTL} = 20 mA
	V_{OUTL2}	–	V_{VEE2} +0.3	V_{VEE2}+0.85	V	I_{OUTL} = 200 mA
	V_{OUTL3}	–	V_{VEE2} +2.1	V_{VEE2}+5	V	I_{OUTL} = 1 A
	V_{OUTL4}	–	V_{VEE2} +7	–	V	I_{OUTL} = 2 A
Low Level Output Peak Current	I_{OUTL}	1.5	2.0	–	A	IN+ = Low, IN- = Low; OUT = Low, V_{VCC2} = 15 V, V_{VEE2} = -8 V

5.4.4 Active Miller Clamp

Table 8 Active Miller Clamp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Low Level Clamp Voltage	$V_{CLAMPL1}$	–	V_{VEE2}+0.03	V_{VEE2} +0.08	V	I_{OUTL} = 20 mA
	$V_{CLAMPL2}$	–	V_{VEE2}+0.3	V_{VEE2} +0.8	V	I_{OUTL} = 200 mA
	$V_{CLAMPL3}$	–	V_{VEE2}+1.9	V_{VEE2} +4.8	V	I_{OUTL} = 1 A
Low Level Clamp Current	I_{CLAMPL}	2	–	–	A	[1]
Clamp Threshold Voltage	V_{CLAMP}	1.6	2.1	2.4	V	Related to VEE2

1) The parameter is not subject to production test - verified by design/characterization

5.4.5 Short Circuit Clamping

Table 9 Short Circuit Clamping

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage (OUT) (V_{OUT} - V_{VCC2})	V_{CLPout}	–	0.8	1.3	V	IN+ = High, IN- = Low, OUT = High I_{OUT} = 500 mA pulse test, t_{CLPmax} = 10 µs)
Clamping voltage (CLAMP) (V_{VCLAMP}-V_{VCC2})	$V_{CLPclamp}$	–	1.3	–	V	IN+ = High, IN- = Low, OUT = High I_{CLAMP} = 500 mA (pulse test, t_{CLPmax} = 10 µs)
Clamping voltage (CLAMP)	$V_{CLPclamp}$	–	0.7	1.1	V	IN+ = High, IN- = Low, OUT = High I_{CLAMP} = 20 mA

5.4.6 Dynamic Characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V, V_{VCC2} = 15 V and V_{VEE2} = -8 V.

Table 10 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input IN+, IN- to output propagation delay ON	T_{PDON}	145	170	195	ns	C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50% @ 25°C
Input IN+, IN- to output propagation delay OFF	T_{PDOFF}	145	165	190	ns	
Input IN+, IN- to output propagation delay distortion (T_{PDOFF} - T_{PDON})	T_{PDISTO}	-35	-5	25	ns	
IN+, IN- input to output propagation delay ON variation due to temp	T_{PDONt}	–	–	25	ns	[1] C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%
IN+, IN- input to output propagation delay OFF variation due to temp	T_{PDOFFt}	–	–	40	ns	[1] C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT} = 50%
IN+, IN- input to output propagation delay distortion variation due to temp (T_{PDOFF}-T_{PDON})	$T_{PDISTOt}$	–	–	20	ns	[1] C_{LOAD} = 100 pF V_{IN+} = 50%, V_{OUT}=50%

Table 10 Dynamic Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise Time	T_{RISE}	10	30	60	ns	C_{LOAD} = 1 nF V_L 10%, V_H 90%
		200	400	800	ns	C_{LOAD} = 34 nF V_L 10%, V_H 90%
Fall Time	T_{FALL}	10	50	90	ns	C_{LOAD} = 1 nF V_L 10%, V_H 90%
		200	350	600	ns	C_{LOAD} = 34 nF V_L 10%, V_H 90%

1) The parameter is not subject to production test - verified by design/characterization

5.4.7 Desaturation Protection

Table 11 Desaturation Protection

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Blanking Capacitor Charge Current	I_{DESATC}	450	500	550	µA	V_{VCC2} =15 V, V_{VEE2}=- 8 V V_{DESAT} = 2 V
Blanking Capacitor Discharge Current	I_{DESATD}	9	14	–	mA	V_{VCC2} =15 V, V_{VEE2} = -8 V V_{DESAT} = 6 V
Desaturation Reference Level	V_{DESAT}	8.3	9	9.5	V	V_{VCC2} = 15 V
Desaturation Filter Time	$T_{DESATfilter}$	–	250	–	ns	V_{VCC2} = 15 V, V_{VEE2} = -8 V V_{DESAT} = 9 V
Desaturation Sense to OUT Low Delay	$T_{DESATOUT}$	–	350	430	ns	V_{OUT} = 90% C_{LOAD} = 1 nF
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	–	–	2.25	µs	$V_{FLT\#}$ = 10%; $I_{FLT\#}$ = 5 mA
Desaturation Low Voltage	V_{DESATL}	0.4	0.6	0.95	V	IN+ = Low, IN- = Low, OUT = Low
Leading edge blanking	$T_{DESATleb}$	–	400	–	ns	Not subject of production test

5.4.8 Active Shut Down

Table 12 Active Shut Down

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active Shut Down Voltage	V_{ACTSD}[1)]	–	–	2.0	V	I_{OUT} = -200 mA, V_{CC2} open

1) With reference to VEE2

6 Insulation Characteristics

Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.

This coupler is suitable for “basic insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

6.1 Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12. Basic Insulation

Table 13 According to DIN EN 60747-5-2

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS}		 I-IV I-III I-II	–
Climatic Classification (IEC68-1)		40/105/21	–
Pollution Degree (EN 60664-1)		2	–
Minimum External Clearance	CLR	8.12	mm
Minimum External Creepage	CPG	8.24	mm
Minimum Comparative Tracking Index	CTI	175	–
Maximum Repetitive Insulation Voltage	V_{IORM}	1420	V_{PEAK}
Input to output test voltage, method b[1] V_{IORM} * 1.875 = V_{PR}, 100% production test with t_m = 1 sec, partial discharge < 5 pC	V_{PR}	2663	V_{PEAK}
Input to output test voltage, method a[1] V_{IORM} * 1.6 = V_{PR}, 100% production test with t_m = 60 sec, partial discharge < 5 pC	V_{PR}	2272	V_{PEAK}
Highest Allowable Overvoltage	V_{IOTM}	6000	V_{PEAK}
Maximum Surge Insulation Voltage	V_{IOSM}	6000	V
Insulation Resistance at $T_{S,}$ V_{IO} = 500 V	R_{IO}	> 10^9	Ω

1) Refer to VDE 0884 for a detailed description of Method a and Method b partial discharge test profiles.

6.2 Recognized under UL 1577 (File E311313)

Table 14 Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1 min	V_{ISO}	3750	V_{rms}
Insulation Test Voltage / 1 s	V_{ISO}	4500	V_{rms}

6.3 Reliability

For Qualification Report please contact your local Infineon Technologies office.

7 Timing Diagramms

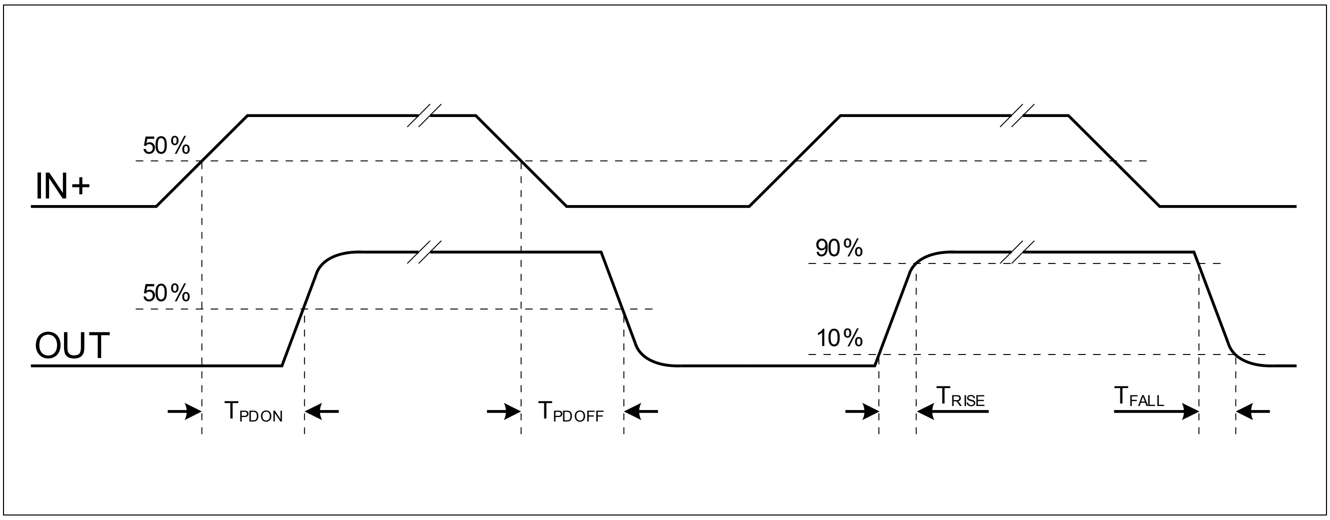


Figure 6 Propagation Delay, Rise and Fall Time

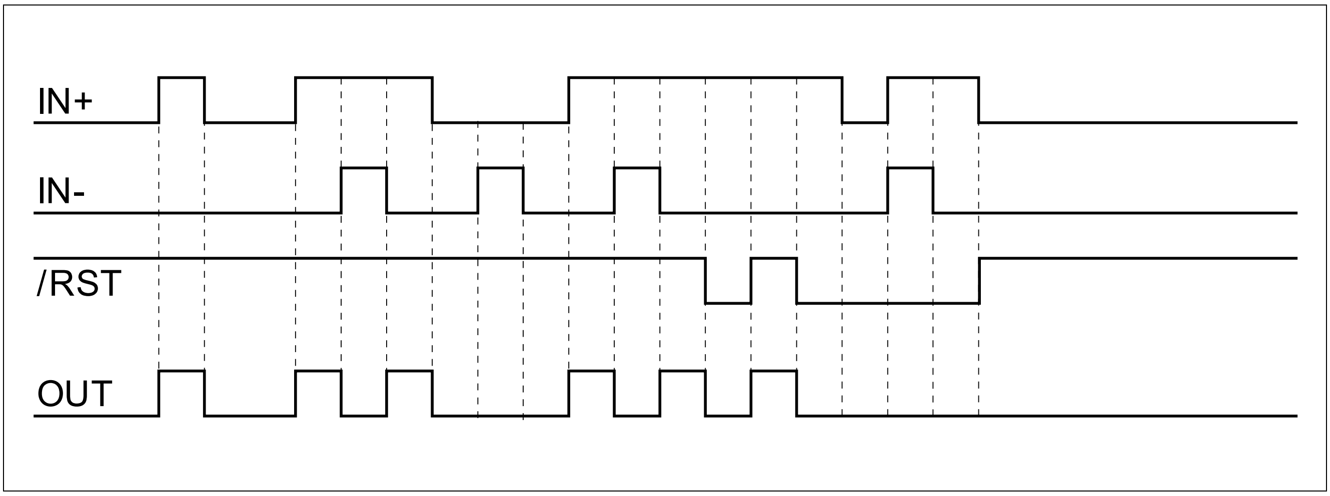


Figure 7 Typical Switching Behavior

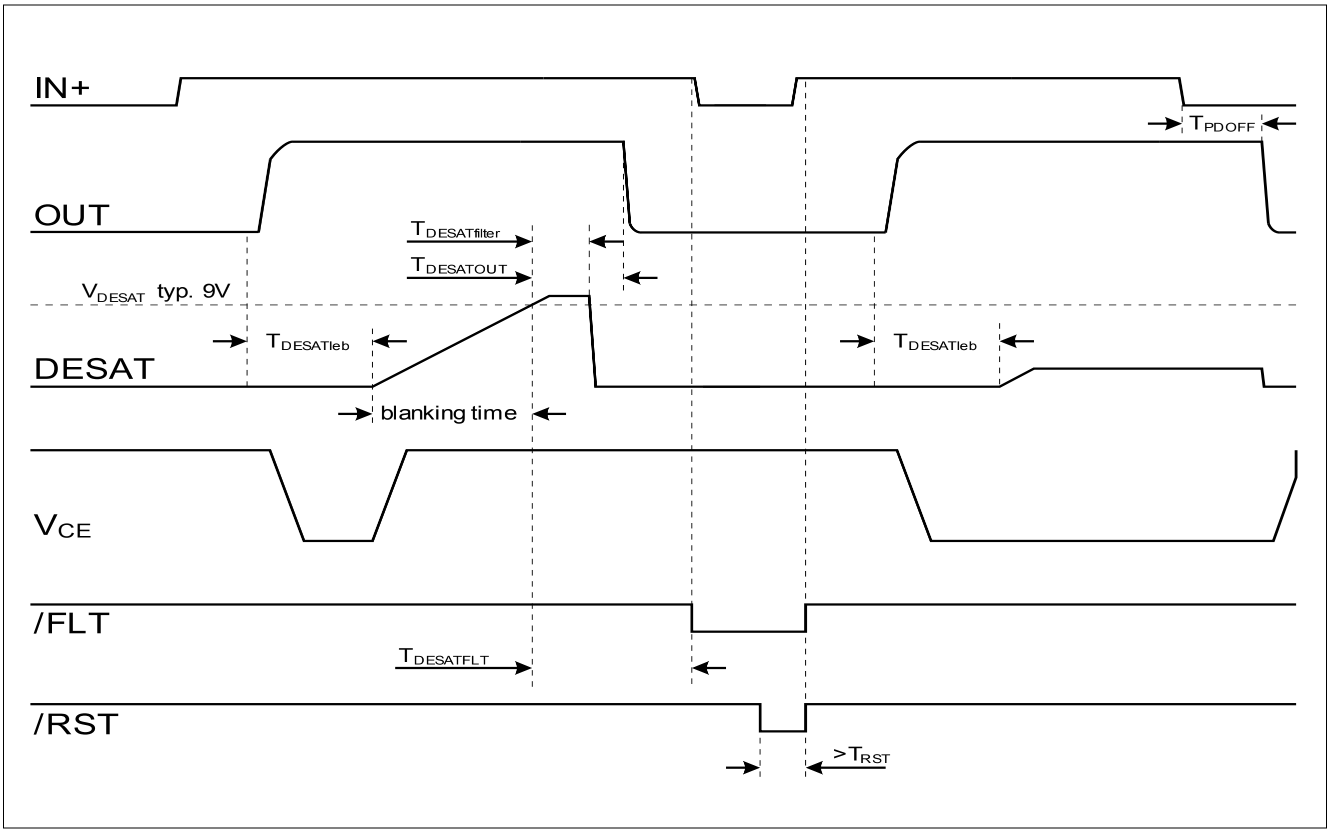


Figure 8 DESAT Switch-Off Behavior

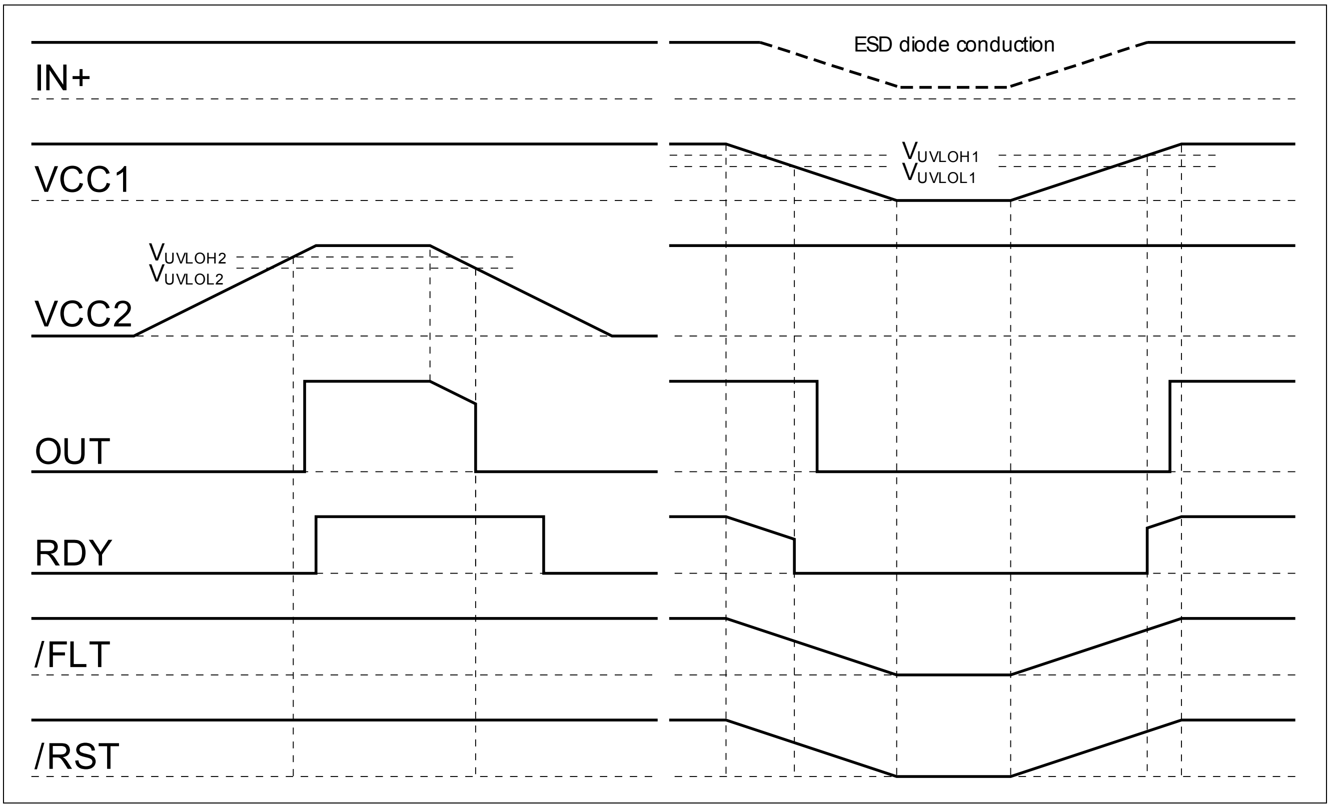
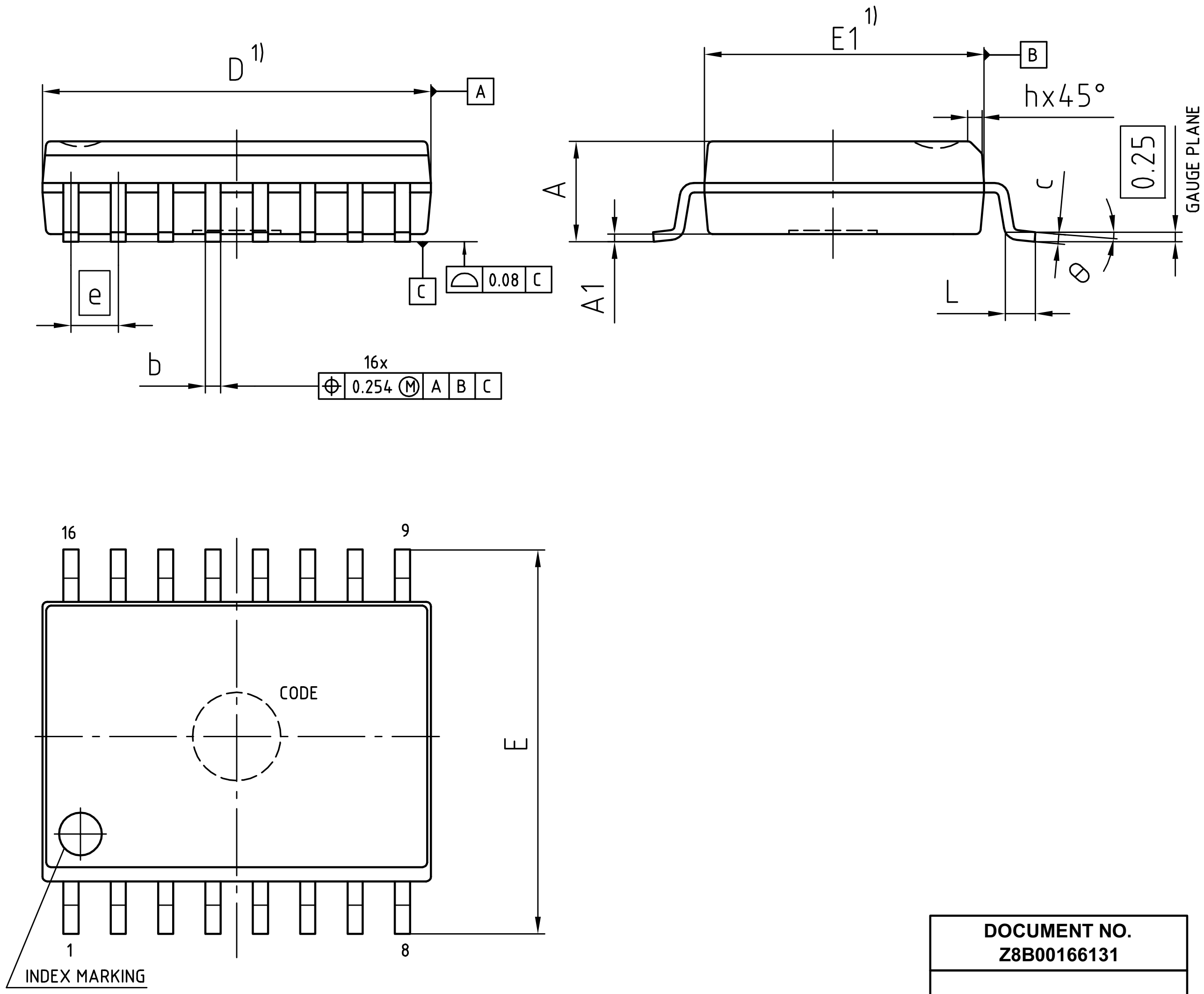


Figure 9 UVLO Behavior

8 Package Outlines



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.64	-	0.104
A1	0.12	0.29	0.005	0.011
b	0.35	0.48	0.014	0.019
c	0.23	0.32	0.009	0.013
D	10.21	10.47	0.402	0.412
E	10.16	10.41	0.400	0.410
E1	7.42	7.59	0.292	0.299
e	1.27 BSC		0.050 BSC	
N	16		16	
L	0.61	1.02	0.024	0.040
h	0.25	0.41	0.010	0.016
Θ	0°	8°	0°	8°

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SCALE 0 1.0 2mm

EUROPEAN PROJECTION

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02

Figure 10 PG-DSO-16-15 (Plastic (Green) Dual Small Outline Package)

9 Application Notes

9.1 Reference Layout for Thermal Data

The PCB layout shown in **Figure 11** represents the reference layout used for the thermal characterisation. Pins 9 and 16 (GND1) and pins 1 and 8 (VEE2) require ground plane connections for achiving maximum power dissipation. The 1ED020I12-B2 is conceived to dissipate most of the heat generated through this pins.

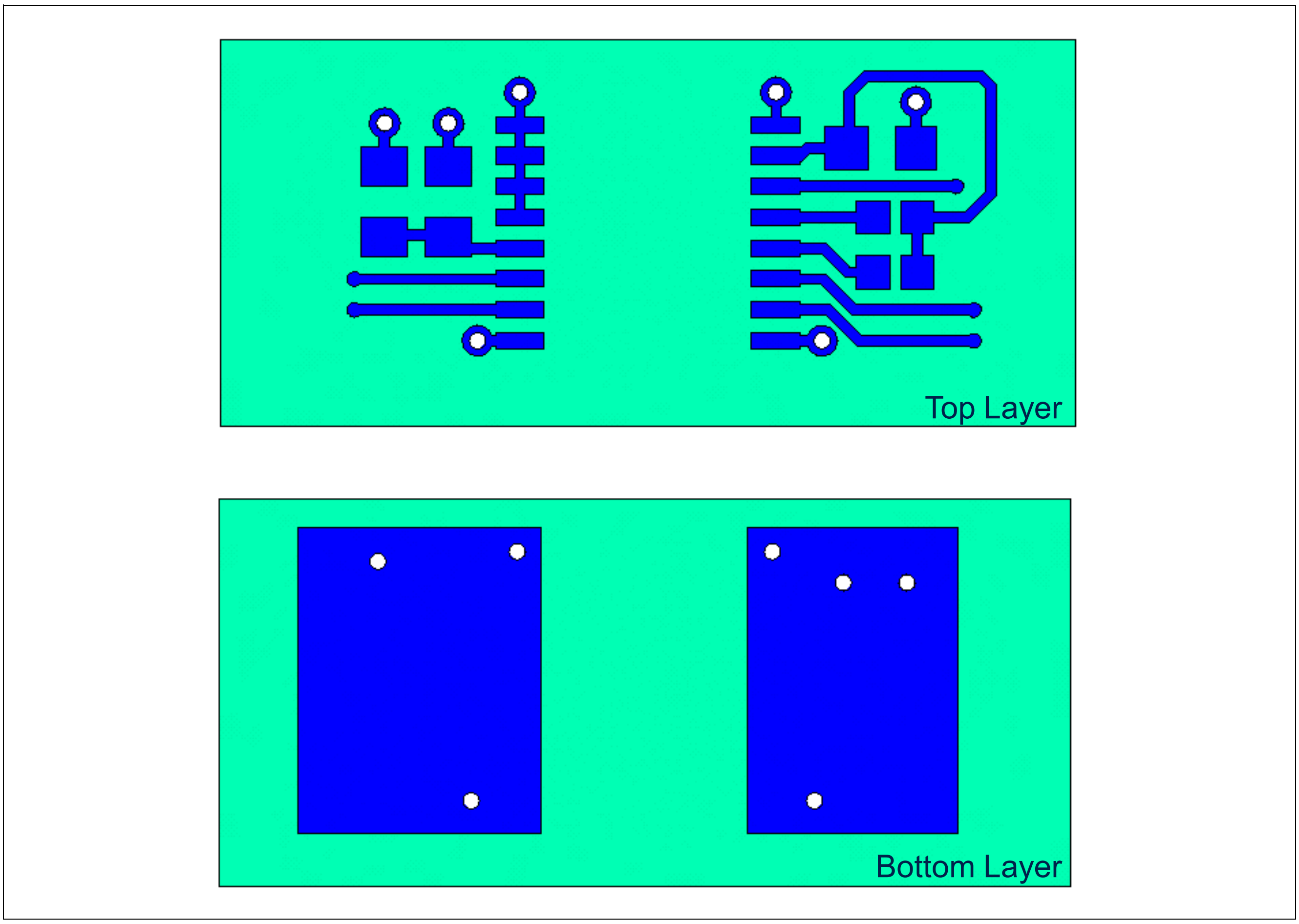

Figure 11 Reference Layout for Thermal Data (Copper thickness 102 µm)

9.2 Printed Circuit Board Guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.
- Lowest trace length for VEE2 to GND2 decoupling could be achieved with capacitor closed to pins 1 and 3.

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