

High Performance Microcontrollers with 10-bit A/D

High Performance RISC CPU:

- · C compiler optimized architecture/instruction set
 - Source code compatible with the PIC16CXX instruction set
- Linear program memory addressing to 2 Mbytes
- Linear data memory addressing to 4 Kbytes

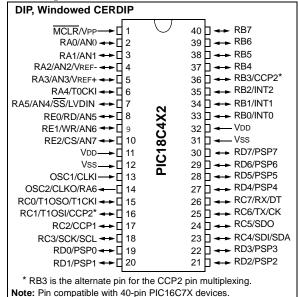
	On-Chip P	On-Chip		
Device	EPROM (bytes)	# Single Word Instructions	RAM (bytes)	
PIC18C242	16K	8192	512	
PIC18C252	32K	16384	1536	
PIC18C442	16K	8192	512	
PIC18C452	32K	16384	1536	

- Up to 10 MIPs operation:
 - DC 40 MHz osc./clock input
 - 4 MHz 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- · Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier

Peripheral Features:

- High current sink/source 25 mA/25 mA
- · Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter with 8-bit period register (time-base for PWM)
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules. CCP pins that can be configured as:
 - Capture input: capture is 16-bit, max. resolution 6.25 ns (Tcy/16)
 - Compare is 16-bit, max. resolution 100 ns (Tcy)
 - PWM output: PWM resolution is 1- to 10-bit. Max. PWM freq. @: 8-bit resolution = 156 kHz 10-bit resolution = 39 kHz
- · Master Synchronous Serial Port (MSSP) module. Two modes of operation:
 - 3-wire SPI (supports all 4 SPI modes)
 - I²C[™] master and slave mode
- · Addressable USART module:
 - Supports interrupt on Address bit
- · Parallel Slave Port (PSP) module

Pin Diagrams



Note: Pin compatible with 40-pin PIC16C7X devices.

Analog Features:

- · Compatible 10-bit Analog-to-Digital Converter module (A/D) with:
 - Fast sampling rate
 - Conversion available during SLEEP
 - DNL = ±1 LSb, INL = ±1 LSb
- Programmable Low Voltage Detection (LVD) module
 - Supports interrupt-on-low voltage detection
- Programmable Brown-out Reset (BOR)

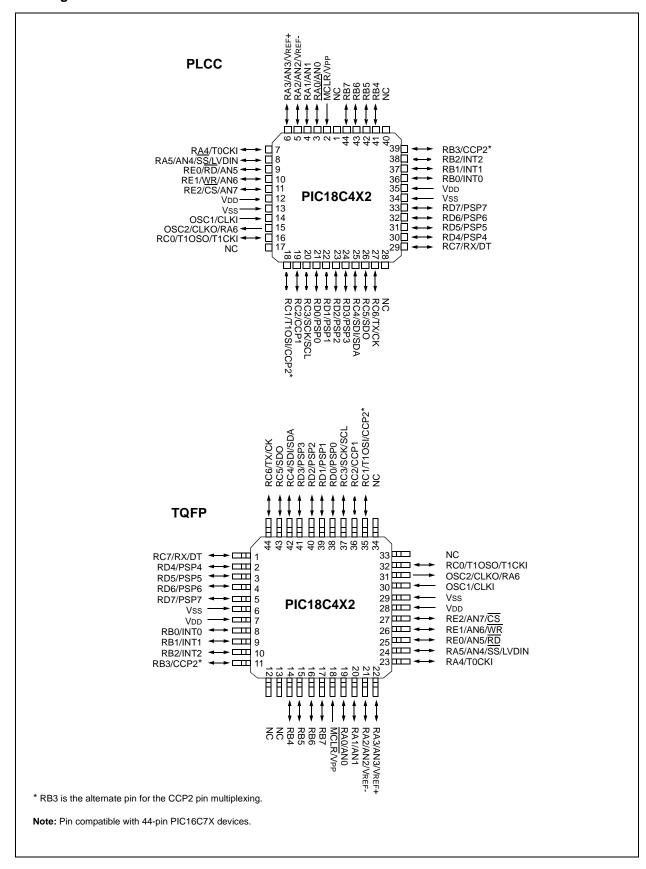
Special Microcontroller Features:

- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- · Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- · Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options including:
 - 4X Phase Lock Loop (of primary oscillator)
 - Secondary Oscillator (32 kHz) clock input
- In-Circuit Serial Programming (ICSP™) via two pins

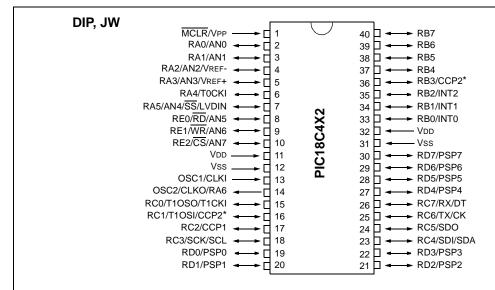
CMOS Technology:

- Low power, high speed EPROM technology
- · Fully static design
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- · Low power consumption

Pin Diagrams

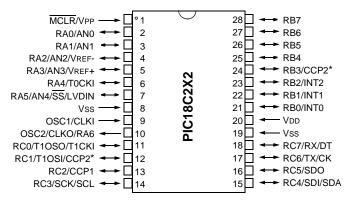


Pin Diagrams (Cont.'d)



Note: Pin compatible with 40-pin PIC16C7X devices.

DIP, SOIC, JW



^{*} RB3 is the alternate pin for the CCP2 pin multiplexing.

Note: Pin compatible with 28-pin PIC16C7X devices.

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the following four devices:

- 1. PIC18C242
- 2. PIC18C252
- 3. PIC18C442
- 4. PIC18C452

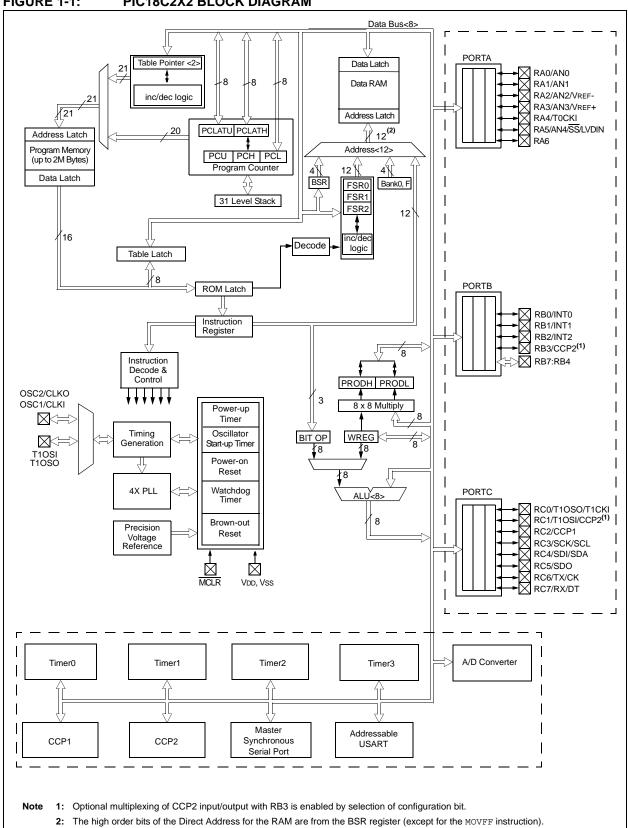
These devices come in 28-pin and 40-pin packages. The 28-pin devices do not have a Parallel Slave Port (PSP) implemented and the number of Analog-to-Digital (A/D) converter input channels is reduced to 5. An overview of features is shown in Table 1-1.

The following two figures are device block diagrams sorted by pin count: 28-pin for Figure 1-1 and 40-pin for Figure 1-2. The 28-pin and 40-pin pinouts are listed in Table 1-2 and Table 1-3, respectively.

TABLE 1-1: DEVICE FEATURES

Features	PIC18C242	PIC18C252	PIC18C442	PIC18C452
Operating Frequency	DC - 40 MHz			
Program Memory (Bytes)	16K	32K	16K	32K
Program Memory (Instructions)	8192	16384	8192	16384
Data Memory (Bytes)	512	1536	512	1536
Interrupt Sources	16	16	17	17
I/O Ports	Ports A, B, C	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART	MSSP, Addressable USART
Parallel Communications	_	_	PSP	PSP
10-bit Analog-to-Digital Module	5 input channels	5 input channels	8 input channels	8 input channels
RESETS (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)			
Programmable Low Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions	75 Instructions	75 Instructions	75 Instructions
Packages	28-pin DIP 28-pin SOIC 28-pin JW	28-pin DIP 28-pin SOIC 28-pin JW	40-pin DIP 44-pin PLCC 44-pin TQFP 40-pin JW	40-pin DIP 44-pin PLCC 44-pin TQFP 40-pin JW

PIC18C2X2 BLOCK DIAGRAM FIGURE 1-1:



- 3: Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations are device dependent.

FIGURE 1-2: PIC18C4X2 BLOCK DIAGRAM Data Bus<8> **PORTA** RA0/AN0 Data Latch Table Pointer <2> RA1/AN1 RA2/AN2/VRFF-Data RAM 8 (up to 4K RA3/AN3/VREF+ inc/dec logic address reach) RA4/T0CKI 21 RA5/AN4/SS/LVDIN Address Latch RA6 PCLATU PCLATH 12(2) Address Latch Program Memory (up to 2M Bytes) Address<12> PCU PCH PCL **PORTB** Program Counter 4 12 Data Latch BSR Bank0, F FSR0 RB0/INT0 FSR1 31 Level Stack RB1/INT1 FSR2 12 RB2/INT2 RB3/CCP2⁽¹⁾ 16 inc/dec RB7:RB4 Decode logic Table Latch **V**8 **PORTC** ROM Latch RC0/T1OSO/T1CKI RC1/T1OSI/CCP2(1) RC2/CCP1 Instruction Register RC3/SCK/SCL RC4/SDI/SDA 8 RC5/SDO Instruction Decode & RC6/TX/CK Control RC7/RX/DT PRODH PRODL OSC2/CLKO OSC1/CLKI 8 x 8 Multiply Power-up **PORTD** $\boxtimes \subseteq$ Timer RD0/PSP0 Timing Generation Oscillator RD1/PSP1 BIT OP WREG Start-up Timer RD2/PSP2 T10SI T10SO RD3/PSP3 Power-on RD4/PSP4 Reset RD5/PSP5 Watchdog 4X PLL RD6/PSP6 Timer RD7/PSP7 8 Precision Brown-out **PORTE** Voltage Reference Reset RE0/AN5/RD MCLR RE1/AN6/WR VDD, VSS RE2/AN7/CS A/D Converter Timer0 Timer1 Timer2 Timer3 ŢĹ Щ Master Addressable Synchronous CCP1 CCP2 Parallel Slave Port USART Serial Port 1: Optional multiplexing of CCP2 input/output with RB3 is enabled by selection of configuration bit. Note 2: The high order bits of the Direct Address for the RAM are from the BSR register (except for the MOVFF instruction). Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations

TABLE 1-2: PIC18C2X2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Buffer		Description		
r III Naille	DIP	SOIC	Type	Туре	Description		
MCLR/VPP MCLR	1	1	I	ST	Master clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active low RESET to the device.		
VPP			Р		Programming voltage input.		
NC	_	_	_	_	These pins should be left unconnected.		
OSC1/CLKI OSC1	9	0	1	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. CMOS otherwise.		
CLKI			I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKIN, OSC2/CLKOUT pins.)		
OSC2/CLKO/RA6 OSC2	10	10	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.		
CLKO			0	_	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.		
RA6			I/O	TTL	General Purpose I/O pin.		
					PORTA is a bi-directional I/O port.		
RA0/AN0	2	2					
RA0			I/O	TTL	Digital I/O.		
AN0			I	Analog	Analog input 0.		
RA1/AN1	3	3					
RA1			I/O	TTL	Digital I/O.		
AN1			ı	Analog	Analog input 1.		
RA2/AN2/VREF-	4	4					
RA2			I/O	TTL	Digital I/O.		
AN2 VREF-			-	Analog	Analog input 2.		
	_	_	'	Analog	A/D Reference Voltage (Low) input.		
RA3/AN3/VREF+ RA3	5	5	I/O	TTL	Digital I/O.		
AN3			1/0	Analog	Analog input 3.		
VREF+			i	Analog	A/D Reference Voltage (High) input.		
RA4/T0CKI	6	6	•	7a.og	7 02 (total and total go (t light) in pair		
RA4	U	O	I/O	ST/OD	Digital I/O. Open drain when configured as output.		
T0CKI			١	ST	Timer0 external clock input.		
RA5/AN4/SS/LVDIN	7	7			·		
RA5			I/O	TTL	Digital I/O.		
AN4			I	Analog	Analog input 4.		
SS			I	ST	SPI Slave Select input.		
LVDIN			I	Analog	Low Voltage Detect Input.		
RA6					See the OSC2/CLKO/RA6 pin.		

CMOS = CMOS compatible input or output

O = Output

P = Power

TABLE 1-2: PIC18C2X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Buffer		Description		
riii Naille	DIP	SOIC	Туре	Туре	Description		
					PORTB is a bi-directional I/O port. PORTB can be software		
					programmed for internal weak pull-ups on all inputs.		
RB0/INT0	21	21					
RB0			I/O	TTL	Digital I/O.		
INT0			I	ST	External Interrupt 0.		
RB1/INT1	22	22					
RB1			I/O	TTL			
INT1			I	ST	External Interrupt 1.		
RB2/INT2	23	23					
RB2			I/O	TTL	Digital I/O.		
INT2			I	ST	External Interrupt 2.		
RB3/CCP2	24	24					
RB3			I/O	TTL	Digital I/O.		
CCP2			I/O	ST	Capture2 input, Compare2 output, PWM2 output.		
RB4	25	25	I/O	TTL	Digital I/O.		
					Interrupt-on-change pin.		
RB5	26	26	I/O	TTL	Digital I/O.		
					Interrupt-on-change pin.		
RB6	27	27	I/O	TTL	Digital I/O.		
					Interrupt-on-change pin.		
			I	ST	ICSP programming clock.		
RB7	28	28	I/O	TTL	Digital I/O.		
					Interrupt-on-change pin.		
			I/O	ST	ICSP programming data.		

CMOS = CMOS compatible input or output

P = Power

O = Output

TABLE 1-2: PIC18C2X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Din Name	Pin Number		Pin Buffe		Decembries
Pin Name	DIP	SOIC	Туре	Type	Description
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11			
RC0			I/O	ST	Digital I/O.
T1OSO			0	_	Timer1 oscillator output.
T1CKI			I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	12	12			
RC1			I/O	ST	Digital I/O.
T1OSI			I	CMOS	Timer1 oscillator input.
CCP2			I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	13			
RC2			I/O	ST	Digital I/O.
CCP1			I/O	ST	Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14			
RC3			I/O	ST	Digital I/O.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL			I/O	ST	Synchronous serial clock input/output for I ² C mode.
RC4/SDI/SDA	15	15			
RC4			I/O	ST	Digital I/O.
SDI			I	ST	SPI Data In.
SDA			I/O	ST	I ² C Data I/O.
RC5/SDO	16	16			
RC5			I/O	ST	Digital I/O.
SDO			0	_	SPI Data Out.
RC6/TX/CK	17	17			
RC6			I/O	ST	Digital I/O.
TX			0	_	USART Asynchronous Transmit.
CK			I/O	ST	USART Synchronous Clock (see related RX/DT).
RC7/RX/DT	18	18			
RC7			I/O	ST	Digital I/O.
RX			I	ST	USART Asynchronous Receive.
DT			I/O	ST	USART Synchronous Data (see related TX/CK).
Vss	8, 19	8, 19	Р		Ground reference for logic and I/O pins.
VDD	20	20	Р	_	Positive supply for logic and I/O pins.

ST = Schmitt Trigger input with CMOS levels I = Input

O = Output

OD = Open Drain (no P diode to VDD)

CMOS = CMOS compatible input or output

P = Power

TABLE 1-3: PIC18C4X2 PINOUT I/O DESCRIPTIONS

Din Nome	Pi	n Numb	er	Pin	Buffer	Description
Pin Name	DIP	PLCC	TQFP	Туре	Type	Description
MCLR/VPP MCLR	1	2	18	I	ST	Master clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active low RESET to the device.
VPP				Р		Programming voltage input.
NC	1			_	_	These pins should be left unconnected.
OSC1/CLKI OSC1	13	14	30	_	ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise.
CLKI				ı	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKIN, OSC2/CLKOUT pins.)
OSC2/CLKO/RA6	14	15	31			Oscillator crystal output.
OSC2				0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				0	_	In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General Purpose I/O pin.
				., 0		PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	4	20			21.11.11.0
RA1				I/O	TTL	Digital I/O.
AN1	4	5	24	ı	Analog	Analog input 1.
RA2/AN2/VREF- RA2	4	5	21	I/O	TTL	Digital I/O.
AN2				ľ	Analog	Analog input 2.
VREF-				- 1	Analog	A/D Reference Voltage (Low) input.
RA3/AN3/VREF+	5	6	22			
RA3				I/O	TTL	Digital I/O.
AN3 VREF+					Analog	Analog input 3. A/D Reference Voltage (High) input.
	G	7	22	'	Analog	A/D Reference voltage (Figh) input.
RA4/T0CKI RA4	6	7	23	I/O	ST/OD	Digital I/O. Open drain when configured as output.
T0CKI				ľ	ST	Timer0 external clock input.
RA5/AN4/SS/LVDIN	7	8	24			·
RA5				I/O	TTL	Digital I/O.
AN4				1	Analog	Analog input 4.
SS					ST	SPI Slave Select input.
LVDIN				ı	Analog	Low Voltage Detect Input.
RA6					CM	See the OSC2/CLKO/RA6 pin.

CMOS = CMOS compatible input or output

P = Power

O = Output

TABLE 1-3: PIC18C4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Din Name	Pi	n Numb	er	Pin	Buffer	Description
Pin Name	DIP	PLCC	TQFP	Туре	Type	Description
						PORTB is a bi-directional I/O port. PORTB can be
						software programmed for internal weak pull-ups on all inputs.
RB0/INT0	33	36	8			
RB0				I/O	TTL	Digital I/O.
INT0				- 1	ST	External Interrupt 0.
RB1/INT1	34	37	9			
RB1				I/O	TTL	
INT1				- 1	ST	External Interrupt 1.
RB2/INT2	35	38	10			
RB2				I/O	TTL	Digital I/O.
INT2				I	ST	External Interrupt 2.
RB3/CCP2	36	39	11			
RB3				I/O	TTL	Digital I/O.
CCP2				I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RB4	37	41	14	I/O	TTL	Digital I/O. Interrupt-on-change pin.
RB5	38	42	15	I/O	TTL	Digital I/O. Interrupt-on-change pin.
RB6	39	43	16	I/O	TTL	Digital I/O. Interrupt-on-change pin.
				ı	ST	ICSP programming clock.
RB7	40	44	17	I/O	TTL	Digital I/O. Interrupt-on-change pin.
				I/O	ST	ICSP programming data.

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels I = Input

O = Output

P = Power

TABLE 1-3: PIC18C4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pi	Pin Number			Pin Buffer	Description	
Pin Name	DIP	PLCC	TQFP	Туре	Туре	Description	
						PORTC is a bi-directional I/O port.	
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	16	32	I/O O -	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.	
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.	
RC2/CCP1 RC2 CCP1	17	19	36	I/O I/O	ST ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.	
RC3/SCK/SCL RC3 SCK	18	20	37	I/O I/O	ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode.	
SCL				I/O	ST	Synchronous serial clock input/output for I ² C mode.	
RC4/SDI/SDA RC4 SDI SDA	23	25	42	I/O I I/O	ST ST ST	Digital I/O. SPI Data In. I ² C Data I/O.	
RC5/SDO RC5 SDO	24	26	43	I/O O	ST —	Digital I/O. SPI Data Out.	
RC6/TX/CK RC6 TX CK	25	27	44	I/O O I/O	ST — ST	Digital I/O. USART Asynchronous Transmit. USART Synchronous Clock (see related RX/DT).	
RC7/RX/DT RC7 RX DT	26	29	1	I/O /O	ST ST ST	Digital I/O. USART Asynchronous Receive. USART Synchronous Data (see related TX/CK).	

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels I = Input O = Output P = Power

TABLE 1-3: PIC18C4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pi	n Numb	er	Pin	Buffer	Description
riii Naille	DIP	PLCC	TQFP	Туре	Туре	Description
						PORTD is a bi-directional I/O port, or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when PSP module is enabled.
RD0/PSP0	19	21	38	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD1/PSP1	20	22	39	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD2/PSP2	21	23	40	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD3/PSP3	22	24	41	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD4/PSP4	27	30	2	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD5/PSP5	28	31	3	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD6/PSP6	29	32	4	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD7/PSP7	30	33	5	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RE0/RD/AN5 RE0 RD	8	9	25	I/O	PORTE is a bi-directional I/O port. ST Digital I/O.	
AN5 RE1/WR/AN6	9	10	26	I/O	TTL Analog	Read control for parallel slave port (see also WR and CS pins). Analog input 5.
RE1 WR			20	2	ST TTL	Digital I/O. Write control for parallel slave port (see $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins).
AN6 RE2/CS/AN7 RE2	10	11	27	I/O	Analog ST	Analog input 6. Digital I/O.
CS					TTL	Chip Select control for parallel slave port (see related RD and WR).
AN7 Vss	10 04	13, 34	6, 29	P	Analog	Analog input 7.
					_	Ground reference for logic and I/O pins.
VDD	11, 32	12, 35	7, 28	Р		Positive supply for logic and I/O pins.

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels I = Input

O = Output

P = Power

2.0 OSCILLATOR CONFIGURATIONS

2.1 Oscillator Types

The PIC18CXX2 can be operated in eight different oscillator modes. The user can program three configuration bits (FOSC2, FOSC1, and FOSC0) to select one of these eight modes:

1.	LP	Low Power Crystal
2.	XT	Crystal/Resonator
3.	HS	High Speed Crystal/Resonator
4.	HS + PLL	High Speed Crystal/Resonator with x 4 PLL enabled
5.	RC	External Resistor/Capacitor
6.	RCIO	External Resistor/Capacitor with RA6 I/O pin enabled
7.	EC	External Clock
8.	ECIO	External Clock with RA6 I/O pin enabled

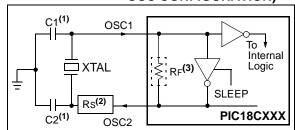
2.2 Crystal Oscillator/Ceramic Resonators

In XT, LP, HS or HS-PLL oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections.

The PIC18CXX2 oscillator design requires the use of a parallel cut crystal.

Note: Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications.

FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

- A series resistor (Rs) may be required for AT strip cut crystals.
- 3: RF varies with the osc mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:								
Mode	Freq	C1	C2					
XT	455 kHz	68 - 100 pF	68 - 100 pF					
	2.0 MHz	15 - 68 pF	15 - 68 pF					
	4.0 MHz	15 - 68 pF	15 - 68 pF					
HS	8.0 MHz	10 - 68 pF	10 - 68 pF					
	16.0 MHz	10 - 22 pF	10 - 22 pF					
	following this		only.					
	Resona	ators Used:						
455 kHz	Panasonic E	FO-A455K04B	± 0.3%					
2.0 MHz	Murata Erie	CSA2.00MG	± 0.5%					
4.0 MHz	Murata Erie	CSA4.00MG	± 0.5%					
8.0 MHz	Murata Erie CSA8.00MT ± 0.5%							
16.0 MHz	Murata Erie	CSA16.00MX	± 0.5%					
All resonat	ors used did r	not have built-in	capacitors.					

- **Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
 - **2:** When operating below 3V VDD, it may be necessary to use high gain HS mode on lower frequency ceramic resonators.
 - **3:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components or verify oscillator performance.

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

	Ranges Tested:								
Mode	Freq	C1	C2						
LP	32.0 kHz	33 pF	33 pF						
	200 kHz	15 pF	15 pF						
XT	200 kHz	47-68 pF	47-68 pF						
	1.0 MHz	15 pF	15 pF						
	4.0 MHz	15 pF	15 pF						
HS	4.0 MHz	15 pF	15 pF						
	8.0 MHz	15-33 pF	15-33 pF						
	20.0 MHz	15-33 pF	15-33 pF						
	25.0 MHz	15-33 pF	15-33 pF						

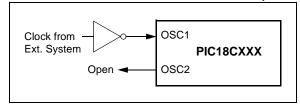
These values are for design guidance only. See notes following this table.

Coe netoe renemming time table.								
Crystals Used								
32.0 kHz	Epson C-001R32.768K-A	± 20 PPM						
200 kHz	STD XTL 200.000kHz	± 20 PPM						
1.0 MHz	ECS ECS-10-13-1	± 50 PPM						
4.0 MHz	ECS ECS-40-20-1	± 50 PPM						
8.0 MHz	Epson CA-301 8.000M-C	± 30 PPM						
20.0 MHz	Epson CA-301 20.000M-C	± 30 PPM						

- **Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
 - 2: Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components or verify oscillator performance.

An external clock source may also be connected to the OSC1 pin in these modes, as shown in Figure 2-2.

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP CONFIGURATION)

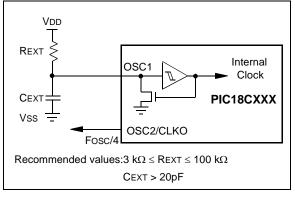


2.3 RC Oscillator

For timing insensitive applications, the "RC" and "RCIO" device options offer additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 2-3 shows how the R/C combination is connected.

In the RC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic.

FIGURE 2-3: RC OSCILLATOR MODE



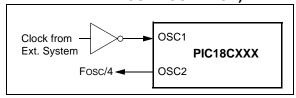
The RCIO oscillator mode functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

2.4 External Clock Input

The EC and ECIO oscillator modes require an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is no oscillator start-up time required after a Power-on Reset or after a recovery from SLEEP mode.

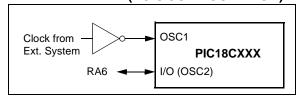
In the EC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC OSC CONFIGURATION)



The ECIO oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)



2.5 HS/PLL

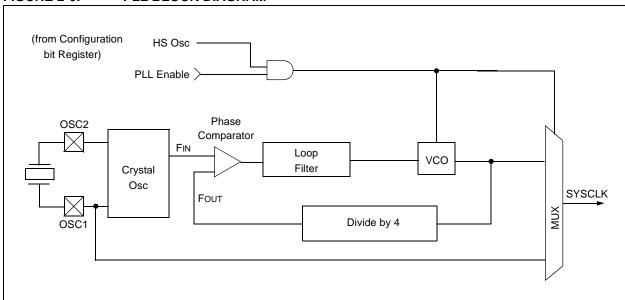
A Phase Locked Loop circuit is provided as a programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 10 MHz, the internal clock frequency will be multiplied to 40 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL can only be enabled when the oscillator configuration bits are programmed for HS mode. If they are programmed for any other mode, the PLL is not enabled and the system clock will come directly from OSC1.

The PLL is one of the modes of the FOSC<2:0> configuration bits. The oscillator mode is specified during device programming.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out that is called TPLL.

FIGURE 2-6: PLL BLOCK DIAGRAM

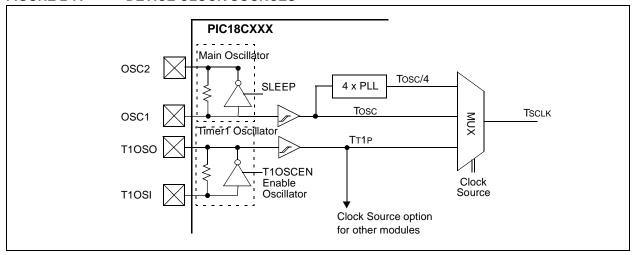


2.6 Oscillator Switching Feature

The PIC18CXX2 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low frequency clock source. For the PIC18CXX2 devices, this alternate clock source is the Timer1 oscillator. If a low frequency crystal (32 kHz, for example) has been attached to the Timer1 oscillator pins and the Timer1 oscillator has

been enabled, the device can switch to a low power execution mode. Figure 2-7 shows a block diagram of the system clock sources. The clock switching feature is enabled by programming the Oscillator Switching Enable (OSCSEN) bit in Configuration Register1H to a '0'. Clock switching is disabled in an erased device. See Section 9.0 for further details of the Timer1 oscillator. See Section 18.0 for Configuration Register details.

FIGURE 2-7: DEVICE CLOCK SOURCES



2.6.1 SYSTEM CLOCK SWITCH BIT

The system clock source switching is performed under software control. The system clock switch bit, SCS (OSCCON<0>) controls the clock switching. When the SCS bit is'0', the system clock source comes from the main oscillator that is selected by the FOSC configuration bits in Configuration Register1H. When the SCS bit is set, the system clock source will come from the Timer1 oscillator. The SCS bit is cleared on all forms of RESET.

The Timer1 oscillator must be enabled and operating to switch the system clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 control register (T1CON). If the Timer1 oscillator is not enabled, then any write to the SCS bit will be ignored (SCS bit forced cleared) and the main oscillator will continue to be the system clock source.

REGISTER 2-1: OSCCON REGISTER

_	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	_	_	_	_	_	-	_	SCS
	bit 7							bit 0

Note:

bit 7-1 Unimplemented: Read as '0'

bit 0 SCS: System Clock Switch bit

When OSCSEN configuration bit = '0' and T1OSCEN bit is set:

- 1 = Switch to Timer1 oscillator/clock pin
- 0 = Use primary oscillator/clock input pin

When OSCSEN and T1OSCEN are in other states:

bit is forced clear

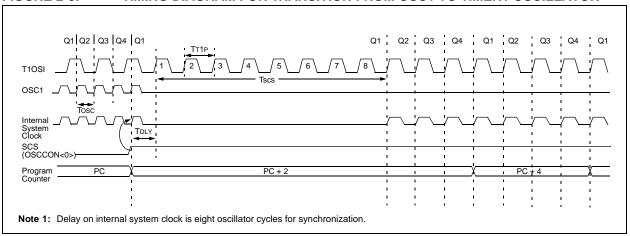
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.6.2 OSCILLATOR TRANSITIONS

The PIC18CXX2 devices contain circuitry to prevent "glitches" when switching between oscillator sources. Essentially, the circuitry waits for eight rising edges of the clock source that the processor is switching to. This ensures that the new clock source is stable and that it's pulse width will not be less than the shortest pulse width of the two clock sources.

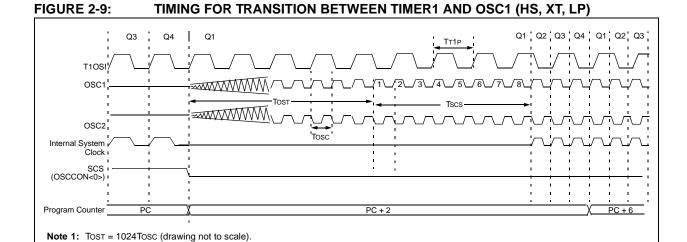
A timing diagram indicating the transition from the main oscillator to the Timer1 oscillator is shown in Figure 2-8. The Timer1 oscillator is assumed to be running all the time. After the SCS bit is set, the processor is frozen at the next occurring Q1 cycle. After eight synchronization cycles are counted from the Timer1 oscillator, operation resumes. No additional delays are required after the synchronization cycles.

FIGURE 2-8: TIMING DIAGRAM FOR TRANSITION FROM OSC1 TO TIMER1 OSCILLATOR



The sequence of events that takes place when switching from the Timer1 oscillator to the main oscillator will depend on the mode of the main oscillator. In addition to eight clock cycles of the main oscillator, additional delays may take place.

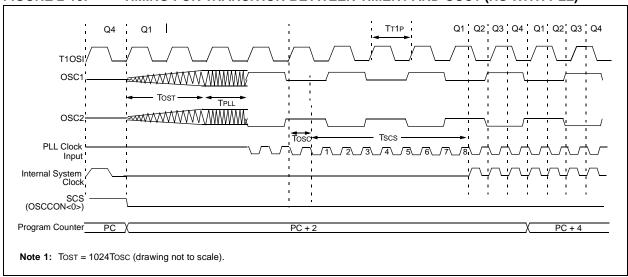
If the main oscillator is configured for an external crystal (HS, XT, LP), then the transition will take place after an oscillator start-up time (TOST) has occurred. A timing diagram indicating the transition from the Timer1 oscillator to the main oscillator for HS, XT and LP modes is shown in Figure 2-9.



If the main oscillator is configured for HS-PLL mode, an oscillator start-up time (Tost) plus an additional PLL time-out (TPLL) will occur. The PLL time-out is typically 2 ms and allows the PLL to lock to the main oscillator

frequency. A timing diagram, indicating the transition from the Timer1 oscillator to the main oscillator for HS-PLL mode, is shown in Figure 2-10.

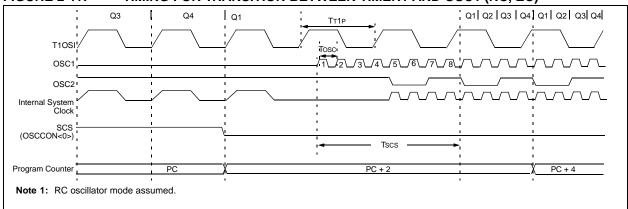
FIGURE 2-10: TIMING FOR TRANSITION BETWEEN TIMER1 AND OSC1 (HS WITH PLL)



If the main oscillator is configured in the RC, RCIO, EC or ECIO modes, there is no oscillator start-up time-out. Operation will resume after eight cycles of the main oscillator have been counted. A timing diagram, indi-

cating the transition from the Timer1 oscillator to the main oscillator for RC, RCIO, EC and ECIO modes, is shown in Figure 2-11.

FIGURE 2-11: TIMING FOR TRANSITION BETWEEN TIMER1 AND OSC1 (RC, EC)



2.7 Effects of SLEEP Mode on the On-chip Oscillator

When the device executes a SLEEP instruction, the on-chip clocks and oscillator are turned off and the device is held at the beginning of an instruction cycle (Q1 state). With the oscillator off, the OSC1 and OSC2 signals will stop oscillating. Since all the transistor

switching currents have been removed, SLEEP mode achieves the lowest current consumption of the device (only leakage currents). Enabling any on-chip feature that will operate during SLEEP will increase the current consumed during SLEEP. The user can wake from SLEEP through external RESET, Watchdog Timer Reset, or through an interrupt.

TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

OSC Mode	OSC1 Pin	OSC2 Pin
RC	Floating, external resistor should pull high	At logic low
RCIO	Floating, external resistor should pull high	Configured as PORTA, bit 6
ECIO	Floating	Configured as PORTA, bit 6
EC	Floating	At logic low
LP, XT, and HS	Feedback inverter disabled, at quiescent voltage level	Feedback inverter disabled, at quiescent voltage level

Note: See Table 3-1, in Section 3.0 RESET, for time-outs due to SLEEP and MCLR Reset.

2.8 Power-up Delays

Power up delays are controlled by two timers, so that no external RESET circuitry is required for most applications. The delays ensure that the device is kept in RESET until the device power supply and clock are stable. For additional information on RESET operation, see the "RESET" section.

The first timer is the Power-up Timer (PWRT), which optionally provides a fixed delay of 72 ms (nominal) on power-up only (POR and BOR). The second timer is the Oscillator Start-up Timer, OST, intended to keep the chip in RESET until the crystal oscillator is stable.

With the PLL enabled (HS/PLL oscillator mode), the time-out sequence following a Power-on Reset is different from other oscillator modes. The time-out sequence is as follows: First, the PWRT time-out is invoked after a POR time delay has expired. Then, the Oscillator Start-up Timer (OST) is invoked. However, this is still not a sufficient amount of time to allow the PLL to lock at high frequencies. The PWRT timer is used to provide an additional fixed 2ms (nominal) time-out to allow the PLL ample time to lock to the incoming clock frequency.

NOTES:

3.0 RESET

The PIC18CXX2 differentiates between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) Watchdog Timer (WDT) Reset (during normal operation)
- e) Programmable Brown-out Reset (BOR)
- f) RESET Instruction
- g) Stack Full Reset
- h) Stack Underflow Reset

Most registers are unaffected by a RESET. Their status is unknown on POR and unchanged by all other RESETS. The other registers are forced to a "RESET state" on Power-on Reset, MCLR, WDT Reset, Brownout Reset, MCLR Reset during SLEEP, and by the RESET instruction.

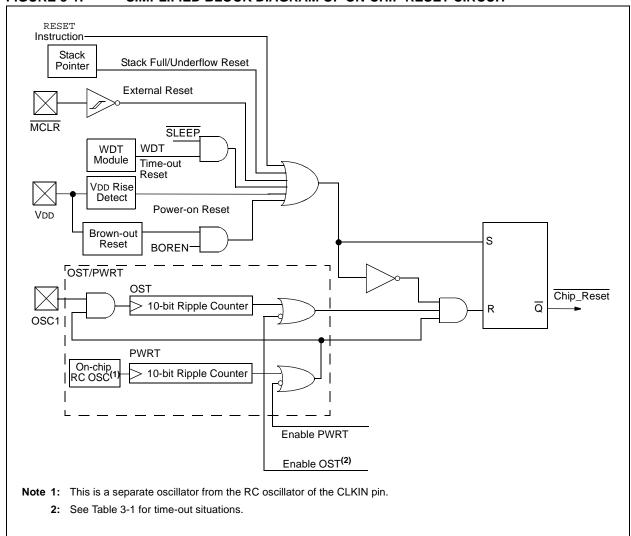
Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, RI, TO, PD, POR and BOR, are set or cleared differently in different RESET situations, as indicated in Table 3-2. These bits are used in software to determine the nature of the RESET. See Table 3-3 for a full description of the RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 3-1.

The Enhanced MCU devices have a $\overline{\text{MCLR}}$ noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

MCLR pin is not driven low by any internal RESETS, including WDT.

FIGURE 3-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

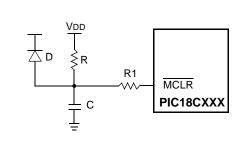


3.1 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected. To take advantage of the POR circuitry, just tie the MCLR pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004). For a slow rise time, see Figure 3-2.

When the device starts normal operation (i.e., exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

FIGURE 3-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow.

The diode D helps discharge the capacitor quickly when VDD powers down.

- 2: $R < 40 \text{ k}\Omega$ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.
- 3: R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR}/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

3.2 Power-up Timer (PWRT)

The Power-up Timer provides a fixed nominal time-out (parameter #33) only on power-up from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/ disable the PWRT.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameter #33 for details.

3.3 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (parameter #32). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

3.4 PLL Lock Time-out

With the PLL enabled, the time-out sequence following a Power-on Reset is different from other oscillator modes. A portion of the Power-up Timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out (TPLL) is typically 2 ms and follows the oscillator start-up time-out (OST).

3.5 Brown-out Reset (BOR)

A configuration bit, BOREN, can disable (if clear/programmed), or enable (if set) the Brown-out Reset circuitry. If VDD falls below parameter D005 for greater than parameter #35, the brown-out situation will reset the chip. A RESET may not occur if VDD falls below parameter D005 for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will then be invoked and will keep the chip in RESET an additional time delay (parameter #33). If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute the additional time delay.

3.6 Time-out Sequence

On power-up, the time-out sequence is as follows: First, PWRT time-out is invoked after the POR time delay has expired. Then, OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 3-3, Figure 3-4, Figure 3-5, Figure 3-6 and Figure 3-7 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Bringing MCLR high will begin execution immediately (Figure 3-5). This is useful for testing purposes or to synchronize more than one PIC18CXXX device operating in parallel.

Table 3-2 shows the RESET conditions for some Special Function Registers, while Table 3-3 shows the RESET conditions for all the registers.

TABLE 3-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator	Power-up	(2)	(2)	Wake-up from
Configuration	PWRTE = 0	PWRTE = 1	Brown-out ⁽²⁾	SLEEP or Oscillator Switch
HS with PLL enabled ⁽¹⁾	72 ms + 1024Tosc + 2ms	1024Tosc + 2 ms	72 ms + 1024Tosc + 2ms	1024Tosc + 2 ms
HS, XT, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc
EC	72 ms	_	72 ms	_
External RC	72 ms	_	72 ms	_

Note 1: 2 ms is the nominal time required for the 4x PLL to lock.

2: 72 ms is the nominal Power-up Timer delay.

REGISTER 3-1: RCON REGISTER BITS AND POSITIONS

R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
IPEN	LWRT	_	RI	TO	PD	POR	BOR
bit 7							bit 0

Note: See Register 4-3 on page 53 for bit definitions.

TABLE 3-2: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter	RCON Register	RI	то	PD	POR	BOR	STKFUL	STKUNF
Power-on Reset	0000h	00-1 1100	1	1	1	0	0	u	u
MCLR Reset during normal operation	0000h	00-u uuuu	u	u	u	u	u	u	u
Software Reset during normal operation	0000h	0u-0 uuuu	0	u	u	u	u	u	u
Stack Full Reset during normal operation	0000h	0u-u uu11	u	u	u	u	u	u	1
Stack Underflow Reset during normal operation	0000h	0u-u uu11	u	u	u	u	u	1	u
MCLR Reset during SLEEP	0000h	00-u 10uu	u	1	0	u	u	u	u
WDT Reset	0000h	0u-u 01uu	1	0	1	u	u	u	u
WDT Wake-up	PC + 2	uu-u 00uu	u	0	0	u	u	u	u
Brown-out Reset	0000h	0u-1 11u0	1	1	1	1	0	u	u
Interrupt wake-up from SLEEP	PC + 2 ⁽¹⁾	uu-u 00uu	u	1	0	u	u	u	u

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (0x000008h or 0x000018h).

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TOSU	242	442	252	452	0 0000	0 0000	0 uuuu (3)
TOSH	242	442	252	452	0000 0000	0000 0000	uuuu uuuu(3)
TOSL	242	442	252	452	0000 0000	0000 0000	uuuu uuuu ⁽³⁾
STKPTR	242	442	252	452	00-0 0000	00-0 0000	uu-u uuuu ⁽³⁾
PCLATU	242	442	252	452	0 0000	0 0000	u uuuu
PCLATH	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
PCL	242	442	252	452	0000 0000	0000 0000	PC + 2 ⁽²⁾
TBLPTRU	242	442	252	452	00 0000	00 0000	uu uuuu
TBLPTRH	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
TABLAT	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
PRODH	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	242	442	252	452	0000 000x	0000 000u	uuuu uuuu(1)
INTCON2	242	442	252	452	1111 -1-1	1111 -1-1	uuuu -u-u ⁽¹⁾
INTCON3	242	442	252	452	11-0 0-00	11-0 0-00	uu-u u-uu ⁽¹⁾
INDF0	242	442	252	452	N/A	N/A	N/A
POSTINC0	242	442	252	452	N/A	N/A	N/A
POSTDEC0	242	442	252	452	N/A	N/A	N/A
PREINC0	242	442	252	452	N/A	N/A	N/A
PLUSW0	242	442	252	452	N/A	N/A	N/A
FSR0H	242	442	252	452	0000	0000	uuuu
FSR0L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	242	442	252	452	N/A	N/A	N/A
POSTINC1	242	442	252	452	N/A	N/A	N/A
POSTDEC1	242	442	252	452	N/A	N/A	N/A
PREINC1	242	442	252	452	N/A	N/A	N/A
PLUSW1	242	442	252	452	N/A	N/A	N/A

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

- Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 4: See Table 3-2 for RESET value for specific condition.
 - **5:** Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
 - **6:** The long write enable is only reset on a POR or \overline{MCLR} Reset.
 - 7: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read as '0'.

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices			ces	Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
FSR1H	242	442	252	452	0000	0000	uuuu
FSR1L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	242	442	252	452	0000	0000	uuuu
INDF2	242	442	252	452	N/A	N/A	N/A
POSTINC2	242	442	252	452	N/A	N/A	N/A
POSTDEC2	242	442	252	452	N/A	N/A	N/A
PREINC2	242	442	252	452	N/A	N/A	N/A
PLUSW2	242	442	252	452	N/A	N/A	N/A
FSR2H	242	442	252	452	0000	0000	uuuu
FSR2L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	242	442	252	452	x xxxx	u uuuu	u uuuu
TMR0H	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	242	442	252	452	1111 1111	1111 1111	uuuu uuuu
OSCCON	242	442	252	452	0	0	u
LVDCON	242	442	252	452	00 0101	00 0101	uu uuuu
WDTCON	242	442	252	452	0	0	u
RCON ^(4, 6)	242	442	252	452	00-1 11q0	00-1 qquu	uu-u qquu
TMR1H	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	242	442	252	452	0-00 0000	u-uu uuuu	u-uu uuuu
TMR2	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
PR2	242	442	252	452	1111 1111	1111 1111	1111 1111
T2CON	242	442	252	452	-000 0000	-000 0000	-uuu uuuu
SSPBUF	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
SSPCON1	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
SSPCON2	242	442	252	452	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', <math>q = value depends on condition

- Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 4: See Table 3-2 for RESET value for specific condition.
 - **5:** Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
 - **6:** The long write enable is only reset on a POR or MCLR Reset.
 - 7: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read as '0'.

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices			ces	Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
ADRESH	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
ADCON1	242	442	252	452	0- 0000	0- 0000	u- uuuu
CCPR1H	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	242	442	252	452	00 0000	00 0000	uu uuuu
CCPR2H	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	242	442	252	452	00 0000	00 0000	uu uuuu
TMR3H	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
T3CON	242	442	252	452	0000 0000	uuuu uuuu	uuuu uuuu
SPBRG	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCREG	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXREG	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA	242	442	252	452	0000 -01x	0000 -01u	uuuu -uuu
RCSTA	242	442	252	452	0000 000x	0000 000u	uuuu uuuu
IPR2	242	442	252	452	1111	1111	uuuu
PIR2	242	442	252	452	0000	0000	uuuu(1)
PIE2	242	442	252	452	0000	0000	uuuu
IPR1	242	442	252	452	1111 1111	1111 1111	uuuu uuuu
	242	442	252	452	-111 1111	-111 1111	-uuu uuuu
PIR1	242	442	252	452	0000 0000	0000 0000	uuuu uuuu(1)
	242	442	252	452	-000 0000	-000 0000	-uuu uuuu (1)
PIE1	242	442	252	452	0000 0000	0000 0000	uuuu uuuu
	242	442	252	452	-000 0000	-000 0000	-uuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', <math>q = value depends on condition

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

- 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
- 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
- 4: See Table 3-2 for RESET value for specific condition.
- 5: Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
- **6:** The long write enable is only reset on a POR or MCLR Reset.
- 7: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read as '0'.

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices			ces	Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TRISE	242	442	252	452	0000 -111	0000 -111	uuuu -uuu
TRISD	242	442	252	452	1111 1111	1111 1111	uuuu uuuu
TRISC	242	442	252	452	1111 1111	1111 1111	uuuu uuuu
TRISB	242	442	252	452	1111 1111	1111 1111	uuuu uuuu
TRISA ^(5, 7)	242	442	252	452	-111 1111 (5)	-111 1111 (5)	-uuu uuuu ⁽⁵⁾
LATE	242	442	252	452	xxx	uuu	uuu
LATD	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATC	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATB	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATA ^(5, 7)	242	442	252	452	-xxx xxxx (5)	-uuu uuuu (5)	-uuu uuuu ⁽⁵⁾
PORTE	242	442	252	452	000	000	uuu
PORTD	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	242	442	252	452	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA ^(5, 7)	242	442	252	452	-x0x 0000 (5)	-u0u 0000 (5)	-uuu uuuu ⁽⁵⁾

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

- Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - **3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 4: See Table 3-2 for RESET value for specific condition.
 - 5: Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
 - **6:** The long write enable is only reset on a POR or MCLR Reset.
 - 7: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read as '0'.

FIGURE 3-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD)

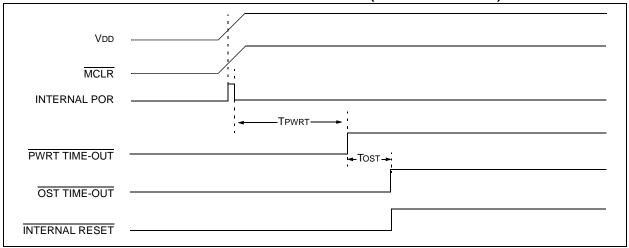


FIGURE 3-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

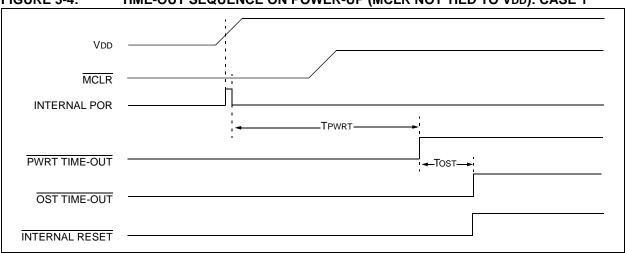
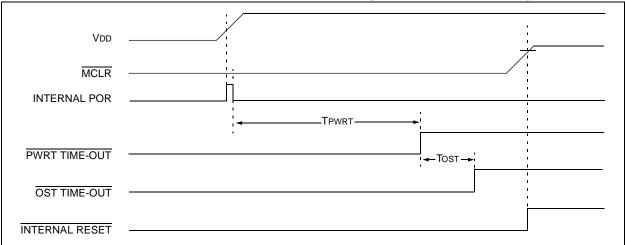
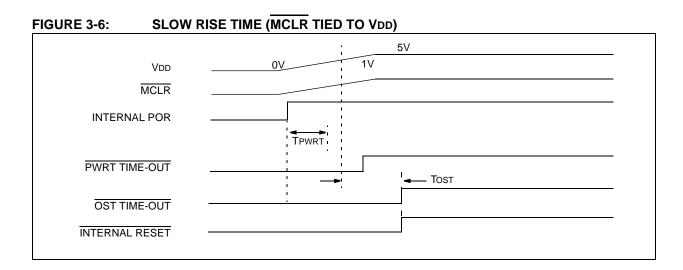
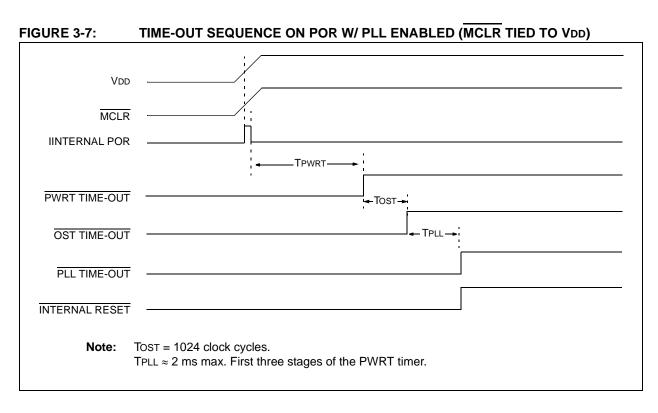


FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2







NOTES:

4.0 MEMORY ORGANIZATION

There are two memory blocks in Enhanced MCU devices. These memory blocks are:

- · Program Memory
- · Data Memory

Program and data memory use separate buses so that concurrent access can occur.

4.1 Program Memory Organization

A 21-bit program counter is capable of addressing the 2-Mbyte program memory space. Accessing a location between the physically implemented memory and the 2-Mbyte address will cause a read of all '0's (a NOP instruction).

PIC18C252 and PIC18C452 have 32 Kbytes of EPROM, while PIC18C242 and PIC18C442 have 16 Kbytes of EPROM. This means that PIC18CX52 devices can store up to 16K of single word instructions, and PIC18CX42 devices can store up to 8K of single word instructions.

The RESET vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

Figure 4-1 shows the Program Memory Map for PIC18C242/442 devices and Figure 4-2 shows the Program Memory Map for PIC18C252/452 devices.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR PIC18C442/242

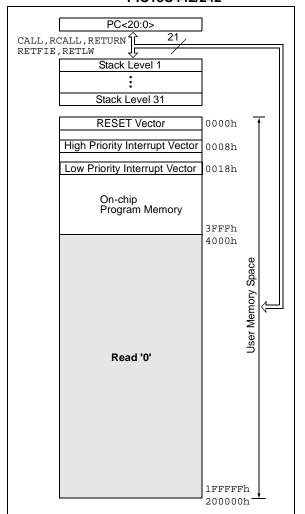
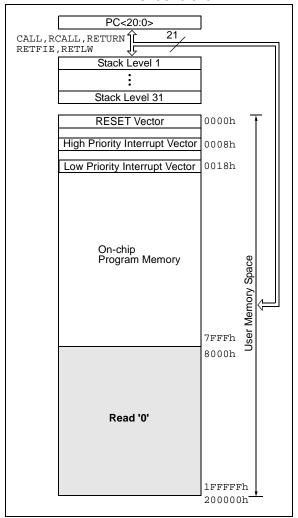


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR PIC18C452/252



4.2 Return Address Stack

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC (Program Counter) is pushed onto the stack when a CALL or RCALL instruction is executed, or an interrupt is acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the call or return instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit stack pointer, with the stack pointer initialized to 00000b after all RESETS. There is no RAM associated with stack pointer 00000b. This is only a RESET value. During a CALL type instruction causing a push onto the stack, the stack pointer is first incremented and the RAM location pointed to by the stack pointer is written with the contents of the PC. During a RETURN type instruction causing a pop from the stack, the contents of the RAM location pointed to by the STKPTR is transferred to the PC and then the stack pointer is decremented.

The stack space is not part of either program or data space. The stack pointer is readable and writable, and the address on the top of the stack is readable and writable through SFR registers. Data can also be pushed to, or popped from, the stack, using the top-of-stack SFRs. Status bits indicate if the stack pointer is at, or beyond the 31 levels provided.

4.2.1 TOP-OF-STACK ACCESS

The top of the stack is readable and writable. Three register locations, TOSU, TOSH and TOSL hold the contents of the stack location pointed to by the STKPTR register. This allows users to implement a software stack, if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU, TOSH and TOSL registers. These values can be placed on a user defined software stack. At return time, the software can replace the TOSU, TOSH and TOSL and do a return.

The user must disable the global interrupt enable bits during this time to prevent inadvertent stack operations.

4.2.2 RETURN STACK POINTER (STKPTR)

The STKPTR register contains the stack pointer value, the STKFUL (stack full) status bit, and the STKUNF (stack underflow) status bits. Register 4-1 shows the STKPTR register. The value of the stack pointer can be 0 through 31. The stack pointer increments when values are pushed onto the stack and decrements when values are popped off the stack. At RESET, the stack pointer value will be 0. The user may read and write the stack pointer value. This feature can be used by a Real Time Operating System for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit can only be cleared in software or by a POR.

The action that takes place when the stack becomes full, depends on the state of the STVREN (Stack Overflow Reset Enable) configuration bit. Refer to Section 18.0 for a description of the device configuration bits. If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit, and reset the device. The STKFUL bit will remain set and the stack pointer will be set to 0.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the stack pointer will increment to 31. Any additional pushes will not overwrite the 31st push and STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and sets the STKUNF bit, while the stack pointer remains at 0. The STKUNF bit will remain set until cleared in software or a POR occurs.

Note:

Returning a value of zero to the PC on an underflow, has the effect of vectoring the program to the RESET vector, where the stack conditions can be verified and appropriate actions can be taken.

REGISTER 4-1: STKPTR REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL	STKUNF	_	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

bit 7⁽¹⁾ STKFUL: Stack Full Flag bit

1 = Stack became full or overflowed

0 = Stack has not become full or overflowed

bit 6(1) STKUNF: Stack Underflow Flag bit

1 = Stack underflow occurred

0 = Stack underflow did not occur

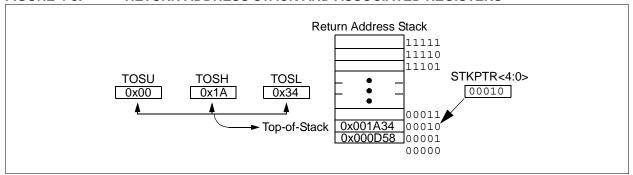
bit 5 **Unimplemented**: Read as '0'

bit 4-0 SP4:SP0: Stack Pointer Location bits

Note 1: Bit 7 and bit 6 can only be cleared in user software or by a POR.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 4-3: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



4.2.3 PUSH AND POP INSTRUCTIONS

Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off the stack, without disturbing normal program execution, is a desirable option. To push the current PC value onto the stack, a PUSH instruction can be executed. This will increment the stack pointer and load the current PC value onto the stack. TOSU, TOSH and TOSL can then be modified to place a return address on the stack.

The ability to pull the TOS value off of the stack and replace it with the value that was previously pushed onto the stack, without disturbing normal execution, is achieved by using the POP instruction. The POP instruction discards the current TOS by decrementing the stack pointer. The previous value pushed onto the stack then becomes the TOS value.

4.2.4 STACK FULL/UNDERFLOW RESETS

These resets are enabled by programming the STVREN configuration bit. When the STVREN bit is disabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit, but not cause a device RESET. When the STVREN bit is enabled, a full or underflow will set the appropriate STKFUL or STKUNF bit and then cause a device RESET. The STKFUL or STKUNF bits are only cleared by the user software or a POR Reset.

4.3 Fast Register Stack

A "fast interrupt return" option is available for interrupts. A Fast Register Stack is provided for the STATUS, WREG and BSR registers and are only one in depth. The stack is not readable or writable and is loaded with the current value of the corresponding register when the processor vectors for an interrupt. The values in the registers are then loaded back into the working registers, if the FAST RETURN instruction is used to return from the interrupt.

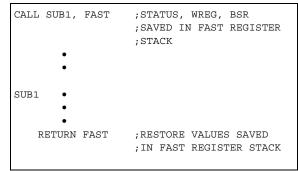
A low or high priority interrupt source will push values into the stack registers. If both low and high priority interrupts are enabled, the stack registers cannot be used reliably for low priority interrupts. If a high priority interrupt occurs while servicing a low priority interrupt, the stack register values stored by the low priority interrupt will be overwritten.

If high priority interrupts are not disabled during low priority interrupts, users must save the key registers in software during a low priority interrupt.

If no interrupts are used, the fast register stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the fast register stack for a subroutine call, a FAST CALL instruction must be executed.

Example 4-1 shows a source code example that uses the fast register stack.

EXAMPLE 4-1: FAST REGISTER STACK CODE EXAMPLE



4.4 PCL, PCLATH and PCLATU

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21-bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<15:8> bits and is not directly readable or writable. Updates to the PCH register may be performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits and is not directly readable or writable. Updates to the PCU register may be performed through the PCLATU register.

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the LSB of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

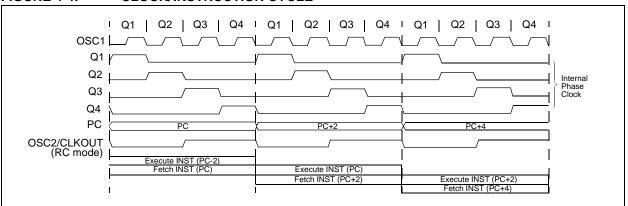
The CALL, RCALL, GOTO and program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

The contents of PCLATH and PCLATU will be transferred to the program counter by an operation that writes PCL. Similarly, the upper two bytes of the program counter will be transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see Section 4.8.1).

4.5 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 4-4.





4.6 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO), then two cycles are required to complete the instruction (Example 4-2).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

EXAMPLE 4-2: INSTRUCTION PIPELINE FLOW

	Tcy0	Tc _Y 1	Tcy2	Tc _Y 3	Tcy4	Tcy5
1. MOVLW 55h	Fetch 1	Execute 1			•	
2. MOVWF PORTB		Fetch 2	Execute 2			
3. BRA SUB_1	•		Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (F	orced NOP)			Fetch 4	Flush (NOP)	
5. Instruction @ addres	s SUB_1				Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

4.7 Instructions in Program Memory

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSB ='0'). Figure 4-5 shows an example of how instruction words are stored in the program memory. To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSB will always read '0' (see Section 4.4).

The CALL and GOTO instructions have an absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 4-5 shows how the instruction "GOTO 000006h" is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single word instructions that the PC will be offset by. Section 19.0 provides further details of the instruction set.

FIGURE 4-5: INSTRUCTIONS IN PROGRAM MEMORY

			LSB = 1	LSB = 0	Word Address ↓
	Program M	,			000000h
	Byte Locat	ions $ ightarrow$			000002h
					000004h
					000006h
Instruction 1:	MOVLW	055h	0Fh	55h	000008h
Instruction 2:	GOTO	000006h	EFh	03h	00000Ah
			F0h	00h	00000Ch
Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
			F4h	56h	000010h
					000012h
					000014h

4.7.1 TWO-WORD INSTRUCTIONS

The PIC18CXX2 devices have four two-word instructions: MOVFF, CALL, GOTO and LFSR. The second word of these instructions has the 4 MSBs set to 1's and is a special kind of NOP instruction. The lower 12-bits of the second word contain data to be used by the instruction. If the first word of the instruction is executed, the data in the second word is accessed. If the

second word of the instruction is executed by itself (first word was skipped), it will execute as a NOP. This action is necessary when the two-word instruction is preceded by a conditional instruction that changes the PC. A program example that demonstrates this concept is shown in Example 4-3. Refer to Section 19.0 for further details of the instruction set.

EXAMPLE 4-3: TWO-WORD INSTRUCTIONS

CASE 1:							
Object Code	Source Code						
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?				
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, execute 2-word instruction				
1111 0100 0101 0110			; 2nd operand holds address of REG2				
0010 0100 0000 0000	ADDWF	REG3	; continue code				
CASE 2:							
Object Code	Source Cod	е					
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?				
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes				
1111 0100 0101 0110			; 2nd operand becomes NOP				
0010 0100 0000 0000	ADDWF	REG3	; continue code				

4.8 Lookup Tables

Lookup tables are implemented two ways. These are:

- Computed GOTO
- · Table Reads

4.8.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL).

A lookup table can be formed with an ADDWF PCL instruction and a group of RETLW 0xnn instructions. WREG is loaded with an offset into the table, before executing a call to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW 0xnn instructions that returns the value 0xnn to the calling function.

The offset value (value in WREG) specifies the number of bytes that the program counter should advance.

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

4.8.2 TABLE READS/TABLE WRITES

A better method of storing data in program memory allows 2 bytes of data to be stored in each instruction location.

Lookup table data may be stored 2 bytes per program word by using table reads and writes. The table pointer (TBLPTR) specifies the byte address and the table latch (TABLAT) contains the data that is read from, or written to program memory. Data is transferred to/from program memory one byte at a time.

A description of the Table Read/Table Write operation is shown in Section 5.0.

4.9 Data Memory Organization

The data memory is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4096 bytes of data memory. Figure 4-6 and Figure 4-7 show the data memory organization for the PIC18CXX2 devices.

The data memory map is divided into as many as 16 banks that contain 256 bytes each. The lower 4 bits of the Bank Select Register (BSR<3:0>) select which bank will be accessed. The upper 4 bits for the BSR are not implemented.

The data memory contains Special Function Registers (SFR) and General Purpose Registers (GPR). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratch pad operations in the user's application. The SFRs start at the last location of Bank 15 (0xFFF) and extend downwards. Any remaining space beyond the SFRs in the Bank may be implemented as GPRs. GPRs start at the first location of Bank 0 and grow upwards. Any read of an unimplemented location will read as '0's.

The entire data memory may be accessed directly, or indirectly. Direct addressing may require the use of the BSR register. Indirect addressing requires the use of a File Select Register (FSRn) and corresponding Indirect File Operand (INDFn). Each FSR holds a 12-bit address value that can be used to access any location in the Data Memory map without banking.

The instruction set and architecture allow operations across all banks. This may be accomplished by indirect addressing or by the use of the MOVFF instruction. The MOVFF instruction is a two-word/two-cycle instruction that moves a value from one register to another.

To ensure that commonly used registers (SFRs and select GPRs) can be accessed in a single cycle, regardless of the current BSR values, an Access Bank is implemented. A segment of Bank 0 and a segment of Bank 15 comprise the Access RAM. Section 4.10 provides a detailed description of the Access RAM.

4.9.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly. Indirect addressing operates using the File Select Registers (FSRn) and corresponding Indirect File Operand (INDFn). The operation of indirect addressing is shown in Section 4.12.

Enhanced MCU devices may have banked memory in the GPR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other RESETS.

Data RAM is available for use as GPR registers by all instructions. The top half of bank 15 (0xF80 to 0xFFF) contains SFRs. All other banks of data memory contain GPR registers, starting with bank 0.

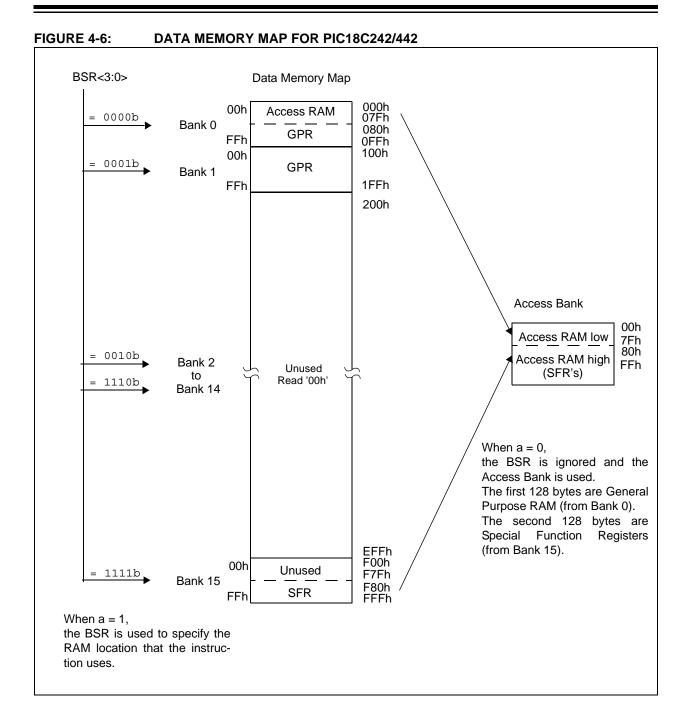
4.9.2 SPECIAL FUNCTION REGISTERS

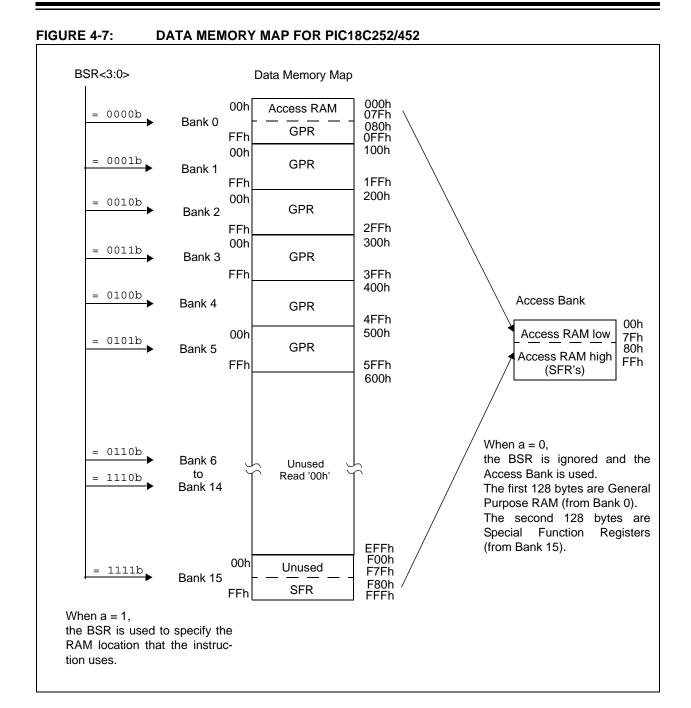
The Special Function Registers (SFRs) are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 4-1 and Table 4-2.

The SFRs can be classified into two sets; those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described in this section, while those related to the operation of the peripheral features are described in the section of that peripheral feature.

The SFRs are typically distributed among the peripherals whose functions they control.

The unused SFR locations will be unimplemented and read as '0's. See Table 4-1 for addresses for the SFRs.





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TABLE 4-1: SPECIAL FUNCTION REGISTER MAP

FFFh	TOSU	FDFh	INDF2 ⁽³⁾	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2 ⁽³⁾	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2 ⁽³⁾	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2 ⁽³⁾	FBCh	CCPR2H	F9Ch	_
FFBh	PCLATU	FDBh	PLUSW2 ⁽³⁾	FBBh	CCPR2L	F9Bh	_
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	_
FF9h	PCL	FD9h	FSR2L	FB9h	_	F99h	_
FF8h	TBLPTRU	FD8h	STATUS	FB8h	_	F98h	
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	_	F97h	
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	_	F96h	TRISE ⁽²⁾
FF5h	TABLAT	FD5h	T0CON	FB5h	_	F95h	TRISD ⁽²⁾
FF4h	PRODH	FD4h	_	FB4h	_	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	
FF0h	INTCON3	FD0h	RCON	FB0h	_	F90h	
FEFh	INDF0 ⁽³⁾	FCFh	TMR1H	FAFh	SPBRG	F8Fh	
FEEh	POSTINC0 ⁽³⁾	FCEh	TMR1L	FAEh	RCREG	F8Eh	
FEDh	POSTDEC0 ⁽³⁾	FCDh	T1CON	FADh	TXREG	F8Dh	LATE ⁽²⁾
FECh	PREINCO ⁽³⁾	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD ⁽²⁾
FEBh	PLUSW0 ⁽³⁾	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	_	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	_	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	_	F88h	_
FE7h	INDF1 ⁽³⁾	FC7h	SSPSTAT	FA7h	_	F87h	_
FE6h	POSTINC1 ⁽³⁾	FC6h	SSPCON1	FA6h	_	F86h	
FE5h	POSTDEC1 ⁽³⁾	FC5h	SSPCON2	FA5h	_	F85h	_
FE4h	PREINC1 ⁽³⁾	FC4h	ADRESH	FA4h	_	F84h	PORTE ⁽²⁾
FE3h	PLUSW1 ⁽³⁾	FC3h	ADRESL	FA3h	_	F83h	PORTD ⁽²⁾
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	_	FA0h	PIE2	F80h	PORTA

Note 1: Unimplemented registers are read as '0'.

2: This register is not available on PIC18C2X2 devices.

3: This is not a physical register.

TABLE 4-2: REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TOSU	_	_		Top-of-Stack	Upper Byte (T	OS<20:16>)			0 0000	37
TOSH	Top-of-Stac	k High Byte (To	OS<15:8>)						0000 0000	37
TOSL	Top-of-Stac	k Low Byte (TO	OS<7:0>)						0000 0000	37
STKPTR	STKFUL	STKUNF	_	Return Stack	Pointer				00-0 0000	38
PCLATU	_	_	_	Holding Regi	ister for PC<20):16>			0 0000	39
PCLATH	Holding Reg	gister for PC<1	5:8>						0000 0000	39
PCL	PC Low Byt	te (PC<7:0>)							0000 0000	39
TBLPTRU	_	_	bit21 ⁽²⁾	Program Mei	mory Table Po	inter Upper By	te (TBLPTR<	20:16>)	0 0000	57
TBLPTRH	Program Me	emory Table Po	ointer High By	te (TBLPTR<1	5:8>)				0000 0000	57
TBLPTRL	Program Me	emory Table Po		0000 0000	57					
TABLAT	Program Me	emory Table La	atch						0000 0000	57
PRODH	Product Re	gister High Byt	е						xxxx xxxx	61
PRODL	Product Re	gister Low Byte	9						xxxx xxxx	61
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	65
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP	1111 -1-1	66
INTCON3	INT2IP	INT1IP	_	INT2IE	INT1IE	_	INT2IF	INT1IF	11-0 0-00	67
INDF0	Uses conte	nts of FSR0 to	address data	memory - valu	e of FSR0 not	changed (not	a physical reg	gister)	N/A	50
POSTINC0	Uses conte	nts of FSR0 to	al register)	N/A	50					
POSTDEC0	Uses conte	nts of FSR0 to	cal register)	N/A	50					
PREINC0	Uses conte	Il register)	N/A	50						
PLUSW0	Uses contents of FSR0 to address data memory - value of FSR0 pre-incremented (not a physical register) value of FSR0 offset by value in WREG								N/A	50
FSR0H	— — Indirect Data Memory Address Pointer 0 High Byte									50
FSR0L	Indirect Data Memory Address Pointer 0 Low Byte									50
WREG	Working Register									
INDF1			address data	memory - valu	e of FSR1 not	changed (not	a physical red	gister)	N/A	50
POSTINC1				memory - valu					N/A	50
POSTDEC1				memory - valu					N/A	50
PREINC1				memory - valu					N/A	50
PLUSW1	Uses conte		address data	memory - valu					N/A	50
FSR1H	_	_	_	_	Indirect Data	Memory Add	ress Pointer 1	High Byte	0000	50
FSR1L	Indirect Dat	a Memory Add	ress Pointer 1	Low Byte	1			<u> </u>	xxxx xxxx	50
BSR	_	_	_		Bank Select	Register			0000	49
INDF2	Uses conte	nts of FSR2 to	address data	memory - valu			a physical red	gister)	N/A	50
POSTINC2				memory - valu		• ,	. ,		N/A	50
POSTDEC2				memory - valu					N/A	50
PREINC2				memory - valu					N/A	50
PLUSW2	Uses conte		address data	memory - valu				· ,	N/A	50
FSR2H	_	_	_	_	Indirect Data	Memory Add	ress Pointer 2	2 High Byte	0000	50
FSR2L	Indirect Data Memory Address Pointer 2 Low Byte									50
STATUS	N OV Z DC C									52
TMR0H	Timer0 Reg	ister High Byte)						0000 0000	95
TMR0L	Timer0 Reg	ister Low Byte							xxxx xxxx	95
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111	93
OSCCON	_	_	ı	_	_	_	_	SCS	0	20
LVDCON	_	_	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0	00 0101	175

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only, and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

TABLE 4-2: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
WDTCON	_	_	_	_	_	_	_	SWDTE	0	183
RCON	IPEN	LWRT	_	RI	TO	PD	POR	BOR	0q-1 11qq	53, 56, 74
TMR1H	Timer1 Reg	ister High Byte)						xxxx xxxx	97
TMR1L	Timer1 Reg	ister Low Byte							xxxx xxxx	97
T1CON	RD16	_	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	0-00 0000	97
TMR2	Timer2 Reg	ister							0000 0000	101
PR2	Timer2 Peri	od Register							1111 1111	102
T2CON	- TOUTPS3 TOUTPS2 TOUTPS1 TOUTPS0 TMR2ON T2CKPS1 T2CKPS0						-000 0000	101		
SSPBUF	SSP Receiv	SSP Receive Buffer/Transmit Register								121
SSPADD	SSP Addres	ss Register in I	² C Slave Mod	le. SSP Baud F	Rate Reload R	egister in I ² C l	Master Mode.		0000 0000	128
SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	116
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	118
SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	120
ADRESH	A/D Result		xxxx xxxx	171,172						
ADRESL	A/D Result		xxxx xxxx	171,172						
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	165
ADCON1	ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	166
CCPR1H	Capture/Co	mpare/PWM R	Register1 High	Byte					xxxx xxxx	111, 113
CCPR1L	Capture/Co	mpare/PWM R	Register1 Low	Byte					xxxx xxxx	111, 113
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	107
CCPR2H	Capture/Co	mpare/PWM R	Register2 High	Byte					xxxx xxxx	111, 113
CCPR2L	Capture/Co	mpare/PWM R	Register2 Low	Byte					xxxx xxxx	111, 113
CCP2CON	_	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	107
TMR3H	Timer3 Reg	ister High Byte)						xxxx xxxx	103
TMR3L	Timer3 Reg	ister Low Byte							xxxx xxxx	103
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	103
SPBRG	USART1 Ba	aud Rate Gene	erator						0000 0000	151
RCREG	USART1 Re	eceive Registe	r						0000 0000	158, 161, 163
TXREG	USART1 Tr	ansmit Registe	er					_	0000 0000	156, 159, 162
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	149
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	150

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only, and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

PIC18CXX2

REGISTER FILE SUMMARY (CONTINUED) TABLE 4-2:

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
IPR2	_	_	_	_	BCLIP	LVDIP	TMR3IP	CCP2IP	1111	73
PIR2	_	_	_	_	BCLIF	LVDIF	TMR3IF	CCP2IF	0000	69
PIE2	_	ı	ı	_	BCLIE	LVDIE	TMR3IE	CCP2IE	0000	71
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	1111 1111	72
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	CCP1IF TMR2IF TMR1IF			68
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	70
TRISE	IBF	OBF	IBOV	PSPMODE	_	Data Direction	on bits for PO	RTE	0000 -111	88
TRISD	Data Directi	on Control Re		1111 1111	85					
TRISC	Data Directi		1111 1111	83						
TRISB	Data Direction Control Register for PORTB									80
TRISA	_	TRISA6 ⁽¹⁾	Data Direction	on Control Reg	ister for PORT	TA .			-111 1111	77
LATE	_	_	_	_	_		E Data Latch, E Data Latch		xxx	87
LATD	Read PORT	D Data Latch,	Write PORTE	Data Latch					xxxx xxxx	85
LATC	Read PORT	C Data Latch,	Write PORTO	Data Latch					xxxx xxxx	83
LATB	Read PORT	TB Data Latch,	Write PORTE	B Data Latch					xxxx xxxx	80
LATA	_	LATA6 ⁽¹⁾	Read PORT	A Data Latch, \	Write PORTA	Data Latch ⁽¹⁾			-xxx xxxx	77
PORTE	Read PORT	E pins, Write	PORTE Data I	Latch					000	87
PORTD	Read PORT	TD pins, Write	PORTD Data	Latch					xxxx xxxx	85
PORTC	Read PORT	C pins, Write	PORTC Data	Latch					xxxx xxxx	83
PORTB	Read PORT	B pins, Write	PORTB Data I	Latch					xxxx xxxx	80
PORTA	_	RA6 ⁽¹⁾	Read PORT	A pins, Write P	ORTA Data La	atch ⁽¹⁾		•	-x0x 0000	77

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only, and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

4.10 Access Bank

The Access Bank is an architectural enhancement, which is very useful for C compiler code optimization. The techniques used by the C compiler may also be useful for programs written in assembly.

This data memory region can be used for:

- · Intermediate computational values
- · Local variables of subroutines
- Faster context saving/switching of variables
- · Common variables
- Faster evaluation/control of SFRs (no banking)

The Access Bank is comprised of the upper 128 bytes in Bank 15 (SFRs) and the lower 128 bytes in Bank 0. These two sections will be referred to as Access RAM High and Access RAM Low, respectively. Figure 4-6 and Figure 4-7 indicate the Access RAM areas.

A bit in the instruction word specifies if the operation is to occur in the bank specified by the BSR register or in the Access Bank. This bit is denoted by the 'a' bit (for access bit).

When forced in the Access Bank (a = '0'), the last address in Access RAM Low is followed by the first address in Access RAM High. Access RAM High maps the Special Function registers, so that these registers

can be accessed without any software overhead. This is useful for testing status flags and modifying control hits

4.11 Bank Select Register (BSR)

The need for a large general purpose memory space dictates a RAM banking scheme. The data memory is partitioned into sixteen banks. When using direct addressing, the BSR should be configured for the desired bank.

BSR<3:0> holds the upper 4 bits of the 12-bit RAM address. The BSR<7:4> bits will always read '0's, and writes will have no effect.

A MOVLB instruction has been provided in the instruction set to assist in selecting banks.

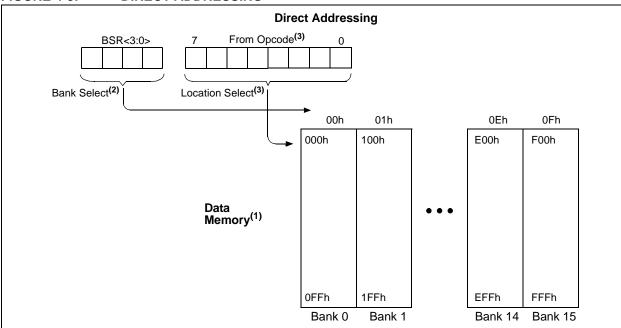
If the currently selected bank is not implemented, any read will return all '0's and all writes are ignored. The STATUS register bits will be set/cleared as appropriate for the instruction performed.

Each Bank extends up to FFh (256 bytes). All data memory is implemented as static RAM.

A MOVFF instruction ignores the BSR, since the 12-bit addresses are embedded into the instruction word.

Section 4.12 provides a description of indirect addressing, which allows linear addressing of the entire RAM space.

FIGURE 4-8: DIRECT ADDRESSING



- Note 1: For register file map detail, see Table 4-1.
 - 2: The access bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.
 - 3: The MOVFF instruction embeds the entire 12-bit address in the instruction.

4.12 Indirect Addressing, INDF and FSR Registers

Indirect addressing is a mode of addressing data memory, where the data memory address in the instruction is not fixed. An FSR register is used as a pointer to the data memory location that is to be read or written. Since this pointer is in RAM, the contents can be modified by the program. This can be useful for data tables in the data memory and for software stacks. Figure 4-9 shows the operation of indirect addressing. This shows the moving of the value to the data memory address, specified by the value of the FSR register.

Indirect addressing is possible by using one of the INDF registers. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself, indirectly (FSR = '0'), will read 00h. Writing to the INDF register indirectly, results in a no operation. The FSR register contains a 12-bit address, which is shown in Figure 4-10.

The INDFn register is not a physical register. Addressing INDFn actually addresses the register whose address is contained in the FSRn register (FSRn is a pointer). This is indirect addressing.

Example 4-4 shows a simple use of indirect addressing to clear the RAM in Bank1 (locations 100h-1FFh) in a minimum number of instructions.

EXAMPLE 4-4: HOW TO CLEAR RAM (BANK1) USING INDIRECT ADDRESSING

```
LFSR FSR0, 0x100 ;

NEXT CLRF POSTINC0 ; Clear INDF register ; & inc pointer

BTFSS FSR0H, 1 ; All done w/ Bank1? GOTO NEXT ; NO, clear next

CONTINUE ; YES, continue
```

There are three indirect addressing registers. To address the entire data memory space (4096 bytes), these registers are 12-bit wide. To store the 12-bits of addressing information, two 8-bit registers are required. These indirect addressing registers are:

- 1. FSR0: composed of FSR0H:FSR0L
- 2. FSR1: composed of FSR1H:FSR1L
- 3. FSR2: composed of FSR2H:FSR2L

In addition, there are registers INDF0, INDF1 and INDF2, which are not physically implemented. Reading or writing to these registers activates indirect addressing, with the value in the corresponding FSR register being the address of the data.

If an instruction writes a value to INDF0, the value will be written to the address pointed to by FSR0H:FSR0L. A read from INDF1 reads the data from the address pointed to by FSR1H:FSR1L. INDFn can be used in code anywhere an operand can be used.

If INDF0, INDF1 or INDF2 are read indirectly via an FSR, all '0's are read (zero bit is set). Similarly, if INDF0, INDF1 or INDF2 are written to indirectly, the operation will be equivalent to a NOP instruction and the STATUS bits are not affected.

4.12.1 INDIRECT ADDRESSING OPERATION

Each FSR register has an INDF register associated with it, plus four additional register addresses. Performing an operation on one of these five registers determines how the FSR will be modified during indirect addressing.

When data access is done to one of the five INDFn locations, the address selected will configure the FSRn register to:

- Do nothing to FSRn after an indirect access (no change) INDFn
- Auto-decrement FSRn after an indirect access (post-decrement) - POSTDECn
- Auto-increment FSRn after an indirect access (post-increment) - POSTINCn
- Auto-increment FSRn before an indirect access (pre-increment) - PREINCn
- Use the value in the WREG register as an offset to FSRn. Do not modify the value of the WREG or the FSRn register after an indirect access (no change) - PLUSWn

When using the auto-increment or auto-decrement features, the effect on the FSR is not reflected in the STATUS register. For example, if the indirect address causes the FSR to equal '0', the Z bit will not be set.

Incrementing or decrementing an FSR affects all 12 bits. That is, when FSRnL overflows from an increment, FSRnH will be incremented automatically.

Adding these features allows the FSRn to be used as a stack pointer, in addition to its uses for table operations in data memory.

Each FSR has an address associated with it that performs an indexed indirect access. When a data access to this INDFn location (PLUSWn) occurs, the FSRn is configured to add the signed value in the WREG register and the value in FSR to form the address before an indirect access. The FSR value is not changed.

If an FSR register contains a value that points to one of the INDFn, an indirect read will read 00h (zero bit is set), while an indirect write will be equivalent to a NOP (STATUS bits are not affected).

If an indirect addressing operation is done where the target address is an FSRnH or FSRnL register, the write operation will dominate over the pre- or post-increment/decrement functions.

FIGURE 4-9: INDIRECT ADDRESSING OPERATION

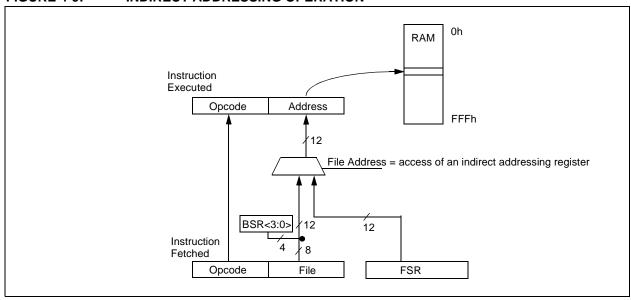
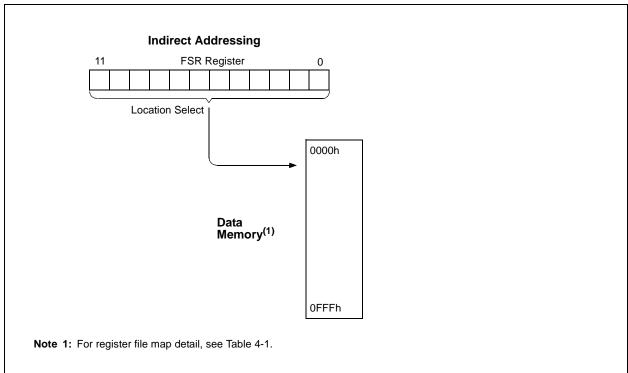


FIGURE 4-10: INDIRECT ADDRESSING



4.13 STATUS Register

The STATUS register, shown in Register 4-2, contains the arithmetic status of the ALU. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, then the write to these five bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF, MOVFF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits from the STATUS register. For other instructions not affecting any status bits, see Table 19-2.

Note: The C and DC bits operate as a borrow and digit borrow bit respectively, in subtraction.

REGISTER 4-2: STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	_	_	N	OV	Z	DC	С
bit 7							bit 0

bit 7-5 Unimplemented: Read as '0'

bit 4 N: Negative bit

This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative, (ALU MSB = 1).

- 1 = Result was negative
- 0 = Result was positive

bit 3 **OV:** Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.

- 1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
- 0 = No overflow occurred

bit 2 Z: Zero bit

- 1 = The result of an arithmetic or logic operation is zero
- 0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit carry/borrow bit

For ADDWF, ADDLW, SUBLW, and SUBWF instructions

- 1 = A carry-out from the 4th low order bit of the result occurred
- 0 = No carry-out from the 4th low order bit of the result

Note:

For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the bit 4 or bit 3 of the source register.

bit 0 C: Carry/borrow bit

For ADDWF, ADDLW, SUBLW, and SUBWF instructions

- 1 = A carry-out from the Most Significant bit of the result occurred
- 0 = No carry-out from the Most Significant bit of the result occurred

Note:

For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

Led	Δr	h	•
Leu	ш	ıu	

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

4.13.1 RCON REGISTER

The Reset Control (RCON) register contains flag bits that allow differentiation between the sources of a device RESET. These flags include the TO, PD, POR, BOR and RI bits. This register is readable and writable.

Note 1: If the BOREN configuration bit is set (Brown-out Reset enabled), the BOR bit is '1' on a Power-on Reset. After a Brown-out Reset has occurred, the BOR bit will be clear and must be set by firmware to indicate the occurrence of the next Brown-out Reset.

If the BOREN configuration bit is clear (Brown-out Reset disabled), BOR is unknown after Power-on Reset and Brown-out Reset conditions.

2: It is recommended that the POR bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.

REGISTER 4-3: RCON REGISTER

	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
Ī	IPEN	LWRT	_	RI	TO	PD	POR	BOR
	bit 7							bit 0

- bit 7 IPEN: Interrupt Priority Enable bit
 - 1 = Enable priority levels on interrupts
 - 0 = Disable priority levels on interrupts (16CXXX compatibility mode)
- bit 6 LWRT: Long Write Enable bit
 - 1 = Enable TBLWT to internal program memory Once this bit is set, it can only be cleared by a POR or MCLR Reset.
 - 0 = Disable TBLWT to internal program memory; TBLWT only to external program memory
- bit 5 Unimplemented: Read as '0'
- bit 4 RI: RESET Instruction Flag bit
 - 1 = The RESET instruction was not executed
 - 0 = The RESET instruction was executed causing a device RESET (must be set in software after a Brown-out Reset occurs)
- bit 3 TO: Watchdog Time-out Flag bit
 - 1 = After power-up, CLRWDT instruction, or SLEEP instruction
 - 0 = A WDT time-out occurred
- bit 2 PD: Power-down Detection Flag bit
 - 1 = After power-up or by the CLRWDT instruction
 - 0 = By execution of the SLEEP instruction
- bit 1 POR: Power-on Reset Status bit
 - 1 = A Power-on Reset has not occurred
 - 0 = A Power-on Reset occurred
 - (must be set in software after a Power-on Reset occurs)
- bit 0 BOR: Brown-out Reset Status bit
 - 1 = A Brown-out Reset has not occurred
 - 0 = A Brown-out Reset occurred

(must be set in software after a Brown-out Reset occurs)

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

PIC18CXX2

NOTES:

5.0 TABLE READS/TABLE WRITES

Enhanced devices have two memory spaces: the program memory space and the data memory space. The program memory space is 16-bits wide, while the data memory space is 8 bits wide. Table Reads and Table Writes have been provided to move data between these two memory spaces through an 8-bit register (TABLAT).

The operations that allow the processor to move data between the data and program memory spaces are:

- Table Read (TBLRD)
- Table Write (TBLWT)

Table Read operations retrieve data from program memory and place it into the data memory space. Figure 5-1 shows the operation of a Table Read with program and data memory.

Table Write operations store data from the data memory space into program memory. Figure 5-2 shows the operation of a Table Write with program and data memory.

Table operations work with byte entities. A table block containing data is not required to be word aligned, so a table block can start and end at any byte address. If a Table Write is being used to write an executable program to program memory, program instructions will need to be word aligned.

FIGURE 5-1: TABLE READ OPERATION

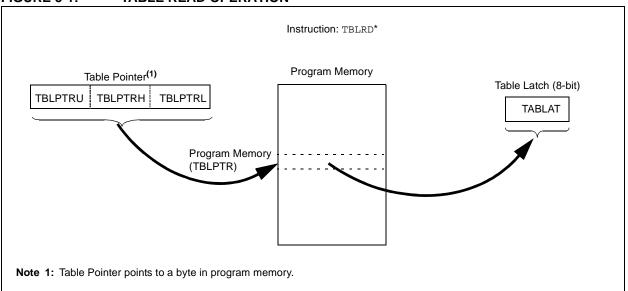
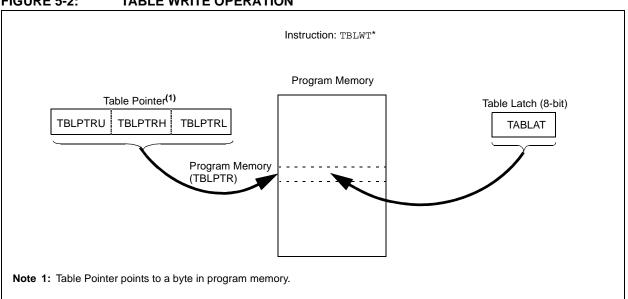


FIGURE 5-2: TABLE WRITE OPERATION



5.1 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- TBLPTR registers
- · TABLAT register
- · RCON register

5.1.1 RCON REGISTER

The LWRT bit specifies the operation of Table Writes to internal memory when the VPP voltage is applied to the MCLR pin. When the LWRT bit is set, the controller continues to execute user code, but long Table Writes are allowed (for programming internal program memory) from user mode. The LWRT bit can be cleared only by performing either a POR or MCLR Reset.

REGISTER 5-1: RCON REGISTER (ADDRESS: FD0h)

R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
IPEN	LWRT	_	RI	TO	PD	POR	BOR
bit 7							bit 0

- - 1 = Enable priority levels on interrupts
 - 0 = Disable priority levels on interrupts (16CXXX compatibility mode)
- bit 6 LWRT: Long Write Enable bit
 - 1 = Enable TBLWT to internal program memory
 - 0 = Disable TBLWT to internal program memory.

Note: Only cleared on a POR or MCLR Reset.

This bit has no effect on TBLWTs to external program memory.

- bit 5 **Unimplemented**: Read as '0'
- bit 4 RI: RESET Instruction Flag bit
 - 1 = No RESET instruction occurred
 - 0 = A RESET instruction occurred
- bit 3 **TO:** Time-out bit
 - 1 = After power-up, CLRWDT instruction, or SLEEP instruction
 - 0 = A WDT time-out occurred
- bit 2 **PD**: Power-down bit
 - 1 = After power-up or by the CLRWDT instruction
 - 0 = By execution of the SLEEP instruction
- bit 1 POR: Power-on Reset Status bit
 - 1 = No Power-on Reset occurred
 - 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
- bit 0 BOR: Brown-out Reset Status bit
 - 1 = No Brown-out Reset or POR Reset occurred
 - 0 = A Brown-out Reset or POR Reset occurred

(must be set in software after a Brown-out Reset occurs)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n - Value at POR reset	'1' - Rit is set	'0' - Bit is cleared	y – Rit is unknown

5.1.2 TABLAT - TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch is used to hold 8-bit data during data transfers between program memory and data memory.

5.1.3 TBLPTR - TABLE POINTER REGISTER

The Table Pointer (TBLPTR) addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers (Table Pointer Upper Byte, High Byte and Low Byte). These three registers (TBLPTRU:TBLPTRH:TBLPTRL) join to form a 22-bit wide pointer. The lower 21-bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the User ID and the Configuration bits.

The Table Pointer, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways, based on the table operation. These operations are shown in Table 5-1. These operations on the TBLPTR only affect the lower 21-bits.

TABLE 5-1: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS

Example	Operation on Table Pointer
TBLRD* TBLWT*	TBLPTR is not modified
TBLRD*+ TBLWT*+	TBLPTR is incremented after the read/write
TBLRD*- TBLWT*-	TBLPTR is decremented after the read/write
TBLRD+* TBLWT+*	TBLPTR is incremented before the read/write

5.2 Internal Program Memory Read/ Writes

5.2.1 TABLE READ OVERVIEW (TBLRD)

The ${\tt TBLRD}$ instructions are used to read data from program memory to data memory.

TBLPTR points to a byte address in program space. Executing TBLRD places the byte pointed to into TAB-LAT. In addition, TBLPTR can be modified automatically for the next Table Read operation.

Table Reads from program memory are performed one byte at a time. The instruction will load TABLAT with the one byte from program memory pointed to by TBLPTR.

5.2.2 INTERNAL PROGRAM MEMORY WRITE BLOCK SIZE

The internal program memory of PIC18CXXX devices is written in blocks. For PIC18CXX2 devices, the write block size is 2 bytes. Consequently, Table Write operations to internal program memory are performed in pairs, one byte at a time.

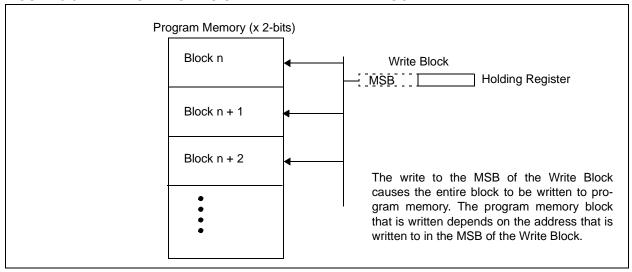
When a Table Write occurs to an even program memory address (TBLPTR<0>=0), the contents of TABLAT are transferred to an internal holding register. This is performed as a short write and the program memory block is not actually programmed at this time. The holding register is not accessible by the user.

When a Table Write occurs to an odd program memory address (TBLPTR<0>=1), a long write is started. During the long write, the contents of TABLAT are written to the high byte of the program memory block and the contents of the holding register are transferred to the low byte of the program memory block.

Figure 5-3 shows the holding register and the program memory write blocks.

If a single byte is to be programmed, the low (even) byte of the destination program word should be read using TBLRD*, modified or changed, if required, and written back to the same address using TBLWT*+. The high (odd) byte should be read using TBLRD*, modified or changed if required, and written back to the same address using TBLWT. A write to the odd address will cause a long write to begin. This process ensures that existing data in either byte will not be changed unless desired.





5.2.2.1 Operation

The long write is what actually programs words of data into the internal memory. When a TBLWT to the MSB of the write block occurs, instruction execution is halted. During this time, programming voltage and the data stored in internal latches is applied to program memory.

For a long write to occur:

- MCLR/VPP pin must be at the programming voltage
- 2. LWRT bit must be set
- TBLWT to the address of the MSB of the write block

If the LWRT bit is clear, a short write will occur and program memory will not be changed. If the TBLWT is not to the MSB of the write block, then the programming phase is not initiated.

Setting the LWRT bit enables long writes when the MCLR pin is taken to VPP voltage. Once the LWRT bit is set, it can be cleared only by performing a POR or MCLR Reset.

To ensure that the memory location has been well programmed, a minimum programming time is required. The long write can be terminated after the programming time has expired by a RESET or an interrupt. Having only one interrupt source enabled to terminate the long write ensures that no unintended interrupts will prematurely terminate the long write.

5.2.2.2 Sequence of Events

The sequence of events for programming an internal program memory location should be:

- Enable the interrupt that terminates the long write. Disable all other interrupts.
- 2. Clear the source interrupt flag.
- If Interrupt Service Routine execution is desired when the device wakes, enable global interrupts.
- 4. Set LWRT bit in the RCON register.
- 5. Raise MCLR/VPP pin to the programming voltage, VPP.
- 6. Clear the WDT (if enabled).
- Set the interrupt source to interrupt at the required time.
- 8. Execute the Table Write for the lower (even) byte. This will be a short write.
- 9. Execute the Table Write for the upper (odd) byte. This will be a long write. The microcontroller will then halt internal operations. (This is not the same as SLEEP mode, as the clocks and peripherals will continue to run.) The interrupt will cause the microcontroller to resume operation.
- 10. If GIE was set, service the interrupt request.
- 11. Lower MCLR/VPP pin to VDD.
- 12. Verify the memory location (Table Read).

5.2.3 INTERRUPTS

The long write must be terminated by a RESET or any interrupt.

The interrupt source must have its interrupt enable bit set. When the source sets its interrupt flag, programming will terminate. This will occur, regardless of the settings of interrupt priority bits, the GIE/GIEH bit, or the PIE/GIEL bit.

Depending on the states of interrupt priority bits, the GIE/GIEH bit or the PIE/GIEL bit, program execution can either be vectored to the high or low priority Interrupt Service Routine (ISR), or continue execution from where programming commenced.

In either case, the interrupt flag will not be cleared when programming is terminated and will need to be cleared by the software.

TABLE 5-2: LONG WRITE EXECUTION, INTERRUPT ENABLE BITS AND INTERRUPT RESULTS

GIE/ GIEH	PIE/ GIEL	Priority	Interrupt Enable	Interrupt Flag	Action
Х	Х	Х	0 (default)	Х	Long write continues even if interrupt flag becomes set.
Х	Х	Х	1	0	Long write continues, will resume operations when the interrupt flag is set.
0 (default)	0 (default)	Х	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
0 (default)	1	1 high priority (default)	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
1	0 (default)	0 low	1	1	Terminates long write, executes next instruction. Interrupt flag not cleared.
0 (default)	1	0 low	1	1	Terminates long write, branches to low priority interrupt vector. Interrupt flag can be cleared by ISR.
1	0 (default)	1 high priority (default)	1	1	Terminates long write, branches to high priority interrupt vector. Interrupt flag can be cleared by ISR.

5.2.4 UNEXPECTED TERMINATION OF WRITE OPERATIONS

If a write is terminated by an unplanned event such as loss of power, an unexpected RESET, or an interrupt that was not disabled, the memory location just programmed should be verified and reprogrammed if needed.

PIC18CXX2

NOTES:

6.0 8 X 8 HARDWARE MULTIPLIER

6.1 Introduction

An 8 x 8 hardware multiplier is included in the ALU of the PIC18CXX2 devices. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored into the 16-bit product register pair (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- · Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 6-1 shows a performance comparison between enhanced devices using the single cycle hardware multiply, and performing the same function without the hardware multiply.

TABLE 6-1: PERFORMANCE COMPARISON

		Program	Cycles	Time			
Routine	Multiply Method	Memory (Words)	(Max)	@ 40 MHz	@ 10 MHz	@ 4 MHz	
0 v 0 unaignad	Without hardware multiply	13	69	6.9 μs	27.6 μs	69 μs	
8 x 8 unsigned	Hardware multiply	1	1	100 ns	400 ns	1 μs	
0 v 0 signed	Without hardware multiply	33	91	9.1 μs	36.4 μs	91 μs	
8 x 8 signed	Hardware multiply	6	6	600 ns	2.4 μs	6 μs	
16 v 16 uppigned	Without hardware multiply	21	242	24.2 μs	96.8 μs	242 μs	
16 x 16 unsigned	Hardware multiply	24	24	2.4 μs	9.6 μs	24 μs	
16 x 16 signed	Without hardware multiply	52	254	25.4 μs	102.6 μs	254 μs	
To x To signed	Hardware multiply	36	36	3.6 μs	14.4 μs	36 μs	

6.2 Operation

Example 6-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 6-2 shows the sequence to do an 8×8 signed multiply. To account for the sign bits of the arguments, each argument's Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 6-1: 8 x 8 UNSIGNED MULTIPLY ROUTINE

```
MOVF ARG1, W ;
MULWF ARG2 ; ARG1 * ARG2 ->
; PRODH:PRODL
```

EXAMPLE 6-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVE
        ARG1,
MULWF
        ARG2
                     : ARG1 * ARG2 ->
                     ; PRODH: PRODL
        ARG2, SB
                    ; Test Sign Bit
SUBWF
        PRODH, F
                     ; PRODH = PRODH
                              - ARG1
MOVF
        ARG2, W
BTFSC
        ARG1, SB
                     ; Test Sign Bit
SUBWF
         PRODH, F
                     ; PRODH = PRODH
                               - ARG2
```

Example 6-3 shows the sequence to do a 16 \times 16 unsigned multiply. Equation 6-1 shows the algorithm that is used. The 32-bit result is stored in four registers, RES3:RES0.

EQUATION 6-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

```
RES3:RES0 = ARG1H:ARG1L • ARG2H:ARG2L

= (ARG1H • ARG2H • 2<sup>16</sup>)+

(ARG1H • ARG2L • 2<sup>8</sup>)+

(ARG1L • ARG2H • 2<sup>8</sup>)+

(ARG1L • ARG2L)
```

EXAMPLE 6-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

```
MOVE
        ARG1L, W
MULWF
        ARG2L
                    ; ARG1L * ARG2L ->
                    ; PRODH: PRODL
MOVFF
        PRODH, RES1 ;
MOVFF
        PRODL, RESO ;
MOVF
        ARG1H, W
                    ; ARG1H * ARG2H ->
MULWF
                    ; PRODH: PRODL
MOVFF
        PRODH, RES3 ;
        PRODL, RES2 ;
MOVFF
MOVF
        ARG1L, W
\texttt{MULWF}
        ARG2H
                    ; ARG1L * ARG2H ->
                    ; PRODH:PRODL
MOVF
        PRODL, W
ADDWF
        RES1, F ; Add cross
MOVF
        PRODH, W
                  ; products
ADDWFC RES2, F
        WREG, F
CLRF
ADDWFC
        RES3, F
                    ;
MOVF
        ARG1H, W
                    ; ARG1H * ARG2L ->
MULWF
        ARG2L
                    ; PRODH:PRODL
MOVF
        PRODL, W
ADDWF
        RES1, F
                    ; Add cross
MOVF
                    ; products
        PRODH, W
ADDWFC RES2, F
CLRF
        WREG, F
                    ;
ADDWFC
        RES3, F
                    ;
```

Example 6-4 shows the sequence to do a 16 x 16 signed multiply. Equation 6-2 shows the algorithm used. The 32-bit result is stored in four registers, RES3:RES0. To account for the sign bits of the arguments, each argument pairs' Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EQUATION 6-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

```
RES3:RES0

= ARG1H:ARG1L • ARG2H:ARG2L

= (ARG1H • ARG2H • 2<sup>16</sup>) +
    (ARG1H • ARG2L • 2<sup>8</sup>) +
    (ARG1L • ARG2H • 2<sup>8</sup>) +
    (ARG1L • ARG2H • 2<sup>8</sup>) +
    (ARG1L • ARG2L) +
    (-1 • ARG2H<7> • ARG1H:ARG1L • 2<sup>16</sup>) +
    (-1 • ARG1H<7> • ARG2H:ARG2L • 2<sup>16</sup>)
```

EXAMPLE 6-4: 16 x 16 SIGNED MULTIPLY ROUTINE

```
MOVE
           ARG1L, W
  MULWF
           ARG2L
                       ; ARG1L * ARG2L ->
                       ; PRODH: PRODL
   MOVFF
           PRODH, RES1 ;
  MOVFF
           PRODL, RESO ;
  MOVF
           ARG1H, W
                      ; ARG1H * ARG2H ->
  MULWF
           ARG2H
                       ; PRODH: PRODL
  MOVFF
           PRODH, RES3 ;
           PRODL, RES2 ;
  MOVFF
  MOVF
           ARG1L, W
  MULWF
           ARG2H
                      ; ARG1L * ARG2H ->
                       ; PRODH:PRODL
           PRODL, W
  MOVF
  ADDWF
           RES1, F ; Add cross
  MOVF
           PRODH, W ; products
           RES2, F
  ADDWFC
           WREG, F
  CLRF
  ADDWFC
           RES3, F
   MOVF
           ARG1H, W
                       ; ARG1H * ARG2L ->
  MULWF
           ARG2L
                       ; PRODH:PRODL
  MOVF
           PRODL, W
  ADDWF
           RES1, F ; Add cross
  MOVF
           PRODH, W ; products
           RES2, F
  ADDWFC
  CLRF
           WREG, F
  ADDWFC
           RES3, F
  BTFSS
           ARG2H, 7
                       ; ARG2H:ARG2L neg?
           SIGN ARG1 ; no, check ARG1
  BRA
           ARG1L, W
  MOVF
  SUBWF
           RES2
  MOVF
           ARG1H, W
  SUBWEB
           RES3
SIGN ARG1
  BTFSS
           ARG1H, 7
                       ; ARG1H:ARG1L neg?
   BRA
           CONT_CODE
                      ; no, done
           ARG2L, W
  MOVF
  SUBWE
           RES2
  MOVF
           ARG2H, W
  SUBWFB
           RES3
CONT_CODE
    :
```

7.0 INTERRUPTS

The PIC18CXX2 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high priority level, or a low priority level. The high priority interrupt vector is at 000008h and the low priority interrupt vector is at 000018h. High priority interrupt events will override any low priority interrupts that may be in progress.

There are ten registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2
- PIE1, PIE2
- IPR1, IPR2

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

Each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- · Priority bit to select high priority or low priority

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set. Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared. When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h, depending on the priority level. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

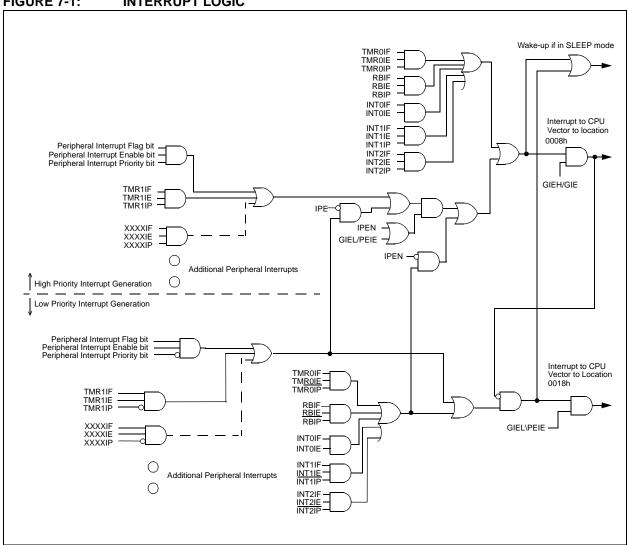
When an interrupt is responded to, the Global Interrupt Enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH, or GIEL bit. High priority interrupt sources can interrupt a low priority interrupt.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INT pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

FIGURE 7-1: **INTERRUPT LOGIC**



7.1 INTCON Registers

The INTCON Registers are readable and writable registers, which contains various enable, priority, and flag bits.

REGISTER 7-1: INTCON REGISTER

GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7 GIE/GIEH: Global Interrupt Enable bit

When IPEN = 0:

1 = Enables all unmasked interrupts

0 = Disables all interrupts

When IPEN = 1:

1 = Enables all high priority interrupts

0 = Disables all high priority interrupts

bit 6 **PEIE/GIEL:** Peripheral Interrupt Enable bit

When IPEN = 0:

1 = Enables all unmasked peripheral interrupts

0 = Disables all peripheral interrupts

When IPEN = 1:

1 = Enables all low priority peripheral interrupts

0 = Disables all low priority peripheral interrupts

bit 5 TMR0IE: TMR0 Overflow Interrupt Enable bit

1 = Enables the TMR0 overflow interrupt

0 = Disables the TMR0 overflow interrupt

bit 4 INT0IE: INT0 External Interrupt Enable bit

1 = Enables the INT0 external interrupt

0 = Disables the INT0 external interrupt

bit 3 RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt

0 =Disables the RB port change interrupt

bit 2 TMR0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)

0 = TMR0 register did not overflow

bit 1 INT0IF: INT0 External Interrupt Flag bit

1 = The INTO external interrupt occurred (must be cleared in software)

0 = The INT0 external interrupt did not occur

bit 0 RBIF: RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)

0 = None of the RB7:RB4 pins have changed state

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

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REGISTER 7-2: INTCON2 REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP
bit 7							bit 0

bit 7 RBPU: PORTB Pull-up Enable bit

1 = All PORTB pull-ups are disabled

0 = PORTB pull-ups are enabled by individual port latch values

bit 6 INTEDG0:External Interrupt0 Edge Select bit

1 = Interrupt on rising edge

0 = Interrupt on falling edge

bit 5 INTEDG1: External Interrupt1 Edge Select bit

1 = Interrupt on rising edge

0 = Interrupt on falling edge

bit 4 INTEDG2: External Interrupt2 Edge Select bit

1 = Interrupt on rising edge

0 = Interrupt on falling edge

bit 3 Unimplemented: Read as '0'

bit 2 TMR0IP: TMR0 Overflow Interrupt Priority bit

1 = High priority

0 = Low priority

bit 1 Unimplemented: Read as '0'

bit 0 RBIP: RB Port Change Interrupt Priority bit

1 = High priority

0 = Low priority

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 7-3: INTCON3 REGISTER

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	_	INT2IE	INT1IE		INT2IF	INT1IF
hit 7							bit 0

bit 7 INT2IP: INT2 External Interrupt Priority bit

1 = High priority

0 = Low priority

bit 6 INT1IP: INT1 External Interrupt Priority bit

1 = High priority

0 = Low priority

bit 5 **Unimplemented:** Read as '0'

bit 4 INT2IE: INT2 External Interrupt Enable bit

1 = Enables the INT2 external interrupt

0 = Disables the INT2 external interrupt

bit 3 **INT1IE:** INT1 External Interrupt Enable bit

1 = Enables the INT1 external interrupt0 = Disables the INT1 external interrupt

bit 2 Unimplemented: Read as '0'

bit 1 INT2IF: INT2 External Interrupt Flag bit

1 = The INT2 external interrupt occurred (must be cleared in software)

0 = The INT2 external interrupt did not occur

bit 0 INT1IF: INT1 External Interrupt Flag bit

1 = The INT1 external interrupt occurred (must be cleared in software)

0 = The INT1 external interrupt did not occur

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

7.2 PIR Registers

The PIR registers contain the individual flag bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Flag Registers (PIR1, PIR2).

- **Note 1:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>).
 - 2: User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt, and after servicing that interrupt.

REGISTER 7-4: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (PIR1)

· · · -							
PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 7 bit 0

bit 7 PSPIF: Parallel Slave Port Read/Write Interrupt Flag bit

1 = A read or a write operation has taken place (must be cleared in software)

0 = No read or write has occurred

bit 6 ADIF: A/D Converter Interrupt Flag bit

1 = An A/D conversion completed (must be cleared in software)

0 = The A/D conversion is not complete

bit 5 RCIF: USART Receive Interrupt Flag bit

1 = The USART receive buffer, RCREG, is full (cleared when RCREG is read)

0 = The USART receive buffer is empty

bit 4 TXIF: USART Transmit Interrupt Flag bit

1 = The USART transmit buffer, TXREG, is empty (cleared when TXREG is written)

0 = The USART transmit buffer is full

bit 3 SSPIF: Master Synchronous Serial Port Interrupt Flag bit

1 = The transmission/reception is complete (must be cleared in software)

0 = Waiting to transmit/receive

bit 2 CCP1IF: CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

bit 1 TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0 TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)

0 = MR1 register did not overflow

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 7-5: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2 (PIR2)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_	BCLIF	LVDIF	TMR3IF	CCP2IF
bit 7							hit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 BCLIF: Bus Collision Interrupt Flag bit

1 = A bus collision occurred (must be cleared in software)

0 = No bus collision occurred

bit 2 LVDIF: Low Voltage Detect Interrupt Flag bit

1 = A low voltage condition occurred (must be cleared in software)
 0 = The device voltage is above the Low Voltage Detect trip point

bit 1 TMR3IF: TMR3 Overflow Interrupt Flag bit

1 = TMR3 register overflowed (must be cleared in software)

0 = TMR3 register did not overflow

bit 0 CCP2IF: CCPx Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

7.3 PIE Registers

The PIE registers contain the individual enable bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Enable Registers (PIE1, PIE2). When IPEN = 0, the PEIE bit must be set to enable any of these peripheral interrupts.

REGISTER 7-6: PERIPHERAL INTERRUPT ENABLE REGISTER 1 (PIE1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

PSPIE: Parallel Slave Port Read/Write Interrupt Enable bit
1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt
ADIE: A/D Converter Interrupt Enable bit
1 = Enables the A/D interrupt
0 = Disables the A/D interrupt
RCIE: USART Receive Interrupt Enable bit
1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt
TXIE: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt
SSPIE: Master Synchronous Serial Port Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt
CCP1IE: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt
TMR2IE: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt
TMR1IE: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt

0 = Disables the TMR1 overflow interrupt

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

REGISTER 7-7: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (PIE2)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	_	BCLIE	LVDIE	TMR3IE	CCP2IE
hit 7							hit 0

bit 7-4 Unimplemented: Read as '0'

bit 3 BCLIE: Bus Collision Interrupt Enable bit

1 = Enabled 0 = Disabled

bit 2 LVDIE: Low Voltage Detect Interrupt Enable bit

1 = Enabled0 = Disabled

bit 1 TMR3IE: TMR3 Overflow Interrupt Enable bit

1 = Enables the TMR3 overflow interrupt0 = Disables the TMR3 overflow interrupt

bit 0 CCP2IE: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt0 = Disables the CCP2 interrupt

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

7.4 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are two Peripheral Interrupt Priority Registers (IPR1, IPR2). The operation of the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

REGISTER 7-8: PERIPHERAL INTERRUPT PRIORITY REGISTER 1 (IPR1)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP
bit 7 bit 0							bit 0	

bit 7 PSPIP: Parallel Slave Port Read/Write Interrupt Priority bit

1 = High priority

0 = Low priority

bit 6 ADIP: A/D Converter Interrupt Priority bit

1 = High priority0 = Low priority

bit 5 RCIP: USART Receive Interrupt Priority bit

1 = High priority0 = Low priority

bit 4 TXIP: USART Transmit Interrupt Priority bit

1 = High priority0 = Low priority

bit 3 SSPIP: Master Synchronous Serial Port Interrupt Priority bit

1 = High priority0 = Low priority

bit 2 **CCP1IP**: CCP1 Interrupt Priority bit

1 = High priority0 = Low priority

bit 1 TMR2IP: TMR2 to PR2 Match Interrupt Priority bit

1 = High priority0 = Low priority

bit 0 TMR1IP: TMR1 Overflow Interrupt Priority bit

1 = High priority0 = Low priority

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 7-9: PERIPHERAL INTERRUPT PRIORITY REGISTER 2 (IPR2)

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
_	_	_	_	BCLIP	LVDIP	TMR3IP	CCP2IP
bit 7							bit 0

bit 7-4 Unimplemented: Read as '0'

bit 3 BCLIP: Bus Collision Interrupt Priority bit

1 = High priority0 = Low priority

bit 2 LVDIP: Low Voltage Detect Interrupt Priority bit

1 = High priority0 = Low priority

bit 1 TMR3IP: TMR3 Overflow Interrupt Priority bit

1 = High priority0 = Low priority

bit 0 CCP2IP: CCP2 Interrupt Priority bit

1 = High priority0 = Low priority

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

7.5 RCON Register

The RCON register contains the bit which is used to enable prioritized interrupts (IPEN).

REGISTER 7-10: RCON REGISTER

R/W-0	R/W-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	LWRT	_	RI	TO	PD	POR	BOR
bit 7							bit 0

bit 7 IPEN: Interrupt Priority Enable bit

1 = Enable priority levels on interrupts

0 = Disable priority levels on interrupts (16CXXX compatibility mode)

bit 6 **LWRT:** Long Write Enable bit

For details of bit operation, see Register 4-3

bit 5 Unimplemented: Read as '0'

bit 4 RI: RESET Instruction Flag bit

For details of bit operation, see Register 4-3

bit 3 **TO**: Watchdog Time-out Flag bit

For details of bit operation, see Register 4-3

bit 2 PD: Power-down Detection Flag bit

For details of bit operation, see Register 4-3

bit 1 POR: Power-on Reset Status bit

For details of bit operation, see Register 4-3

bit 0 BOR: Brown-out Reset Status bit

For details of bit operation, see Register 4-3

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

7.6 INTO Interrupt

External interrupts on the RB0/INT0, RB1/INT1 and RB2/INT2 pins are edge triggered: either rising, if the corresponding INTEDGx bit is set in the INTCON2 register, or falling, if the INTEDGx bit is clear. When a valid edge appears on the RBx/INTx pin, the corresponding flag bit INTxF is set. This interrupt can be disabled by clearing the corresponding enable bit INTxE. Flag bit INTxF must be cleared in software in the Interrupt Service Routine before re-enabling the interrupt. All external interrupts (INT0, INT1 and INT2) can wake-up the processor from SLEEP, if bit INTxE was set prior to going into SLEEP. If the global interrupt enable bit GIE set, the processor will branch to the interrupt vector following wake-up.

Interrupt priority for INT1 and INT2 is determined by the value contained in the interrupt priority bits, INT1IP (INTCON3<6>) and INT2IP (INTCON3<7>). There is no priority bit associated with INT0. It is always a high priority interrupt source.

7.7 TMR0 Interrupt

In 8-bit mode (which is the default), an overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit TMR0IF. In 16-bit mode, an overflow (FFFFh \rightarrow 0000h) in the TMR0H:TMR0L registers will set flag bit TMR0IF. The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). Interrupt priority for Timer0 is determined by the value contained in the interrupt priority bit TMR0IP (INTCON2<2>). See Section 8.0 for further details on the Timer0 module.

7.8 PORTB Interrupt-on-Change

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit, RBIE (INTCON<3>). Interrupt priority for PORTB Interrupt-on-change is determined by the value contained in the interrupt priority bit, RBIP (INTCON2<0>).

7.9 Context Saving During Interrupts

During an interrupt, the return PC value is saved on the stack. Additionally, the WREG, STATUS and BSR registers are saved on the fast return stack. If a fast return from interrupt is not used (see Section 4.3), the user may need to save the WREG, STATUS and BSR registers in software. Depending on the user's application, other registers may also need to be saved. Example 7-1 saves and restores the WREG, STATUS and BSR registers during an Interrupt Service Routine.

EXAMPLE 7-1: SAVING STATUS, WREG AND BSR REGISTERS IN RAM

```
W TEMP
MOVWF
                              ; W_TEMP is in virtual bank
MOVEE
       STATUS, STATUS_TEMP
                              ; STATUS TEMP located anywhere
MOVFF
       BSR, BSR TEMP
                              ; BSR located anywhere
; USER ISR CODE
MOVFF
       BSR TEMP, BSR
                              ; Restore BSR
MOVF
       W TEMP, W
                              ; Restore WREG
       STATUS TEMP, STATUS
                              ; Restore STATUS
```

NOTES:

8.0 I/O PORTS

Depending on the device selected, there are either five ports, or three ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The data latch (LAT register) is useful for read-modifywrite operations on the value that the I/O pins are driving.

8.1 PORTA, TRISA and LATA Registers

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as digital inputs.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register reads and writes the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

The other PORTA pins are multiplexed with analog inputs and the analog VREF+ and VREF- inputs. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 8-1: INITIALIZING PORTA

CLRF PORTA	; Initialize PORTA by
	; clearing output
	; data latches
CLRF LATA	; Alternate method
	; to clear output
	; data latches
MOVLW 0x07	; Configure A/D
MOVWF ADCON1	; for digital inputs
MOVLW 0xCF	; Value used to
	; initialize data
	; direction
MOVWF TRISA	; Set RA<3:0> as inputs
	; RA<5:4> as outputs
	-

FIGURE 8-1: BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS

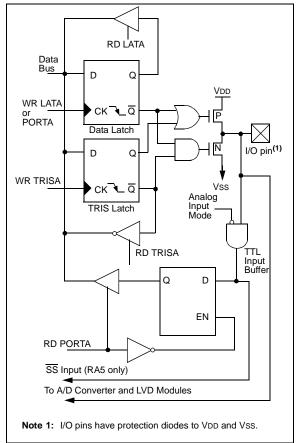


FIGURE 8-2: BLOCK DIAGRAM OF RA4/T0CKI PIN

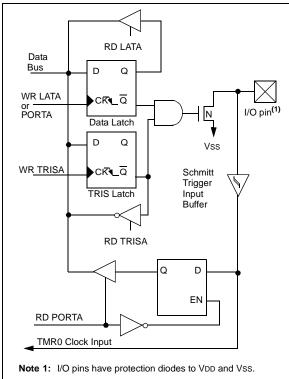


FIGURE 8-3: BLOCK DIAGRAM OF RA6

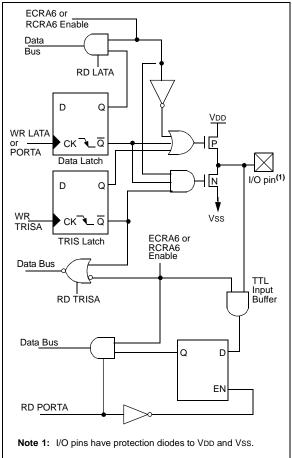


TABLE 8-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function			
RA0/AN0	bit0	TTL	Input/output or analog input.			
RA1/AN1	bit1	TTL	Input/output or analog input.			
RA2/AN2/VREF-	bit2	TTL	Input/output or analog input or VREF			
RA3/AN3/VREF+	bit3	TTL	Input/output or analog input or VREF+.			
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0. Output is open drain type.			
RA5/SS/AN4/LVDIN	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input, or low voltage detect input.			
OSC2/CLKO/RA6	bit6	TTL	OSC2 or clock output or I/O pin.			

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTA	_	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
LATA	_	Latch A	Data Out	out Regis	ter				xx xxxx	uu uuuu
TRISA	_	PORTA	ORTA Data Direction Register						11 1111	11 1111
ADCON1	ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0	0- 0000	0- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

8.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as digital inputs.

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register reads and writes the latched output value for PORTB.

EXAMPLE 8-2: INITIALIZING PORTB

CLRF PORTB	; Initialize PORTB by
	; clearing output
	; data latches
CLRF LATB	; Alternate method
	; to clear output
	; data latches
MOVLW 0xCF	; Value used to
	; initialize data
	; direction
MOVWF TRISB	; Set RB<3:0> as inputs
	; RB<5:4> as outputs
	; RB<7:6> as inputs

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of the PORTB pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

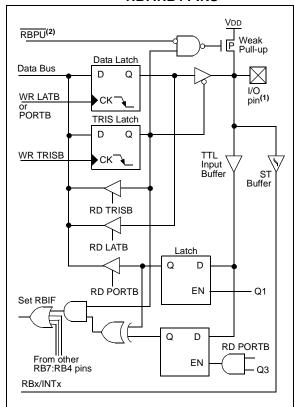
- Any read or write of PORTB (except with the MOVFF instruction). This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

RB3 can be configured by the configuration bit CCP2MX as the alternate peripheral pin for the CCP2 module (CCP2MX = '0').

FIGURE 8-4: BLOCK DIAGRAM OF RB7:RB4 PINS



- Note 1: I/O pins have diode protection to VDD and Vss.
 - 2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (INTCON2<7>).

FIGURE 8-5: BLOCK DIAGRAM OF RB2:RB0 PINS

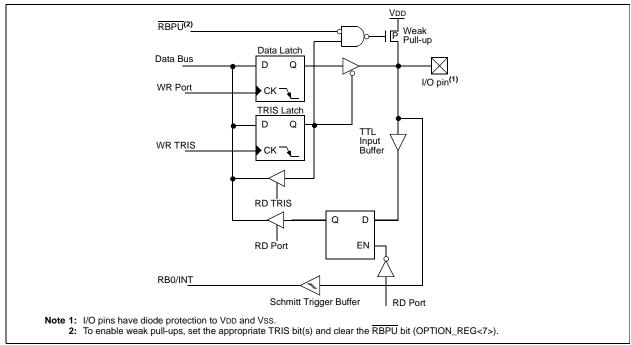


FIGURE 8-6: BLOCK DIAGRAM OF RB3

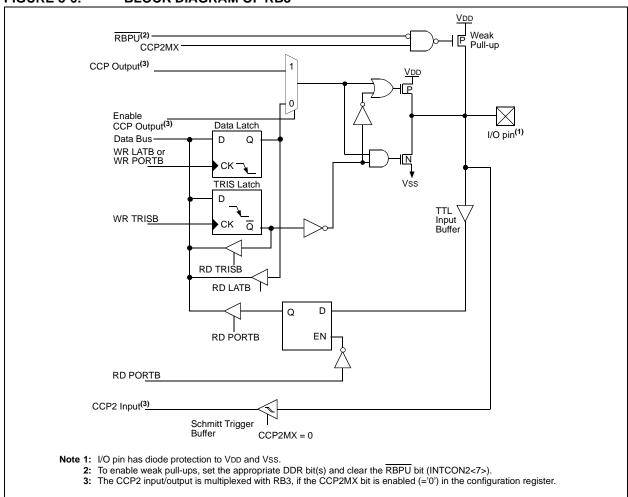


TABLE 8-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT0	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input1. Internal software programmable weak pull-up.
RB1/INT1	bit1	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input2. Internal software programmable weak pull-up.
RB2/INT2	bit2	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input3. Internal software programmable weak pull-up.
RB3/CCP2 ⁽³⁾	bit3	TTL/ST ⁽⁴⁾	Input/output pin. Capture2 input/Compare2 output/PWM output when CCP2MX configuration bit is enabled. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

- 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
- 3: A device configuration bit selects which I/O pin the CCP2 pin is multiplexed on.
- 4: This buffer is a Schmitt Trigger input when configured as the CCP2 input.

TABLE 8-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
LATB	LATB Da	ATB Data Output Register								
TRISB	PORTB	Data Direction	n Register						1111 1111	1111 1111
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	_	TMR0IP	_	RBIP	1111 -1-1	1111 -1-1
INTCON3	INT2IP	INT1IP	_	INT2IE	INT1IE	_	INT2IF	INT1IF	11-0 0-00	11-0 0-00

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

8.3 PORTC, TRISC and LATC Registers

PORTC is an 8-bit wide, bi-directional port. The corresponding Data Direction Register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as digital inputs.

The Data Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register reads and writes the latched output value for PORTC.

PORTC is multiplexed with several peripheral functions (Table 8-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register, without concern due to peripheral overrides.

RC1 is normally configured by the configuration bit CCP2MX as the default peripheral pin for the CCP2 module (default/erased state, CCP2MX = '1').

EXAMPLE 8-3: INITIALIZING PORTC

CLRF	PORTC	; Initialize PORTC by
		; clearing output
		; data latches
CLRF	LATC	; Alternate method
		; to clear output
		; data latches
MOVLW	0xCF	; Value used to
		; initialize data
		; direction
MOVWF	TRISC	; Set RC<3:0> as inputs
		; RC<5:4> as outputs
		; RC<7:6> as inputs

FIGURE 8-7: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)

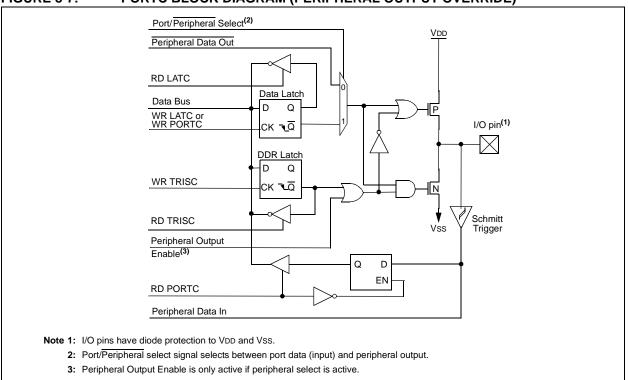


TABLE 8-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit1	ST	Input/output port pin, Timer1 oscillator input, or Capture2 input/ Compare2 output/PWM output when CCP2MX configuration bit is disabled.
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or Data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port Data output.
RC6/TX/CK	bit6	ST	Input/output port pin, Addressable USART Asynchronous Transmit, or Addressable USART Synchronous Clock.
RC7/RX/DT	bit7	ST	Input/output port pin, Addressable USART Asynchronous Receive, or Addressable USART Synchronous Data.

Legend: ST = Schmitt Trigger input

TABLE 8-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
LATC	LATC D	ATC Data Output Register xxxx xxxx uuu								uuuu uuuu
TRISC	PORTC	ORTC Data Direction Register								1111 1111

Legend: x = unknown, u = unchanged

8.4 PORTD, TRISD and LATD Registers

This section is only applicable to the PIC18C4X2 devices.

PORTD is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as digital inputs.

The Data Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register reads and writes the latched output value for PORTD.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL. See Section 8.6 for additional information on the Parallel Slave Port (PSP).

EXAMPLE 8-4: INITIALIZING PORTD

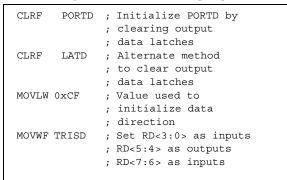


FIGURE 8-8: PORTD BLOCK DIAGRAM IN I/O PORT MODE

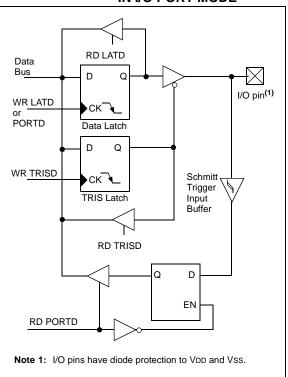


TABLE 8-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit0.
RD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit1.
RD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit2.
RD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit3.
RD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit4.
RD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit5.
RD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit6.
RD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin or parallel slave port bit7.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 8-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS	
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu	
LATD	LATD [Data Out	put Regis	ster					xxxx xxxx	uuuu uuuu	
TRISD	PORTE	PORTD Data Direction Register 1111 1111 11									
TRISE	IBF	OBF	IBOV	on bits	0000 -111	0000 -111					

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

8.5 PORTE, TRISE and LATE Registers

This section is only applicable to the PIC18C4X2 devices.

PORTE is a 3-bit wide, bi-directional port. The corresponding Data Direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, these pins are configured as digital inputs.

The Data Latch register (LATE) is also memory mapped. Read-modify-write operations on the LATE register reads and writes the latched output value for PORTE.

PORTE has three pins (RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7), which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers.

Register 8-1 shows the TRISE register, which also controls the parallel slave port operation.

PORTE pins are multiplexed with analog inputs. When selected as an analog input, these pins will read as '0's.

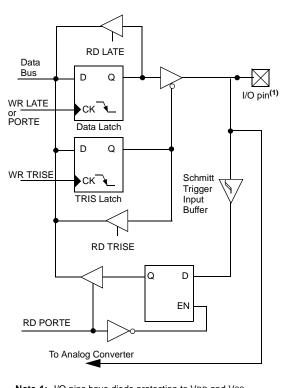
TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.

Note: On a Power-on Reset, these pins are configured as analog inputs.

EXAMPLE 8-5: INITIALIZING PORTE

	LL U-J.	INTIALIZING FORTE
CLRF	PORTE	; Initialize PORTE by
		; clearing output
		; data latches
CLRF	LATE	; Alternate method
		; to clear output
		; data latches
MOVLW	0x07	; Configure A/D
MOVWF	ADCON1	; for digital inputs
MOVLW	0x03	; Value used to
		; initialize data
		; direction
MOVWF	TRISC	; Set RE<0> as inputs
		; RE<1> as outputs
		; RE<2> as inputs

FIGURE 8-9: PORTEBLOCK DIAGRAM IN I/O PORT MODE



Note 1: I/O pins have diode protection to VDD and Vss.

REGISTER 8-1: TRISE REGISTER

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	_	TRISE2	TRISE1	TRISE0
bit 7							bit 0

bit 7 IBF: Input Buffer Full Status bit

1 = A word has been received and waiting to be read by the CPU

0 = No word has been received

bit 6 **OBF**: Output Buffer Full Status bit

1 = The output buffer still holds a previously written word

0 = The output buffer has been read

bit 5 **IBOV**: Input Buffer Overflow Detect bit (in Microprocessor mode)

1 = A write occurred when a previously input word has not been read

(must be cleared in software)

0 = No overflow occurred

bit 4 **PSPMODE**: Parallel Slave Port Mode Select bit

1 = Parallel Slave Port mode

0 = General purpose I/O mode

bit 3 Unimplemented: Read as '0'

bit 2 TRISE2: RE2 Direction Control bit

1 = Input

0 = Output

bit 1 TRISE1: RE1 Direction Control bit

1 = Input

0 = Output

bit 0 TRISE0: RE0 Direction Control bit

1 = Input

0 = Output

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

TABLE 8-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/RD/AN5	bit0	ST/TTL ⁽¹⁾	Input/output port pin or read control input in Parallel Slave Port mode or analog input: RD
			1 = Not a read operation0 = Read operation. Reads PORTD register (if chip selected).
RE1/WR/AN6	bit1	ST/TTL ⁽¹⁾	Input/output port pin or write control input in Parallel Slave Port mode or analog input: WR 1 = Not a write operation 0 = Write operation. Writes PORTD register (if chip selected).
RE2/CS/AN7	bit2	ST/TTL ⁽¹⁾	Input/output port pin or chip select control input in Parallel Slave Port mode or analog input: CS 1 = Device is not selected 0 = Device is selected

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 8-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTE	_	_	-	_	_	RE2	RE1	RE0	000	000
LATE	_	_	_	_	_	LATE Data	Output Reg	ister	xxx	uuu
TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Data Direction bits			0000 -111	0000 -111
ADCON1	ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

8.6 Parallel Slave Port

The Parallel Slave Port is implemented on the 40-pin devices only (PIC18C4X2).

PORTD operates as an 8-bit wide, parallel slave port, or microprocessor port, when control bit PSPMODE (TRISE<4>) is set. It is asynchronously readable and writable by the external world through RD control input pin RE0/RD and WR control input pin RE1/WR.

It can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD to be the RD input, RE1/WR to be the WR input and RE2/CS to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set). The A/D port configuration bits PCFG2:PCFG0 (ADCON1<2:0>) must be set, which will configure pins RE2:RE0 as digital I/O.

A write to the PSP occurs when both the \overline{CS} and \overline{WR} lines are first detected low. A read from the PSP occurs when both the \overline{CS} and \overline{RD} lines are first detected low.

The PORTE I/O pins become control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs), and the ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

FIGURE 8-10: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE

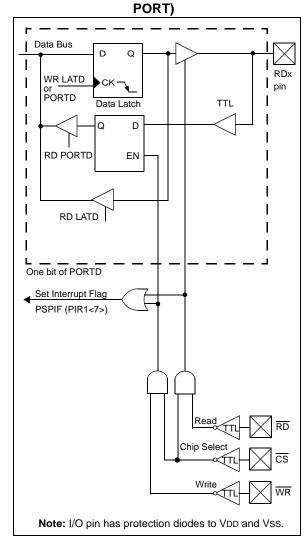
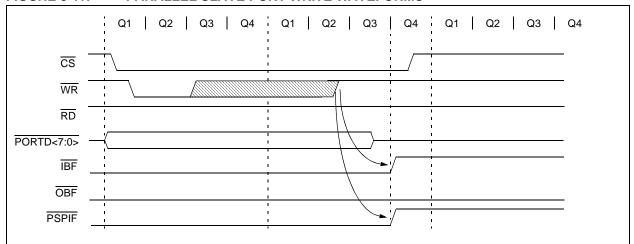


FIGURE 8-11: PARALLEL SLAVE PORT WRITE WAVEFORMS



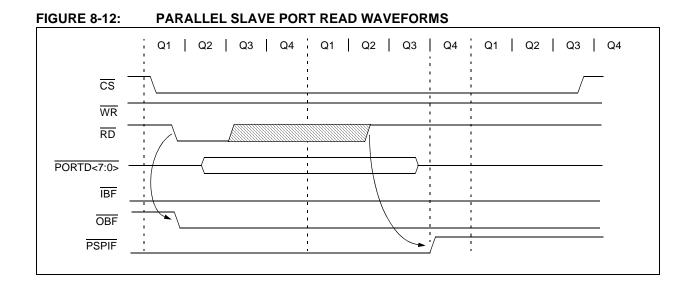


TABLE 8-11: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTD	Port Data	Latch whe	n written; F	Port pins when	read				xxxx xxxx	uuuu uuuu
LATD	LATD Data	Data Output bits			xxxx xxxx	uuuu uuuu				
TRISD	PORTD D	ata Directi	on bits						1111 1111	1111 1111
PORTE	_	_	_	_	_	RE2	RE1	RE0	000	000
LATE	_	_	_	_	_	LATE Data	a Output bits	3	xxx	uuu
TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE D	ata Directio	n bits	0000 -111	0000 -111
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IF	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
ADCON1	ADFM	ADCS2	-	-	PCFG3	PCFG2	PCFG1	PCFG0	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Parallel Slave Port.

NOTES:

9.0 TIMERO MODULE

The Timer0 module has the following features:

- Software selectable as an 8-bit or 16-bit timer/ counter
- Readable and writable
- Dedicated 8-bit software programmable prescaler
- · Clock source selectable to be external or internal
- Interrupt-on-overflow from FFh to 00h in 8-bit mode and FFFFh to 0000h in 16-bit mode
- · Edge select for external clock

Figure 9-1 shows a simplified block diagram of the Timer0 module in 8-bit mode and Figure 9-2 shows a simplified block diagram of the Timer0 module in 16-bit mode

The T0CON register (Register 9-1) is a readable and writable register that controls all the aspects of Timer0, including the prescale selection.

REGISTER 9-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR00N	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							hit 0

bit 7 TMR00N: Timer0 On/Off Control bit

1 = Enables Timer0

0 = Stops Timer0

bit 6 T08BIT: Timer0 8-bit/16-bit Control bit

1 = Timer0 is configured as an 8-bit timer/counter

0 = Timer0 is configured as a 16-bit timer/counter

bit 5 TOCS: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4 T0SE: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on TOCKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Timer0 Prescaler Assignment bit

1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.

0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2:0 TOPS2:TOPS0: Timer0 Prescaler Select bits

111 = 1:256 prescale value

110 = 1:128 prescale value

101 = 1:64 prescale value

100 = 1:32 prescale value

011 = 1:16 prescale value

010 = 1:8 prescale value

001 = 1:4 prescale value

000 = 1:2 prescale value

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

FIGURE 9-1: TIMERO BLOCK DIAGRAM IN 8-BIT MODE

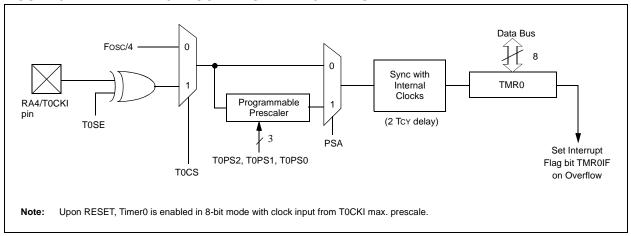
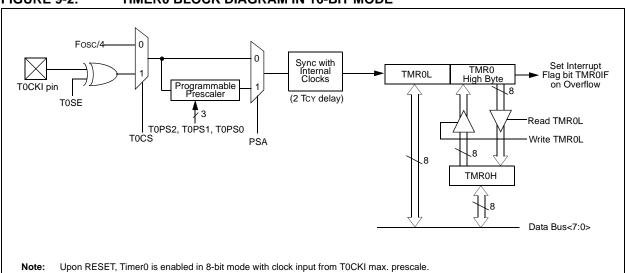


FIGURE 9-2: TIMERO BLOCK DIAGRAM IN 16-BIT MODE



9.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing the TOCS bit. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit. In Counter mode, Timer0 will increment either on every rising, or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit (T0SE). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

9.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not readable or writable.

The PSA and T0PS2:T0PS0 bits determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF $\,$ TMR0 , $\,$ MOVWF $\,$ TMR0 , $\,$ BSF $\,$ TMR0 , $\,$ x....etc.) will clear the prescaler count.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

9.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution).

9.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF bit. The interrupt can be masked by clearing the TMR0IE bit. The TMR0IE bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

9.4 16-Bit Mode Timer Reads and Writes

TMR0H is not the high byte of the timer/counter in 16-bit mode, but is actually a buffered version of the high byte of Timer0 (refer to Figure 9-2). The high byte of the Timer0 counter/timer is not directly readable nor writable. TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16-bits of Timer0 without having to verify that the read of the high and low byte were valid due to a rollover between successive reads of the high and low byte.

A write to the high byte of Timer0 must also take place through the TMR0H buffer register. Timer0 high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16-bits of Timer0 to be updated at once.

TABLE 9-1: REGISTERS ASSOCIATED WITH TIMERO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
TMR0L	Timer0 Modu	ule's Low Byte	xxxx xxxx	uuuu uuuu						
TMR0H	Timer0 Modu	ule's High Byte	Register						0000 0000	0000 0000
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
T0CON	TMR00N	T08BIT	T0CS	T0SE	1111 1111	1111 1111				
TRISA	_	_	PORTA D	ata Directi	11 1111	11 1111				

 $\label{eq:localization} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \ \textbf{u} = \textbf{unchanged}, \ \textbf{-} = \textbf{unimplemented locations read as '0'}. \ \textbf{Shaded cells are not used by Timer0}.$

NOTES:

10.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers: TMR1H and TMR1L)
- Readable and writable (both registers)
- · Internal or external clock select
- Interrupt-on-overflow from FFFh to 0000h
- · Reset from CCP module special event trigger

Figure 10-1 is a simplified block diagram of the Timer1 module.

Register 10-1 details the Timer1 control register. This register controls the operating mode of the Timer1 module, and contains the Timer1 oscillator enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit TMR1ON (T1CON<0>).

REGISTER 10-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	_	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N
bit 7							bit 0

- bit 7 RD16: 16-bit Read/Write Mode Enable bit
 - 1 = Enables register Read/Write of TImer1 in one 16-bit operation
 0 = Enables register Read/Write of Timer1 in two 8-bit operations
- bit 6 Unimplemented: Read as '0'
- bit 5-4 T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits
 - 11 = 1:8 Prescale value
 - 10 = 1:4 Prescale value
 - 01 = 1:2 Prescale value
 - 00 = 1:1 Prescale value
- bit 3 T10SCEN: Timer1 Oscillator Enable bit
 - 1 = Timer1 Oscillator is enabled
 - 0 = Timer1 Oscillator is shut-off

The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2 T1SYNC: Timer1 External Clock Input Synchronization Select bit

When TMR1CS = 1:

- 1 = Do not synchronize external clock input
- 0 = Synchronize external clock input

When TMR1CS = 0:

This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

- bit 1 TMR1CS: Timer1 Clock Source Select bit
 - 1 = External clock from pin RC0/T10S0/T13CKI (on the rising edge)
 - 0 = Internal clock (Fosc/4)
- bit 0 TMR1ON: Timer1 On bit
 - 1 = Enables Timer1
 - 0 = Stops Timer1

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

10.1 **Timer1 Operation**

Timer1 can operate in one of these modes:

- · As a timer
- · As a synchronous counter
- · As an asynchronous counter

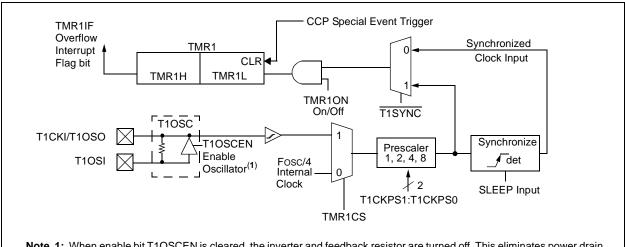
The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

When TMR1CS = 0, Timer1 increments every instruction cycle. When TMR1CS = 1, Timer1 increments on every rising edge of the external clock input or the Timer1 oscillator, if enabled.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ianored.

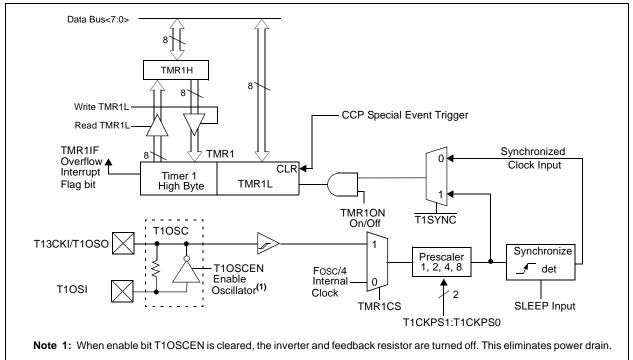
Timer1 also has an internal "RESET input". This RESET can be generated by the CCP module (Section 13.0).

FIGURE 10-1: TIMER1 BLOCK DIAGRAM



Note 1: When enable bit T10SCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

FIGURE 10-2: TIMER1 BLOCK DIAGRAM: 16-BIT READ/WRITE MODE



10.2 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 10-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

TABLE 10-1: CAPACITOR SELECTION FOR THE ALTERNATE OSCILLATOR

Osc Type	Freq.	C1	C2
LP	32 kHz	TBD ⁽¹⁾	TBD ⁽¹⁾

	Crystal to be Tested:	
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM

- **Note 1:** Microchip suggests 33 pF as a starting point in validating the oscillator circuit.
 - 2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
 - 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - **4:** Capacitor values are for design guidance only.

10.3 Timer1 Interrupt

The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

10.4 Resetting Timer1 using a CCP Trigger Output

If the CCP module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note: The special event triggers from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

10.5 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 10-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 high byte buffer. This provides the user with the ability to accurately read all 16-bits of Timer1, without having to determine whether a read of the high byte, followed by a read of the low byte, is valid, due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H buffer register. Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once. TMR1H is updated from the high byte when TMR1L is read.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 high byte buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

TABLE 10-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	RD16		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module. **Note 1:** The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

11.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- · Interrupt on TMR2 match of PR2
- SSP module optional use of TMR2 output to generate clock shift

Timer2 has a control register shown in Register 11-1. Timer2 can be shut-off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption. Figure 11-1 is a simplified block diagram of the Timer2 module. Register 11-1 shows the Timer2 control register. The prescaler and postscaler selection of Timer2 are controlled by this register.

11.1 Timer2 Operation

Timer2 can be used as the PWM time-base for the PWM mode of the CCP module. The TMR2 register is readable and writable, and is cleared on any device RESET. The input clock (Fosc/4) has a prescale option of 1:1, 1:4, or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>). The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- · a write to the TMR2 register
- a write to the T2CON register
- any device RESET (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 11-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 Unimplemented: Read as '0'

bit 6-3 TOUTPS3:TOUTPS0: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale 0001 = 1:2 Postscale

•

٠

•

1111 = 1:16 Postscale

bit 2 TMR2ON: Timer2 On bit

1 = Timer2 is on 0 = Timer2 is off

bit 1-0 T2CKPS1:T2CKPS0: Timer2 Clock Prescale Select bits

00 =Prescaler is 1 01 =Prescaler is 4 1x =Prescaler is 16

Legend:

 $R = Readable \ bit \ W = Writable \ bit \ U = Unimplemented \ bit, read as '0'$

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

11.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

11.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module, which optionally uses it to generate the shift clock.

FIGURE 11-1: TIMER2 BLOCK DIAGRAM

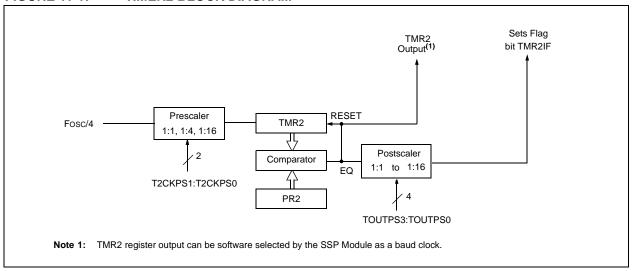


TABLE 11-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
TMR2	Timer2 Module Register								0000 0000	0000 0000
T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

12.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter (two 8-bit registers: TMR3H and TMR3L)
- Readable and writable (both registers)
- · Internal or external clock select
- Interrupt-on-overflow from FFFh to 0000h
- · Reset from CCP module trigger

Figure 12-1 is a simplified block diagram of the Timer3 module.

Register 12-1 shows the Timer3 control register. This register controls the operating mode of the Timer3 module and sets the CCP clock source.

Register 10-1 shows the Timer1 control register. This register controls the operating mode of the Timer1 module, as well as contains the Timer1 oscillator enable bit (T1OSCEN), which can be a clock source for Timer3.

REGISTER 12-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

- bit 7 RD16: 16-bit Read/Write Mode Enable
 - 1 = Enables register Read/Write of Timer3 in one 16-bit operation
 - 0 = Enables register Read/Write of Timer3 in two 8-bit operations
- bit 6-3 T3CCP2:T3CCP1: Timer3 and Timer1 to CCPx Enable bits
 - 1x = Timer3 is the clock source for compare/capture CCP modules
 - 01 = Timer3 is the clock source for compare/capture of CCP2, Timer1 is the clock source for compare/capture of CCP1
 - 00 = Timer1 is the clock source for compare/capture CCP modules
- bit 5-4 T3CKPS1:T3CKPS0: Timer3 Input Clock Prescale Select bits
 - 11 = 1:8 Prescale value
 - 10 = 1:4 Prescale value
 - 01 = 1:2 Prescale value
 - 00 = 1:1 Prescale value
- bit 2 T3SYNC: Timer3 External Clock Input Synchronization Control bit (Not usable if the system clock comes from Timer1/Timer3.)

When TMR3CS = 1:

- 1 = Do not synchronize external clock input
- 0 = Synchronize external clock input

When TMR3CS = 0:

This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.

- bit 1 TMR3CS: Timer3 Clock Source Select bit
 - 1 = External clock input from Timer1 oscillator or T1CKI (on the rising edge after the first falling edge)
 - 0 = Internal clock (Fosc/4)
- bit 0 TMR3ON: Timer3 On bit
 - 1 = Enables Timer3
 - 0 = Stops Timer3

Leaend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

12.1 **Timer3 Operation**

Timer3 can operate in one of these modes:

- · As a timer
- · As a synchronous counter
- · As an asynchronous counter

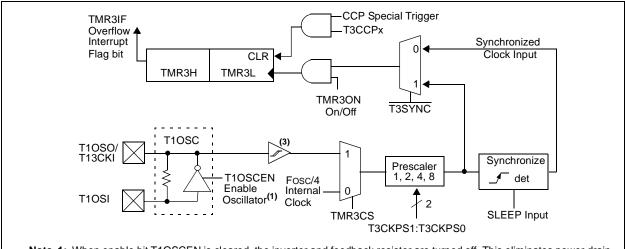
The operating mode is determined by the clock select bit, TMR3CS (T3CON<1>).

When TMR3CS = 0, Timer3 increments every instruction cycle. When TMR3CS = 1, Timer3 increments on every rising edge of the Timer1 external clock input or the Timer1 oscillator, if enabled.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ianored.

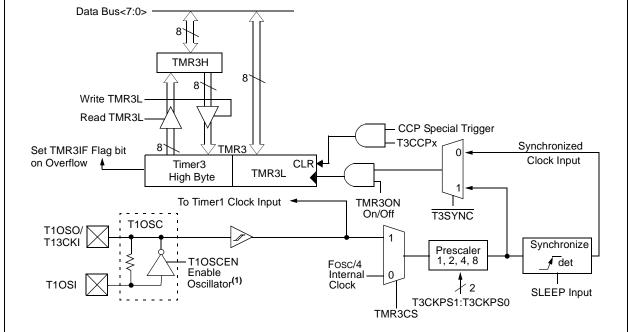
Timer3 also has an internal "RESET input". This RESET can be generated by the CCP module (Section 12.0).

FIGURE 12-1: TIMER3 BLOCK DIAGRAM



Note 1: When enable bit T10SCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

TIMER3 BLOCK DIAGRAM CONFIGURED IN 16-BIT READ/WRITE MODE **FIGURE 12-2:**



Note 1: When enable bit T1OSCEN is cleared, the inverter and feedback resistor are turned off. This eliminates power drain.

12.2 Timer1 Oscillator

The Timer1 oscillator may be used as the clock source for Timer3. The Timer1 oscillator is enabled by setting the T1OSCEN (T1CON<3>) bit. The oscillator is a low power oscillator rated up to 200 KHz. See Section 10.0 for further details.

12.3 Timer3 Interrupt

The TMR3 Register pair (TMR3H:TMR3L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR3IF (PIR2<1>). This interrupt can be enabled/disabled by setting/clearing TMR3 interrupt enable bit, TMR3IE (PIE2<1>).

12.4 Resetting Timer3 Using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer3.

Note: The special event triggers from the CCP module will not set interrupt flag bit TMR3IF (PIR1<0>).

Timer3 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer3 is running in Asynchronous Counter mode, this RESET operation may not work. In the event that a write to Timer3 coincides with a special event trigger from CCP1, the write will take precedence. In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer3.

TABLE 12-1: REGISTERS ASSOCIATED WITH TIMER3 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR2	_	_	_	_	BCLIF	LVDIF	TMR3IF	CCP2IF	0000 0000	0000 0000
PIE2	_	_	_	_	BCLIE	LVDIE	TMR3IE	CCP2IE	0000 0000	0000 0000
IPR2	_	_	_	_	BCLIP	LVDIP	TMR3IP	CCP2IP	0000 0000	0000 0000
TMR3L	Holding R	egister for t	he Least Siç	gnificant Byt	e of the 16-b	it TMR3 Re	gister		xxxx xxxx	uuuu uuuu
TMR3H	Holding R	Register for t	he Most Sig	nificant Byte	of the 16-bi	t TMR3 Reg	gister		xxxx xxxx	uuuu uuuu
T1CON	RD16		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	-000 0000	-uuu uuuu

 $\label{eq:local_equation} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \textbf{u} = \textbf{unchanged}, \textbf{-} = \textbf{unimplemented}, \textbf{read as '0'}. \quad \textbf{Shaded cells are not used by the Timer1 module}.$

NOTES:

13.0 CAPTURE/COMPARE/PWM (CCP) MODULES

Each CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register, or as a PWM master/slave Duty Cycle register. Table 13-1 shows the timer resources of the CCP module modes.

The operation of CCP1 is identical to that of CCP2, with the exception of the special event trigger. Therefore, operation of a CCP module in the following sections is described with respect to CCP1.

Table 13-2 shows the interaction of the CCP modules.

REGISTER 13-1: CCP1CON REGISTER/CCP2CON REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
hit 7							hit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 DCxB1:DCxB0: PWM Duty Cycle bit1 and bit0

Capture mode:

Unused

Compare mode:

Unused

PWM mode:

These bits are the two LSbs (bit1 and bit0) of the 10-bit PWM duty cycle. The upper eight bits (DCx9:DCx2) of the duty cycle are found in CCPRxL.

bit 3-0 CCPxM3:CCPxM0: CCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets CCPx module)

0001 = Reserved

0010 = Compare mode, toggle output on match (CCPxIF bit is set)

0011 = Reserved

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode,

Initialize CCP pin Low, on compare match force CCP pin High (CCPIF bit is set)

1001 = Compare mode,

Initialize CCP pin High, on compare match force CCP pin Low (CCPIF bit is set)

1010 = Compare mode,

Generate software interrupt on compare match (CCPIF bit is set, CCP pin is unaffected)

1011 = Compare mode,

Trigger special event (CCPIF bit is set)

11xx = PWM mode

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

13.1 CCP1 Module

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

TABLE 13-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

13.2 CCP2 Module

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. All are readable and writable.

TABLE 13-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	TMR1 or TMR3 time-base. Time-base can be different for each CCP.
Capture	Compare	The compare could be configured for the special event trigger, which clears either TMR1, or TMR3, depending upon which time-base is used.
Compare	Compare	The compare(s) could be configured for the special event trigger, which clears TMR1, or TMR3, depending upon which time-base is used.
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt).
PWM	Capture	None.
PWM	Compare	None.

13.3 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 or TMR3 registers when an event occurs on pin RC2/CCP1. An event is defined as:

- · every falling edge
- · every rising edge
- · every 4th rising edge
- · every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

13.3.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

13.3.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (either Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work. The timer to be used with each CCP module is selected in the T3CON register.

13.3.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit, CCP1IF, following any such change in operating mode.

13.3.4 CCP PRESCALER

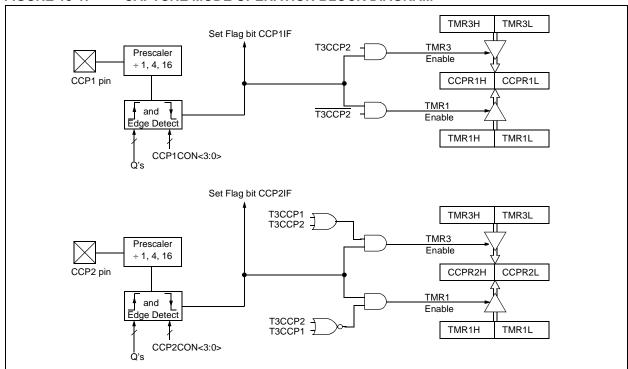
There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 13-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 13-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF CCP1CON, F; Turn CCP module off
MOVLW NEW_CAPT_PS; Load WREG with the
; new prescaler mode
; value and CCP ON
MOVWF CCP1CON ; Load CCP1CON with
; this value
```

FIGURE 13-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



13.4 Compare Mode

In Compare mode, the 16-bit CCPR1 (CCPR2) register value is constantly compared against either the TMR1 register pair value or the TMR3 register pair value. When a match occurs, the RC2/CCP1 (RC1/CCP2) pin is:

- · driven High
- · driven Low
- · toggle output (High to Low or Low to High)
- · remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP2M3:CCP2M0). At the same time, interrupt flag bit, CCP1IF (CCP2IF) is set.

13.4.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRISC bit.

Note:

Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

13.4.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

13.4.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

13.4.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCPx resets either the TMR1 or TMR3 register pair. Additionally, the CCP2 Special Event Trigger will start an A/D conversion if the A/D module is enabled.

Note: The special event trigger from the CCP2 module will not set the Timer1 or Timer3 interrupt flag bits.

FIGURE 13-2: COMPARE MODE OPERATION BLOCK DIAGRAM

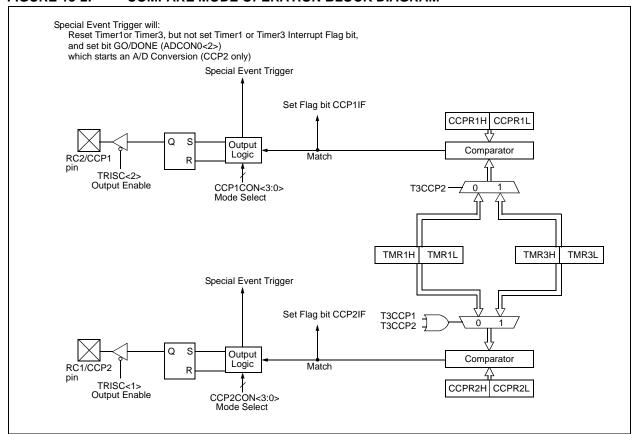


TABLE 13-3: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1 AND TIMER3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
TRISC	PORTC Da	ata Direction		1111 1111	1111 1111					
TMR1L	Holding Re	gister for th		xxxx xxxx	uuuu uuuu					
TMR1H	Holding Re	gister for th		xxxx xxxx	uuuu uuuu					
T1CON	RD16	_	T1CKPS1	T1CKPS0	T10SCEN	T1SYNC	TMR1CS	TMR10N	00 0000	uu uuuu
CCPR1L	Capture/Co	mpare/PW		xxxx xxxx	uuuu uuuu					
CCPR1H	Capture/Co	ompare/PW	M Register1	(MSB)					xxxx xxxx	uuuu uuuu
CCP1CON	_	_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000
CCPR2L	Capture/Co	mpare/PW	M Register2	(LSB)					xxxx xxxx	uuuu uuuu
CCPR2H	Capture/Co	ompare/PW	M Register2	(MSB)					xxxx xxxx	uuuu uuuu
CCP2CON	_	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00 0000	00 0000
PIR2	_	_	_	_	BCLIF	LVDIF	TMR3IF	CCP2IF	0000 0000	0000 0000
PIE2	_	_	_	_	BCLIE	LVDIE	TMR3IE	CCP2IE	0000 0000	0000 0000
IPR2	_	_	_	_	BCLIP	LVDIP	TMR3IP	CCP2IP	0000 0000	0000 0000
TMR3L	Holding Re	gister for th	e Least Sig	nificant Byte	of the 16-bi	t TMR3 Reg	gister		xxxx xxxx	uuuu uuuu
TMR3H	Holding Re	gister for th	ne Most Sigr	ificant Byte	of the 16-bit	TMR3 Reg	jister		xxxx xxxx	uuuu uuuu
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	-000 0000	-uuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

13.5 PWM Mode

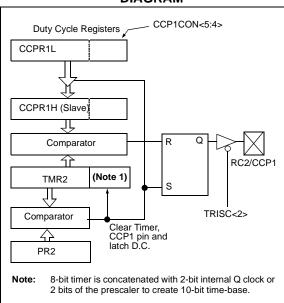
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 13-3 shows a simplified block diagram of the CCP module in PWM mode.

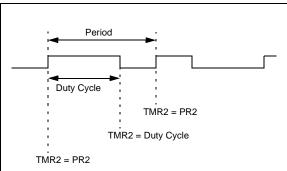
For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 13.5.3.

FIGURE 13-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 13-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 13-4: PWM OUTPUT



13.5.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- · TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 11.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

13.5.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation:

PWM Resolution (max) =
$$\frac{\log(\frac{Fosc}{FPWM})}{\log(2)}$$
bits

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

13.5.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

TABLE 13-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	14	12	10	8	7	6.58

TABLE 13-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu PC BC	R,	all o	e on other SETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	0000	000x	0000	000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000	0000	0000	0000
TRISC	PORTC Da		1111	1111	1111	1111						
TMR2	Timer2 Module Register									0000	0000	0000
PR2	Timer2 Mo	dule Period	Register						1111	1111	1111	1111
T2CON	1	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000	0000	-000	0000
CCPR1L	Capture/Co	ompare/PWI	M Register1	(LSB)					xxxx	xxxx	uuuu	uuuu
CCPR1H	Capture/Co	ompare/PWI	M Register1	(MSB)					xxxx	xxxx	uuuu	uuuu
CCP1CON		_	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000
CCPR2L	Capture/Compare/PWM Register2 (LSB)									xxxx	uuuu	uuuu
CCPR2H	Capture/Compare/PWM Register2 (MSB)									xxxx	uuuu	uuuu
CCP2CON	_	_	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00	0000	00	0000

 $\label{eq:local_equation} \textbf{Legend:} \quad \textbf{x} = \textbf{unknown}, \textbf{u} = \textbf{unchanged}, \textbf{-} = \textbf{unimplemented}, \textbf{read as '0'}. \textbf{Shaded cells are not used by PWM and Timer2}.$

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NOTES:

14.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

14.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI™)
- Inter-Integrated Circuit (I²C[™])
 - Full Master mode
 - Slave mode (with general address call)

The I²C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- · Slave mode

14.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2).

REGISTER 14-1: SSPSTAT: MSSP STATUS REGISTER

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/\overline{A}	Р	S	R/W	UA	BF
bit 7							bit 0

bit 7 SMP: Sample bit

SPI Master mode:

- 1 = Input data sampled at end of data output time
- 0 = Input data sampled at middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode

In I2C Master or Slave mode:

- 1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
- 0 = Slew rate control enabled for high speed mode (400 kHz)
- bit 6 CKE: SPI Clock Edge Select bit

CKP = 0:

- 1 = Data transmitted on rising edge of SCK
- 0 = Data transmitted on falling edge of SCK

CKP = 1:

- 1 = Data transmitted on falling edge of SCK
- 0 = Data transmitted on rising edge of SCK
- bit 5 **D/A:** Data/Address bit (I²C mode only)
 - 1 = Indicates that the last byte received or transmitted was data
 - 0 = Indicates that the last byte received or transmitted was address
- bit 4 **P:** STOP bit

(I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)

- 1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
- 0 = STOP bit was not detected last

Legend:			
R = Readable bit	W = Writable bit	W = Writable bit U = Unimplemented bit, read as	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 14-1: SSPSTAT: MSSP STATUS REGISTER (CONTINUED)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	Р	S	R/W	UA	BF
bit 7							bit 0

bit 0

bit 3 S: START bit

(I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)

- 1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
- 0 = START bit was not detected last

bit 2 **R/W:** Read/Write bit information (I²C mode only)

This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit, or not ACK bit.

In I²C Slave mode:

- 1 = Read
- 0 = Write

In I²C Master mode:

- 1 = Transmit is in progress
- 0 = Transmit is not in progress

OR-ing this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

bit 1 **UA:** Update Address bit (10-bit I²C mode only)

- 1 = Indicates that the user needs to update the address in the SSPADD register
- 0 = Address does not need to be updated

bit 0 BF: Buffer Full Status bit

Receive (SPI and <u>I²C</u> modes):

- 1 = Receive complete, SSPBUF is full
- 0 = Receive not complete, SSPBUF is empty

Transmit (I²C mode only):

- 1 = Data transmit in progress (does not include the ACK and STOP bits), SSPBUF is full
- 0 = Data transmit complete (does not include the ACK and STOP bits), SSPBUF is empty

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 14-2: SSPCON1: MSSP CONTROL REGISTER1

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |
| bit 7 | | | | | | | bit 0 |

bit 7 WCOL: Write Collision Detect bit

Master mode:

- 1 = A write to the SSPBUF register was attempted while the I²C conditions were not valid for a transmission to be started
- 0 = No collision

Slave mode:

- 1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
- 0 = No collision
- bit 6 SSPOV: Receive Overflow Indicator bit

In SPI mode:

- 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode.
 - In Slave mode, the user must read the SSPBUF, even if only transmitting data to avoid setting overflow.
 - In Master mode, the overflow bit is not set, since each new reception (and transmission) is initiated by writing to the SSPBUF register (must be cleared in software).
- 0 = No overflow

In I²C mode:

- 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
- 0 = No overflow

bit 5 SSPEN: Synchronous Serial Port Enable bit

In both modes when enabled, these pins must be properly configured as input or output.

In SPI mode:

- 1 = Enables serial port and configures SCK, SDO, SDI, and SS as the source of the serial port pins
- 0 = Disables serial port and configures these pins as I/O port pins

In I²C mode:

- 1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins
- 0 = Disables serial port and configures these pins as I/O port pins

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 14-2: SSPCON1: MSSP CONTROL REGISTER1 (CONTINUED)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |
| bit 7 | | | | | | | bit 0 |

bit 0

bit 4 CKP: Clock Polarity Select bit

In SPI mode:

1 = Idle state for clock is a high level

0 = Idle state for clock is a low level

In I²C Slave mode:

SCK release control

1 = Enable clock

0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

In I²C Master mode:

Unused in this mode

bit 3-0 SSPM3:SSPM0: Synchronous Serial Port Mode Select bits

0000 = SPI Master mode, clock = Fosc/4

0001 = SPI Master mode, clock = Fosc/16

0010 = SPI Master mode, clock = Fosc/64

0011 = SPI Master mode, clock = TMR2 output/2

0100 = SPI Slave mode, clock = SCK pin. \overline{SS} pin control enabled.

0101 = SPI Slave mode, clock = SCK pin. SS pin control disabled. SS can be used as I/O pin.

 $0110 = I^2C$ Slave mode, 7-bit address

 $0111 = I^2C$ Slave mode, 10-bit address

 $1000 = I^2C$ Master mode, clock = Fosc / (4 * (SSPADD+1))

1001 = Reserved

1010 = Reserved

 $1011 = I^2C$ firmware controlled Master mode (Slave idle)

1100 = Reserved

1101 = Reserved

 $1110 = I^2C$ Slave mode, 7-bit address with START and STOP bit interrupts enabled

1111 = I²C Slave mode, 10-bit address with START and STOP bit interrupts enabled

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 14-3: SSPCON2: MSSP CONTROL REGISTER2

bit 7			•	•			bit 0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

- bit 7 GCEN: General Call Enable bit (In I²C Slave mode only)
 - 1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
 - 0 = General call address disabled
- bit 6 **ACKSTAT:** Acknowledge Status bit (In I²C Master mode only)

In Master Transmit mode:

- 1 = Acknowledge was not received from slave
- 0 = Acknowledge was received from slave
- bit 5 **ACKDT:** Acknowledge Data bit (In I²C Master mode only)

In Master Receive mode:

Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.

- 1 = Not Acknowledge
- 0 = Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit (In I²C Master mode only)

In Master Receive mode:

- 1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
- 0 = Acknowledge sequence idle
- bit 3 RCEN: Receive Enable bit (In I²C Master mode only)
 - 1 = Enables Receive mode for I²C
 - 0 = Receive idle
- bit 2 **PEN:** STOP Condition Enable bit (In I²C Master mode only)

SCK Release Control:

- 1 = Initiate STOP condition on SDA and SCL pins. Automatically cleared by hardware.
- 0 = STOP condition idle
- bit 1 RSEN: Repeated START Condition Enabled bit (In I²C Master mode only)
 - 1 = Initiate Repeated START condition on SDA and SCL pins. Automatically cleared by hardware.
 - 0 = Repeated START condition idle
- bit 0 **SEN:** START Condition Enabled bit (In I²C Master mode only)
 - 1 = Initiate START condition on SDA and SCL pins. Automatically cleared by hardware.
 - 0 = START condition idle

Note: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

14.3 SPI Mode

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- · Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL/LVOIN

Additionally, a fourth pin may be used when in a Slave mode of operation:

Slave Select (SS) - RA5/SS/AN4

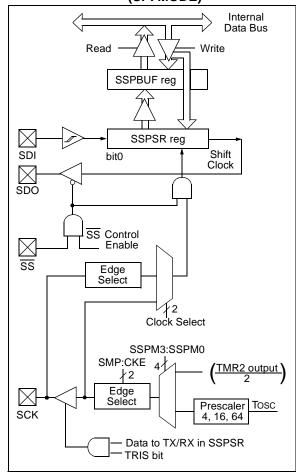
14.3.1 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data input sample phase (middle or end of data output time)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- · Slave Select mode (Slave mode only)

Figure 14-1 shows the block diagram of the MSSP module, when in SPI mode.

FIGURE 14-1: MSSP BLOCK DIAGRAM (SPI MODE)



The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR. until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit, BF (SSPSTAT<0>), and the interrupt flag bit, SSPIF, are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit, WCOL (SSPCON1<7>), will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

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When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a

transmitter. Generally the MSSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 14-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

EXAMPLE 14-1: LOADING THE SSPBUF (SSPSR) REGISTER

LOOP BT	FSS SSPSTAT, BF TO LOOP	;Has data been received(transmit complete)?
	VF SSPBUF, W	;WREG reg = contents of SSPBUF
MO	VWF RXDATA	;Save in user RAM, if data is meaningful
MO'	VF TXDATA, W VWF SSPBUF	;W reg = contents of TXDATA;New data to xmit

The SSPSR is not directly readable or writable, and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP status register (SSPSTAT) indicates the various status conditions.

14.3.2 ENABLING SPI I/O

To enable the serial port, SSP enable bit, SSPEN (SSPCON1<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON registers, and then set the SSPEN bit. This configures the SDI, SDO, SCK, and SS pins as serial

port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- · SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> bit cleared
- SCK (Master mode) must have TRISC<3> bit cleared
- SCK (Slave mode) must have TRISC<3> bit set
- SS must have TRISC<4> bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

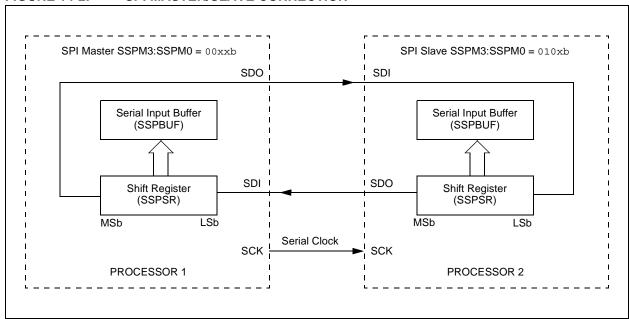
14.3.3 TYPICAL CONNECTION

Figure 14-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to same Clock Polarity (CKP), then both con-

trollers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- Master sends dummy data Slave sends data

FIGURE 14-2: SPI MASTER/SLAVE CONNECTION



14.3.4 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 14-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "Line Activity Monitor" mode.

The clock polarity is selected by appropriately programming the CKP bit (SSPCON1<4>). This then, would give waveforms for SPI communication as shown in

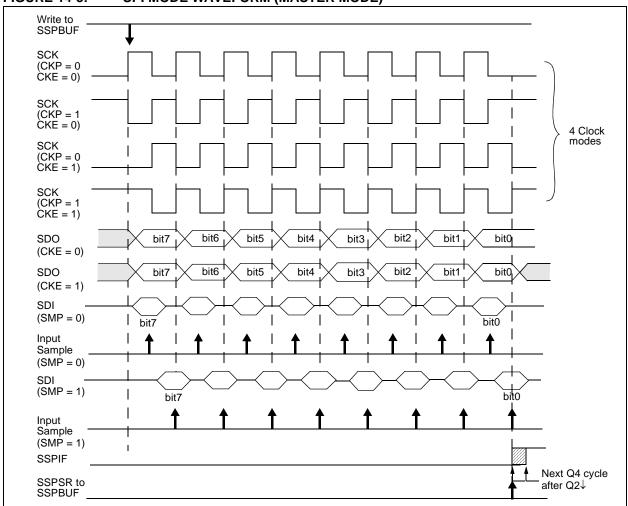
Figure 14-3, Figure 14-5, and Figure 14-6, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum data rate (at 40 MHz) of 10.00 Mbps.

Figure 14-3 shows the waveforms for Master mode. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 14-3: SPI MODE WAVEFORM (MASTER MODE)



14.3.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

14.3.6 SLAVE SELECT SYNCHRONIZATION

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the \overline{SS} pin to function as an input. The Data Latch must be high. When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven. When the \overline{SS} pin goes high,

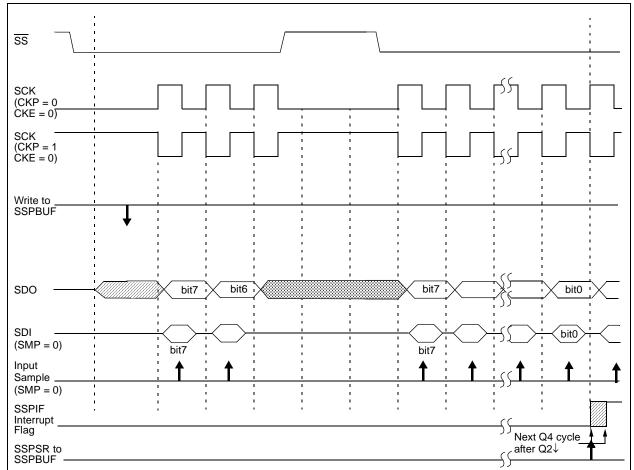
the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

- Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.
 - 2: If the SPI is used in Slave mode with CKE set, then the SS pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the SS pin to a high level, or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.







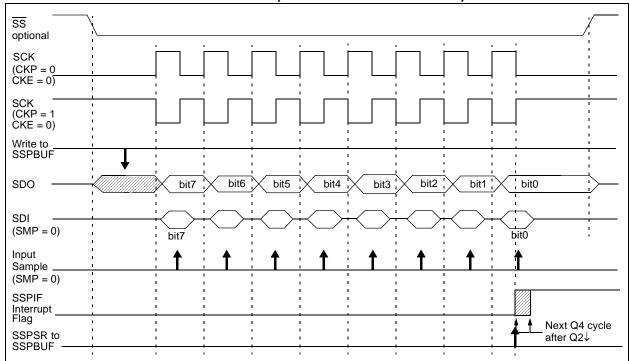
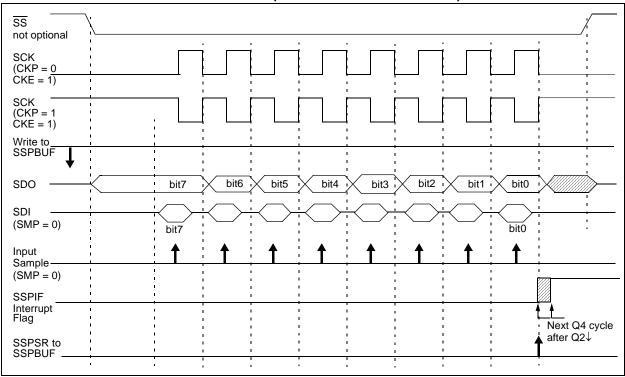


FIGURE 14-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



14.3.7 SLEEP OPERATION

In Master mode, all module clocks are halted, and the transmission/reception will remain in that state until the device wakes from SLEEP. After the device returns to normal mode, the module will continue to transmit/receive data.

In Slave mode, the SPI transmit/receive shift register operates asynchronously to the device. This allows the device to be placed in SLEEP mode, and data to be shifted into the SPI transmit/receive shift register. When all 8-bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device from SLEEP.

14.3.8 EFFECTS OF A RESET

A RESET disables the MSSP module and terminates the current transfer.

14.3.9 BUS MODE COMPATIBILITY

Table 14-1 shows the compatibility between the standard SPI modes and the states of the CKP and CKE control bits.

TABLE 14-1: SPI BUS MODES

Standard SPI Mode	Control Bits State				
Terminology	CKP	CKE			
0, 0	0	1			
0, 1	0	0			
1, 0	1	1			
1, 1	1	0			

There is also a SMP bit which controls when the data is sampled.

TABLE 14-2: REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF (1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE (1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP (1)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
TRISC	PORTC Data Direction Register								1111 1111	1111 1111
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
TRISA	_	PORTA Data Direction Register							11 1111	11 1111
SSPSTAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

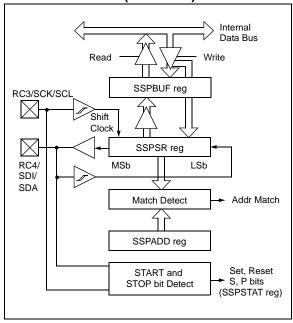
14.4 MSSP I²C Operation

The MSSP module in I²C mode, fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

The MSSP module functions are enabled by setting MSSP enable bit SSPEN (SSPCON<5>).

FIGURE 14-7: MSSP BLOCK DIAGRAM (I²C MODE)



The MSSP module has six registers for I^2C operation. These are the:

- MSSP Control Register1 (SSPCON1)
- MSSP Control Register2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- MSSP Shift Register (SSPSR) Not directly accessible
- MSSP Address Register (SSPADD)

The SSPCON1 register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Master mode, clock = OSC/4 (SSPADD +1)
- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with START and STOP bit interrupts enabled
- I²C Slave mode (10-bit address), with START and STOP bit interrupts enabled
- I²C Firmware controlled master operation, slave is idle

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to be inputs by setting the appropriate TRISC bits.

14.4.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the MSSP module not to give this \overline{ACK} pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. The BF bit is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I^2C specification, as well as the requirement of the MSSP module, are shown in timing parameter #100 and parameter #101.

14.4.1.1 Addressing

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit BF is set.
- c) An ACK pulse is generated.
- d) MSSP interrupt flag bit SSPIF (PIR1<3>) is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/\overline{W} (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7-9 for slave-transmitter:

- Receive first (high) byte of Address (bits SSPIF, BF and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
- Update the SSPADD register with the first (high) byte of Address. If match releases SCL line, this will clear bit UA.
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive Repeated START condition.
- Receive first (high) byte of Address (bits SSPIF and BF are set).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

14.4.1.2 Reception

When the R/\overline{W} bit of the address byte is clear and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address <u>byte</u> overflow condition exists, then no Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

14.4.1.3 Transmission

When the R/\overline{W} bit of the incoming address byte is set and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The \overline{ACK} pulse will be sent on the ninth bit and pin RC3/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 14-9).

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not \overline{ACK}), then the data transfer is complete. When the \overline{ACK} is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the START bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Pin RC3/SCK/SCL should be enabled by setting bit CKP.

FIGURE 14-8: I²C SLAVE MODE WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

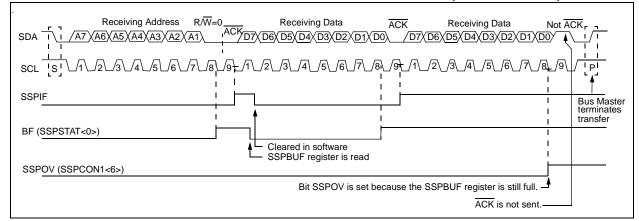
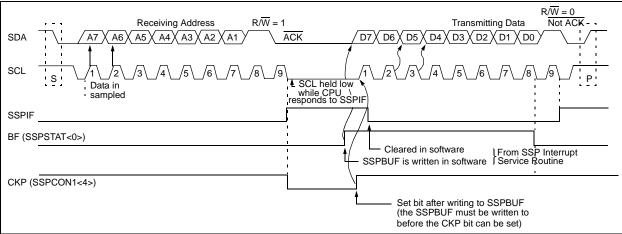
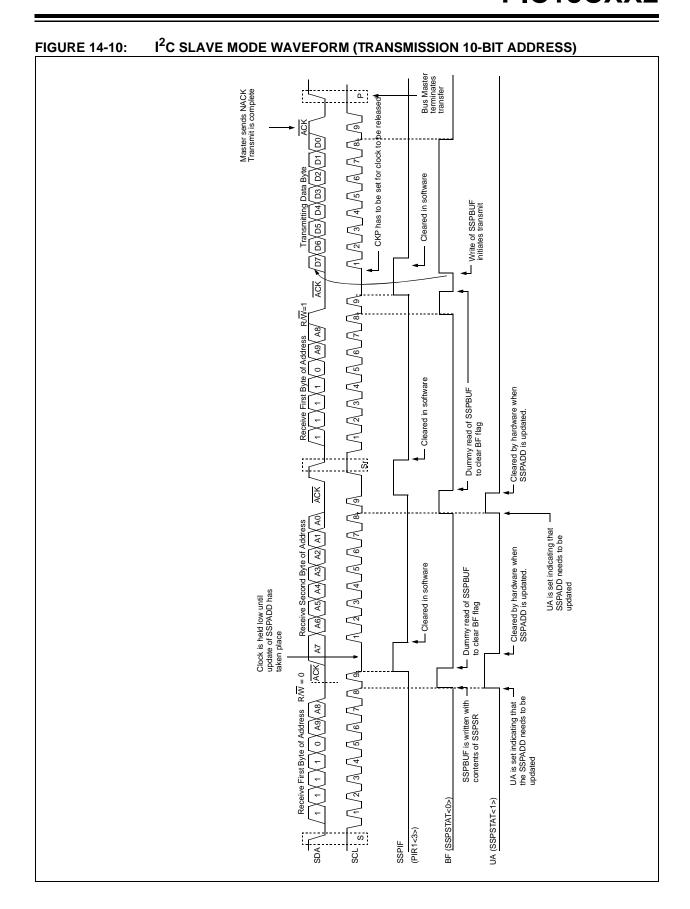
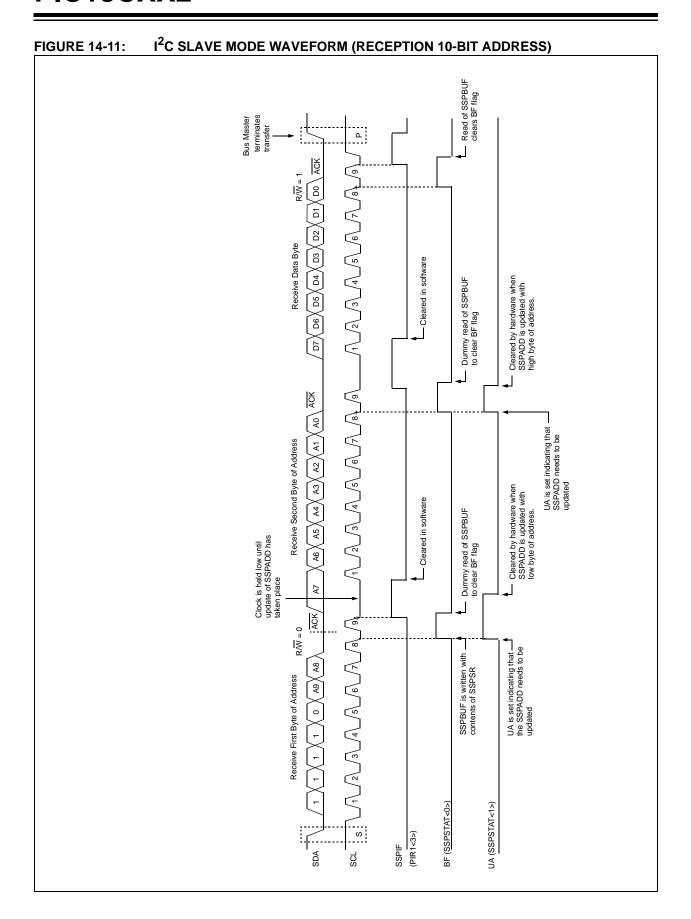


FIGURE 14-9: I²C SLAVE MODE WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)







14.4.2 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I²C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I^2C protocol. It consists of all 0's with R/W = 0.

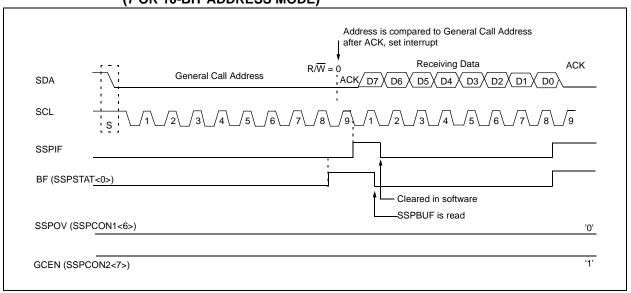
The general call address is recognized when the General Call Enable bit (GCEN) is enabled (SSPCON2<7> is set). Following a START bit detect, 8-bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit), and on the falling edge of the ninth bit (ACK bit), the SSPIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match, and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-bit address mode, then the second half of the address is not necessary, the UA bit will not be set, and the slave will begin receiving data after the Acknowledge (Figure 14-12).

FIGURE 14-12: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE (7 OR 10-BIT ADDRESS MODE)



14.4.3 MASTER MODE

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is idle, with both the S and P bits clear.

In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP interrupt, if enabled):

- · START condition
- STOP condition
- Data transfer byte transmitted/received
- Acknowledge Transmit
- Repeated START

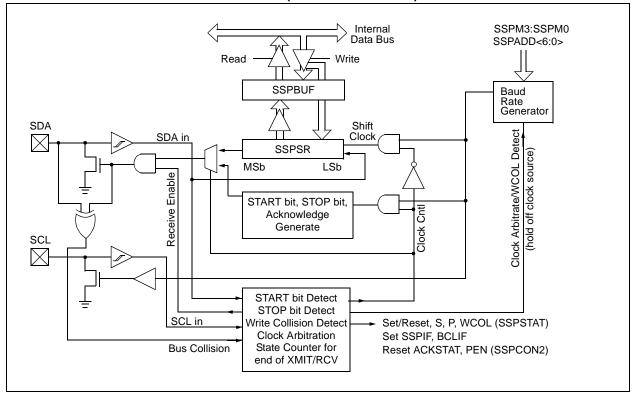
14.4.4 I²C MASTER MODE SUPPORT

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON1 and by setting the SSPEN bit. Once Master mode is enabled, the user has six options.

- Assert a START condition on SDA and SCL.
- Assert a Repeated START condition on SDA and SCL.
- Write to the SSPBUF register initiating transmission of data/address.
- 4. Generate a STOP condition on SDA and SCL.
- 5. Configure the I²C port to receive data.
- 6. Generate an Acknowledge condition at the end of a received byte of data.

Note: The MSSP module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to imitate transmission, before the START condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

FIGURE 14-13: MSSP BLOCK DIAGRAM (I²C MASTER MODE)



14.4.4.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I^2C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. START and STOP conditions indicate the beginning and end of transmission.

The baud rate generator used for the SPI mode operation is now used to set the SCL clock frequency for either 100 kHz, 400 kHz, or 1 MHz I²C operation. The baud rate generator reload value is contained in the lower 7 bits of the SSPADD register. The baud rate generator will automatically begin counting on a write to the SSPBUF. Once the given operation is complete, (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

A typical transmit sequence would go as follows:

- The user generates a START condition by setting the START enable bit, SEN (SSPCON2<0>).
- b) SSPIF is set. The MSSP module will wait the required start time before any other operation takes place.
- c) The user loads the SSPBUF with the address to transmit.
- Address is shifted out the SDA pin until all 8 bits are transmitted.
- e) The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
- The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF hit
- g) The user loads the SSPBUF with eight bits of data.
- b) Data is shifted out the SDA pin until all 8 bits are transmitted.
- The MSSP module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
- j) The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
- k) The user generates a STOP condition by setting the STOP enable bit, PEN (SSPCON2<2>).
- Interrupt is generated once the STOP condition is complete.

14.4.5 BAUD RATE GENERATOR

In I²C Master mode, the reload value for the BRG is located in the lower 7 bits of the SSPADD register (Figure 14-14). When the BRG is loaded with this value, the BRG counts down to 0 and stops until another reload has taken place. The BRG count is dec-

remented twice per instruction cycle (TcY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically. If Clock Arbitration is taking place, for instance, the BRG will be reloaded when the SCL pin is sampled high (Figure 14-15).

FIGURE 14-14: BAUD RATE GENERATOR BLOCK DIAGRAM

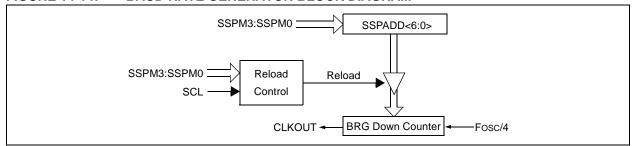
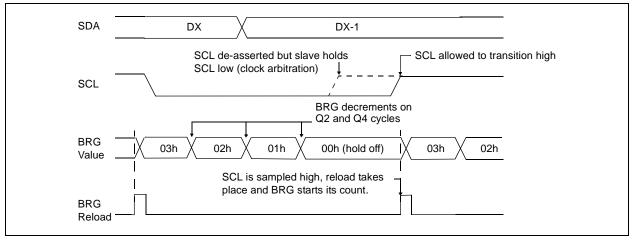


FIGURE 14-15: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



14.4.6 I²C MASTER MODE START CONDITION TIMING

To initiate a START condition, the user sets the START condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the baud rate generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low, while SCL is high, is the START condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the baud rate generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the baud rate generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the baud rate generator is suspended leaving the SDA line held low and the START condition is complete.

Note: If, at the beginning of the START condition, the SDA and SCL pins are already sampled low, or if during the START condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF is set, the START condition is

aborted, and the I²C module is reset into its IDLE state.

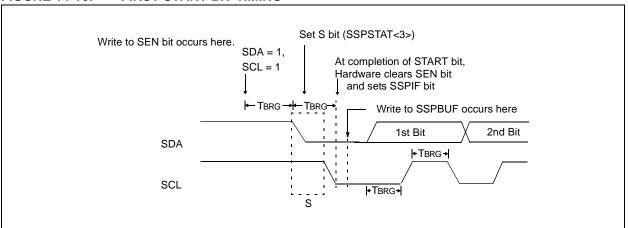
14.4.6.1 WCOL Status Flag

Note:

If the user writes the SSPBUF when a START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the START condition is complete.

FIGURE 14-16: FIRST START BIT TIMING



14.4.7 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the idle state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (T_{BRG}). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG, while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the baud rate generator will not be reloaded, leaving the SDA pin held low. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the baud rate generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

- **2:** A bus collision during the Repeated START condition occurs if:
 - SDA is sampled low when SCL goes from low to high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode), or eight bits of data (7-bit mode).

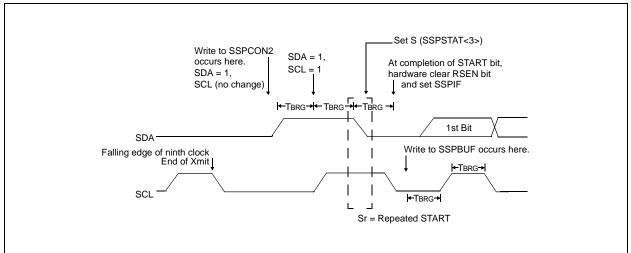
14.4.7.1 WCOL Status Flag

Note:

If the user writes the SSPBUF when a Repeated START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Because queueing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated START condition is complete.

FIGURE 14-17: REPEAT START CONDITION WAVEFORM



14.4.8 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or the other half of a 10-bit address, is accomplished by simply writing a value to the SSPBUF register. This action will set the buffer full flag bit, BF, and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time specification parameter 106). SCL is held low for one baud rate generator rollover count (TBRG). Data should be valid before SCL is released high (see Data setup time specification parameter 107). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. allowing the slave device being addressed to respond with an ACK bit during the ninth bit time, if an address match occurs, or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPIF bit is set and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 14-18).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will de-assert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the baud rate generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

14.4.8.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared, when all 8 bits are shifted out.

14.4.8.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress, (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

14.4.8.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge $(\overline{ACK} = 0)$, and is set when the slave does not Acknowledge $(\overline{ACK} = 1)$. A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

14.4.9 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the receive enable bit, RCEN (SSPCON2<3>).

Note: The MSSP module must be in an IDLE state before the RCEN bit is set, or the RCEN bit will be disregarded.

The baud rate generator begins counting, and on each rollover, the state of the SCL pin changes (high to low/ low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the baud rate generator is suspended from counting, holding SCL low. The MSSP is now in IDLE state, awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception, by setting the Acknowledge sequence enable bit. (SSPCON2<4>).

14.4.9.1 BF Status Flag

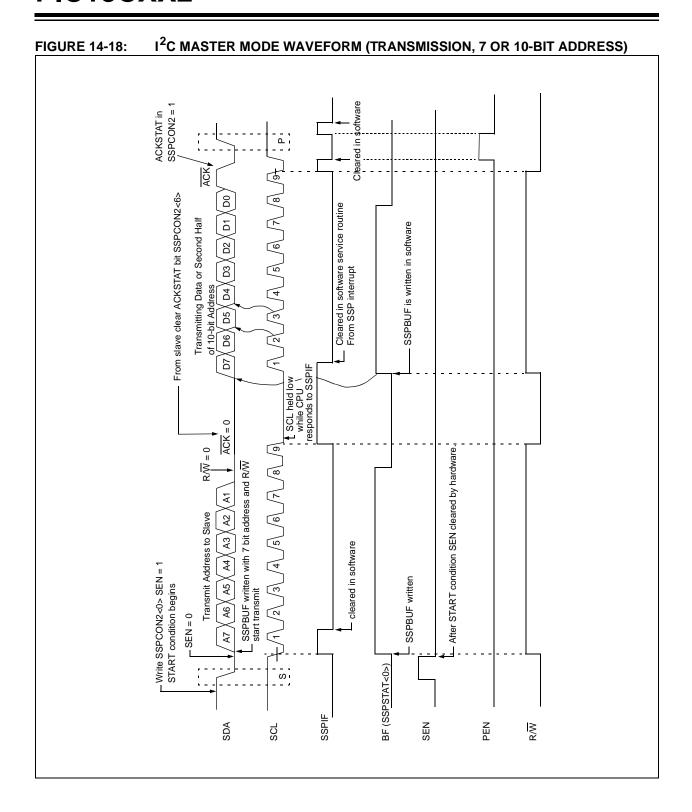
In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

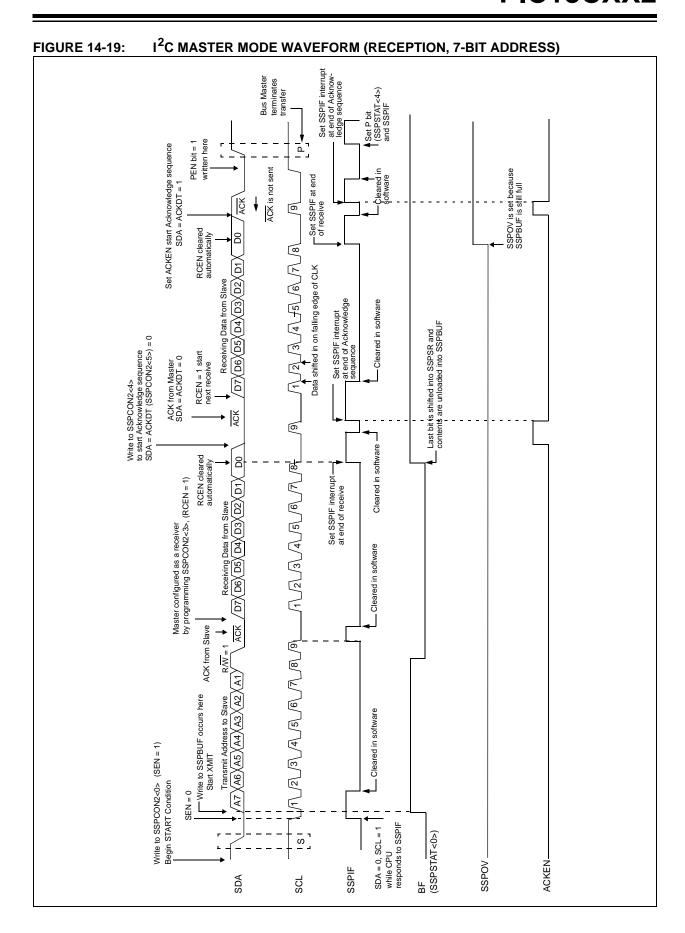
14.4.9.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

14.4.9.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).





14.4.10 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit is presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The baud rate generator then counts for one rollover period (TBRG) and the SCL pin is de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the baud rate generator is turned off and the MSSP module then goes into IDLE mode (Figure 14-20).

14.4.10.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

14.4.11 STOP CONDITION TIMING

A STOP bit is asserted on the SDA pin at the end of a receive/transmit by setting the STOP sequence enable bit, PEN (SSPCON2<2>). At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the baud rate generator is reloaded and counts down to 0. When the baud rate generator times out, the SCL pin will be brought high, and one TBRG (baud rate generator rollover count) later, the SDA pin will be de-asserted. When the SDA pin is sampled high while SCL is high, the P bit (SSPSTAT<4>) is set. A TBRG later, the PEN bit is cleared and the SSPIF bit is set (Figure 14-21).

14.4.11.1 WCOL Status Flag

If the user writes the SSPBUF when a STOP sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).



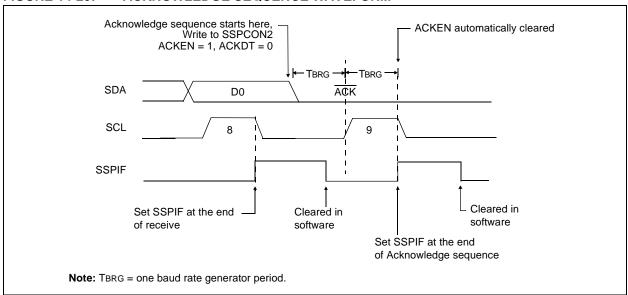
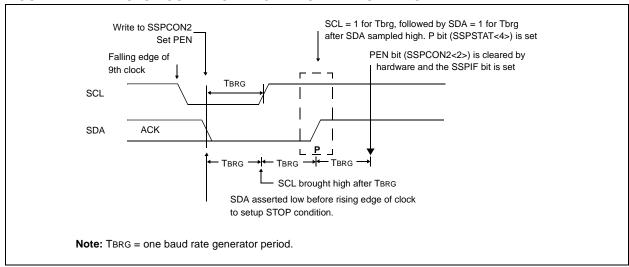


FIGURE 14-21: STOP CONDITION RECEIVE OR TRANSMIT MODE



14.4.12 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit, or Repeated START/STOP condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count, in the event that the clock is held low by an external device (Figure 14-22).

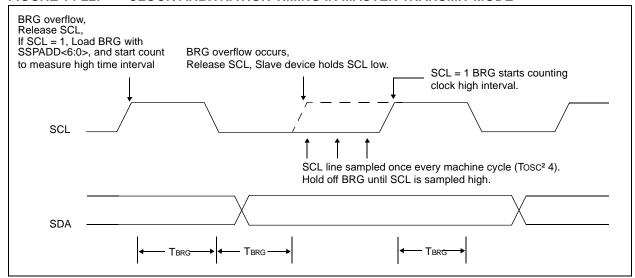
14.4.13 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data, and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the MSSP interrupt is enabled).

14.4.14 EFFECT OF A RESET

A RESET disables the MSSP module and terminates the current transfer.

FIGURE 14-22: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



14.4.15 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET, or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored, for arbitration, to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- · Data Transfer
- · A START Condition
- · A Repeated START Condition
- An Acknowledge Condition

14.4.16 MULTI -MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on

SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I^2C port to its IDLE state (Figure 14-23).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are de-asserted, and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine, and if the I^2C bus is free, the user can resume communication by asserting a START condition.

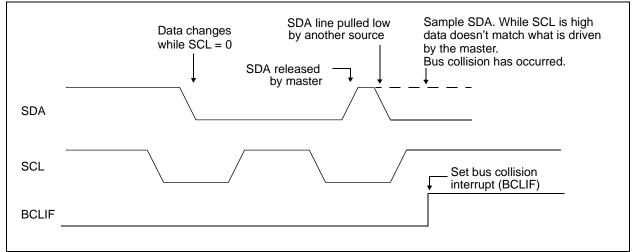
If a START, Repeated START, STOP, or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are de-asserted, and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine, and if the I²C bus is free, the user can resume communication by asserting a START condition.

The master will continue to monitor the SDA and SCL pins. If a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of START and STOP conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is idle and the S and P bits are cleared.

FIGURE 14-23: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



14.4.16.1 Bus Collision During a START Condition

During a START condition, a bus collision occurs if:

- SDA or SCL are sampled low at the beginning of the START condition (Figure 14-24).
- b) SCL is sampled low before SDA is asserted low (Figure 14-25).

During a START condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- · the START condition is aborted,
- · the BCLIF flag is set, and
- the MSSP module is reset to its IDLE state (Figure 14-24).

The START condition begins with the SDA and SCL pins de-asserted. When the SDA pin is sampled high, the baud rate generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the START condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 14-26). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The baud rate generator is then reloaded and counts down to 0, and during this time, if the SCL pins are sampled as '0', a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

the reason that bus collision is not a factor during a START condition, is that no two bus masters can assert a START condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision, because the two masters must be allowed to arbitrate the first address following the START condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated START, or STOP conditions.

FIGURE 14-24: BUS COLLISION DURING START CONDITION (SDA ONLY)

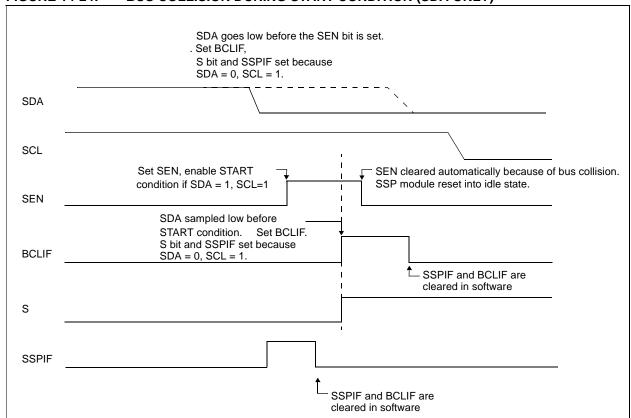


FIGURE 14-25: BUS COLLISION DURING START CONDITION (SCL = 0)

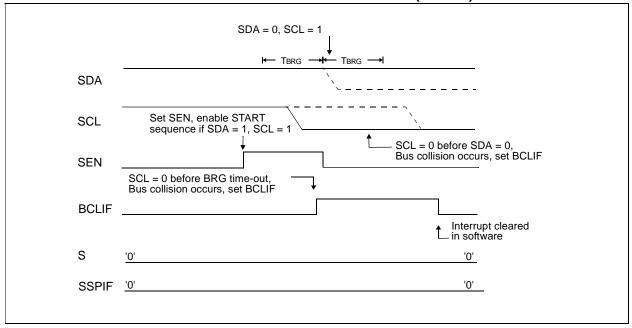
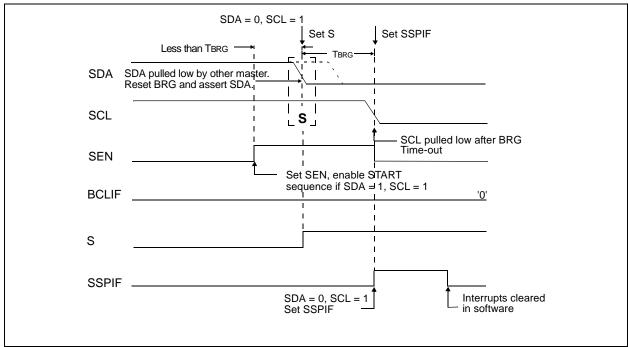


FIGURE 14-26: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



14.4.16.2 Bus Collision During a Repeated START Condition

During a Repeated START condition, a bus collision occurs if:

- A low level is sampled on SDA when SCL goes from low level to high level.
- SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user de-asserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then de-asserted, and when sampled high, the SDA pin is sampled.

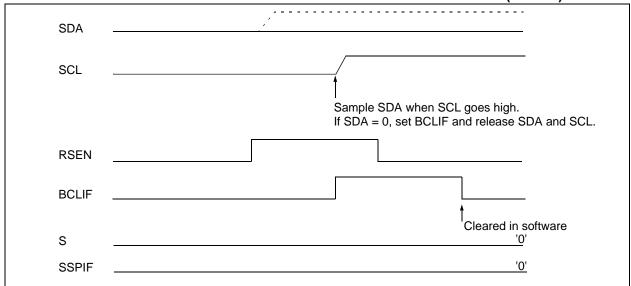
If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 14-27). If SDA is sampled high, the BRG is

reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

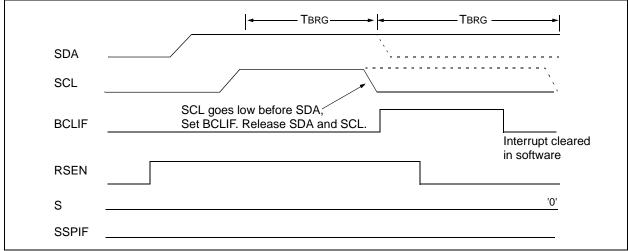
If SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated START condition, Figure 14-28.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated START condition is complete.









14.4.16.3 Bus Collision During a STOP Condition

Bus collision occurs during a STOP condition if:

- After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- b) After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 14-29). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 14-30).

FIGURE 14-29: BUS COLLISION DURING A STOP CONDITION (CASE 1)

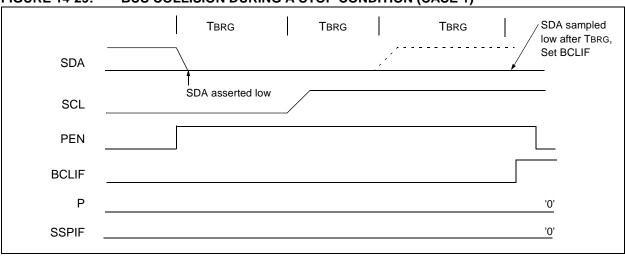
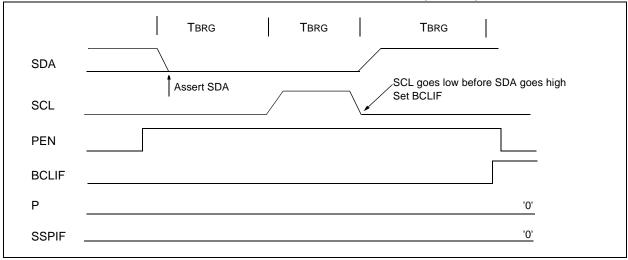


FIGURE 14-30: BUS COLLISION DURING A STOP CONDITION (CASE 2)



15.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI.) The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers, or it can be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

The USART can be configured in the following modes:

- · Asynchronous (full duplex)
- Synchronous Master (half duplex)
- Synchronous Slave (half duplex)

In order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter:

- bit SPEN (RCSTA<7>) must be set (= 1), and
- bits TRISC<7:6> must be cleared (= 0).

Register 15-1 shows the Transmit Status and Control Register (TXSTA) and Register 15-2 shows the Receive Status and Control Register (RCSTA).

REGISTER 15-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D
bit 7							bit 0

bit 7 CSRC: Clock Source Select bit

Asynchronous mode:

Don't care

Synchronous mode:

- 1 = Master mode (clock generated internally from BRG)
- 0 = Slave mode (clock from external source)
- bit 6 TX9: 9-bit Transmit Enable bit
 - 1 = Selects 9-bit transmission
 - 0 = Selects 8-bit transmission
- bit 5 TXEN: Transmit Enable bit
 - 1 = Transmit enabled
 - 0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

- bit 4 SYNC: USART Mode Select bit
 - 1 = Synchronous mode
 - 0 = Asynchronous mode
- bit 3 Unimplemented: Read as '0'
- bit 2 BRGH: High Baud Rate Select bit

Asynchronous mode:

- 1 = High speed
- 0 = Low speed

Synchronous mode:

Unused in this mode

- bit 1 TRMT: Transmit Shift Register Status bit
 - 1 = TSR empty
 - 0 = TSR full
- bit 0 **TX9D:** 9th bit of transmit data. Can be Address/Data bit or a parity bit.

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 15-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

bit 7 SPEN: Serial Port Enable bit

1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)

0 = Serial port disabled

bit 6 **RX9**: 9-bit Receive Enable bit

1 = Selects 9-bit reception

0 = Selects 8-bit reception

bit 5 SREN: Single Receive Enable bit

Asynchronous mode:

Don't care

Synchronous mode - master:

1 = Enables single receive

0 = Disables single receive

This bit is cleared after reception is complete.

Synchronous mode - slave:

Unused in this mode

bit 4 CREN: Continuous Receive Enable bit

Asynchronous mode:

1 = Enables continuous receive

0 = Disables continuous receive

Synchronous mode:

1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)

0 = Disables continuous receive

bit 3 ADDEN: Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):

1 = Enables address detection, enable interrupt and load of the receive buffer when RSR<8> is set

0 = Disables address detection, all bytes are received, and ninth bit can be used as parity bit

bit 2 **FERR**: Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

bit 1 **OERR**: Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)

0 = No overrun error

bit 0 **RX9D:** 9th bit of received data, can be Address/Data bit or a parity bit.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

n = Value at POR reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

15.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 15-1 shows the formula for computation of the baud rate for different USART modes, which only apply in Master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 15-1. From this, the error in baud rate can be determined.

Example 15-1 shows the calculation of the baud rate error for the following conditions:

- Fosc = 16 MHz
- Desired Baud Rate = 9600
- BRGH = 0
- SYNC = 0

It may be advantageous to use the high baud rate (BRGH = 1), even for slower baud clocks. This is because the Fosc/(16(X + 1)) equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

15.1.1 SAMPLING

The data on the RC7/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

EXAMPLE 15-1: CALCULATING BAUD RATE ERROR

Desired Baud Rate	= Fosc / (64 (X + 1))
Solving for X:	
X X X	= ((Fosc / Desired Baud rate) / 64) - 1 = ((16000000 / 9600) / 64) - 1 = [25.042] = 25
Calculated Baud Rate	= 16000000 / (64 (25 + 1)) = 9615
Error	= (Calculated Baud Rate - Desired Baud Rate) Desired Baud Rate = (9615 - 9600) / 9600 = 0.16%

TABLE 15-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	NA

Legend: X = value in SPBRG (0 to 255)

TABLE 15-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
SPBRG	Baud Ra	te Gener	ator Regi	ster					0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

TABLE 15-3: BAUD RATES FOR SYNCHRONOUS MODE

BAUD	Fos	sc = 40 l	ИHz	Fosc = 20 MHz			F	osc = 16	MHz	Fosc = 10 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actua I Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	NA	_	_	NA	_	_	NA	_	_	NA	_	_
1.2	NA	_	_	NA	_	_	NA	_	_	NA	_	_
2.4	NA	_	_	NA	_	_	NA	_	_	NA	_	_
9.6	NA	_	_	NA	_	_	NA	_	_	9.766	+1.73	255
19.2	NA	_	_	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129
76.8	76.92	0	129	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32
96	96.15	0	103	96.15	+0.16	51	95.24	-0.79	41	96.15	+0.16	25
300	303.03	-0.01	32	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7
500	500.00	0	19	500	0	9	500	0	7	500	0	4
HIGH	39.06	_	255	5000	_	0	4000	_	0	2500	_	0
LOW	10000.00		0	19.53		255	15.625		255	9.766		255

BAUD	Fos	c = 7.159	09 MHz	Fosc = 5.0688 MHz			F	osc = 4	MHz	Fosc = 3.579545 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
0.3	NA	_	_	NA	_	_	NA	_		NA	_	_
1.2	NA	_	_									
2.4	NA	_	_	NA	_	_	NA		_	NA	_	_
9.6	9.622	+0.23	185	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92
19.2	19.24	+0.23	92	19.2	0	65	19.231	+0.16	51	19.04	-0.83	46
76.8	77.82	+1.32	22	79.2	+3.13	15	76.923	+0.16	12	74.57	-2.90	11
96	94.20	-1.88	18	97.48	+1.54	12	1000	+4.17	9	99.43	+3.57	8
300	298.3	-0.57	5	316.8	+5.60	3	NA		_	298.3	-0.57	2
500	NA	_	_	NA	_	_	NA		_	NA	_	_
HIGH	1789.8	_	0	1267	_	0	100		0	894.9	_	0
LOW	6.991	_	255	4.950	_	255	3.906		255	3.496	_	255

BAUD	F	osc = 1	MHz	Fosc = 32.768 kHz				
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		
0.3	NA	_	_	0.303	+1.14	26		
1.2	1.202	+0.16	207	1.170	-2.48	6		
2.4	2.404	+0.16	103	NA	_	_		
9.6	9.615	+0.16	25	NA	_	_		
19.2	19.24	+0.16	12	NA	_	_		
76.8	83.34	+8.51	2	NA	_	_		
96	NA	_	_	NA	_	_		
300	NA	_	_	NA	_	_		
500	NA	_	_	NA	_	_		
HIGH	250	_	0	8.192	_	0		
LOW	0.9766		255	0.032		255		

TABLE 15-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD	F	osc = 40	MHz	Fosc = 20 MHz			F	osc = 16	MHz	Fosc = 10 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
0.3	NA	_	_									
1.2	NA	_	_	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129
2.4	2.44	-1.70	255	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64
9.6	9.62	-0.16	64	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15
19.2	18.94	+1.38	32	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7
76.8	78.13	-1.70	7	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1
96	89.29	+7.52	6	104.2	+8.51	2	NA	_	_	NA	_	_
300	312.50	-4.00	1	312.5	+4.17	0	NA	_	_	NA	_	_
500	625.00	-20.00	0	NA	_	_	NA	_	_	NA	_	_
HIGH	2.44	_	255	312.5	_	0	250	_	0	156.3	_	0
LOW	625.00	_	0	1.221	_	255	0.977	_	255	0.6104	_	255

BAUD	Fos	c = 7.159	09 MHz	Fosc = 5.0688 MHz			F	osc = 4 l	MHz	Fosc = 3.579545 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
0.3	NA	_	_	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185
1.2	1.203	+0.23	92	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46
2.4	2.380	-0.83	46	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22
9.6	9.322	-2.90	11	9.9	+3.13	7	NA	_	_	9.322	-2.90	5
19.2	18.64	-2.90	5	19.8	+3.13	3	NA	_	_	18.64	-2.90	2
76.8	NA	_	_	79.2	+3.13	0	NA	_	_	NA	_	_
96	NA	_		NA	_	_	NA	_	_	NA	_	_
300	NA	_	_									
500	NA	_		NA	_	_	NA	_	_	NA	_	_
HIGH	111.9	_	0	79.2	_	0	62.500	_	0	55.93	_	0
LOW	0.437	_	255	0.3094	_	255	3.906	_	255	0.2185	_	255

DALID	F	osc = 1	MHz	Fosc = 32.768 kHz				
BAUD RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		
0.3	0.300	+0.16	51	0.256	-14.67	1		
1.2	1.202	+0.16	12	NA	_	_		
2.4	2.232	-6.99	6	NA	_	_		
9.6	NA	_	_	NA	_	_		
19.2	NA	_	_	NA	_	_		
76.8	NA	_	_	NA	_	_		
96	NA	_	_	NA	_	_		
300	NA	_	_	NA	_	_		
500	NA	_	_	NA	_	_		
HIGH	15.63	_	0	0.512	_	0		
LOW	0.0610	_	255	0.0020	_	255		

TABLE 15-5: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BALID	Fosc = 40 MHz		F	Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
9.6	9.77	-1.70	255	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64
19.2	19.23	-0.16	129	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32
38.4	38.46	-0.16	64	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15
57.6	58.14	-0.93	42	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10
115.2	113.64	+1.38	21	113.63	-1.36	10	111.11	-3.55	8	125	+8.51	4
250	250.00	0	9	250	0	4	250	0	3	NA	_	_
625	625.00	0	3	625	0	1	NA	_	_	625	0	0
1250	1250.00	0	1	1250	0	0	NA	_	_	NA	_	_

BAUD	Fo	sc = 7.10	6MHz	Fosc = 5.068 MHz			Fosc = 4 MHz			Fosc = 3.579545 MHz		
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)									
9.6	9.520	-0.83	46	9.6	0	32	NA	_	_	9.727	+1.32	22
19.2	19.454	+1.32	22	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11
38.4	37.286	-2.90	11	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5
57.6	55.930	-2.90	7	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3
115.2	111.860	-2.90	3	105.6	-8.33	2	19.231	+0.16	12	111.86	-2.90	1
250	NA	_	_	NA	_	_	NA	_	_	223.72	-10.51	0
625	NA	_	_									
1250	NA	_	_									

BAUD	F	osc = 1	MHz	Fos	c = 32.76	68 kHz
RATE (K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
9.6	8.928	-6.99	6	NA	_	_
19.2	20.833	+8.51	2	NA	_	_
38.4	31.25	-18.61	1	NA	_	_
57.6	62.5	+8.51	0	NA	_	_
115.2	NA	_	_	NA	_	_
250	NA	_	_	NA	_	_
625	NA	_	_	NA	_	_
1250	NA	_	_	NA	_	_

15.2 USART Asynchronous Mode

In this mode, the USART uses standard non-return-to-zero (NRZ) format (one START bit, eight or nine data bits and one STOP bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The baud rate generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- · Baud Rate Generator
- Sampling Circuit
- · Asynchronous Transmitter
- · Asynchronous Receiver

15.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 15-1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new

data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TcY), the TXREG register is empty and flag bit TXIF (PIR1<4>) is set. This interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicated the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. Status bit TRMT is a read only bit, which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

- **Note 1:** The TSR register is not mapped in data memory, so it is not available to the user.
 - 2: Flag bit TXIF is set when enable bit TXEN is set.

To set up an asynchronous transmission:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 15.1).
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, set enable bit TXIE.
- If 9-bit transmission is desired, set transmit bit TX9. Can be used as address/data bit.
- Enable the transmission by setting bit TXEN, which will also set bit TXIF.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Load data to the TXREG register (starts transmission).

FIGURE 15-1: USART TRANSMIT BLOCK DIAGRAM

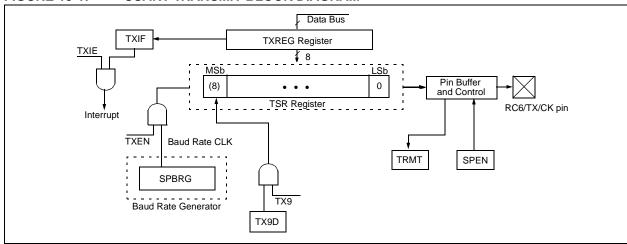


FIGURE 15-2: ASYNCHRONOUS TRANSMISSION

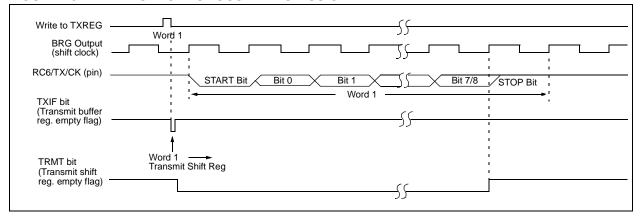


FIGURE 15-3: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)

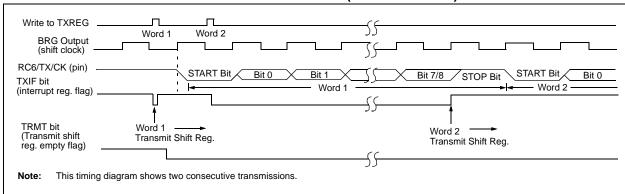


TABLE 15-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART Transmit Register							0000 0000	0000 0000	
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	Generato		0000 0000	0000 0000					

Legend: x = unknown, - = unimplemented locations read as '0'.

Shaded cells are not used for Asynchronous Transmission.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

15.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 15-4. The data is received on the RC7/RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate, or at Fosc. This mode would typically be used in RS-232 systems.

To set up an Asynchronous Reception:

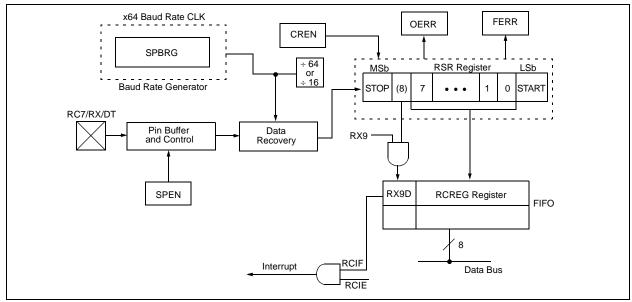
- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 15.1).
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- 3. If interrupts are desired, set enable bit RCIE.
- 4. If 9-bit reception is desired, set bit RX9.
- 5. Enable the reception by setting bit CREN.
- Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing enable bit CREN.

15.2.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is required, set the BRGH bit.
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- 3. If interrupts are required, set the RCEN bit and select the desired priority level with the RCIP bit.
- 4. Set the RX9 bit to enable 9-bit reception.
- 5. Set the ADDEN bit to enable address detect.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF bit will be set when reception is complete. The interrupt will be acknowledged if the RCIE and GIE bits are set.
- 8. Read the RCSTA register to determine if any error occurred during reception, as well as read bit 9 of data (if applicable).
- Read RCREG to determine if the device is being addressed.
- 10. If any error occurred, clear the CREN bit.
- 11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.

FIGURE 15-4: USART RECEIVE BLOCK DIAGRAM





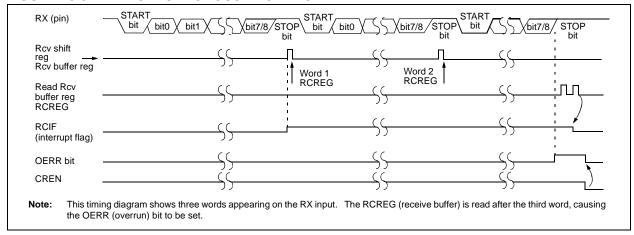


TABLE 15-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INTOIF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
RCREG	USART Re	ceive Re	gister						0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	Generato		0000 0000	0000 0000					

Legend: x = unknown, - = unimplemented locations read as '0'.

Shaded cells are not used for Asynchronous Reception.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

15.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner, (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

15.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 15-1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer register TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and inter-

rupt bit TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE, and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit TRMT (TXSTA<1>) shows the status of the TSR register. TRMT is a read only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 15.1).
- Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

TABLE 15-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART T	USART Transmit Register							0000 0000	0000 0000
TXSTA	CSRC TX9 TXEN SYNC — BRGH TRMT TX9								0000 -010	0000 -010
SPBRG	Baud Rat	e Genera		0000 0000	0000 0000					

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Master Transmission.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

FIGURE 15-6: SYNCHRONOUS TRANSMISSION

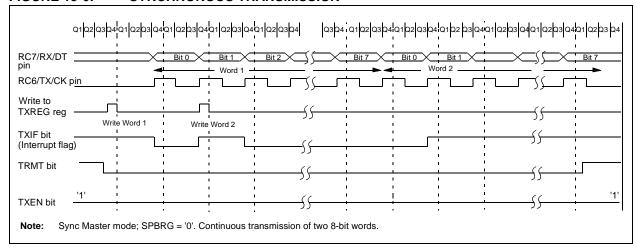
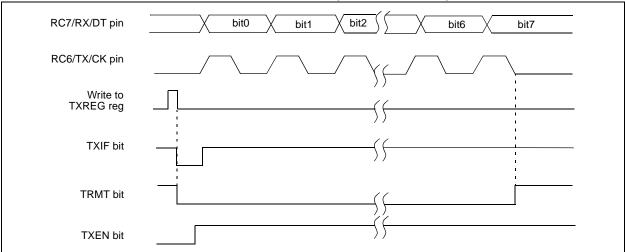


FIGURE 15-7: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



15.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either enable bit SREN (RCSTA<5>), or enable bit CREN (RCSTA<4>). Data is sampled on the RC7/RX/DT pin on the falling edge of the clock. If enable bit SREN is set, only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 15.1).
- Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.

- 3. Ensure bits CREN and SREN are clear.
- 4. If interrupts are desired, set enable bit RCIE.
- 5. If 9-bit reception is desired, set bit RX9.
- 6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
- Interrupt flag bit RCIF will be set when reception is complete and an interrupt will be generated if the enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- If any error occurred, clear the error by clearing bit CREN.

TABLE 15-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

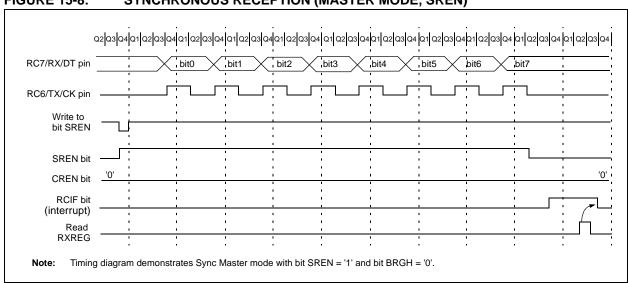
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
RCREG	USART R	USART Receive Register						0000 0000	0000 0000	
TXSTA	CSRC	TX9	TXEN	SYNC	1	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	e Genera	tor Registe		0000 0000	0000 0000				

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Master Reception.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

FIGURE 15-8: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



15.4 USART Synchronous Slave Mode

Synchronous Slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the RC6/TX/CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

15.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- b) The second word will remain in TXREG register.
- c) Flag bit TXIF will not be set.
- d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.
- e) If enable bit TXIE is set, the interrupt will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. Clear bits CREN and SREN.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- Enable the transmission by setting enable bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.

TABLE 15-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x
TXREG	USART T	USART Transmit Register							0000 0000	0000 0000
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRG	Baud Rate	e Genera		0000 0000	0000 0000					

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Slave Transmission.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

15.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register, and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete. An interrupt will be generated if enable bit RCIE was set.
- 6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.

TABLE 15-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu PO BO	R,	Valu all o RES	ther
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000	000x	0000	000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000	0000	0000	0000
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000	-00x	0000	-00x
RCREG	USART R	USART Receive Register							0000	0000	0000	0000
TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000	-010	0000	-010
SPBRG	Baud Rate	Baud Rate Generator Register									0000	0000

Legend: x = unknown, - = unimplemented, read as '0'.

Shaded cells are not used for Synchronous Slave Reception.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

NOTES:

16.0 COMPATIBLE 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has five inputs for the PIC18C2x2 devices and eight for the PIC18C4x2 devices. This module has the ADCON0 and ADCON1 register definitions that are compatible with the mid-range A/D module.

The A/D allows conversion of an analog input signal to a corresponding 10-bit digital number.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 16-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 16-2, configures the functions of the port pins.

REGISTER 16-1: ADCONO REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON
bit 7							bit 0

bit 7-6 ADCS1:ADCS0: A/D Conversion Clock Select bits (ADCON0 bits in bold)

ADCON1 <adcs2></adcs2>	ADCON0 <adcs1:adcs0></adcs1:adcs0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	0.0	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 CHS2:CHS0: Analog Channel Select bits

000 = channel 0 (AN0)

001 = channel 1 (AN1)

010 = channel 2 (AN2)

011 = channel 3 (AN3)

100 = channel 4 (AN4)

101 = channel 5 (AN5)

110 = channel 6 (AN6) 111 = channel 7 (AN7)

Note: The PIC18C2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2 GO/DONE: A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)

0 = A/D conversion not in progress

bit 1 Unimplemented: Read as '0'

bit 0 ADON: A/D On bit

1 = A/D converter module is powered up

0 = A/D converter module is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 16-2: ADCON1 REGISTER

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 ADFM: A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'. 0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 ADCS2: A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <adcs2></adcs2>	ADCON0 <adcs1:adcs0></adcs1:adcs0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 Unimplemented: Read as '0'

bit 3-0 PCFG3:PCFG0: A/D Port Configuration Control bits

PCFG	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	Α	Α	Α	Α	Α	Α	Α	Α	Vdd	Vss	8/0
0001	Α	Α	Α	Α	VREF+	Α	Α	Α	AN3	Vss	7/1
0010	D	D	D	Α	Α	Α	Α	Α	Vdd	Vss	5/0
0011	D	D	D	Α	VREF+	Α	Α	Α	AN3	Vss	4/1
0100	D	D	D	D	Α	D	Α	Α	Vdd	Vss	3/0
0101	D	D	D	D	VREF+	D	Α	Α	AN3	Vss	2/1
011x	D	D	D	D	D	D	D	D	_	_	0/0
1000	Α	Α	Α	Α	VREF+	VREF-	Α	Α	AN3	AN2	6/2
1001	D	D	Α	Α	Α	Α	Α	Α	Vdd	Vss	6/0
1010	D	D	Α	Α	VREF+	Α	Α	Α	AN3	Vss	5/1
1011	D	D	Α	Α	VREF+	VREF-	Α	Α	AN3	AN2	4/2
1100	D	D	D	Α	VREF+	VREF-	Α	Α	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	Α	Α	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	Α	Vdd	Vss	1/0
1111	D	D	D	D	VREF+	VREF-	D	Α	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

- n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: On any device RESET, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss) or the voltage level on the RA3/AN3/ VREF+ pin and RA2/AN2/VREF-.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

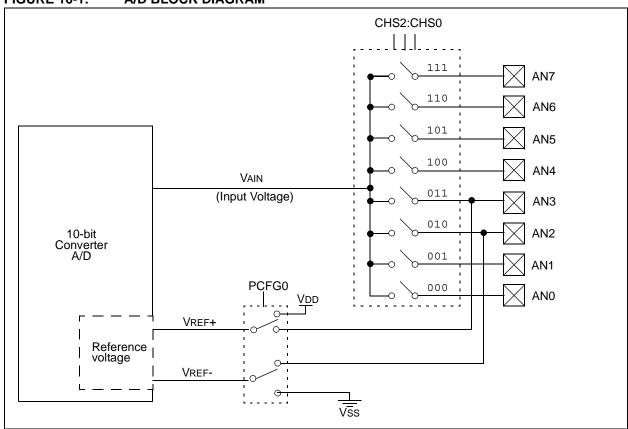
The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off and any conversion is aborted.

Each port pin associated with the A/D converter can be configured as an analog input (RA3 can also be a voltage reference) or as a digital I/O.

The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH/ADRESL registers, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 16-1.

FIGURE 16-1: A/D BLOCK DIAGRAM



The value that is in the ADRESH/ADRESL registers is not modified for a Power-on Reset. The ADRESH/ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 16.1. After this acquisition time has elapsed, the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

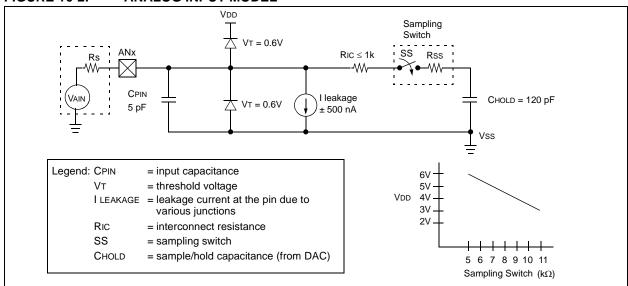
- Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
- 2. Configure A/D interrupt (if desired):
 - · Clear ADIF bit
 - · Set ADIE bit
 - · Set GIE bit
- 3. Wait the required acquisition time.
- 4. Start conversion:
 - Set GO/DONE bit (ADCON0)
- 5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared OR
 - · Waiting for the A/D interrupt
- Read A/D Result registers (ADRESH/ADRESL); clear bit ADIF if required.
- For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

16.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 16-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is $2.5 \ k\Omega$. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

FIGURE 16-2: ANALOG INPUT MODEL



To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 16-1: ACQUISITION TIME

```
TACQ = Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient

= TAMP + TC + TCOFF
```

EQUATION 16-2: A/D MINIMUM CHARGING TIME

Example 16-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following application system assumptions:

 $\begin{array}{lll} \bullet & \mathsf{CHOLD} & = & 120 \ \mathsf{pF} \\ \bullet & \mathsf{Rs} & = & 2.5 \ \mathsf{k}\Omega \\ \bullet & \mathsf{Conversion} \ \mathsf{Error} \leq & 1/2 \ \mathsf{LSb} \\ \bullet & \mathsf{VDD} & = & 5\mathsf{V} \to \mathsf{Rss} = 7 \ \mathsf{k}\Omega \\ \bullet & \mathsf{Temperature} & = & 50 ^{\circ}\mathsf{C} \ \mathsf{(system max.)} \\ \bullet & \mathsf{VHOLD} & = & 0\mathsf{V} \ @ \ \mathsf{time} = 0 \\ \end{array}$

EXAMPLE 16-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

```
Tacq = Tamp + Tc + Tcoff

Temperature coefficient is only required for temperatures > 25°C.

Tacq = 2 \mu s + Tc + [(Temp - 25^{\circ}C)(0.05 \mu s/°C)]

Tc = -Chold (Ric + Rss + Rs) ln(1/2047)
-120 pF (1 kΩ + 7 kΩ + 2.5 kΩ) ln(0.0004885)
-120 pF (10.5 kΩ) ln(0.0004885)
-1.26 \mu s (-7.6241)
9.61 \mu s

Tacq = 2 \mu s + 9.61 \mu s + [(50°C - 25^{\circ}C)(0.05 \mu s/°C)]
11.61 \mu s + 1.25 \mu s
12.86 \mu s
```

16.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. The seven possible options for TAD are:

- 2Tosc
- 4Tosc
- 8Tosc
- 16Tosc
- 32Tosc
- 64Tosc
- · Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μ s.

Table 16-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

16.3 Configuring Analog Port Pins

The ADCON1, TRISA and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

- Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.
 - 2: Analog levels on any pin that is defined as a digital input (including the AN4:AN0 pins) may cause the input buffer to consume current that is out of the devices specification.

TABLE 16-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock	Source (TAD)	Device Frequency								
Operation	ADCS2:ADCS0	40 MHz	20 MHz	5 MHz	1.25 MHz	333.33 kHz				
2Tosc	000	50 ns	100 ns ⁽²⁾	400 ns ⁽²⁾	1.6 μs	6 μs				
4Tosc	100	100 ns	200 ns ⁽²⁾	800 ns ⁽²⁾	3.2 μs	12 μs				
8Tosc	001	200 ns	400 ns ⁽²⁾	1.6 µs	6.4 μs	24 μS ⁽³⁾				
16Tosc	101	400 ns	800 ns ⁽²⁾	3.2 μs	12.8 μs	48 μs ⁽³⁾				
32Tosc	010	800 ns	1.6 µs	6.4 μs	25.6 μs ⁽³⁾	96 μs ⁽³⁾				
64Tosc	110	1.6 µs	3.2 μs	12.8 μs	51.2 μs ⁽³⁾	192 μs ⁽³⁾				
RC	011	2 - 6 μs ⁽¹⁾								

Legend: Shaded cells are outside of recommended range.

- Note 1: The RC source has a typical TAD time of 4 μ s.
 - 2: These values violate the minimum required TAD time.
 - 3: For faster conversion times, the selection of another clock source is recommended.

TABLE 16-2: TAD vs. DEVICE OPERATING FREQUENCIES (FOR EXTENDED, LC, DEVICES)

AD Clock	Source (TAD)	Device Frequency							
Operation ADCS2:ADCS0		4 MHz	2 MHz	1.25 MHz	333.33 kHz				
2Tosc	000	500 ns ⁽²⁾	1.0 μs ⁽²⁾	1.6 μs ⁽²⁾	6 μs				
4Tosc	100	1.0 μs ⁽²⁾	2.0 μs ⁽²⁾	3.2 μs ⁽²⁾	12 μs				
8Tosc	001	2.0 μs ⁽²⁾	4.0 μs	6.4 μs	24 μS ⁽³⁾				
16Tosc	101	4.0 μS ⁽²⁾	8.0 µs	12.8 μs	48 μS ⁽³⁾				
32Tosc	010	8.0 µs	16.0 μs	25.6 μs ⁽³⁾	96 μs ⁽³⁾				
64Tosc 110		16.0 μs	32.0 μs	51.2 μs ⁽³⁾	192 μS ⁽³⁾				
RC	011	3 - 9 μs ^(1,4)							

Legend: Shaded cells are outside of recommended range.

- Note 1: The RC source has a typical TAD time of 6 μs.
 - 2: These values violate the minimum required TAD time.
 - 3: For faster conversion times, the selection of another clock source is recommended.

16.4 A/D Conversions

Figure 16-3 shows the operation of the A/D converter after the GO bit has been set. Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, acquisition on the selected channel is automatically started.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

16.5 Use of the CCP2 Trigger

An A/D conversion can be started by the "special event trigger" of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D conversion and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH/ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

FIGURE 16-3: A/D CONVERSION TAD CYCLES

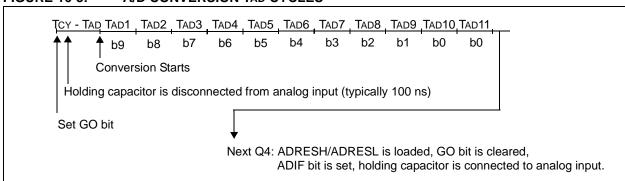


TABLE 16-3: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0000 0000	0000 0000
PIR2	_	_	_	_	BCLIF	LVDIF	TMR3IF	CCP2IF	0000	0000
PIE2	_	_	_	_	BCLIE	LVDIE	TMR3IE	CCP2IE	0000	0000
IPR2	_	_	_	_	BCLIP	LVDIP	TMR3IP	CCP2IP	0000	0000
ADRESH	A/D Result	t Register							xxxx xxxx	uuuu uuuu
ADRESL	A/D Result	t Register							xxxx xxxx	uuuu uuuu
ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/ DONE	_	ADON	0000 00-0	0000 00-0
ADCON1	ADFM	ADCS2	_	_	PCFG3	PCFG2	PCFG1	PCFG0	000	000
PORTA	_	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
TRISA	_	PORTA D	ORTA Data Direction Register						11 1111	11 1111
PORTE	_	_	_	_	_	RE2	RE1	RE0	000	000
LATE	_	_	_	_	_	LATE2	LATE1	LATE0	xxx	uuu
TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Da	ata Direction	n bits	0000 -111	0000 -111

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: The PSPIF, PSPIE and PSPIP bits are reserved on the PIC18C2X2 devices. Always maintain these bits clear.

17.0 LOW VOLTAGE DETECT

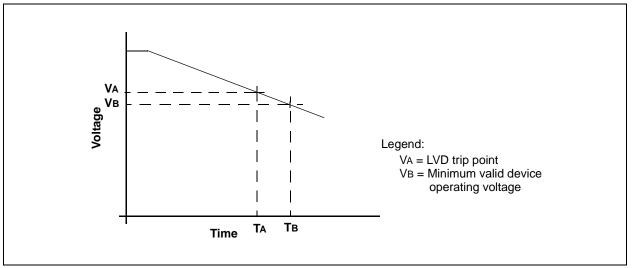
In many applications, the ability to determine if the device voltage (VDD) is below a specified voltage level is a desirable feature. A window of operation for the application can be created, where the application software can do "housekeeping tasks" before the device voltage exits the valid operating range. This can be done using the Low Voltage Detect module.

This module is a software programmable circuitry, where a device voltage trip point can be specified. When the voltage of the device becomes lower then the specified point, an interrupt flag is set. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to that interrupt source.

The Low Voltage Detect circuitry is completely under software control. This allows the circuitry to be "turned off" by the software, which minimizes the current consumption for the device.

Figure 17-1 shows a possible application voltage curve (typically for batteries). Over time, the device voltage decreases. When the device voltage equals voltage VA, the LVD logic generates an interrupt. This occurs at time TA. The application software then has the time, until the device voltage is no longer in valid operating range, to shut-down the system. Voltage point VB is the minimum valid operating voltage specification. This occurs at time TB. The difference TB - TA is the total time for shut-down.



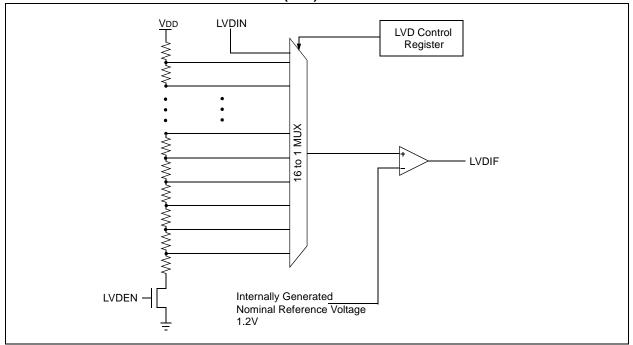


The block diagram for the LVD module is shown in Figure 17-2. A comparator uses an internally generated reference voltage as the set point. When the selected tap output of the device voltage crosses the set point (is lower than), the LVDIF bit is set.

Each node in the resistor divider represents a "trip point" voltage. The "trip point" voltage is the minimum supply voltage level at which the device can operate before the LVD module asserts an interrupt. When the

supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the 1.2V internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal setting the LVDIF bit. This voltage is software programmable to any one of 16 values (see Figure 17-2). The trip point is selected by programming the LVDL3:LVDL0 bits (LVDCON<3:0>).

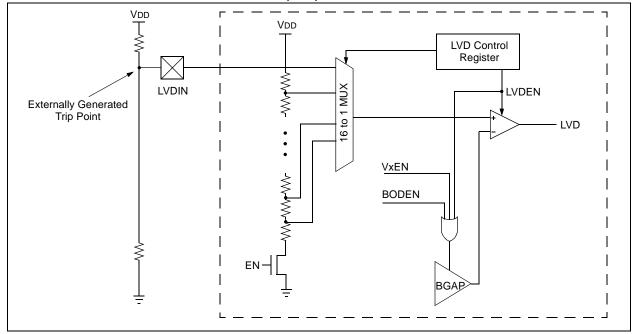
FIGURE 17-2: LOW VOLTAGE DETECT (LVD) BLOCK DIAGRAM



The LVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits LVDL3:LVDL0 are set to 1111. In this state, the comparator input is multiplexed from the external input pin LVDIN (Figure 17-3).

This gives flexibility, because it allows a user to configure the Low Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 17-3: LOW VOLTAGE DETECT (LVD) WITH EXTERNAL INPUT BLOCK DIAGRAM



17.1 Control Register

The Low Voltage Detect Control register controls the operation of the Low Voltage Detect circuitry.

REGISTER 17-1: LVDCON REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
_	_	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0
bit 7							bit 0

bit 7-6 Unimplemented: Read as '0'

bit 5 IRVST: Internal Reference Voltage Stable Flag bit

- 1 = Indicates that the Low Voltage Detect logic will generate the interrupt flag at the specified voltage range
- 0 = Indicates that the Low Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled
- bit 4 LVDEN: Low Voltage Detect Power Enable bit
 - 1 = Enables LVD, powers up LVD circuit
 - 0 = Disables LVD, powers down LVD circuit
- bit 3-0 LVDL3:LVDL0: Low Voltage Detection Limit bits
 - 1111 = External analog input is used (input comes from the LVDIN pin)
 - 1110 = 4.5V min. 4.77V max.
 - 1101 = 4.2V min. 4.45V max.
 - 1100 = 4.0V min. 4.24V max.
 - 1011 = 3.8V min. 4.03V max.
 - 1010 = 3.6V min. 3.82V max.
 - 1001 = 3.5V min. 3.71V max.
 - 1000 = 3.3V min. 3.50V max.
 - 0111 = 3.0V min. 3.18V max.
 - 0110 = 2.8V min. 2.97V max. 0101 = 2.7V min. - 2.86V max.
 - 0100 = 2.5V min. 2.65V max.
 - 0011 = 2.4V min. 2.54V max.
 - 0010 = 2.2V min. 2.33V max.
 - 0001 = 2.0V min. 2.12V max.
 - 0000 = 1.8V min. 1.91V max.

Note: LVDL3:LVDL0 modes which result in a trip point below the valid operating voltage of the device are not tested.

Legend:

R = Readable bit W = Writable bit

U = Unimplemented bit, read as '0' - n = Value at POR reset

17.2 Operation

Depending on the power source for the device voltage, the voltage normally decreases relatively slowly. This means that the LVD module does not need to be constantly operating. To decrease the current requirements, the LVD circuitry only needs to be enabled for short periods, where the voltage is checked. After doing the check, the LVD module may be disabled.

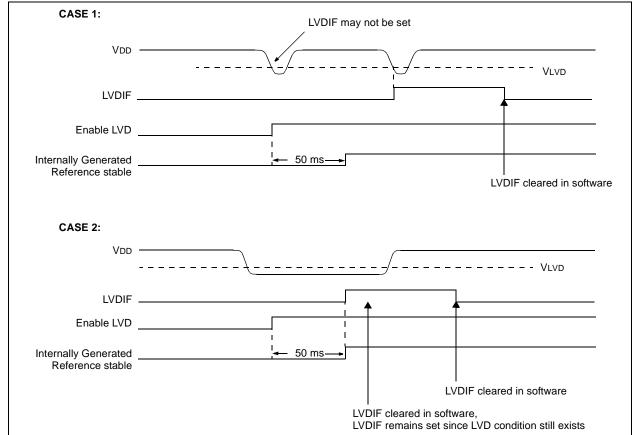
Each time that the LVD module is enabled, the circuitry requires some time to stabilize. After the circuitry has stabilized, all status flags may be cleared. The module will then indicate the proper state of the system.

The following steps are needed to set up the LVD module:

- 1. Write the value to the LVDL3:LVDL0 bits (LVD-CON register), which selects the desired LVD Trip Point.
- 2. Ensure that LVD interrupts are disabled (the LVDIE bit is cleared, or the GIE bit is cleared).
- 3. Enable the LVD module (set the LVDEN bit in the LVDCON register).
- 4. Wait for the LVD module to stabilize (the IRVST bit to become set).
- 5. Clear the LVD interrupt flag, which may have falsely become set until the LVD module has stabilized (clear the LVDIF bit).
- Enable the LVD interrupt (set the LVDIE and the GIE bits).

Figure 17-4 shows typical waveforms that the LVD module may be used to detect.

FIGURE 17-4: LOW VOLTAGE DETECT WAVEFORMS CASE 1:



17.2.1 REFERENCE VOLTAGE SET POINT

The Internal Reference Voltage of the LVD module may be used by other internal circuitry (the Programmable Brown-out Reset). If these circuits are disabled (lower current consumption), the reference voltage circuit requires a time to become stable before a low voltage condition can be reliably detected. This time is invariant of system clock speed. This start-up time is specified in electrical specification parameter #36. The low voltage interrupt flag will not be enabled until a stable reference voltage is reached. Refer to the waveform in Figure 17-4.

17.2.2 CURRENT CONSUMPTION

When the module is enabled, the LVD comparator and voltage divider are enabled and will consume static current. The voltage divider can be tapped from multiple places in the resistor array. Total current consumption, when enabled, is specified in electrical specification parameter #D022B.

17.3 Operation During SLEEP

When enabled, the LVD circuitry continues to operate during SLEEP. If the device voltage crosses the trip point, the LVDIF bit will be set and the device will wake-up from SLEEP. Device execution will continue from the interrupt vector address, if interrupts have been globally enabled.

17.4 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the LVD module to be turned off.

NOTES:

18.0 SPECIAL FEATURES OF THE CPU

There are several features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- OSC Selection
- RESET
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- · Code Protection
- · ID Locations
- · In-circuit Serial Programming

All PIC18CXX2 devices have a Watchdog Timer, which is permanently enabled via the configuration bits or software-controlled. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

18.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location 300000h.

The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h - 3FFFFFh), which can only be accessed using table reads and table writes.

TABLE 18-1: CONFIGURATION BITS AND DEVICE IDS

File	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	CP	CP	CP	CP	CP	CP	CP	CP	1111 1111
300001h	CONFIG1H	_	_	OSCSEN	_	_	FOSC2	FOSC1	FOSC0	111111
300002h	CONFIG2L	_	_	_	_	BORV1	BORV0	BODEN	PWRTEN	1111
300003h	CONFIG2H	_	_	_	_	WDTPS2	WDTPS1	WDTPS0	WDTEN	1111
300005h	CONFIG3H	_	_	_	_	_	_	1	CCP2MX	1
300006h	CONFIG4L	_	1	ı	-	_	_	LVEN	STVREN	11
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	0000 0000
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 0010

Legend: x = unknown, u = unchanged, -= unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'

REGISTER 18-1: CONFIGURATION REGISTER 1 HIGH (CONFIG1H: BYTE ADDRESS 300001h)

R/P-1	R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
Reserved	Reserved	OSCSEN	_	_	FOSC2	FOSC1	FOSC0
bit 7							bit 0

bit 7-6 Reserved: Read as '1'

bit 5 OSCSEN: Oscillator System Clock Switch Enable bit

1 = Oscillator system clock switch option is disabled (main oscillator is source)

0 = Oscillator system clock switch option is enabled (oscillator switching is enabled)

bit 4-3 Unimplemented: Read as '0'

bit 2-0 FOSC2:FOSC0: Oscillator Selection bits

111 = RC oscillator w/OSC2 configured as RA6

110 = HS oscillator with PLL enabled/Clock frequency = (4 x Fosc)

101 = EC oscillator w/OSC2 configured as RA6

100 = EC oscillator w/OSC2 configured as divide-by-4 clock output

011 = RC oscillator 010 = HS oscillator

001 = XT oscillator

000 = LP oscillator

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'

- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 18-2: CONFIGURATION REGISTER 1 LOW (CONFIG1L: BYTE ADDRESS 300000h)

| R/P-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CP | CP | CP | CP | СР | CP | СР | CP |
| hit 7 | | | | | | | hit 0 |

bit 7-0 **CP:** Code Protection bits (apply when in Code Protected Microcontroller mode)

1 = Program memory code protection off

0 = All of program memory code protected

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'

- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 18-3: CONFIGURATION REGISTER 2 HIGH (CONFIG2H: BYTE ADDRESS 300003h)

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
_	_	_	_	WDTPS2	WDTPS1	WDTPS0	WDTEN
bit 7							bit 0

bit 7-4 Unimplemented: Read as '0'

bit 3-1 WDTPS2:WDTPS0: Watchdog Timer Postscale Select bits

111 = 1:1

110 = 1:2

101 = 1:4

100 = 1:8

011 = 1:16

010 = 1:32

001 = 1:64

000 = 1:128

bit 0 WDTEN: Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled (control is placed on the SWDTEN bit)

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 18-4: CONFIGURATION REGISTER 2 LOW (CONFIG2L: BYTE ADDRESS 300002h)

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
_	_	_	_	BORV1	BORV0	BOREN	PWRTEN
bit 7							bit 0

bit 7-4 Unimplemented: Read as '0'

bit 3-2 BORV1:BORV0: Brown-out Reset Voltage bits

11 = VBOR set to 2.5V

10 = VBOR set to 2.7V

01 = VBOR set to 4.2V

00 = VBOR set to 4.5V

bit 1 BOREN: Brown-out Reset Enable bit⁽¹⁾

1 = Brown-out Reset enabled

0 = Brown-out Reset disabled

Note: Enabling Brown-out Reset <u>automatically</u> enables the Power-up Timer (PWRT),

regardless of the value of bit PWRTEN. Ensure the Power-up Timer is enabled any

time Brown-out Reset is enabled.

bit 0 **PWRTEN**: Power-up Timer Enable bit⁽¹⁾

1 = PWRT disabled

0 = PWRT enabled

Note: Enabling Brown-out Reset automatically enables the Power-up Timer (PWRT),

regardless of the value of bit PWRTE. Ensure the Power-up Timer is enabled any

time Brown-out Reset is enabled.

Legend:

 $R = Readable \ bit$ $P = Programmable \ bit$ $U = Unimplemented \ bit, read as '0' - n = Value \ when \ device \ is \ unprogrammed$ $u = Unchanged \ from \ programmed \ state$

REGISTER 18-5: CONFIGURATION REGISTER 3 HIGH (CONFIG3H: BYTE ADDRESS 300005h)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1
_	_	_	_	_	_	_	CCP2MX
bit 7							bit 0

bit 7-1 Unimplemented: Read as '0'

bit 0 CCP2MX: CCP2 Mux bit

1 = CCP2 input/output is multiplexed with RC1 0 = CCP2 input/output is multiplexed with RB3

Legend:

 $R = Readable \ bit$ $P = Programmable \ bit$ $U = Unimplemented \ bit, read as '0'$ $- <math>n = Value \ when \ device \ is \ unprogrammed$ $u = Unchanged \ from \ programmed \ state$

REGISTER 18-6: CONFIGURATION REGISTER 4 LOW (CONFIG4L: BYTE ADDRESS 300006h)

U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
_	_	_	_	_	_	Reserved	STVREN
bit 7							bit 0

bit 7-2 **Unimplemented:** Read as '0' bit 1 **Reserved:** Maintain this bit set

bit 0 STVREN: Stack Full/Underflow Reset Enable bit

1 = Stack Full/Underflow will cause RESET

0 = Stack Full/Underflow will not cause RESET

Legend:

 $R = Readable \ bit$ $P = Programmable \ bit$ $U = Unimplemented \ bit, read as '0' - n = Value \ when \ device \ is \ unprogrammed$ $u = Unchanged \ from \ programmed \ state$

18.2 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKI pin. That means that the WDT will run, even if the clock on the OSC1/CLKI and OSC2/CLKO/RA6 pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The TO bit in the RCON register will be cleared upon a WDT time-out.

The Watchdog Timer is enabled/disabled by a device configuration bit. If the WDT is enabled, software execution may not disable this function. When the WDTEN configuration bit is cleared, the SWDTEN bit enables/ disables the operation of the WDT.

The WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT postscaler may be assigned using the configuration bits.

Note: The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

Note: When a CLRWDT instruction is executed and the postscaler is assigned to the WDT, the postscaler count will be cleared, but the postscaler assignment is not changed.

18.2.1 CONTROL REGISTER

Register 18-7 shows the WDTCON register. This is a readable and writable register, which contains a control bit that allows software to override the WDT enable configuration bit, only when the configuration bit has disabled the WDT.

REGISTER 18-7: WDTCON REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
_	_	_	_	_	_	_	SWDTEN
bit 7							bit 0

bit 7-1 Unimplemented: Read as '0'

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit

- 1 = Watchdog Timer is on
- 0 = Watchdog Timer is turned off if the WDTEN configuration bit in the configuration register = '0'

Legend:

R = Readable bit W = Writable bit

U = Unimplemented bit, read as '0' - n = Value at POR Reset

18.2.2 WDT POSTSCALER

The WDT has a postscaler that can extend the WDT Reset period. The postscaler is selected at the time of device programming, by the value written to the CONFIG2H configuration register.

FIGURE 18-1: WATCHDOG TIMER BLOCK DIAGRAM

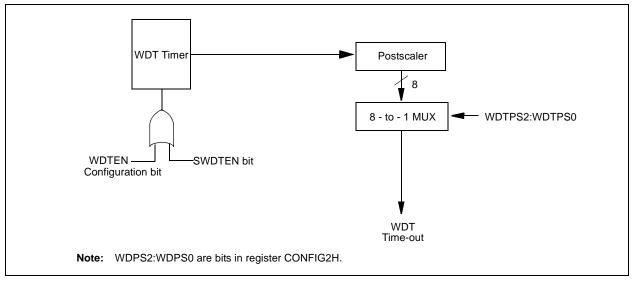


TABLE 18-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG2H	_	_	_	_	WDTPS2	WDTPS2	WDTPS0	WDTEN
RCON	IPEN	LWRT	_	RI	TO	PD	POR	BOR
WDTCON	_	-	_	_	_	_	_	SWDTEN

Legend: Shaded cells are not used by the Watchdog Timer.

18.3 Power-down Mode (SLEEP)

Power-down mode is entered by executing a ${\tt SLEEP}$ instruction.

If enabled, the Watchdog Timer will be cleared, but keeps running, the \overline{PD} bit (RCON<3>) is cleared, the \overline{TO} (RCON<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or Vss, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

18.3.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. External RESET input on $\overline{\text{MCLR}}$ pin.
- Watchdog Timer Wake-up (if WDT was enabled).
- Interrupt from INT pin, RB port change, or a Peripheral Interrupt.

The following peripheral interrupts can wake the device from SLEEP:

- 1. PSP read or write.
- TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 3. TMR3 interrupt. Timer3 must be operating as an asynchronous counter.
- 4. CCP capture mode interrupt.
- Special event trigger (Timer1 in Asynchronous mode using an external clock).
- 6. MSSP (START/STOP) bit detect interrupt.
- 7. MSSP transmit or receive in Slave mode (SPI/I²C).
- 8. USART RX or TX (Synchronous Slave mode).
- 9. A/D conversion (when A/D clock source is RC).

Other peripherals cannot generate interrupts, since during SLEEP, no on-chip clocks are present.

External MCLR Reset will cause a device RESET. All other events are considered a continuation of program execution and will cause a "wake-up". The TO and PD bits in the RCON register can be used to determine the cause of the device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. The TO bit is cleared, if a WDT time-out occurred (and caused wake-up).

When the SLEEP instruction is being executed, the next instruction (PC + 2) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

18.3.2 WAKE-UP USING INTERRUPTS

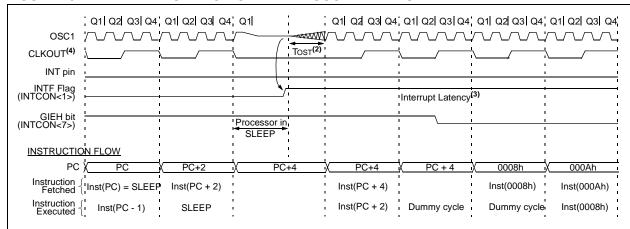
When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If an interrupt condition (interrupt flag bit and interrupt enable bits are set) occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt condition occurs during or after
 the execution of a SLEEP instruction, the device
 will immediately wake up from SLEEP. The SLEEP
 instruction will be completely executed before the
 wake-up. Therefore, the WDT and WDT
 postscaler will be cleared, the TO bit will be set
 and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

FIGURE 18-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT^(1,2)



Note 1: XT, HS or LP oscillator mode assumed.

- 2: GIE = '1' assumed. In this case, after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
- 3: Tost = 1024Tosc (drawing not to scale) This delay will not occur for RC and EC osc modes.
- 4: CLKOUT is not available in these osc modes, but shown here for timing reference.

18.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip Technology does not recommend code protecting windowed devices.

18.5 ID Locations

Five memory locations (200000h - 200004h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are accessible during normal execution through the TBLRD instruction or during program/verify. The ID locations can be read when the device is code protected.

18.6 In-Circuit Serial Programming

PIC18CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

19.0 INSTRUCTION SET SUMMARY

The PIC18CXXX instruction set adds many enhancements to the previous PIC instruction sets, while maintaining an easy migration from these PIC MCU instruction sets.

Most instructions are a single program memory word (16-bits), but there are three instructions that require two program memory locations.

Each single word instruction is a 16-bit word divided into an OPCODE, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- Byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- · Control operations

The PIC18CXXX instruction set summary in Table 19-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 19-1 shows the opcode field descriptions.

Most byte-oriented instructions have three operands:

- 1. The file register (specified by 'f')
- 2. The destination of the result (specified by 'd')
- 3. The accessed memory (specified by 'a')

The file register designator 'f' specifies which file register is to be used by the instruction.

The destination designator 'd' specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

- 1. The file register (specified by 'f')
- The bit in the file register (specified by 'b')
- 3. The accessed memory (specified by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator 'f' represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by 'k')
- The desired FSR register to load the literal value into (specified by 'f')
- No operand required (specified by '--')

The **control** instructions may use some of the following operands:

- A program memory address (specified by 'n')
- The mode of the Call or Return instructions (specified by 's')
- The mode of the Table Read and Table Write instructions (specified by 'm')
- No operand required (specified by '—')

All instructions are a single word, except for three double word instructions. These three instructions were made double word instructions so that all the required information is available in these 32-bits. In the second word, the 4 MSb's are 1's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP.

The double word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s. Two word branch instructions (if true) would take 3 μ s.

Figure 19-1 shows the general formats that the instructions can have.

All examples use the format `nnh' to represent a hexadecimal number, where `h' signifies a hexadecimal digit.

The Instruction Set Summary, shown in Table 19-2, lists the instructions recognized by the Microchip assembler (MPASMTM).

Section 19.1 provides a description of each instruction.

TABLE 19-1: OPCODE FIELD DESCRIPTIONS

a	
	RAM access bit
	a = 0: RAM location in Access RAM (BSR register is ignored)
	a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7)
BSR	Bank Select Register. Used to select the current RAM bank.
d	Destination select bit;
	d = 0: store result in WREG,
_	d = 1: store result in file register f.
dest	Destination either the WREG register or the specified register file location
f	8-bit Register file address (0x00 to 0xFF)
fs	12-bit Register file address (0x000 to 0xFFF). This is the source address.
fd	12-bit Register file address (0x000 to 0xFFF). This is the destination address.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value)
label	Label name
mm	The mode of the TBLPTR register for the Table Read and Table Write instructions
	Only used with Table Read and Table Write instructions:
*	No Change to register (such as TBLPTR with Table reads and writes)
*+	Post-Increment register (such as TBLPTR with Table reads and writes)
* -	Post-Decrement register (such as TBLPTR with Table reads and writes)
+*	Pre-Increment register (such as TBLPTR with Table reads and writes)
n	The relative address (2's complement number) for relative branch instructions, or the direct address for Call/Branch and Return instructions
PRODH	Product of Multiply high byte
PRODL	Product of Multiply low byte
s	Fast Call/Return mode select bit.
	s = 0: do not update into/from shadow registers
	s = 1: certain registers loaded into/from shadow registers (Fast mode)
u	Unused or Unchanged
WREG	Working register (accumulator)
х	Don't care (0 or 1)
	The assembler will generate code with $x = 0$. It is the recommended form of use for compatibility with all
	Microchip software tools.
TBLPTR	21-bit Table Pointer (points to a Program Memory location)
TABLAT	8-bit Table Latch
TOS	Top-of-Stack
PC	Program Counter
PCL	Program Counter Low Byte
PCH	Program Counter High Byte
PCLATH	Program Counter High Byte Latch
PCLATU	Program Counter Upper Byte Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer
TO	Time-out bit
PD	Power-down bit
C, DC, Z, OV, N	ALU status bits Carry, Digit Carry, Zero, Overflow, Negative
[]	Optional
()	Contents
\rightarrow	Assigned to
	Register bit field
< > E	Register bit field In the set of

FIGURE 19-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations **Example Instruction** 10 9 8 7 ADDWF MYREG, W, B OPCODE d a f (FILE #) d = 0 for result destination to be WREG register d = 1 for result destination to be file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address Byte to Byte move operations (2-word) 12 11 OPCODE f (Source FILE #) MOVFF MYREG1, MYREG2 15 12 11 0 f (Destination FILE #) 1111 f = 12-bit file register address Bit-oriented file register operations 12 11 9 8 7 BSF MYREG, bit, B OPCODE b (BIT #) f (FILE #) b = 3-bit position of bit in file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address Literal operations 15 OPCODE k (literal) MOVLW 0x7F k = 8-bit immediate value **Control** operations CALL, GOTO and Branch operations 15 0 OPCODE **GOTO Label** n<7:0> (literal) 12 11 0 15 1111 n<19:8> (literal) n = 20-bit immediate value 15 **CALL MYFUNC OPCODE** n<7:0> (literal) 15 0 12 11 n<19:8> (literal) S = Fast bit 15 11 10 0 **BRA MYFUNC** OPCODE n<10:0> (literal) 8 7 0 OPCODE **BC MYFUNC** n<7:0> (literal)

TABLE 19-2: PIC18CXXX INSTRUCTION SET

Mnemo	onic,	Decerintian	Cycles	16-k	oit Instr	uction V	Vord	Status	Notes
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
BYTE-ORII	ENTED F	FILE REGISTER OPERATIONS							
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1,2
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2
CPFSEQ	f, a	Compare f with WREG, skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4
CPFSGT	f, a	Compare f with WREG, skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4
CPFSLT	f, a	Compare f with WREG, skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2
DECF	f, d, a	Decrement f	1 `	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2
INCF	f, d, a	Increment f	1 `	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1 ` ′	0001	00da	ffff	ffff	Z, N	1, 2
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z. N	1
MOVFF	f _s , f _d	Move f _s (source) to 1st word	2		ffff	ffff	ffff		
	-5, -u	f _d (destination)2nd word	_		ffff	ffff	ffff		
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N	1, 2
RLCF	f, d, a	Rotate Left f through Carry	1	0011		ffff		C, Z, N	., –
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff		Z, N	1, 2
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	C, Z, N	., _
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff		
SETF	f, a, a	Set f	<u> </u>	0110	100a	ffff	ffff	None	
SUBFWB	f, d, a	Subtract f from WREG with	<u> </u>		01da	ffff	ffff	C, DC, Z, OV, N	1, 2
COBI WE	1, u, u	borrow	'	0101	olda			0, 50, 2, 00, 10	1, 2
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	
SUBWFB	f, d, a	Subtract WREG from f with	1		10da	ffff	ffff	C, DC, Z, OV, N	1, 2
OODWI B	1, u, u	borrow	•	0101	Ioda	TTTT	TTTT	0, 50, 2, 00, 10	1, 2
SWAPF	f, d, a	Swap nibbles in f	1	0011	10da	ffff	ffff	None	4
TSTFSZ	f, a, a	Test f, skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1		10da	ffff		Z, N	1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS		Ţ	0001	IUua	TTTT	TTTT	Z, IV		
		1	1001	1-1-1-	5555	5555	None	1.2	
	f, b, a		1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	· ·		bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011		ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, d, a	Bit Toggle f	1	0111	bbba	ffff	ffff	ivone	1, 2

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

^{2:} If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

^{3:} If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

^{4:} Some instructions are 2 word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.

^{5:} If the table write starts the write cycle to internal memory, the write will continue until terminated.

TABLE 19-2: PIC18CXXX INSTRUCTION SET (CONTINUED)

Mnemo	nic,	Decembries	Cycles	16-k	oit Instr	uction V	Vord	Status	Natas
Opera	nds	Description	Cycles	MSb			LSb	Affected	Notes
CONTROL	OPERA	TIONS							
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	2	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	1 (2)	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call subroutine1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT	_	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	_	Decimal Adjust WREG	1	0000	0000	0000	0111	С	
GOTO	n	Go to address1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP	_	No Operation	1	0000	0000	0000	0000	None	
NOP	_	No Operation (Note 4)	1	1111	xxxx	xxxx	xxxx	None	
POP	_	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	_	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software device RESET	1	0000	0000	1111	1111	All	
RETFIE	S	Return from interrupt enable	2	0000	0000	0001	000s	GIE/GIEH,	
								PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	S	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	_	Go into standby mode	1	0000	0000	0000	0011	TO, PD	

- Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
 - 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.
 - **3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
 - **4:** Some instructions are 2 word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.
 - 5: If the table write starts the write cycle to internal memory, the write will continue until terminated.

TABLE 19-2: PIC18CXXX INSTRUCTION SET (CONTINUED)

Mnen	nonic,	Description	Cycles	16-	bit Inst	ruction \	Word	Status	Notes
Oper	ands	Description	Cycles	MSb			LSb	Affected	Notes
LITERAL	OPERATI	ONS							
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move literal (12-bit) 2nd word	2	1110	1110	OOff	kkkk	None	
		to FSRx 1st word		1111	0000	kkkk	kkkk		
MOVLB	k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW	k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA ME	MORY ↔	PROGRAM MEMORY OPERATI	ONS						
TBLRD*		Table Read	2	0000	0000	0000	1000	None	
TBLRD*+		Table Read with post-increment		0000	0000	0000	1001	None	
TBLRD*-		Table Read with post-decrement		0000	0000	0000	1010	None	
TBLRD+*		Table Read with pre-increment		0000	0000	0000	1011	None	
TBLWT*		Table Write	2 (5)	0000	0000	0000	1100	None	
TBLWT*+	•	Table Write with post-increment		0000	0000	0000	1101	None	
TBLWT*-		Table Write with post-decrement		0000	0000	0000	1110	None	
TBLWT+*	•	Table Write with pre-increment		0000	0000	0000	1111	None	

- Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
 - 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.
 - 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
 - **4:** Some instructions are 2 word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.
 - 5: If the table write starts the write cycle to internal memory, the write will continue until terminated.

19.1 Instruction Set

ADDLW ADD literal to WREG

Syntax: [label] ADDLW k

Operands: $0 \le k \le 255$ Operation: (WREG) + $k \to WREG$

Status Affected: N,OV, C, DC, Z

Encoding: 0000 1111 kkkk kkkk

Description: The contents of WREG are added

to the 8-bit literal 'k' and the result is

placed in WREG.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	WREG

Example: ADDLW 0x15

Before Instruction

WREG = 0x10

After Instruction

WREG = 0x25

ADDWF ADD WREG to f Syntax: [label] ADDWF f [,d [,a] f [,d [,a] Operands: $0 \leq f \leq 255$ $d \in [0,1]$ $a \in \left[0,1\right]$ Operation: (WREG) + (f) \rightarrow dest Status Affected: N,OV, C, DC, Z Encoding: 0010 01da ffff ffff Description: Add WREG to register 'f'. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR is used. Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: ADDWF REG, 0, 0

Before Instruction

WREG = 0x17 REG = 0xC2

After Instruction

WREG = 0xD9 REG = 0xC2

ADDWFC ADD WREG and Carry bit to f

Syntax: [label] ADDWFC f [,d [,a]

Operands: $0 \le f \le 255$

 $\begin{array}{l} d \in [0,1] \\ a \in [0,1] \end{array}$

Operation: $(WREG) + (f) + (C) \rightarrow dest$

Status Affected: N,OV, C, DC, Z

Encoding: 0010 00da ffff ffff

Description: Add WREG, the Carry Flag and data

memory location 'f'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed in data memory location 'f'. If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the

BSR will not be overridden.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process Write	Write to
	register 'f'	Data	destination

Example: ADDWFC REG, 0, 1

Before Instruction

Carry bit= 1 REG = 0×02 WREG = $0 \times 4D$

After Instruction

Carry bit= 0REG = 0×02 WREG = 0×50 ANDLW AND literal with WREG

Syntax: [label] ANDLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .AND. $k \rightarrow WREG$

Status Affected: N,Z

Encoding: 0000 1011 kkkk kkkk

Description: The contents of WREG are ANDed with the 8-bit literal 'k'. The result is

placed in WREG.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to
	'k'	Data	WREG

Example: ANDLW 0x5F

Before Instruction

WREG = 0xA3

After Instruction

WREG = 0x03

ANDWF AND WREG with f

Syntax: [label] ANDWF f [,d [,a]

Operands: $0 \le f \le 255$

 $d\in [0,1] \\ a\in [0,1]$

Operation: (WREG) .AND. (f) \rightarrow dest

Status Affected: N,Z

Encoding: 0001

Description: The contents of WREG are AND'ed

with register 'f'. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden

ffff

ffff

01da

(default).

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: ANDWF REG, 0, 0

Before Instruction

WREG = 0x17 REG = 0xC2

After Instruction

WREG = 0x02 REG = 0xC2

BC Branch if Carry

Syntax: [label] BC n Operands: $-128 \le n \le 127$ Operation: if carry bit is '1'

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0010 nnnn nnnn

Description: If the Carry bit is '1', then the pro-

gram will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BC 5

Before Instruction

PC = address (HERE)

After Instruction

If Carry = 1;
 PC = address (HERE+12)

If Carry = 0;

PC = address (HERE+2)

BCF Bit Clear f Syntax: [label] BCF f,b[,a] Operands: $0 \leq f \leq 255$ $0 \le b \le 7$ $a \in [0,1]$ Operation: $0 \rightarrow f < b >$ Status Affected: None Encoding: 1001 bbba ffff ffff Description: Bit 'b' in register 'f' is cleared. If 'a'

is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value

(default).

Words: 1 Cycles: 1

Q Cycle Activity:

 Q1
 Q2
 Q3
 Q4

 Decode
 Read register 'f'
 Process P

Example: BCF FLAG_REG, 7, 0

Before Instruction

FLAG_REG = 0xC7

After Instruction

FLAG REG = 0x47

BN Branch if Negative

Syntax: [label] BN n Operands: $-128 \le n \le 127$ Operation: if negative bit is '1' $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0110 nnnn nnnn

Description: If the Negative bit is '1', then the

program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1 Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BN Jump

Before Instruction

PC = address (HERE)

After Instruction

If Negative = 1;
 PC = address (Jump)

If Negative = 0;
 PC = address (HERE+2)

BNC Branch if Not Carry

Syntax: [label] BNC n

Operands: $-128 \le n \le 127$ Operation: if carry bit is '0'

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0011 nnnn nnnn

Description: If the Carry bit is '0', then the pro-

gram will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process Data	Write to PC
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BNC Jump

Before Instruction

PC = address (HERE)

After Instruction

If Carry = 0;

PC = address (Jump)

If Carry = 1;

PC = address (HERE+2)

BNN Branch if Not Negative

Syntax: [label] BNN n Operands: $-128 \le n \le 127$ Operation: if negative bit is '0'

Status Affected: None

Encoding: 1110 0111 nnnn nnnn

 $(PC) + 2 + 2n \rightarrow PC$

Description: If the Negative bit is '0', then the

program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BNN Jump

Before Instruction

PC = address (HERE)

After Instruction

If Negative= 0;
 PC = address (Jump)

If Negative = 1;
 PC = address (HERE+2)

BNOV	Branch i	f Not Ov	erflow	
Syntax:	[label] E	BNOV	n	
Operands:	$-128 \le n \le 127$			
Operation:	if overflow bit is '0' (PC) + 2 + 2n \rightarrow PC			
Status Affected:	None			
Encoding:	1110	0101	nnnn	nnnn
Description:	If the Ove	will bran	ch.	

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process Data	Write to PC
No operation	No operation	No operation	No operation
oporation	oporation	oporation	oporation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BNOV Jump

Before Instruction

PC = address (HERE)

After Instruction

If Overflow = 0;
 PC = address (Jump)
If Overflow = 1;
 PC = address (HERE+2)

BNZ Branch if Not Zero

Syntax: [label] BNZ n Operands: $-128 \le n \le 127$ Operation: if zero bit is '0'

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0001 nnnn nnnn

Description: If the Zero bit is '0', then the pro-

gram will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1
Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BNZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If Zero = 0;

PC = address (Jump)

If Zero = 1;

PC = address (HERE+2)

BRA Unconditional Branch

Syntax: [label] BRA n Operands: $-1024 \le n \le 1023$

Operation: $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1101 0nnn nnnn nnnn

Description: Add the 2's complement number '2n' to the PC. Since the PC will

have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is a two-

cycle instruction.

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

Example: HERE BRA Jump

Before Instruction

PC = address (HERE)

After Instruction

PC = address (Jump)

BSF Bit Set f

Syntax: [label] BSF f,b[,a]

Operands: $0 \le f \le 255$

 $0 \le b \le 7$ $a \in [0,1]$

Operation: $1 \rightarrow f < b >$

Status Affected: None

Encoding: 1000 bbba fffff ffff

Description: Bit 'b' in register 'f' is set. If 'a' is 0

Access Bank will be selected, overriding the BSR value. If 'a' = 1, then

the bank will be selected as per the

BSR value.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: BSF FLAG_REG, 7, 1

Before Instruction

FLAG REG= 0x0A

After Instruction

FLAG_REG= 0x8A

BTFSC		Bit Test Fi	le, Skip if Cle	ear	BTF	ss	Bit Test Fi	le, Skip if Se	t
Syntax:		[<i>label</i>] B1	TFSC f,b[,a]		Synt	ax:	[label] B1	FSS f,b[,a]	
Operands:		$0 \le f \le 255$			Ope	ands:	$0 \leq f \leq 255$		
		$0 \le b \le 7$					$0 \le b < 7$		
a ∈ [0,1]		•		a ∈ [0,1]					
•	Operation: $skip if (f < b >) = 0$		•	ation:	skip if (f <b< td=""><td>») = 1</td><td></td></b<>	») = 1			
Status Affecte	ed:	None		1		is Affected:	None	1	1
Encoding:		1011	bbba ff	ff ffff	Enco	oding:	1010	bbba ffi	ff ffff
Description:			egister 'f' is 0		Desc	ription:		egister 'f' is 1 t	hen the next
			ction is skippe), then the ne				instruction	ıs skippea. , then the nex	vt instruction
			ring the curre					ing the curre	
		execution i	s discarded, a	and a NOP is			tion execut	ion, is discard	ded and a
			nstead, makin					cuted instead instruction. I	
		•	uction. If 'a' is nk will be sele				•	nk will be sele	•
			SSR value. If					SR value. If '	
			ill be selected	as per the				ill be selected	as per the
Words:		BSR value 1	(default).		Word	de:	BSR value	(default).	
						-			
Cycles:		1(2) Note: 3 cv	cles if skip ar	nd followed	Cycl	es:	1(2) Note: 3 o	cycles if skip a	and followed
			2-word instru					a 2-word inst	
Q Cycle Acti	vity:				QC	ycle Activity:			
Q1		Q2	Q3	Q4		Q1	Q2	Q3	Q4
Decod	-	Read	Process Data	No		Decode	Read	Process Data	No
If skip:		register 'f'		operation	lf sk	in:	register 'f'		operation
u skip. Q1		Q2	Q3	Q4	11 31	.ιρ. Q1	Q2	Q3	Q4
No		No	No	No		No	No	No	No
operation	on	operation	operation	operation		operation	operation	operation	operation
If skip and fo	llowed	•			If sk	ip and follow	ed by 2-word		
Q1		Q2	Q3	Q4		Q1	Q2	Q3	Q4
No operation	on	No operation	No operation	No operation		No operation	No operation	No operation	No operation
No		No	No	No		No	No	No	No
operation	on	operation	operation	operation		operation	operation	operation	operation
F					-				
Example:		HERE B'	TFSC FLAG	, 1, 0	Exar	<u>npie</u> :	HERE B'	TFSS FLAG	, 1, 0
		TRUE :					TRUE :		
Before Ir	struct	ion				Before Instru	ction		
PC			dress (HERE)			PC		lress (HERE)	
After Ins	tructioi FLAG<1					After Instruct If FLAG			
	PC	= add	dress (TRUE)			PC	= add	lress (FALSI	Ξ)
If I	FLAG<1 PC		dress (FALSI	Ξ)		If FLAG PC		lress (TRUE)	

BTG Bit Toggle f

Syntax: [label] BTG f,b[,a]

Operands: $0 \le f \le 255$

 $0 \le b < 7$ a $\in [0,1]$

Operation: $(\overline{f < b>}) \rightarrow f < b>$

Status Affected: None

Encoding: 0111 bbba ffff ffff

Description: Bit 'b' in data memory location 'f' is

inverted. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value

(default).

Words: 1

Q Cycle Activity:

Cycles:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: BTG PORTC, 4, 0

1

Before Instruction:

 $PORTC = 0111 \ 0101 \ [0x75]$

After Instruction:

 $PORTC = 0110 \ 0101 \ [0x65]$

BOV Branch if Overflow

Syntax: [label] BOV n Operands: $-128 \le n \le 127$ Operation: if overflow bit is '1'

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0100 nnnn nnnn

Description: If the Overflow bit is '1', then the

program will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BOV Jump

Before Instruction

PC = address (HERE)

After Instruction

If Overflow = 1;
 PC = address (Jump)
If Overflow = 0;

PC = address (HERE+2)

BZ Branch if Zero

Syntax: [label] BZ n Operands: $-128 \le n \le 127$ Operation: if Zero bit is '1'

 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding: 1110 0000 nnnn nnnn

Description: If the Zero bit is '1', then the pro-

gram will branch.

The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then

a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write to PC
	'n'	Data	
No	No	No	No
operation	operation	operation	operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	No
	'n'	Data	operation

Example: HERE BZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If Zero = 1;
 PC = address (Jump)
If Zero = 0;
 PC = address (HERE+2)

CALL Subroutine Call

Syntax: [label] CALL k [,s]

Operands: $0 \le k \le 1048575$

 $s \in [0,1]$

Operation: $(PC) + 4 \rightarrow TOS$,

 $k \rightarrow PC<20:1>$,

if s = 1

 $(\mathsf{WREG}) \to \mathsf{WS},$

 $(STATUS) \rightarrow STATUSS,$

(BSR) → BSRS

Status Affected: None

Encoding:

1st word (k<7:0>)
2nd word(k<19:8>)

1110	110s	k ₇ kkk	kkkk ₀
1111	k ₁₉ kkk	kkkk	kkkk ₈

Description: Subroutine call of entire 2M byte

memory range. First, return address (PC+ 4) is pushed onto the return stack. If 's' = 1, the W, STATUS and BSR registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If 's' = 0, no update occurs (default). Then the 20-bit value 'k' is loaded into PC<20:1>.

CALL is a two-cycle instruction.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	Push PC to stack	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: HERE CALL THERE, 1

Before Instruction

PC = Address(HERE)

After Instruction

PC = Address(THERE) TOS = Address (HERE + 4)

WS = WREG BSRS= BSR STATUSS = STATUS Syntax: [label] CLRF f [,a]

Operands: $0 \le f \le 255$ $a \in [0,1]$ Operation: $000h \rightarrow f$

Clear f

 $000h \rightarrow f$ $1 \rightarrow Z$

Status Affected: Z

CLRF

Encoding: 0110 101a fffff ffff

Description: Clears the contents of the specified register. If 'a' is 0, the Access Bank

will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value

(default).

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: CLRF FLAG_REG, 1

Before Instruction

 $FLAG_REG = 0x5A$

After Instruction

FLAG REG = 0x00

CLRWDT Clear Watchdog Timer

Syntax: [label] CLRWDT

Operands: None

Operation: $000h \rightarrow WDT$,

 $000h \rightarrow WDT$ postscaler,

 $1 \to \overline{\text{TO}}, \\ 1 \to \overline{\text{PD}}$

Status Affected: TO, PD

Encoding: 0000 0000 0000 0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the

postscaler of the WDT. Status bits

 $\overline{\mathsf{TO}}$ and $\overline{\mathsf{PD}}$ are set.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	No
	operation	Data	operation

Example: CLRWDT

Before Instruction

WDT counter = ?

After Instruction

COMF	Complement f				
Syntax:	[label] COMF f [,d [,a]				
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$				
Operation:	$(\overline{f}) \rightarrow dc$	est			
Status Affected:	N,Z				
Encoding:	0001	11da	ffff	ffff	
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).				
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q1	Q2	Q3		Q4	
Decode	Read	Proces	s V	Vrite to	

	Decode	Read register 'f'	Proce Dat			Write to destination
Exar	mple:	COMF	REG,	0,	0	
	D - f f	4!				

Before Instruction

REG = 0x13

After Instruction

REG = 0x13WREG = 0xEC

CPFSEQ	Compare f with WREG,
CFF3EQ	skip if f = WREG

Syntax: [label] CPFSEQ f [,a]

Operands: $0 \le f \le 255$

 $a \in [0,1]$

Operation: (f) - (WREG),

skip if (f) = (WREG)

(unsigned comparison)

Status Affected: None

Encoding: 0110 001a ffff ffff

Description: Compares the contents of data

memory location 'f' to the contents of WREG by performing an

unsigned subtraction.

If 'f' = WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the

BSR value (default).

Words: 1 Cycles: 1(2)

Note: 3 cycles if skip and followed

by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	No
	register 'f'	Data	operation
-			

If skip:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation
No	No	No	No
operation	operation	operation	operation

Example: HERE CPFSEQ REG, 0

NEQUAL :

Before Instruction

PC Address = HERE WREG = ? REG = ?

After Instruction

If REG = WREG;

PC = Address (EQUAL)

If REG ≠ WREG;

PC = Address (NEQUAL)

Compare f with WREG, **CPFSGT** skip if f > WREG

Syntax: [label] CPFSGT f[,a]

 $0 \le f \le 255$ Operands:

 $a \in [0,1]$

(f) - (WREG),Operation:

skip if (f) > (WREG)

(unsigned comparison)

Status Affected: None

Encodina: 0110 010a ffff ffff

Description: Compares the contents of data

memory location 'f' to the contents of the WREG by performing an

unsigned subtraction.

If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be

selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value

(default).

1(2)

1 Words:

Note: 3 cycles if skip and followed

by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	No
	register 'f'	Data	operation

If skip:

Cycles:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation
No	No	No	No
operation	operation	operation	operation

Example: HERE CPFSGT REG, 0

> NGREATER GREATER

Before Instruction

PC Address (HERE)

WREG

After Instruction

Tf REG WREG:

PC Address (GREATER) =

If REG \leq WREG:

> PC Address (NGREATER)

Compare f with WREG, **CPFSLT** skip if f < WREG

Syntax: [label] CPFSLT f[,a]

 $0 \le f \le 255$ Operands:

 $a \in [0,1]$

(f) - (WREG),Operation:

skip if (f) < (WREG)

(unsigned comparison)

Status Affected: None

Encodina: 0110 000a ffff ffff

Description: Compares the contents of data

memory location 'f' to the contents of WREG by performing an

unsigned subtraction.

If the contents of 'f' are less than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0. the Access Bank will be

selected. If 'a' is 1, the BSR will not

be overridden (default).

Words: 1 Cycles: 1(2)

Note: 3 cycles if skip and followed

by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4	
Decode	Read	Process	No	
	register 'f'	Data	operation	

If skip:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation operation		operation
No No		No	No
operation	operation	operation	operation

Example: HERE CPFSLT REG, 1

NLESS LESS

Before Instruction

Address (HERE) PC

After Instruction

If REG WREG;

PC Address (LESS)

If REG WREG;

PCAddress (NLESS)

DAV	V	Decimal A	Adjust WRE	G R	egister	
Synt	ax:	[label] Di	[label] DAW			
Оре	rands:	None				
Ope	ration:	If [WREG<3:0> >9] or [DC = 1] ther (WREG<3:0>) + 6 \rightarrow WREG<3:0> else (WREG<3:0>) \rightarrow WREG<3:0>;				
		(WREG<7 else	$<7:4>>9$] or $<7:4>) + 6 \rightarrow$ $<7:4>) \rightarrow WR$	ŴRE	G<7:4>	
Statu	us Affected:	С				
Enco	oding:	0000	0000 00	00	0111	
Desc	cription:	WREG, re addition of packed B0	sts the eightsulting from two variabled DD format) a backed BCD	the es (e and p	earlier each in roduces	
Wor	ds:	1				
Cycl	es:	1				
QC	cycle Activity:					
	Q1	Q2	Q3		Q4	
	Decode	Read	Process		Write	

Q1	Q2	Q3	Q4
Decode	Read register WREG	Process Data	Write WREG

Example1: DAW

Before Instruction

WREG = 0xA5 C = 0 DC = 0

After Instruction

 $\begin{array}{lll} \text{WREG} & = & 0 \times 05 \\ \text{C} & = & 1 \\ \text{DC} & = & 0 \\ \end{array}$

Example 2:

Before Instruction

WREG = 0xCE C = 0 DC = 0

After Instruction

 $\begin{array}{rcl} \text{WREG} & = & 0 \times 34 \\ \text{C} & = & 1 \\ \text{DC} & = & 0 \end{array}$

DECF	Decreme	nt f		
Syntax:	[label] DECF f [,d [,a]			
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	$(f) - 1 \rightarrow dest$			
Status Affected:	C,DC,N,OV,Z			
Encoding:	0000 01da ffff ffff			ffff
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).			

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: DECF CNT, 1, 0

Before Instruction

 $\begin{array}{ccc} CNT & = & 0 \times 01 \\ Z & = & 0 \end{array}$

After Instruction

CNT = 0x00 Z = 1

DECFSZ	Decreme	nt f, skip if (D	DCFSNZ		Decreme	nt f, skip if	not 0
Syntax:	[label] [DECFSZ f[,d [,a]]	Syntax:		[label] D	CFSNZ f[,d [,a]
Operands:	$0 \le f \le 258$ $d \in [0,1]$ $a \in [0,1]$	5		Operands	S :	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	5	
Operation:	(f) $-1 \rightarrow 0$ skip if results			Operation	n:	(f) $-1 \rightarrow 0$ skip if res		
Status Affected:	None			Status Aff	ected:	None		
Encoding:	0010	11da ff	ff ffff	Encoding	:	0100	11da ff	ff ffff
Description:	decrement placed in result is placed in least to the result ion, which discarded instead, minstruction Bank will the BSR value bank will be the bank will be the bank will be the bank will be bank will be bank will be the bank will be bank will be bank will be the bank will be t	nts of regist ted. If 'd' is 0 WREG. If 'd' acced back in the same and a NOP in the same and a NOP in the selected, ralue. If 'a' = the selected are (default).	o, the result is is 1, the is 1, the in register 'f' ext instructed hetched, is sexecuted occupied he Access overriding 1, then the	Description	on:	remented placed in result is p (default). If the result instruction fetched, is executed cycle instruction. Access Barrier overriding then the barrier of the second of th	. If 'd' is 0, th WREG. If 'd laced back i lt is not 0, th n, which is a sinstead, ma ruction. If 'a' ank will be s	' is 1, the n register 'f' ne next lready and a NOP is king it a two- is 0, the elected, lue. If 'a' = 1, selected as
Words:	1	,		Words:		1	,	,
Cycles:		ycles if skip a 2-word ins	and followed struction.	Cycles:			ycles if skip a 2-word ins	and followed struction.
Q Cycle Activity:				Q Cycle	Activity	:		
Q1	Q2	Q3	Q4	-	Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination	De	code	Read register 'f'	Process Data	Write to destination
If skip:				If skip:				
Q1	Q2	Q3	Q4		Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation		No ration	No operation	No operation	No operation
If skip and follow	· ·		1 .			ved by 2-wor	· ·	<u> </u>
Q1	Q2	Q3	Q4	-	Q1	Q2	Q3	Q4
No	No	No	No		No	No	No	No
operation	operation	operation	operation	ope	ration	operation	operation	operation
No operation	No operation	No operation	No operation		No ration	No operation	No operation	No operation
Example:	HERE CONTINUE	DECFSZ GOTO	CNT, 1, 1 LOOP	<u>Example</u> :		ZERO	DCFSNZ TE : :	MP, 1, 0
Before Instru	uction	ss (HERE)			re Instr	uction =	?	
After Instruction CNT If CNT PC If CNT PC	tion = CNT - = 0; = Addres ≠ 0;			After	IEMP Instruc IEMP If TEM PC If TEM PC	etion = = = = = = =	TEMP - 1 0; Address 0; Address	(ZERO)

GOTO	Unconditional Branch			
Syntax:	[label] GOTO k			
Operands:	$0 \leq k \leq 1048575$			
Operation:	$k \rightarrow PC < 20:1 >$			
Status Affected:	None			
Encoding:				

1st word (k<7:0>) 2nd word(k<19:8>)

1111	k ₁₉ kkk	,	kkkk ₈
1110	1111	k ₇ kkk	kkkk.

Description: GOTO allows an unconditional

branch anywhere within entire 2 Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a two-cycle

instruction.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: GOTO THERE

After Instruction

PC = Address (THERE)

INCF	Increment f					
Syntax:	[label]	INCF	f [,d [,a]			
Operands:	$0 \le f \le 255$ d $\in [0,1]$ a $\in [0,1]$					
Operation:	$(f) + 1 \rightarrow$	dest				
Status Affected:	C,DC,N,OV,Z					
Encoding:	0010	10da	ffff	ffff		

Description:

The contents of register 'f' are incremented. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the

BSR value (default).

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: INCF CNT, 1, 0

Before Instruction

CNT = 0xFF Z = 0 C = ? DC = ?

After Instruction

 $\begin{array}{ccccc} {\rm CNT} & = & 0\,{\times}0\,0 \\ {\rm Z} & = & 1 \\ {\rm C} & = & 1 \\ {\rm DC} & = & 1 \end{array}$

INC	FSZ	Incremen	t f, skip if 0		INFS	SNZ	Incremen	t f, skip if n	ot 0	
Synt	ax:	[label]	NCFSZ f[,d [,a]	Synt	ax:	[label] IN	[label] INFSNZ f [,d [,a]		
Ope	rands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	5		Ope	rands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	5		
Ope	ration:	(f) + 1 \rightarrow 0 skip if resu			Ope	ration:	(f) + 1 \rightarrow 0 skip if resu			
Statu	us Affected:	None			Stati	us Affected:	None			
Enco	oding:	0011	11da ff:	ff ffff	Ence	oding:	0100	10da ff	ff ffff	
Desc	cription:				Des	cription:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). If the result is not 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).			
Word	ds:	1			Wor	ds:	1			
Cycl	Cycles: 1(2) Note: 3 cycles if skip and followed by a 2-word instruction.		Cycl	Cycles: 1(2) Note: 3 cycles if skip and by a 2-word instruc						
Q C	cycle Activity:				QC	Cycle Activity	:			
	Q1	Q2	Q3	Q4	•	Q1	Q2	Q3	Q4	
	Decode	Read register 'f'	Process Data	Write to destination		Decode	Read register 'f'	Process Data	Write to destination	

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

If skip:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation
No	No	No	No
operation	operation	operation	operation

Example:	HERE	INCFSZ	CNT,	1,	0
•	NZERO	:			
	ZERO	:			

Before Instruction

PC = Address (HERE)

After Instruction

CNT	=	CNT + 1
If CNT	=	0;
PC	=	Address(ZERO)
If CNT	≠	0;
PC	=	Address(NZERO)

	Decode	Read register 'f'	Process Data	Write to destination
If sk	kip:			
	Ω1	Ω2	Q3	Ω4

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation
No	No	No	No
operation	operation	operation	operation

Example:	HERE	INFSNZ	REG,	1,	0
<u> </u>	ZERO				
	NZERO				

Before Instruction

PC = Address (HERE)

After Instruction

a manachon					
3	=	REG + 1			
REG	\neq	0;			
PC	=	Address	(NZERO)		
REG	=	0;			
PC	=	Address	(ZERO)		
	REG PC REG	REG ≠ PC = REG =	E = REG + 1 REG ≠ 0; PC = Address		

IORLW Inclusive OR literal with WREG

Syntax: [label] IORLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .OR. $k \rightarrow WREG$

Status Affected: N,Z

Encoding: 0000 1001 kkkk kkkk

Description: The contents of WREG are OR'ed with the eight-bit literal 'k'. The

result is placed in WREG.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	WREG

Example: IORLW 0x35

Before Instruction

WREG = 0x9A

After Instruction

WREG = 0xBF

IORWF	Inclusive OR WREG with f			
Syntax:	[label] IORWF f [,d [,a]			
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	(WREG) .OR. (f) \rightarrow dest			
Status Affected:	N,Z			
Encoding:	0001 00da ffff ffff			
Description:	Inclusive OR WREG with register 'f'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).			
Words:	1			

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: IORWF RESULT, 0, 1

Before Instruction

RESULT = 0x13 WREG = 0x91

After Instruction

RESULT = 0x13WREG = 0x93 LFSR Load FSR

Syntax: [label] LFSR f,k

Operands: $0 \le f \le 2$

 $0 \le k \le 4095$

Operation: $k \rightarrow FSRf$

Status Affected: None

Encoding: 1110 1110 00ff $k_{11}kkk$ 1111 0000 $k_{7}kkk$ kkkk

Description: The 12-bit literal 'k' is loaded into

the file select register pointed to

by 'f'.

Words: 2 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write
	'k' MSB	Data	literal 'k'
			MSB to
			FSRfH
Decode	Read literal	Process	Write literal
	'k' LSB	Data	'k' to FSRfL

Example: LFSR 2, 0x3AB

After Instruction

FSR2H = 0x03FSR2L = 0xAB

MOVF	Move f			
Syntax:	[label]	MOVF	f [,d [,a]	
Operands:	$0 \le f \le 25$ $d \in [0,1]$ $a \in [0,1]$	55		
Operation:	$f \to dest$			
Status Affected:	N,Z			
Encoding:	0101	00da	ffff	ffff
Description:	The contents of register 'f' are			

The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). Location 'f' can be anywhere in the 256 byte bank. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write WREG
	register 'f'	Data	

(default).

Example: MOVF REG, 0, 0

Before Instruction

REG = 0x22WREG = 0xFF

After Instruction

REG = 0x22 WREG = 0x22

MOVFF Move f to f

Syntax: [label] MOVFF f_s,f_d

Operands: $0 \le f_s \le 4095$

 $0 \leq f_d \leq 4095$

Operation: $(f_s) \rightarrow f_d$ Status Affected: None

Encoding: 1st word (source) 2nd word (destin.)

1100 ffff ffff ffff_s
1111 ffff ffff ffff_d

Description:

The contents of source register ${}^{t}f_{s}{}^{t}$ are moved to destination register ${}^{t}f_{d}{}^{t}$. Location of source ${}^{t}f_{s}{}^{t}$ can be anywhere in the 4096 byte data space (000h to FFFh), and location of destination ${}^{t}f_{d}{}^{t}$ can also be anywhere from 000h to FFFh.

Either source or destination can be WREG (a useful special situation). MOVFF is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port).

The MOVFF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register.

Words: 2 Cycles: 2 (3)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f' (src)	Process Data	No operation
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: MOVFF REG1, REG2

Before Instruction

REG1 = 0x33REG2 = 0x11

After Instruction

REG1 = 0x33, REG2 = 0x33 MOVLB Move literal to low nibble in BSR

Syntax: [label] MOVLB k

Status Affected: None

Encoding: 0000 0001 kkkk kkk

Description: The 8-bit literal 'k' is loaded into the Bank Select Register (BSR).

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process	Write
	'k'	Data	literal 'k' to
			BSR

Example: MOVLB 5

Before Instruction

BSR register = 0x02

After Instruction

BSR register = 0x05

MOVLW Move literal to WREG

Syntax: [label] MOVLW k

Operands: $0 \le k \le 255$ Operation: $k \to WREG$

Status Affected: None

Encoding: 0000 1110 kkkk kkkk

Description: The eight-bit literal 'k' is loaded into

WREG.

Words: 1 Cycles: 1

Q Cycle Activity:

 Q1
 Q2
 Q3
 Q4

 Decode
 Read | Process | Write to literal 'k' | Data | WREG

Example: MOVLW 0x5A

After Instruction

WREG = 0x5A

MOVWF Move WREG to f

Syntax: [label] MOVWF f [,a]

Operands: $0 \le f \le 255$

 $a \in [0,1]$

Operation: $(WREG) \rightarrow f$

Status Affected: None

Encoding: 0110 111a ffff ffff

Description: Move data from WREG to register

'f'. Location 'f' can be anywhere in the 256 byte bank. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the

BSR value (default).

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: MOVWF REG, 0

Before Instruction

WREG = 0x4F

REG = 0xFF

After Instruction

 $\begin{array}{rcl} \text{WREG} & = & 0x4F \\ \text{REG} & = & 0x4F \end{array}$

MULLW	Multiply Literal with WREG			
Syntax:	[label]	MULLW	k	
Operands:	$0 \leq k \leq 255$			

Operation: (WREG) $x k \rightarrow PRODH:PRODL$

Status Affected: None

Encoding: 0000 1101 kkkk kkkk

Description: An unsigned multiplication is car-

An unsigned multiplication is carried out between the contents of WREG and the 8-bit literal 'k'. The 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte.

WREG is unchanged.

None of the status flags are

affected.

Note that neither overflow, nor carry is possible in this operation. A zero result is possible but

not detected.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	literal 'k'	Data	registers
			PRODH:
			PRODL

Example: MULLW 0xC4

Before Instruction

 $\begin{array}{llll} \text{WREG} & = & \text{0xE2} \\ \text{PRODH} & = & ? \\ \text{PRODL} & = & ? \end{array}$

After Instruction

WREG = 0xE2PRODH = 0xADPRODL = 0x08

Syntax: [label] MULWF f [,a]

Operands: $0 \le f \le 255$

a ∈ [0,1]

Operation: $(WREG) \times (f) \rightarrow PRODH:PRODL$

Status Affected: None

Encoding: 0000 001a ffff ffff

Description:

An unsigned multiplication is carried out between the contents of WREG and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high

byte.

Both WREG and 'f' are

unchanged.

None of the status flags are

affected.

Note that neither overflow, nor carry is possible in this operation. A zero result is possible but not detected. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a'= 1, then the bank will be selected

as per the BSR value (default).

1

Q Cycle Activity:

Words: Cycles:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	registers
			PRODH:
			PRODL

Example: MULWF REG, 1

Before Instruction

WREG = 0xC4
REG = 0xB5
PRODH = ?
PRODL = ?

1

After Instruction

WREG = 0xC4 REG = 0xB5 PRODH = 0x8A PRODL = 0x94 **NEGF** Negate f Syntax: [label] NEGF f [,a] Operands: $0 \le f \le 255$ $a \in [0,1]$ Operation: $(\overline{f}) + 1 \rightarrow f$ Status Affected: N,OV, C, DC, Z Encoding: 110a 0110 ffff ffff Description: Location 'f' is negated using two's complement. The result is placed in the data memory location 'f'. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value. Words: 1

Cycles: Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write
	register 'f'	Data	register 'f'

Example: NEGF REG, 1

Before Instruction

REG = $0011 \ 1010 \ [0x3A]$

After Instruction

 $REG = 1100 \ 0110 \ [0xC6]$

NOF	•	No Operation				
Synt	ax:	[label]	NOP			
Ope	rands:	None				
Ope	ration:	No operation				
Statu	us Affected:	ed: None				
Enco	oding:	0000	0000	000	0.0	0000
		1111	XXXX	XXX	CΧ	XXXX
Description:		No operation.				
Wor	ds:	1				
Cycles:		1				
QC	cycle Activity:					
	Q1	Q2	Q3	3		Q4
	Decode	No	No			No

operation

operation

operation

Example:

None.

POP Pop Top of Return Stack

Syntax: [label] POP

Operands: None

Operation: $(TOS) \rightarrow bit bucket$

Status Affected: None

Encoding: 0000 0000 0000 0110

Description: The TOS value is pulled off the

return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the

return stack.

This instruction is provided to enable the user to properly manage the return stack to incorporate a

software stack.

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	POP TOS	No
	operation	value	operation

Example: POP

GOTO NEW

Before Instruction

TOS = 0031A2hStack (1 level down) = 014332h

After Instruction

TOS = 014332h PC = NEW

PUSH Push Top of Return Stack

Syntax: [label] PUSH

Operands: None

Operation: $(PC+2) \rightarrow TOS$

Status Affected: None

Encoding: 0000 0000 0000 0101

Description: The PC+2 is pushed onto the top of

the return stack. The previous TOS value is pushed down on the stack. This instruction allows to implement a software stack by modifying TOS, and then push it onto the return

stack.

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	PUSH PC+2	No	No
	onto return	operation	operation
	stack		

Example: PUSH

Before Instruction

TOS = 00345Ah PC = 000124h

After Instruction

PC = 000126h TOS = 000126h Stack (1 level down) = 00345Ah RCALL Relative Call

Syntax: [label] RCALL n

Operands: $-1024 \le n \le 1023$ Operation: (PC) + 2 \rightarrow TOS, (PC) + 2 + 2n \rightarrow PC

Status Affected: None

Encoding: 1101 1nnn

Description: Subroutine call with a jump up to 1K from the current location. First, return address (PC+2) is pushed

onto the stack. Then, add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is a two-cycle

nnnn

nnnn

instruction.

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal	Process Data	Write to PC
	Push PC to stack		
No	No	No	No
operation	operation	operation	operation

Example: HERE RCALL Jump

Before Instruction

PC = Address(HERE)

After Instruction

PC = Address(Jump)
TOS = Address (HERE+2)

RESET	Reset			
Syntax:	[label]	RESET		
Operands:	None			
Operation:	Reset all are affect	٠.	·	
Status Affected:	All			
Encoding:	0000	0000	1111	1111
Description:	This instr			•
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3	3	Q4

Q1	Q2	Q3	Q4
Decode	Start	No	No
	reset	operation	operation

Example: RESET

After Instruction

Registers = Reset Value Flags* = Reset Value RETFIE Return from Interrupt

Syntax: [label] RETFIE [s]

Operands: $s \in [0,1]$ Operation: $(TOS) \rightarrow PC$,

1 → GIE/GIEH or PEIE/GIEL,

if s = 1

 $(WS) \rightarrow WREG,$

 $(STATUSS) \rightarrow STATUS,$

 $(BSRS) \rightarrow BSR$,

PCLATU, PCLATH are unchanged.

Status Affected: GIE/GIEH, PEIE/GIEL.

Encoding: 0000 0000 0001 000s

Description: Return from Interrupt. Stack is

popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low priority global interrupt enable bit. If 's' = 1, the contents of

the shadow registers WS,

STATUSS and BSRS are loaded into their corresponding registers, WREG, STATUS and BSR. If

's' = 0, no update of these registers

occurs (default).

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	pop PC from stack
			Set GIEH or GIEL
No operation	No operation	No operation	No operation

Example: RETFIE 1

After Interrupt

PC = TOS
W = WS
BSR = BSRS
STATUS = STATUSS
GIE/GIEH, PEIE/GIEL= 1

RETLW Return Literal to WREG

Syntax: [label] RETLW k

Operands: $0 \le k \le 255$ Operation: $k \to WREG$, $(TOS) \to PC$,

PCLATU, PCLATH are unchanged

Status Affected: None

Encoding: 0000 1100 kkkk kkkk

Description: WREG is loaded with the eight-bit

literal 'k'. The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains

unchanged.

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	pop PC from stack, Write
			to WREG
No	No	No	No
operation	operation	operation	operation

Example:

```
CALL TABLE ; WREG contains table
```

; offset value
; WREG now has
; table value

:

TABLE

ADDWF PCL ; WREG = offset

.

:

RETLW kn ; End of table

Before Instruction

WREG = 0x07

After Instruction

WREG = value of kn

RETURN	Return from Subroutine

Syntax: [label] RETURN [s] Operands: $s \in [0,1]$

 $\begin{array}{l} \text{(WS)} \rightarrow \text{WREG,} \\ \text{(STATUSS)} \rightarrow \text{STATUS,} \\ \text{(BSRS)} \rightarrow \text{BSR,} \end{array}$

PCLATU, PCLATH are unchanged

Status Affected: None

Encoding: 0000 0000 0001 001s

Description:

Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers, WREG,

STATUS and BSR. If 's' = 0, no update of these registers occurs

(default).

Words: 1 Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	pop PC from
	operation	Data	stack
No	No	No	No
operation	operation	operation	operation

Example: RETURN

After Interrupt
PC = TOS

	RLCF	Rotate Left f through Carry
--	------	-----------------------------

Syntax: [label] RLCF f [,d [,a] Operands: $0 \le f \le 255$

 $d \in [0,1]$ $a \in [0,1]$

Operation: $(f < n >) \rightarrow dest < n+1 >$,

 $(f<7>) \rightarrow C,$ (C) \rightarrow dest<0>

Status Affected: C,N,Z

Encoding: 0011 01da fffff

Description: The contents of register 'f' are

rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the

ffff

BSR value (default).

C register f

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: RLCF REG, 0, 0

Before Instruction

REG = 1110 0110

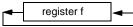
After Instruction

REG = 1110 0110 WREG = 1100 1100 C = 1

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RLNCF	Rotate Left f (no carry)			
Syntax:	[label]	RLNCF	f [,d [,a	a]
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	$(f < n >) \rightarrow dest < n+1 >$, $(f < 7 >) \rightarrow dest < 0 >$			
Status Affected:	N,Z			
Encoding:	0100	01da	ffff	ffff
Description:	The contents of register 'f' are rotated one bit to the left. If 'd' is 0, the result is placed in WREG. If 'd'			

The contents of register 'f' are rotated one bit to the left. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).



Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: RLNCF REG, 1, 0

Before Instruction

REG = 1010 1011

After Instruction

REG = 0101 0111

RRCF Rotate Right f through Carry

Syntax: [label] RRCF f [,d [,a] Operands: $0 \le f \le 255$

 $d \in [0,1] \\ a \in [0,1]$

Operation: $(f<n>) \rightarrow dest<n-1>$,

 $(f<0>) \rightarrow C,$ (C) \rightarrow dest<7>

Status Affected: C,N,Z

Encoding: 0011 00da ffff ffff

Description: The contents of register 'f' are

rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).



Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: RRCF REG, 0, 0

Before Instruction

REG = 1110 0110 C = 0

After Instruction

REG = 1110 0110 WREG = 0111 0011 C = 0 RRNCF Rotate Right f (no carry)

Syntax: [label] RRNCF f [,d [,a]

Operands: $0 \le f \le 255$

 $d \in [0,1]$ $a \in [0,1]$

Operation: $(f<n>) \rightarrow dest<n-1>, \\ (f<0>) \rightarrow dest<7>$

Status Affected: N,Z

Encoding:

0100 00da ffff ffff

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is 0,

the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).



Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: RRNCF REG, 1, 0

Before Instruction

REG = 1101 0111

After Instruction

REG = 1110 1011

Example 2: RRNCF REG, 0, 0

Before Instruction

WREG = ?

REG = 1101 0111

After Instruction

WREG = 1110 1011 REG = 1101 0111 SETF Set f

Syntax: [label] SETF f [,a]

Operands: $0 \le f \le 255$

a ∈ [0,1]

Operation: $FFh \rightarrow f$

Status Affected: None

Description:

Encoding: 0110 100a ffff ffff

The contents of the specified register are set to FFh. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the

BSR value (default).

Words: 1 Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
Ī	Decode	Read	Process	Write
		register 'f'	Data	register 'f'

Example: SETF REG, 1

Before Instruction

REG = 0x5A

After Instruction

REG = 0xFF

SLEEP	Enter SLEEP mode		
SLEEP	Enter SLEEP mode		
Syntax:	[label] SLEEP		
Operands:	None		
Operation:	00h → WDT, 0 → WDT postscaler, 1 → \overline{TO} , 0 → \overline{PD}		
Status Affected:	TO, PD		
Encoding:	0000 0000 0000 0011		
Description:	The power-down status bit (PD) is cleared. The time-out status bit (TO) is set. Watchdog Timer and its postscaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.		

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No	Process	Go to
	operation	Data	sleep

Example: SLEEP

Before Instruction

 $\frac{\overline{\text{TO}}}{\overline{\text{PD}}} = ?$

After Instruction

 $\frac{\text{TO}}{\text{PD}} = 0$

† If WDT causes wake-up, this bit is cleared.

SUBFWB	Subtract f from WREG with b	borrow		
Syntax:	[label] SUBFWB f [,d [,a	1]		
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	$(WREG) - (f) - (\overline{C}) \to dest$			
Status Affected:	N,OV, C, DC, Z			
Encoding:	0101 01da ffff ffff			
Description:	Subtract register 'f' and carry flag (borrow) from WREG (2's complement method). If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).			
Words:	1			

Words: 1
Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example 1: SUBFWB REG, 1, 0

Before Instruction

REG = 3 WREG = 2 C = 1

After Instruction

REG = FF WREG = 2 C = 0 Z = 0

N = 1 ; result is negative

Example 2: SUBFWB REG, 0, 0

Before Instruction

REG = 2 WREG = 5 C = 1

After Instruction

REG = 2 WREG = 3 C = 1 Z = 0

Example 3: SUBFWB REG, 1, 0

Before Instruction

 $\begin{array}{ccc} REG & = & 1 \\ WREG & = & 2 \\ C & = & 0 \end{array}$

After Instruction

REG = 0 WREG = 2 C = 1 Z = 1

; result is zero

; result is positive

SUBLW	Subtrac	t WREG from	literal	SUBWF	Subtract	WREG from	n f
Syntax:	[label]	SUBLW k		Syntax:	[label] ;	SUBWF f[,d [,a]
Operands:	$0 \le k \le 2$	55		Operands:	$0 \le f \le 25$	55	
Operation:	k – (WR	EG) \rightarrow WREG	;		d ∈ [0,1]		
Status Affected:	N,OV, C	•			a ∈ [0,1]		
Encoding:	0000	1000 kkk	k kkkk	Operation:		$(EG) \rightarrow dest$	
Description:		s subtracted f		Status Affected:	N,OV, C,	DC, Z	
Description.		literal 'k'. The		Encoding:	0101	11da ff	ff ffff
		n WREG.		Description:		WREG from	
Words:	1					plement met	hod). If 'd' is in WREG. If
Cycles:	1						ored back in
Q Cycle Activity	/ :				register '	f' (default). If	'a' is 0, the
Q1	Q2	Q3	Q4			Bank will be s g the BSR va	
Decode	Read	Process	Write to			ne bank will b	
	literal 'k'	Data	WREG			e BSR value	
Example 1:	SUBLW	0x02		Words:	1		
Before Instr	uction			Cycles:	1		
WREG	= 1			Q Cycle Activity	:		
C	= ?			Q1	Q2	Q3	Q4
After Instruc				Decode	Read	Process	Write to
WREG C	= 1 = 1	; result i	s positive		register 'f'	Data	destination
Z N	= 0 = 0	•	1	Example 1:	SUBWF	REG, 1, 0	
14	- 0			Before Instr	uction		
Example 2:	SUBLW	0x02		REG	= 3		
Before Instr	uction			WREG C	= 2 = ?		
WREG	= 2			After Instruc			
C	= ?			REG	= 1		
After Instruc				WREG C	= 2 = 1	. rogult i	s positive
WREG C	= 0 = 1	; result :	is zero	Z	= 0	; lesuit i	is posicive
Z N	= 1 = 0	•		N	= 0		
Example 3:		0x02		Example 2:	SUBWF	REG, 0, 0	
Before Instr		UNUZ		Before Instru			
WREG	= 3			REG WREG	= 2 = 2		
C	= ?			С	= ?		
After Instruc	ction			After Instruc			
WREG		; (2's comp		REG WREG	= 2 = 0		
C Z	= 0 = 0	; result is	negative	C	= 1	; result i	ls zero
N	= 1			Z N	= 1 = 0		
				Example 3:	SUBWF	REG, 1, 0	
				Before Instru	uction		
				REG	= 1		
				WREG	= 2		
				C After Instrue	= ?		
				After Instruc	tion = FFh	;(2's comp	olement)
				WREG	= 2		·,
				C Z	= 0 = 0	; result i	ls negative
				N	= 1		

SUBWFB	Subtract	WREG from	f with Borrow	SWAPF	Swap f		
Syntax:	[label]	SUBWFB f	[,d [,a]	Syntax:	[label] S	SWAPF f[,	d [,a]
Operands:	$0 \le f \le 25$ $d \in [0,1]$ $a \in [0,1]$	55		Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	5	
Operation:	* * * * * * * * * * * * * * * * * * * *	$EG) - (\overline{C}) \rightarrow$	dest	Operation:	,	dest<7:4>, dest<3:0>	
Status Affected:	N,OV, C,			Status Affected:	None	7 403140.07	
Encoding:	0101		ff ffff	Encoding:	0011	10da ff	ff ffff
Description:	(borrow) f ment met stored in ' is stored I If 'a' is 0, selected, 'a' is 1, the	hod). If 'd' is 0 WREG. If 'd' is back in registe the Access Ba overriding the	f' (2's comple- t, the result is s 1, the result er 'f' (default). enk will be BSR value. If ill be selected	Description:	The upper ister 'f' are result is pl the result (default). I Bank will be the BSR very bank will be the BSR very bank will be serviced.	and lower rexchanged. aced in WRI is placed in f'a' is 0, the persented, ralue. If 'a' is persented a	nibbles of reg- If 'd' is 0, the EG. If 'd' is 1, register 'f' Access overriding 1, then the
Words:	1				BSR value	e (default).	
Cycles:	1			Words:	1		
Q Cycle Activity:			•	Cycles:	1		
Q1	Q2	Q3	Q4	Q Cycle Activity			
Decode	Read register 'f'	Process Data	Write to destination	Q1	Q2	Q3	Q4
Example 1:	SUBWFB	REG, 1, 0		Decode	Read register 'f'	Process Data	Write to destination
Before Instru	uction						
REG	= 0x19	(0001 100		Example:	SWAPF F	REG, 1, 0	
WREG C	= 0x0D = 1	(0000 110	1)	Before Instru			
After Instruc				REG After Instruc	= 0x53		
REG	= 0x0C	(0000 1013	•	REG	= 0x35		
WREG C	= 0x0D $= 1$	(0000 110	L)				
Z N	= 0 = 0	; result is	s positive				
Example 2:	SUBWFB	REG, 0, 0	-				
Before Instru	uction						
REG WREG C	= 0x1B = 0x1A = 0	(0001 103 (0001 103					
After Instructure REG WREG	= 0x1B = 0x00	(0001 101	1)				
C Z N	= 1 = 1 = 0	; result is	s zero				
Example 3:	SUBWFB	REG, 1, 0					
Before Instru	uction						
REG WREG	= 0x03 $= 0x0E$	(0000 001 (0000 110					
C C	= 0X0E = 1	(0000 110	1)				
After Instruc							
REG	= 0xF5	(1111 010; [2's comp					
WREG	= 0x0E = 0	(0000 110	1)				
C Z	= 0						
N	= 1	; result is	s negative				

TBLRD	Table Rea	d		
Syntax:	[label]	TBLRD (*; *+; *-; +	-*)
Operands:	None			
Operation:	TBLPTI if TBLRD * (Prog M (TBLPT if TBLRD * (Prog M (TBLPT if TBLRD - (TBLPT	flem (TBL R - No Ch +, flem (TBL R) +1 \rightarrow -, flem (TBL R) -1 \rightarrow -,*, -R) +1 \rightarrow	PTR)) → nange; PTR)) → TBLPTR; TBLPTR; TBLPTR; PTR)) →	TABLAT;
Status Affected:	None			
Encoding:	0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*
Description:	This instru	ction is u	sed to rea	d the

TBLRD	Table Re	ead ((cor	nt'd)
Example 1:	TBLRD	*+ ;		
Before Instruc	ction			
TABLAT TBLPTR MEMORY(()x00A356)	=	=	0x55 0x00A356 0x34
After Instruction	on			
TABLAT TBLPTR				0x34 0x00A357
Example 2:	TBLRD	+* ;		
Before Instruc	ction			
)x01A357))x01A358)	=	=	0xAA 0x01A357 0x12 0x34
After Instruction	on			
TABLAT TBLPTR			=	0x34 0x01A358

(

contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used.

The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2 Mbyte address range.

TBLPTR[0] = 0: Least Significant Byte of Program Memory Word TBLPTR[0] = 1: Most Significant Byte of Program Memory Word

The TBLRD instruction can modify the value of TBLPTR as follows:

• no change

• post-increment

post-decrementpre-increment

• p

Cycles: 2
Q Cycle Activity:

Words:

Q1	Q2	Q3	Q4
Decode	No	No	No
	operation	operation	operation
No	No	No	No
operation	operation	operation	operation
	(Read		(Write
	Program		TABLAT)
	Memory)		

TBL	WT	Table Wr	ite					
Synt	ax:	[label]	TBLWT	(*; *+; *-;	+*)			
Ope	rands:	None	None					
Ope	ration:	(TABI or Ho TBLP if TBLWT (TABI or Ho (TBLI	if TBLWT*, (TABLAT) → Prog Mem (TBLPTR) or Holding Register; TBLPTR - No Change; if TBLWT*+, (TABLAT) → Prog Mem (TBLPTR) or Holding Register; (TBLPTR) +1 → TBLPTR;					
		(TABI or Ho (TBLF if TBLWT (TBLF (TABI	if TBLWT*-, (TABLAT) → Prog Mem (TBLPTR) or Holding Register; (TBLPTR) -1 → TBLPTR; if TBLWT+*, (TBLPTR) +1 → TBLPTR; (TABLAT) → Prog Mem (TBLPTR) or Holding Register;					
Statu	us Affected:	None		T	, ,			
Enco	oding:	0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*			
		The TBLI to each b TBLPTR range. TI selects w memory	of Program PTR (a 21- pyte in the p has a 2 M he LSb of t chich byte of location to PTR[0] = 0	bit pointed by the TBLP of the pro- access.	er) points memory. ess FR gram			
		•	Byte of Program Memory Word TBLPTR[0] = 1:Most Significant					
		-	of Program		-			
		value of	The TBLWT instruction can modify the value of TBLPTR as follows:					
		no chano st-in	-					
		•	post-incrementpost-decrement					
			rement					
Word	ds:	1	·					
Cycl		2 (many	2 (many if long write is to on-chip EPROM program memory)					
QC	ycle Activit	y:						
ı	Q1	Q2	Q3		Q4			
	Decode	No	No	1	lo ration			
	No	operation No	operation No		ation Io			
	operation	operation (Read	operation	opei	ation Holding			

Example 1:	TBLWT	*+;

Before Instruction

TABLAT = 0x55 TBLPTR = 0x00A356 MEMORY(0x00A356) = 0xFF

After Instructions (table write completion)

TABLAT = 0x55 TBLPTR = 0x00A357 MEMORY(0x00A356) = 0x55

Example 2: TBLWT +*;

Before Instruction

TABLAT = 0x34 TBLPTR = 0x01389A MEMORY(0x01389A) = 0xFF MEMORY(0x01389B) = 0xFF

After Instruction (table write completion)

TABLAT = 0x34 TBLPTR = 0x01389B MEMORY(0x01389A) = 0xFF MEMORY(0x01389B) = 0x34

TABLAT)

Register or Memory)

TSTFSZ Test f, skip if 0

[label] TSTFSZ f[,a] Syntax:

Operands: $0 \leq f \leq 255$

 $a \in [0,1]$

skip if f = 0Operation:

Status Affected: None

Encoding: 0110 Description: If f' = 0, the next instruction,

fetched during the current instruction execution, is discarded and a NOP is executed, making this a twocycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).

011a

ffff

ffff

Words: 1

1(2) Cycles:

> Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	No
	register 'f'	Data	operation

If skip:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No	No	No	No
operation	operation	operation	operation
No	No	No	No
operation	operation	operation	operation

Example: TSTFSZ CNT, 1 HERE

NZERO ZERO

Before Instruction

PC = Address(HERE)

After Instruction

If CNT 0x00,

Address (ZERO) PC If CNT 0x00,

Address (NZERO)

XORLW Exclusive OR literal with WREG

Syntax: [label] XORLW k

Operands: $0 \le k \le 255$

Operation: (WREG) .XOR. $k \rightarrow WREG$

Status Affected: N,Z

Encoding: 0000 1010 kkkk kkkk

Description: The contents of WREG are

> XORed with the 8-bit literal 'k'. The result is placed in WREG.

Words: Cycles:

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	literal 'k'	Data	WREG

Example: XORLW 0xAF

Before Instruction

WREG 0xB5

After Instruction

WREG 0x1A

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XORWF Exclusive OR WREG with f

Syntax: [label] XORWF f [,d [,a]

Operands: $0 \le f \le 255$

 $d\in [0,1]\\ a\in [0,1]$

Operation: (WREG) .XOR. (f) \rightarrow dest

Status Affected: N,Z

Encoding: 0001 10da

Description: Exclusive OR the contents of

WREG with register 'f'. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in the register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the

ffff

ffff

BSR value (default).

Words: 1 Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read	Process	Write to
	register 'f'	Data	destination

Example: XORWF REG, 1, 0

Before Instruction

REG = 0xAFWREG = 0xB5

After Instruction

REG = 0x1AWREG = 0xB5

20.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- · Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/ MPLIB™ Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC™ In-Circuit Emulator
- · In-Circuit Debugger
 - MPLAB ICD for PIC16F87X
- · Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART® Plus Entry-Level Development Programmer
- · Low Cost Demonstration Boards
 - PICDEM™ 1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELOQ® Demonstration Board

20.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- · An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor
- · A project manager
- Customizable toolbar and key mapping
- · A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- · Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

20.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- · Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process.

20.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

20.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for precompiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

20.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multiproject software development tool.

20.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

20.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

20.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC16F87X and can be used to develop for this and other PIC microcontrollers from the PIC16CXXX family. The MPLAB ICD utilizes the in-circuit debugging capability built into the PIC16F87X. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

20.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

20.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

20.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A). PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE incircuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

20.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C[™] bus and separate headers for connection to an LCD module and a keypad.

20.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

20.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

20.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

TARIE 20-1.	DEVELOPMENT	TOOLS EDOM	MICPOCHID
IADLE ZU-I.	DEVELOPMENT	TOOLS FROM	MICKUCHIE

oo® Transponder Kit IIDTM Programmer's Kit Hz microIDTM loper's Kit Hz Anticollision microIDTM NALA Anticollision NALA Anticollision	MATE® II srsal Device Programmer	TART® Plus Entry Level	AB® ICD In-Circuit	IC TM In-Circuit Emulator	MCREXX HCSXXX SPCXX/ S	WCKE)	HCRXX			DC43C	>	(CO91)	C	BICIECS	(2)9101d	5	*	bicage X	blotect	bicage:			AB® Integrated IOPIDENT Environment AB® C17 C Compiler AB® C18 C Compiler AB® C18 C Compiler AB® C18 C Compiler AB® ICE In-Circuit Emulator IC™ In-Circuit Emulator AB® ICE In-Circuit Emulator IC™ In
	MI'M 2 Demonstration T	ATE® II ATE® III ATE®	AFE® I plus Entry Level \(\) \\ \(\) \\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	9er Chin-Circuit 9gr	## Bit	>																	microID TM Developer's Kit MCP2510 CAN Developer's Kit
Loa® Transponder Kit	M TM 1 Demonstration ✓	ATE® II sal Device Programmer	ART® Plus Entry Level	S [®] CD In-Circuit ger	Participated Part	>>				,													Board PICDEM™ 17 Demonstration Board KEELoa® Evaluation Kit KEELoa® Transponder Kit
DEM™ 17 Demonstration rd Loa® Evaluation Kit	M TM 2 Demonstration	ATE® II sal Device Programmer	ART® Plus Entry Level	3°ICD In-Circuit ger ART® Plus Entry Level	Solute grated Solute grate							>									>		PICDEM™ 3 Demonstration Board PICDEM™ 14A Demonstration Board
M TM 14A Demonstration M TM 17 Demonstration 2® Evaluation Kit	M TM 1 Demonstration	ATE® II sal Device Programmer	ART® Plus Entry Level	3° ICD In-Circuit ART® ILL ART® ILL <td>9° Integrated</td> <td></td> <td></td> <td></td> <td>`</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td></td> <td></td> <td>-</td> <td></td> <td></td> <td></td> <td>PICDEM™ 2 Demonstration Board</td>	9° Integrated				`							-			-				PICDEM™ 2 Demonstration Board
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In-Circuit Emulator		valuator	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		rue to the control of				>	`	`>	`	`	`	`	>	*	>	>	>	>	>	AB® ICE In-Circuit Emulator
Se ICE In-Circuit Emulator					\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		>	>	>	>	>	>	^	>	>	>	>	>	>	>	>	>	SM TM Assembler/ NK TM Object Linker
With Assembler/ Name Assembler of Mink Assembler of Mink Assembler of Mink Assembler of Mink 2 Demonstration With Assembler of Mink 3 Demonstration With Assembler of Mink 3 Demonstration With Assembler of Mink 3 Demonstration With Assemble of Mink 4 Demonstration With Assemble of M	1	Interpretation	Indiator	imulator	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \				>														AB® C18 C Compiler
### Assembler	The control of the	The state of the	The state of the		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \					`	`												AB® C17 C Compiler
Second Compiler Compiler	Translator Tra	Transition Tra	Translator Tra	imulator					>	>	>	>	>	>	>	>	>	>	>	>	>	>	\B [®] Integrated opment Environment

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PIC18CXX2

NOTES:

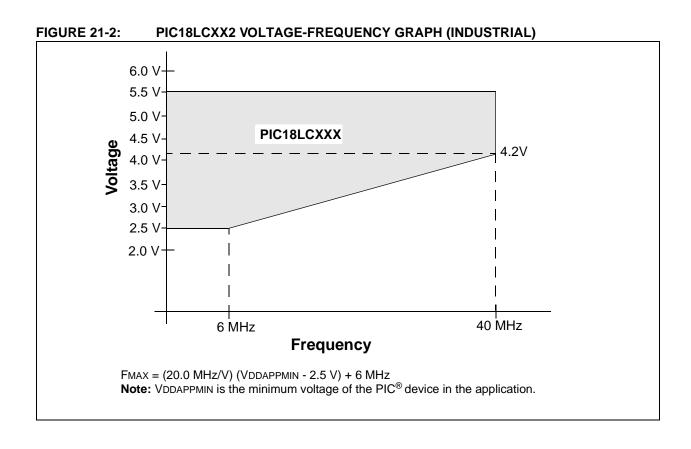
21.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3 V to (VDD + 0.3 V)
Voltage on VDD with respect to Vss	0.3 V to +7.5 V
Voltage on MCLR with respect to Vss (Note 2)	0 V to +13.25 V
Voltage on RA4 with respect to Vss	0 V to +8.5 V
Total power dissipation (Note 1)	1.0 W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, lik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, lok (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB, and PORTE (Note 3) (combined)	200 mA
Maximum current sourced by PORTA, PORTB, and PORTE (Note 3) (combined)	200 mA
Maximum current sunk by PORTC and PORTD (Note 3) (combined)	200 mA
Maximum current sourced by PORTC and PORTD (Note 3) (combined)	200 mA
Note 1: Power dissipation is calculated as follows:	

- Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD \sum IOH} + \sum {(VDD-VOH) x IOH} + \sum (Vol x IOL)
 - 2: Voltage spikes below Vss at the \overline{MCLR}/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the \overline{MCLR}/VPP pin, rather than pulling this pin directly to Vss.
 - 3: PORTD and PORTE not available on the PIC18C2X2 devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



21.1 **DC Characteristics**

PIC18LC (Indus				ard Ope			litions (unless otherwise stated) -40°C ≤ TA ≤ +85°C for industrial
PIC18CX (Indus	X2 strial, Exte	nded)		ard Ope		ire	litions (unless otherwise stated) -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
	VDD	Supply Voltage					
D001		PIC18LCXX2	2.5	_	5.5	V	HS, XT, RC and LP osc mode
D001		PIC18CXX2	4.2	_	5.5	V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5	_	_	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal		_	0.7	V	See section on Power-on Reset for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	_	_	V/ms	See section on Power-on Reset for details
	VBOR	Brown-out Reset Voltage	ge	•		•	
D005		PIC18LCXX2					
		BORV1:BORV0 = 11	2.5	_	2.66	V	
		BORV1:BORV0 = 10	2.7	_	2.86	V	
		BORV1:BORV0 = 01	4.2	—	4.46	V	
		BORV1:BORV0 = 00	4.5	—	4.78	V	
D005		PIC18CXX2					
		BORV1:BORV0 = 1x	N.A.	_	N.A.	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	4.2	_	4.46	V	
		BORV1:BORV0 = 00	4.5	_	4.78	V	

Legend: Shading of rows is to assist in readability of the table.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD

- MCLR = VDD; WDT enabled/disabled as specified.
- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).
- 4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

21.1 DC Characteristics (Continued)

PIC18LC2 (Indus				Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$ for industrial					
PIC18CX	X2 strial, Exte	nded)		ard Ope		ire	litions (unless otherwise stated) -40° C \leq TA \leq +85°C for industrial -40° C \leq TA \leq +125°C for extended		
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions		
	IDD	Supply Current ^(2,4)							
D010		PIC18LCXX2			2	mA	XT, RC, RCIO osc configurations Fosc = 4 MHz, VDD = 2.5V		
D010		PIC18CXX2	_	_	4	mA	XT, RC, RCIO osc configurations Fosc = 4 MHz, VDD = 4.2V		
D010A		PIC18LCXX2	_	_	55	μА	LP osc configuration Fosc = 32 kHz, VDD = 2.5V		
D010A		PIC18CXX2		-	250	μА	LP osc configuration Fosc = 32 kHz, VDD = 4.2V		
D010C		PIC18LCXX2	_	_	38	mA	EC, ECIO osc configurations FOSC = 40 MHz, VDD = 5.5V		
D010C		PIC18CXX2		-	38	mA	EC, ECIO osc configurations FOSC = 40 MHz, VDD = 5.5V		
D013		PIC18LCXX2			3.5 25 38	mA mA mA	HS osc configuration Fosc = 6 MHz, VDD = 2.5V Fosc = 25 MHz, VDD = 5.5V HS + PLL osc configurations Fosc = 10 MHz, VDD = 5.5V		
D013		PIC18CXX2	_ _		25 38	mA mA	HS osc configuration Fosc = 25 MHz, VDD = 5.5V HS + PLL osc configurations Fosc = 10 MHz, VDD = 5.5V		
D014		PIC18LCXX2	_		55	μΑ	Timer1 osc configuration Fosc = 32 kHz, VDD = 2.5V		
D014		PIC18CXX2	_ _		200 250	μΑ μΑ	OSCB osc configuration FOSC = 32 kHz, $VDD = 4.2V$, $-40^{\circ}C$ to $+85^{\circ}C$ FOSC = 32 kHz, $VDD = 4.2V$, $-40^{\circ}C$ to $+125^{\circ}C$		

Legend: Shading of rows is to assist in readability of the table.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

 $\underline{\mathsf{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD $\underline{\mathsf{MCLR}}$ = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).
- **4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

21.1 DC Characteristics (Continued)

PIC18LC			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18CX	Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended							
Param No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions	
	IPD	Power-down Current ⁽³⁾						
D020		PIC18LCXX2	_	<.5 —	2 4	μ Α μ Α	VDD = 2.5V, -40°C to +85°C VDD = 5.5V, -40°C to +85°C	
D020		PIC18CXX2	_	<1	3	μΑ	VDD = 4.2V, -40°C to +85°C	
			_	_	4	μΑ	$VDD = 5.5V, -40^{\circ}C \text{ to } +85^{\circ}C$	
D021B			_	_	15	μΑ	$VDD = 4.2V, -40^{\circ}C \text{ to } +125^{\circ}C$	
			_	_	20	μΑ	$VDD = 5.5V, -40^{\circ}C \text{ to } +125^{\circ}C$	
		Module Differential Cur	rent			1		
D022	Δ lwdt	Watchdog Timer	_	_	1	μΑ	VDD = 2.5V	
		PIC18LCXX2			15	μΑ	VDD = 5.5V	
D022		Watchdog Timer		_	15	μA	$VDD = 5.5V, -40^{\circ}C \text{ to } +85^{\circ}C$	
		PIC18CXX2			20	μΑ	VDD = 5.5V, -40°C to +125°C	
D022A	∆lbor	Brown-out Reset PIC18LCXX2	_	1	45	μΑ	VDD = 2.5V	
D022A		Brown-out Reset	_	_	50	μΑ	$VDD = 5.5V, -40^{\circ}C \text{ to } +85^{\circ}C$	
		PIC18CXX2	—	_	50	μΑ	$VDD = 5.5V, -40^{\circ}C \text{ to } +125^{\circ}$	
D022B	ΔILVD	Low Voltage Detect PIC18LCXX2	_	_	45	μΑ	VDD = 2.5V	
D022B		Low Voltage Detect		_	50	μΑ	VDD = 4.2V, -40°C to +85°C	
		PIC18CXX2		_	50	μ A	VDD = 4.2V, -40°C to +125°C	
D025	Δloscb	Timer1 Oscillator PIC18LCXX2			15	μА	VDD = 2.5V	
D025		Timer1 Oscillator	_	_	100	μΑ	VDD = 4.2V, -40°C to +85°C	
		PIC18CXX2	_	_	120	μΑ	$VDD = 4.2V, -40^{\circ}C \text{ to } +125^{\circ}C$	

Legend: Shading of rows is to assist in readability of the table.

- Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD MCLR = VDD; WDT enabled/disabled as specified.

- 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).
- **4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kOhm.

21.2 DC Characteristics: PIC18CXX2 (Industrial, Extended) PIC18LCXX2 (Industrial)

DC CH	ARACTE	RISTICS	Standard O Operating to		nditions (unless otherwise stated) -40 °C \leq TA \leq +85°C for industrial -40 °C \leq TA \leq +125°C for extended		
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
	VIL	Input Low Voltage					
		I/O ports:					
D030		with TTL buffer	Vss	0.15VDD	V	VDD < 4.5V	
D030A			_	8.0	V	$4.5V \le VDD \le 5.5V$	
D031		with Schmitt Trigger buffer	Vss	0.2Vdd	V		
		RC3 and RC4	Vss	0.3VDD	V		
D032		MCLR	Vss	0.2Vdd	V		
D032A		OSC1 (in XT, HS and LP modes) and T1OSI	Vss	0.3Vdd	V		
D033		OSC1 (in RC and EC mode) ⁽¹⁾	Vss	0.2VDD	V		
	ViH	Input High Voltage					
		I/O ports:					
D040		with TTL buffer	0.25VDD + 0.8V	VDD	V	VDD < 4.5V	
D040A			2.0	VDD	V	$4.5V \leq VDD \leq 5.5V$	
D041		with Schmitt Trigger buffer	0.8VDD	VDD	V		
		RC3 and RC4	0.7VDD	VDD	V		
D042		MCLR, OSC1 (EC mode)	0.8VDD	VDD	V		
D042A		OSC1 (in XT, HS and LP modes) and T1OSI	0.7VDD	VDD	V		
D043		OSC1 (RC mode) ⁽¹⁾	0.9VDD	VDD	V		
	lıL	Input Leakage Current ^(2,3)					
D060		I/O ports	_	±1	μА	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance	
D061		MCLR	_	±5	μА	Vss ≤ VPIN ≤ VDD	
D063		OSC1	_	±5	μ A	$Vss \le VPIN \le VDD$	
	IPU	Weak Pull-up Current					
D070	IPURB	PORTB weak pull-up current	50	400	μА	VDD = 5V, VPIN = VSS	

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC MCU be driven with an external clock while in RC mode.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

21.2 DC Characteristics: PIC18CXX2 (Industrial, Extended) PIC18LCXX2 (Industrial) (Continued)

DC CHARACTERISTICS			Standard O Operating to		nditions (unless otherwise stated) $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended		
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
	Vol	Output Low Voltage					
D080		I/O ports	_	0.6	V	IOL = 8.5 mA , VDD = 4.5V , -40°C to $+85^{\circ}\text{C}$	
D080A			_	0.6	V	IOL = 7.0 mA , VDD = 4.5V , -40°C to $+125^{\circ}\text{C}$	
D083		OSC2/CLKOUT (RC mode)	_	0.6	V	IOL = 1.6 mA , VDD = 4.5V , -40°C to $+85^{\circ}\text{C}$	
D083A			_	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C	
	Vон	Output High Voltage ⁽³⁾					
D090		I/O ports	VDD - 0.7	_	V	IOH = -3.0 mA, VDD = 4.5 V, -40 °C to $+85$ °C	
D090A			VDD - 0.7	_	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C	
D092		OSC2/CLKOUT (RC mode)	VDD - 0.7	_	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C	
D092A			VDD - 0.7	_	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C	
D150	Vod	Open Drain High Voltage	_	8.5	V	RA4 pin	
		Capacitive Loading Specs on Output Pins					
D101	Cio	All I/O pins and OSC2 (in RC mode)	_	50	pF	To meet the AC Timing Specifications	
D102	Св	SCL, SDA	_	400	pF	In I ² C mode	

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC MCU be driven with an external clock while in RC mode.

^{2:} The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

^{3:} Negative current is defined as current sourced by the pin.

FIGURE 21-3: LOW VOLTAGE DETECT CHARACTERISTICS

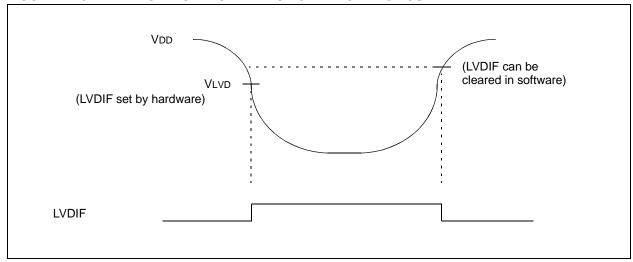


TABLE 21-1: LOW VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended									
Param No.	Symbol	Chara	cteristic	Min	Max	Units	Conditions		
D420	VLVD	LVD Voltage	LVV<3:0> = 0100	2.5	2.66	V			
			LVV<3:0> = 0101	2.7	2.86	V			
			LVV<3:0> = 0110	2.8	2.98	V			
			LVV<3:0> = 0111	3.0	3.2	V			
			LVV<3:0> = 1000	3.3	3.52	V			
			LVV<3:0> = 1001	3.5	3.72	V			
			LVV<3:0> = 1010	3.6	3.84	V			
			LVV<3:0> = 1011	3.8	4.04	V			
			LVV<3:0> = 1100	4.0	4.26	V			
			LVV<3:0> = 1101	4.2	4.46	V			
			LVV<3:0> = 1110	4.5	4.78	V			

TABLE 21-2: EPROM PROGRAMMING REQUIREMENTS

			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +40^{\circ}\text{C}$					
Param. No.	Sym	Characteristic	Min Max Uni		Units	Conditions		
		Internal Program Memory Programming Specs (Note 1)						
D110	VPP	Voltage on MCLR/VPP pin	12.75	13.25	V	(Note 2)		
D111	VDDP	Supply voltage during programming	4.75	5.25	V			
D112	IPP	Current into MCLR/VPP pin	_	50	mΑ			
D113	IDDP	Supply current during programming	_	30	mA			
D114	TPROG	Programming pulse width	50	1000	μS	Terminated via internal/external interrupt or a RESET		
D115	TERASE	EPROM erase time						
		Device operation ≤ 3V	60	_	min.			
		Device operation ≥ 3V	30	_	min.			

Note 1: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in the PIC18CXXX Programming Specifications (Literature Number DS39028).

^{2:} The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

21.3 AC (Timing) Characteristics

21.3.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2	ppS	3. Tcc:st	(I ² C specifications only)
2. TppS		4. Ts	(I ² C specifications only)
T			
F	Frequency	Т	Time
Lowercas	e letters (pp) and their meanings:		
рр			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR
Uppercas	e letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
1	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
I ² C only			
AA	output access	High	High
BUF	Bus free	Low	Low
Tcc:st (l ²	C specifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

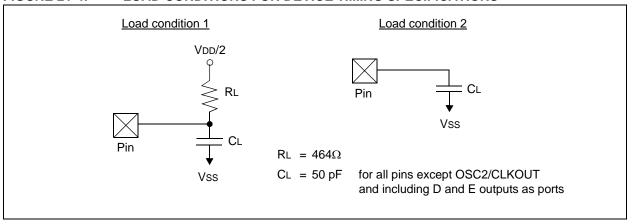
21.3.2 TIMING CONDITIONS

The temperature and voltages specified in Table 21-3 apply to all timing specifications unless otherwise noted. Figure 21-4 specifies the load conditions for the timing specifications.

TABLE 21-3: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

	Standard Operating Conditions (unless otherwise stated)						
	Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
AC CHARACTERISTICS	$-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended						
	Operating voltage VDD range as described in DC spec Section 21.1. LC parts operate for industrial temperatures only.						

FIGURE 21-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



21.3.3 TIMING DIAGRAMS AND SPECIFICATIONS



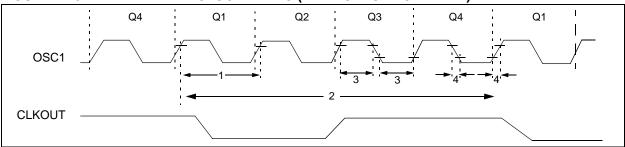


TABLE 21-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	Fosc	External CLKIN	DC	4	MHz	XT osc
		Frequency ⁽¹⁾	DC	25	MHz	HS osc
			4	10	MHz	HS + PLL osc
			DC	40	kHz	LP osc
			DC	40	MHz	EC, ECIO
		Oscillator Frequency ⁽¹⁾	DC	4	MHz	RC osc
			0.1	4	MHz	XT osc
			4	25	MHz	HS osc
			4	10	MHz	HS + PLL osc
			5	200	kHz	LP osc mode
1	Tosc	External CLKIN Period ⁽¹⁾	250	_	ns	XT and RC osc
			40	_	ns	HS osc
			100	250	ns	HS + PLL osc
			25	_	μS	LP osc
			25		ns	EC, ECIO
		Oscillator Period ⁽¹⁾	250	_	ns	RC osc
			250	10,000	ns	XT osc
			25	250	ns	HS osc
			100	250	ns	HS + PLL osc
			25	_	μS	LP osc
2	TCY	Instruction Cycle Time ⁽¹⁾	100	_	ns	Tcy = 4/Fosc
3	TosL,	External Clock in (OSC1)	30	_	ns	XT osc
	TosH	High or Low Time	2.5	_	μS	LP osc
			10		ns	HS osc
4	TosR,	External Clock in (OSC1)	_	20	ns	XT osc
	TosF	Rise or Fall Time		50	ns	LP osc
			_	7.5	ns	HS osc

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

TABLE 21-5: PLL CLOCK TIMING SPECIFICATION (VDD = 4.2V - 5.5V)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
	TRC	PLL Start-up Time (Lock Time)	_	2	ms	
	ΔCLK	CLKOUT Stability (Jitter) using PLL	-2	+2	%	

FIGURE 21-6: CLKOUT AND I/O TIMING

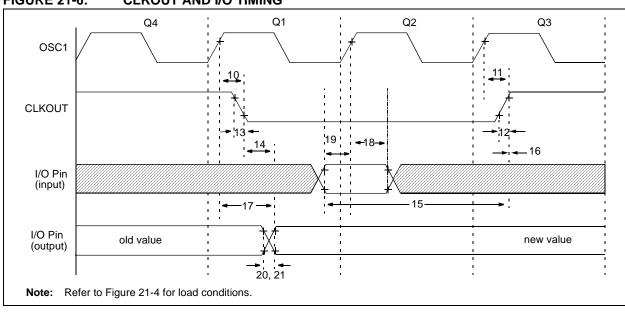


TABLE 21-6: CLKOUT AND I/O TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Тур	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		_	75	200	ns	(1)
11	TosH2ckH	OSC1↑ to CLKOUT↑		_	75	200	ns	(1)
12	TckR	CLKOUT rise time		_	35	100	ns	(1)
13	TckF	CLKOUT fall time		_	35	100	ns	(1)
14	TckL2ioV	CLKOUT ↓ to Port out	valid	_	_	0.5Tcy + 20	ns	(1)
15	TioV2ckH	Port in valid before CLF	KOUT ↑	0.25Tcy + 25		_	ns	(1)
16	TckH2iol	Port in hold after CLKO	0	_	_	ns	(1)	
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to P	_	50	150	ns		
18	TosH2iol	OSC1 [↑] (Q2 cycle) to	PIC18 C XXX	100		_	ns	
18A		Port input invalid (I/O in hold time)	PIC18 LC XXX	200	_	_	ns	
19	TioV2osH	Port input valid to OSC (I/O in setup time)	1↑	0		_	ns	
20	TioR	Port output rise time	PIC18 C XXX	_	12	25	ns	
20A			PIC18 LC XXX	_		50	ns	
21	TioF	Port output fall time	PIC18CXXX	_	12	25	ns	
21A			PIC18 LC XXX	_	_	50	ns	
22††	TINP	INT pin high or low time	 	Tcy	_	_	ns	
23††	TRBP	RB7:RB4 change INT h	nigh or low time	Tcy	_	_	ns	
24††	TRCP	RC7:RC4 change INT h	nigh or low time	20			ns	

^{††} These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

FIGURE 21-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

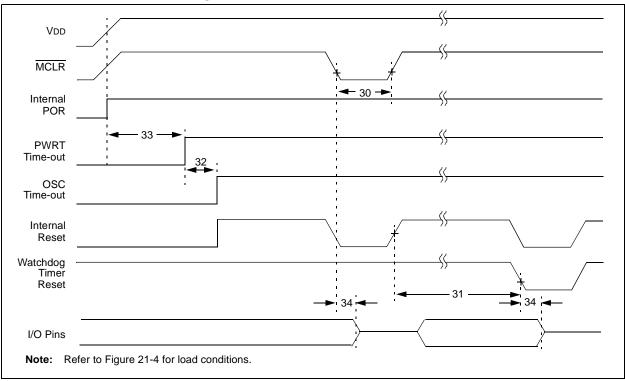


FIGURE 21-8: BROWN-OUT RESET TIMING

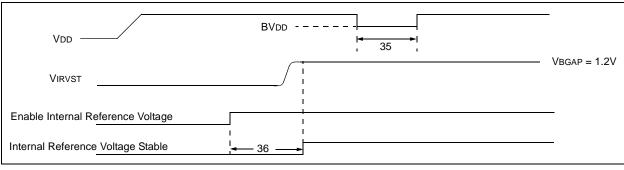


TABLE 21-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Тур	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	2	_	_	μS	
31	TWDT	Watchdog Timer Time-out Period (No Postscaler)	7	18	33	ms	
32	Tost	Oscillation Start-up Timer Period	1024Tosc	1	1024Tosc	_	Tosc = OSC1 period
33	TPWRT	Power up Timer Period	28	72	132	ms	
34	Tıoz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset		2	_	μS	
35	TBOR	Brown-out Reset Pulse Width	200	_	_	μS	VDD ≤ BVDD (See D005)
36	Tivrst	Time for Internal Reference Voltage to become stable	_	20	50	μS	

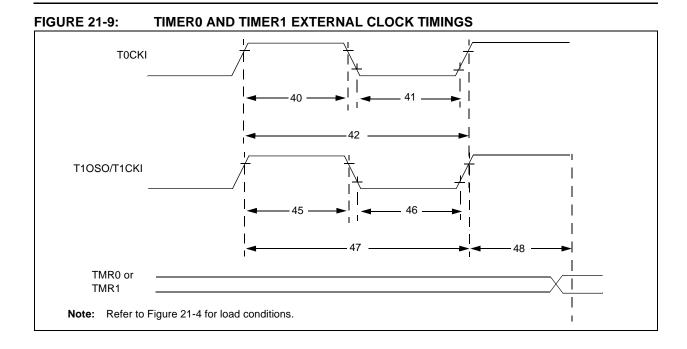


TABLE 21-8: TIMERO AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol		Characteris	tic	Min	Max	Units	Conditions
40	Tt0H	T0CKI F	ligh Pulse Width	No Prescaler	0.5Tcy + 20	_	ns	
				With Prescaler	10	_	ns	
41	Tt0L	T0CKI L	ow Pulse Width	No Prescaler	0.5Tcy + 20	_	ns	
				With Prescaler	10	-	ns	
42	Tt0P	T0CKI P	Period	No Prescaler	Tcy + 10	1	ns	
				With Prescaler	Greater of: 20 ns or <u>Tcy + 40</u> N		ns	N = prescale value (1, 2, 4,, 256)
45	Tt1H	T1CKI	Synchronous, no	prescaler	0.5Tcy + 20	_	ns	
		High	Synchronous,	PIC18CXXX	10	_	ns	
		Time	with prescaler	PIC18 LC XXX	25	-	ns	
			Asynchronous	PIC18CXXX	30	1	ns	
				PIC18 LC XXX	40	_	ns	
46	Tt1L	T1CKI Low	Synchronous, no	prescaler	0.5Tcy + 20		ns	
			Synchronous,	PIC18CXXX	15	_	ns	
		Time	me with prescaler	PIC18 LC XXX	30	_	ns	
			Asynchronous	PIC18CXXX	30		ns	
				PIC18 LC XXX	40	_	ns	
47	Tt1P	T1CKI input period	Synchronous		Greater of: 20 ns or <u>Tcy + 40</u> N		ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60	_	ns	
	Ft1	T1CKI o	scillator input freq	uency range	DC	50	kHz	
48	Tcke2tmrl	Delay fro	om external T1CK crement	I clock edge to	2Tosc	7Tosc	_	

FIGURE 21-10: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)

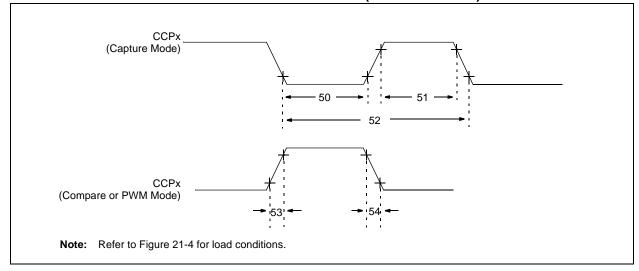


TABLE 21-9: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions	
50 TccL		CCPx input low	No Prescaler		0.5Tcy + 20	_	ns	
		time	With Prescaler	PIC18CXXX	10	_	ns	
				PIC18 LC XXX	20	_	ns	
51	TccH	CCPx input high time	No Prescaler		0.5Tcy + 20	_	ns	
			With Prescaler	PIC18CXXX	10	_	ns	
				PIC18 LC XXX	20	_	ns	
52	TccP	CCPx input period			3Tcy + 40 N	_	ns	N = prescale value (1,4 or 16)
53	TccR	CCPx output fall time PIC18CXXX PIC18LCXXX		PIC18CXXX	_	25	ns	
				_	50	ns		
54	TccF	CCPx output fall time		PIC18CXXX	_	25	ns	
				PIC18 LC XXX	_	50	ns	

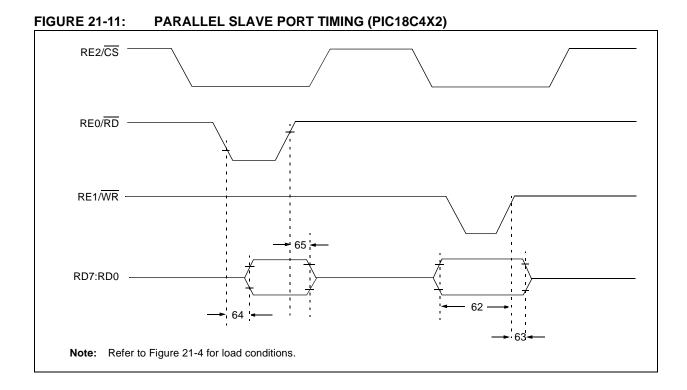


TABLE 21-10: PARALLEL SLAVE PORT REQUIREMENTS (PIC18C4X2)

Param. No.	Symbol	Characteristic			Max	Units	Conditions	
62	TdtV2wrH	Data in valid before WR↑ or CS↑ (setup time)		20	_	ns		
				25	_	ns	Extended Temp. Range	
63	TwrH2dtl	WR↑ or CS↑ to data–in invalid	PIC18CXXX	20	_	ns		
		(hold time)	PIC18 LC XXX	35	_	ns		
64	TrdL2dtV	RD↓ and CS↓ to data–out valid		_	80	ns		
					90	ns	Extended Temp. Range	
65	TrdH2dtl	RD↑ or CS↑ to data–out invalid			30	ns		
66	TibfINH	Inhibit of the IBF flag bit being cleared from WR↑ or CS↑		_	3TcY			

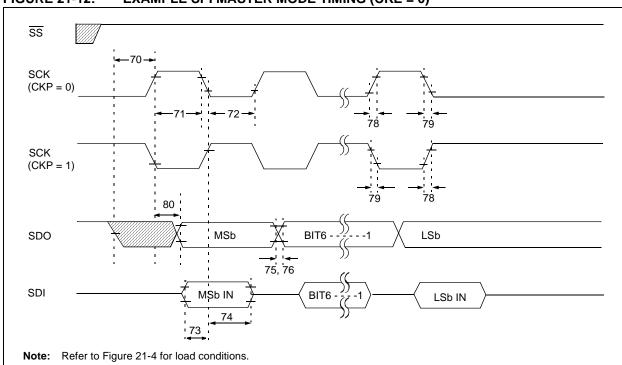


FIGURE 21-12: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)

TABLE 21-11: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param. No.	Symbol	Characteristi	Min	Max	Units	Conditions	
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	_	ns		
71	TscH	SCK input high time	Continuous	1.25Tcy + 30	_	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCK input low time	Continuous	1.25Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to	100	_	ns		
73A	Тв2в	Last clock edge of Byte1 to the of Byte2	1.5Tcy + 40	_	ns	(Note 2)	
74	TscH2diL, TscL2diL	Hold time of SDI data input to	100	_	ns		
75	TdoR	SDO data output rise time	PIC18 C XXX	_	25	ns	
			PIC18 LC XXX	_	45	ns	
76	TdoF	SDO data output fall time	_	25	ns		
78	TscR	SCK output rise time (Master mode)	PIC18 C XXX	_	25	ns	
			PIC18 LC XXX	_	45	ns	
79	TscF	SCK output fall time (Master m	_	25	ns		
80	TscH2doV,	SDO data output valid after	PIC18 C XXX		50	ns	
	TscL2doV	SCK edge	PIC18 LC XXX		100	ns	

Note 1: Requires the use of Parameter # 73A.

2: Only if Parameter # 71A and # 72A are used.

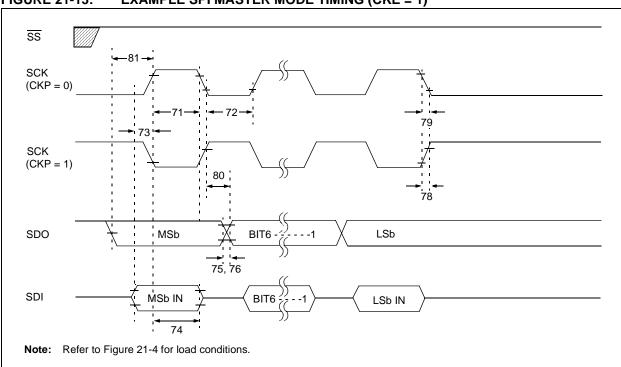


FIGURE 21-13: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

TABLE 21-12: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characterist	ic	Min	Max	Units	Conditions
71	TscH	SCK input high time	Continuous	1.25Tcy + 30	_	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCK input low time Continuous		1.25Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input t	100	_	ns		
73A	Тв2в	Last clock edge of Byte1 to the of Byte2	1.5Tcy + 40	_	ns	(Note 2)	
74	TscH2diL, TscL2diL	Hold time of SDI data input to	SCK edge	100	_	ns	
75	TdoR	SDO data output rise time	PIC18 C XXX	_	25	ns	
			PIC18 LC XXX		45	ns	
76	TdoF	SDO data output fall time		_	25	ns	
78	TscR	SCK output rise time	PIC18 C XXX	_	25	ns	
		(Master mode)	PIC18 LC XXX		45	ns	
79	TscF	SCK output fall time (Master i	mode)	_	25	ns	
80	TscH2doV,	SDO data output valid after PIC18 C XXX		_	50	ns	
	TscL2doV	SCK edge PIC18 LC XXX			100	ns	
81	TdoV2scH, TdoV2scL	SDO data output setup to SC	K edge	Tcy		ns	

Note 1: Requires the use of Parameter # 73A.

2: Only if Parameter # 71A and # 72A are used.

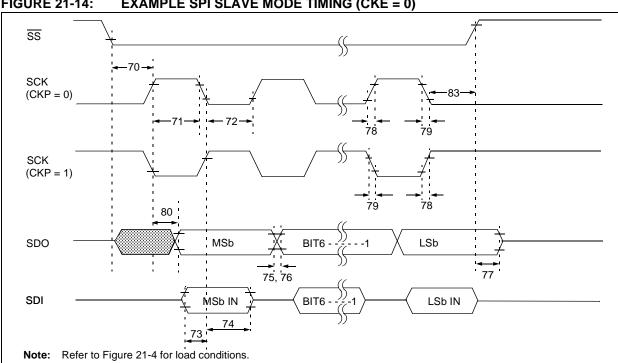


FIGURE 21-14: **EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)**

TABLE 21-13: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0))

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	Tcy	ı	ns		
71	TscH	SCK input high time	out high time Continuous		_	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCK input low time	Continuous	1.25Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK	tup time of SDI data input to SCK edge			ns	
73A	Тв2в	Last clock edge of Byte1 to the first cl	Last clock edge of Byte1 to the first clock edge of Byte2			ns	(Note 2)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK	edge	100		ns	
75	TdoR	SDO data output rise time	PIC18 C XXX	_	25	ns	
			PIC18 LC XXX		45	ns	
76	TdoF	SDO data output fall time		_	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance		10	50	ns	
78	TscR	SCK output rise time	PIC18 C XXX	_	25	ns	
		(Master mode)	PIC18 LC XXX		45	ns	
79	TscF	SCK output fall time (Master mode)			25	ns	
80	TscH2doV,	SDO data output valid after SCK	out valid after SCK PIC18 C XXX		50	ns	
	TscL2doV	edge	PIC18 LC XXX		100	ns	
83	TscH2ssH, TscL2ssH	SS ↑ after SCK edge		1.5Tcy + 40	_	ns	

Note 1: Requires the use of Parameter # 73A.

2: Only if Parameter # 71A and # 72A are used.

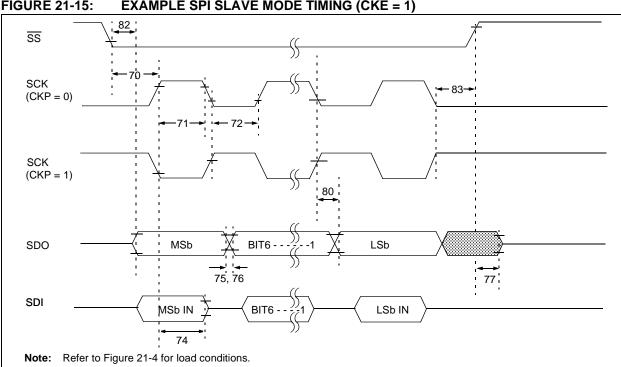


FIGURE 21-15: **EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)**

TABLE 21-14: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param. No.	Symbol	Characteristic	;	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS↓ to SCK↓ or SCK↑ input	K↓ or SCK↑ input			ns	
71	TscH	SCK input high time	ime Continuous		_	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCK input low time	Continuous	1.25Tcy + 30	_	ns	
72A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
73A	Тв2в	Last clock edge of Byte1 to the first	clock edge of Byte2	1.5Tcy + 40	_	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SC	K edge	100	_	ns	
75	TdoR	SDO data output rise time	PIC18CXXX	_	25	ns	
			PIC18 LC XXX		45	ns]
76	TdoF	SDO data output fall time		_	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance		10	50	ns	
78	TscR	SCK output rise time	PIC18 C XXX	_	25	ns	
		(Master mode)	PIC18 LC XXX	_	45	ns]
79	TscF	SCK output fall time (Master mod	e)	_	25	ns	
80	TscH2doV,	SDO data output valid after SCK	PIC18CXXX	_	50	ns	
	TscL2doV	edge	PIC18 LC XXX		100	ns	
82	TssL2doV	SDO data output valid after SS↓	t valid after SS↓ PIC18 C XXX		50	ns	
		edge	PIC18 LC XXX		100	ns	
83	TscH2ssH, TscL2ssH	SS ↑ after SCK edge		1.5Tcy + 40	_	ns	

Note 1: Requires the use of Parameter # 73A.

2: Only if Parameter # 71A and # 72A are used.

FIGURE 21-16: I²C BUS START/STOP BITS TIMING

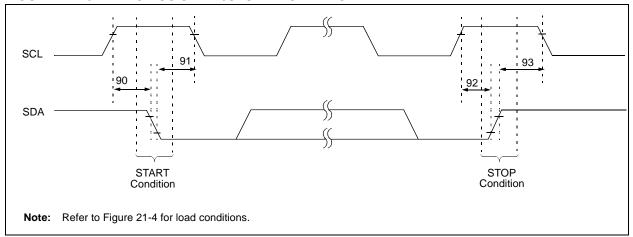


TABLE 21-15: I²C BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characte	ristic	Min	Max	Units	Conditions
90	Tsu:sta	START condition	100 kHz mode	4700	_	ns	Only relevant for Repeated
		Setup time	400 kHz mode	600	_		START condition
91	Thd:sta	START condition	100 kHz mode	4000	_	ns	After this period the first
		Hold time	400 kHz mode	600	_		clock pulse is generated
92	Tsu:sto	STOP condition	100 kHz mode	4700	_	ns	
		Setup time	400 kHz mode	600	_		
93	Thd:sto	STOP condition	100 kHz mode	4000	_	ns	
		Hold time	400 kHz mode	600	_		

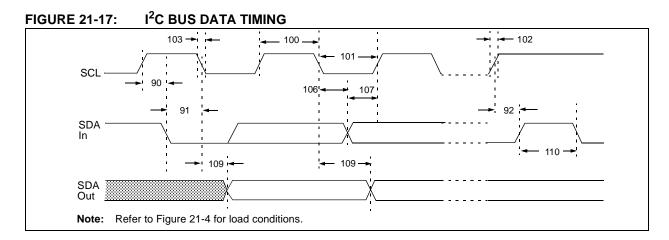


TABLE 21-16: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characte	ristic	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	_	μЅ	PIC18CXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	_	μS	PIC18CXXX must operate at a minimum of 10 MHz
			SSP Module	1.5TcY	_		
101	TLOW	Clock low time	100 kHz mode	4.7	_	μS	PIC18CXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	_	μS	PIC18CXXX must operate at a minimum of 10 MHz
			SSP Module	1.5TcY	_		
102	TR	SDA and SCL rise	100 kHz mode	_	1000	ns	
		time	400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	_	300	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10 to 400 pF
90	Tsu:sta	START condition	100 kHz mode	4.7	_	μS	Only relevant for Repeated
		setup time	400 kHz mode	0.6	_	μS	START condition
91	THD:STA	START condition hold	100 kHz mode	4.0	_	μS	After this period the first clock
		time	400 kHz mode	0.6		μS	pulse is generated
106	THD:DAT	Data input hold time	100 kHz mode	0	_	ns	
			400 kHz mode	0	0.9	μS	
107	TSU:DAT	Data input setup time	100 kHz mode	250	_	ns	(Note 2)
			400 kHz mode	100	_	ns	
92	Tsu:sto	STOP condition setup	100 kHz mode	4.7	_	μS	
		time	400 kHz mode	0.6	_	μS	
109	TAA	Output valid from	100 kHz mode	_	3500	ns	(Note 1)
		clock	400 kHz mode	_	_	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free before
			400 kHz mode	1.3	_	μS	a new transmission can start
D102	Св	Bus capacitive loading		_	400	pF	

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

^{2:} A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.

TR max. + Tsu:DAT = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

FIGURE 21-18: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS

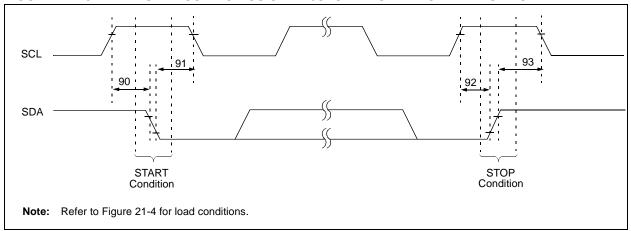


TABLE 21-17: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	Tsu:sta	START condition	100 kHz mode	2(Tosc)(BRG + 1)		ns	Only relevant for
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	_		Repeated START condition
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_		Condition
91	THD:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ns	After this period the
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	_		first clock pulse is
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_		generated
92	Tsu:sto	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ns	
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	_		
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_		
93	THD:STO	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ns	
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	_		
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_		

Note 1: Maximum pin capacitance = 10 pF for all $I^2\text{C}$ pins.

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FIGURE 21-19: MASTER SSP I²C BUS DATA TIMING

TABLE 21-18: MASTER SSP I²C BUS DATA REQUIREMENTS

Param. No.	Symbol	Charac	cteristic	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)		ms	
101	TLOW	Clock low time	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)		ms	
102	TR	SDA and SCL	100 kHz mode			ns	CB is specified to be
		rise time	400 kHz mode	20 + 0.1CB	300	ns	from 10 to 400 pF
			1 MHz mode ⁽¹⁾	_	300	ns	
103	TF	SDA and SCL	100 kHz mode	_	300	ns	CB is specified to be
		fall time	400 kHz mode	20 + 0.1CB	300	ns	from 10 to 400 pF
			1 MHz mode ⁽¹⁾	_	100	ns	
90	Tsu:sta	START condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	Only relevant for
		setup time	400 kHz mode	2(Tosc)(BRG + 1)	_	ms	Repeated START
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	condition
91	THD:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	After this period the
		hold time	400 kHz mode	2(Tosc)(BRG + 1)	_	ms	first clock pulse is
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	generated
106	THD:DAT	Data input	100 kHz mode	0	_	ns	
		hold time	400 kHz mode	0	0.9	ms	
			1 MHz mode ⁽¹⁾	TBD	_	ns	
107	TSU:DAT	Data input	100 kHz mode	250	_	ns	(Note 2)
		setup time	400 kHz mode	100	_	ns	
			1 MHz mode ⁽¹⁾	TBD	_	ns	
92	Tsu:sto	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	_	ms	
		setup time	400 kHz mode	2(Tosc)(BRG + 1)	_	ms	
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	_	ms	
109	TAA	Output valid from	100 kHz mode	_	3500	ns	
		clock	400 kHz mode	_	1000	ns	
			1 MHz mode ⁽¹⁾	_	_	ns	
110	TBUF	Bus free time	100 kHz mode	4.7	_	ms	Time the bus must be
			400 kHz mode	1.3	_	ms	free before a new
			1 MHz mode ⁽¹⁾	TBD	_	ms	transmission can start
D102	Св	Bus capacitive loa		_	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I^2C pins.

^{2:} A fast mode I²C bus device can be used in a standard mode I²C bus system, but parameter #107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, parameter #102 + parameter #107 = 1000 + 250 = 1250 ns (for 100 kHz mode) before the SCL line is released.

FIGURE 21-20: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

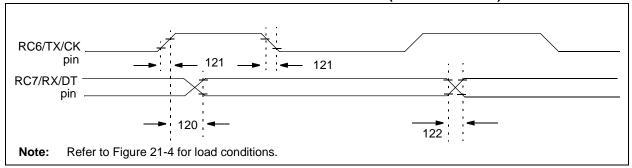


TABLE 21-19: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param. No.	Symbol	Characteristic	Characteristic		Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE)					
		Clock high to data out valid	PIC18CXXX		40	ns	
			PIC18 LC XXX		100	ns	
121	Tckrf	Clock out rise time and fall time	PIC18 C XXX		25	ns	
		(Master mode)	PIC18 LC XXX	_	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC18 C XXX	_	25	ns	
			PIC18 LC XXX	_	50	ns	

FIGURE 21-21: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

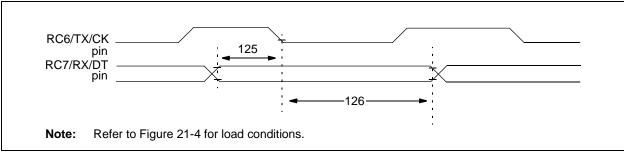


TABLE 21-20: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
125	TdtV2ckl	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	10		ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	_	ns	

TABLE 21-21: A/D CONVERTER CHARACTERISTICS: PIC18CXX2 (INDUSTRIAL, EXTENDED) PIC18LCXX2 (INDUSTRIAL)

Param No.	Symbol	Charac	teristic	Min	Тур	Max	Units	Conditions
A01	NR	Resolution		_	_	10	bit	VREF = VDD ≥ 3.0V
				_	_	10	bit	VREF = VDD < 3.0V
A03	EIL	Integral linearity	/ error	_	_	<±1	LSb	VREF = VDD ≥ 3.0V
						<±2	LSb	VREF = VDD < 3.0V
A04	EDL	Differential linearity error			_	<±1	LSb	$VREF = VDD \ge 3.0V$
						<±2	LSb	VREF = VDD < 3.0V
A05	EFS	Full scale error			_	<±1	LSb	$VREF = VDD \ge 3.0V$
				_		<±1	LSb	VREF = VDD < 3.0V
A06	Eoff	Offset error		_	_	<±1	LSb	VREF = VDD ≥ 3.0V
				_		<±1	LSb	VREF = VDD < 3.0V
A10	_	Monotonicity	Monotonicity		guaranteed ⁽³⁾		_	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage		0V	_	_	V	
A20A		(VREFH - VREFL)	3V	_	_	V	For 10-bit resolution
A21	VREFH	Reference volta	ige High	AVss	_	AVDD + 0.3V	V	
A22	VREFL	Reference volta	age Low	AVss - 0.3V	_	AVDD	V	
A25	VAIN	Analog input vo	ltage	AVss - 0.3V	_	VREF + 0.3V	V	
A30	ZAIN	Recommended analog voltage		_	_	10.0	kΩ	
A40	lad	A/D conversion	PIC18 C XXX	_	180	_	μΑ	Average current
		current (VDD)	PIC18 LC XXX		90	_	μА	consumption when A/D is on (Note 1) .
A50	IREF	VREF input curr	ent (Note 2)	10	_	1000	μ A	During VAIN acquisition. Based on differential of VHOLD to VAIN. To charge CHOLD, see Section 16.0.
					_	10	μА	During A/D conversion cycle.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

VREF current is from RA2/AN2/VREF- and RA3/AN3/VREF+ pins or AVDD and AVSS pins, whichever is selected as reference input.

- **2:** $VSS \le VAIN \le VREF$
- 3: The A/D conversion result never decreases with an increase in the Input Voltage, and has no missing codes.

FIGURE 21-22: A/D CONVERSION TIMING

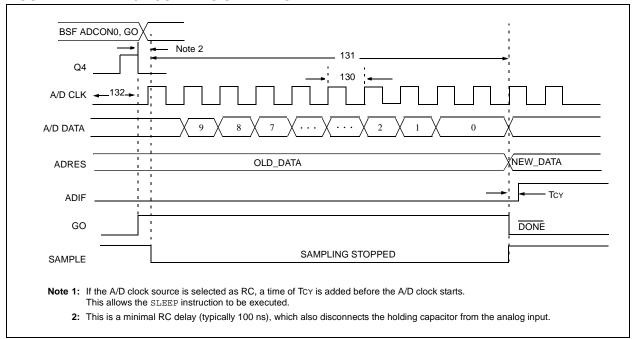


TABLE 21-22: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characte	eristic	Min	Max	Units	Conditions
130	TAD	A/D clock period	PIC18 C XXX	1.6	20 ⁽⁵⁾	μS	Tosc based, VREF ≥ 3.0V
		PIC18LCXXX		3.0	20 ⁽⁵⁾	μS	Tosc based, VREF full range
		PIC18 C XXX		2.0	6.0	μS	A/D RC mode
			3.0	9.0	μS	A/D RC mode	
131	TCNV	Conversion time (not including acquisition	11	12	TAD		
132	TACQ	Acquisition time (Note	3)	15 10	_	μS μS	-40°C ≤ Temp ≤ 125°C 0°C ≤ Temp ≤ 125°C
135	Tswc	Switching Time from co	onvert → sample	_	(Note 4)		
136	Тамр	Amplifier settling time (1	_	μS	This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).	

Note 1: ADRES register may be read on the following TcY cycle.

- 2: See Section 16.0 for minimum conditions, when input voltage has changed more than 1 LSb.
- **3:** The time for the holding capacitor to acquire the "New" input voltage, when the voltage changes full scale after the conversion (AVDD to AVss, or AVss to AVDD). The source impedance (*Rs*) on the input channels is 50 Ω.
- 4: On the next Q4 cycle of the device clock.
- **5:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

22.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for design guidance and are not tested.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C. 'Max' or 'min' represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

FIGURE 22-1: TYPICAL IDD vs. Fosc OVER VDD (HS MODE)

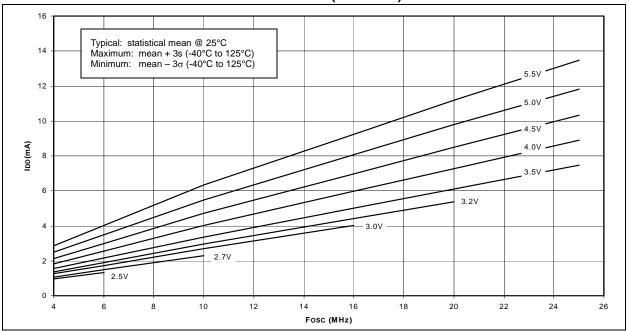


FIGURE 22-2: MAXIMUM IDD vs. Fosc OVER VDD (HS MODE)

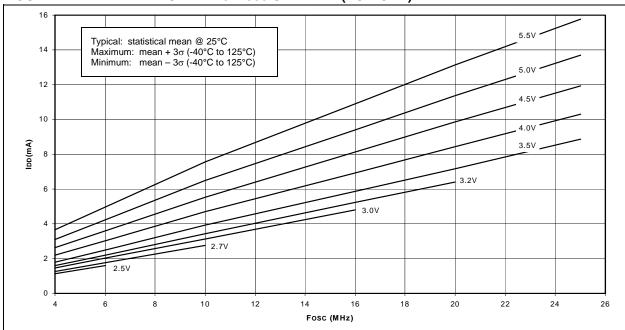


FIGURE 22-3: TYPICAL IDD vs. FOSC OVER VDD (HS/PLL MODE)

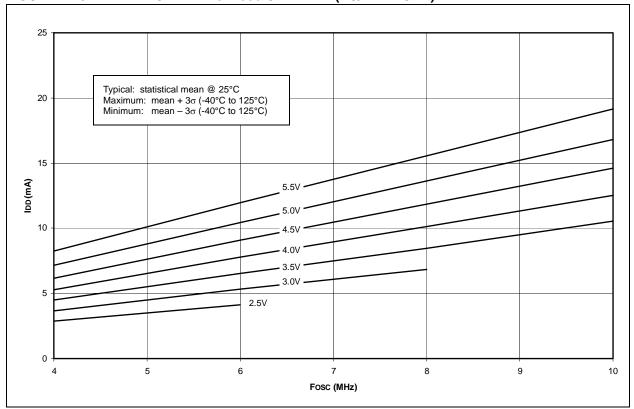
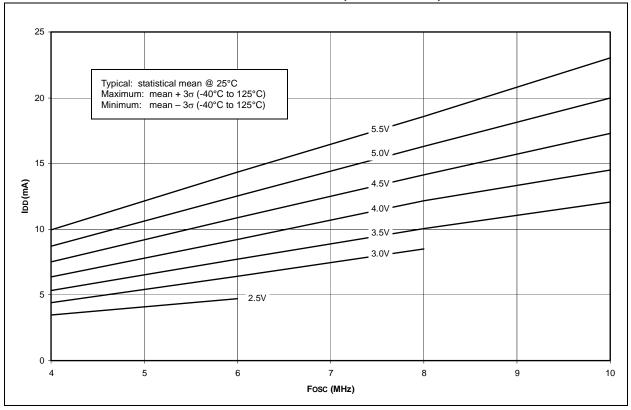
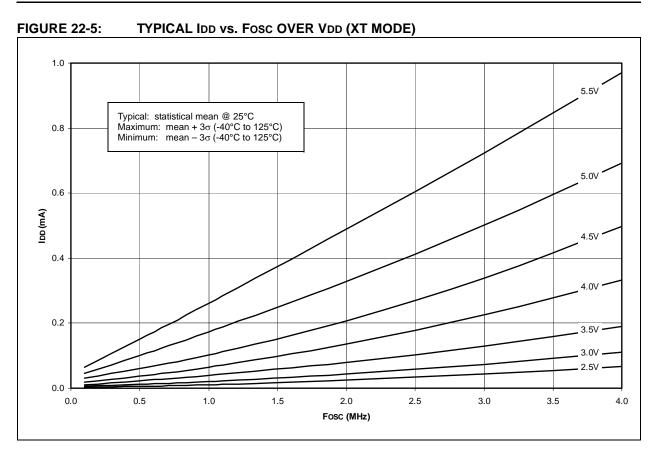


FIGURE 22-4: MAXIMUM IDD vs. FOSC OVER VDD (HS/PLL MODE)





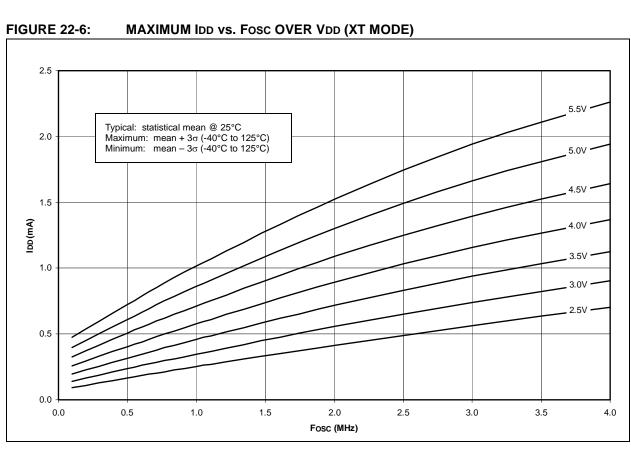
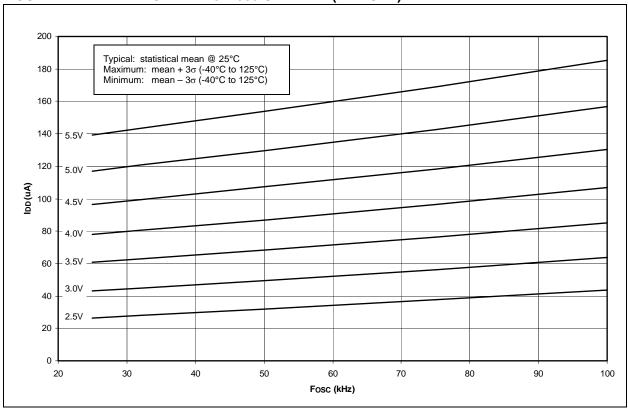
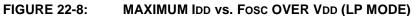


FIGURE 22-7: TYPICAL IDD vs. FOSC OVER VDD (LP MODE)





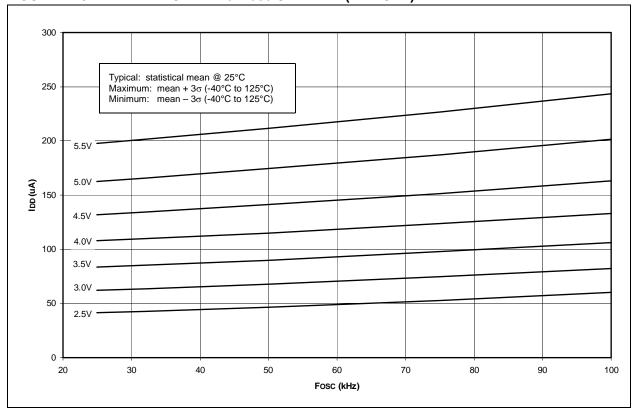


FIGURE 22-9: TYPICAL AND MAXIMUM IDD vs. VDD (TIMER1 AS MAIN OSCILLATOR, 32.768 kHz, C = 47 pF)

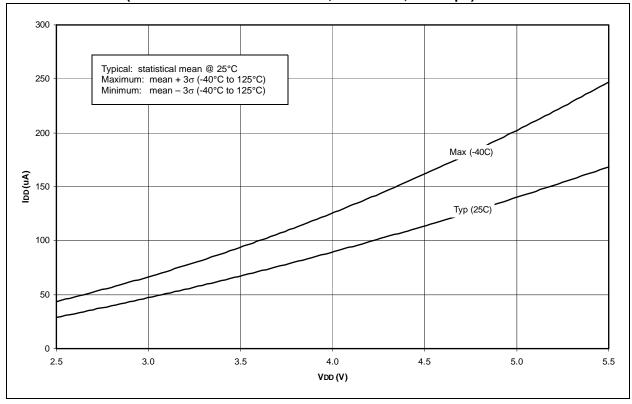


FIGURE 22-10: AVERAGE FOSC vs. VDD FOR VARIOUS VALUES OF R (RC MODE, C = 20 pF, 25°C)

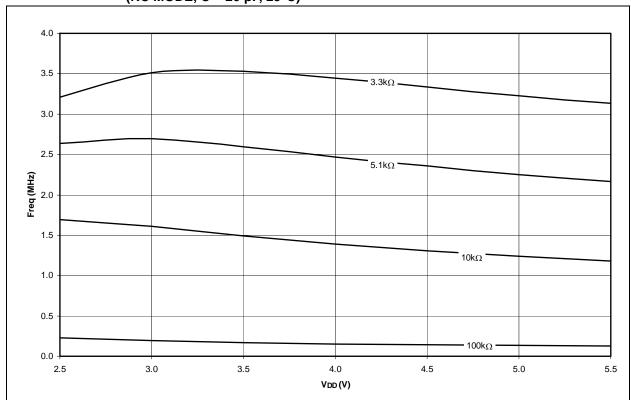


FIGURE 22-11: AVERAGE FOSC vs. VDD FOR VARIOUS VALUES OF R (RC MODE, C = 100 pF, 25°C)

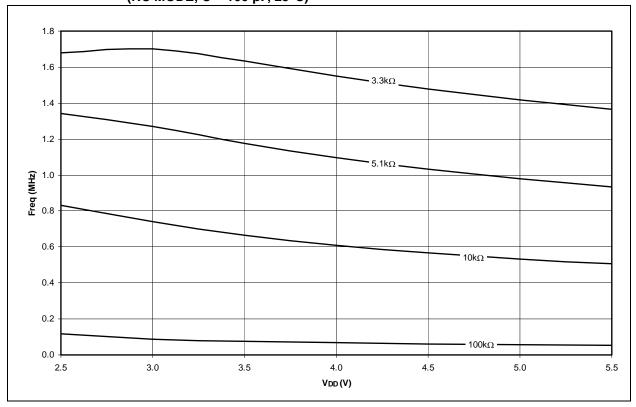
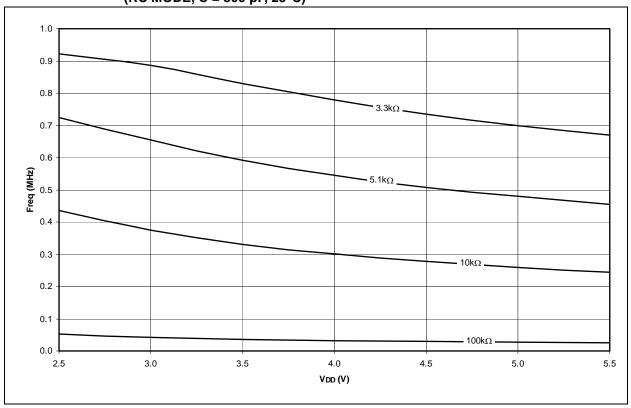


FIGURE 22-12: AVERAGE FOSC vs. VDD FOR VARIOUS VALUES OF R (RC MODE, $C = 300 \text{ pF}, 25^{\circ}\text{C}$)



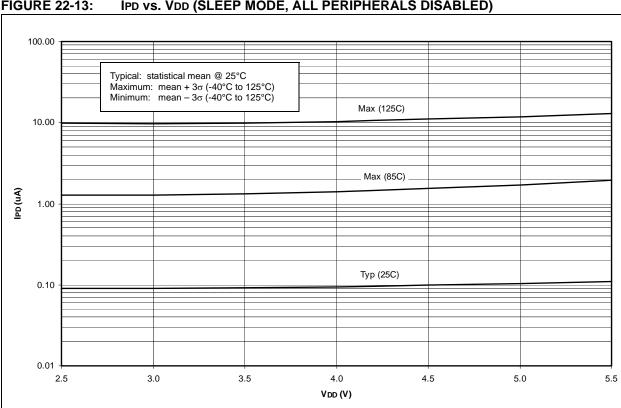


FIGURE 22-13: IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)



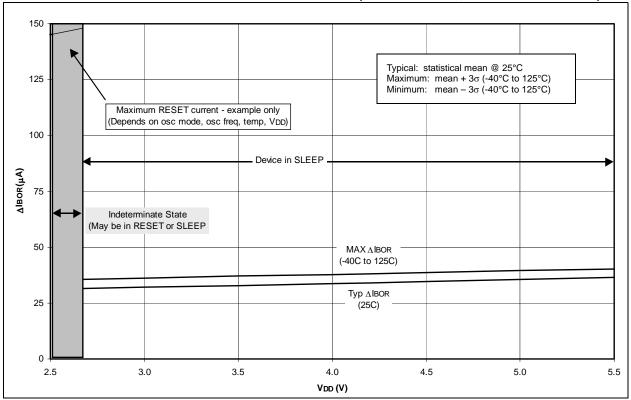


FIGURE 22-15: TYPICAL AND MAXIMUM ∆ITMR1 vs. VDD OVER TEMPERATURE (-40°C TO +125°C, TIMER1 WITH OSCILLATOR, XTAL=32 kHZ, C1 AND C2 = 47 pF)

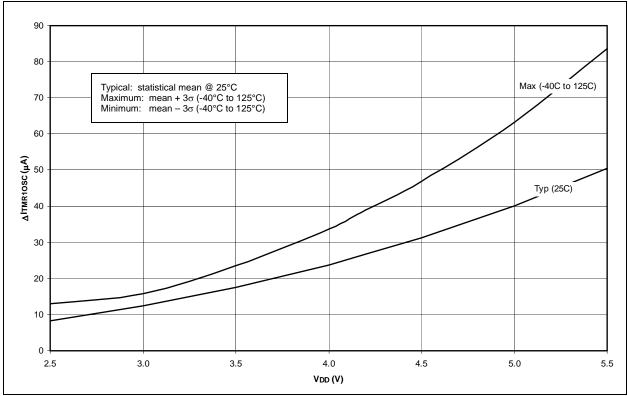
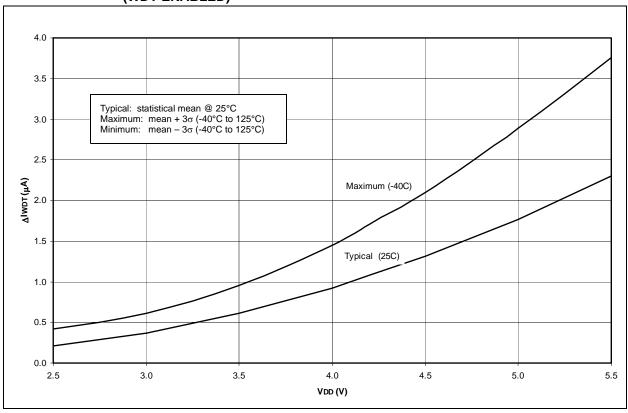
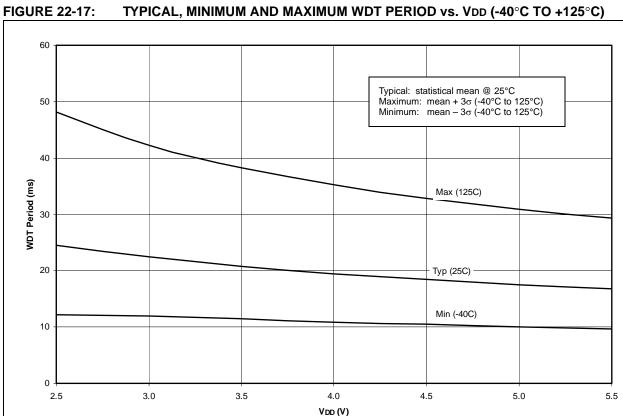
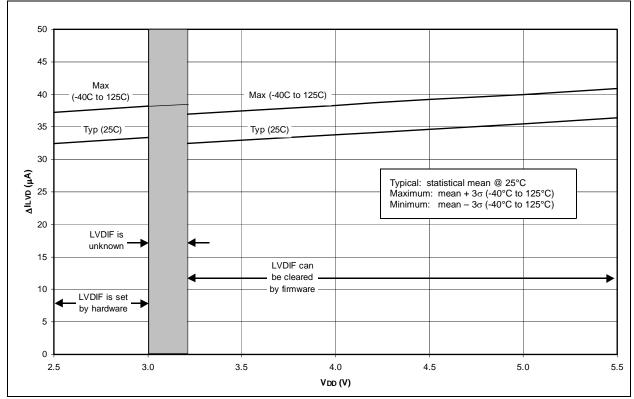


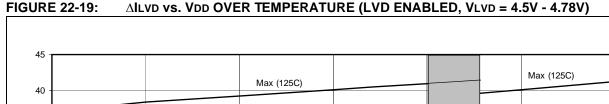
FIGURE 22-16: TYPICAL AND MAXIMUM AIWDT vs. VDD OVER TEMPERATURE (WDT ENABLED)











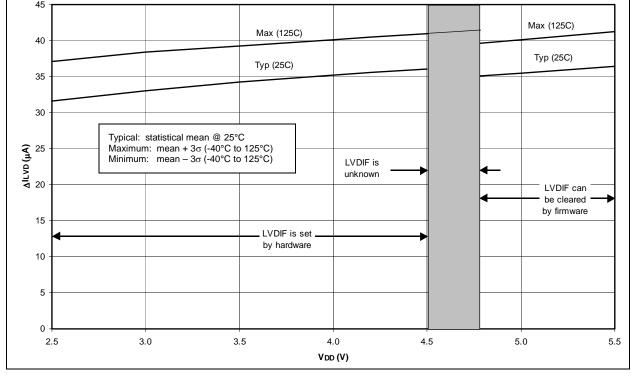
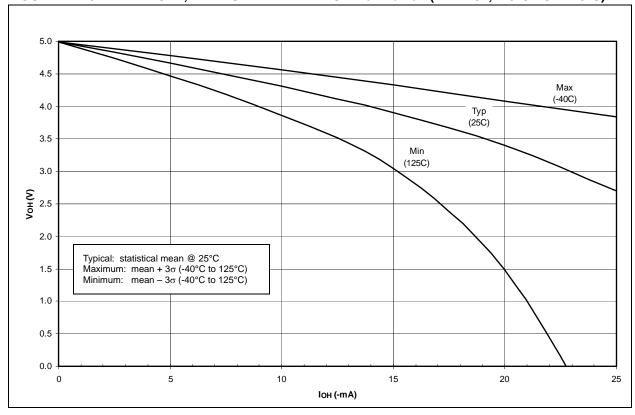
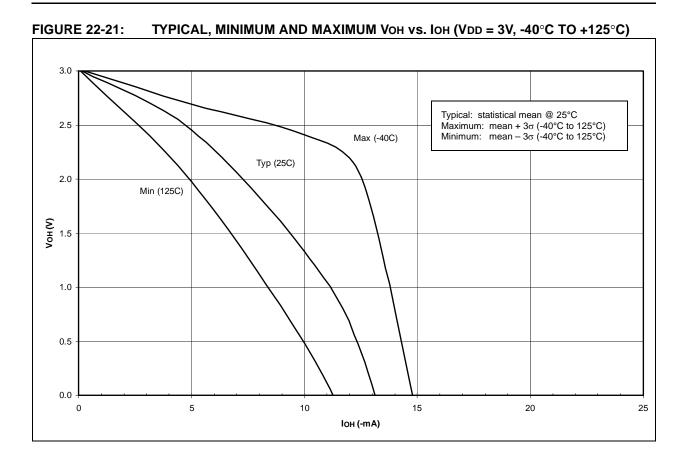


FIGURE 22-20: TYPICAL, MINIMUM AND MAXIMUM Voh vs. Ioh (VDD = 5V, -40°C TO +125°C)





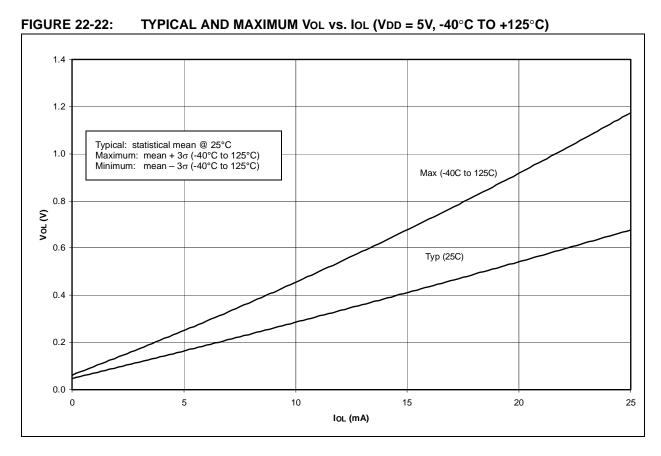


FIGURE 22-23: TYPICAL AND MAXIMUM Vol vs. lol (VDD = 3V, -40°C TO +125°C)

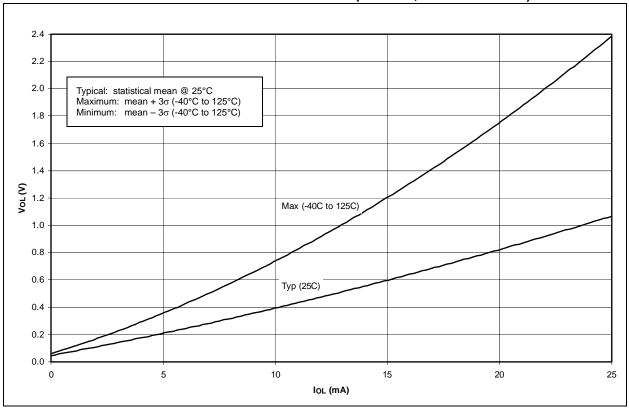
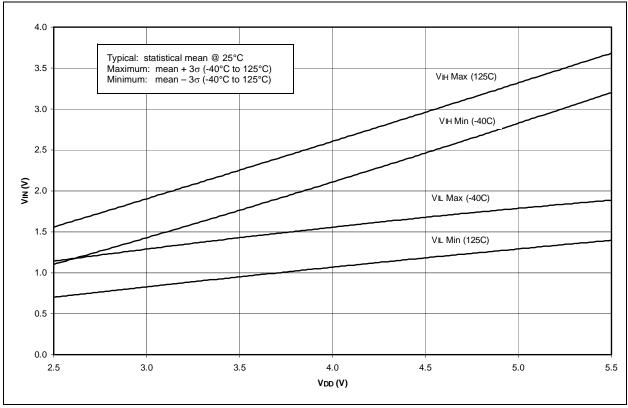
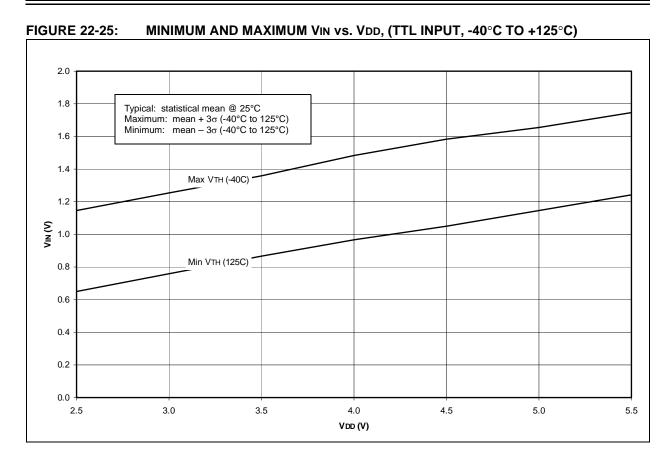
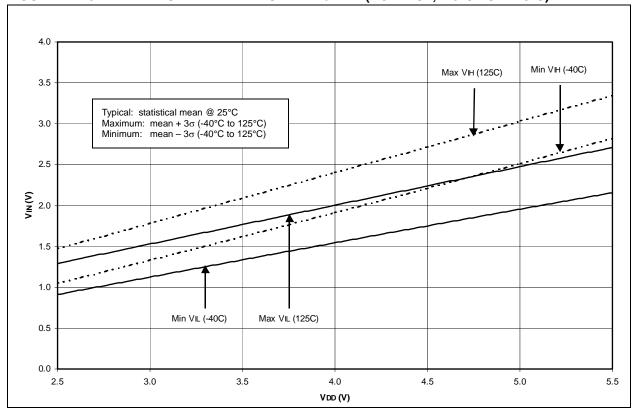


FIGURE 22-24: MINIMUM AND MAXIMUM VIN vs. VDD (ST INPUT, -40°C TO +125°C)









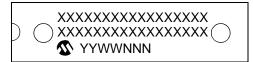
PIC18CXX2

NOTES:

23.0 PACKAGING INFORMATION

23.1 Package Marking Information

28-Lead PDIP (Skinny DIP)



Example



28-Lead SOIC



Example



Legend: XX...X Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
B Pb-free JEDEC designator for Matte Tin (Sn)
This package is Pb-free. The Pb-free JEDEC designator (e3)
can be found on the outer packaging for this package.

In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Cont'd)

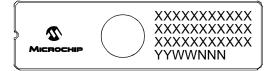
40-Lead PDIP



Example



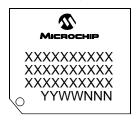
28- and 40-Lead JW (CERDIP)



Example



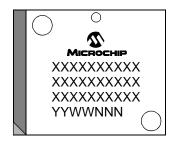
44-Lead TQFP



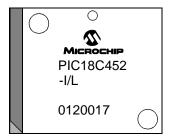
Example



44-Lead PLCC



Example

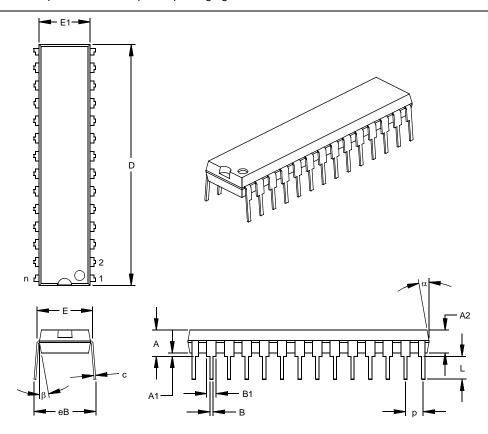


23.2 **Package Details**

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-line (SP) - 300 mil (PDIP)

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES*		MILLIMETERS			
Dimension I	imits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.140	.150	.160	3.56	3.81	4.06	
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.310	.325	7.62	7.87	8.26	
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49	
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65	
Lower Lead Width	В	.016	.019	.022	0.41	0.48	0.56	
Overall Row Spacing §	eВ	.320	.350	.430	8.13	8.89	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

Notes:

Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

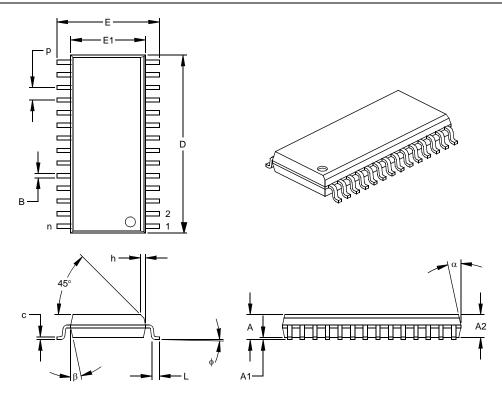
JEDEC Equivalent: MO-095

Drawing No. C04-070

^{*} Controlling Parameter § Significant Characteristic

28-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Units INCHES*			MILLIMETERS		
Dimension	Dimension Limits		NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	Е	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	Г	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	ф	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.013	0.23	0.28	0.33
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

Notes:

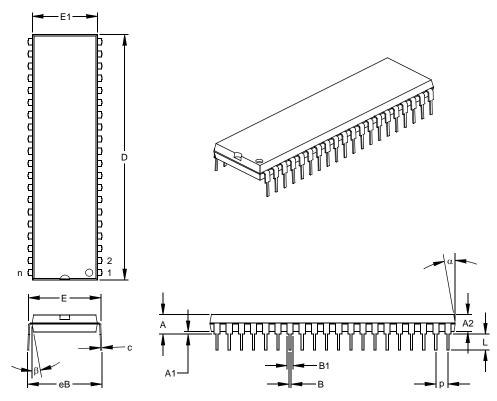
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-052

^{*} Controlling Parameter § Significant Characteristic

40-Lead Plastic Dual In-line (P) - 600 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimens	sion Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		40			40	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.530	.545	.560	13.46	13.84	14.22
Overall Length	D	2.045	2.058	2.065	51.94	52.26	52.45
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

^{*} Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.

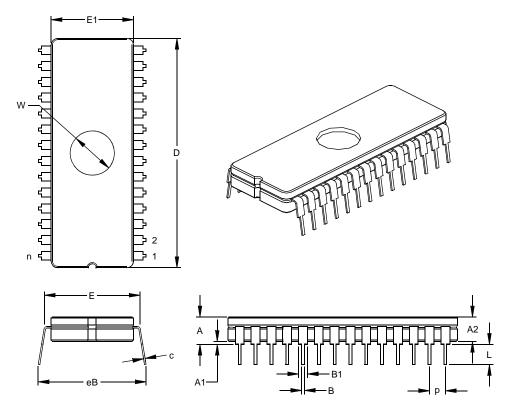
JEDEC Equivalent: MO-011

Drawing No. C04-016

[§] Significant Characteristic

28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

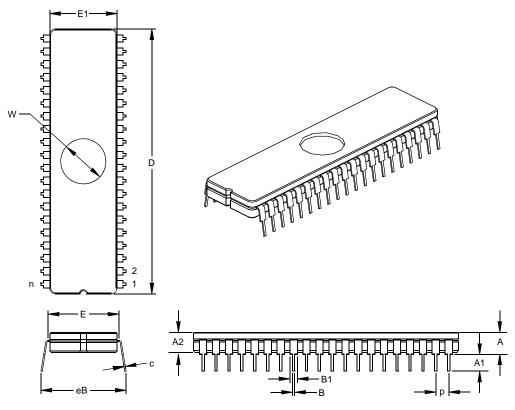


	Units		INCHES*			MILLIMETERS		
Dimension	on Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.195	.210	.225	4.95	5.33	5.72	
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19	
Standoff	A1	.015	.038	.060	0.38	0.95	1.52	
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88	
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36	
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85	
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81	
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30	
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65	
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58	
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03	
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37	

 ^{*}Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013

40-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

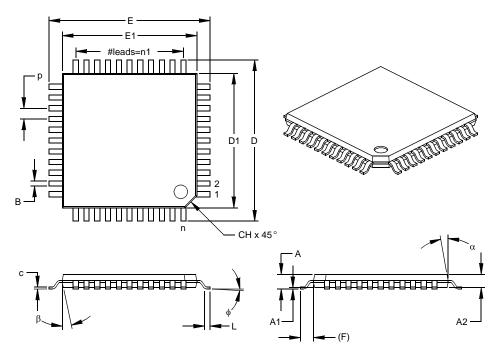


	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		40			40	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.185	.205	.225	4.70	5.21	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.030	.045	.060	0.76	1.14	1.52
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	2.040	2.050	2.060	51.82	52.07	52.32
Tip to Seating Plane	L	.135	.140	.145	3.43	3.56	3.68
Lead Thickness	С	.008	.011	.014	0.20	0.28	0.36
Upper Lead Width	B1	.050	.053	.055	1.27	1.33	1.40
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eВ	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.340	.350	.360	8.64	8.89	9.14

Controlling Parameter
 Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-014

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		MILLIMETERS*		
Dimensio	on Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	ф	0	3.5	7	0	3.5	7
Overall Width	Е	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

^{*} Controlling Parameter

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

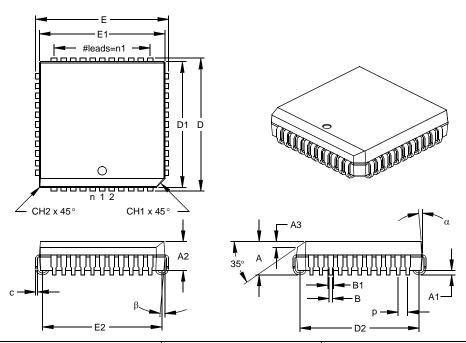
.010" (0.254mm) per side.
JEDEC Equivalent: MS-026

Drawing No. C04-076

[§] Significant Characteristic

44-Lead Plastic Leaded Chip Carrier (L) - Square (PLCC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.050			1.27	
Pins per Side	n1		11			11	
Overall Height	Α	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.024	.029	.034	0.61	0.74	0.86
Corner Chamfer 1	CH1	.040	.045	.050	1.02	1.14	1.27
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	Е	.685	.690	.695	17.40	17.53	17.65
Overall Length	D	.685	.690	.695	17.40	17.53	17.65
Molded Package Width	E1	.650	.653	.656	16.51	16.59	16.66
Molded Package Length	D1	.650	.653	.656	16.51	16.59	16.66
Footprint Width	E2	.590	.620	.630	14.99	15.75	16.00
Footprint Length	D2	.590	.620	.630	14.99	15.75	16.00
Lead Thickness	С	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	В	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.

JEDEC Equivalent: MO-047

Drawing No. C04-048

^{*} Controlling Parameter § Significant Characteristic

PIC18CXX2

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (July 1999)

Original data sheet for PIC18CXX2 family.

Revision B (March 2001)

Added DC and AC characteristics graphs (Section 22.0).

Revision C (January 2013)

Added a note to each package outline drawing.

TABLE 1: DEVICE DIFFERENCES

Feature	PIC18C242	PIC18C252	PIC18C442	PIC18C452
Program Memory (Kbytes)	16	32	16	32
Data Memory (Bytes)	512	1536	512	1536
A/D Channels	5	5	8	8
Parallel Slave Port (PSP)	No	No	Yes	Yes
Package Types	28-pin DIP 28-pin SOIC 28-pin JW	28-pin DIP 28-pin SOIC 28-pin JW	40-pin DIP 44-pin PLCC 44-pin TQFP 40-pin JW	40-pin DIP 44-pin PLCC 44-pin TQFP 40-pin JW

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table 1.

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18CXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18CXXX) is provided in AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442." The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18CXXX) is provided in AN726, "PIC17CXXX to PIC18CXXX Migration." This Application Note is available as Literature Number DS00726.

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- · Distributor or Representative
- · Local Sales Office
- Field Application Engineer (FAE)
- · Technical Support

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PIC18CXX2 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. Device	- <u>X /XX XXX</u> 	Examples: a) PIC18LC452 - I/P 301 = Industrial temp., PDIP package, 4 MHz, Extended VDD limits, QTP pattern #301. b) PIC18LC242 - I/SO = Industrial temp.,
Device	PIC18CXX2 ⁽¹⁾ , PIC18CXX2T ⁽²⁾ ; VDD range 4.2V to 5.5V PIC18LCXX2 ⁽¹⁾ , PIC18LCXX2T ⁽²⁾ ; VDD range 2.5V to 5.5V	solic package, Extended VDD limits. c) PIC18C442 - E/P = Extended temp., PDIP package, 40MHz, normal VDD limits.
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package	JW = Windowed CERDIP ⁽³⁾ PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny plastic dip P = PDIP L = PLCC	Note 1: C = Standard Voltage range LC = Wide Voltage Range 2: T = in tape and reel - SOIC, PLCC, and TQFP packages only. 3: JW Devices are UV erasable and can
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	be programmed to any device configu- ration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

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