PRELIMINARY

AMD

# Am79761

## Physical Layer 10-Bit Transceiver for Gigabit Ethernet (GigaPHY™-SD)

## DISTINCTIVE CHARACTERISTICS

- **Gigabit Ethernet Transceiver operates at 1.25 Gigabits per second (Gbps)**
- **Suitable for both Coaxial and Optical Link applications**
- **10-bit TTL Interface for Transmit and Receive Data**
- **Monolithic Clock Synthesis and Clock Recovery requires no external components**
- **Word Synchronization Function (Comma Detect)**
- **Low Power Operation - 700 mW typical**
- **64-pin Standard PQFP**
  - **— 14 x 14 mm (0˚ C - 70˚ C)**
  - **— 10 x 10 mm (0˚ C - 50˚ C)**
- **125 MHz TTL Reference Clock**
- **Loopback Diagnostic**
- **Single +3.3 V Supply**

## GENERAL DESCRIPTION

The Am79761 Gigabit Ethernet Physical Layer Serializer/Deserializer (GigaPHY-SD) device is a 1.25 Gbps Ethernet Transceiver optimized for Gigabit Ethernet/ 1000BASE-X applications. It implements the Physical Medium Attachment (PMA) layer for a single port.

The GigaPHY-SD device can interface to fiber-optic media to support 1000BASE-LX and 1000BASE-SX applications and can interface to copper coax to support 1000BASE-CX applications.

The functions performed by the device include serializing the 8B/10B 10-bit data for transmission, deserializing received code groups, recovering the clock from the incoming data stream, and word synchronization.

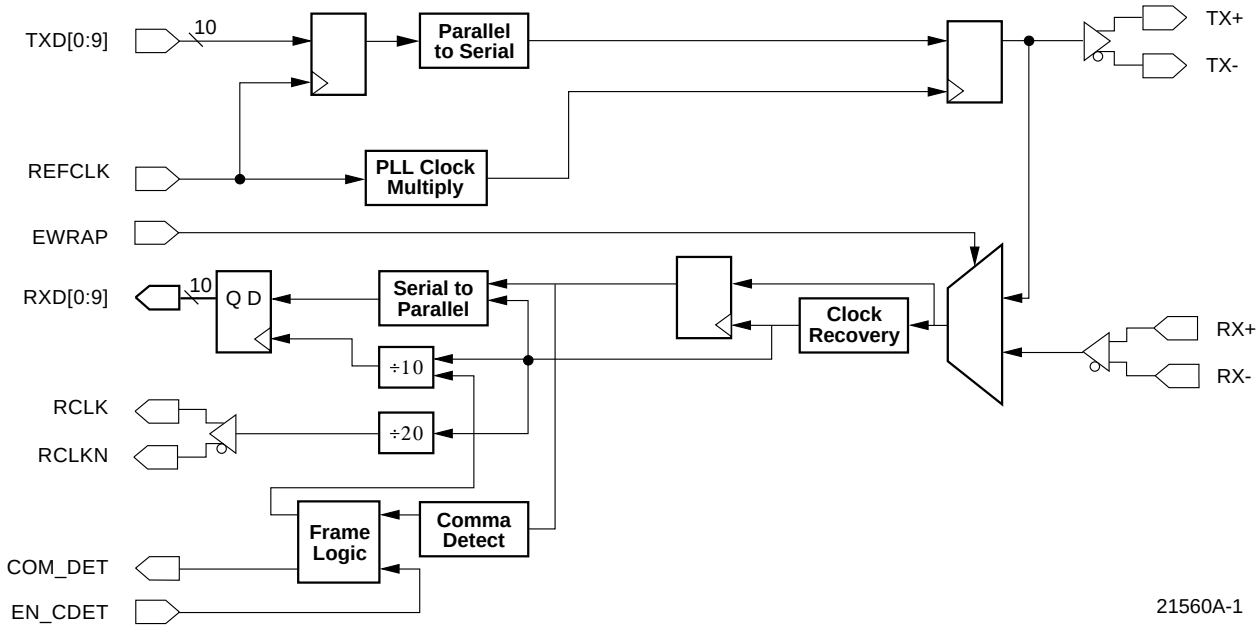
When transmitting, the GigaPHY-SD device receives 10-bit 8B/10B code groups at 125 million code groups per second. It then serializes the parallel data stream, adding a reference clock, and transmits it through the PECL drivers.

When receiving, the GigaPHY-SD device receives the PECL data stream from the network. It then recovers the clock from the data stream, deserializes the data stream into a 10-bit code group, and transmits it to the Physical Coding Sublayer (PCS) logic above. Optionally, it detects comma characters used to align the incoming word.

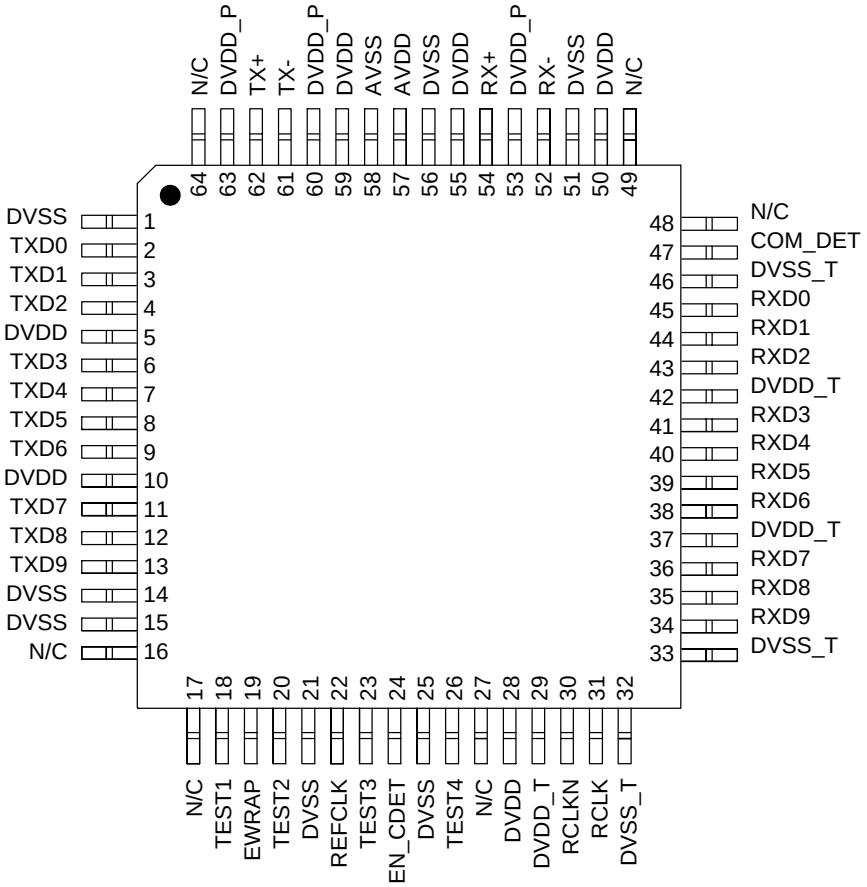
This document contains information on a product under development at Advanced Micro Devices. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

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Issue Date: **April 1998**

## BLOCK DIAGRAM



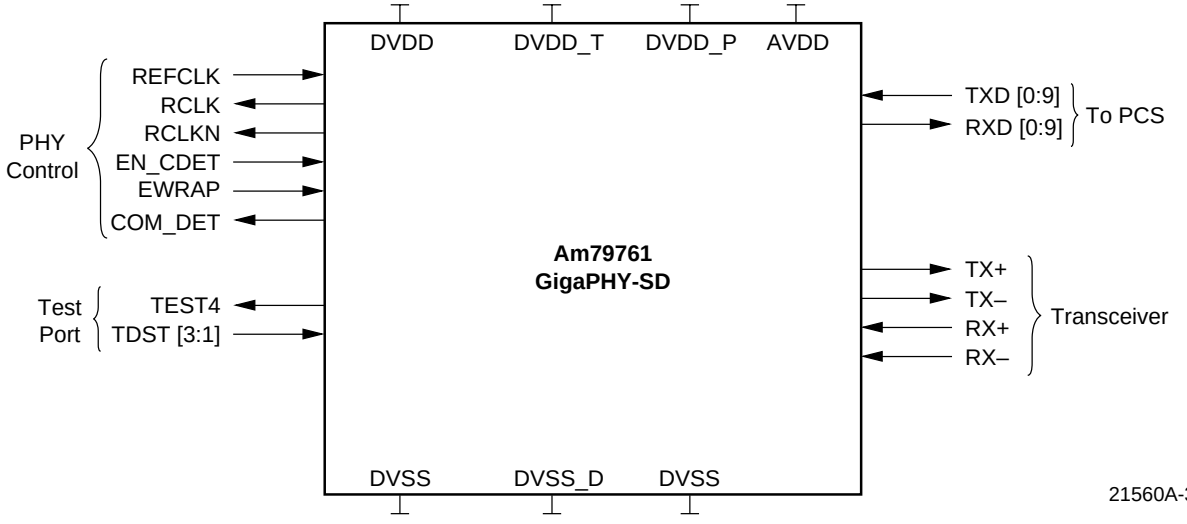
## CONNECTION DIAGRAM




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***Note:***
*N/C = No Connect*

## LOGIC SYMBOL

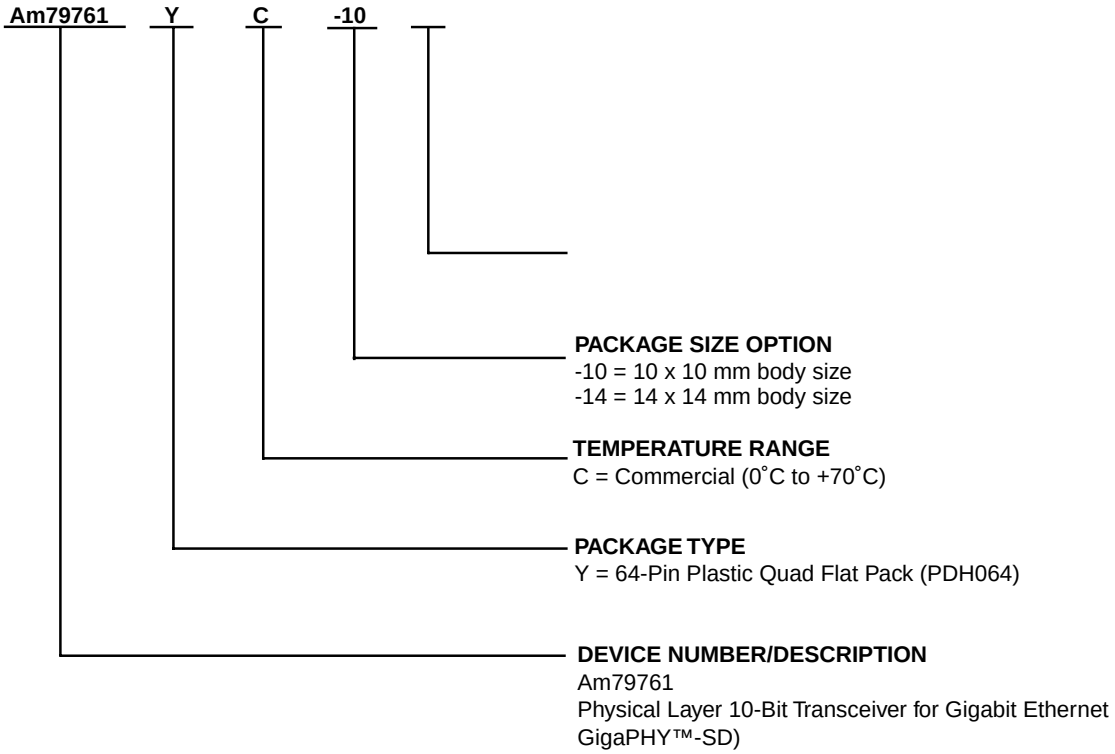



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## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.




| Valid Combinations | |
|---|---|
| Am79761YC | -10 |
| Am79761YC | -14 |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## RELATED PRODUCTS

| Part No. | Description |
|---|---|
| Am7990 | Local Area Network Controller for Ethernet (LANCE) |
| Am7992B | Serial Interface Adapter (SIA) |
| Am7996 | IEEE 802.3/Ethernet/Cheapernet Transceiver |
| Am79C90 | CMOS Local Area Network Controller for Ethernet (C-LANCE) |
| Am79C98 | Twisted Pair Ethernet Transceiver (TPEX) |
| Am79C100 | Twisted Pair Ethernet Transceiver Plus (TPEX+) |
| Am79C871 | Quad Fast Ethernet Transceiver for 100BASE-X Repeaters (QFEXr™) |
| Am79C981 | Integrated Multiport Repeater Plus (IMR+™) |
| Am79C982 | basic Integrated Multiport Repeater (bIMR™) |
| Am79C983 | Integrated Multiport Repeater 2 (IMR2™) |
| Am79C984A | enhanced Integrated Multiport Repeater (eIMR™) |
| Am79C985 | enhanced Integrated Multiport Repeater Plus (eIMR+™) |
| Am79C987 | Hardware Implemented Management Information Base (HIMIB™) |
| Am79C988A | Quad Integrated Ethernet Transceiver (QuIET™) |
| Am79C900 | Integrated Local Area Communications Controller (ILACC™) |
| Am79C940 | Media Access Controller for Ethernet (MACE™) |
| Am79C960 | PCnet™-ISA Single-Chip Ethernet Controller (for ISA bus) |
| Am79C961 | PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support) |
| Am79C961A | PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA |
| Am79C965 | PCnet™-32 Single-Chip 32-Bit Ethernet Controller |
| Am79C970 | PCnet™-PCI Single-Chip Ethernet Controller (for PCI bus) |
| Am79C970A | PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus) |
| Am79C971 | PCnet™-*FAST* Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus |

## PIN DESIGNATION

## Listed by Pin Number

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | DVSS | 17 | N/C | 33 | DVSS_T | 49 | N/C |
| 2 | TXD0 | 18 | TEST1 | 34 | RXD9 | 50 | DVDD |
| 3 | TXD1 | 19 | EWRAP | 35 | RXD8 | 51 | DVSS |
| 4 | TXD2 | 20 | TEST2 | 36 | RXD7 | 52 | RX- |
| 5 | DVDD | 21 | DVSS | 37 | DVDD_T | 53 | DVDD_P |
| 6 | TXD3 | 22 | REFCLK | 38 | RXD6 | 54 | RX+ |
| 7 | TXD4 | 23 | TEST3 | 39 | RXD5 | 55 | DVDD |
| 8 | TXD5 | 24 | EN_CDET | 40 | RXD4 | 56 | DVSS |
| 9 | TXD6 | 25 | DVSS | 41 | RXD3 | 57 | AVDD |
| 10 | DVDD | 26 | TEST4 | 42 | DVDD_T | 58 | AVSS |
| 11 | TXD7 | 27 | N/C | 43 | RXD2 | 59 | DVDD |
| 12 | TXD8 | 28 | DVDD | 44 | RXD1 | 60 | DVDD_P |
| 13 | TXD9 | 29 | DVDD_T | 45 | RXD0 | 61 | TX- |
| 14 | DVSS | 30 | RCLKN | 46 | DVSS_T | 62 | TX+ |
| 15 | DVSS | 31 | RCLK | 47 | COM_DET | 63 | DVDD_P |
| 16 | N/C | 32 | DVSS_T | 48 | N/C | 64 | N/C |

## PIN DESCRIPTION

**TX+, TX-**
**Serial Transmit Data**
**PECL Output**

These pins are the 1000BASE-X port differential drivers which transmit the serial stream to the network. These pins are connected to the copper or fiber optic connectors.

When EWRAP is LOW, the pins assume normal operation. When HIGH, TX+ is logic HIGH and TX- is logic LOW.

**RX+, RX-**
**Serial Receive Data**
**PECL Input**

These pins are the 1000BASE-X port differential receiver pair, receiving a serial stream of data from the network. These pins are connected to the copper or fiber optic connectors.

When EWRAP is LOW, the pins assume normal operation. The pins are internally biased.

**TXD[0:9]**
**Transmit Data**
**TTL Input**

The TXD[0:9] pin is a set of 10 data signals which are driven from the Physical Coding Sublayer (PCS) above. The 10 bits of data are clocked in parallel on the rising edge of REFCLK. TXD0 is transmitted first on TX±.

**RXD[0:9]**
**Receive Data**
**TTL Output**

The RXD[0:9] pin is a set of 10 data signals which are sent to the Physical Coding Sublayer (PCS) above. The 10 bits of data are clocked out in parallel on the rising edges of RCLK and RCLKN. RXD0 is received first on RX±.

**REFCLK**
**Reference Clock**
**TTL Input**

This input is used for the 125-Mhz clock. The rising edge of this clock latches TXD[0:9] into an input register. This clock serves as the reference clock at 1/10th the baud rate for the PLL.

**RCLK, RCLKN**
**Receive Clock**
**TTL Output**

These pins provide the differential receive clock signals, derived from the RX± data stream, and are at 1/20th the baud rate of the receive stream. Parallel data on RXD[0:9] is provided at each rising transition of RCLK and RCLKN.

**EN_CDET**
**Enable Comma Detect**
**TTL Input**

This pin is used to enable the word synchronization mode. When logic HIGH, the COM_DET output is enabled and word synchronization is active.

**COM_DET**
**Comma Detect Indicator**
**TTL Output**

Comma Detect is asserted to indicate that the incoming word on RXD[0:9] contains a Comma character (0011111xxx). COM_DET goes HIGH for half of a RCLK period, and can be captured when RCKLN is rising.

In order for COM_DET to provide indication, EN_CDET must be enabled (logic HIGH).

**EWRAP**
**Loopback Enable**
**TTL Input**

When EWRAP is asserted, the transmitted data stream is sent back to the receiver through an internal loopback path. TX+ is logic HIGH, and TX- is logic LOW in this mode.

This pin is logic LOW for normal operation.

**TEST[1:3]**
**Factory Test Pins**
**Input**

These pins should be tied to DVDD for normal operation.

**TEST[4]**
**Factory Test Pin**
**Output**

This pin should be left unconnected for normal operation.

**DVDD**
**Power**

These pins supply power to the digital blocks of the device. They must be connected to a 3.3 V ±5% source.

**DVDD_T**
**TTL Power**

These pins supply power to the TTL blocks of the device. They must be connected to a 3.3 V ±5% source.

**DVDD_P**
**PECL Power**

These pins supply power to the PECL blocks of the device. They must be connected to a 3.3 V ±5% source. It is critical that the signal supplied to these pins are clean to ensure good performance of the device.

**AVDD**
**Analog Power**

These pins supply power to the analog blocks of the device. They must be connected to a 3m.3 V ±5% source and require careful decoupling to ensure proper device performance.

**DVSS**
**Ground**

These pins are the ground connections for the digital blocks. They must be connected to the common external ground plane.

**DVSS_T**
**Ground**

These pins are the ground connections for the TTL blocks. They must be connected to the common external ground plane.

**AVSS**
**Ground**

These pins are the ground connections for the analog blocks. They must be connected to an analog ground plane.

# FUNCTIONAL DESCRIPTION

## Overview

The GigaPHY-SD device provides the PMA functionality for 1000BASE-X systems. The GigiaPHY-SD communicates with the PCS through the 10-bit code groups and communicates with the Physical Medium Dependent (PMD) layer to transmit and receive data from the network, through either fiber optic or copper coax media.

The GigaPHY-SD device consists of the following functional blocks:

- 1000BASE-X Transmit block including:
  - — Clock Synthesizer
  - — Serializer and Transmission interface
- 1000BASE-X Receive block including:
  - — Clock Recovery
  - — Deserializer
  - — Word Alignment and synchronization

## Clock Synthesizer

The Am79761 clock synthesizer multiplies the reference frequency provided on the REFCLK pin by 10 to achieve a baud rate clock at nominally 1.25 GHz. The clock synthesizer contains a fully monolithic PLL which does not require any external components.

## Serializer

The Am79761 device accepts TTL input data as a parallel 10-bit character on the TXD[0:9] bus which is latched into the input latch on the rising edge of REFCLK. This data will be serialized and transmitted on the TX PECL differential outputs at a baud rate of ten times the frequency of the REFCLK input, with bit TXD0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the IEEE 802.3 specification.

## Transmission Character Interface

An encoded byte is 10 bits and is referred to as a transmission character. The 10-bit interface on the Am79761 device corresponds to a transmission character. This mapping is shown in Table 20.

**Table 20. Transmission Order and Mapping of an 8B/10B Character**

| Parallel Data Bits | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 8B/10B Bit Position | j | h | g | f | i | e | d | c | b | a |
| Comma Character | X | X | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

Last Data Bit Transmitted ↑ First Data Bit Transmitted ↑

## Clock Recovery

The Am79761 device accepts differential high speed serial inputs on the RX± pins, extracts the clock and retimes the data. The Am79761 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 0.01% of ten times the REFCLK frequency. For example, if the REFCLK used is 125 MHz, then the incoming serial baud rate must be 1.25 gigabaud ±0.01 percent.

## Deserializer

The re-timed serial bit stream is converted into a 10-bit parallel output character. The Am79761 device provides complementary TTL recovered clocks, RCLK and RCLKN, which are at 1/20th of the serial baud rate. This architecture is designed to simplify demultiplexing of the 10-bit data characters into a 20-bit half-word in the downstream controller chip. The clocks are generated by dividing down the high-speed clock which is phase locked to the serial data. The serial data is re-timed by the internal high-speed clock and deserialized.

The resulting parallel data will be captured by the adjoining protocol logic on the rising edges of RCLK and RCLKN. In order to maximize the setup and hold times available at this interface, the parallel data is loaded into the output register at a point nominally midway between the transition edges of RCLK and RCLKN.

If serial input data is not present or does not meet the required baud rate, the Am79761 will continue to produce a recovered clock so that downstream logic may continue to function. The RCLK and RCLKN output frequency under these circumstances may differ from their expected frequency by no more than ±1 percent.

## Word Alignment

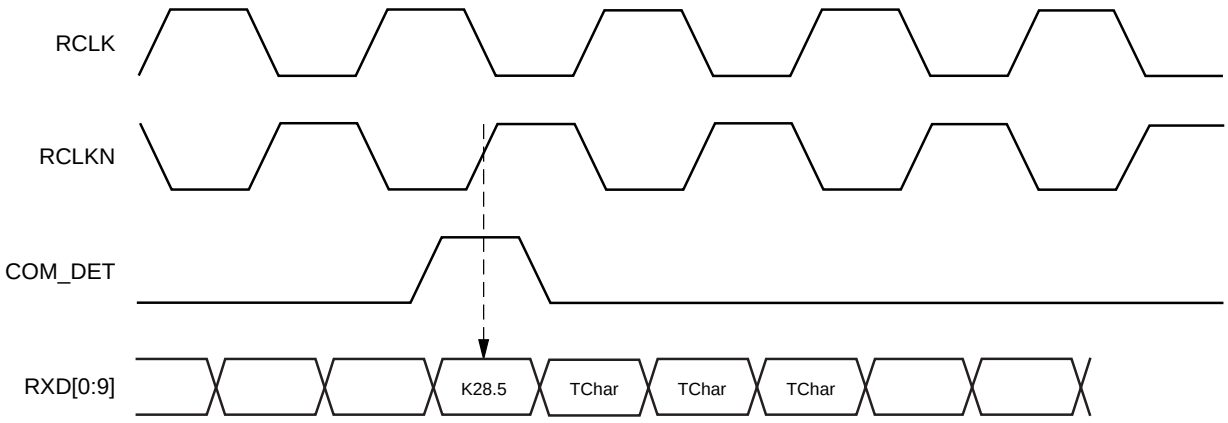
The Am79761 device provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the Am79761 device constantly examines the serial data for the presence of the Comma character. This pattern is 0011111XXX, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5, and K28.7, which are defined specifically for synchronization purposes. Improper alignment of the comma character is defined as any of the following conditions:

1. The comma is not aligned within the 10-bit transmission character such that TXD0...TXD6 = "0011111."
2. The comma straddles the boundary between two 10-bit transmission characters.
3. The comma is properly aligned but occurs in the received character presented during the rising edge of RCLK rather than RCLKN.

When EN_CDET is HIGH and an improperly aligned comma is encountered, the internal data is shifted in such a manner that the comma character is aligned properly in RXD[0:9]. This results in proper character and half-word alignment. When the parallel data alignment changes in response to an improperly aligned comma pattern, some data which would have been presented on the parallel output port may be lost. However, the synchronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

When encountering a comma character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the comma character and has a duration equal to the data, or half of an RCLK period. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RCLKN. Functional waveforms for synchronization are given in Figure 18 and Figure 19.

Figure 18 shows the case when a comma character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the comma character on RXD[0:9]. Figure 19 shows the case where K28.5 is detected, but it is out of phase and a change in the output data alignment is required. Note that up to three characters prior to the comma character may be corrupted by the realignment process.




*Note : TChar = 10-bit Transmission Character*

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**Figure 18. Detection of a Properly Aligned Comma Character**

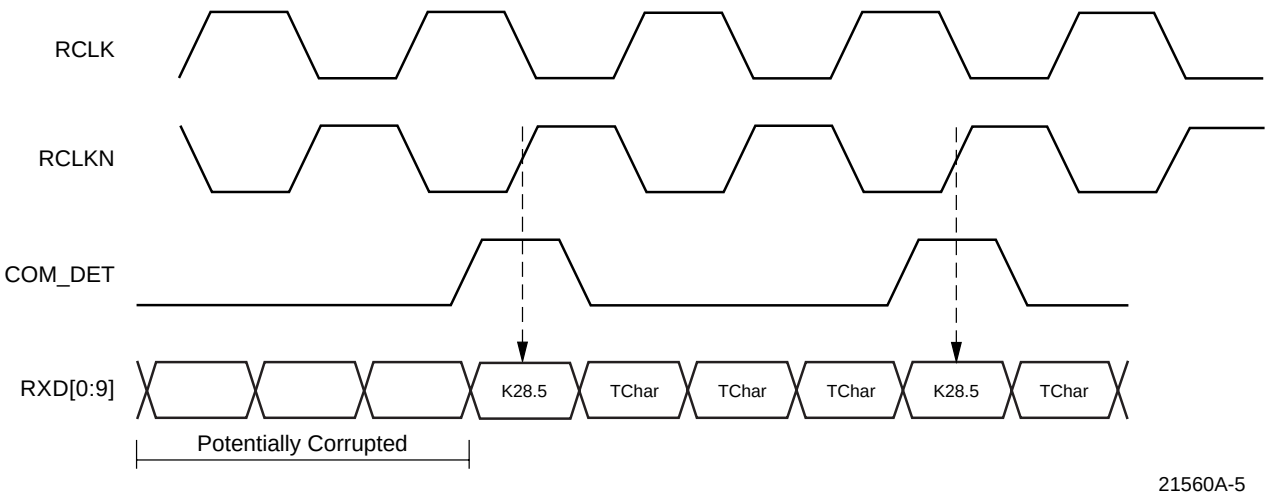



**Figure 19. Receiving Two Consecutive K28.5 + TCharacter Transmission Words**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . .-65° C to +150° C

Ambient Temperature Under Bias . .-55° C to +125° C

Power Supply Voltage ($V_{DD}$) . . . . . -0.5 V to +4.0 V

DC Voltage (PECL Inputs) . . . . . .-0.5 V to $V_{DD}$ +0.5 V

DC Voltage (TTL Inputs). . . . . -0.5 V to +5.5 V

Output Current (TTL Outputs) . . . . . .-±50 mA

Output Current (PECL Outputs). . . . . .-±50 mA

Maximum Input ESD (Human Body Model) . . . 1500 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature ($T_A$) 0° C to +70° C for 14 x 14 mm PQFP

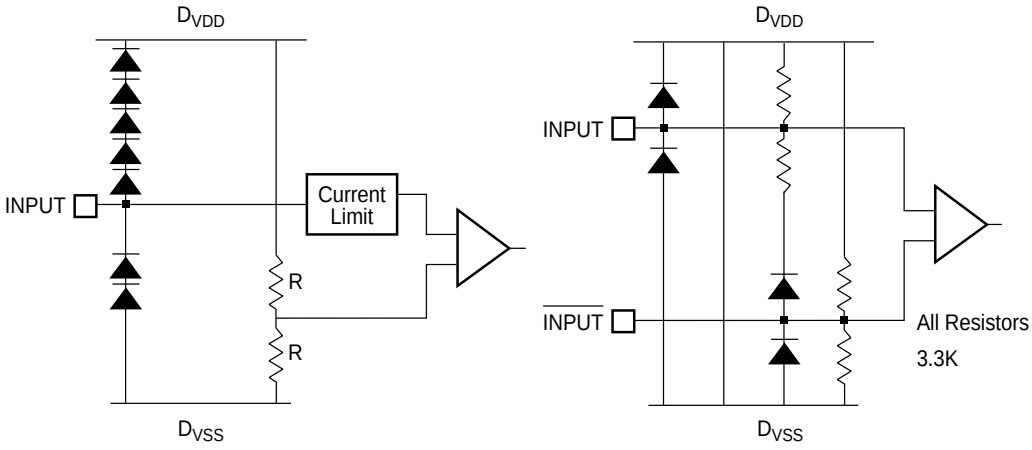
. . . . . 0° C to +50° C for 10 x 10 mm PQFP

Power Supply Voltage ($D_{VDD}$) . . . . . +3.3 V ±5%

*Operating ranges define those limits between which functionality of the device is guaranteed.*

## DC CHARACTERISTICS (over recommended operating conditions)

| Symbol | Parameter Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH voltage (TTL) | | 2.0 | — | 5.5 | V |
| $V_{IL}$ | Input LOW voltage (TTL) | | 0 | — | 0.8 | V |
| $I_{IH}$ | Input HIGH current (TTL) | $V_{IN}$ =2.4 V | — | 50 | 500 | µA |
| $I_{IL}$ | Input LOW current (TTL) | $V_{IN}$ =0.5 V | — | — | -500 | µA |
| $V_{OH}$ | Output HIGH voltage (TTL) | $I_{OH}$ = -1.0 mA | 2.4 | — | — | V |
| $V_{OL}$ | Output LOW voltage (TTL) | $I_{OL}$ = +1.0 mA | — | — | 0.5 | V |
| $\Delta V_{OUT75}$ | TX Output differential peak-to-peak voltage swing | 75 Ω to $V_{DD}$ – 2.0 V | 1200 | — | 2200 | mVp-p |
| $\Delta V_{OUT50}$ | TX Output differential peak-to-peak voltage swing | 50 Ω to $V_{DD}$ – 2.0 V | 1200 | — | 2200 | mVp-p |
| $\Delta V_{IN}$ | Receiver differential peak-to-peak Input Sensitivity RX | Internally biased to $V_{DD}$/2 | 400 | — | 3200 | mVp-p |
| $I_{DD}$ | Supply Current | Outputs open, $V_{DD}$ = $V_{DD}$ max | — | 210 | 290 | mA |
| $P_D$ | Power dissipation | Outputs open, $V_{DD}$ = $V_{DD}$ max | — | 700 | 1000 | mW |




**REFCLK and TTL Inputs**

**A**

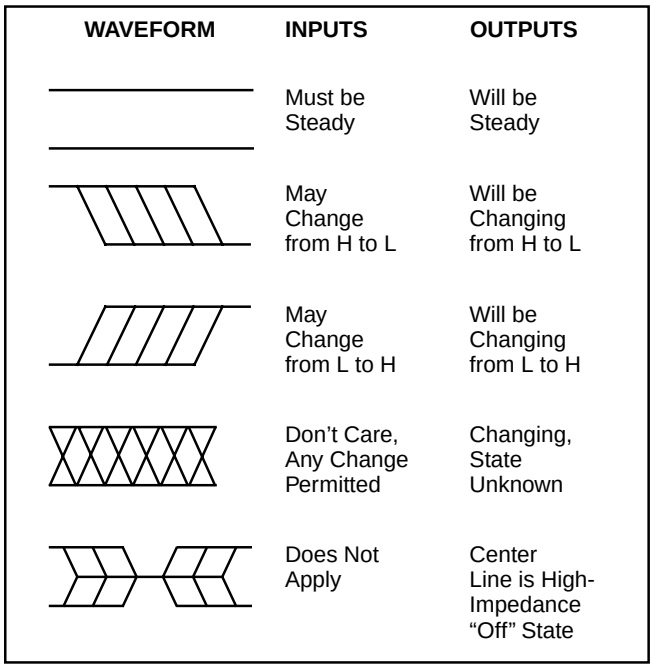
**High Speed Differential Input (RX±)**

**B**

21560A-6

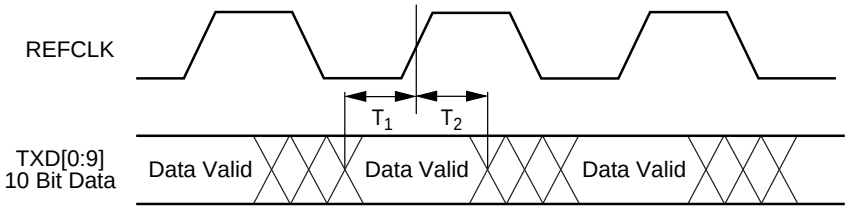
**Figure 20. Input Structures**

## KEY TO SWITCHING WAVEFORMS




KS000010-PAL

## AC CHARACTERISTICS




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**Figure 21. Transmit Timing Waveforms**

**Table 21. Transmit AC Characteristics**

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_1$ | TXD[0:9] Setup time to the rising edge of REFCLK | Measured between the valid data level of TXD[0:9] to the 1.4 V point of REFCLK | 1.5 | — | ns |
| $T_2$ | TXD[0:9] hold time after the rising edge of REFCLK | | 1.0 | — | ns |
| $T_{SDR}$, $T_{SDF}$ | TX± rise and fall time | 20% to 80%, 75 Ω load to $V_{SS}$, Tested on a sample basis | — | 300 | ps |
| $T_{LAT}$ | Latency from rising edge of REFCLK to TXD0 appearing on TX±- | bc = Bit clocks<br>ns = Nano second | 11bc - 1ns | — | — |

## AC CHARACTERISTICS (Continued)

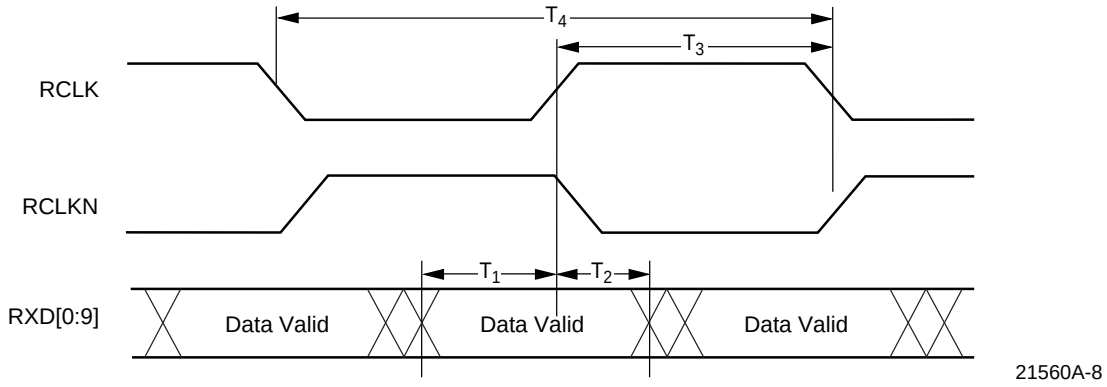



**Figure 22. Receive Timing Waveform**

**Table 22. Receive AC Characteristics**

| Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_1$ | Data or COM_DET Valid prior to RCLK/RCLKN rise | Measured between the 1.4 V point of RCLK or RCLKN and a valid level of RXD[0:9]. All outputs driving 10 pF load. | 3.0 | — | ns |
| $T_2$ | Data or COM_DET Valid after RCLK or RCLKN rise | | 2.0 | — | ns |
| $T_3$ | Deviation of RCLK rising edge to RCLKN rising edge delay from nominal. $delay = \frac{f_{baud}}{10} \pm T_3$ | Nominal delay is 10 bit times. Tested on sample basis | -500 | 500 | ps |
| $T_4$ | Deviation of RCLK, RCLKN frequency from nominal. $f_{RCLK} = \frac{f_{REFCLK}}{2} \pm T_4$ | Whether or not locked to serial data | -1.0 | 1.0 | % |
| $T_R$, $T_F$ | RXD[0:9], COM_DET, RCLK, RCLKN rise and fall time | Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$, into 10 pf load. | — | 2.4 | ns |
| $R_{lat}$ | Latency from RX± to RXD[0:9] | bc = Bit clock<br>ns = Nano second | 15 bc + 2 ns | 34 bc + 2 ns | — |
| $T_{LOCK}$ | Data acquisition lock time @ 1.25 Gbps | 8B/10B IDLE pattern.<br>Tested on a sample basis | — | 2.0 | µs |
| Receive Data Jitter | Receive Data Jitter Power $\int_{100KHz}^{\frac{1}{2 \times BitTime}} PhaseNoise$ | dBc, RMS for $10^{-12}$ Bit Error Ratio Tested on a sample basis | — | 40 | ps |

## REFERENCE CLOCK REQUIREMENTS

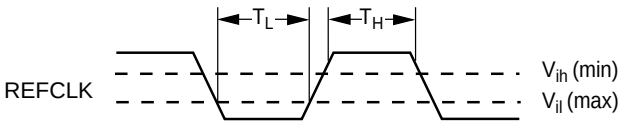


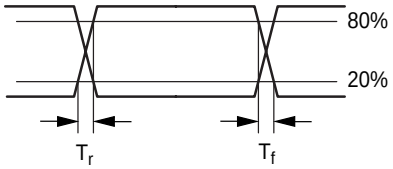

**Figure 23. REFCLK Timing Waveform**

**Table 23. Reference Clock Requirements**

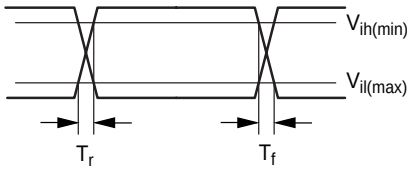
| Symbol | Parameter Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| FR | Frequency Range | Range over which both transmit and receive reference clocks on any link may be centered | 123 | 127 | MHz |
| FO | Frequency Offset | Maximum frequency offset between transmit and receive reference clocks on one link | -200 | 200 | ppm |
| DC | REFCLK duty cycle | Measured at 1.5 V | 30 | 70 | % |
| $T_{RCR}$,$T_{RCF}$ | REFCLK rise and fall time | Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ | — | 1.0 | ns |

## MEASUREMENTS

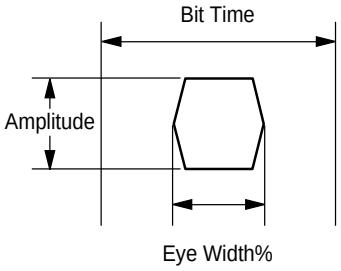
**Serial Input Rise and Fall Time**




**TTL Input and Output Rise and Fall Time**

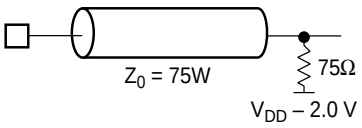



**Receiver Input Eye Diagram Jitter Tolerance Task Mask**

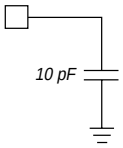



**Parametric Test Load Circuit**

**Serial Output Load**




**TTL AC Output Load**

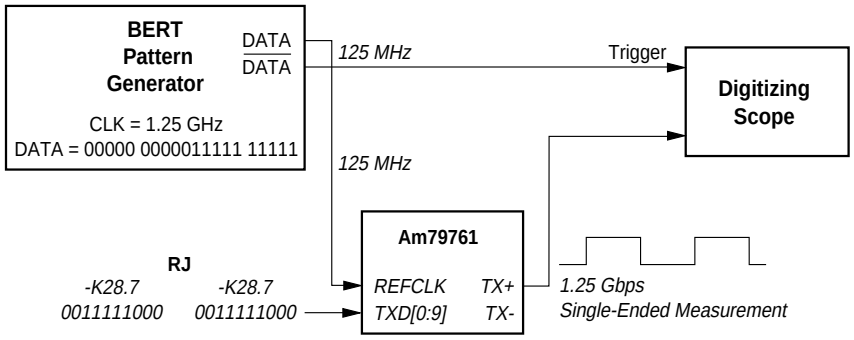



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**Figure 24. Parametric Measurement Information**

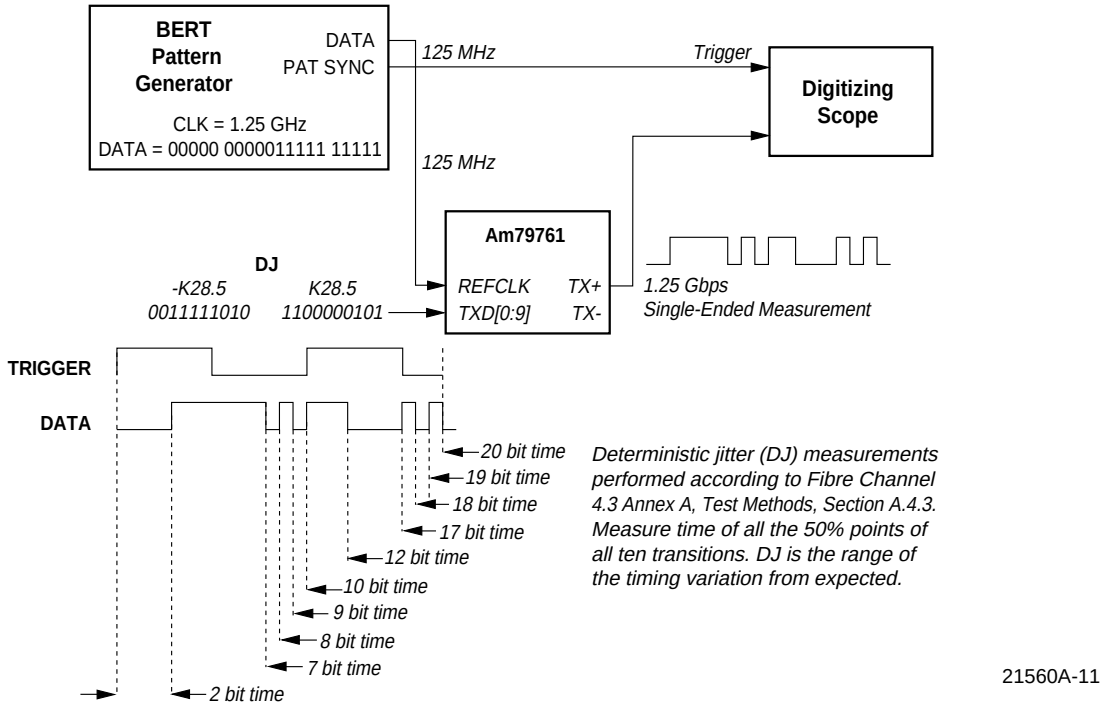
## MEASUREMENTS (Continued)

**Random Jitter Measurement**




*Random jitter (RJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.4. Measure standard deviation of all 50% crossing points. Peak to peak RJ is ±7 sigma of distribution.*

**Deterministic Jitter Measurement**




*Deterministic jitter (DJ) measurements performed according to Fibre Channel 4.3 Annex A, Test Methods, Section A.4.3. Measure time of all the 50% points of all ten transitions. DJ is the range of the timing variation from expected.*

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**Figure 25. Transmitter Jitter Measurement Method**

| **Transmitter Output Jitter Allocation** | | | | | |
|---|---|---|---|---|---|
| $T_{rj}$ | Serial data output random jitter (RMS) | RMS, tested on a sample basis (refer to Figure 8) | — | 20 | ps |
| $T_{DJ}$ | Serial data output deterministic jitter (p-p) | Peak to peak, tested on a sample basis (refer to Figure 8) | — | 100 | ps |

## THERMAL CONSIDERATIONS

The Am79761 is packaged in a 14-mm or a 10-mm conventional PQFP with an internal heat spreader. These packages use an industry-standard EIAJ footprint, but have been enhanced to improve thermal dissipation. The construction of the packages are as shown in Figure 26.

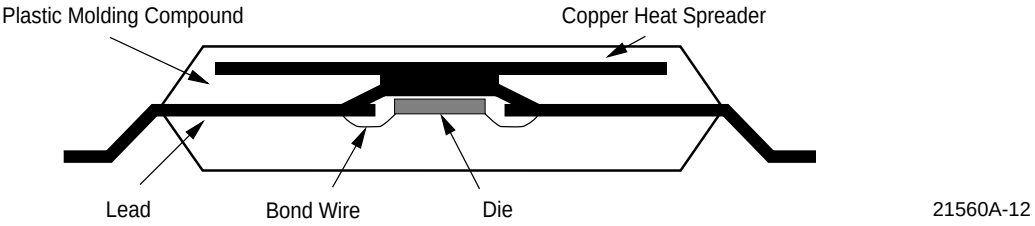



**Figure 26. Package Cross Section**

**Table 24. Thermal Resistance**

| Symbol | Description | 10 mm Value | 14 mm Value | Units |
|---|---|---|---|---|
| $\theta_{jc}$ | Thermal resistance from junction to case | 10.0 | 9.5 | $^{o}$C/W |
| $\theta_{ca}$ | Thermal resistance from case to ambient in still air including conduction through the leads. | 50.8 | 29 | $^{o}$C/W |
| $\theta_{ca\text{-}100}$ | Thermal resistance from case to ambient with 100 LFM airflow | 41.2 | 26.1 | $^{o}$C/W |
| $\theta_{ca\text{-}200}$ | Thermal resistance from case to ambient with 200 LFM airflow | 36.9 | 23.8 | $^{o}$C/W |
| $\theta_{ca\text{-}400}$ | Thermal resistance from case to ambient with 400 LFM airflow | 31.8 | 20.5 | $^{o}$C/W |
| $\theta_{ca\text{-}600}$ | Thermal resistance from case to ambient with 600 LFM airflow | 27.8 | 17.9 | $^{o}$C/W |

The Am79761 is designed to operate with a junction temperature up to 105$^{o}$C. The user must guarantee that the temperature specification is not violated. With the Thermal Resistances shown above, the 10x10 PQFP can operate in still air ambient temperatures of 50$^{o}$C, while the 14x14 PQFP can operate in still air ambient temperatures of 72$^{o}$C. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

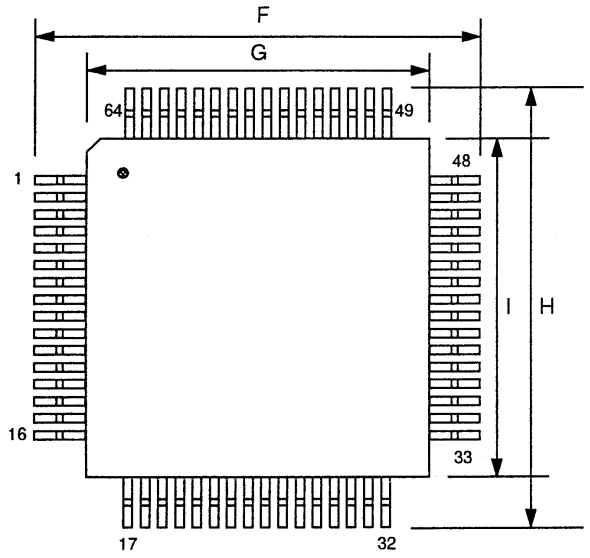
***Notes:***

1. *$50^{o}C=110^{o}C\text{-}1W*(10^{o}C/W+50.8^{o}C/W)$*
2. *$72^{o}C=110^{o}C\text{-}1W*(95^{o}C/W+29^{o}C/W)$*

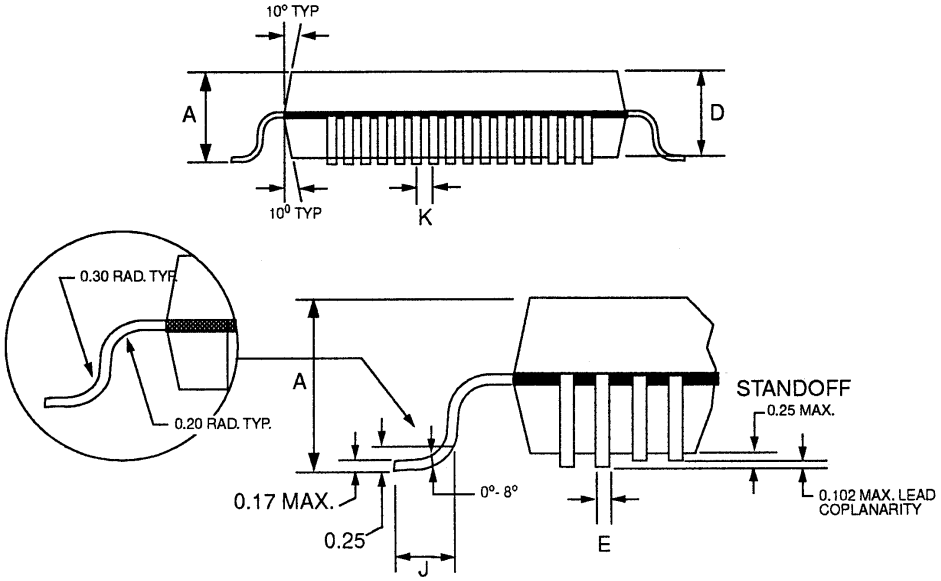
## PHYSICAL DIMENSIONS

## PDH064

## 64-Pin (measured in millimeters)




| Item | 10 mm | 14 mm | Tol. |
|---|---|---|---|
| A | 2.45 | 2.45 | MAX |
| D | 2.00 | 2.00 | +0.10 |
| E | 0.30 | 0.35 | ±.05 |
| F | 13.20 | 17.20 | ±.25 |
| G | 10.00 | 14.00 | ±.10 |
| H | 13.20 | 17.20 | ±.25 |
| I | 10.00 | 14.00 | ±.10 |
| J | 0.88 | 0.80 | ±.15 |
| K | 0.50 | 0.80 | BASIC |




*Drawing not to scale.*
*All units in mm unless otherwise noted.*

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