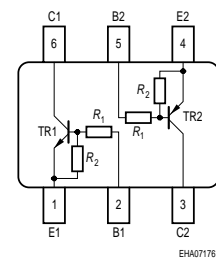
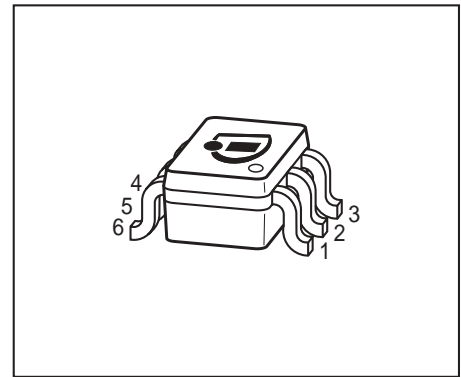
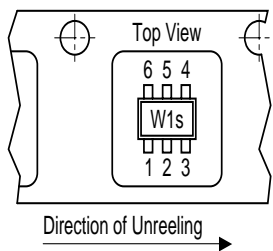


NPN/PNP Silicon Digital Transistor Array

- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP Transistors in one package
- Built in bias resistor NPN and PNP ($R_1=2.2\text{ k}\Omega$, $R_2=47\text{ k}\Omega$)
- Pb-free (RoHS compliant) package¹⁾
- Qualified according AEC Q101


Tape loading orientation


Marking on SOT-363 package (for example W1s) corresponds to pin 1 of device

Position in tape: pin 1 opposite of feed hole side

EHA07193

| Type | Marking | Pin Configuration | | | | | Package |
|---------|---------|-------------------|------|------|------|------|---------|
| | | 1=E1 | 2=B1 | 3=C2 | 4=E2 | 5=B2 | |
| BCR08PN | WFs | | | | | | SOT363 |

Maximum Ratings for NPN and PNP Types

| Parameter | Symbol | Value | Unit |
|--|--------------|-------------|------------------|
| Collector-emitter voltage | V_{CEO} | 50 | V |
| Collector-base voltage | V_{CBO} | 50 | |
| Input forward voltage | $V_{i(fwd)}$ | 20 | |
| Input reverse voltage | $V_{i(rev)}$ | 5 | |
| DC collector current | I_C | 100 | mA |
| Total power dissipation, $T_S = 115\text{ }^\circ\text{C}$ | P_{tot} | 250 | mW |
| Junction temperature | T_j | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -65 ... 150 | |

Thermal Resistance

| | | | |
|--|------------|------------|-----|
| Junction - soldering point ²⁾ | R_{thJS} | ≤ 140 | K/W |
|--|------------|------------|-----|

¹Pb-containing package may be available upon special request

²For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A=25^\circ\text{C}$, unless otherwise specified

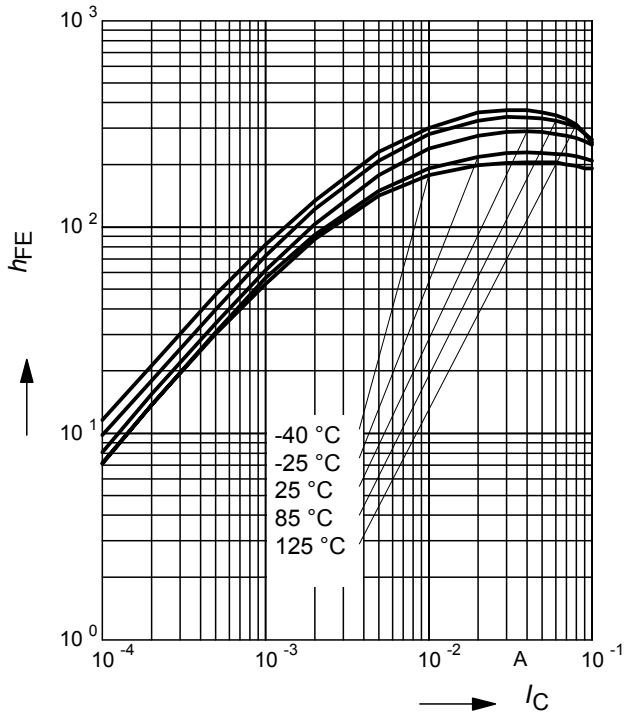
| Parameter | Symbol | Values | | | Unit |
|--|---------------|--------|-------|-------|------------------|
| | | min. | typ. | max. | |
| DC Characteristics for NPN and PNP Types | | | | | |
| Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$ | $V_{(BR)CEO}$ | 50 | - | - | V |
| Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$ | $V_{(BR)CBO}$ | 50 | - | - | |
| Collector cutoff current $V_{CB} = 40 \text{ V}, I_E = 0$ | I_{CBO} | - | - | 100 | nA |
| Emitter cutoff current $V_{EB} = 5 \text{ V}, I_C = 0$ | I_{EBO} | - | - | 164 | μA |
| DC current gain 1) $I_C = 5 \text{ mA}, V_{CE} = 5 \text{ V}$ | h_{FE} | 70 | - | - | - |
| Collector-emitter saturation voltage 1) $I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$ | V_{CEsat} | - | - | 0.3 | V |
| Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{ V}$ | $V_{i(off)}$ | 0.4 | - | 0.8 | |
| Input on Voltage $I_C = 2 \text{ mA}, V_{CE} = 0.3 \text{ V}$ | $V_{i(on)}$ | 0.5 | - | 1.1 | |
| Input resistor | R_1 | 1.5 | 2.2 | 2.9 | $\text{k}\Omega$ |
| Resistor ratio | R_1/R_2 | 0.042 | 0.047 | 0.052 | - |
| AC Characteristics for NPN and PNP Types | | | | | |
| Transition frequency $I_C = 10 \text{ mA}, V_{CE} = 5 \text{ V}, f = 100 \text{ MHz}$ | f_T | - | 170 | - | MHz |
| Collector-base capacitance $V_{CB} = 10 \text{ V}, f = 1 \text{ MHz}$ | C_{cb} | - | 2 | - | pF |

 1) Pulse test: $t < 300\mu\text{s}; D < 2\%$

NPN Type

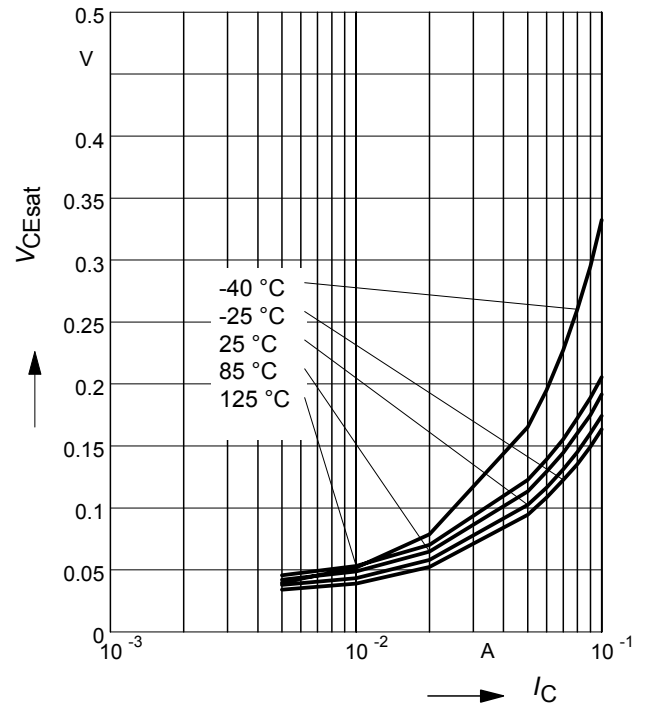
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



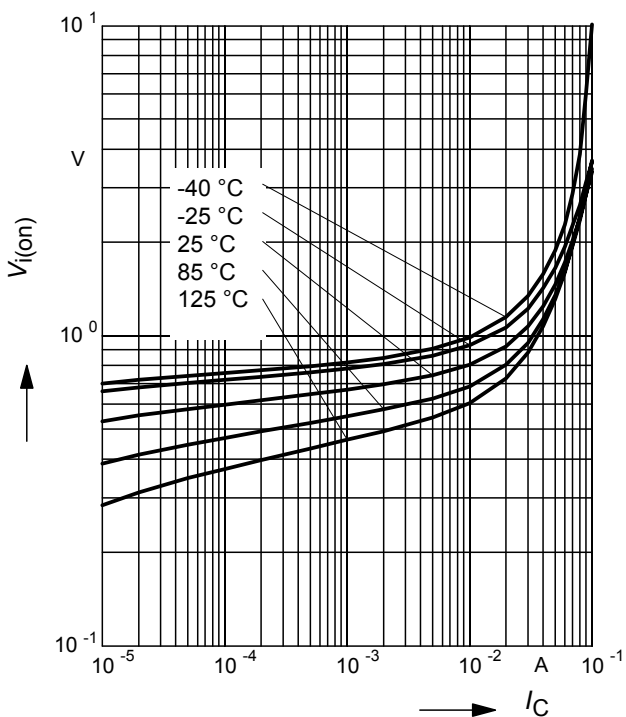
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), I_C/I_B = 20$



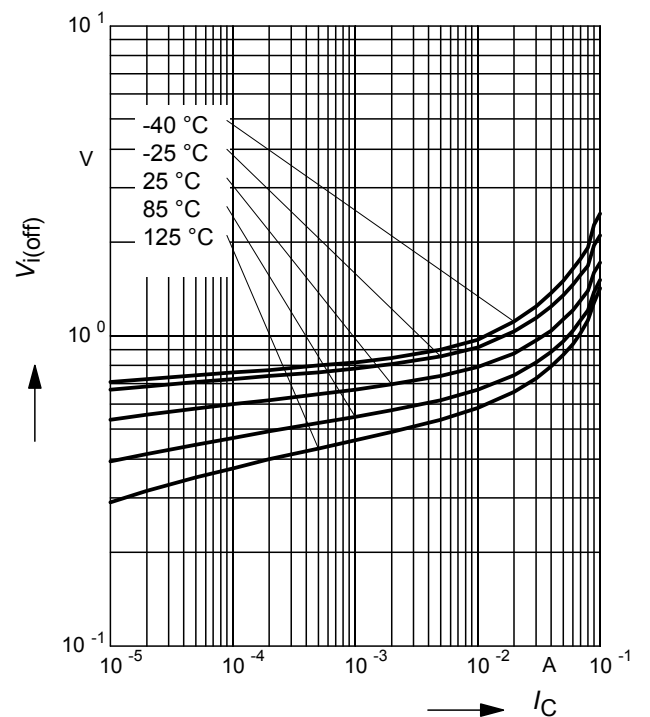
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



Input off voltage $V_{i(off)} = f(I_C)$

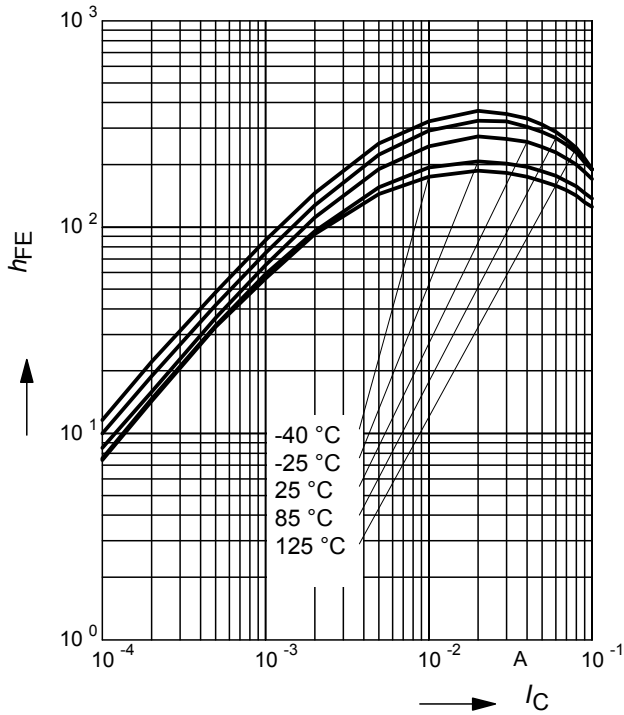
$V_{CE} = 5V$ (common emitter configuration)



PNP Type

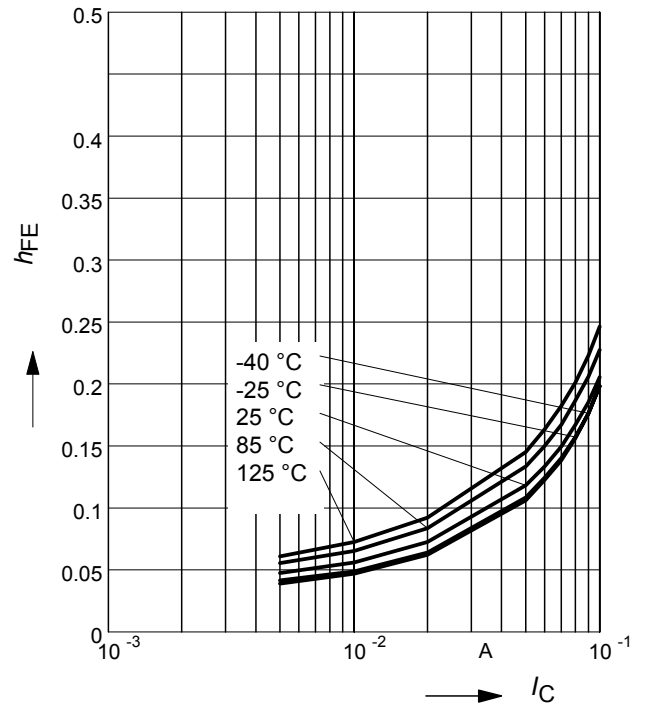
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



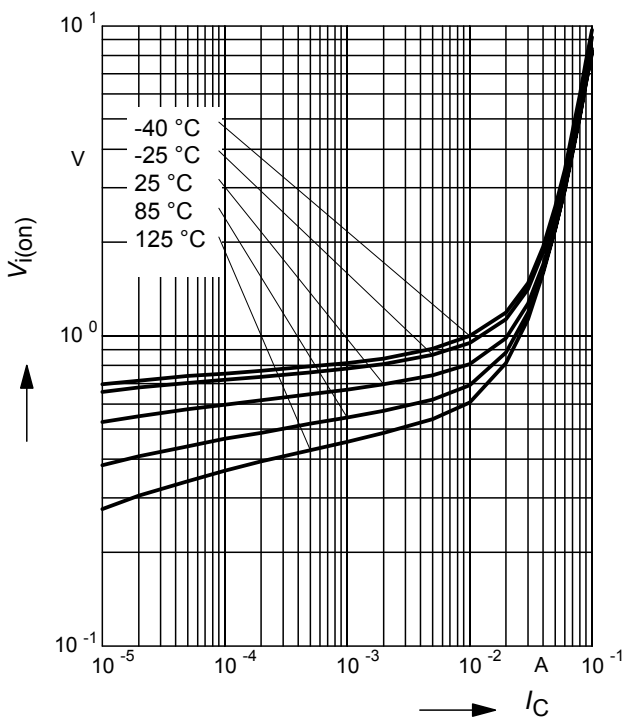
Collector-Emitter Saturation Voltage $V_{CEsat} = f(I_C), I_C/I_B = 20$

$V_{CEsat} = f(I_C), I_C/I_B = 20$



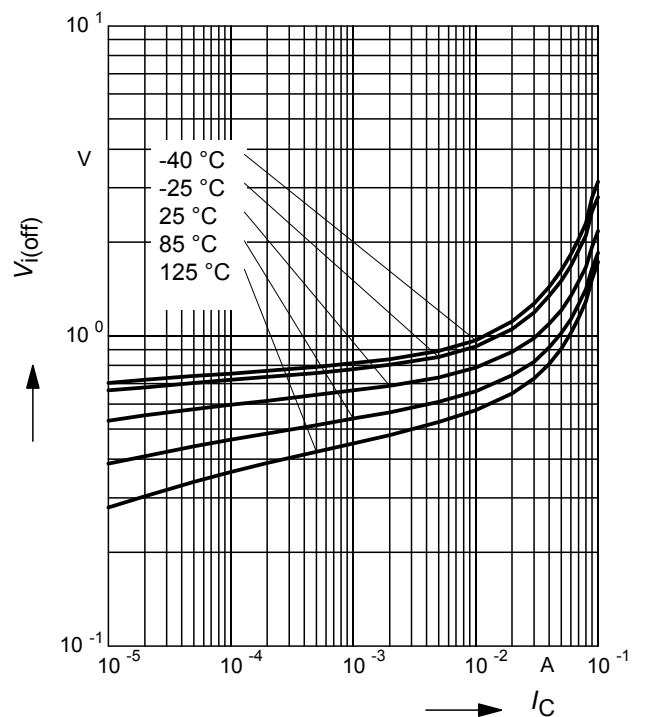
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)

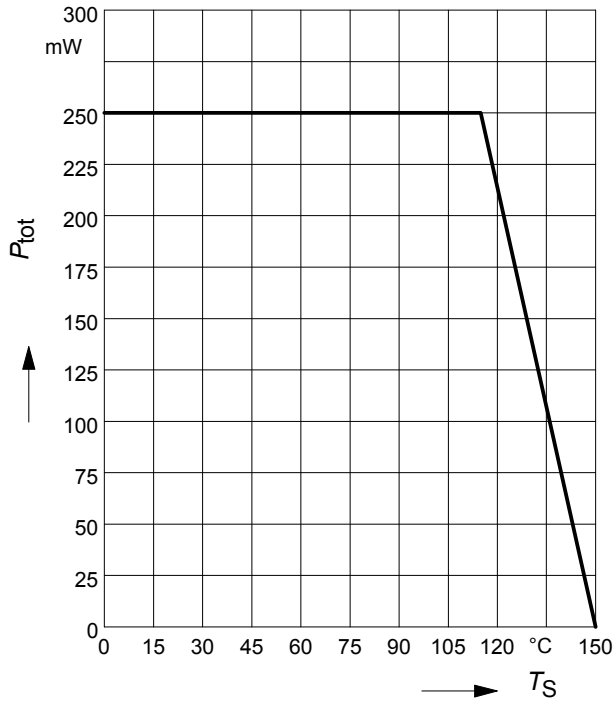


Input off voltage $V_{i(off)} = f(I_C)$

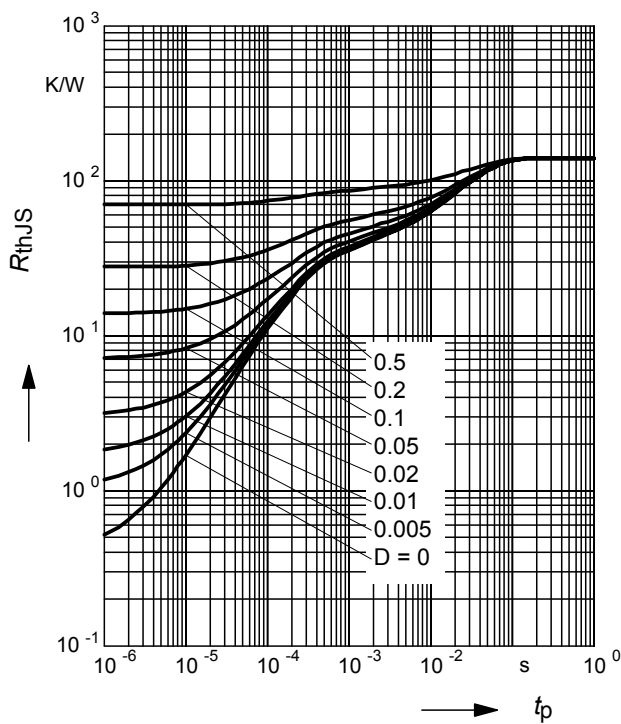
$V_{CE} = 5V$ (common emitter configuration)



Total power dissipation $P_{tot} = f(T_S)$

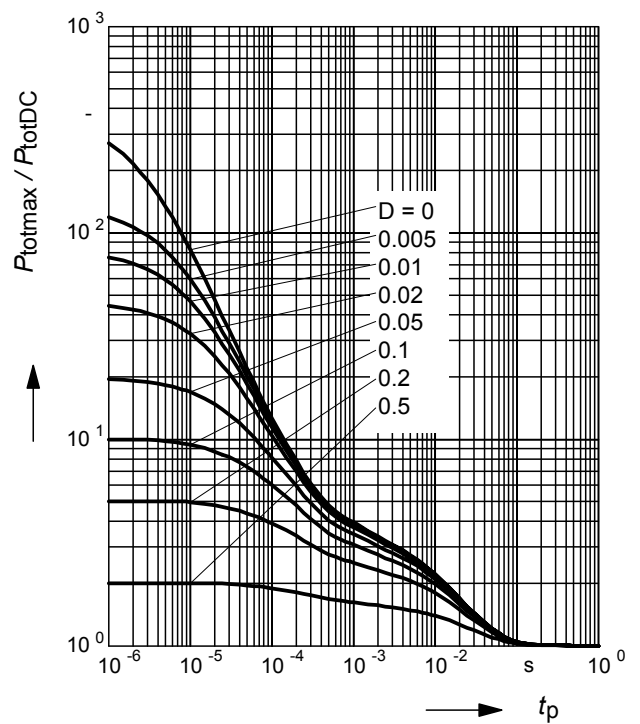


Permissible Pulse Load $R_{thJS} = f(t_p)$

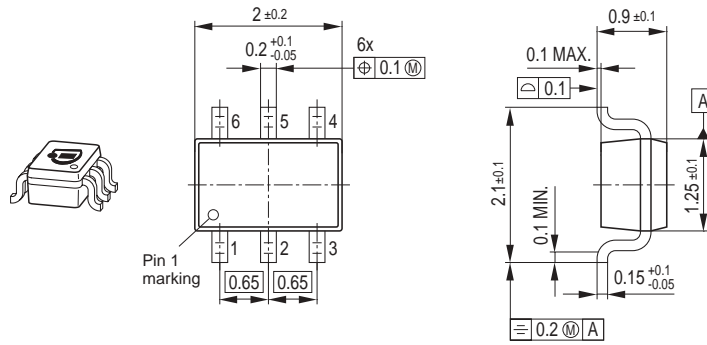


Permissible Pulse Load

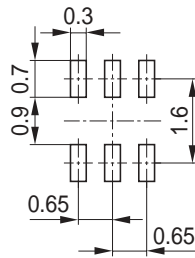
$P_{totmax} / P_{totDC} = f(t_p)$



Package Outline

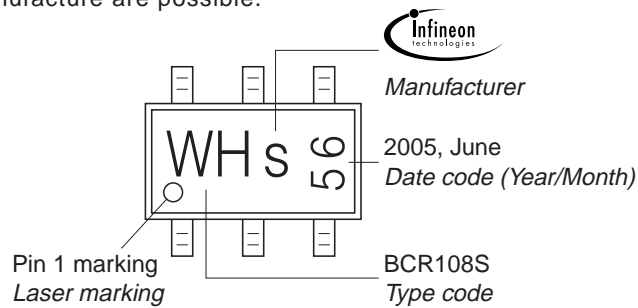


Foot Print



Marking Layout (Example)

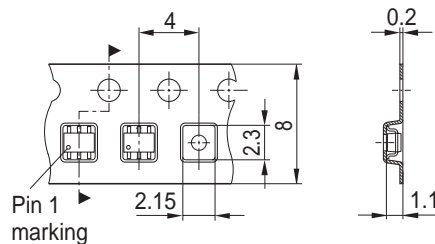
Small variations in positioning of Date code, Type code and Manufacture are possible.



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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