Octal, 12-/16-Bit *nano*DAC+ with 2 ppm/°C Reference, SPI Interface

Data Sheet

AD5672R/AD5676R

FEATURES

High performance
- **High relative accuracy (INL): ±3 LSB maximum at 16 bits**
- **Total unadjusted error (TUE): ±0.14% of FSR maximum**
- **Offset error: ±1.5 mV maximum**
- **Gain error: ±0.06% of FSR maximum**
- **Low drift 2.5 V reference: 2 ppm/°C typical**

Wide operating ranges
- **−40°C to +125°C temperature range**
- **2.7 V to 5.5 V power supply range**

Easy implementation
- **User selectable gain of 1 or 2 (GAIN pin/gain bit)**
- **1.8 V logic compatibility**

50 MHz SPI with readback or daisy chain

20-lead, RoHS-compliant TSSOP and LFCSP

APPLICATIONS

Optical transceivers

Base station power amplifiers

Process control (PLC input/output cards)

Industrial automation

Data acquisition systems

GENERAL DESCRIPTION

The AD5672R/AD5676R are low power, octal, 12-/16-bit buffered voltage output digital-to-analog converters (DACs). They include a 2.5 V, 2 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The AD5672R/AD5676R are available in a 20-lead TSSOP and in a 20-lead LFCSP and incorporate a power-on reset circuit and a RSTSEL pin that ensures that the DAC outputs power up to zero scale or midscale and remains there until a valid write. The AD5672R/AD5676R contain a power-down mode, reducing the current consumption to 1 µA typical while in power-down mode.

Table 1. Octal *nano*DAC+® Devices

Interface	Reference	16-Bit	12-Bit
SPI	Internal	AD5676R	AD5672R
	External	AD5676	Not applicable
I²C	Internal	AD5675R	AD5671R

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   AD5672R (12-bit): ±1 LSB maximum.
   AD5676R (16-bit): ±3 LSB maximum.
2. Low Drift, 2.5 V On-Chip Reference.

FUNCTIONAL BLOCK DIAGRAM

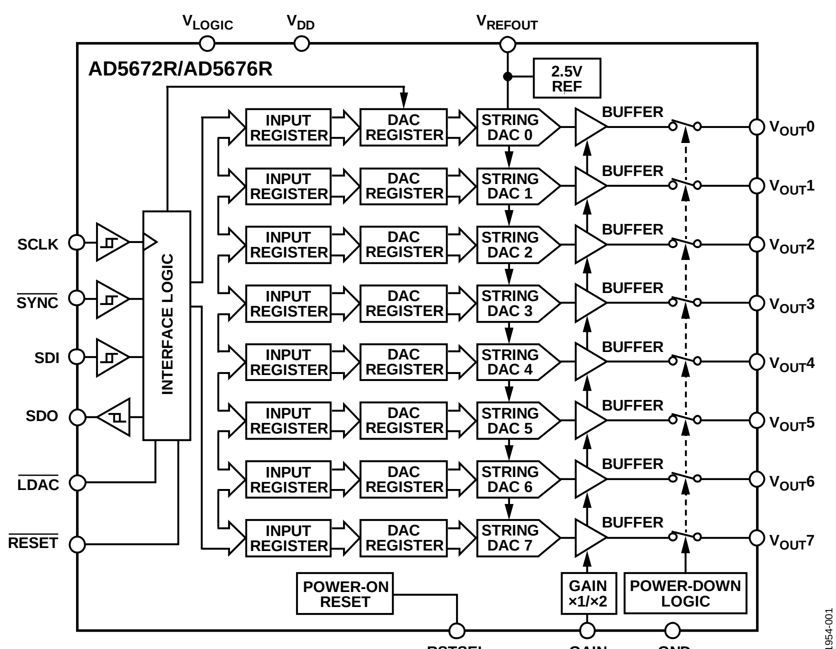

Figure 1.

Rev. D Document Feedback

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10/2014—Revision 0: Initial Version

SPECIFICATIONS

AD5672R SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, resistive load (R_L) = 2 kΩ, capacitive load (C_L) = 200 pF, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	12			Bits	
Relative Accuracy (INL)		±0.12	±1	LSB	Gain = 1
		±0.12	±1	LSB	Gain = 2
Differential Nonlinearity (DNL)		±0.01	±0.1	LSB	Gain = 1
		±0.01	±0.1	LSB	Gain = 2
Zero Code Error		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error		−0.75	±2	mV	Gain = 1
		−0.1	±1.5	mV	Gain = 2
Full-Scale Error		−0.018	±0.14	% of full-scale range (FSR)	Gain = 1
		−0.013	±0.07	% of FSR	Gain = 2
Gain Error		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.06	% of FSR	Gain = 2
TUE		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift		±1		µV/°C	
DC Power Supply Rejection Ratio (PSRR)		0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk		±2		µV	Due to single channel, full-scale output change
		±3		µV/mA	Due to load current change
		±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		2.5	V	Gain = 1
	0		5	V	Gain = 2
Output Current Drive (I_{OUT})			15	mA	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 1 kΩ
Resistive Load[2]	1			kΩ	
Load Regulation		183		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[3]		40		mA	
Load Impedance at Rails[4]		25		Ω	
Power-Up Time		2.5		µs	Exiting power-down mode, V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage[5]	2.4975		2.5025	V	
Reference Temperature Coefficient[6, 7]		2	5	ppm/°C	See the Terminology section
Output Impedance		0.04		Ω	
Output Voltage Noise		13		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient temperature, frequency (f) = 10 kHz, C_L = 10 nF, gain = 1 or 2
Load Regulation Sourcing		29		µV/mA	At ambient temperature
Load Regulation Sinking		74		µV/mA	At ambient temperature
Output Current Load Capability		±20		mA	V_{DD} ≥ 3 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Line Regulation		43		µV/V	At ambient temperature
Long-Term Stability/Drift		12		ppm	After 1000 hours at 125°C
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
LOGIC INPUTS					
Input Current			±1	µA	Per pin
Input Voltage					
Low, V_{IL}			$0.3 \times V_{LOGIC}$	V	
High, V_{IH}	$0.7 \times V_{LOGIC}$			V	
Pin Capacitance		3		pF	
LOGIC OUTPUTS (SDO)					
Output Voltage					
Low, V_{OL}			0.4	V	I_{OL} = 200 µA
High, V_{OH}	$V_{LOGIC} - 0.4$			V	I_{OH} = −200 µA
Floating State Output Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.62		5.5	V	
V_{LOGIC} Supply Current (I_{LOGIC})			1	µA	Power-on, −40°C to +105°C
			1.3	µA	Power-on, −40°C to +125°C
			0.5	µA	Power-down, −40°C to +105°C
			1.3	µA	Power-down, −40°C to +125°C
V_{DD}	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V	Gain = 2
V_{DD} Supply Current (I_{DD})					$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[8]		1.1	1.26	mA	Internal reference off, −40°C to +85°C
		1.8	2.0	mA	Internal reference on, −40°C to +85°C
		1.1	1.3	mA	Internal reference off
		1.8	2.1	mA	Internal reference on
All Power-Down Modes[9]		1	1.7	µA	Tristate to 1 kΩ, −40°C to +85°C
		1	1.7	µA	Power-down to 1 kΩ, −40°C to +85°C
		1	2.5	µA	Tristate, −40°C to +105°C
		1	2.5	µA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5	µA	Tristate to 1 kΩ, −40°C to +125°C
		1	5.5	µA	Power-down to 1 kΩ, −40°C to +125°C

[1] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when the internal reference voltage (V_{REF}) = V_{DD} with gain = 1, or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 12 to 4080.
[2] Together, Channel 0, Channel 1, Channel 2, and Channel 3 can source/sink 40 mA. Similarly, together, Channel 4, Channel 5, Channel 6, and Channel 7 can source/sink 40 mA up to a junction temperature of 125°C.
[3] V_{DD} = 5 V. The devices include current limiting intended to protect the devices during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.
[4] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.
[5] Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the Internal Reference Setup section.
[6] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +125°C.
[7] Reference temperature coefficient calculated as per the box method. See the Terminology section for further information.
[8] Interface inactive. All DACs active. DAC outputs unloaded.
[9] All DACs powered down.

AD5676R SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, R_L = 2 kΩ, C_L = 200 pF, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE[1]								
Resolution	16			16			Bits	
Relative Accuracy (INL)		±1.8	±8		±1.8	±3	LSB	Gain = 1
		±1.7	±8		±1.7	±3	LSB	Gain = 2
Differential Nonlinearity (DNL)		±0.7	±1		±0.7	±1	LSB	Gain = 1
		±0.5	±1		±0.5	±1	LSB	Gain = 2
Zero Code Error		0.8	3		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error		−0.75	±6		−0.75	±2	mV	Gain = 1
		−0.1	±4		−0.1	±1.5	mV	Gain = 2
Full-Scale Error		−0.018	±0.28		−0.018	±0.14	% of FSR	Gain = 1
		−0.013	±0.14		−0.013	±0.07	% of FSR	Gain = 2
Gain Error		+0.04	±0.24		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.12		−0.02	±0.06	% of FSR	Gain = 2
TUE		±0.03	±0.3		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.25		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift		±1			±1		µV/°C	
DC Power Supply Rejection Ratio (PSRR)		0.25			0.25		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS								
Output Voltage Range	0		2.5	0		2.5	V	Gain = 1
	0		5	0		5	V	Gain = 2
Output Current Drive			15			15	mA	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 1 kΩ
Resistive Load[2]	1			1			kΩ	
Load Regulation		183			183		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ I_{OUT} ≤ +30 mA
		177			177		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[3]		40			40		mA	
Load Impedance at Rails[4]		25			25		Ω	
Power-Up Time		2.5			2.5		µs	Exiting power-down mode, V_{DD} = 5 V
REFERENCE OUTPUT								
Output Voltage[5]	2.4975		2.5025	2.4975		2.5025	V	
Reference Temperature Coefficient[6, 7]		5	20		2	5	ppm/°C	See the Terminology section
Output Impedance		0.04			0.04		Ω	
Output Voltage Noise		13			13		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240			240		nV/√Hz	At ambient temperature, f = 10 kHz, C_L = 10 nF, gain = 1 or 2
Load Regulation Sourcing		29			29		µV/mA	At ambient temperature
Load Regulation Sinking		74			74		µV/mA	At ambient temperature
Output Current Load Capability		±20			±20		mA	V_{DD} ≥ 3 V
Line Regulation		43			43		µV/V	At ambient temperature
Long-Term Stability/Drift		12			12		ppm	After 1000 hours at 125°C
Thermal Hysteresis		125			125		ppm	First cycle
		25			25		ppm	Additional cycles

Parameter	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
LOGIC INPUTS								
Input Current			±1			±1	µA	Per pin
Input Voltage								
Low, V_{INL}			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
High, V_{INH}	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		3			3		pF	
LOGIC OUTPUTS (SDO)								
Output Voltage								
Low, V_{OL}			0.4			0.4	V	I_{SINK} = 200 µA
High, V_{OH}	V_{LOGIC} − 0.4			V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 µA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
I_{LOGIC}			1			1	µA	Power-on, −40°C to +105°C
			1.3			1.3	µA	Power-on, −40°C to +125°C
			0.5			0.5	µA	Power-down, −40°C to +105°C
			1.3			1.3	µA	Power-down, −40°C to +125°C
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}								V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[8]		1.1	1.26		1.1	1.26	mA	Internal reference off, −40°C to +85°C
		1.8	2.0		1.8	2.0	mA	Internal reference on, −40°C to +85°C
		1.1	1.3		1.1	1.3	mA	Internal reference off
		1.8	2.1		1.8	2.1	mA	Internal reference on
All Power-Down Modes[9]		1	1.7		1	1.7	µA	Tristate to 1 kΩ, −40°C to +85°C
		1	1.7		1	1.7	µA	Power-down to 1 kΩ, −40°C to +85°C
		1	2.5		1	2.5	µA	Tristate, −40°C to +105°C
		1	2.5		1	2.5	µA	Power-down to 1 kΩ, −40°C to +105°C
		1	5.5		1	5.5	µA	Tristate to 1 kΩ, −40°C to +125°C
		1	5.5		1	5.5	µA	Power-down to 1 kΩ, −40°C to +125°C

1 DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when V_{REF} = V_{DD} with gain = 1, or when $V_{REF}/2$ = V_{DD} with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280.
2 Together, Channel 0, Channel 1, Channel 2, and Channel 3 can source/sink 40 mA. Similarly, together, Channel 4, Channel 5, Channel 6, and Channel 7 can source/sink 40 mA up to a junction temperature of 125°C.
3 V_{DD} = 5 V. The devices include current limiting intended to protect the devices during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.
4 When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.
5 Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the Internal Reference Setup section.
6 Reference is trimmed and tested at two temperatures and is characterized from −40°C to +125°C.
7 Reference temperature coefficient calculated as per the box method. See the Terminology section for further information.
8 Interface inactive. All DACs active. DAC outputs unloaded.
9 All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, all specifications T_{MIN} to T_{MAX} unless otherwise noted. The operating temperature range is −40°C to +125°C; T_A = 25°C.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE SETTLING TIME[1]					
AD5672R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
AD5676R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
SLEW RATE		0.8		V/µs	
DIGITAL-TO-ANALOG GLITCH IMPULSE[1]		1.4		nV-sec	1 LSB change around major carry (internal reference, gain = 1)
DIGITAL FEEDTHROUGH[1]		0.13		nV-sec	
CROSSTALK[1]					
Digital		0.1		nV-sec	
Analog		−0.25		nV-sec	
		−1.3		nV-sec	Internal reference, gain = 2
DAC-to-DAC		−2.0		nV-sec	Internal reference, gain = 2
TOTAL HARMONIC DISTORTION[2]		−80		dB	At T_A, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
OUTPUT NOISE SPECTRAL DENSITY[1]		300		nV/√Hz	DAC code = midscale, 10 kHz, gain = 2
OUTPUT NOISE[1]		6		µV p-p	0.1 Hz to 10 Hz, gain = 1
SIGNAL-TO-NOISE RATIO (SNR)		90		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SPURIOUS-FREE DYNAMIC RANGE (SFDR)		83		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)		80		dB	At T_A = 25°C, bandwidth = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] See the Terminology section. Measured using internal reference and gain = 1, unless otherwise noted.
[2] Digitally generated sine wave (f_{OUT}) at 1 kHz.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; V_{REFIN} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Symbol	1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t_1	20		20		ns
SCLK High Time	t_2	8		8		ns
SCLK Low Time	t_3	10		12		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time	t_4	15		11		ns
Data Setup Time	t_5	2		3		ns
Data Hold Time	t_6	2		2		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	4		4		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	15		12		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{SYNC}}$ Rising Edge (DAC Register Updates)	t_9	870		830		ns
$\overline{\text{SYNC}}$ Falling Edge to SCLK Fall Ignore	t_{10}	4		4		ns
$\overline{\text{LDAC}}$ Pulse Width Low	t_{11}	8		8		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Rising Edge	t_{12}	25		25		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Falling Edge	t_{13}	25		25		ns
$\overline{\text{LDAC}}$ Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_{14}	840		800		ns
Minimum Pulse Width Low	t_{15}	8		10		ns
$\overline{\text{RESET}}$ Activation Time	t_{16}	90		90		ns
Power-Up Time[1]		5.5		5.5		μs

[1] Time to exit power-down to normal mode of AD5672R/AD5676R operation, $\overline{\text{SYNC}}$ rising edge to 90% of DAC midscale value, with output unloaded.

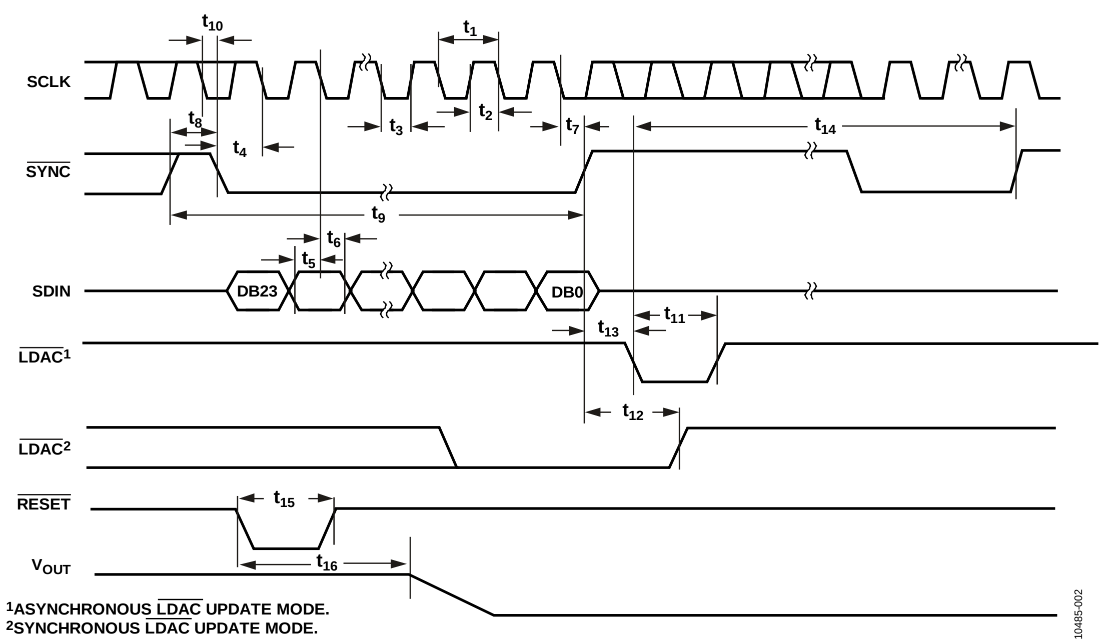


Figure 2. Serial Write Operation

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7$ V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; $V_{REF} = 2.5$ V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. V_{DD} = 2.7 V to 5.5 V.

Table 6.

		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCLK Cycle Time	t_1	130		110		ns
SCLK High Time	t_2	33		23		ns
SCLK Low Time	t_3	12		7		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge	t_4	80		80		ns
Data Setup Time	t_5	2		2		ns
Data Hold Time	t_6	2		2		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	35		10		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	55		30		ns
SDO Data Valid from SCLK Rising Edge	t_9	60		50		ns
$\overline{\text{SYNC}}$ Rising Edge to SCLK Falling Edge	t_{10}	2		6		ns
$\overline{\text{SYNC}}$ Rising Edge to SDO Disable	t_{11}	40		35		ns

Circuit and Timing Diagrams

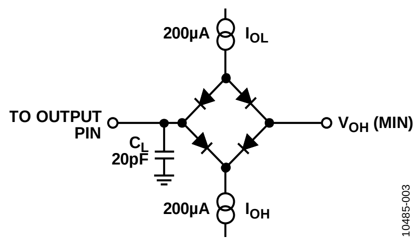


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

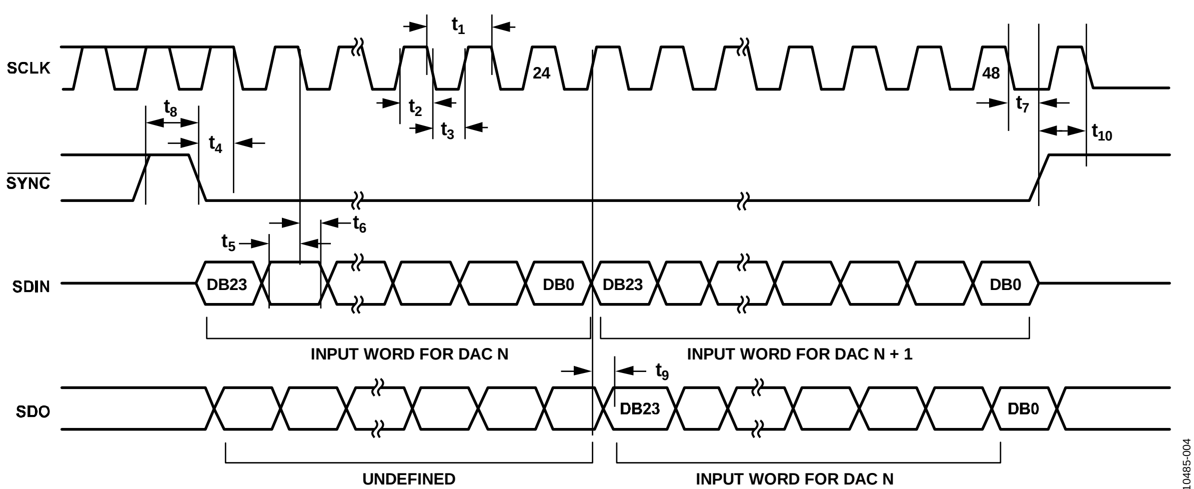


Figure 4. Daisy Chain Timing Diagram

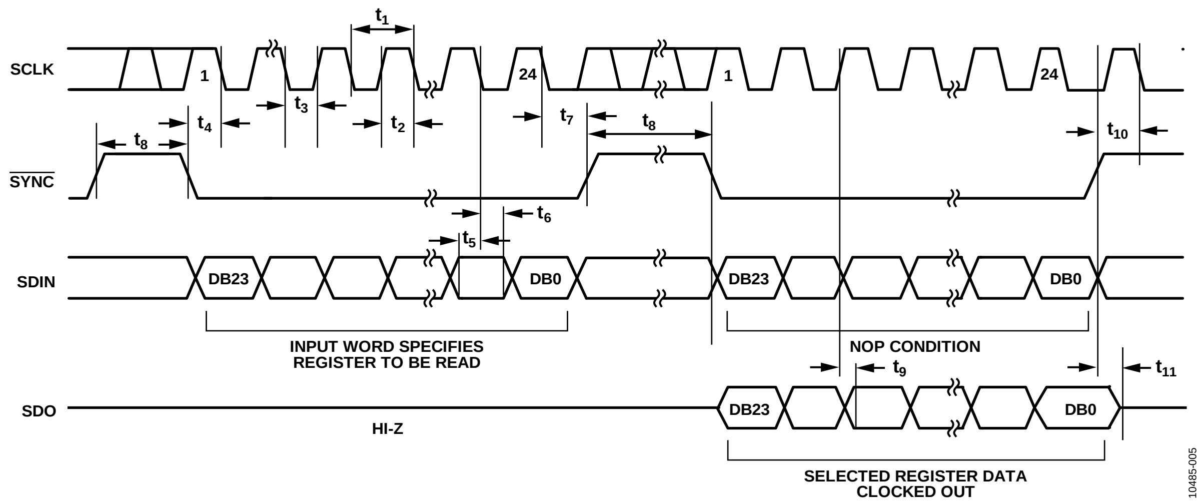


Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
$V_{OUT}x$ to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Reflow Soldering Peak Temperature, Pb-Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

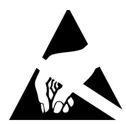
Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
20-Lead TSSOP (RU-20)[1]	98.65	44.39	17.58	1.77	43.9	°C/W
20-Lead LFCSP (CP-20-8)[2]	82	16.67	32.5	0.43	22	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51

[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

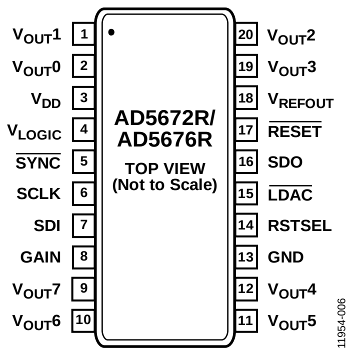


Figure 6. TSSOP Pin Configuration

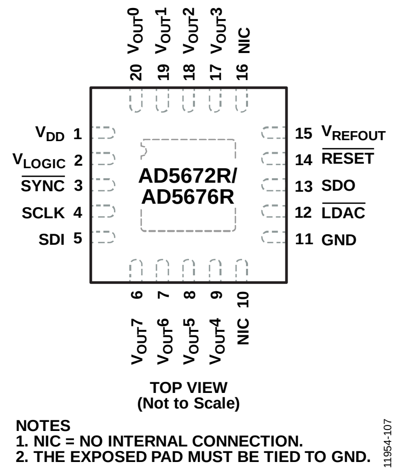


Figure 7. LFCSP Pin Configuration

Table 9. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	$V_{OUT}1$	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
2	20	$V_{OUT}0$	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
3	1	V_{DD}	Power Supply Input. These devices operate from 2.7 V to 5.5 V. Decouple the V_{DD} supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	2	V_{LOGIC}	Digital Power Supply. The voltage on this pin ranges from 1.62 V to 5.5 V.
5	3	$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data transfers in on the falling edges of the next 24 clocks.
6	4	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data transfers at rates of up to 50 MHz.
7	5	SDI	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
8	N/A[1]	GAIN	Span Set Pin. When this pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}.
9	6	$V_{OUT}7$	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
10	7	$V_{OUT}6$	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
11	8	$V_{OUT}5$	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
12	9	$V_{OUT}4$	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
N/A[1]	10	NIC	No Internal Connection.
13	11	GND	Ground Reference Point for All Circuitry on the Device.
14	N/A[1]	RSTSEL	Power-On Reset Pin. Tie this pin to GND to power up all eight DACs to zero scale. Tie this pin to V_{LOGIC} to power up all eight DACs to midscale.
15	12	$\overline{LDAC}$	Load DAC. $\overline{LDAC}$ operates in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data, which allows all DAC outputs to update simultaneously. This pin can also be tied permanently low.
16	13	SDO	Serial Data Output. This pin can be used to daisy-chain a number of devices together, or it can be used for readback. The serial data transfers on the rising edge of SCLK and is valid on the falling edge.
17	14	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin.
18	15	V_{REFOUT}	Reference Output Voltage. When using the internal reference, this is the reference output pin.
19	17	$V_{OUT}3$	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
20	18	$V_{OUT}2$	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.
N/A[1]	0	EPAD	Exposed Pad. The exposed pad must be tied to GND.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

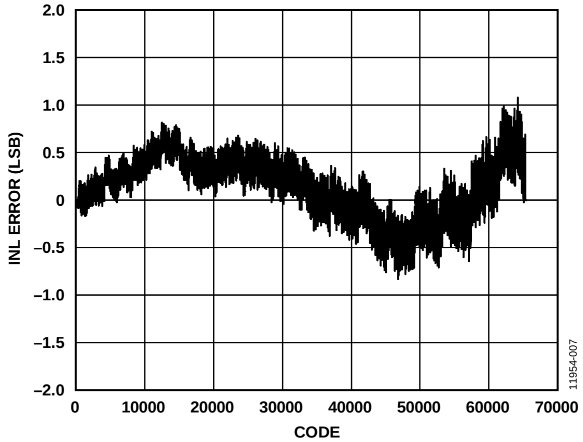


Figure 8. AD5676R INL Error vs. Code

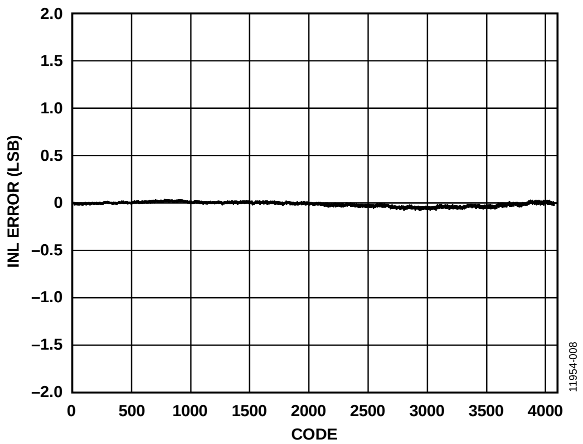


Figure 9. AD5672R INL Error vs. Code

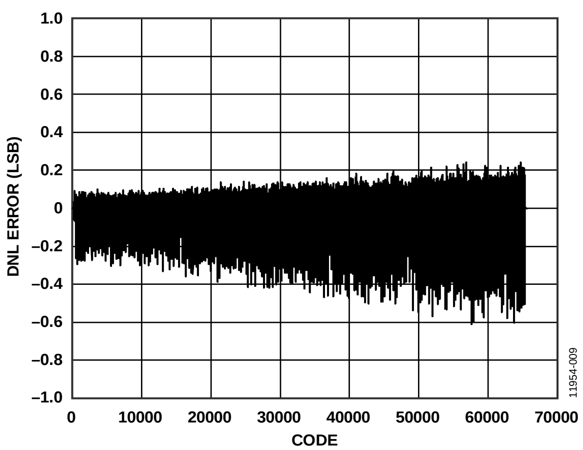


Figure 10. AD5676R DNL Error vs. Code

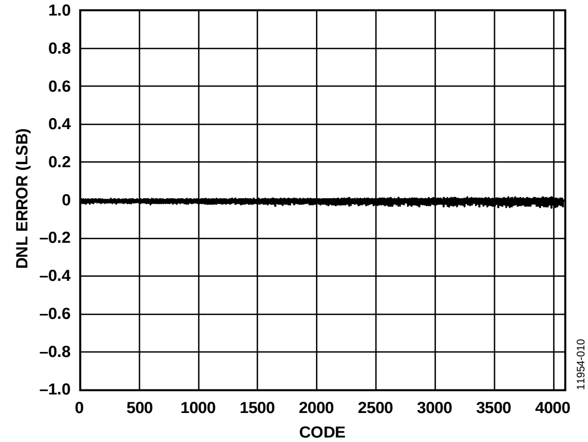


Figure 11. AD5672R DNL Error vs. Code

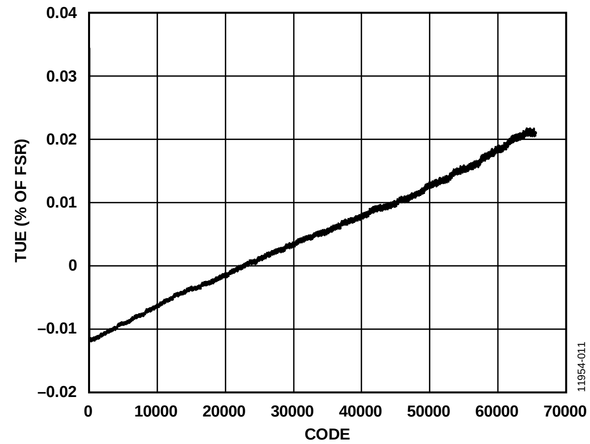


Figure 12. AD5676R TUE vs. Code

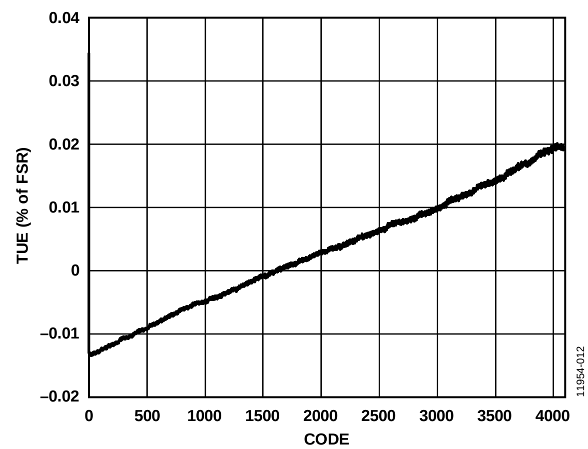


Figure 13. AD5672R TUE vs. Code

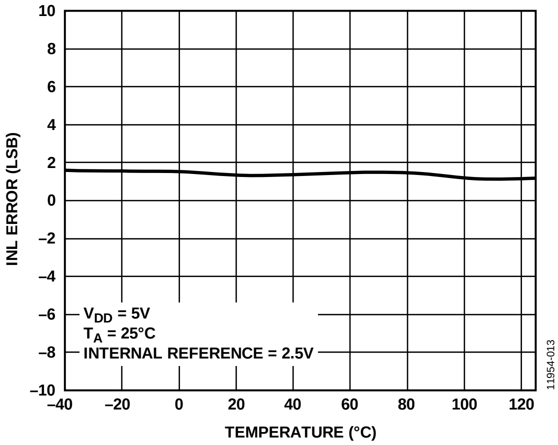


Figure 14. AD5676R INL Error vs. Temperature

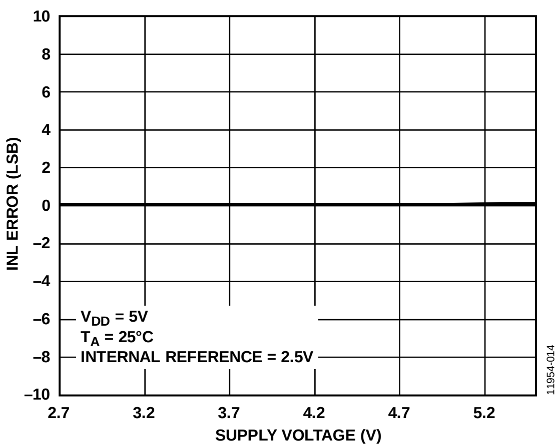


Figure 15. AD5672R INL Error vs. Supply Voltage

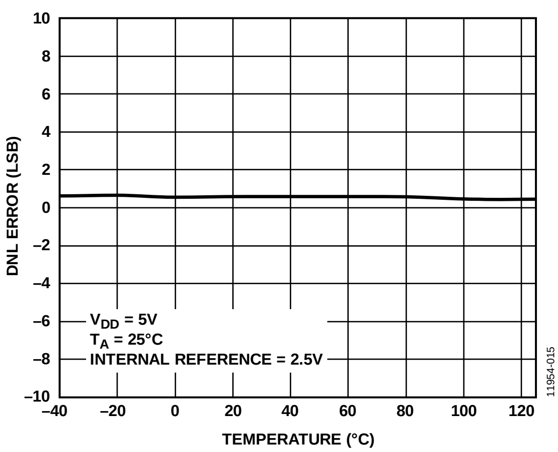


Figure 16. AD5676R DNL Error vs. Temperature

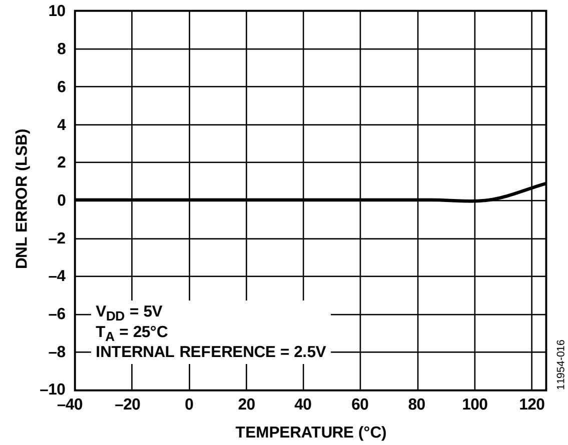


Figure 17. AD5672R DNL Error vs. Temperature

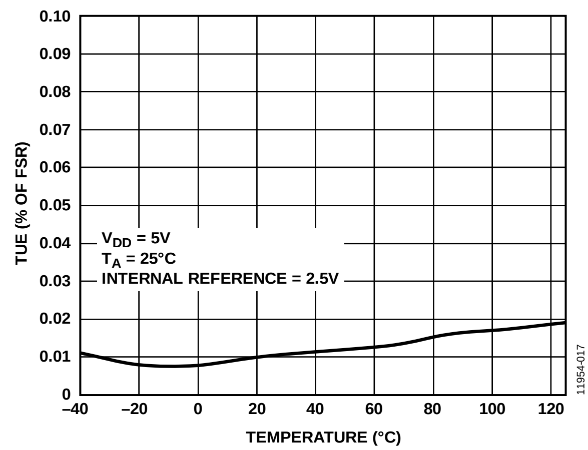


Figure 18. AD5676R TUE vs. Temperature

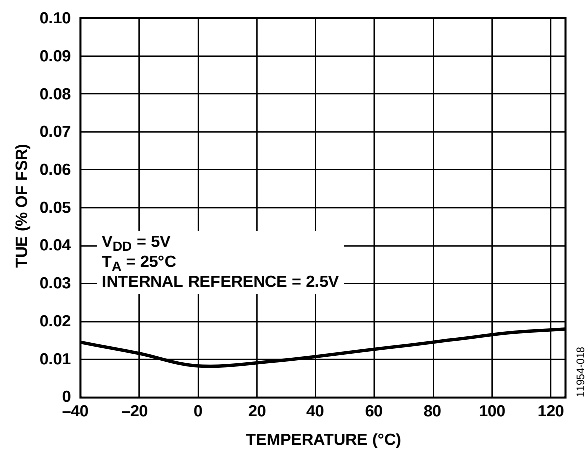


Figure 19. AD5672R TUE vs. Temperature

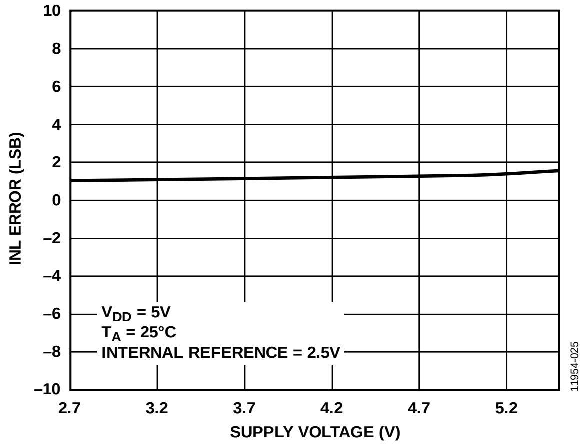


Figure 20. AD5676R INL Error vs. Supply Voltage

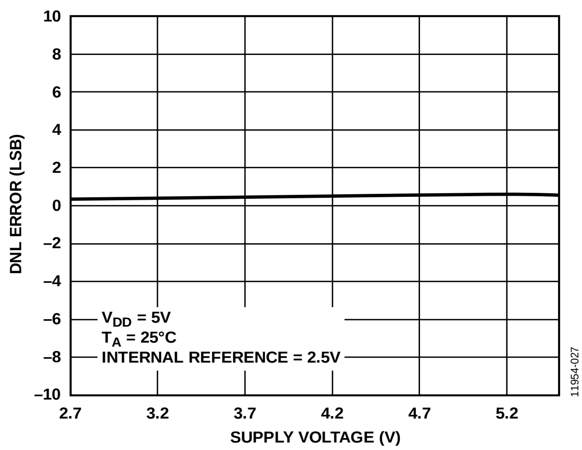


Figure 21. AD5676R DNL Error vs. Supply Voltage

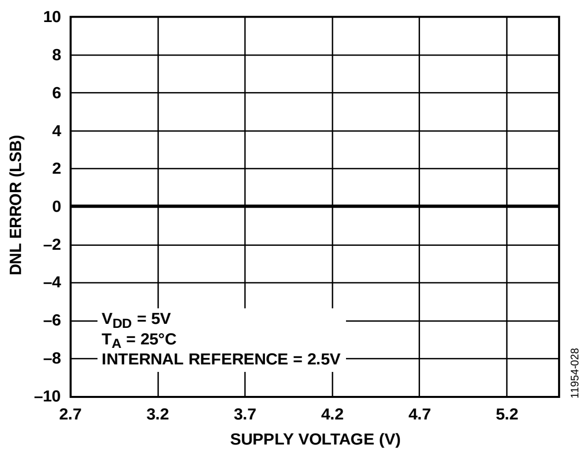


Figure 22. AD5672R DNL Error vs. Supply Voltage

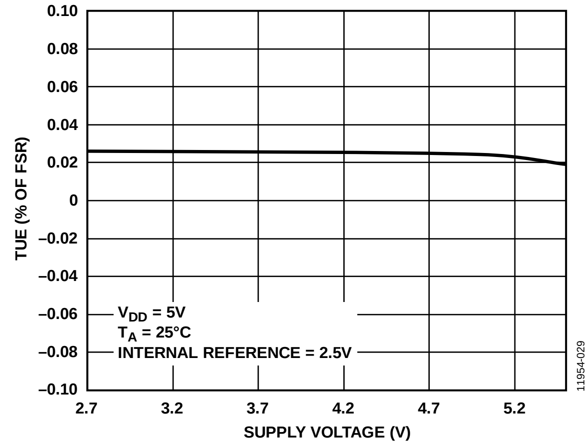


Figure 23. AD5676R TUE vs. Supply Voltage

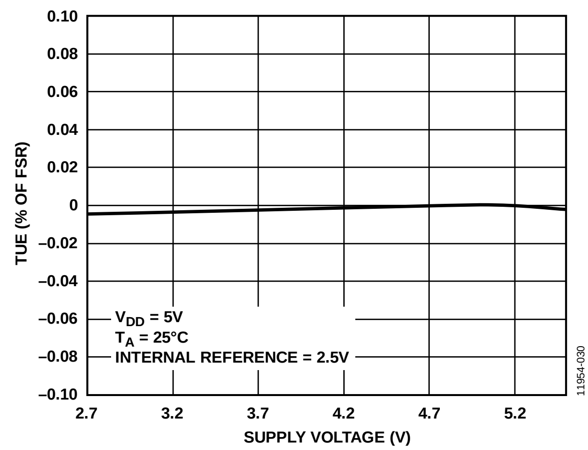


Figure 24. AD5672R TUE vs. Supply Voltage

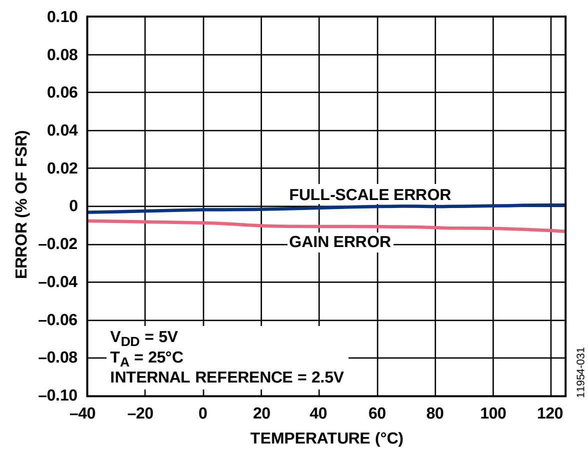


Figure 25. AD5676R Gain Error and Full-Scale Error vs. Temperature

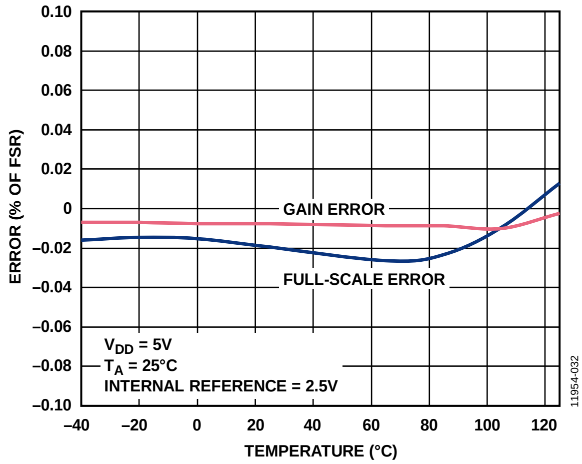


Figure 26. AD5672R Gain Error and Full-Scale Error vs. Temperature

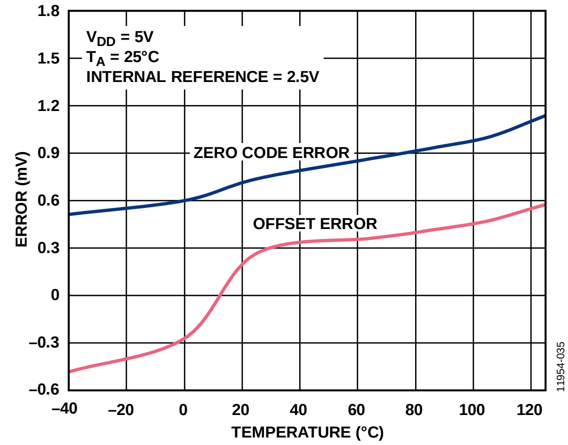


Figure 29. AD5676R Zero Code Error and Offset Error vs. Temperature

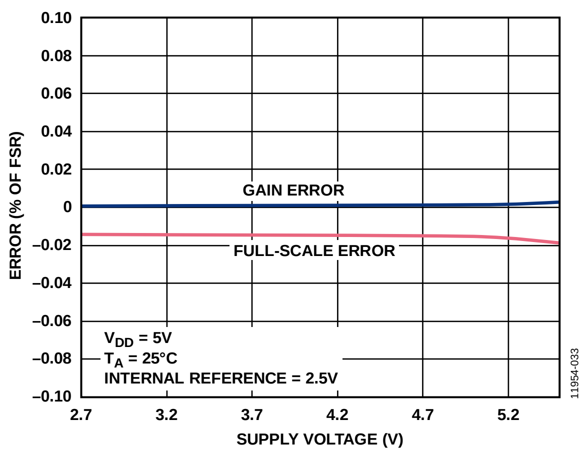


Figure 27. AD5676R Gain Error and Full-Scale Error vs. Supply Voltage

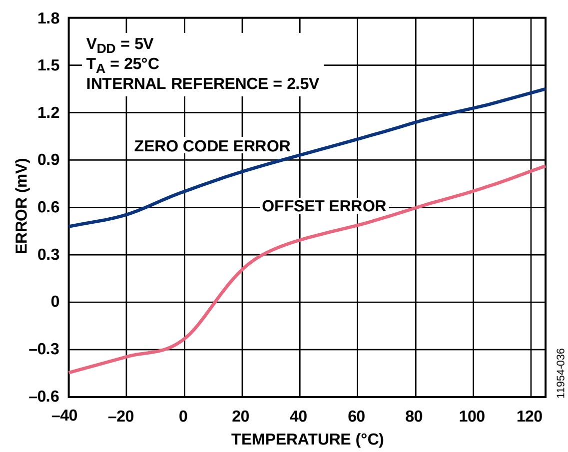


Figure 30. AD5672R Zero Code Error and Offset Error vs. Temperature

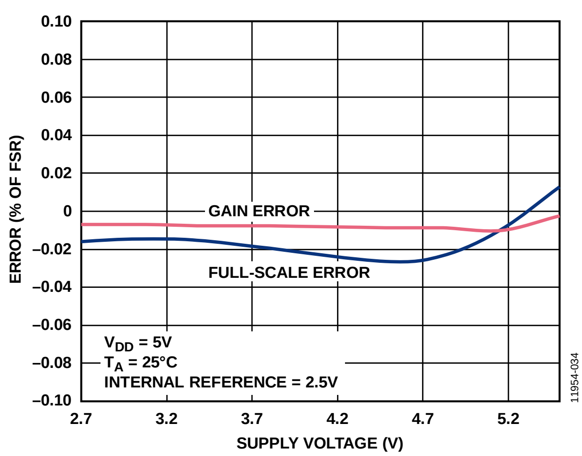


Figure 28. AD5672R Gain Error and Full-Scale Error vs. Supply Voltage

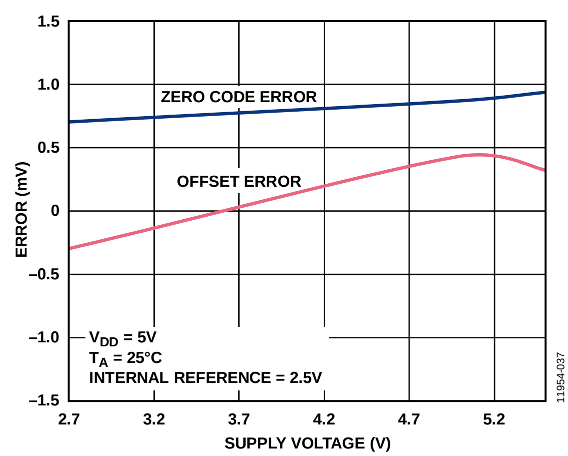


Figure 31. AD5676R Zero Code Error and Offset Error vs. Supply Voltage

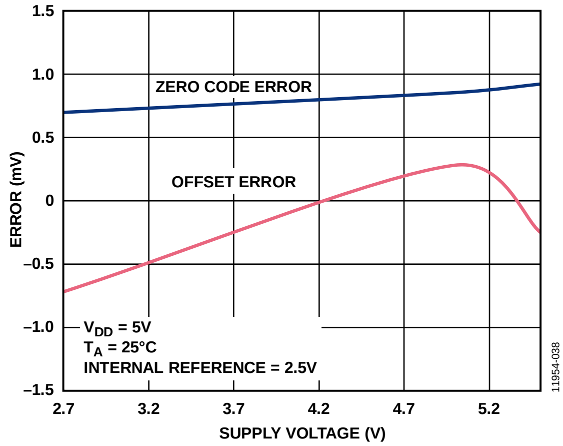


Figure 32. AD5672R Zero Code Error and Offset Error vs. Supply Voltage

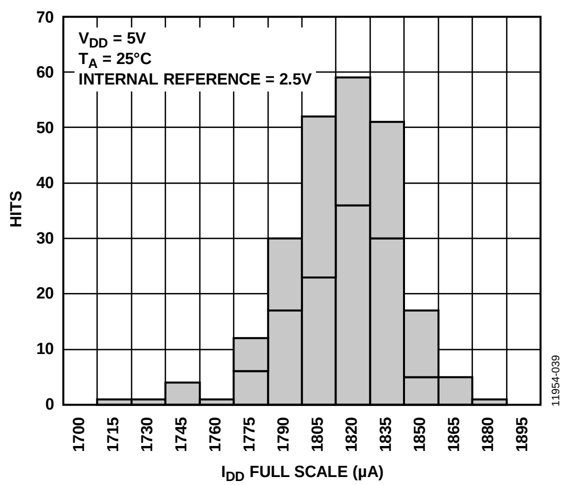


Figure 33. Supply Current (I_{DD}) Histogram with Internal Reference

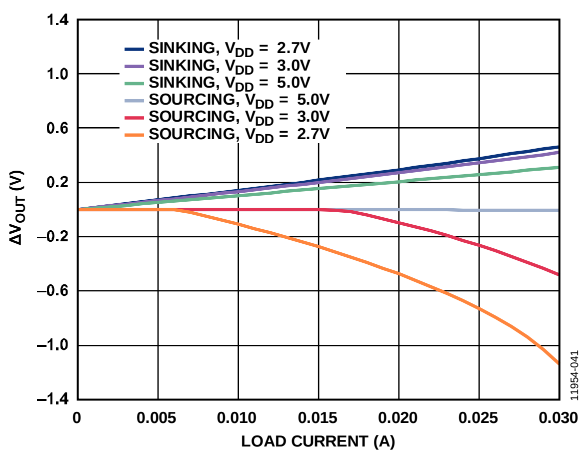


Figure 34. Headroom/Footroom (ΔV_{OUT}) vs. Load Current

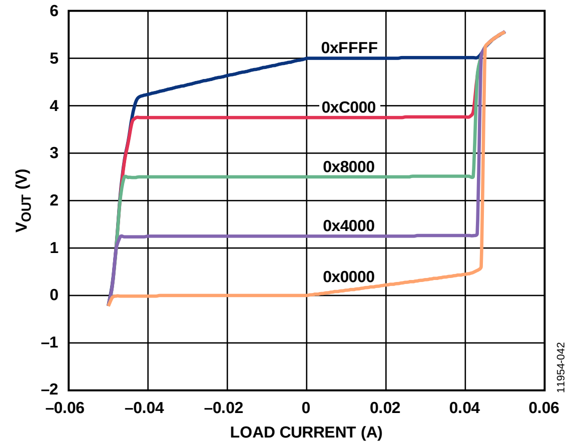


Figure 35. Source and Sink Capability at 5 V

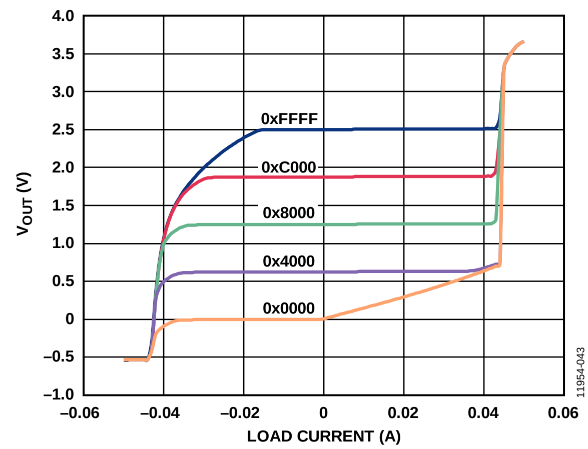


Figure 36. Source and Sink Capability at 3 V

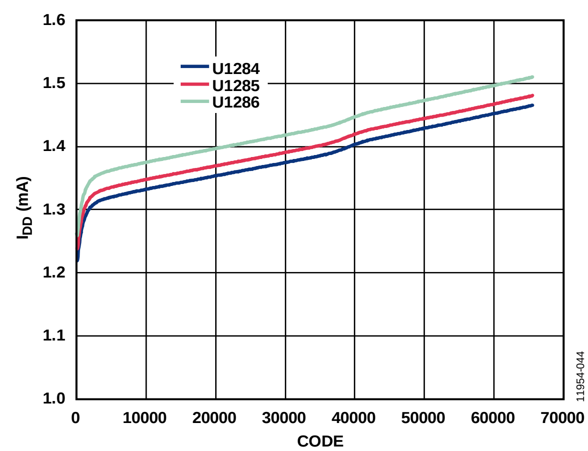


Figure 37. I_{DD} vs. Code

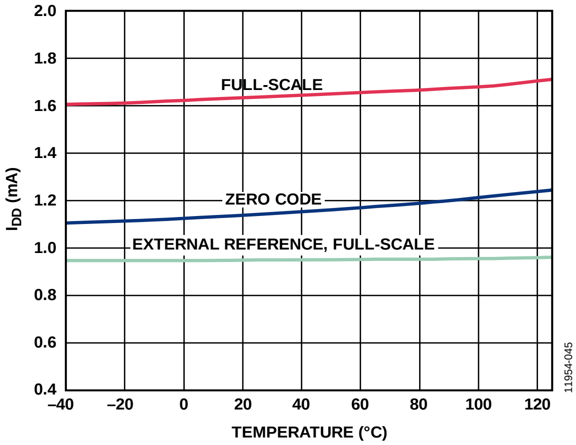


Figure 38. I_{DD} vs. Temperature

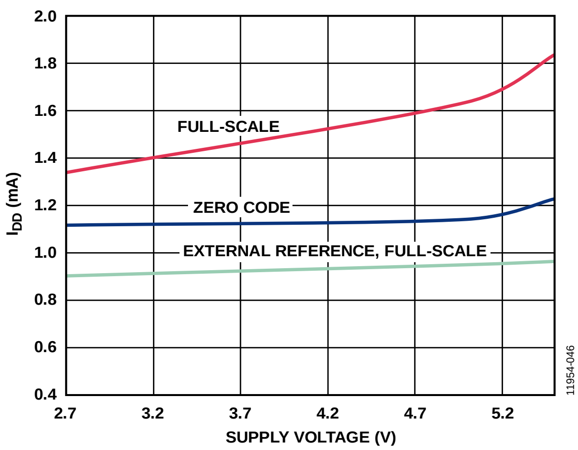


Figure 39. I_{DD} vs. Supply Voltage

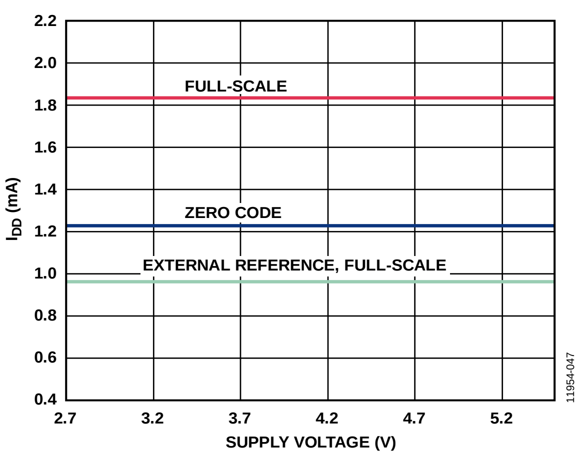


Figure 40. I_{DD} vs. Zero Code and Full-Scale

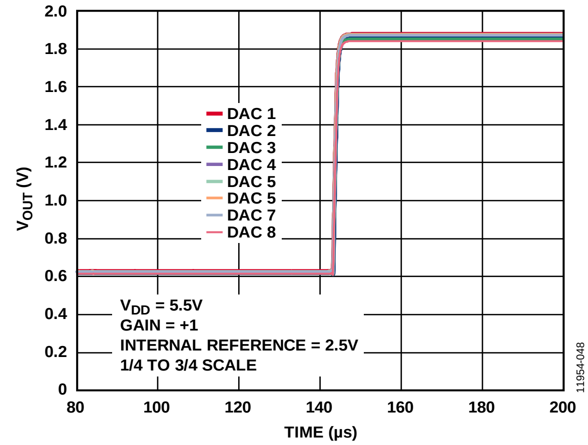


Figure 41. Full-Scale Settling Time

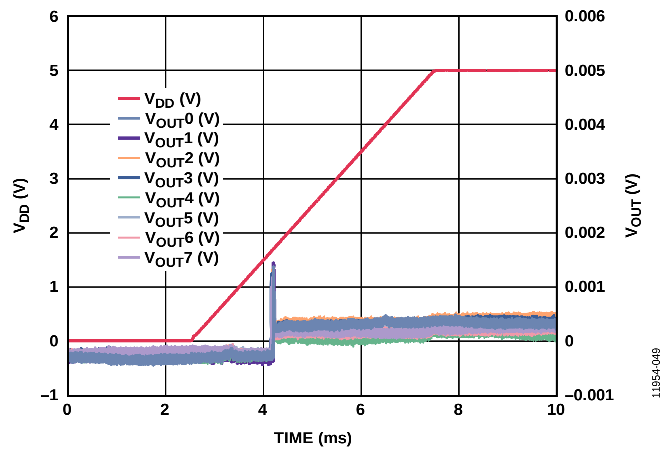


Figure 42. Power-On Reset to 0 V and Midscale

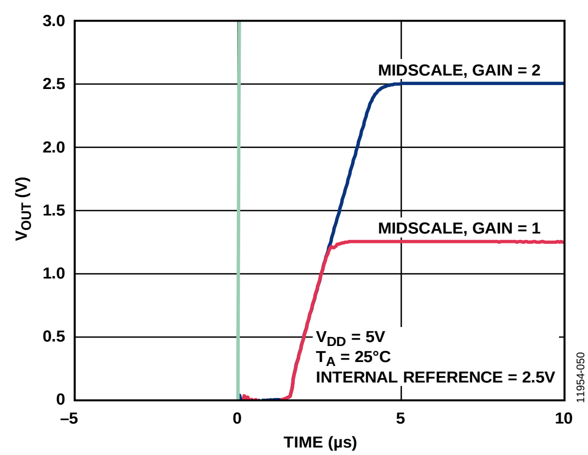


Figure 43. Exiting Power-Down to Midscale

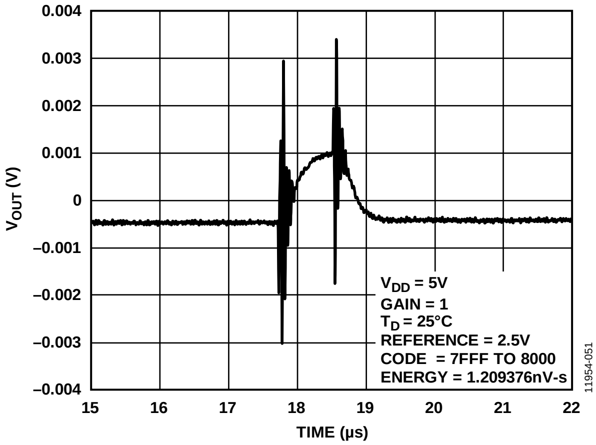


Figure 44. Digital-to-Analog Glitch Impulse

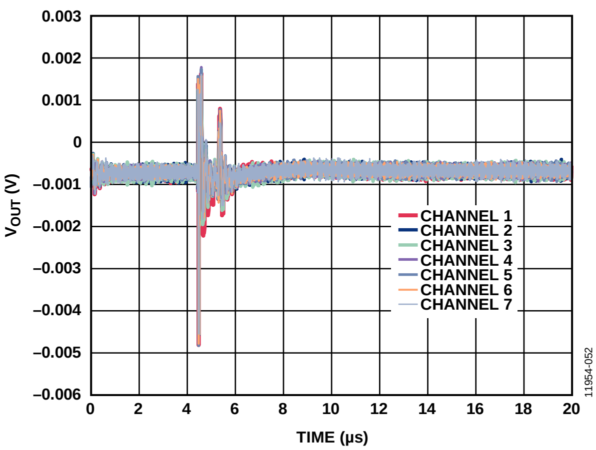


Figure 45. Analog Crosstalk

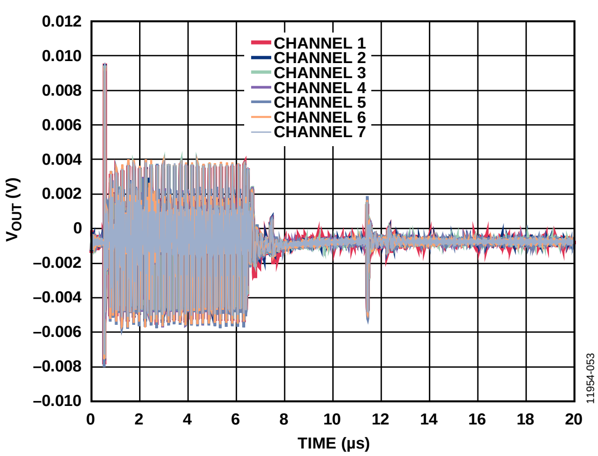


Figure 46. DAC-to-DAC Crosstalk

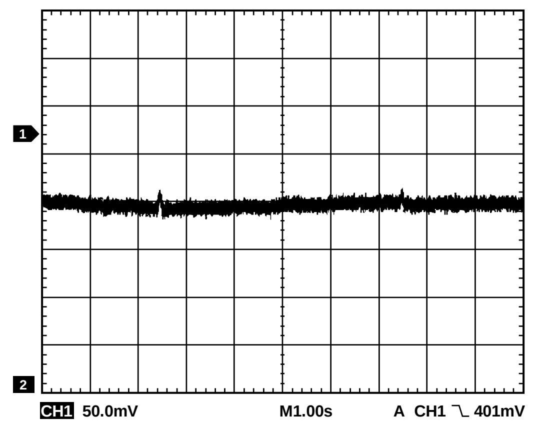


Figure 47. 0.1 Hz to 10 Hz Output Noise

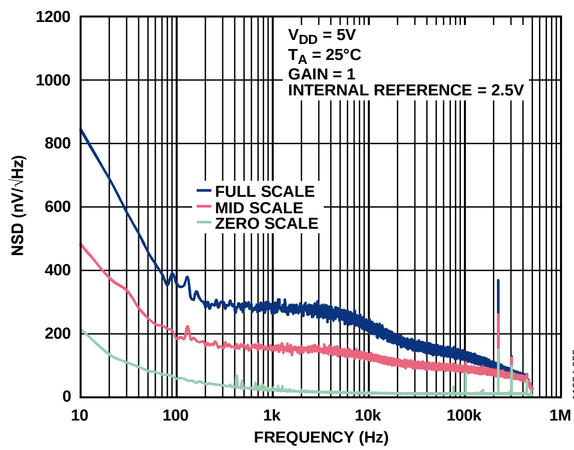


Figure 48. Noise Spectral Density (NSD)

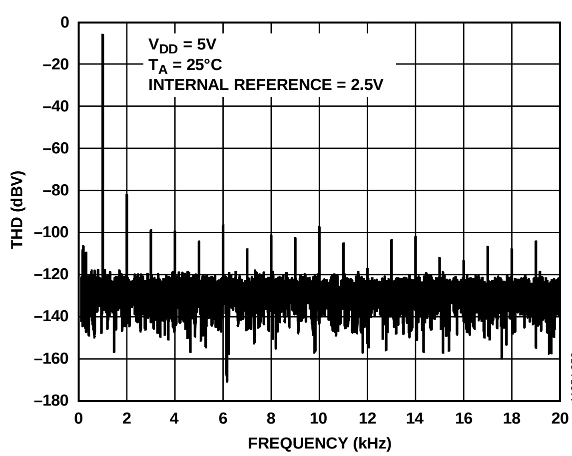


Figure 49. Total Harmonic Distortion (THD) at 1 kHz

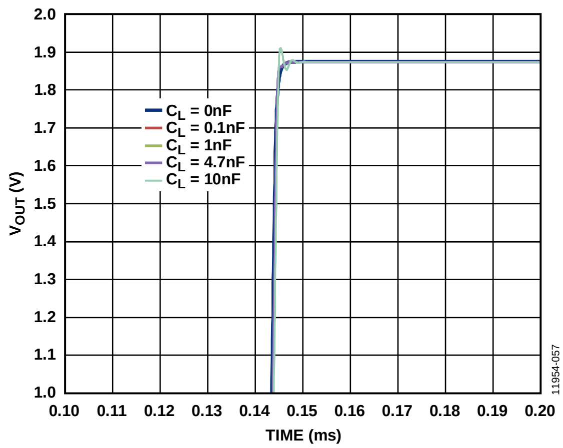


Figure 50. Settling Time at Various Capacitive Loads

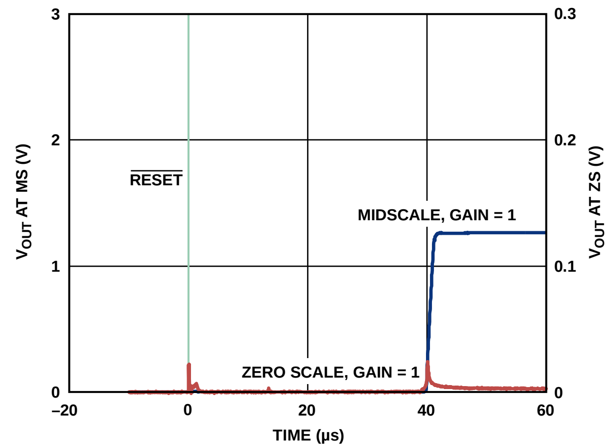


Figure 52. Hardware Reset

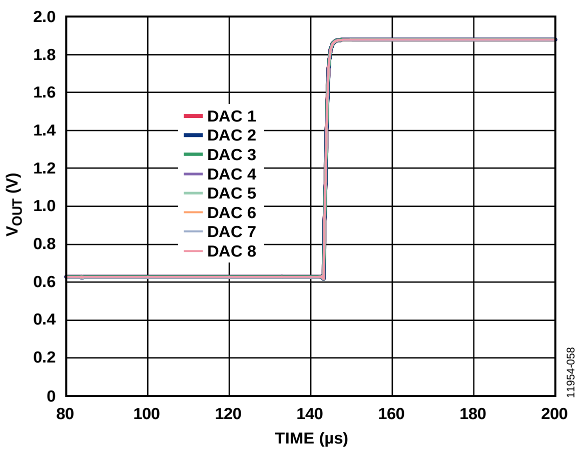


Figure 51. Settling Time, 5.5 V

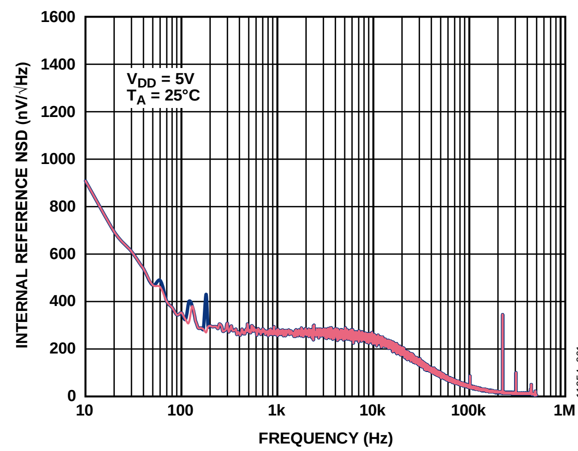


Figure 53. Internal Reference NSD vs. Frequency

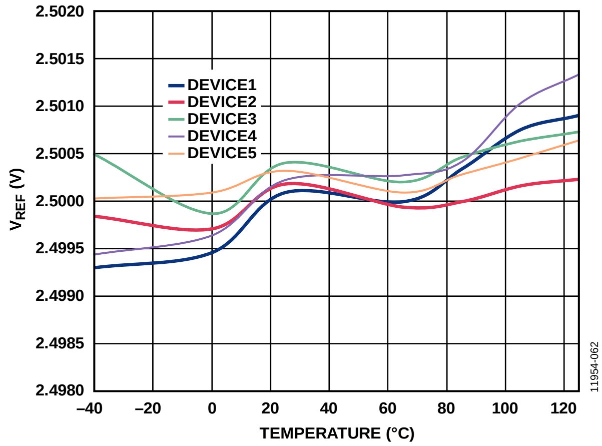


Figure 54. Internal Reference Voltage (V_{REF}) vs. Temperature (A Grade)

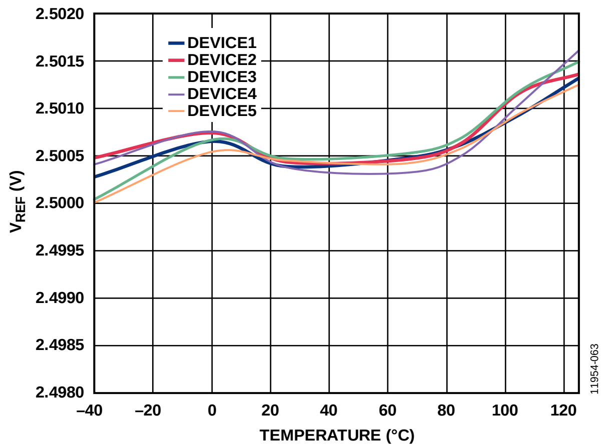


Figure 55. Internal Reference Voltage (V_{REF}) vs. Temperature (B Grade)

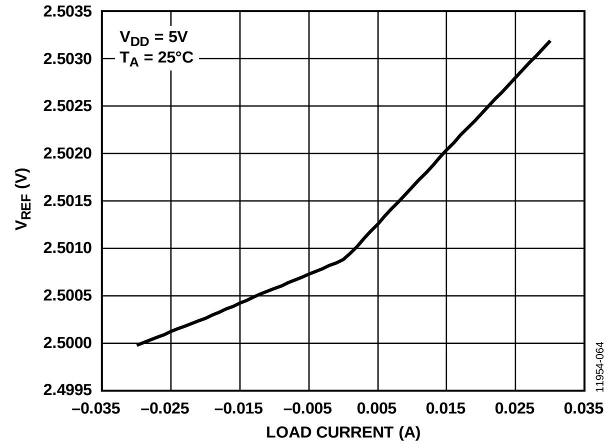


Figure 56. Internal Reference Voltage (V_{REF}) vs. Load Current and Supply Voltage (V_{DD})

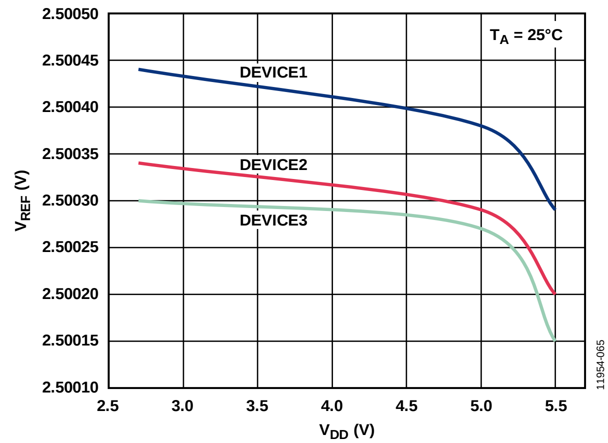


Figure 57. Internal Reference Voltage (V_{REF}) vs. Supply Voltage (V_{DD})

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. These DACs are guaranteed monotonic by design.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. The ideal output is 0 V. The zero code error is always positive because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. The ideal output is V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR).

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
The dc power supply rejection ratio indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{\text{SYNC}}$.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by first loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then, execute a software $\overline{\text{LDAC}}$ and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temp\ \ Range} \right] \times 10^6$$

where:
$V_{REF\,(MAX)}$ is the maximum reference output measured over the total temperature range.
$V_{REF\,(MIN)}$ is the minimum reference output measured over the total temperature range.
$V_{REF\,(NOM)}$ is the nominal reference output voltage, 2.5 V.
Temp Range is the specified temperature range of −40°C to +125°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5672R/AD5676R are octal, 12-/16-bit, serial input, voltage output DACs with an internal reference. The devices operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5672R/AD5676R in a 24-bit word format via a 3-wire serial interface. The AD5672R/AD5676R incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to 1 µA.

TRANSFER FUNCTION

The internal reference is on by default.

The gain of the output amplifier can be set to ×1 or ×2 using the gain select pin (GAIN) on the TSSOP or the gain bit on the LFCSP. When the GAIN pin is tied to GND, all eight DAC outputs have a span from 0 V to V_{REF}. When the GAIN pin is tied to V_{LOGIC}, all eight DACs output a span of 0 V to 2 × V_{REF}. When using the LFCSP, the gain bit in the internal reference and gain setup register is used to set the gain of the output amplifier. The gain bit is 0 by default. When the gain bit is 0, the output span of all eight DACs is 0 V to V_{REF}. When the gain bit is 1, the output span of all eight DACs is 0 V to 2 × V_{REF}. The gain bit is ignored on the TSSOP.

DAC ARCHITECTURE

The AD5672R/AD5676R implement a segmented string DAC architecture with an internal output buffer. Figure 58 shows the internal block diagram.

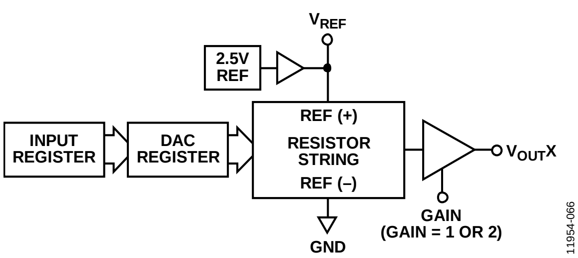


Figure 58. Single DAC Channel Architecture Block Diagram

Figure 59 shows the resistor string structure. The code loaded to the DAC register determines the node on the string where the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches and connecting the string to the amplifier. Because each resistance in the string has same value, R, the string DAC is guaranteed monotonic.

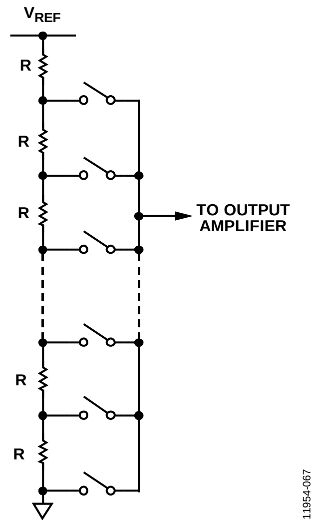


Figure 59. Resistor String Structure

Internal Reference

The AD5672R/AD5676R on-chip reference is enabled at power-up, but can be disabled via a write to the control register. See the Internal Reference Setup section for details.

The AD5672R/AD5676R have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V, depending on the state of the GAIN pin or gain bit. The internal reference associated with the device is available at the V_{REFOUT} pin. This buffered reference is capable of driving external loads of up to 15 mA.

Output Amplifiers

The output buffer amplifier generates rail-to-rail voltages on its output. The actual range depends on the value of V_{REF}, the gain setting, the offset error, and the gain error.

The output amplifiers can drive a load of 1 kΩ in parallel with 10 nF to GND. The slew rate is 0.8 V/µs with a typical ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

The AD5672R/AD5676R use a 3-wire serial interface (SYNC, SCLK, and SDI that is compatible with SPI, QSPI™, and MICROWIRE interface standards, as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence. The AD5672R/AD5676R contain an SDO pin to allow the user to daisy-chain multiple devices together (see the Daisy-Chain Operation section) or for readback.

Input Shift Register

The input shift register of the AD5672R/AD5676R is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0 (see Table 10), followed by the 4-bit DAC address bits, A3 to A0 (see Table 11), and finally, the 16-bit data-word.

The data-word comprises 12-bit or 16-bit input code, followed by zero or four don't care bits for the AD5676R and AD5672R, respectively (see Figure 60 and Figure 61). These data bits are transferred to the input register on the 24 falling edges of SCLK and are updated on the rising edge of SYNC.

Commands execute on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

Table 10. Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	No operation
0	0	0	1	Write to Input Register n where n = 1 to 8, depending on the DAC selected from the address bits in Table 11 (dependent on LDAC)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up the DAC
0	1	0	1	Hardware LDAC mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference and gain setup register
1	0	0	0	Set up the DCEN register (daisy-chain enable)
1	0	0	1	Set up the readback register (readback enable)
1	0	1	0	Update all channels of the input register simultaneously with the input data
1	0	1	1	Update all channels of the DAC register and input register simultaneously with the input data
1	1	0	0	Reserved
…	…	…	…	
1	1	1	1	No operation, daisy-chain mode

Table 11. Address Commands

Channel Address[3:0]				
A3	**A2**	**A1**	**A0**	**Selected Channel**
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7

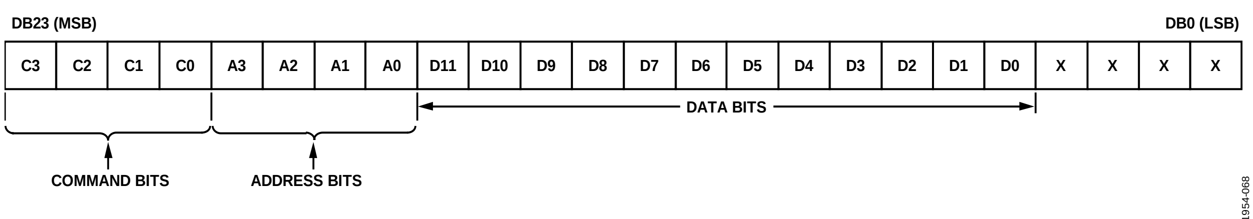


Figure 60. AD5672R Input Shift Register Content

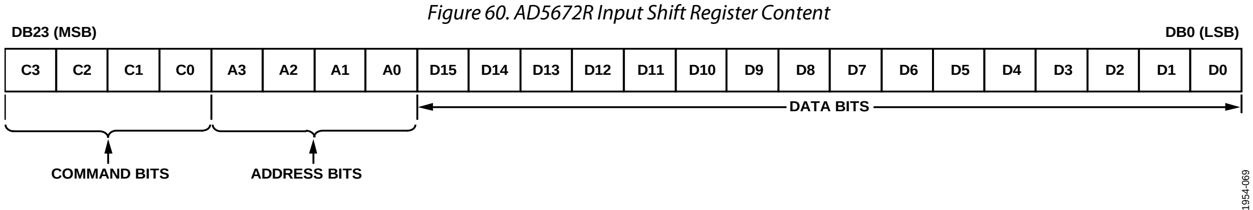


Figure 61. AD5676R Input Shift Register Content

STANDALONE OPERATION

Bring the SYNC line low to begin the write sequence. Data from the SDI line is clocked into the 24-bit input shift register on the falling edge of SCLK. After the last of 24 data bits is clocked in, bring SYNC high. The programmed function is then executed, that is, an LDAC-dependent change in DAC register contents and/or a change in the mode of operation. If SYNC is taken high at a clock before the 24^{th} clock, it is considered a valid frame, and invalid data is loaded to the DAC. Bring SYNC high for a minimum of 20 ns (single channel, see t_8 in Figure 2) before the next write sequence so that a falling edge of SYNC can initiate the next write sequence. Idle SYNC at rails between write sequences for even lower power operation. The SYNC line is kept low for 24 falling edges of SCLK, and the DAC is updated on the rising edge of SYNC.

When data is transferred into the input register of the addressed DAC, all DAC registers and outputs update by taking LDAC low while the SYNC line is high.

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on LDAC)

Command 0001 allows the user to write the dedicated input register of each DAC individually. When LDAC is low, the input register is transparent, if not controlled by the LDAC mask register.

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers and outputs with the contents of the input registers selected and updates the DAC outputs directly. Data Bit D7 to Bit D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

Write to and Update DAC Channel n (Independent of LDAC)

Command 0011 allows the user to write to the DAC registers and updates the DAC outputs directly. The address bits are used to select the DAC channel.

DAISY-CHAIN OPERATION

For systems that contain several DACs, the SDO pin can daisy-chain several devices together and is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 10). The daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The default setting is standalone mode, where DB0 = 0. Table 12 shows how the state of the bit corresponds to the mode of operation of the device.

Table 12. Daisy-Chain Enable (DCEN) Register

DB0	Description
0	Standalone mode (default)
1	DCEN mode

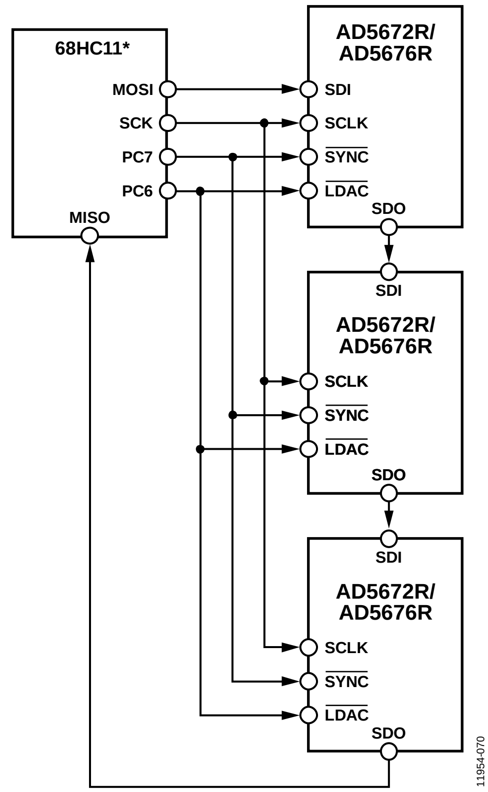


Figure 62. Daisy-Chaining the AD5672R/AD5676R

The SCLK pin is continuously applied to the input shift register when SYNC is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the SDI input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of devices updated. If SYNC is taken high at a clock that is not a multiple of 24, it is considered a valid frame, and invalid data may be loaded to the DAC. When the serial transfer to all devices is complete, SYNC goes high, which latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be continuous or a gated clock. If SYNC is held low for the correct number of clock cycles, a continuous SCLK source is used. In gated clock mode, use a burst clock containing the exact number of clock cycles, and take SYNC high after the final clock to latch the data.

READBACK OPERATION

Readback mode is invoked through a software executable readback command. If the SDO output is disabled via the daisy-chain mode disable bit in the control register, it is automatically enabled for the duration of the read operation, after which it is disabled again. Command 1001 is reserved for the readback function. This command, in association with the address bits A3 to A0, selects the DAC input register to read (see Table 10 and Table 11). Note that, during readback, only one input register can be selected. The remaining data bits in the write sequence are don't care bits. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register.

For example, to read back the DAC register for Channel 0, implement the following sequence:

1. Write 0x900000 to the AD5672R/AD5676R input register. This configures the device for read mode with the DAC register of Channel 0 selected. Note that all data bits, DB15 to DB0, are don't care bits.
2. Follow this with a second write, a no operation (NOP) condition, 0x000000 or 0xF00000 when in daisy-chain mode. During this write, the data from the register is clocked out on the SDO line. DB23 to DB20 contain undefined data, and the last 16 bits contain the DB19 to DB4 DAC register contents.

When $\overline{\text{SYNC}}$ is high, the SDO pin is driven by a weak latch, which holds the last data bit. The SDO pin can be overdriven by the SDO pin of another device, thus allowing multiple devices to be read using the same SPI interface.

POWER-DOWN OPERATION

The AD5672R/AD5676R contain two separate power-down modes. Command 0100 is designated for the power-down function (see Table 10). These power-down modes are software programmable by setting 16 bits, Bit DB15 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 13 shows how the state of the two bits corresponds to the mode of operation of the device.

Any or all DACs (DAC A to DAC D) power down to the selected mode by setting the corresponding bits. See Table 14 for the contents of the input shift register during the power-down/power-up operation.

Table 13. Modes of Operation

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
Tristate	1	1

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with a typical power consumption of 1 mA at 5 V. However, for the two power-down modes, the supply current typically falls to 1 µA. In addition to this fall, the output stage switches internally from the amplifier output to a resistor network of known values. Therefore the DAC channel output impedance is defined when the channel is powered down. There are two different power-down options. The output is either connected internally to GND through a 1 kΩ resistor or it is left open circuited (tristate). Figure 63 shows the output stage.

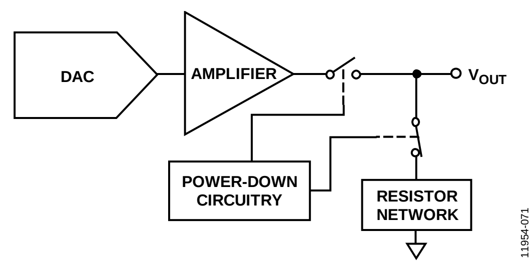


Figure 63. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register updates while the device is in power-down mode. The time required to exit power-down is typically 2.5 µs for V_{DD} = 5 V.

To reduce the current consumption further, power off the on-chip reference. See the Internal Reference Setup section.

Table 14. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation

			DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0
[DB23:DB20]	DB19	[DB18:DB16]	[DB15: B14]	[DB13: B12]	[DB11: B10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	0	XXX[1]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

[1] X means don't care

LOAD DAC (HARDWARE LDAC PIN)

The AD5672R/AD5676R DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the LDAC pin.

Instantaneous DAC Updating (LDAC Held Low)

LDAC is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of SYNC and the output begins to change (see Table 16).

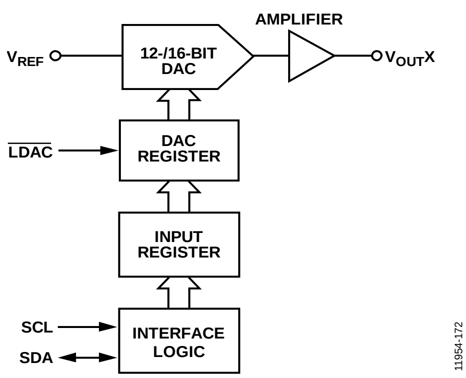


Figure 64. Simplified Diagram of Input Loading Circuitry for a Single DAC

Deferred DAC Updating (LDAC is Pulsed Low)

LDAC is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by taking LDAC low after SYNC is taken high. The update now occurs on the falling edge of LDAC.

LDAC MASK REGISTER

Command 0101 is reserved for this software LDAC function. Address bits are ignored. Writing to the DAC, using Command 0101, loads the 8-bit LDAC register (DB7 to DB0). The default for each channel is 0; that is, the LDAC pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the LDAC pin, regardless of the state of the hardware LDAC pin. This flexibility is useful in applications where the user wishes to select which channels respond to the LDAC pin.

The LDAC register gives the user extra flexibility and control over the hardware LDAC pin (see Table 15). Setting the LDAC bits (DB0 to DB7) to 0 for a DAC channel means that this channel update is controlled by the hardware LDAC pin.

Table 15. LDAC Overwrite Definition

Load LDAC Register		
LDAC Bits (DB7 to DB0)	**LDAC Pin**	**LDAC Operation**
00000000	1 or 0	Determined by the LDAC pin.
11111111	X[1]	DAC channels update and override the LDAC pin. DAC channels see LDAC as 1.

[1] X means don't care.

Table 16. Write Commands and LDAC Pin Truth Table[1]

Command	Description	Hardware LDAC Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on LDAC)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low hardware LDAC pin transition always updates the contents of the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the LDAC mask register.
[2] When LDAC is permanently tied low, the LDAC mask bits are ignored.

HARDWARE RESET ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ pin is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the $\overline{\text{RESET}}$ select pin. It is necessary to keep the $\overline{\text{RESET}}$ pin low for a minimum time (see Table 5) to complete the operation. When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the outputs cannot be updated with a new value. Any events on the $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ pins during power-on reset are ignored. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5672R/AD5676R contain a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this is outside the linear region of the DAC; by connecting the RSTSEL pin high, $V_{OUT}x$ power up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. The RSTSEL pin is only available on the TSSOP. When the AD5672R/AD5676R LFCSP is used, the outputs power up to 0 V.

SOFTWARE RESET

A software executable reset function is also available that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function. The DAC address bits must be set to 0x0 and the data bits set to 0x1234 for the software reset command to execute.

AMPLIFIER GAIN SELECTION ON LFCSP

The output amplifier gain setting for the LFCSP is determined by the state of the DB2 bit in the internal reference and gain setup register (see Table 17 and Table 18).

INTERNAL REFERENCE SETUP

The on-chip reference is on at power-up by default. To reduce the supply current, turn off this reference by setting the software programmable bit, DB0, in the control register. Table 17 shows how the state of the bit corresponds to the mode of operation. Command 0111 is reserved for setting up the internal reference and the gain setting on the LFCSP (see Table 10).

Table 17. Internal Reference and Gain Setup Register

Bit	Description
DB2	Amplifier gain setting
	DB2 = 0: amplifier gain = 1 (default)
	DB2 = 1: amplifier gain = 2
DB0	Reference enable
	DB0 = 0: internal reference enabled (default)
	DB0 = 1: internal reference disabled

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc. performs a reliability test called precondition to mimic the effect of soldering a device to a board. The output voltage specification quoted previously includes the effect of this reliability test.

Figure 65 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

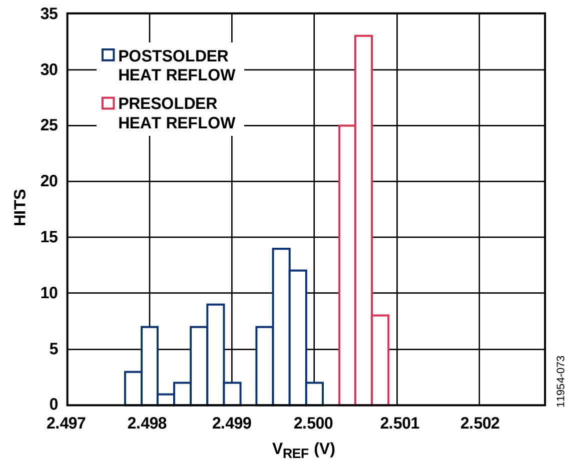


Figure 65. Solder Heat Reflow Reference Voltage Shift

LONG-TERM TEMPERATURE DRIFT

Figure 66 shows the change in V_{REF} value after 1000 hours in the life test at 150°C.

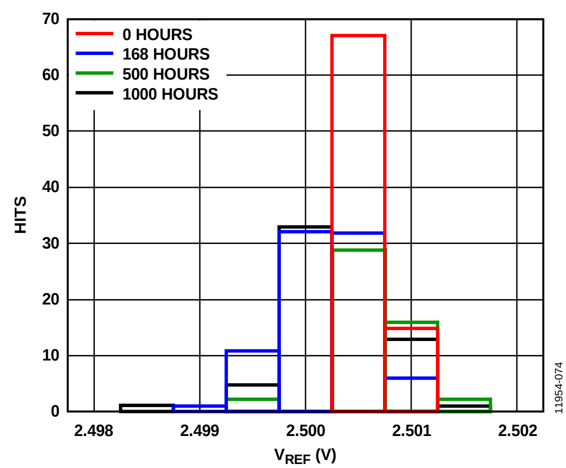


Figure 66. Reference Drift Through to 1000 Hours

Table 18. 24-Bit Input Shift Register Contents for Internal Reference and Gain Setup Command

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB3	DB2	DB1	DB0 (LSB)
0	1	1	1	Don't care	Gain	Reserved. Set to 0	Reference enable

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

Figure 67 shows thermal hysteresis data. It is measured by sweeping the temperature from ambient to −40°C, then to +125°C, and returning to ambient. The V_{REF} delta, shown in blue in Figure 67, is then measured between the two ambient measurements. The same temperature sweep and measurements were immediately repeated and the results are shown in red in Figure 67.

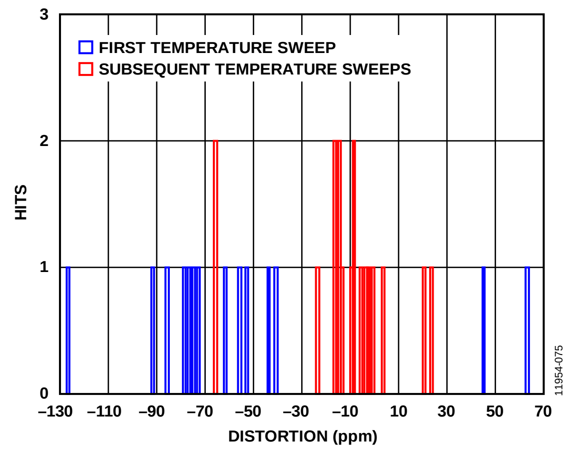


Figure 67. Thermal Hysteresis

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The following supplies typically power the AD5672R/AD5676R: V_{DD} = 3.3 V and V_{LOGIC} = 1.8 V.

The ADP7118 can be used to power the V_{DD} pin. The ADP160 can be used to power the V_{LOGIC} pin. Figure 68 shows this setup. The ADP7118 can operate from input voltages up to 20 V. The ADP160 can operate from input voltages up to 5.5 V.

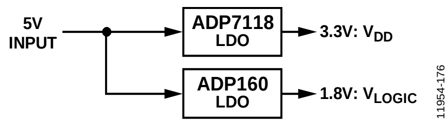


Figure 68. Low Noise Power Solution for the AD5672R/AD5676R

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5672R/AD5676R is performed via a serial bus that uses a standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The devices require a 24-bit data-word with data valid on the rising edge of $\overline{\text{SYNC}}$.

AD5672R/AD5676R TO ADSP-BF531 INTERFACE

The SPI interface of the AD5672R/AD5676R can easily connect to industry-standard DSPs and microcontrollers. Figure 69 shows the AD5672R/AD5676R connected to the Analog Devices Blackfin® DSP. The Blackfin has an integrated SPI port that can connect directly to the SPI pins of the AD5672R/AD5676R.

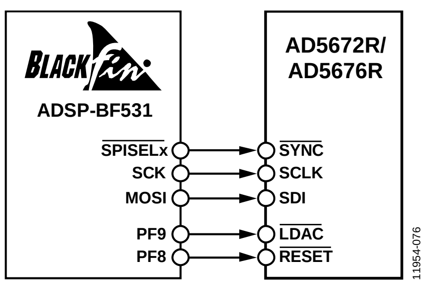


Figure 69. ADSP-BF531 Interface

AD5672R/AD5676R TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 70 shows how a SPORT interface is used to control the AD5672R/AD5676R.

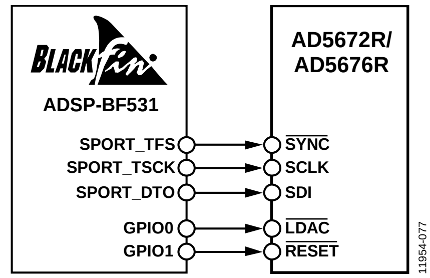


Figure 70. SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5672R/AD5676R are mounted so that the devices lie on the analog plane.

The AD5672R/AD5676R must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are tantalum bead type. The 0.1 µF capacitors must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The GND plane on the device can be increased (as shown in Figure 71) to provide a natural heat sinking effect.

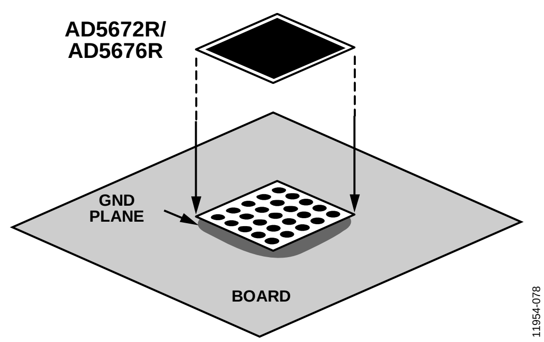
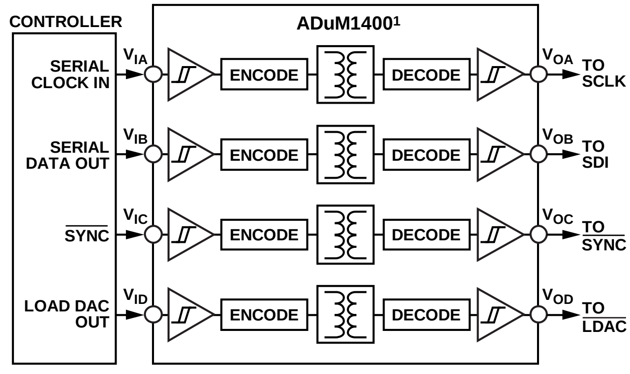


Figure 71. Pad Connection to the Board

GALVANICALLY ISOLATED INTERFACE

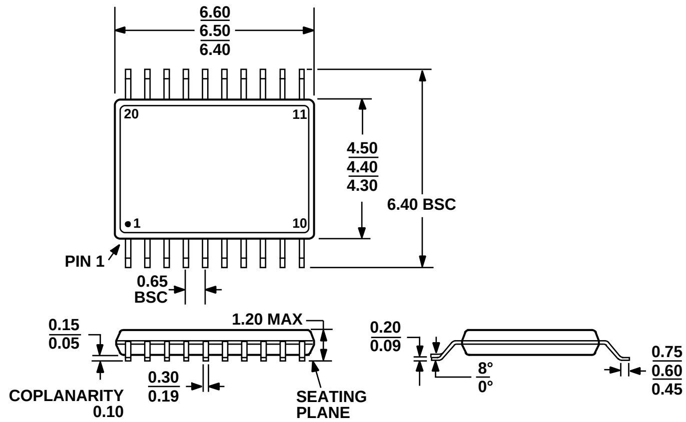
In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5672R/AD5676R makes the devices ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 72 shows a 4-channel isolated interface to the AD5672R/AD5676R using an ADuM1400. For further information, visit www.analog.com/icoupler.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

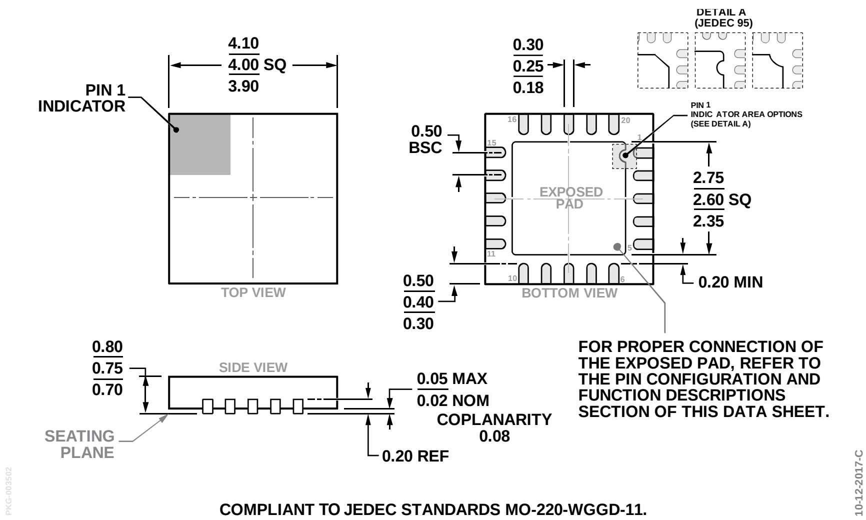
Figure 72. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 73. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 74. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Resolution (Bits)	Temperature Range	Accuracy (LSB INL)	Typical Reference Temperature Coefficient (ppm/°C)	Package Description	Package Option
AD5672RBRUZ	12	−40°C to +125°C	±1	2	20-Lead TSSOP	RU-20
AD5672RBRUZ-REEL7	12	−40°C to +125°C	±1	2	20-Lead TSSOP	RU-20
AD5672RBCPZ-REEL7	12	−40°C to +125°C	±1	2	20-Lead LFCSP	CP-20-8
AD5672RBCPZ-RL	12	−40°C to +125°C	±1	2	20-Lead LFCSP	CP-20-8
AD5676RARUZ	16	−40°C to +125°C	±8	5	20-Lead TSSOP	RU-20
AD5676RARUZ-REEL7	16	−40°C to +125°C	±8	5	20-Lead TSSOP	RU-20
AD5676RACPZ-REEL7	16	−40°C to +125°C	±8	5	20-Lead LFCSP	CP-20-8
AD5676RACPZ-RL	16	−40°C to +125°C	±8	5	20-Lead LFCSP	CP-20-8
AD5676RBRUZ	16	−40°C to +125°C	±3	2	20-Lead TSSOP	RU-20
AD5676RBRUZ-REEL7	16	−40°C to +125°C	±3	2	20-Lead TSSOP	RU-20
AD5676RBCPZ-REEL7	16	−40°C to +125°C	±3	2	20-Lead LFCSP	CP-20-8
AD5676RBCPZ-RL	16	−40°C to +125°C	±3	2	20-Lead LFCSP	CP-20-8
EVAL-AD5676RSDZ					Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5676RSDZ is used to evaluate the AD5672R and AD5676R.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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