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# AS1100

## Serially Interfaced, 8-Digit LED Driver

### 1 General Description

The AS1100 is an LED driver for 7 segment numeric displays of up to 8 digits. The AS1100 can be programmed via a conventional 4 wire serial interface.

The device includes a BCD code-B decoder, a multiplex scan circuitry, segment and display drivers, and a 64 Bit memory. The memory is used to store the LED settings, so that continuous reprogramming is not necessary.

Every individual segment can be addressed and updated separately. Only one external resistor is required to set the current through the LED display. Brightness can be controlled either in an analog or digital way. The user can choose the internal code-B decoder to display numeric digits or to address each segment directly.

The AS1100 features an extremely low shutdown current of only 20µA and an operational current of less than 500µA. The number of visible digits can be programmed as well. The AS1100 can be reset by software and an external clock can be used. Several test modes support easy debugging.

The AS1100 is offered in a 24-pin SOIC package.

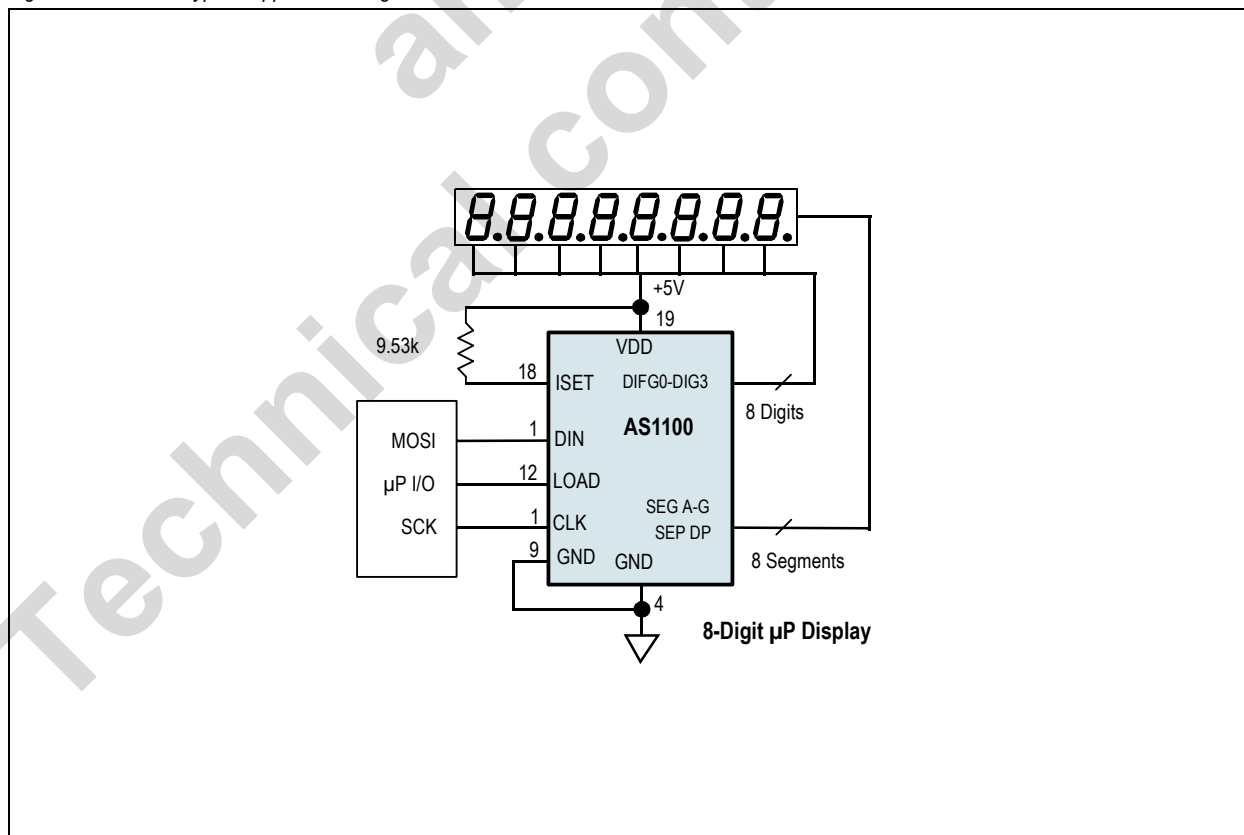
### 2 Key Features

- 10MHz Serial Interface
- Individual LED Segment Control
- Decode/No-Decode Digit Selection
- 20µA Low-Power Shutdown (Data Retained)
- Extremely low Operating Current 0.5mA in open loop
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Display
- Software Reset
- Optional External clock
- 24-pin SOIC Package

### 3 Applications

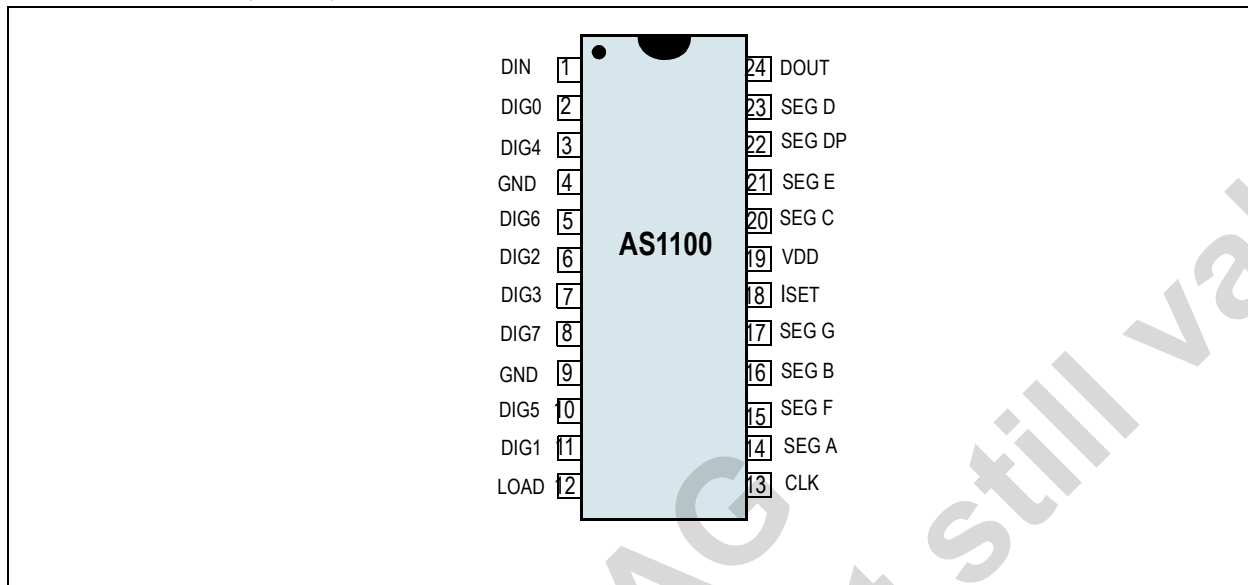
The AS1100 is an ideal solution for Bar-Graph Displays, Industrial Controllers, Panel Meters, LED Matrix Displays and White Goods such as washing machines and dishwasher.

Figure 1. AS1100 - Typical Application Diagram



## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



### 4.1 Pin Descriptions

Table 1. Pin Descriptions

| Pin Number        | Pin Name      | Description  |
|-------------------|---------------|--|
| 1                 | DIN           | <b>Data input.</b> Data is programmed into the 16Bit shift register on the rising CLK edge   |
| 2, 3, 5:8, 10, 11 | DIG 0 : DIG 7 | 8 digit driver lines that sink the current from the common cathode of the display. In shutdown mode the AS1100 switches the outputs to VDD.  |
| 4, 9              | GND           | Both GND pins must be connected.   |
| 12                | LOAD/CS       | <b>Strobe input.</b> With the rising edge of the LOAD signal the 16 bit of serial data is latched into the register.   |
| 13                | CLK           | <b>Clock input.</b> The interface is capable to support clock frequencies up to 10MHz. The serial data is clocked into the internal shift register with the rising edge of the CLK signal. On the DOUT pin the data is applied with the falling edge of CLK. |
| 14:17, 20:23      | SEGA:G, DP    | <b>Seven segment driver lines including the decimal point.</b> When a segment is turned off the output is connected to GND.  |
| 18                | ISET          | The current into ISET determines the peak current through the segments and therefore the brightness.   |
| 19                | VDD           | <b>Positive Supply Voltage (+5V)</b>   |
| 24                | DOUT          | <b>Serial data output for cascading drivers.</b> The output is valid after 16.5 clock cycles. The output is never set to high impedance.   |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter  | Min  | Max                   | Units | Notes  |
|--|------|-----------------------|-------|--|
| <b>Electrical Parameters</b>                     |      |                       |       |  |
| VDD to GND                                       | -0.3 | 7                     | V     |  |
| All other pins to GND                            | -0.3 | VDD + 0.3<br>(max 7V) | V     |  |
| <b>Current</b>                                   |      |                       |       |  |
| DIG 0: DIG 7 Sink Current                        |      | 500                   | mA    |  |
| SEG A : SEG G, SEG DP                            |      | 100                   | mA    |  |
| Latch-Up Immunity                                |      | ±200                  | mA    | Norm: JEDEC 78   |
| <b>Electrostatic Discharge</b>                   |      |                       |       |  |
| Digital outputs                                  |      | 500                   | V     | Norm: MIL 883 E method 3015  |
| All other pins                                   |      | 1000                  | V     |  |
| <b>Continuous Power Dissipation (TA = +85°C)</b> |      |                       |       |  |
| Wide SOIC  |      | 941                   | mW    | Derate 11.8mW/°C<br>above +70°C  |
| <b>Temperature Ranges and Storage Conditions</b> |      |                       |       |  |
| Storage Temperature Range                        | -55  | +150                  | °C    |  |
| Package Body Temperature (Wide SOIC)             |      | +260                  | °C    | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".<br>The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Humidity   | 5    | 85                    | %     | Non-condensing   |
| Moisture Sensitive Level                         |      | 3                     |       | Represents a max. floor life time of 168h  |

## 6 Electrical Characteristics

$V_{DD} = 5V$ ,  $R_{SET} = 9.53k\Omega \pm 1\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

| Symbol                        | Parameter                                  | Conditions   | Min          | Typ | Max  | Units         |
|-------------------------------|--|--|--------------|-----|------|---------------|
| TAMB                          | Operating Temperature Range                |  | -40          |     | +85  | °C            |
| VDD                           | Operating Supply Voltage                   |  | 4.0          | 5.0 | 5.5  | V             |
| IDDS                          | Shutdown Supply Current                    | All digital inputs at VDD or GND,<br>$T_A = +25^\circ\text{C}$ |              | 20  | 50   | $\mu\text{A}$ |
| IDD                           | Operating Supply Current                   | RSET = open circuit  |              |     | 500  | $\mu\text{A}$ |
|                               |  | All segments and decimal point on,<br>$I_{SEG} = -40\text{mA}$ |              | 330 |      | mA            |
| fOSC                          | Display Scan Rate                          | 8 digits scanned   | 500          | 800 | 1300 | Hz            |
| IDIGIT                        | Digit Drive Sink Current                   | $V_{OUT} = 0.65V$  | 320          |     |      | mA            |
| I <sub>SEG</sub>              | Segment Drive Source Current               | $T_A = +25^\circ\text{C}$ , $V_{OUT} = (V_{DD} - 1V)$          | -30          | -40 | -45  | mA            |
| $\Delta I_{SEG}$              | Segment Drive Current Matching             |  |              | 3.0 |      | %             |
| IDIGIT                        | Digit Drive Source Current                 | Digit off, $V_{DIGIT} = (V_{DD} - 0.3V)$                       | -2           |     |      | mA            |
| I <sub>SEG</sub>              | Segment Drive Sink Current                 | Segment off, $V_{SEG} = 0.3V$                                  | 5            |     |      | mA            |
| <b>Logic Inputs</b>           |  |  |              |     |      |               |
| $I_{IH}$ , $I_{IL}$           | Input Current DIN, CLK, LOAD               | $V_{IN} = 0V$ or $V_{DD}$                                      | -1           |     | 1    | $\mu\text{A}$ |
| $V_{IH}$                      | Logic High Input Voltage                   |  | 3.5          |     |      | V             |
| $V_{IL}$                      | Logic Low Input Voltage                    |  |              |     | 0.8  | V             |
| $V_{OH}$                      | Output High Voltage                        | DOUT, $I_{SOURCE} = -1\text{mA}$                               | $V_{DD} - 1$ |     |      | V             |
| $V_{OL}$                      | Output Low Voltage                         | DOUT, $I_{SINK} = 1.6\text{mA}$                                |              |     | 0.4  | V             |
|                               | Hysteresis Voltage                         | DIN, CLK, LOAD   |              | 1   |      | V             |
| <b>Timing Characteristics</b> |  |  |              |     |      |               |
| $t_{CP}$                      | CLK Clock Period                           |  | 100          |     |      | ns            |
| $t_{CH}$                      | CLK Pulse Width High                       |  | 50           |     |      | ns            |
| $t_{CL}$                      | CLK Pulse Width Low                        |  | 50           |     |      | ns            |
| $t_{CSH}$                     | CLK Rise to LOAD Rise Hold Time            |  | 0            |     |      | ns            |
| $t_{DS}$                      | DIN Setup Time                             |  | 25           |     |      | ns            |
| $t_{DH}$                      | DIN Hold Time                              |  | 0            |     |      | ns            |
| $t_{DO}$                      | Output Data Propagation Delay              | $C_{LOAD} = 50\text{pF}$                                       |              |     | 25   | ns            |
| $t_{LDCK}$                    | LOAD Rising Edge to Next Clock Rising Edge |  | 50           |     |      | ns            |
| $t_{CSW}$                     | Minimum LOAD Pulse High                    |  | 50           |     |      | ns            |
| $t_{DSPD}$                    | Data-to-Segment Delay                      |  |              |     | 2.25 | ms            |

## 7 Typical Operating Characteristics

Figure 3. Segment Driver Capability,  
VDD = 5V, Logic Level = High

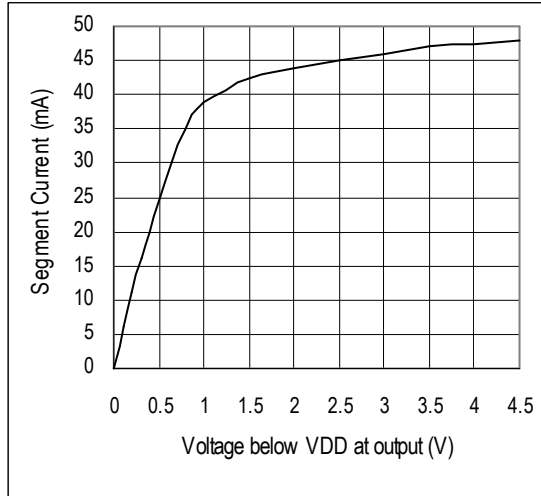
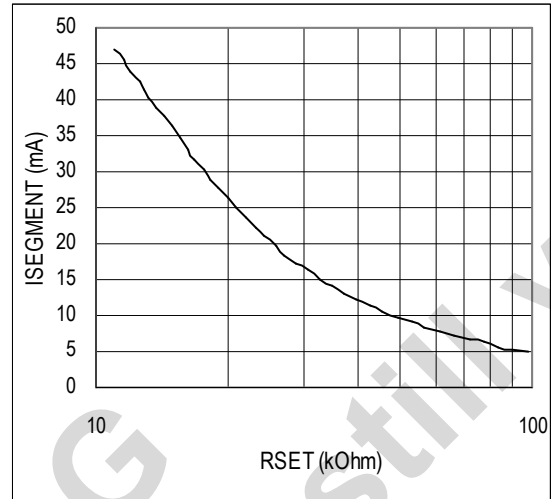


Figure 4. Segment Current vs. RSET



## 8 Detailed Description

### 8.1 Serial-Addressing Modes

Programming of the AS1100 is done via 4 wire serial interface. A programming sequence consists of 16-bit packages. The data is shifted into the internal 16 Bit register with the rising edge of the CLK signal. With the rising edge of the LOAD signal the data is latched into a digital or control register depending on the address. The LOAD signal must go to high after the 16th rising clock edge. The LOAD signal can also come later but just before the next rising edge of CLK, otherwise data would be lost. The content of the internal shift register is applied 16.5 clock cycles later to the DOUT pin. The data is clocked out at the falling edge of CLK. The Bits of the 16Bit-programming package are described in Table 5. The first 4 Bits D15-D12 are don't care, D11-D8 contain the address and D7-D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is given in Figure 5.

Figure 5. Timing Diagram

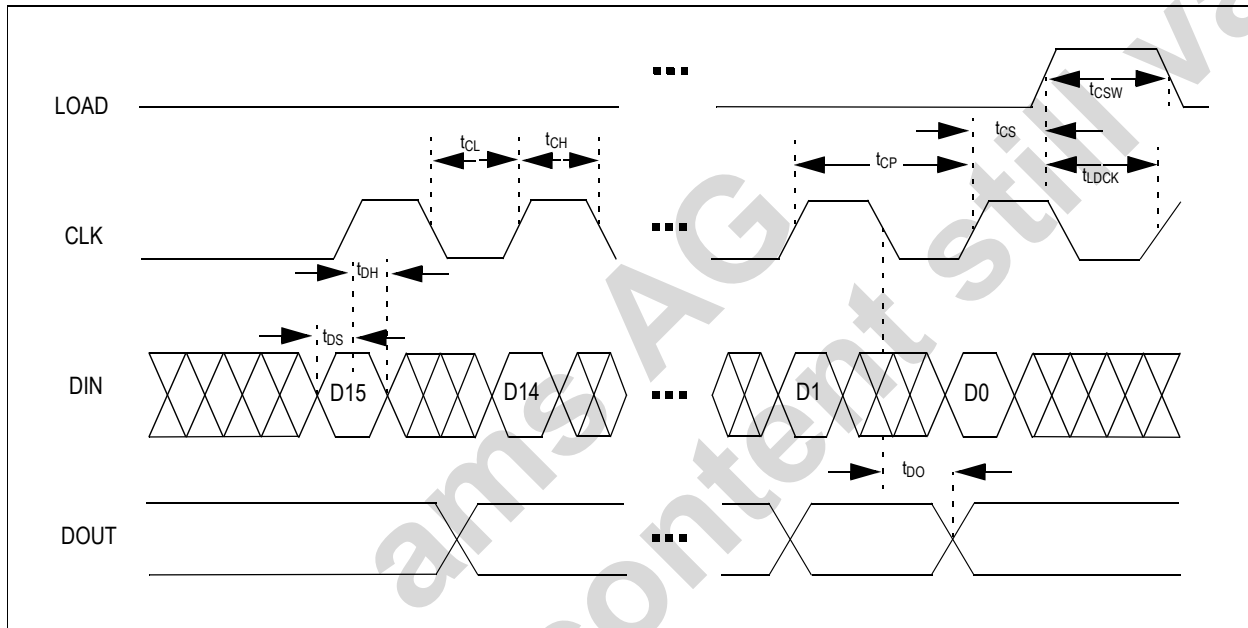


Table 4. Serial Data Format (16bits)

| D15 | D14 | D13 | D12 | D11     | D10 | D9 | D8 | D7  | D6   | D5 | D4 | D3 | D2  | D1 | D0 |
|-----|-----|-----|-----|---------|-----|----|----|-----|------|----|----|----|-----|----|----|
| X   | X   | X   | X   | Address |     |    |    | MSB | Data |    |    |    | LSB |    |    |

### 8.2 Digit and Control Registers

The AS1100 incorporates 15 registers, which are listed in Table 5. The digit and control registers are selected via the 4Bit address word. The 8 digit registers are realized with a 64bit memory. Each digit can be controlled directly without rewriting the whole contents. The control registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test, and reset/external clock register.

### 8.3 Shutdown Mode

The AS1100 features a shutdown mode, where it consumes only 20µA current. The shutdown mode is entered via a write to register 0Ch. Then all segment current sources are pulled to ground and all digit drivers are connected to VDD, so that nothing is displayed. All internal digit registers keep the programmed values. The shutdown mode can either be used for power saving or for generating a flashing display by repeatedly entering and leaving the shutdown mode. The AS1100 needs typically 250µs to exit the shutdown mode. During shutdown the AS1100 is fully programmable. Only the display test function overrides the shutdown mode.

### 8.4 Initial Power-Up

After powering up the system all register are reset, so that the display is blank. The AS1100 starts the shutdown mode. All registers should be programmed for normal operation. The default settings enable only scan of one digit, the internal decoder is disabled, data register and intensity register are set to the minimum value.

## 8.5 Decode-Mode Register

In the AS1100 a BCD decoder is included. Every digit can be selected via register 09h to be decoded. The BCD code consists of the numbers 0-9, E,H, L,P and -. In register 09h a logic high enables the decoder for the appropriate digit. In case that the decoder is bypassed (logic low) the data Bits D7-D0 correspond to the segment lines of the AS1100. In Table 7 some possible settings for register 09h are shown. Bit D7, which corresponds to the decimal point, is not affected by the settings of the decoder. Logic high means that the decimal point is displayed. In Table 8 the font of the Code B decoder is shown. In Table 9 the correspondence of the register to the appropriate segments of a 7 segment display is shown (see Figure 6).

## 8.6 Intensity Control and Interdigit Blanking

Brightness of the display can be controlled in an analog way by changing the external resistor (RSET). The current, which flows between VDD and ISET, defines the current that flows through the LEDs. The LED current is 100 times the ISET current. The minimum value of RSET should be 9.53kΩ, which corresponds to 40mA segment current. The brightness of the display can also be controlled digitally via register 0Ah. The brightness can be programmed in 16 steps and is shown in Table 10. An internal pulse width modulator controls the intensity of the display.

## 8.7 Scan-Limit Register

The scan limit register 0Bh selects the number of digits displayed. When all 8 digits are displayed the update frequency is typically 800Hz. If the number of digits displayed is reduced, the update frequency is reduced as well. The frequency can be calculated using  $8f_{OSC}/N$ , where N is the number of digits. Since the number of displayed digits influences the brightness, the resistor RSET should be adjusted accordingly. The Table 12 shows the maximum allowed current, when fewer than 4 digits are used. To avoid differences in brightness the scan limit register should not be used to blank portions of the display (leading zeros).

Table 5. Register Address Map

| Register             | Address |     |     |    |    | Hex Code |
|----------------------|---------|-----|-----|----|----|----------|
|                      | D15-D12 | D11 | D10 | D9 | D8 |          |
| No-Op                | X       | 0   | 0   | 0  | 0  | 0xX0     |
| Digit 0              | X       | 0   | 0   | 0  | 1  | 0xX1     |
| Digit 1              | X       | 0   | 0   | 1  | 0  | 0xX2     |
| Digit 2              | X       | 0   | 0   | 1  | 1  | 0xX3     |
| Digit 3              | X       | 0   | 1   | 0  | 0  | 0xX4     |
| Digit 4              | X       | 0   | 1   | 0  | 1  | 0xX5     |
| Digit 5              | X       | 0   | 1   | 1  | 0  | 0xX6     |
| Digit 6              | X       | 0   | 1   | 1  | 1  | 0xX7     |
| Digit 7              | X       | 1   | 0   | 0  | 0  | 0xX8     |
| Decode Mode          | X       | 1   | 0   | 0  | 1  | 0xX9     |
| Intensity            | X       | 1   | 0   | 1  | 0  | 0xXA     |
| Scan Limit           | X       | 1   | 0   | 1  | 1  | 0xXB     |
| Shutdown             | X       | 1   | 1   | 0  | 0  | 0xXC     |
| Not used             | X       | 1   | 1   | 0  | 1  | 0xXD     |
| Reset and ext. Clock | X       | 1   | 1   | 1  | 0  | 0xXE     |
| Display Test         | X       | 1   | 1   | 1  | 1  | 0xFF     |

Table 6. Shutdown Register Format (address (hex) = 0xXC)

| Mode             | Address Code (Hex) | Register Data |    |    |    |    |    |    |    |
|------------------|--------------------|---------------|----|----|----|----|----|----|----|
|                  |                    | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Shutdown Mode    | 0xXC               | X             | X  | X  | X  | X  | X  | X  | 0  |
| Normal Operation | 0xXC               | X             | X  | X  | X  | X  | X  | X  | 1  |



Table 7. Decode-mode Register Examples (address (hex) = 0xX9)

| Decode Mode   | Register Data |    |    |    |    |    |    |    | Hex Code |
|---|---------------|----|----|----|----|----|----|----|----------|
|   | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| No decode for digits 7–0                                  | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x00     |
| Code B decode for digit 0<br>No decode for digits 7–1     | 0             | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0x01     |
| Code B decode for digits 3–0<br>No decode for digits 7– 4 | 0             | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0x0F     |
| Code B decode for digits 7–0                              | 1             | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0xFF     |

Table 8. Code B font

| 7-Segment Character | Register Data |       |    |    |    |    | On Segments = 1 |   |   |   |   |   |   |   |
|---------------------|---------------|-------|----|----|----|----|-----------------|---|---|---|---|---|---|---|
|                     | D7*           | D6-D4 | D3 | D2 | D1 | D0 | DP*             | A | B | C | D | E | F | G |
| 0                   |               | X     | 0  | 0  | 0  | 0  |                 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1                   |               | X     | 0  | 0  | 0  | 1  |                 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2                   |               | X     | 0  | 0  | 1  | 0  |                 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3                   |               | X     | 0  | 0  | 1  | 1  |                 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4                   |               | X     | 0  | 1  | 0  | 0  |                 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5                   |               | X     | 0  | 1  | 0  | 1  |                 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6                   |               | X     | 0  | 1  | 1  | 0  |                 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7                   |               | X     | 0  | 1  | 1  | 1  |                 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8                   |               | X     | 1  | 0  | 0  | 0  |                 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9                   |               | X     | 1  | 0  | 0  | 1  |                 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| --                  |               | X     | 1  | 0  | 1  | 0  |                 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| E                   |               | X     | 1  | 0  | 1  | 1  |                 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| H                   |               | X     | 1  | 1  | 0  | 0  |                 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| L                   |               | X     | 1  | 1  | 0  | 1  |                 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| P                   |               | X     | 1  | 1  | 1  | 0  |                 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| blank               |               | X     | 1  | 1  | 1  | 1  |                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note:** The decimal point is set by bit D7 = 1

Table 9. No-decode Mode Data Bits and Corresponding Segment Lines

|                            | Register Data |    |    |    |    |    |    |    |
|----------------------------|---------------|----|----|----|----|----|----|----|
|                            | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Corresponding Segment Line | DP            | A  | B  | C  | D  | E  | F  | G  |

Figure 6. Standard 7-segment LED

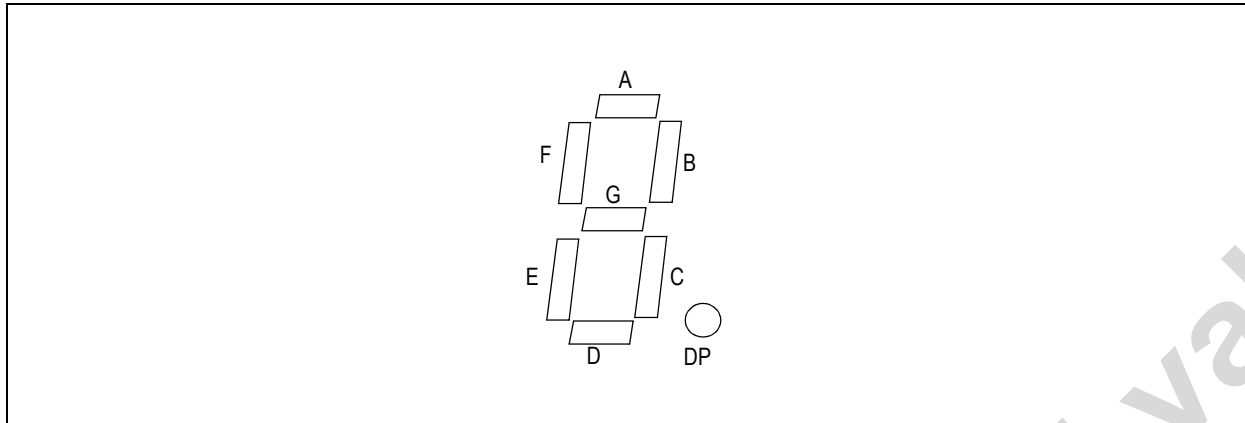


Table 10. Intensity Register Format (address (hex) = 0xXA)

| Duty Cycle     | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex Code |
|----------------|----|----|----|----|----|----|----|----|----------|
| 1/32 (min on)  | X  | X  | X  | X  | 0  | 0  | 0  | 0  | 0xX0     |
| 3/32           | X  | X  | X  | X  | 0  | 0  | 0  | 1  | 0xX1     |
| 5/32           | X  | X  | X  | X  | 0  | 0  | 1  | 0  | 0xX2     |
| 7/32           | X  | X  | X  | X  | 0  | 0  | 1  | 1  | 0xX3     |
| 9/32           | X  | X  | X  | X  | 0  | 1  | 0  | 0  | 0xX4     |
| 11/32          | X  | X  | X  | X  | 0  | 1  | 0  | 1  | 0xX5     |
| 13/32          | X  | X  | X  | X  | 0  | 1  | 1  | 0  | 0xX6     |
| 15/32          | X  | X  | X  | X  | 0  | 1  | 1  | 1  | 0xX7     |
| 17/32          | X  | X  | X  | X  | 1  | 0  | 0  | 0  | 0xX8     |
| 19/32          | X  | X  | X  | X  | 1  | 0  | 0  | 1  | 0xX9     |
| 21/32          | X  | X  | X  | X  | 1  | 0  | 1  | 0  | 0xXA     |
| 23/32          | X  | X  | X  | X  | 1  | 0  | 1  | 1  | 0xXB     |
| 25/32          | X  | X  | X  | X  | 1  | 1  | 0  | 0  | 0xXC     |
| 27/32          | X  | X  | X  | X  | 1  | 1  | 0  | 1  | 0xXD     |
| 29/32          | X  | X  | X  | X  | 1  | 1  | 1  | 0  | 0xXE     |
| 31/32 (max on) | X  | X  | X  | X  | 1  | 1  | 1  | 1  | 0xFF     |

Table 11. Scan-limit Register Format (address (hex) = 0xXB)

| Decode Mode                   | Register Data |    |    |    |    |    |    |    | Hex Code |
|-------------------------------|---------------|----|----|----|----|----|----|----|----------|
|                               | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |          |
| Display digit 0 only          | X             | X  | X  | X  | X  | 0  | 0  | 0  | 0xX0     |
| Display digit 0 & 1           | X             | X  | X  | X  | X  | 0  | 0  | 1  | 0xX1     |
| Display digit 0 1 2           | X             | X  | X  | X  | X  | 0  | 1  | 0  | 0xX2     |
| Display digit 0 1 2 3         | X             | X  | X  | X  | X  | 0  | 1  | 1  | 0xX3     |
| Display digit 0 1 2 3 4       | X             | X  | X  | X  | X  | 1  | 0  | 0  | 0xX4     |
| Display digit 0 1 2 3 4 5     | X             | X  | X  | X  | X  | 1  | 0  | 1  | 0xX5     |
| Display digit 0 1 2 3 4 5 6   | X             | X  | X  | X  | X  | 1  | 1  | 0  | 0xX6     |
| Display digit 0 1 2 3 4 5 6 7 | X             | X  | X  | X  | X  | 1  | 1  | 1  | 0xX7     |

## 8.8 Display Test Register

With the display test register 0Fh all LED can be tested. In the test mode all LEDs are switched on at maximum brightness (duty cycle 31/32). All programming of digit and control registers are maintained. The format of the register is given in Table 13.

Table 12. Maximum Segment Current for 1-, 2-, or 3-digit Displays

| Number of digits Displayed | Maximum Segment Current (mA) |
|----------------------------|------------------------------|
| 1                          | 10                           |
| 2                          | 20                           |
| 3                          | 30                           |

Table 13. Display-test Register Format (address (hex) = 0xXF)

| Mode              | Register Data |    |    |    |    |    |    |    |
|-------------------|---------------|----|----|----|----|----|----|----|
|                   | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Normal Operation  | X             | X  | X  | X  | X  | X  | X  | 0  |
| Display Test Mode | X             | X  | X  | X  | X  | X  | X  | 1  |

**Note:** The AS1100 remains in display-test mode until the display-test register is reconfigured for normal operation.

## 8.9 No-Op Register (Cascading of AS1100)

The no-operation register 00h is used when AS1100s are cascaded in order to support more than 8 digit displays. The cascading must be done in a way that all DOUT are connected to DIN of the following AS1100. The LOAD and CLK signals are connected to all devices. For a write operation for example to the fifth device the command must be followed by four no-operation commands. When the LOAD signal finally goes to high all shift registers are latched. The first four devices have got no-operation commands and only the fifth device sees the intended command and updates its register.

## 8.10 Reset and External Clock Register

This register is addressed via the serial interface. It allows to switch the device to external clock mode (If D0=1 the CLK pin of the serial interface operates as system clock input.) and to apply an external reset (D1). This brings all registers (except reg. E) to default state. For standard operation the register contents should be "00h".

Table 14. Reset and External Clock Register (address (hex) = 0xXE)

| Mode                             | Address code (Hex) | Register Data |    |    |    |    |    |    |    |
|----------------------------------|--------------------|---------------|----|----|----|----|----|----|----|
|                                  |                    | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Normal Operation, internal clock | 0xXE               | X             | X  | X  | X  | X  | X  | 0  | 0  |
| Normal Operation, external clock | 0xXE               | X             | X  | X  | X  | X  | X  | 0  | 1  |
| Reset state, internal clock      | 0xXE               | X             | X  | X  | X  | X  | X  | 1  | 0  |
| Reset state, external clock      | 0xXE               | X             | X  | X  | X  | X  | X  | 1  | 1  |

## 9 Application Information

### 9.1 Supply Bypassing and Wiring

In order to achieve optimal performance the AS1100 shall be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance. Furthermore, it is recommended to connect a 10 $\mu$ F electrolytic and a 0.1 $\mu$ F ceramic capacitor between VDD and GND to avoid power supply ripple. Also, both GNDs must be connected to ground.

### 9.2 Selecting R<sub>SET</sub> Resistor and Using External Drivers

The current through the segments is controlled via the external resistor R<sub>SET</sub>. Segment current is about 100 times the current in ISET. The right values for ISET are given in Table 15. The maximum current the AS1100 can drive is 40mA. If higher currents are needed, external drivers must be used. In that case it is no longer necessary that the AS1100 drives high currents. A recommended value for R<sub>SET</sub> is 47k $\Omega$ . In cases that the AS1100 only drives few digits, Table 12 specifies the maximum currents and R<sub>SET</sub> must be set accordingly. Refer to absolute maximum ratings to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 15. R<sub>SET</sub> vs. Segment Current and LED Forward Voltage

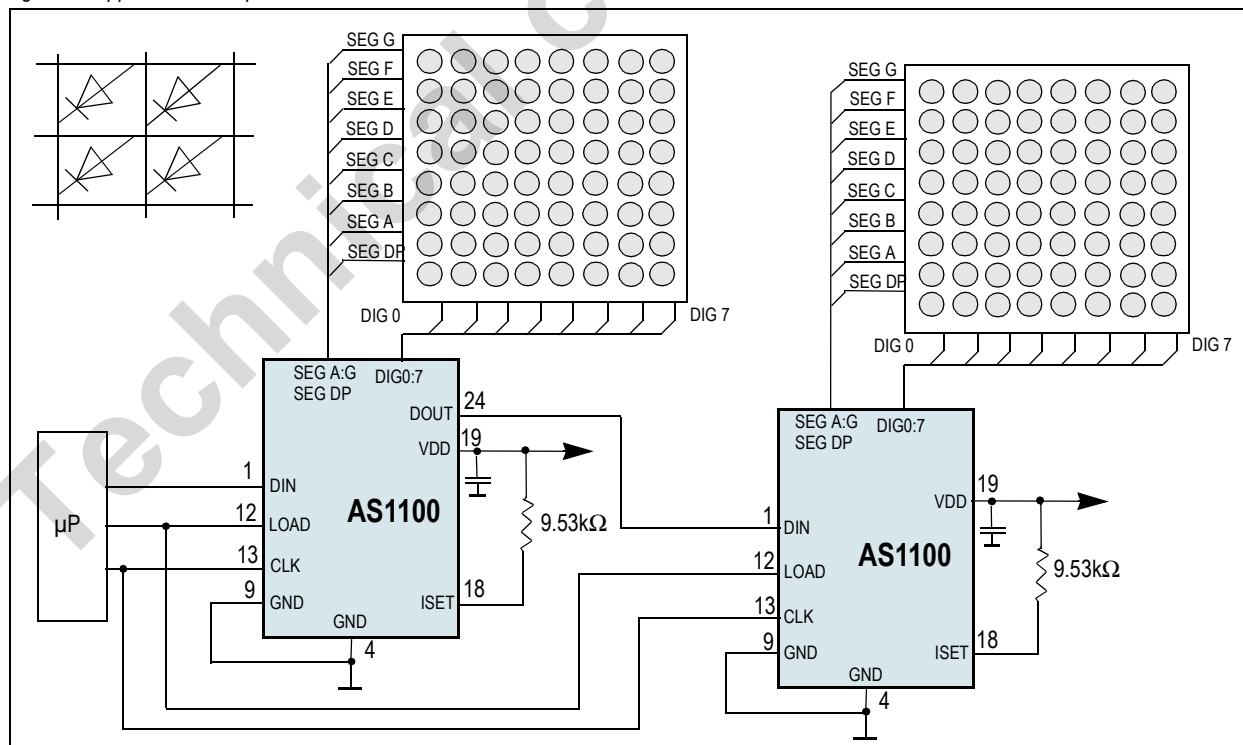
| ISEG (mA) | VLED(V)        |                |                |                |                |
|-----------|----------------|----------------|----------------|----------------|----------------|
|           | 1.5            | 2.0            | 2.5            | 3.0            | 3.5            |
| 40        | 12.2k $\Omega$ | 11.8k $\Omega$ | 11.0k $\Omega$ | 10.6k $\Omega$ | 9.69k $\Omega$ |
| 30        | 17.8k $\Omega$ | 17.1k $\Omega$ | 15.8k $\Omega$ | 15.0k $\Omega$ | 14.0k $\Omega$ |
| 20        | 29.8k $\Omega$ | 28.0k $\Omega$ | 25.9k $\Omega$ | 24.5k $\Omega$ | 22.6k $\Omega$ |
| 10        | 66.7k $\Omega$ | 63.7k $\Omega$ | 59.3k $\Omega$ | 55.4k $\Omega$ | 51.2k $\Omega$ |

### 9.3 8x8 LED Dot Matrix Driver

The example in Figure 7 uses the AS1100 to drive an 8x8 LED dot matrix. The LED columns have common cathode and are connected to the DIG0-7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as shown in Table 5. The decode mode register (0x9) has to be programmed to '00000000' as stated in Table 4. The single LEDs in a column can be addressed as stated in Table 9, where D0 corresponds to segment G and D7 corresponds to segment DP.

**Note:** For a multiple-digit dot matrix, multiple AS1100 devices must be cascaded.

Figure 7. Application Example as LED Dot Matrix Driver



## 9.4 Calculating the Power Dissipation

The upper limit for power dissipation (PD) for the AS1100 is determined from the following equation:

$$PD = (V_{DD} \times 0.5mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N) \quad (EQ 1)$$

### Where:

V<sub>DD</sub> = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 8)

V<sub>LED</sub> = LED forward voltage

I<sub>SEG</sub> = segment current set by R<sub>SET</sub>

Dissipation Example:

I<sub>SEG</sub> = 40mA, N = 8, DUTY = 31/32, V<sub>LED</sub> = 1.8V at 40mA, V<sub>DD</sub> = 5.25V

PD = 5.25V(0.5mA) + (5.25V - 1.8V)(31/32 x 40mA x 8) = 1.07W

Thus, for a PDIP package  $\theta_{JA} = +75^{\circ}\text{C/W}$  (from Table 13), the maximum allowed ambient temperature T<sub>A</sub> is given by:

$$T_{J,MAX} = T_A + PD \times \theta_{JA} = 150^{\circ}\text{C} = T_A + 1.07\text{W} \times 75^{\circ}\text{C/W}$$

### Where:

T<sub>A</sub> = +69.7°C.

The T<sub>A</sub> limit for SO Packages in the dissipation example above is +59.0°C.

Table 16. Package Thermal Resistance Data

| Package   | Thermal Resistance ( $\theta_{JA}$ ) |
|---|--------------------------------------|
| 24 Wide SO  | +85°C/w                              |
| Maximum Junction Temperature (T <sub>J</sub> ) = +150°C |                                      |
| Maximum Ambient Temperature (T <sub>A</sub> ) = +85°C   |                                      |

## 10 Package Drawings and Markings

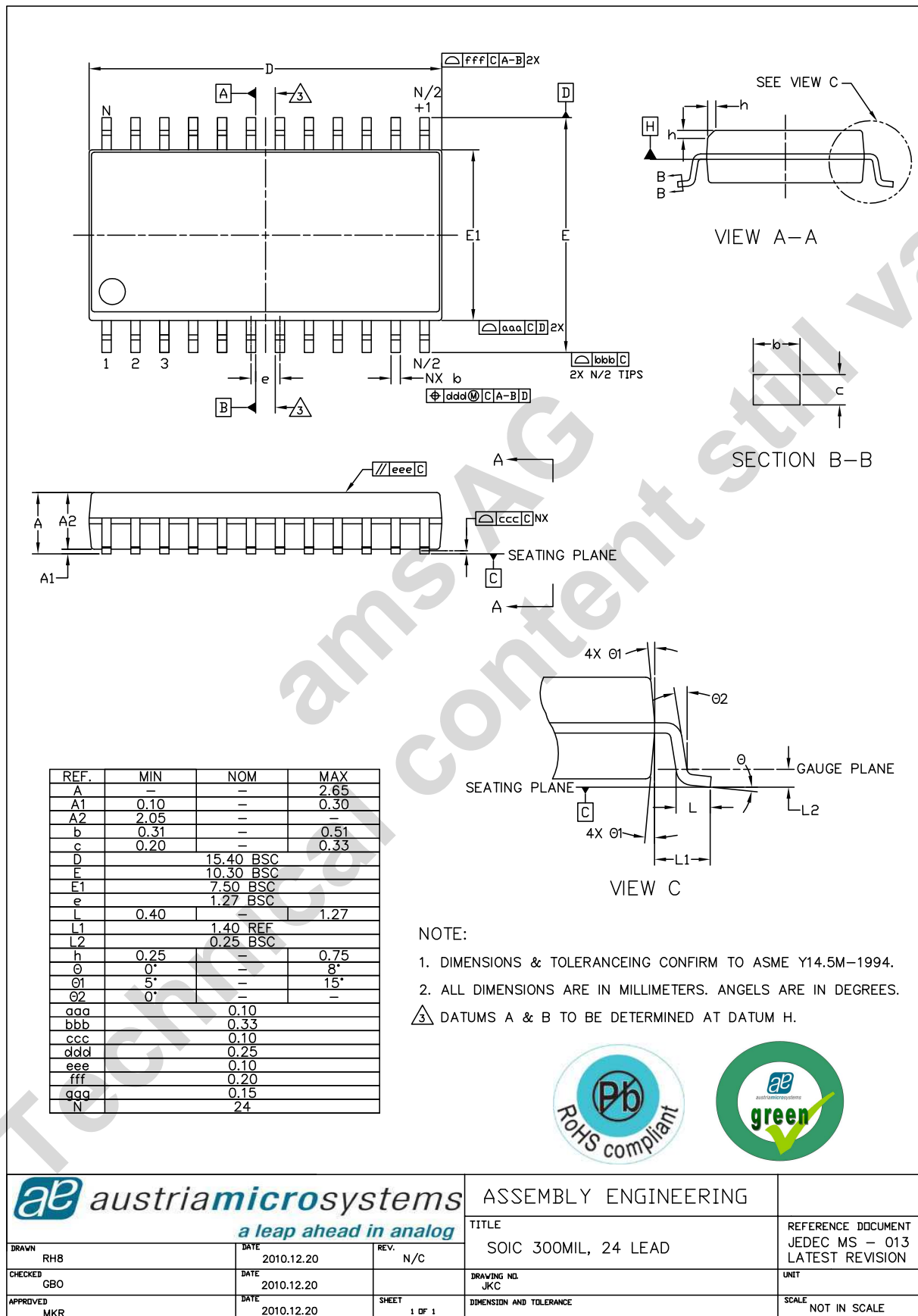
Figure 8. AS1100 Marking



Table 17. Packaging Code YYWWQZZ

| YY                                  | WW                 | Q                | ZZ                              |
|-------------------------------------|--------------------|------------------|---------------------------------|
| last two digits of the current year | manufacturing week | plant identifier | free choice / traceability code |

Figure 9. SOIC 24-pin Package Diagram



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|                               |                    |   |
|-------------------------------|--------------------|---|
| ASSEMBLY ENGINEERING          |                    |   |
| TITLE<br>SOIC 300MIL, 24 LEAD |                    | REFERENCE DOCUMENT<br>JEDEC MS - 013<br>LATEST REVISION |
| DRAWN<br>RHS                  | DATE<br>2010.12.20 | REV.<br>N/C   |
| CHECKED<br>GBO                | DATE<br>2010.12.20 | DRAWING NO.<br>JKC                                      |
| APPROVED<br>MKR               | DATE<br>2010.12.20 | SHEET<br>1 OF 1   |
| DIMENSION AND TOLERANCE       |                    | SCALE<br>NOT IN SCALE                                   |

## 11 Ordering Information

The device is available as the standard products shown in [Table 18](#).

Table 18. Ordering Information

| Ordering Code | Marking  | Description                             | Temp Range     | Delivery Form | Package     |
|---------------|----------|---|----------------|---------------|-------------|
| AS1100WL      | AS1100WL | Serially Interfaced, 8-Digit LED Driver | 0°C to +70°C   | Tubes         | SOIC 24-pin |
| AS1100WE      | AS1100WE | Serially Interfaced, 8-Digit LED Driver | -40°C to +85°C | Tubes         | SOIC 24-pin |
| AS1100WL-T    | AS1100WL | Serially Interfaced, 8-Digit LED Driver | 0°C to +70°C   | Tape & Reel   | SOIC 24-pin |
| AS1100WE-T    | AS1100WE | Serially Interfaced, 8-Digit LED Driver | -40°C to +85°C | Tape & Reel   | SOIC 24-pin |

**Note:** All products are RoHS compliant and austriamicrosystems green.

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