DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4016
Quad bilateral switches

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

Quad bilateral switches 74HC/HCT4016

FEATURES

- Low “ON” resistance:
  160 Ω (typ.) at V_{CC} = 4.5 V
  120 Ω (typ.) at V_{CC} = 6.0 V
  80 Ω (typ.) at V_{CC} = 9.0 V
- Individual switch controls
- Typical “break before make” built in
- Output capability: non-standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT4016 are high-speed Si-gate CMOS devices and are pin compatible with the “4016” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4016 have four independent analog switches (transmission gates).
Each switch has two input/output terminals (Y_n, Z_n) and an active HIGH enable input (E_n). When E_n is connected to V_{CC}, a low bidirectional path between Y_n and Z_n is established (ON condition). When E_n is connected to ground (GND), the switch is disabled and a high impedance between Y_n and Z_n is established (OFF condition).

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; V_{CC} >> (V_Y, V_Z) >> GND. Inputs Y_n and Z_n are electrically equivalent terminals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/ t_{PZL}	turn “ON” time E_n to V_{OS}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	16	17	ns
t_{PHZ}/ t_{PLZ}	turn “OFF” time E_n to V_{OS}		14	20	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	12	12	pF
C_S	max. switch capacitance		5	5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs

   C_L = output load capacitance in pF
   C_S = max. switch capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	Y_0 to Y_3	independent inputs/outputs
7	GND	ground (0 V)
2, 3, 9, 10	Z_0 to Z_3	independent inputs/outputs
13, 5, 6, 12	E_0 to E_3	enable inputs (active HIGH)
14	V_{CC}	positive supply voltage

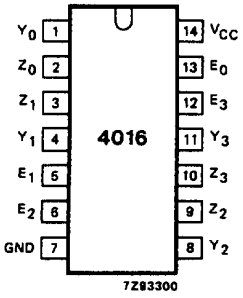


Fig.1 Pin configuration.

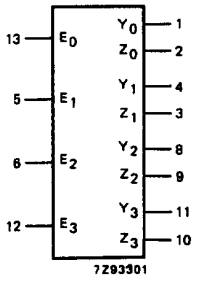


Fig.2 Logic symbol.

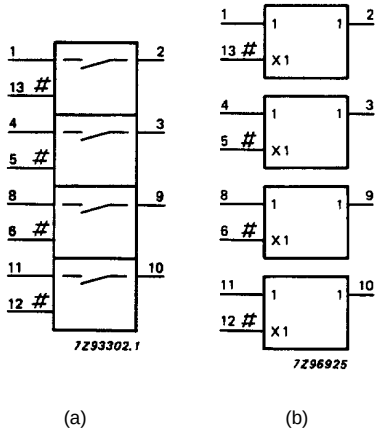


Fig.3 IEC logic symbol.

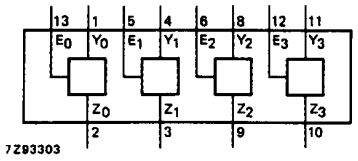


Fig.4 Functional diagram.

APPLICATIONS

- Signal gating
- Modulation
- Demodulation
- Chopper

FUNCTION TABLE

INPUT E_n	CHANNEL IMPEDANCE
L	high
H	low

Notes

1. H = HIGH voltage level
   L = LOW voltage level

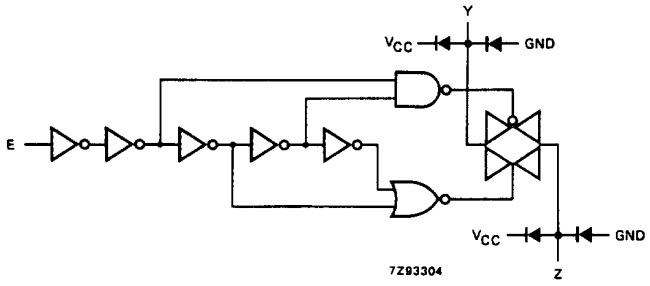


Fig.5 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V V_{CC} = 10.0 V

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V

For 74HCT: V_{CC} = 4.5 V

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS			
		74HC/HCT											
		+25			−40 to +85		−40 to +125			V_{CC} (V)	I_S (μA)	V_{is}	V_I
		min.	typ.	max.	min.	max.	min.	max.					
R_{ON}	ON resistance (peak)		– 160 120 85	– 320 240 170		– 400 300 213		– 480 360 255	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC} to GND	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		160 80 70 60	– 160 140 120		– 200 175 150		– 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND	V_{IH} or V_{IL}
R_{ON}	ON resistance (rail)		170 90 80 65	– 180 160 135		– 225 200 170		– 270 240 205	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V_{CC}	V_{IH} or V_{IL}
ΔR_{ON}	maximum ΔON resistance between any two channels		– 16 12 9						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V_{CC} to GND	V_{IH} or V_{IL}

Notes to the DC Characteristics

1. At supply voltages approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
2. For test circuit measuring R_{ON} see Fig.6.

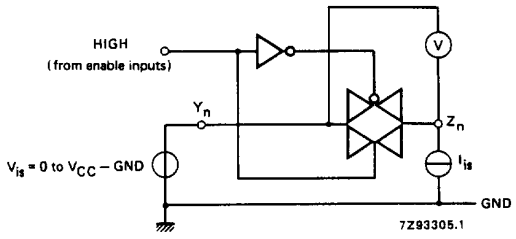


Fig.6 Test circuit for measuring R_{ON}.

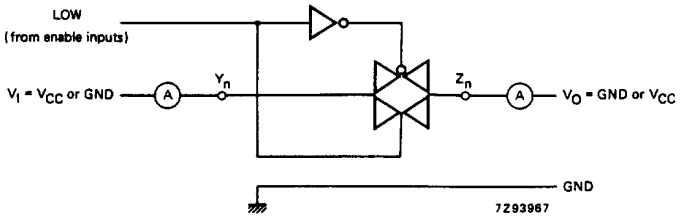


Fig.7 Test circuit for measuring OFF-state current.

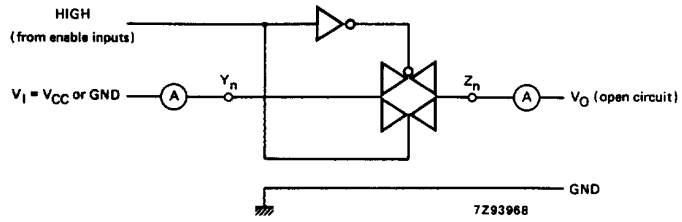


Fig.8 Test circuit for measuring ON-state current.

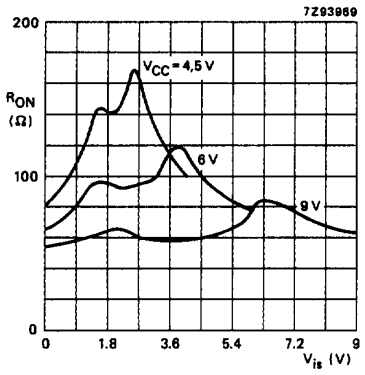


Fig.9 Typical R_{ON} as a function of input voltage V_{is} for V_{is} = 0 to V_{CC}.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.3		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70		0.50 1.35 1.80 2.70	V	2.0 4.5 6.0 9.0		
$\pm I_I$	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	µA	6.0 10.0	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	µA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig.7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	µA	10.0	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig.8)
I_{CC}	quiescent supply current			2.0 4.0		20.0 40.0		40.0 80.0	µA	6.0 10.0	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		17 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0	R_L = ∞; C_L = 50 pF (see Fig.16)
t_{PZH}/ t_{PZL}	turn “ON” time E_n to V_{os}		52 19 15 11	190 38 32 28		240 48 41 35		235 57 48 42	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PHZ}/ t_{PLZ}	turn “OFF” time E_n to V_{os}		47 17 14 13	145 29 25 22		180 36 31 28		220 44 38 33	ns	2.0 4.5 6.0 9.0	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_S$	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig.7)
$\pm I_S$	analog switch ON-state current			0.1		1.0		1.0	μA	5.5	V_{IH} or V_{IL}	$\lvert V_S \rvert$ = V_{CC} − GND (see Fig.8)
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	4.5 to 5.5	V_{CC} or GND	V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} –2.1V	other inputs at V_{CC} or GND

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
E_N	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay V_{is} to V_{os}		6	12		15		18	ns	4.5	$R_L = \infty$; C_L = 50 pF (see Fig.16)
t_{PZH}	turn “ON” time E_n to V_{os}		19	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PZL}	turn “ON” time E_n to V_{os}		20	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)
t_{PHZ}/ t_{PLZ}	turn “OFF” time E_n to V_{os}		23	35		44		53	ns	4.5	R_L = 1 kΩ; C_L = 50 pF (see Figs 17 and 18)

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} (V)	$V_{is(p-p)}$ (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.80 0.40	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig.14)
	sine-wave distortion f = 10 kHz	2.40 1.20	% %	4.5 9.0	4.0 8.0	R_L = 10 kΩ; C_L = 50 pF (see Fig.14)
	switch “OFF” signal feed-through	−50 −50	dB dB	4.5 9.0	note 3	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Figs 10 and 15)
	crosstalk between any two switches	−60 −60	dB dB	4.5 9.0	note 3	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (see Fig.12)
$V_{(p-p)}$	crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 220	mV mV	4.5 9.0		R_L = 600 Ω; C_L = 50 pF; f = 1 MHz (E_n, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns) (see Fig.13)
f_{max}	minimum frequency response (−3dB)	150 160	MHz MHz	4.5 9.0	note 4	R_L = 50 Ω; C_L = 10 pF (see Figs 11 and 14)
C_S	maximum switch capacitance	5	pF			

Notes

1. V_{is} is the input voltage at a Y_n or Z_n terminal, whichever is assigned as an input.
2. V_{os} is the output voltage at a Y_n or Z_n terminal, whichever is assigned as an output.
3. Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
4. Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

Test conditions:
V_{CC} = 4.5 V; GND = 0 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

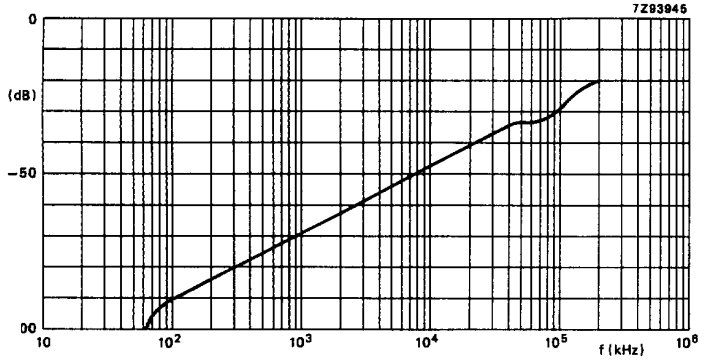


Fig.10 Typical switch “OFF” signal feed-through as a function of frequency.

Test conditions:
V_{CC} = 4.5 V; GND = 0 V;
R_L = 50 Ω; R_{source} = 1 kΩ.

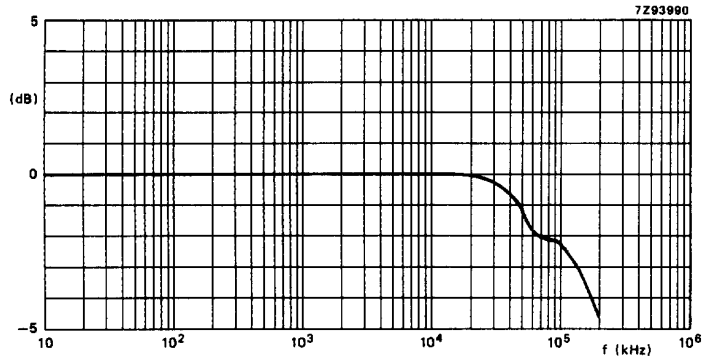


Fig.11 Typical frequency response.

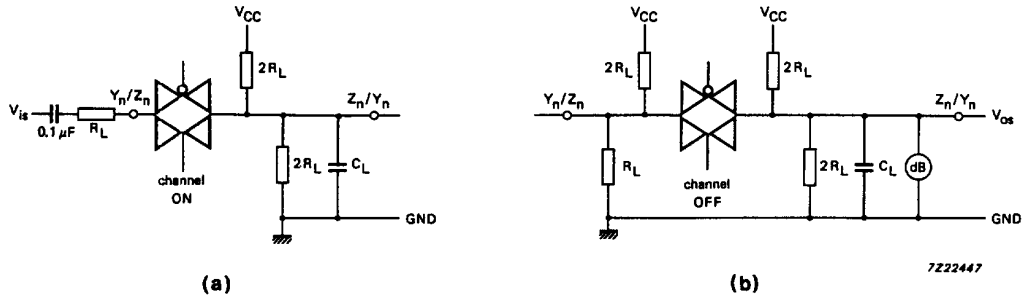
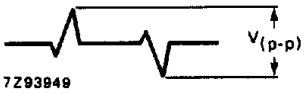


Fig.12 Test circuit for measuring crosstalk between any two switches.
(a) channel ON condition; (b) channel OFF condition.

The crosstalk is defined as follows (oscilloscope output):



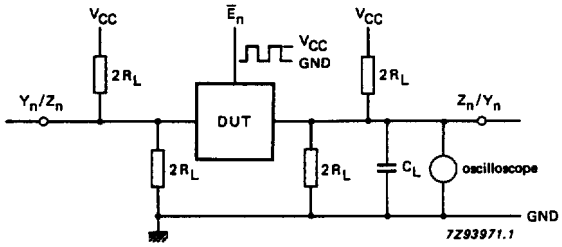


Fig.13 Test circuit for measuring crosstalk between control and any switch.

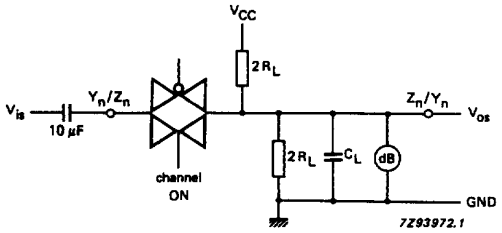


Fig.14 Test circuit for measuring sine-wave distortion and minimum frequency response.

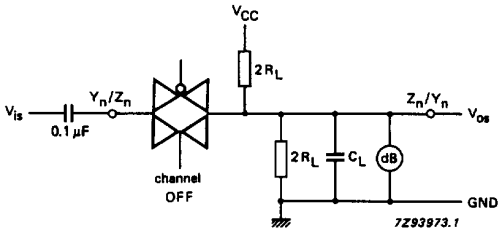
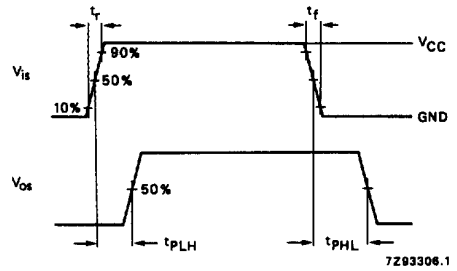


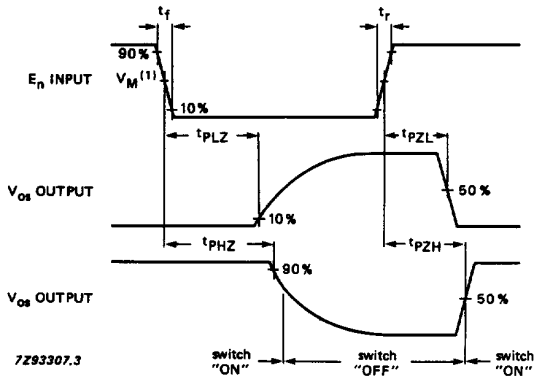
Fig.15 Test circuit for measuring switch “OFF” signal feed-through.

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.16 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.



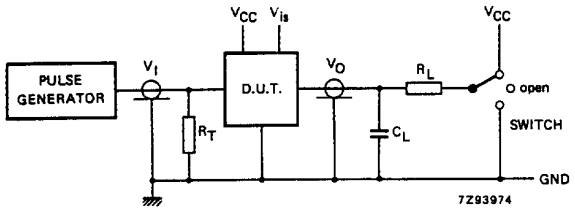
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.17 Waveforms showing the turn-ON and turn-OFF times.

TEST CIRCUIT AND WAVEFORMS

Conditions

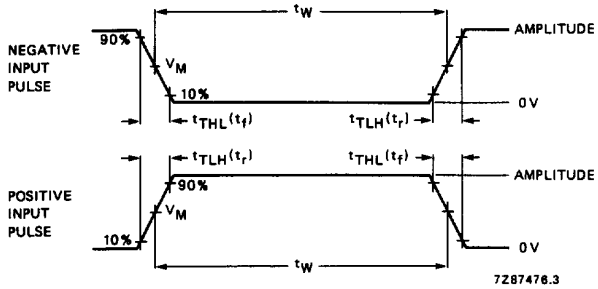
TEST	SWITCH	V_{is}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
others	open	pulse



C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
$t_r = t_f$ = 6 ns; when measuring f_{max}, there is no constraint t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Fig.18 Test circuit for measuring AC performance.



C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
$t_r = t_f$ = 6 ns; when measuring f_{max}, there is no constraint t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Fig.19 Input pulse definitions.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

LifeElectronics
Живое партнерство

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