MCP6546/6R/6U/7/8/9

Open-Drain Output Sub-Microamp Comparators

Features

- Low Quiescent Current: 600 nA/Comparator (typical)
- Rail-to-Rail Input: V_{SS} - 0.3V to V_{DD} + 0.3V
- Open-Drain Output: $V_{OUT} \leq 10V$
- Propagation Delay: 4 µs (typical, 100 mV Overdrive)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Single Available in SOT-23-5, SC-70-5* Packages
- Available in Single, Dual and Quad
- Chip Select ($\overline{CS}$) with MCP6548
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typical)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Typical Applications

- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multi-vibrators

Related Devices

- CMOS/TTL-Compatible Output: MCP6541/2/3/4

Description

The Microchip Technology Inc. MCP6546/6R/6U/7/8/9 family of comparators, is offered in single (MCP6546, MCP6546R, MCP6546U), single with chip select ($\overline{CS}$) (MCP6548), dual (MCP6547) and quad (MCP6549) configurations. The outputs are open-drain and are capable of driving heavy DC or capacitive loads.

These comparators are optimized for low power, single-supply application with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The open-drain output of the MCP6546/6R/6U/7/8/9 family can be used as a level-shifter for up to 10V using a pull-up resistor. It can also be used as a wired-OR logic. The internal Input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. These comparators operate with a single-supply voltage as low as 1.6V and draw a quiescent current of less than 1 µA/comparator.

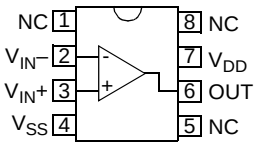
The related MCP6541/2/3/4 family of comparators from Microchip has a push-pull output that supports rail-to-rail output swing and interfaces with CMOS/TTL logic.

* SC-70-5 E-Temp parts are not available at this release of the data sheet.

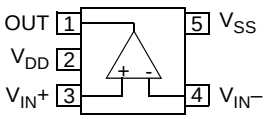
MCP6546U SOT-23-5 is E-Temp only.

Package Types

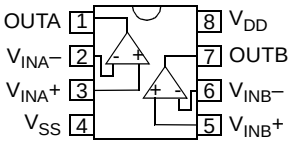
MCP6546
PDIP, SOIC, MSOP



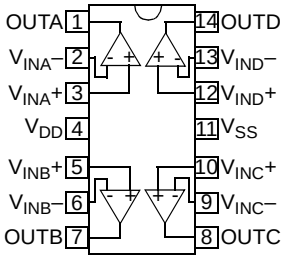
MCP6546R
SOT-23-5



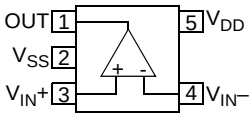
MCP6547
PDIP, SOIC, MSOP



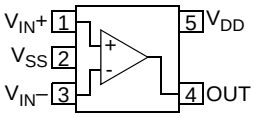
MCP6549
PDIP, SOIC, TSSOP



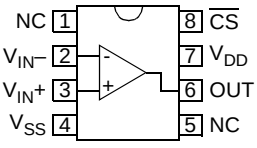
MCP6546
SC-70-5, SOT23-5



MCP6546U
SC-70-5, SOT-23-5



MCP6548
PDIP, SOIC, MSOP



© 2002-2012 Microchip Technology Inc.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
Open-Drain Output..... V_{SS} + 10.5V
Analog Input (V_{IN}+, V_{IN}-)†† ..... V_{SS} - 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection on All Pins:
(HBM;MM) 2 kV;200V (MCP6546U)
(HBM;MM) ..... 4 kV; 200V (all other parts)

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device, at those or any other conditions above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = V_{SS}, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD} (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.6	—	5.5	V	$V_{PU} \geq V_{DD}$
Quiescent Current (per comparator)	I_Q	0.3	0.6	1	µA	I_{OUT} = 0
Input						
Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
Common Mode Rejection Ratio	CMRR	50	65	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Power Supply Rejection Ratio	PSRR	63	80	—	dB	V_{CM} = V_{SS}
Input Offset Voltage	V_{OS}	-7.0	±1.5	+7.0	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3	—	µV/°C	T_A = -40°C to +125°C, V_{CM} = V_{SS}
Input Hysteresis Voltage	V_{HYST}	1.5	3.3	6.5	mV	V_{CM} = V_{SS} **(Note 1)**
Linear Temp. Co.	TC_1	—	6.7	—	µV/°C	T_A = -40°C to +125°C, V_{CM} = V_{SS} **(Note 2)**
Quadratic Temp. Co.	TC_2	—	-0.035	—	µV/°C^2	T_A = -40°C to +125°C, V_{CM} = V_{SS} **(Note 2)**
Input Bias Current	I_B	—	1	—	pA	V_{CM} = V_{SS}
At Temperature (I-Temp parts)	I_B	—	25	100	pA	T_A = +85°C, V_{CM} = V_{SS} **(Note 3)**
At Temperature (E-Temp parts)	I_B	—	1200	5000	pA	T_A = +125°C, V_{CM} = V_{SS} **(Note 3)**
Input Offset Current	I_{OS}	—	±1	—	pA	V_{CM} = V_{SS}

Note 1: The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: V_{HYST} at differential temperatures is estimated using:
V_{HYST} (T_A) = V_{HYST} + (T_A -25°C) TC_1 + (T_A - 25°C)^2TC_2.

3: Input bias current at temperature is not tested for the SC-70-5 package.

4: Do not short the output above V_{SS} + 10V. Limit the output current to Absolute Maximum Rating of 30 mA. The minimum V_{PU} test limit was V_{DD} before Dec. 2004 (week code 52).

© 2002-2012 Microchip Technology Inc.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}– = V_{SS}$, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$ (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Common Mode Input Impedance	Z_{CM}	—	10^{13}||4	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Open-Drain Output						
Output Pull-Up Voltage	V_{PU}	1.6	—	10	V	(**Note 4**)
High-Level Output Current	I_{OH}	-100	—	—	nA	V_{DD} = 1.6V to 5.5V, V_{PU} = 10V **(Note 4)**
Low-Level Output Voltage	V_{OL}	V_{SS}	—	V_{SS} + 0.2	V	I_{OUT} = 2 mA, $V_{PU} = V_{DD}$ = 5V
Short-Circuit Current	I_{SC}	—	±1.5	—	mA	$V_{PU} = V_{DD}$ = 1.6V **(Note 4)**
	I_{SC}	–	30	—	mA	$V_{PU} = V_{DD}$ = 5.5V **(Note 4)**
Output Pin Capacitance	C_{OUT}	—	8	—	pF	

Note 1: The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: V_{HYST} at differential temperatures is estimated using:
$V_{HYST}(T_A) = V_{HYST} + (T_A - 25°C)\,TC_1 + (T_A - 25°C)^2 TC_2$.

3: Input bias current at temperature is not tested for the SC-70-5 package.

4: Do not short the output above V_{SS} + 10V. Limit the output current to Absolute Maximum Rating of 30 mA. The minimum V_{PU} test limit was V_{DD} before Dec. 2004 (week code 52).

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, Step = 200 mV, Overdrive = 100 mV, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Fall Time	t_F	—	0.7	—	µs	**(Note 1)**
Propagation Delay (High-to-Low)	t_{PHL}	—	4.0	8.0	µs	
Propagation Delay (Low-to-High)	t_{PLH}	—	3.0	8.0	µs	**(Note 1)**
Propagation Delay Skew	t_{PDS}	—	-1.0	—	µs	**(Notes 1 and 2)**
Maximum Toggle Frequency	f_{MAX}	—	225	—	kHz	V_{DD} = 1.6V
	f_{MAX}	—	165	—	kHz	V_{DD} = 5.5V
Input Noise Voltage	E_{ni}	—	200	—	$µV_{P-P}$	10 Hz to 100 kHz

Note 1: t_R and t_{PLH} depend on the load (R_L and C_L); these specifications are valid for the indicated load only.

2: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

MCP6548 CHIP SELECT ($\overline{CS}$) CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}- = V_{SS}$, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF (Refer to Figures 1-1 and 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS} = V_{SS}$
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	1	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, V_{DD} Current	I_{DD}	—	18	—	pA	$\overline{CS} = V_{DD}$
$\overline{CS}$ Input High, GND Current	I_{SS}	—	-20	—	pA	$\overline{CS} = V_{DD}$
Comparator Output Leakage	$I_{O(LEAK)}$	—	1	—	pA	$V_{OUT} = V_{SS}$+10V, $\overline{CS} = V_{DD}$
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Comparator Output Low Turn-on Time	t_{ON}	—	2	50	ms	$\overline{CS}$ = 0.2V_{DD} to $V_{OUT} = V_{DD}/2$, $V_{IN}- = V_{DD}$
$\overline{CS}$ High to Comparator Output High Z Turn-off Time	t_{OFF}	—	10	—	µs	$\overline{CS}$ = 0.8V_{DD} to $V_{OUT} = V_{DD}/2$, $V_{IN}- = V_{DD}$
$\overline{CS}$ Hysteresis	V_{CS_HYST}	—	0.6	—	V	V_{DD} = 5V

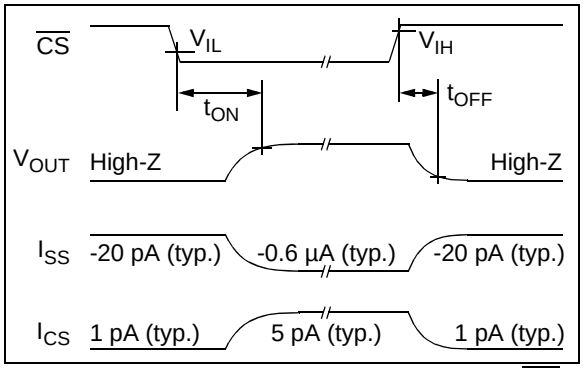


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ pin on the MCP6548.*

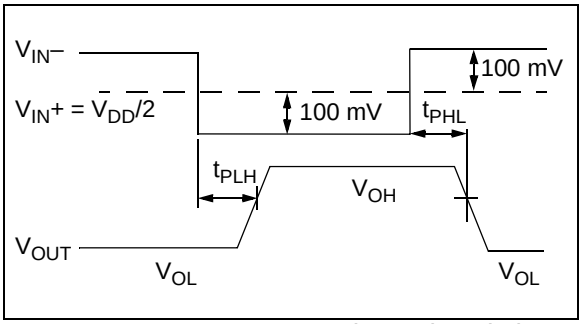


FIGURE 1-2: *Propagation Delay Timing Diagram.*

© 2002-2012 Microchip Technology Inc.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC-70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The MCP6546/6R/6U/7/8/9 I-temp family operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.1 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

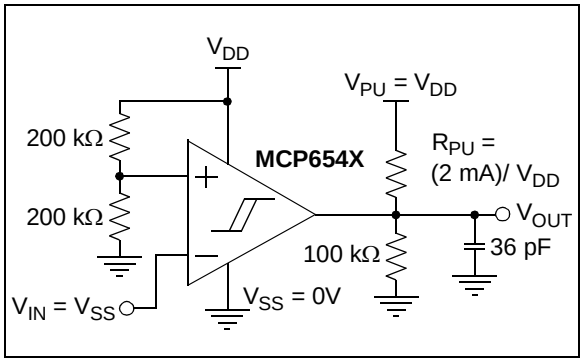


FIGURE 1-3: *AC and DC Test Circuit for the Open-Drain Output Comparators.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

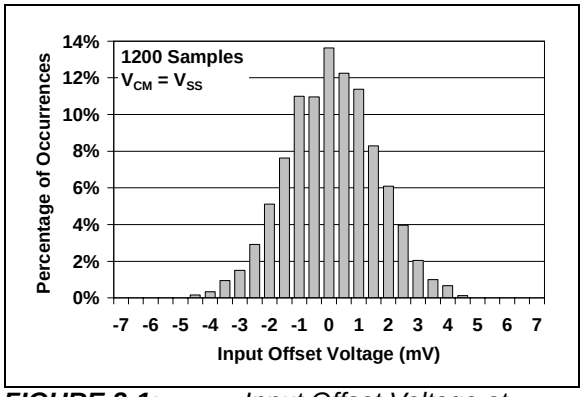


FIGURE 2-1: *Input Offset Voltage at $V_{CM} = V_{SS}$.*

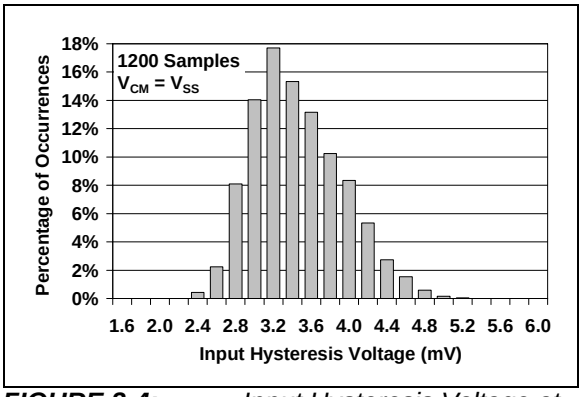


FIGURE 2-4: *Input Hysteresis Voltage at $V_{CM} = V_{SS}$.*

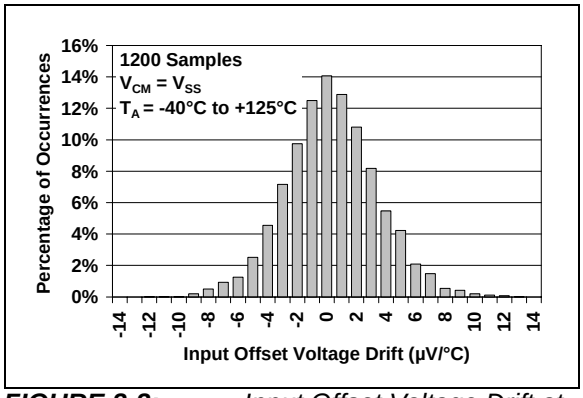


FIGURE 2-2: *Input Offset Voltage Drift at $V_{CM} = V_{SS}$.*

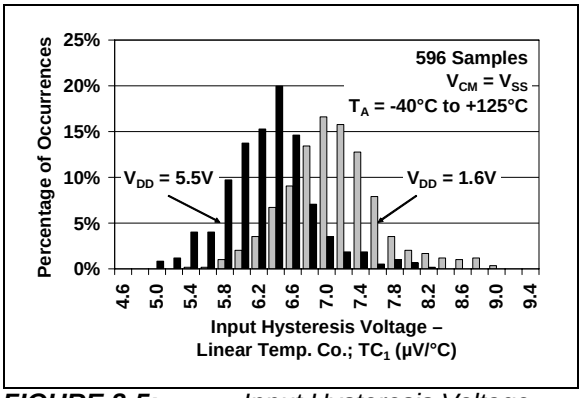


FIGURE 2-5: *Input Hysteresis Voltage Linear Temp. Co. (TC_1) at $V_{CM} = V_{SS}$.*

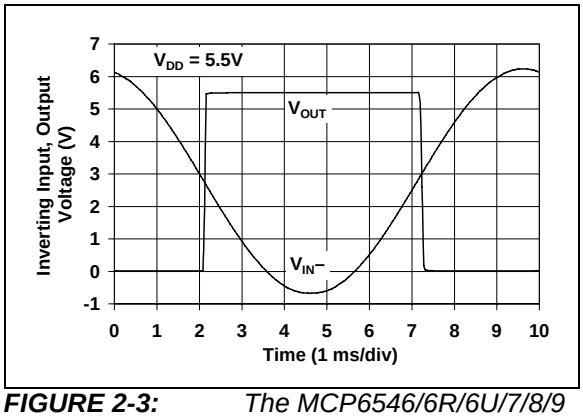


FIGURE 2-3: *The MCP6546/6R/6U/7/8/9 Comparators Show No Phase Reversal.*

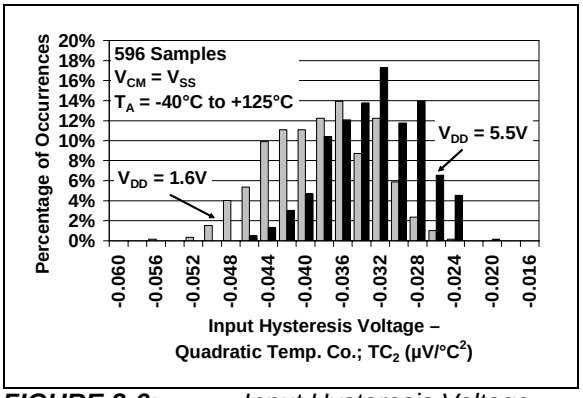


FIGURE 2-6: *Input Hysteresis Voltage Quadratic Temp. Co. (TC_2) at $V_{CM} = V_{SS}$.*

© 2002-2012 Microchip Technology Inc.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

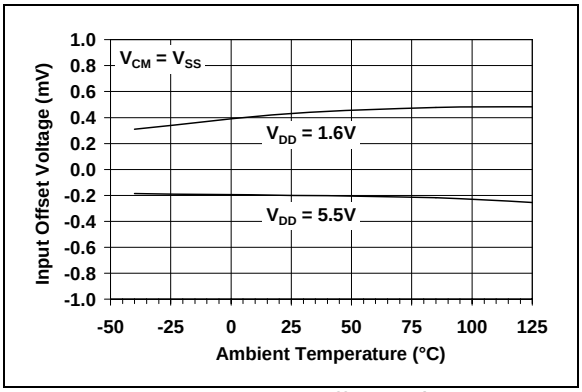


FIGURE 2-7: *Input Offset Voltage vs. Ambient Temperature at V_{CM} = V_{SS}.*

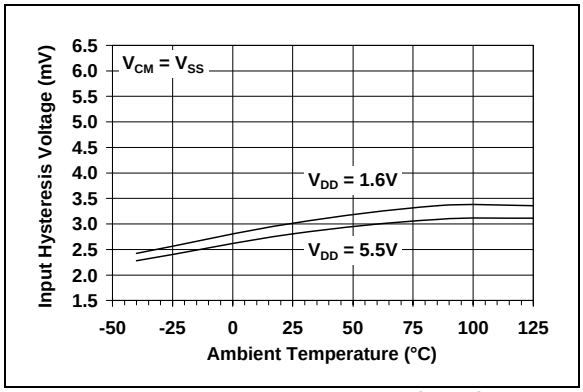


FIGURE 2-10: *Input Hysteresis Voltage vs. Ambient Temperature at V_{CM} = V_{SS}.*

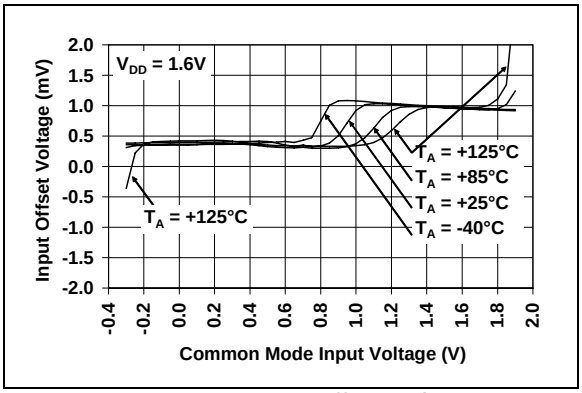


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

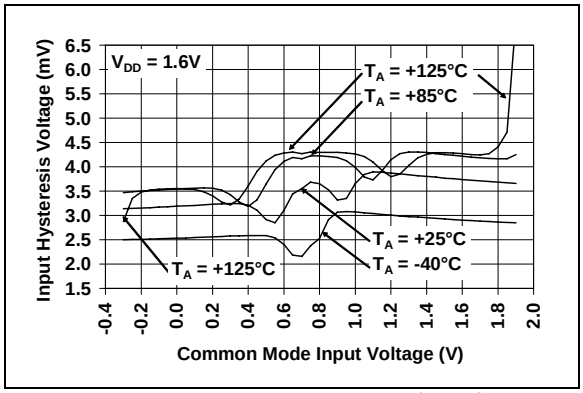


FIGURE 2-11: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

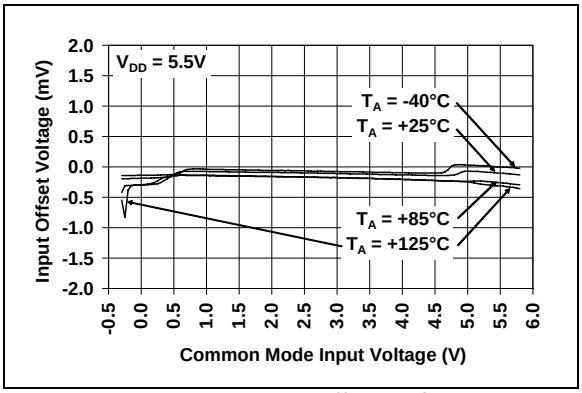


FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

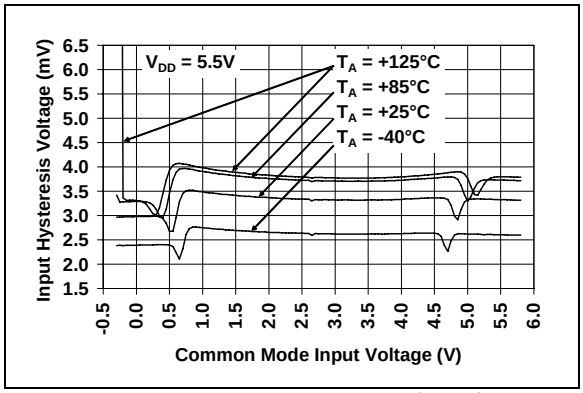


FIGURE 2-12: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

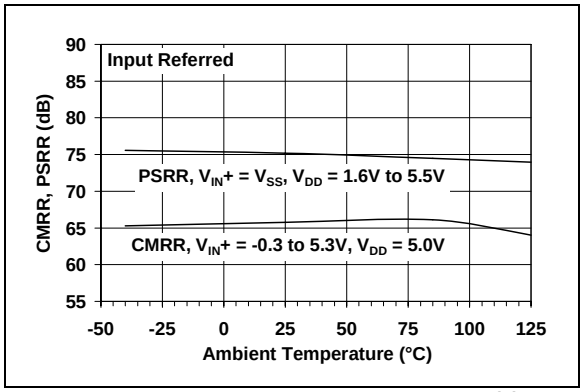


FIGURE 2-13: *CMRR,PSRR vs. Ambient Temperature.*

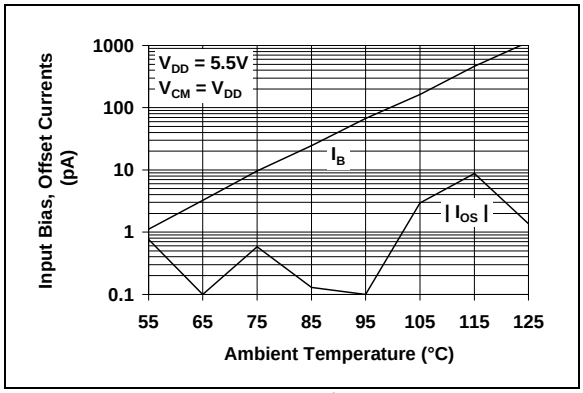


FIGURE 2-14: *Input Bias Current, Input Offset Current vs. Ambient Temperature.*

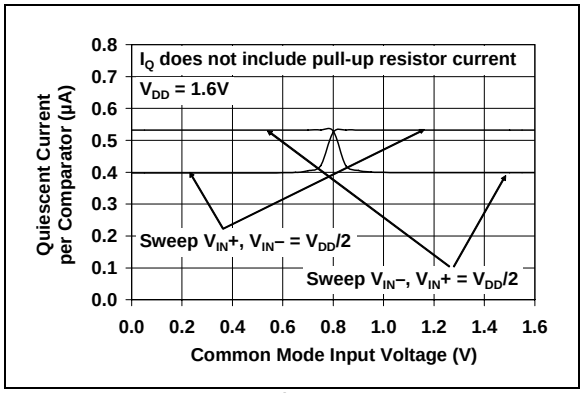


FIGURE 2-15: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

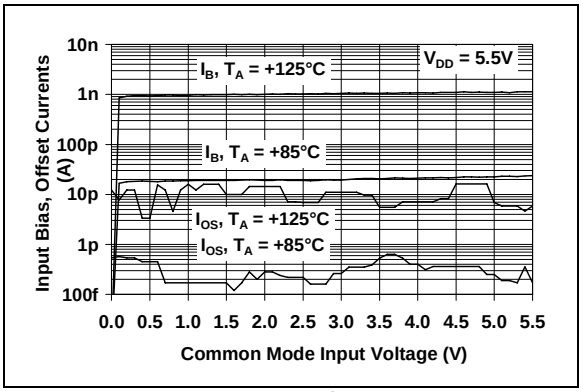


FIGURE 2-16: *Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.*

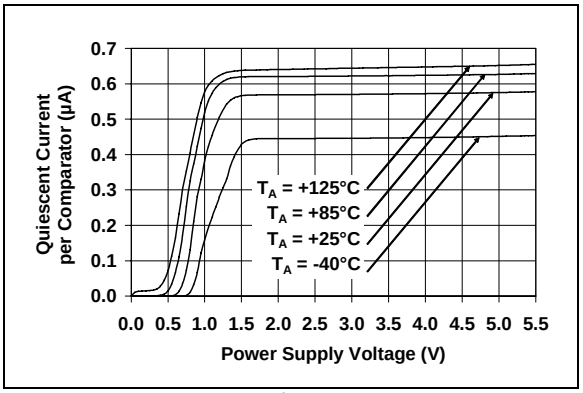


FIGURE 2-17: *Quiescent Current vs. Power Supply Voltage.*

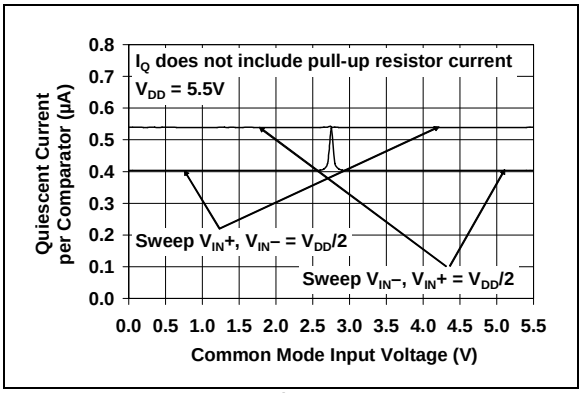


FIGURE 2-18: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

© 2002-2012 Microchip Technology Inc.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

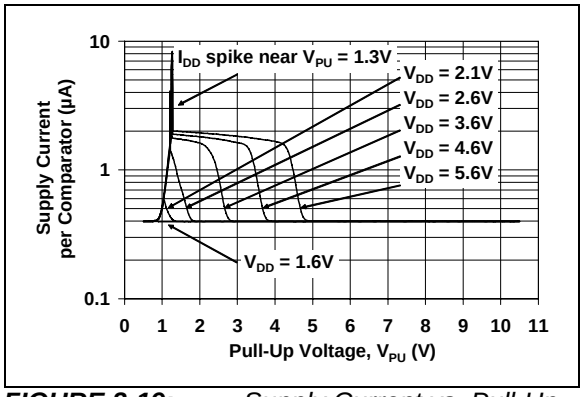


FIGURE 2-19: *Supply Current vs. Pull-Up Voltage.*

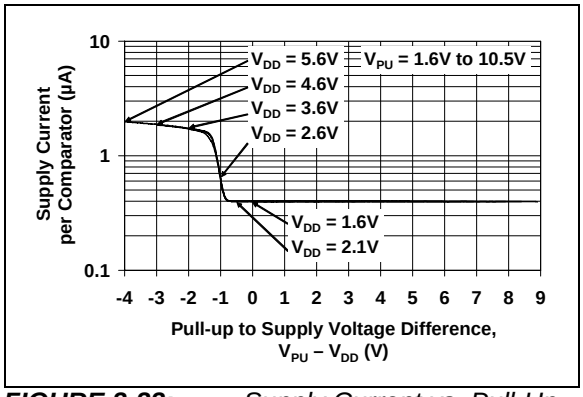


FIGURE 2-22: *Supply Current vs. Pull-Up to Supply Voltage Difference.*

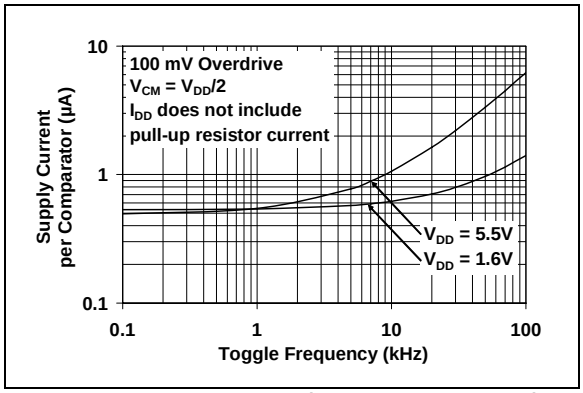


FIGURE 2-20: *Supply Current vs. Toggle Frequency.*

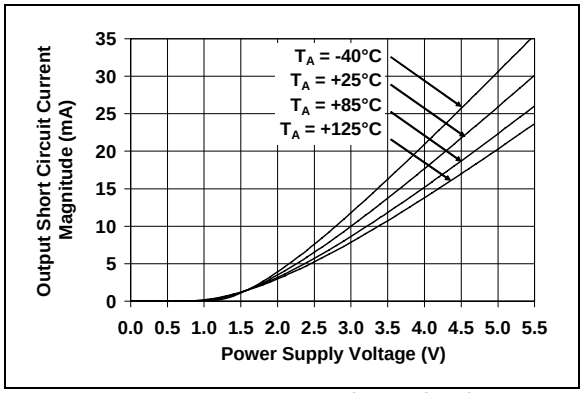


FIGURE 2-23: *Output Short Circuit Current Magnitude vs. Power Supply Voltage.*

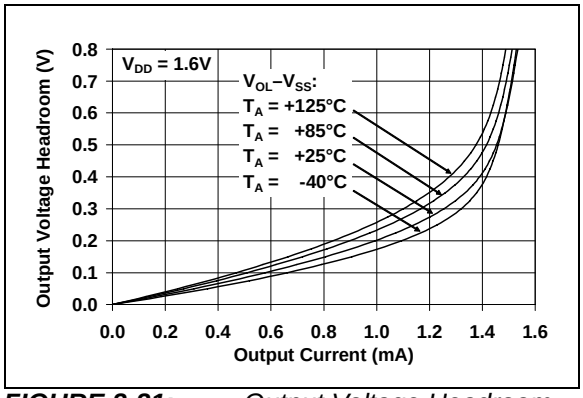


FIGURE 2-21: *Output Voltage Headroom vs. Output Current at V_{DD} = 1.6V.*

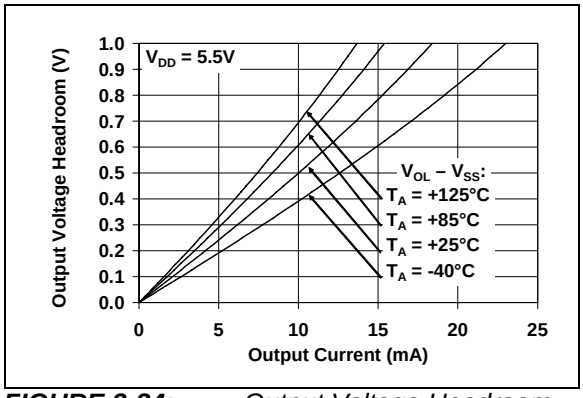


FIGURE 2-24: *Output Voltage Headroom vs. Output Current at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}–$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

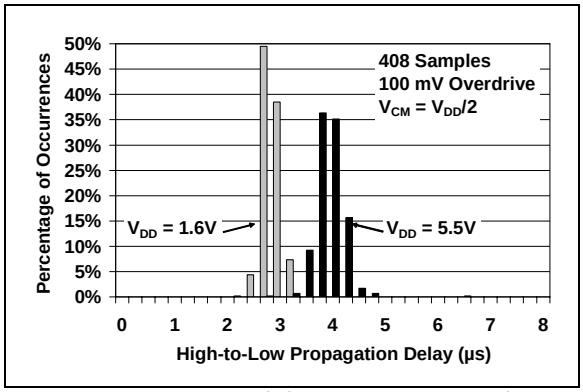


FIGURE 2-25: *High-to-Low Propagation Delay.*

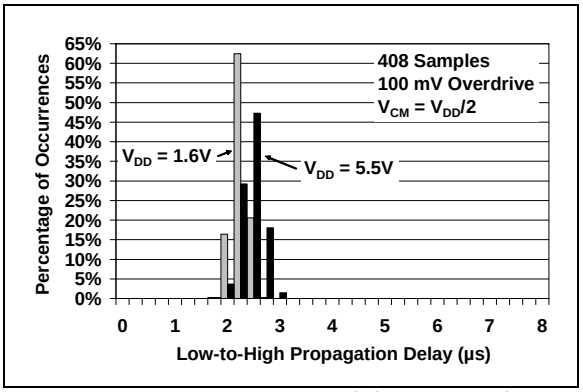


FIGURE 2-28: *Low-to-High Propagation Delay.*

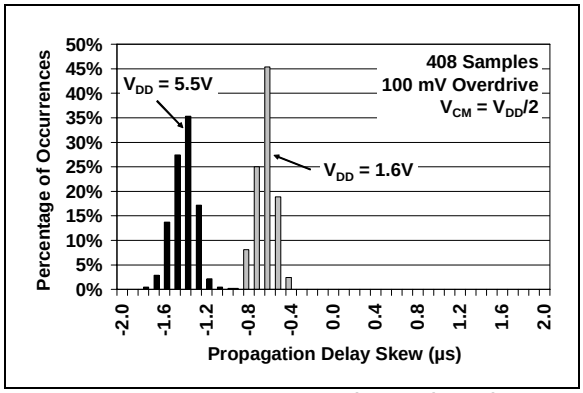


FIGURE 2-26: *Propagation Delay Skew.*

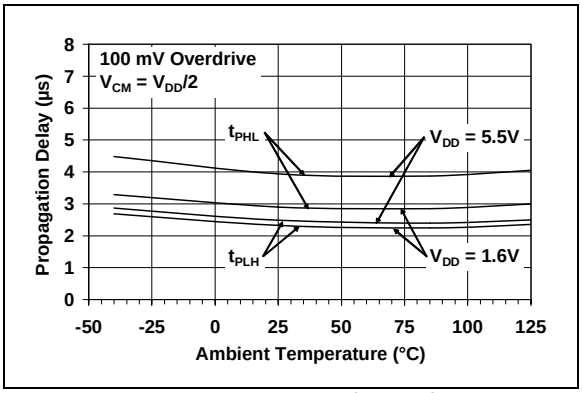


FIGURE 2-29: *Propagation Delay vs. Ambient Temperature.*

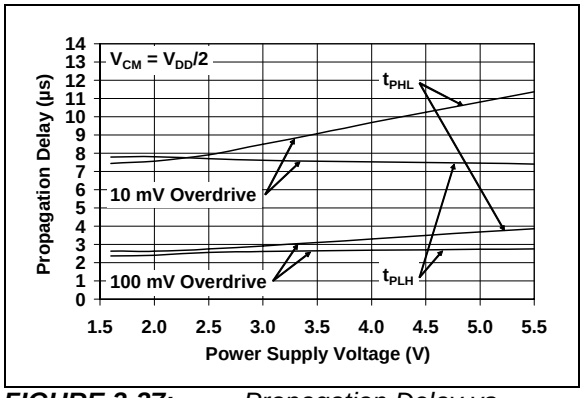


FIGURE 2-27: *Propagation Delay vs. Power Supply Voltage.*

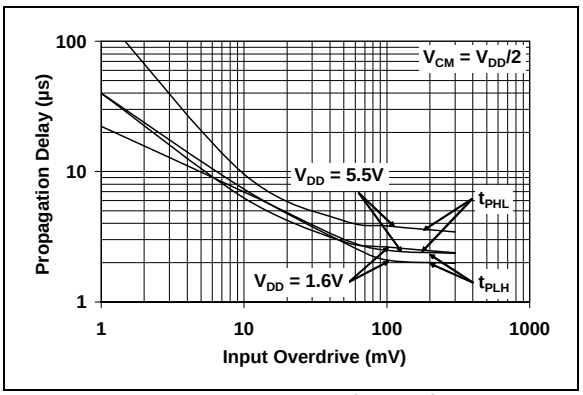


FIGURE 2-30: *Propagation Delay vs. Input Overdrive.*

© 2002-2012 Microchip Technology Inc.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

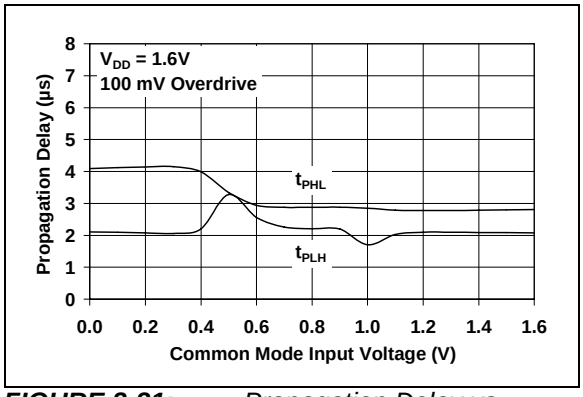


FIGURE 2-31: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

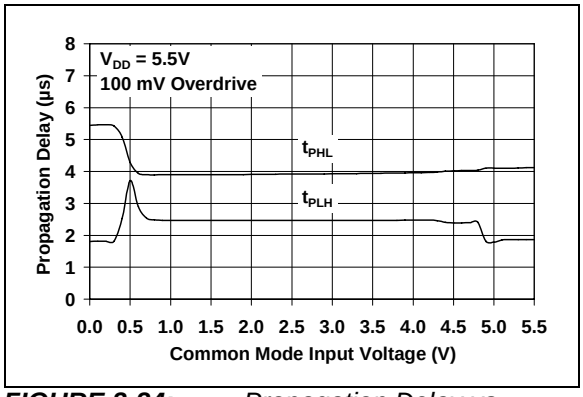


FIGURE 2-34: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

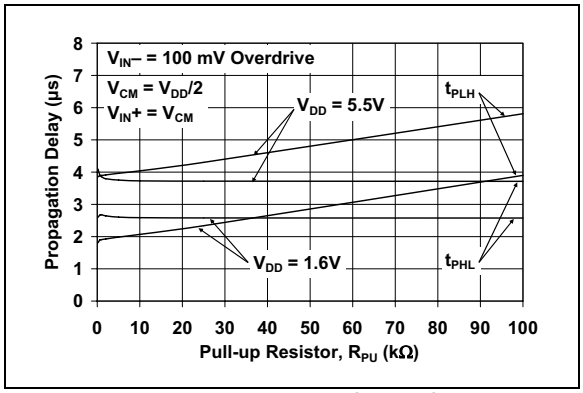


FIGURE 2-32: *Propagation Delay vs. Pull-up Resistor.*

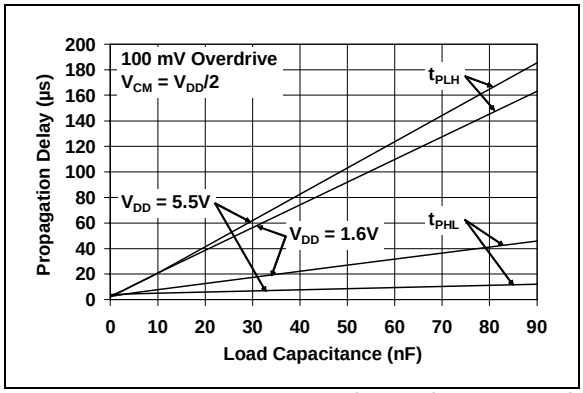


FIGURE 2-35: *Propagation Delay vs. Load Capacitance.*

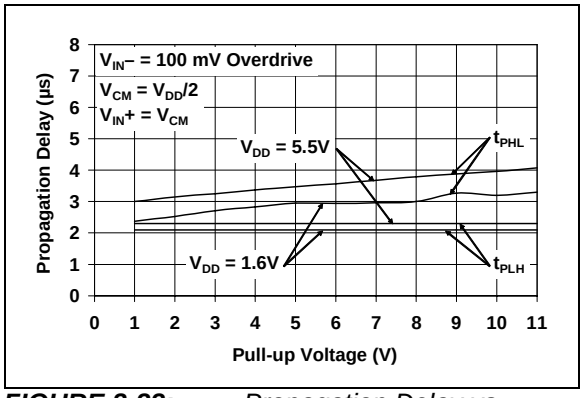


FIGURE 2-33: *Propagation Delay vs. Pull-up Voltage.*

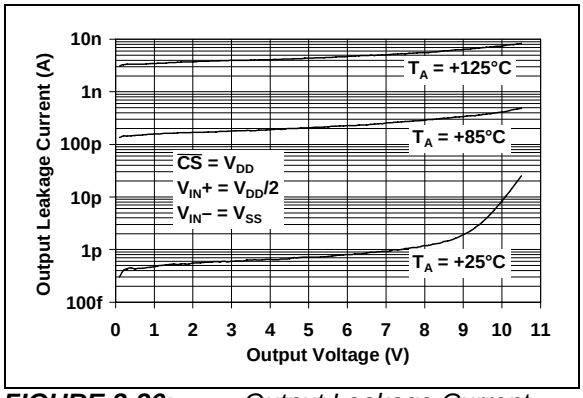


FIGURE 2-36: *Output Leakage Current ($\overline{CS}$ = V_{DD}) vs. Output Voltage (MCP6548 only).*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

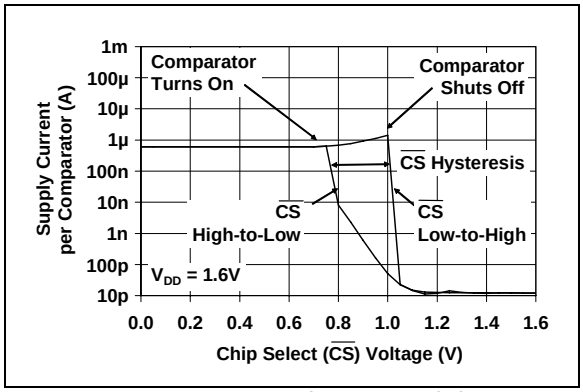


FIGURE 2-37: *Supply Current (Shoot-through Current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 1.6V (MCP6548 only).*

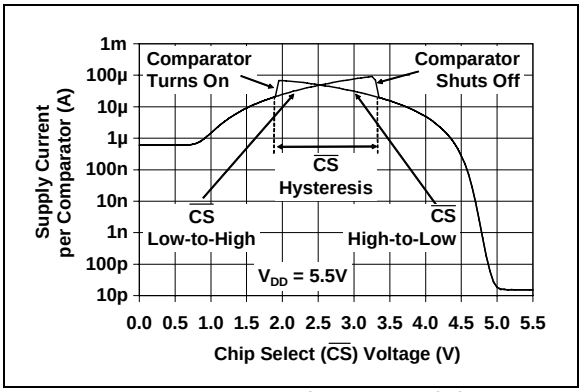


FIGURE 2-40: *Supply Current (Shoot-through Current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 5.5V (MCP6548 only).*

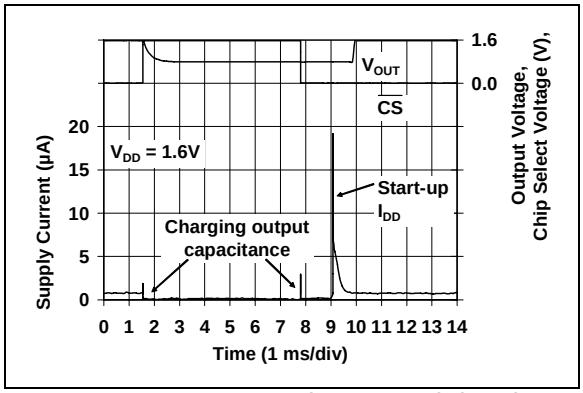


FIGURE 2-38: *Supply Current (Charging Current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 1.6V (MCP6548 only).*

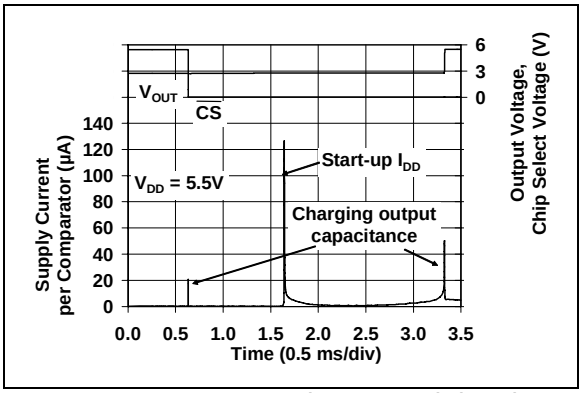


FIGURE 2-41: *Supply Current (Charging Current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 5.5V (MCP6548 only).*

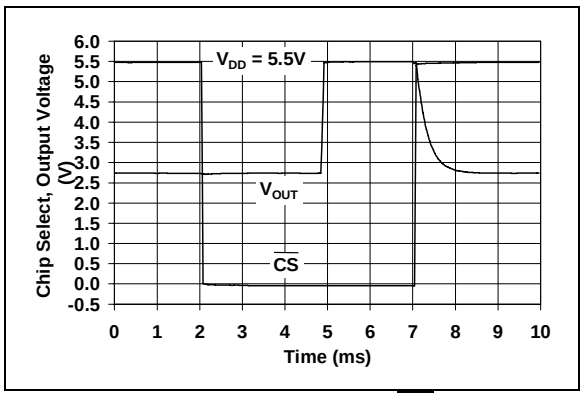


FIGURE 2-39: *Chip Select ($\overline{CS}$) Step Response (MCP6548 only).*

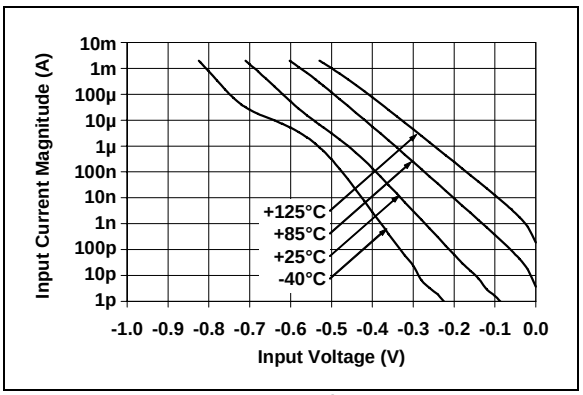


FIGURE 2-42: *Input Bias Current vs. Input Voltage.*

© 2002-2012 Microchip Technology Inc.

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6546	MCP6546	MCP6546R	MCP6546U	MCP6547	MCP6548	MCP6549	Symbol	Description
PDIP, SOIC, MSOP	SC-70, SOT-23	SOT-23-5	SC-70, SOT-23-5	PDIP, SOIC, MSOP	PDIP, SOIC, MSOP	PDIP, SOIC, TSSOP		
6	1	1	4	1	6	1	OUT, OUTA	Digital Output (comparator A)
2	4	4	3	2	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (comparator A)
3	3	3	1	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (comparator A)
7	5	2	5	8	7	4	V_{DD}	Positive Power Supply
—	—	—	—	5	—	5	$V_{INB}+$	Non-inverting Input (comparator B)
—	—	—	—	6	—	6	$V_{INB}-$	Inverting Input (comparator B)
—	—	—	—	7	—	7	OUTB	Digital Output (comparator B)
—	—	—	—	—	—	8	OUTC	Digital Output (comparator C)
—	—	—	—	—	—	9	$V_{INC}-$	Inverting Input (comparator C)
—	—	—	—	—	—	10	$V_{INC}+$	Non-inverting Input (comparator C)
4	2	5	2	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	—	—	12	$V_{IND}+$	Non-inverting Input (comparator D)
—	—	—	—	—	—	13	$V_{IND}-$	Inverting Input (comparator D)
—	—	—	—	—	—	14	OUTD	Digital Output (comparator D)
—	—	—	—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	—	—	—	1, 5	—	NC	No Internal Connection

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 $\overline{CS}$ Digital Input

This is a CMOS, Schmitt-triggered input that places the part into a low power mode of operation.

3.3 Digital Outputs

The comparator outputs are CMOS, open-drain digital outputs. They are designed to make level shifting and wired-OR easy to implement.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.6V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}, except the output pins which can be as high as 10V above V_{SS}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

NOTES:

© 2002-2012 Microchip Technology Inc.

4.0 APPLICATIONS INFORMATION

The MCP6546/6R/6U/7/8/9 family of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low power consumption.

4.1 Comparator Inputs

4.1.1 PHASE REVERSAL

The MCP6546/6R/6U/7/8/9 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors, and to minimize input bias current (IB). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass ESD events within the specified limits.

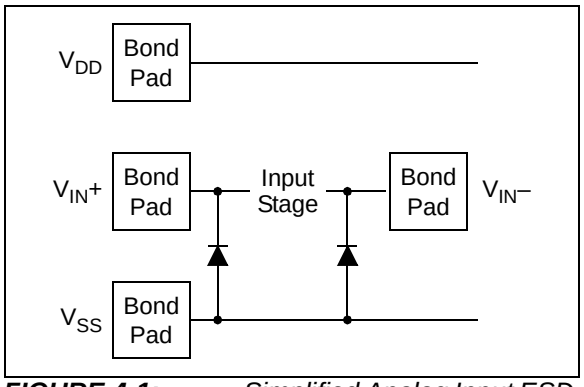


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the $V_{IN}+$ and $V_{IN}–$ pins (see Absolute Maximum Ratings † at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins ($V_{IN}+$ and $V_{IN}–$) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pin. Diodes D_1 and D_2 prevent the input pin ($V_{IN}+$ and $V_{IN}–$) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

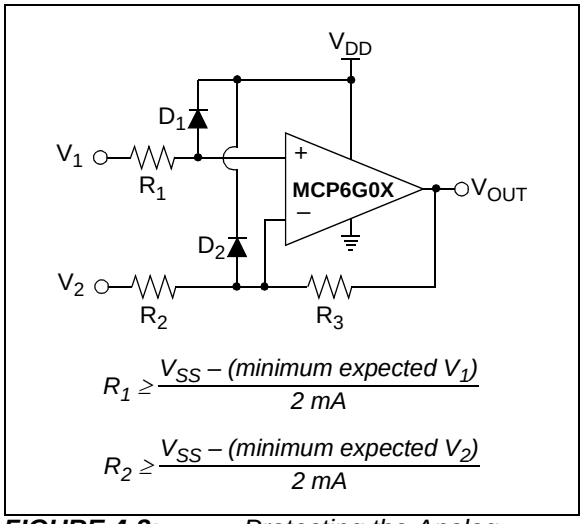


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, the currents through diodes D_1 and D_2 need to be limited by some other mechanism. The resistor then serves as in-rush current limiter; the DC current into the input pins ($V_{IN}+$ and $V_{IN}–$) should be very small.

A significant amount of current can flow out of the inputs when the common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-42. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The input stage of this family of devices uses two differential input stages in parallel, one operates at low input voltages, and the other at high input voltages. With this topology, the input voltage is 0.3V above V_{DD} and 0.3V below V_{SS}. The input offset voltage is measured at both V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The MCP6546/6R/6U/7/8/9 family has internally-set hysteresis that is small enough to maintain input offset accuracy (<7 mV), and large enough to eliminate output chattering caused by the comparator's own input noise voltage (200 μV_{P-P}). Figure 4-3 illustrates this capability.

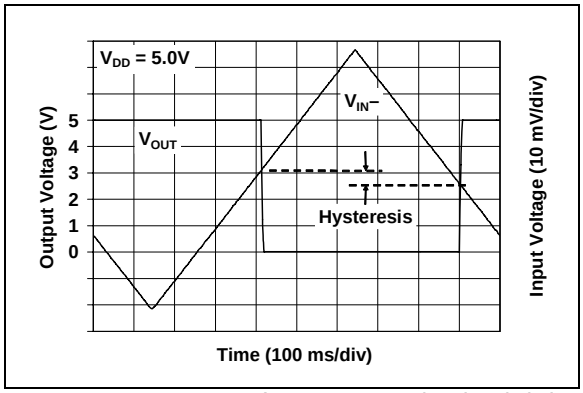


FIGURE 4-3: *The MCP6546/6R/6U/7/8/9 Comparators' Internal Hysteresis Eliminates Output Chatter Caused By Input Noise Voltage.*

4.2 Open-Drain Output

The open-drain output is designed to make level-shifting and wired-OR logic easy to implement. The output can go as high as 10V for 9V battery-powered applications. The output stage minimizes switching current (shoot-through current from supply-to-supply) when the output changes state. See Figures 2-15, 2-18 and 2-37 through 2-41, for more information.

4.3 MCP6548 Chip Select ($\overline{CS}$)

The MCP6548 is a single comparator with a Chip Select ($\overline{CS}$) pin. When $\overline{CS}$ is pulled high, the total current consumption drops to 20 pA (typical). 1 pA (typical) flows through the $\overline{CS}$ pin, 1 pA (typical) flows through the output pin and 18 pA (typical) flows through the V_{DD} pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling $\overline{CS}$ low, the comparator is enabled. If the $\overline{CS}$ pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

The internal $\overline{CS}$ circuitry is designed to minimize glitches when cycling the $\overline{CS}$ pin. This helps conserve power, which is especially important in battery-powered applications.

4.4 Externally Set Hysteresis

Greater flexibility in selecting hysteresis, or input trip points, is achieved by using external resistors.

Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other, thus reducing dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control).

4.4.1 INVERTING CIRCUIT

Figure 4-4 shows an inverting circuit for a single-supply application using three resistors, besides the pull-up resistor. The resulting hysteresis diagram is shown in Figure 4-5.

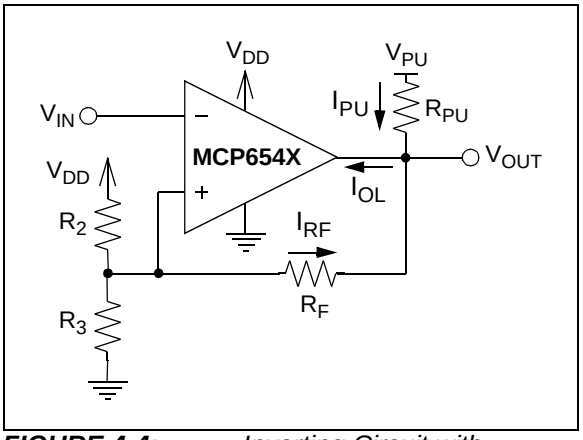


FIGURE 4-4: *Inverting Circuit with Hysteresis.*

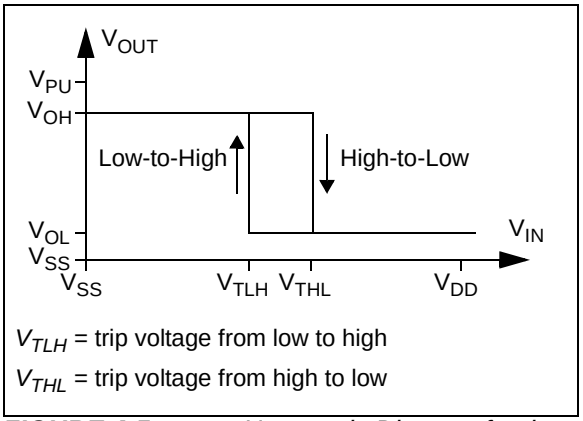


FIGURE 4-5: *Hysteresis Diagram for the Inverting Circuit.*

In order to determine the trip voltages (V_{THL} and V_{TLH}) for the circuit shown in Figure 4-4, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{DD}, as shown in Figure 4-6.

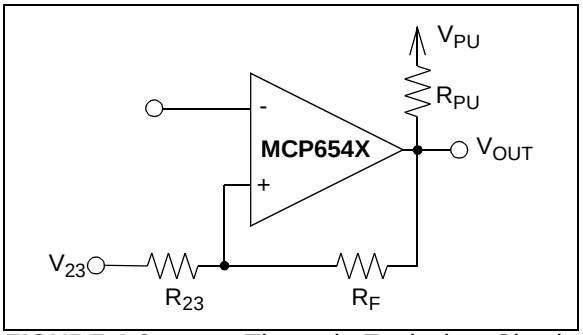


FIGURE 4-6: *Thevenin Equivalent Circuit.*

© 2002-2012 Microchip Technology Inc.

EQUATION 4-1:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-2:

$$V_{THL} = V_{PU}\left(\frac{R_{23}}{R_{23} + R_F + R_{PU}}\right) + V_{23}\left(\frac{R_F + R_{PU}}{R_{23} + R_F + R_{PU}}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

Figures 2-21 and 2-24 can be used to determine typical values for V_{OL}. This voltage is dependent on the output current I_{OL} as shown in Figure 4-4. This current can be determined using the equation below:

EQUATION 4-3:

$$I_{OL} = I_{PU} + I_{RF}$$

$$I_{OL} = \left(\frac{V_{PU} - V_{OL}}{R_{PU}}\right) + \left(\frac{V_{23} - V_{OL}}{R_{23} + R_F}\right)$$

V_{OH} can be calculated using the equation below:

EQUATION 4-4:

$$V_{OH} = (V_{PU} - V_{23}) \times \left(\frac{R_{23} + R_F}{R_{23} + R_F + R_{PU}}\right)$$

As explained in **Section 4.1 "Comparator Inputs"**, it is important to keep the non-inverting input below V_{DD}+0.3V when $V_{PU} > V_{DD}$.

4.5 Supply Bypass

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge-rate performance.

4.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-27). The supply current increases with increasing toggle frequency (Figure 2-30), especially with higher capacitive loads.

4.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Avoid toggling the output more than necessary. Do not use Chip Select ($\overline{CS}$) too frequently, in order to conserve power. Capacitive loads will draw additional power at start-up.

4.8 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6546/6R/6U/7/8/9 family's bias current at 25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

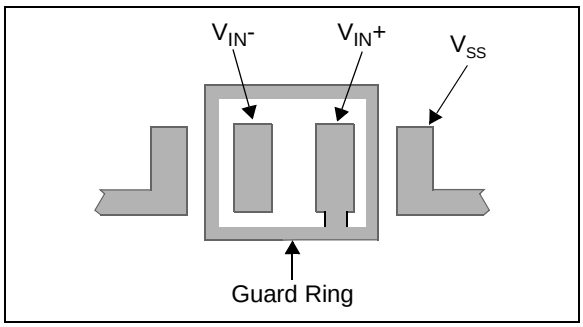


FIGURE 4-7: *Example Guard Ring Layout for Inverting Circuit.*

1. For the Inverting Configuration (Figures 4-4 and 4-7):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input pad, without touching the guard ring.

4.9 Unused Comparators

An unused amplifier in a quad package (MCP6549) should be configured as shown in Figure 4-8. This circuit prevents the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current (see Figure 2-15 and Figure 2-18).

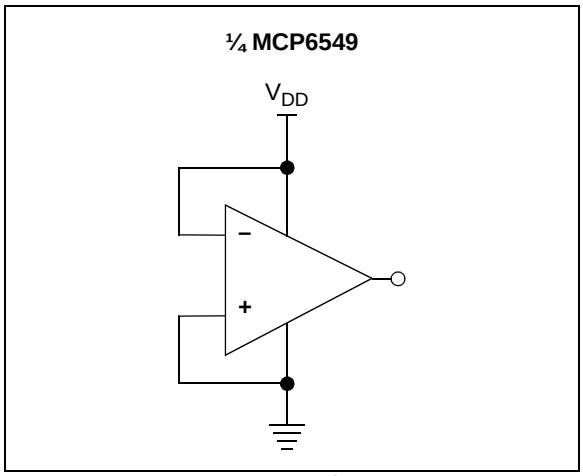


FIGURE 4-8: *Unused Comparators.*

4.10 Typical Applications

4.10.1 PRECISE COMPARATOR

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6041) to gain-up the input signal before it reaches the comparator. Figure 4-9 shows an example of this approach.

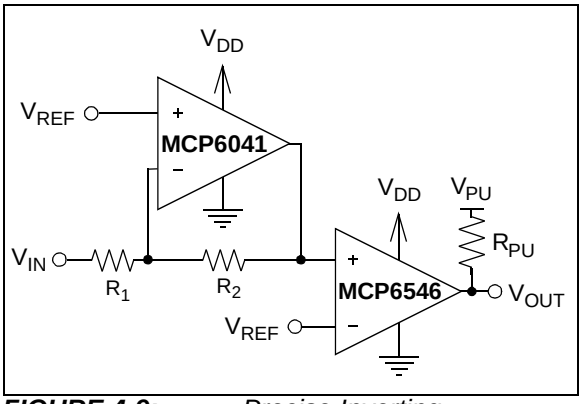


FIGURE 4-9: *Precise Inverting Comparator.*

4.10.2 WINDOWED COMPARATOR

Figure 4-10 shows one approach to designing a windowed comparator. The wired-OR connection produces a high output (logic 1) when the input voltage is between V_{RB} and V_{RT} (where $V_{RT} > V_{RB}$).

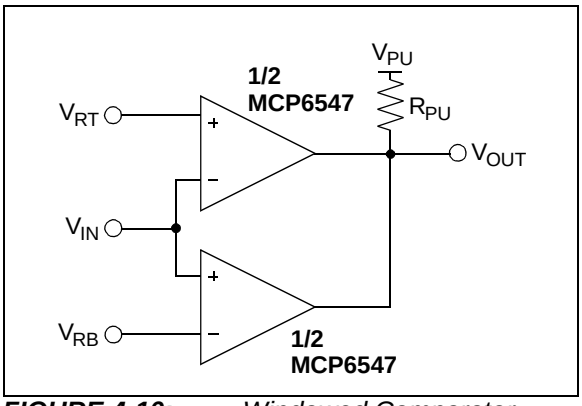


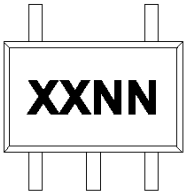
FIGURE 4-10: *Windowed Comparator.*

© 2002-2012 Microchip Technology Inc.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

5-Lead SC-70 (**MCP6546, MCP6546U**)

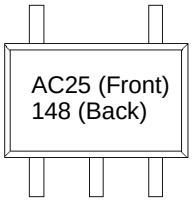


Device	I-Temp Code	E-Temp Code
MCP6546	ACNN	Note 2
MCP6546U	BBNN	Note 2

Note 1: I-Temp parts prior to March 2005 are marked “ACN”

2: SC-70-5 E-Temp parts not available at this release of the data sheet.

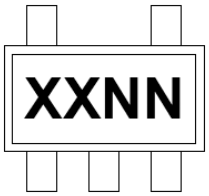
Example: (I-temp)



OR

Example: (I-temp)

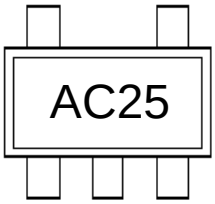
5-Lead SOT-23 **(MCP6546, MCP6546R, MCP6546U)**



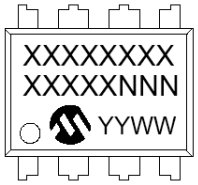
Device	I-Temp Code	E-Temp Code
MCP6546	ACNN	GWNN
MCP6546R	AHNN	GXNN
MCP6546U	—	AWNN

Note: Applies to 5-Lead SOT-23

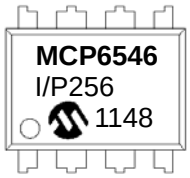
Example: (I-temp)



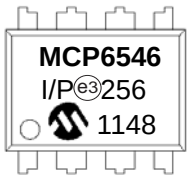
8-Lead PDIP (300 mil) **(MCP6546, MCP6547, MCP6548, MCP6549)**



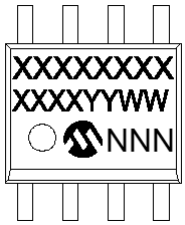
Examples:

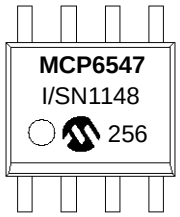


OR



8-Lead SOIC (150 mil) **(MCP6546, MCP6547, MCP6548, MCP6549)**





OR

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3))

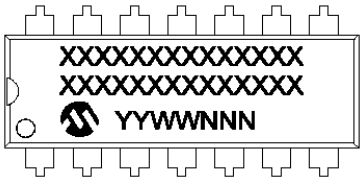
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

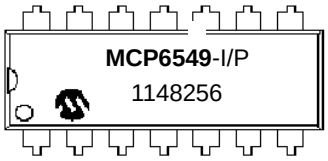
8-Lead MSOP (**MCP6546, MCP6547, MCP6548**)

Example:

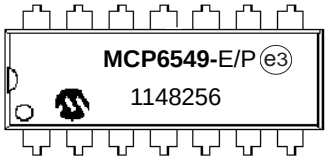
14-Lead PDIP (300 mil) **(MCP6549)**



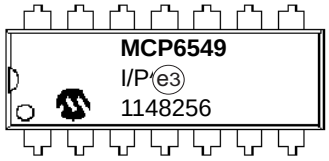
Example:



OR



OR



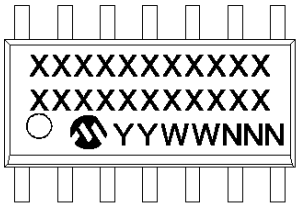
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3))

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

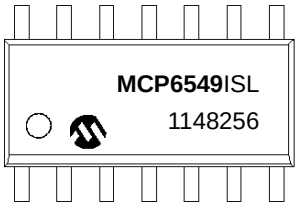
© 2002-2012 Microchip Technology Inc.

Package Marking Information (Continued)

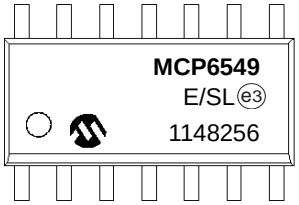
14-Lead SOIC (150 mil) **(MCP6549)**



Example:

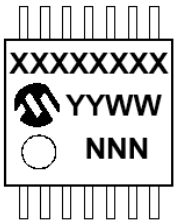


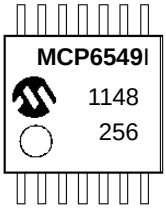
OR



14-Lead TSSOP **(MCP6549)**

Example:



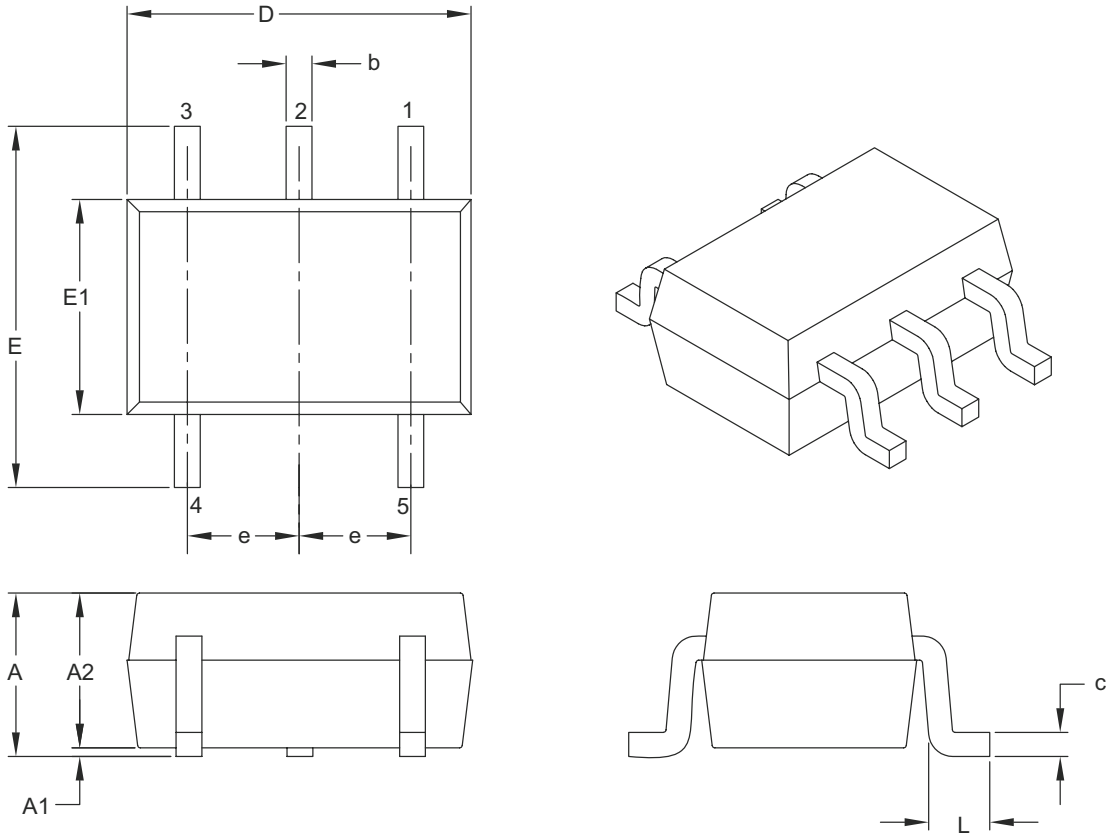


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3))

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

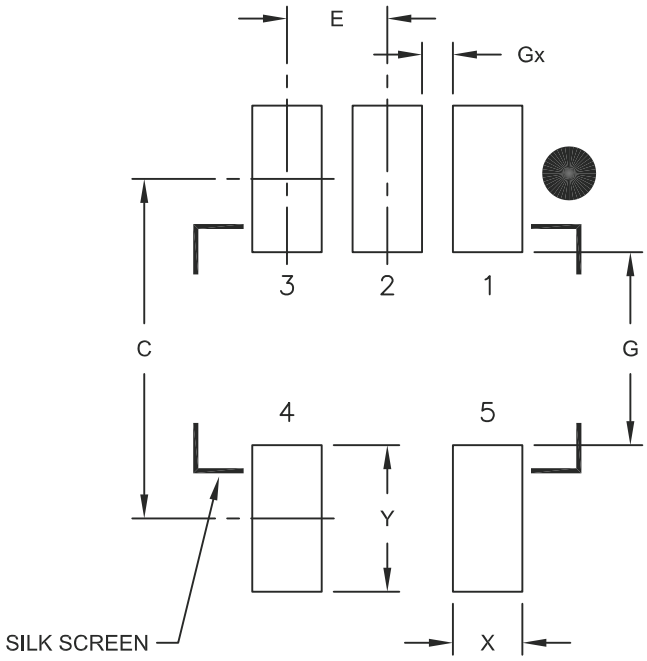
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

© 2002-2012 Microchip Technology Inc.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

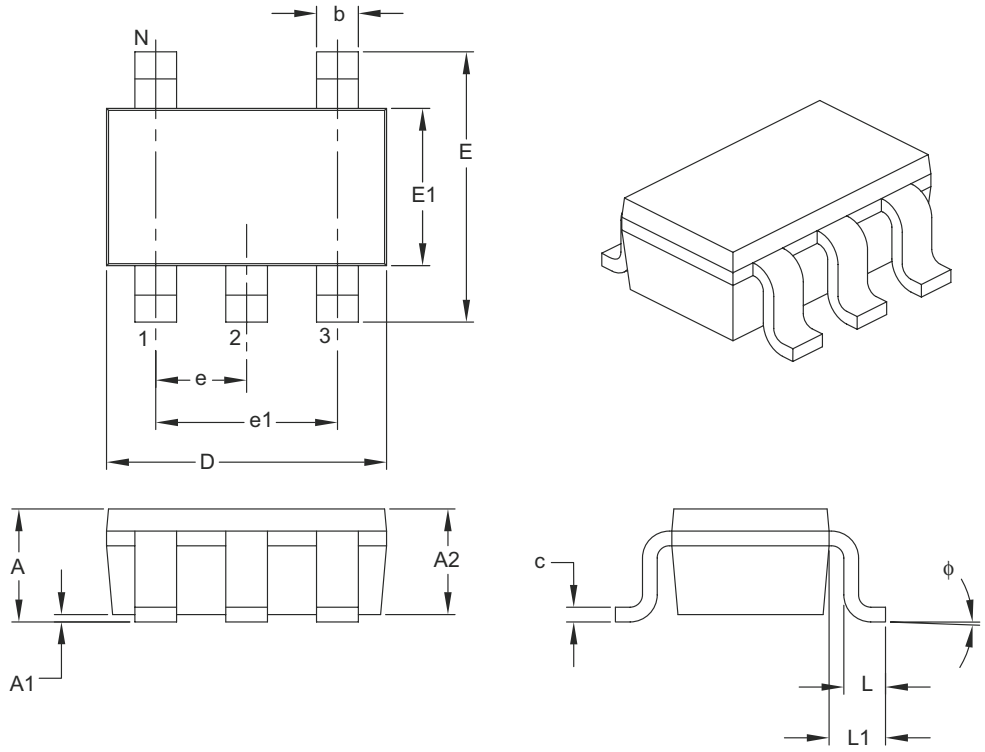
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

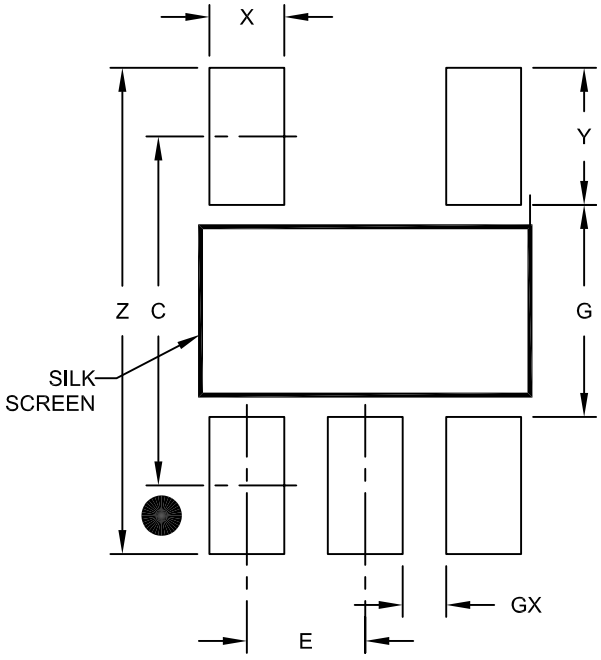
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

© 2002-2012 Microchip Technology Inc.

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

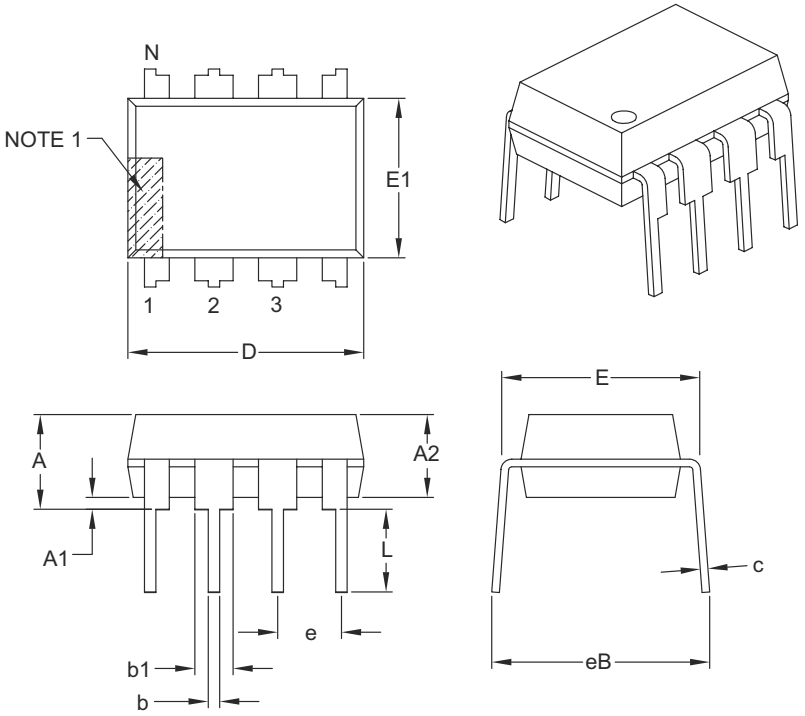
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

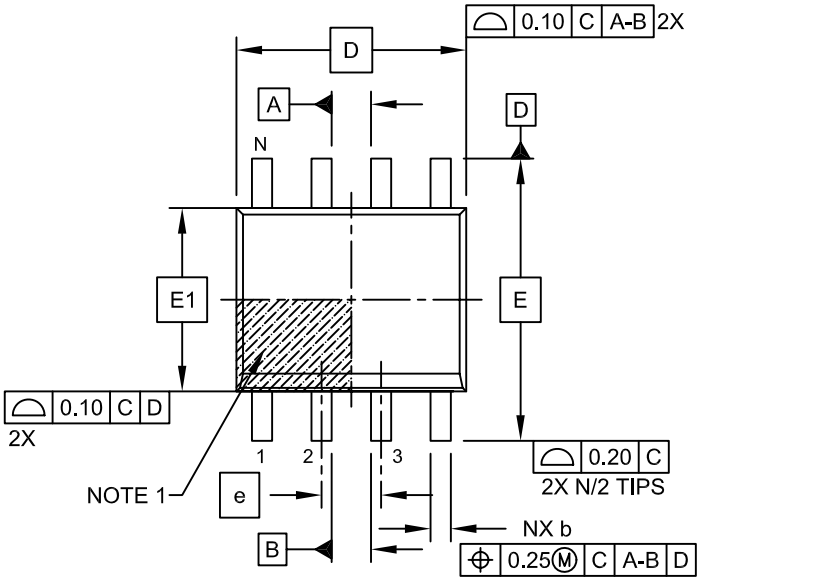
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

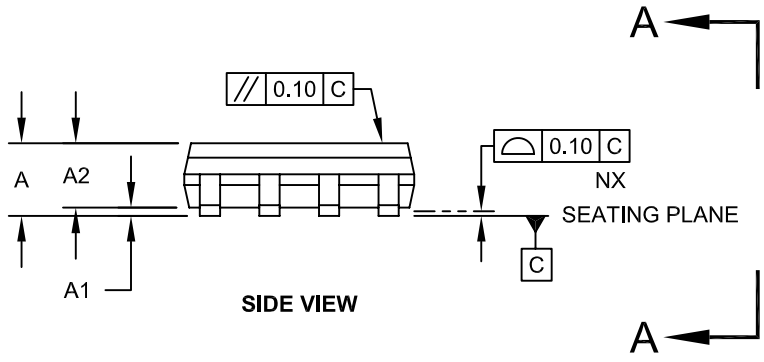
© 2002-2012 Microchip Technology Inc.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

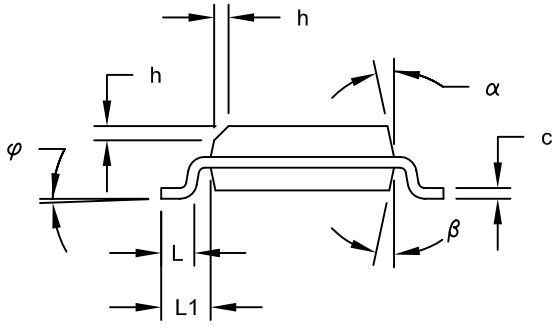
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

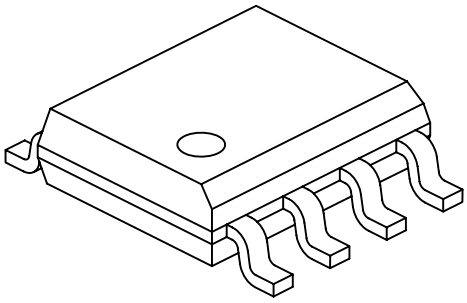


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

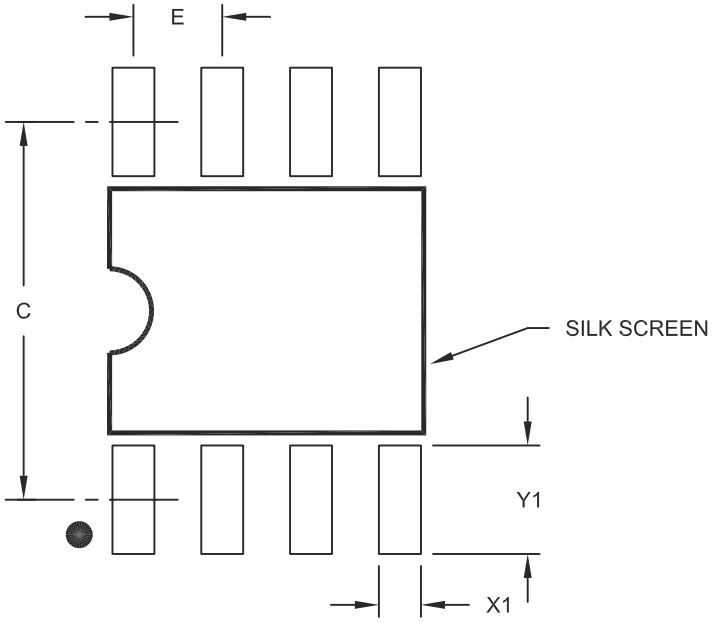
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

© 2002-2012 Microchip Technology Inc.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

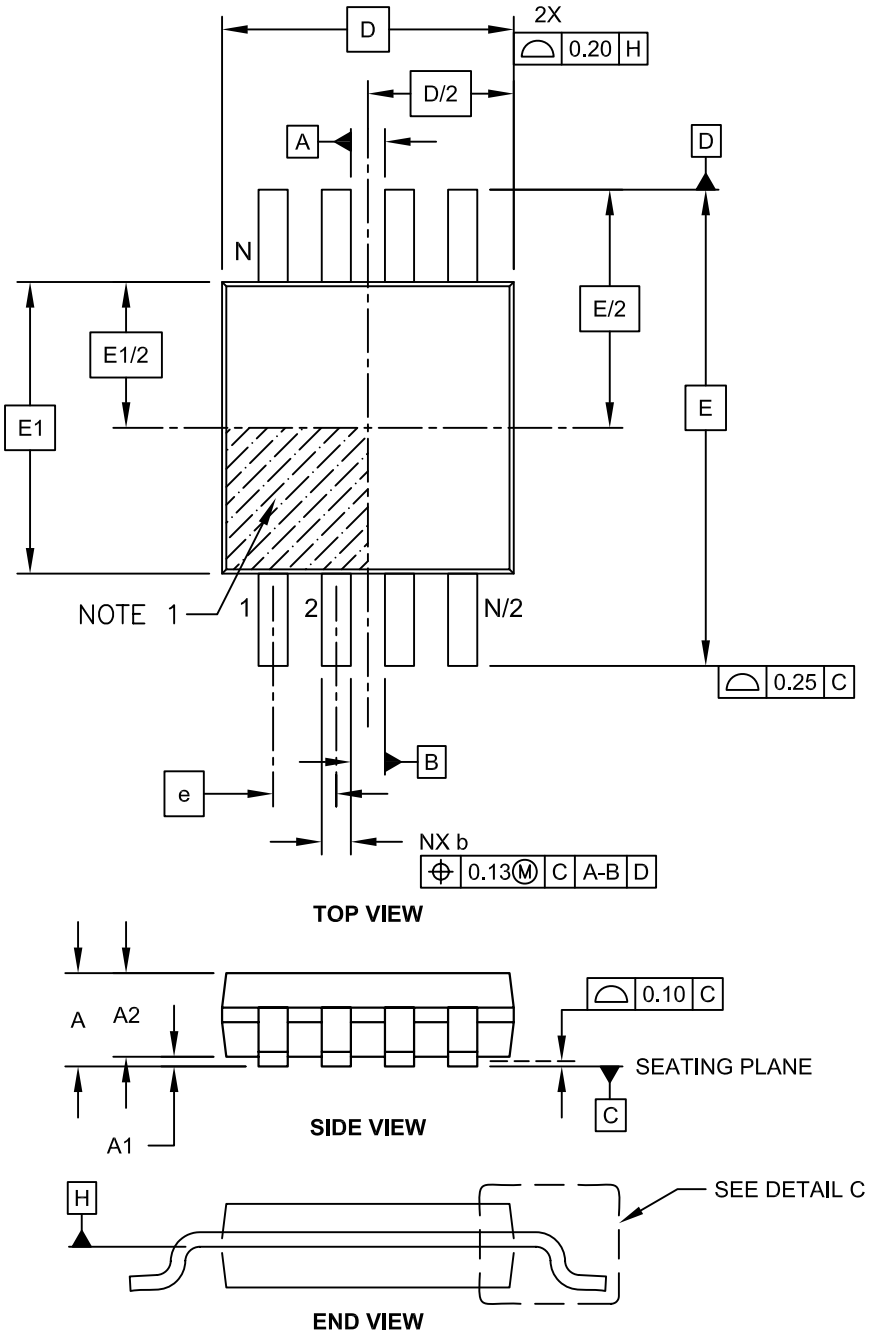
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

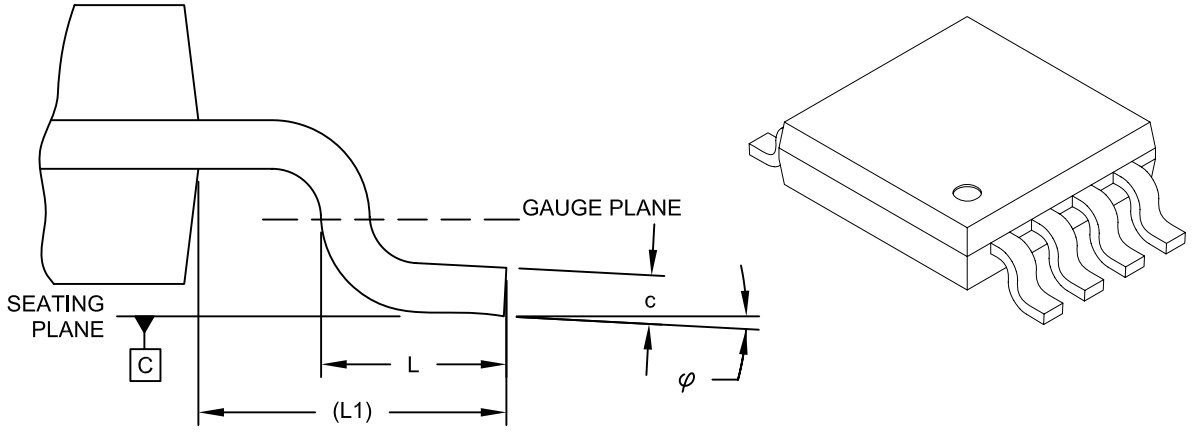


Microchip Technology Drawing C04-111C Sheet 1 of 2

© 2002-2012 Microchip Technology Inc.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

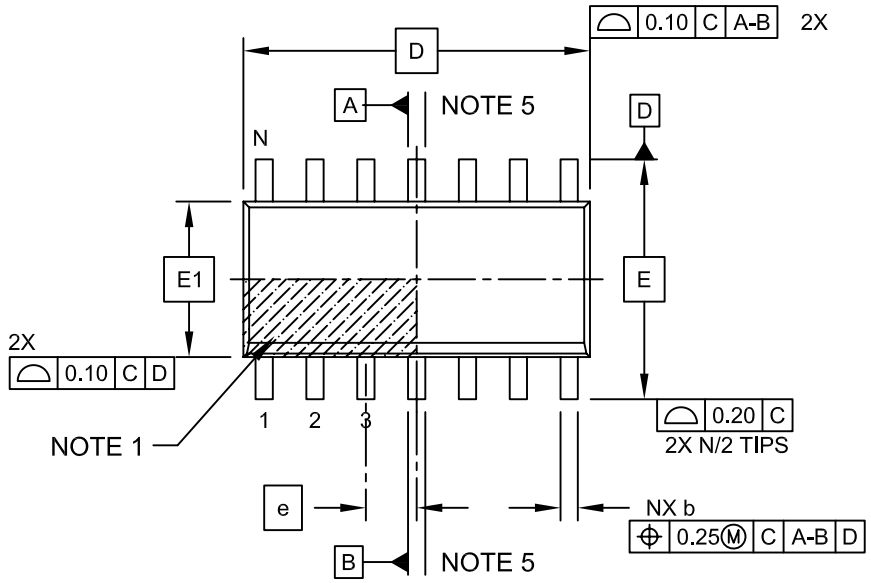
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

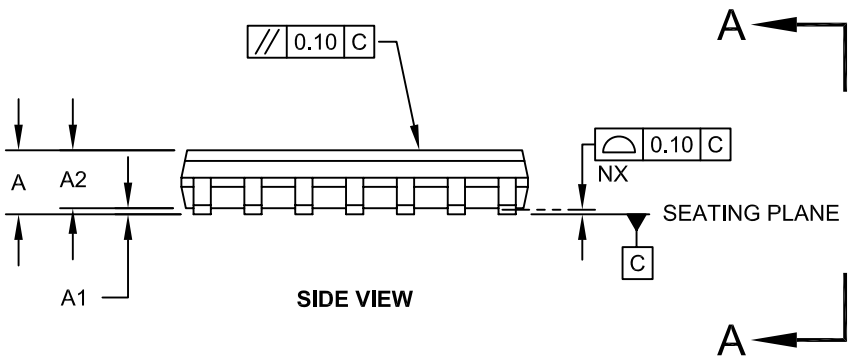
Microchip Technology Drawing C04-111C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

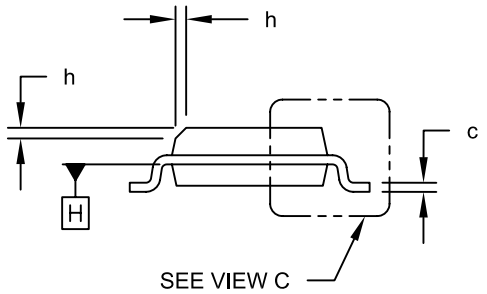
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



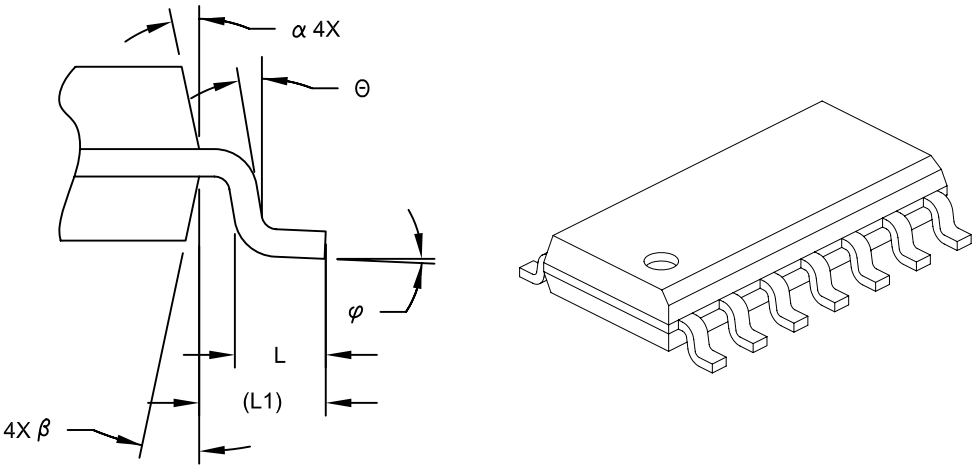
VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

© 2002-2012 Microchip Technology Inc.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

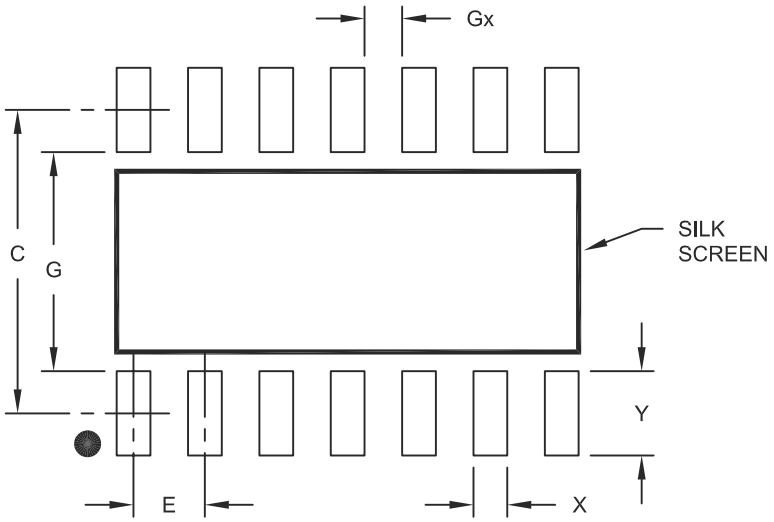
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

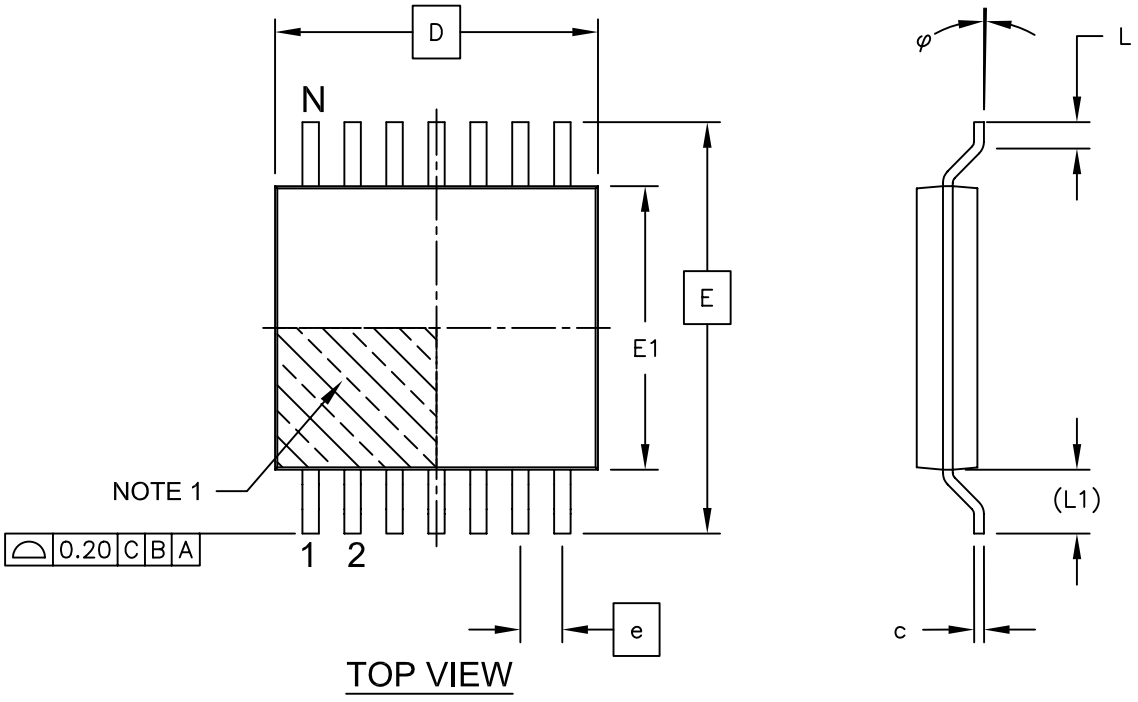
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

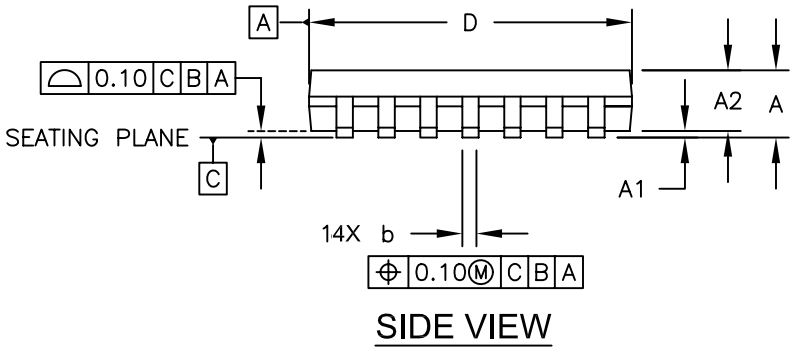
Microchip Technology Drawing No. C04-2065A

© 2002-2012 Microchip Technology Inc.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

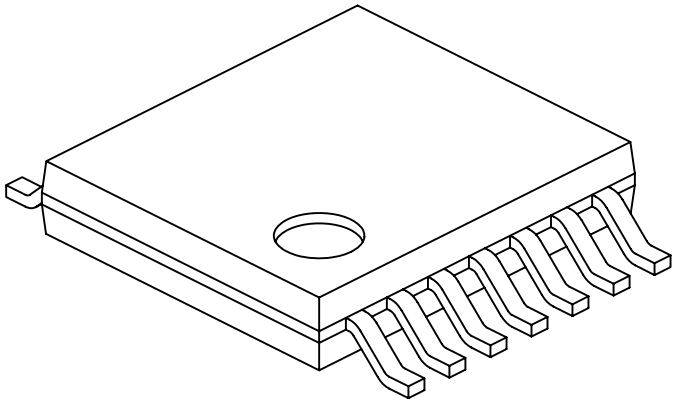




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

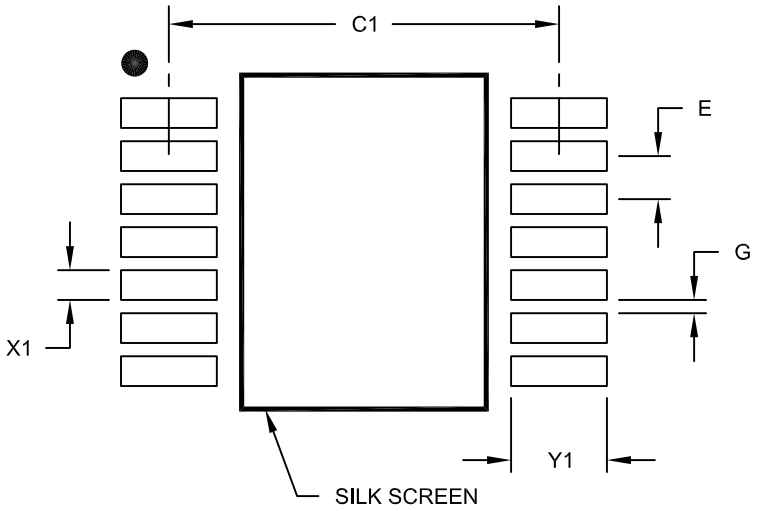
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

© 2002-2012 Microchip Technology Inc.

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

NOTES:

© 2002-2012 Microchip Technology Inc.

APPENDIX A: REVISION HISTORY

Revision G (February 2012)

The following is the list of modifications:

1. Updated the **Package Types** drawing to correct the device representation of the SC-70 package.
2. Updated package temperatures in the **Temperature Characteristics** table.
3. Corrected the marking information table for the 5-Lead SC-70 package (MCP6546 and MCP6546U) in **Section 5.1, Package Marking Information**.
4. Updated the package outline drawings in **Section 5.1 "Package Marking Information"**, to show all views for each package.
5. Minor editorial changes.

Revision F (September 2007)

The following is the list of modifications:

1. Corrected polarity of MCP6546U SOT-23-5 pin-out diagram on the first page.
2. Updated package outline drawings in **Section 5.1 "Package Marking Information"** per Marcom.

Revision E (September 2006)

The following is the list of modifications:

1. Added MCP6546U pinout for the SOT-23-5 package.
2. Clarified Absolute Maximum Analog Input Voltage and Current Specifications.
3. Added application information on unused comparators.
4. Added disclaimer to package outline drawings.

Revision D (May 2006)

The following is the list of modifications:

1. Added E-temp parts.
2. Changed minimum pull-up voltage specification (V_{PU}) to 1.6V for parts starting Dec. 2004 (week code 52); previous parts are specified at a minimum of V_{DD}.
3. Changed V_{HYST} temperature specifications to linear and quadratic temperature coefficients.
4. Changed specifications and plots to include E-Temp parts.
5. Added **Section 3.0 "Pin Descriptions"**.
6. Corrected package markings (**Section 5.1 "Package Marking Information"**).
7. Added **Appendix A: "Revision History"**.

Revision C (May 2003)

- Undocumented changes.

Revision B (December 2002)

- Undocumented changes.

Revision A (February 2002)

- Original Release of this Document.

NOTES:

© 2002-2012 Microchip Technology Inc.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device:	MCP6546:	Single Comparator
	MCP6546T:	Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)
	MCP6546RT:	Single Comparator (Rotated - Tape and Reel) (SOT-23 only)
	MCP6546UT:	Single Comparator (Tape and Reel) (SC-70, SOT-23)**(SOT-23-5 is E-Temp only)**
	MCP6547:	Dual Comparator
	MCP6547T:	Dual Comparator (Tape and Reel for SOIC and MSOP)
	MCP6548:	Single Comparator with $\overline{CS}$
	MCP6548T:	Single Comparator with $\overline{CS}$ (Tape and Reel for SOIC and MSOP)
	MCP6549:	Quad Comparator
	MCP6549T:	Quad Comparator (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
	E * =	-40°C to +125°C
	* SC-70-5 E-Temp parts not available at this release of the data sheet.	
Package:	LT =	Plastic Package (SC-70), 5-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead (MCP6549)
	ST =	Plastic TSSOP (4.4mm Body), 14-lead (MCP6549)

Examples:

a)	MCP6546T-I/LT:	Tape and Reel, Industrial Temperature, 5LD SC-70.
b)	MCP6546T-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23.
c)	MCP6546-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP.
d)	MCP6546-E/P:	Extended Temperature, 8LD PDIP.
e)	MCP6546-E/SN:	Extended Temperature, 8LD SOIC.
a)	MCP6546RT-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT23.
a)	MCP6546UT-E/LT:	Tape and Reel, Industrial Temperature, 5LD SC-70
b)	MCP6546UT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT23.
a)	MCP6547-I/MS:	Industrial Temperature, 8LD MSOP.
b)	MCP6547T-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP.
c)	MCP6547-I/P:	Industrial Temperature, 8LD PDIP.
d)	MCP6547-E/SN:	Extended Temperature, 8LD SOIC.
a)	MCP6548-I/SN:	Industrial Temperature, 8LD SOIC.
b)	MCP6548T-I/SN:	Tape and Reel, Industrial Temperature, 8LD SOIC.
c)	MCP6548-I/P:	Industrial Temperature, 8LD PDIP.
d)	MCP6548-E/SN:	Extended Temperature, 8LD SOIC.
a)	MCP6549T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC.
b)	MCP6549T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC.
c)	MCP6549-I/P:	Industrial Temperature, 14LD PDIP.
d)	MCP6549-E/ST:	Extended Temperature, 14LD TSSOP.

NOTES:

© 2002-2012 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE**.** Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC32 logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 978-1-62076-019-2

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2009

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/11

© 2002-2012 Microchip Technology Inc.

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru