MLX75123BA Time-of-Flight Companion Chip

Datasheet

Features

- Combines four high speed ADCs with a digital sensor control for Melexis' TOF camera sensors
- Integrated light source control with modulation frequencies between 12-40 MHz
- Programmable modulation frequencies to avoid module to module crosstalk
- Up to 8 raw phases per frame
- Pre-processed sum/subtract output modes for reduced data bandwidth
- Continuous or triggered operation modes
- Configurable over I^2C up to 400kHz
- 12-bit parallel camera interface up to 80Mpix/s
- Region of interest (ROI) selection and binning mode
- Horizontal/vertical flip/mirror modes
- Per-phase statistics and diagnostics
- 4 general purpose outputs
- Ambient operating temperature ranges of -20 +85°C and -40 +105°C
- AEC-Q100 qualification available!

Description

The MLX75123BA is a fully integrated companion chip for use with Melexis' Time-of-Flight (TOF) sensors (e.g. MLX75024). The IC is designed for automotive and non-automotive applications, including, but not limited to, gesture recognition, driver monitoring, skeleton tracking, people or obstacle detection and traffic monitoring.

It connects natively with several Melexis TOF sensors and features a configurable sequencer to operate them. The four built-in high-speed ADCs convert the analog sensor signals accurately to a digital 12-bit value. The digital sensor data is provided through a parallel camera port. An I^2C interface is implemented for system control, operating up to 400kHz.

Furthermore, MLX75123BA provides a synchronized control signal to drive the modulated light source (LED or laser based).

Combined with a Melexis TOF sensor, the MLX75123BA offers a cost-effective, integrated Time-Of-Flight camera solution, supporting a resolution up to 320x240 pixels (QVGA), at a maximum raw data frame-rate of 600Hz.

The device is available in a compact 7x7mm AQFN package and offers a variety of integration possibilities.

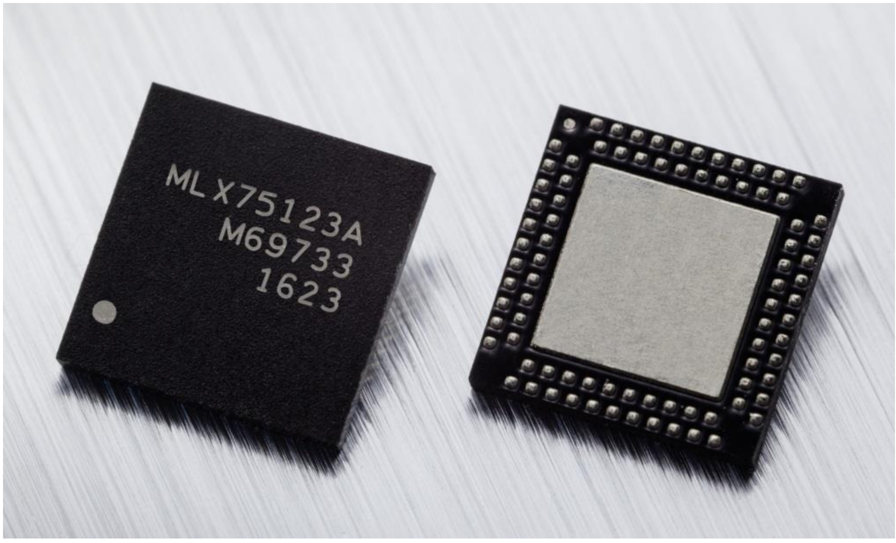


Figure 1 : MLX75123 package

Contents

1. Datasheet Changelog

Version	Date	Changes
1.0	17.01.2017	Initial version
1.1	11.04.2017	Updated section 14.3 : USER[0..3] are visible in Metadata1, not MetaData2 Updated section 8.1 : Clock thresholds depend on VDDD_1V8, not VDD_IO Updated section 0 : VIDEO_DRIVE has 2 options (low & high), not 16 Added and updated electrical operating conditions in section 8.2 Updated the power consumption values from section 9 Changed BLOCK_ENABLE register to BLOCK_DISABLE in section 17
1.2	02.08.2017	Added LEDP specifications for single ended mode Updated description of parameters in section 8.2 Updated default register values in section 14 Minor updates to register descriptions Updated default register values from chapter 14
1.3	31.01.2018	Updated ordering information in section 2 Updated description of I2C_SAVEREGMAP in section 13.5 Corrected calculation method for distance & amplitude in section 12 Update footprint recommendations in section 20.1 Several other minor description updates
1.4	23.3.2018	Removed Tx_Py_SETUP registers (not needed for application) Updated Tx_Py_SETTINGS bit[6] value to fixed high Added phase read out calculation Updated multiple register descriptions
1.5	03.07.2018	Updated register map and metadata 1&2 for MLX75123-BA
1.6	06.07.2018	Added binning, updated block diagram
1.7	30.08.2018	Updated VDDT_3V3 pin and reference schematic
1.8	01.02.2019	Few layout and design changes + corrections Discriminating MLX75023 and MLX75024 registers Updated default register map (phase shift 45deg) Added link between VDD_IO and input CLK level
1.9	03.12.2019	Added note about the CONFIG register settings being applied at next reset Added section about Tx_Py_SETUP Changed naming conventions for Tx_Bx_LATCH register
1.10	10.02.2020	Corrected Tx_Py_SETUP register addresses
1.11	12.03.2020	Modified the I2C SAVEREGMAP command

Table 1 : Datasheet changelog

2. Ordering Information

Product	Temperature Code	Package	Option Code	Packing Form
MLX75123	R	LA	BAG-000	RE
MLX75123	S	LA	BAG-000	RE
MLX75123	R	LA	ABA-000[1]	RE
MLX75123	S	LA	ABA-000[1]	RE

Table 2 : Order code(s)

Legend:

Temperature Code	R : -40°C to 105°C S : -20°C to 85°C
Package Code	LA : Array QFN package, 84pins
Option Code	BAG-000
Packing Form	RE : Reel SP : Sample bag (10 pcs)
Ordering Example	MLX75123RLA-BAG-000-RE

Table 3 : Ordering information details

Blank packages (dummy samples) of the MLX75123 can be ordered using the following order code : MLXDUMMYRLA-DUM-000-SP.

[1] MLX75123AB is replaced by MLX75123BA and will no longer be supported in the future.

3. Application System Architecture

A complete TOF system or camera module typically includes the following main components:

- MLX75123 + MLX750xx TOF chipset
- A synchronized high bandwidth near infrared (NIR) illumination source (LED or laser)
- Beam shaping optics for the light distribution
- A receiving sensor lens, optimized for maximum NIR transmittance
- A microprocessor or DSP for system control and sensor data calculation/ processing

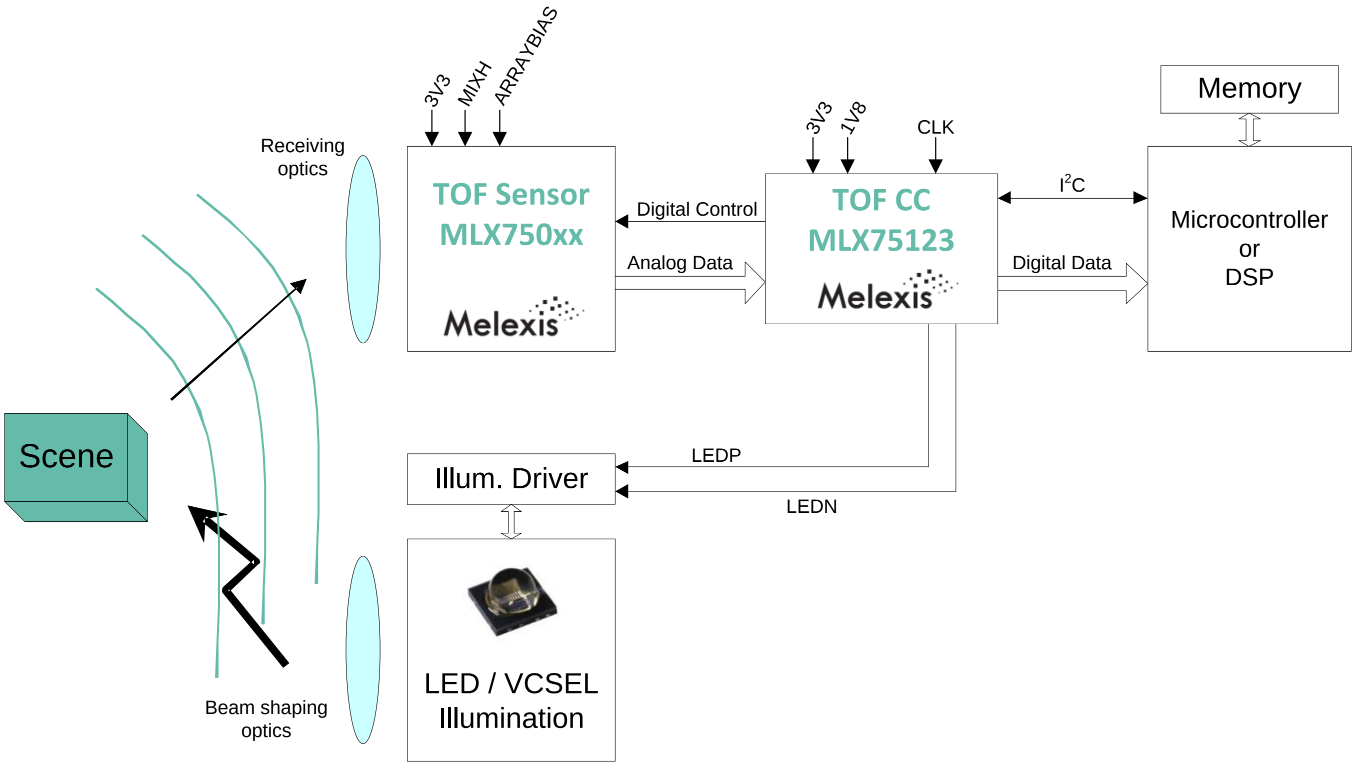


Figure 2: System architecture

4. System Block Diagram

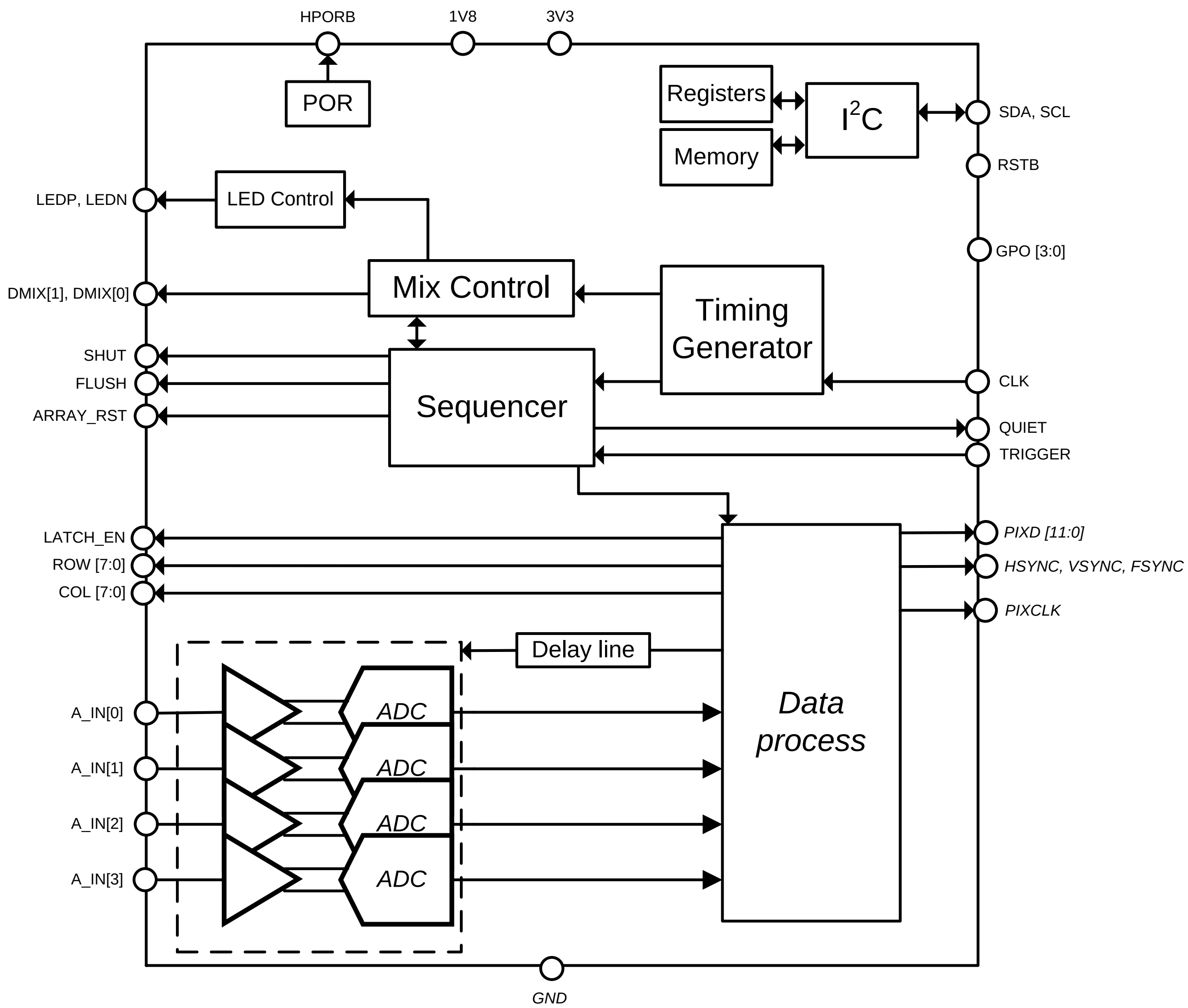


Figure 3 : System block diagram

5. Pinout Description

Designator	Pin #	Function	Description	Domain
PIXCLK	B28	Digital Out	Camera interface pixel clock	VDD_IO
HSYNC	B29	Digital Out	Camera interface horizontal sync	VDD_IO
VSYNC	A32	Digital Out	Camera interface vertical sync	VDD_IO
FSYNC	A31	Digital Out	Frame sync bit (optional)	VDD_IO
PIXD[11] PIXD[10] PIXD[9] PIXD[8] PIXD[7] PIXD[6] PIXD[5] PIXD[4] PIXD[3] PIXD[2] PIXD[1] PIXD[0]	B22 A25 B23 A26 B24 A27 B25 A28 B26 A29 B27 A30	Digital Out	Camera interface pixel data	VDD_IO
QUIET	A15	Digital Out	Configurable indication output	VDD_IO
CLK	B13	Digital In	Input clock	VDD_IO
TRIGGER	A13	Digital In	Frame trigger (= active high)	VDD_IO
RSTB	A14	Digital In	Reset pin of the MLX75123 (= active low)	VDD_IO
SDA SCL	B11 A12	Digital Out Digital In	I^2C clock and data	VDD_I2C
LEDP LEDN	B31 A34	Digital Out	Single ended or differential LED control signal	VDDD_3V3
DMIX[1] DMIX[0]	B32 A35	Digital Out	Differential pixel modulation signals	VDDD_3V3
LATCH_EN	A4	Digital Out	Pixel array latch enable	VDDD_3V3
SHUT	B2	Digital Out	Pixel array shutter	VDDD_3V3
ARRAY_RST	A3	Digital Out	Pixel array reset signal	VDDD_3V3
FLUSH	B3	Digital Out	Pixel array flush output	VDDD_3V3
ROW[7] ROW[6] ROW[5] ROW[4] ROW[3] ROW[2] ROW[1] ROW[0]	A2 B1 A1 A44 B40 A43 B39 A42	Digital Out	Row addressing	VDDD_3V3
COL[7] COL[6] COL[5] COL[4] COL[3] COL[2] COL[1] COL[0]	A37 B34 A38 B35 A39 B36 A40 B37	Digital Out	Column addressing	VDDD_3V3

Table 4.1

Designator	Pin #	Function	Description	Domain
A_IN[3] A_IN[2] A_IN[1] A_IN[0]	B7 A7 A6 B6	Analog In	Analog input of the pixel data	
HPORB	A19	Digital Out	Power on reset output signal (= active high)	
VDDA_1V8	B14	1V8 Supply	Analog supply in the 1.8V domain for the PLL (referenced to GNDA_1V8)	
VDDA_ADC_1V8	A9 B5	1V8 Supply	Analog supply for the ADC in the 1.8V analog domain (referenced to GNDA_ADC_1V8)	
VDDA_ADC_S_1V8	A10	1V8 Supply	Analog supply for the ADC in 1.8V analog domain for switched circuitry (referenced to GNDA_ADC_S_1V8)	
VDDD_1V8	B20	1V8 Supply	Digital supply in 1.8V digital domain (referenced to GNDD_1V8)	
VDDA_3V3	B4	3V3 Supply	Analog supply for the ADC in the 3.3V analog domain (referenced to GNDA_ADC_1V8)	
VDDT_3V3	B17	3V3 Supply	Analog supply for the comparator used in the power on reset control loop	
VDDD_3V3	A36 B38	3V3 Supply	Digital supply in 3.3V digital domain for the interface with the 75024 (referenced to GNDD_1V8)	
VDD_IO	B21 B30	Supply	IO supply pin, to guarantee proper operation of the MLX75123 CLK input must be at the same voltage level of VDD_IO. (1.8 or 3.3V) (referenced to GNDD_1V8)	
VDD_I2C	B12	Supply	1.8 or 3.3V supply for I2C interface (referenced to GNDD_1V8)	
GNDA_1V8	A16	GND	Analog ground in the 1.8V domain for the PLL	
GNDA_ADC_1V8	A5 B8	GND	Analog ADC ground for 1.8V	
GNDA_ADC_S_1V8	B9	GND	Analog ADC ground for the ADC in 1.8V analog domain switched	
GNDD_1V8	A22	GND	Digital ground in 1.8V digital domain	
GND_IO	A8 B15 A24 A33 B33 A41	GND	Digital ground for the interface to application processor	
GNDA_T_3V3	A18	GND	Analog ground for the comparator used in the power on reset control loop	
GPO[0] GPO[1] GPO[2] GPO[3]	B18 A20 B19 A21	Digital Out	General purpose output pins supplied by VDDT_3V3	
TEST[3] TEST[2] TEST[1] TEST[0]	B10 A11 B16 A17	GND	Test pins reserved for Melexis purposes, please connect to GND_IO.	
n.c.	A23		Not connected	

Table 4.2

6. Pin configuration and functions

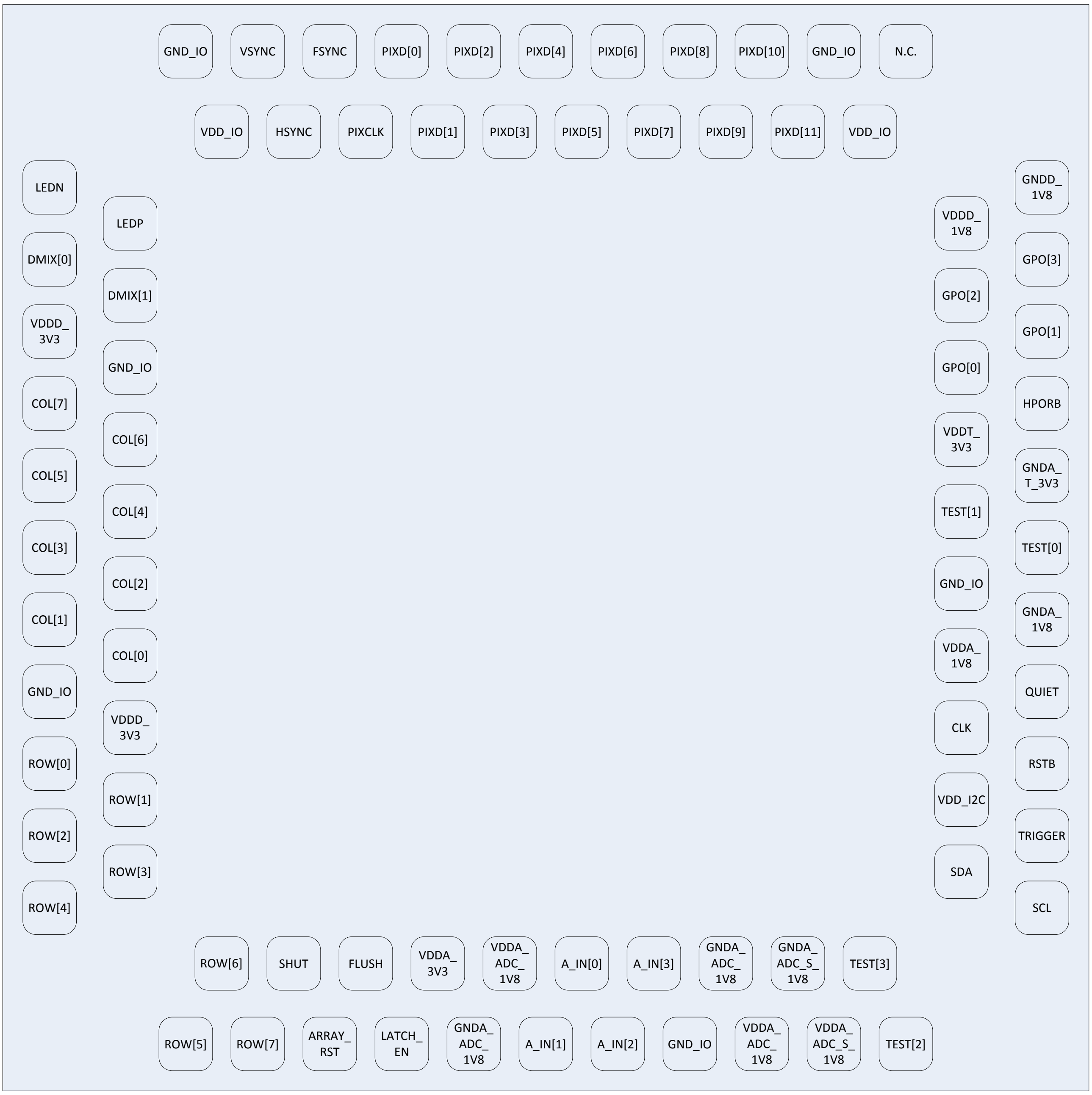


Figure 4: Array QFN package, 84 pins. Top view.

7. Absolute Maximum Ratings[1]

Parameter	Min.	Typ.	Max.[1]	Unit
3V3 supply voltage : VDDA_3V3, VDDD_3V3, VDD_IO, VDD_I2C	-0.2		4	V
1V8 supply voltage : VDDA_1V8, VDDA_ADC_1V8, VDDA_ADC_S_1V8, VDDD_1V8	-0.2		2.3	V
Analog input voltage A_IN[3], A_IN[2], A_IN[1], A_IN[0]	-0.2		VDDA_3V3 + 0.2	V
Digital IO voltage for MLX75024 : COL[x], ROW[x], DMIX[x], LATCH_EN, SHUT, ARRAY_RST, FLUSH	-0.2		VDDD_3V3 + 0.2	V
Digital IO voltage I2C	-0.2		VDD_I2C + 0.2	V
Digital IO voltage for video Interface : HSYNC, VSYNC, FSYNC, PIXCLK, PIXD[x], CLK, TRIGGER, RSTB	-0.2		VDD_IO + 0.2	V
Operating junction temperature	-40		125	°C
Storage temperature	-40		150	°C
ESD : Human Body Model			2	kV

Table 5 : Absolute Maximum Ratings

Note [1] : Absolute maximum ratings should never be exceeded to avoid permanent hardware failure.

8. Electrical Specifications

8.1. Crystal Oscillator Requirements

The clock input requires an accurate and clean input signal. It's recommended to use a crystal oscillator with the following specifications towards this purpose. The clock input ESD protection circuit limits the max. amplitude to VDD_IO+0.2V.
This requirement excludes the combination of a 3V3 clock generator together with 1V8 for VDD_IO. The oscillator drift is a less significant parameter and will not impact MLX75123 behaviour because all timing related parameters scale directly with this clock.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency		40		80	MHz
Positive clock threshold	V_{TH+}	1		VDD_IO + 0.2	V
Negative clock threshold	V_{TH-}			0.6	V
Jitter			30	60	ps

Table 6 : Input clock requirements

8.2. Operating Conditions

The operation conditions of MLX75123 are highly dependent on the configuration of the device.
Values listed in the Table 7 are measured at typical application conditions[1] :

- 80 MHz input clock
- 20 MHz modulation frequency
- 250 us integration time
- Four phase acquisition
- 50 distance FPS (= 200 raw frames)
- ± 5pF load on all output buffers

Parameter	Min.	Typ. -40 °C[2]	Typ. 25 °C[2]	Typ. 105 °C[2]	Peak[3]	Max.[6]	Unit
1V8 analog supply voltage	1.7	1.8	1.8			2	V
VDDA_1V8 supply current		4.57	4.52	4.45		tbd	mA
VDDA_ADC_1V8 supply current [3]		39.60	42.44	46.39	221	tbd	mA
VDDA_ADC_S_1V8 supply current [3]		9.58	10.25	11.05	58	tbd	mA
1V8 digital supply voltage	1.7	1.8	1.8	1.8		2	V
VDDD_1V8 supply current		8.5	8.61	8.84		tbd	mA
VDDD_I2C supply current @1V8			n/A [4]			tbd	mA
VDDD_IO supply current @1V8 [3, 5]		16	16.18	16.43	39	tbd	mA
3V3 analog supply voltage	3	3.3	3.3	3.3		3.6	V
VDDA_3V3 supply current			0.001			tbd	mA
3V3 digital supply voltage	3	3.3	3.3	3.3		3.6	V
VDDD_3V3 supply current [3]		1.29	1.28	1.29	7.85	tbd	mA
VDDD_I2C supply current @3V3			n/A [4]			tbd	mA
VDDD_IO supply current @3V3 [3, 5]		37.09	36.47	37.34	37	tbd	mA

Table 7 : Power requirements

Note [1] : A power calculator that simulates the power consumption at different application parameters is available on request

Note [2] : Temperatures listed in Table 7 are ambient temperatures

Note [3] : Some power domains only work for a specific time (for example during sensor read out). The overall (or average) power consumption thus depends on the duty cycle of that domain, but the peak current determines the power supply requirements and decouple techniques. Please refer to chapter 15 for more information.

Note [4] : The power consumption of VDDD_I2C depends on the amount of communication between MLX75123 and the host controller. When the device is only initialized once at start up no further power will be consumed.

Note [5] : The average power consumption of VDDD_IO depends on the actual data content that is being transmitted. Values in Table 7 are considered worst case conditions because in our setup the PIXD lines are toggling heavily.

Note [6] : The max. current consumption measured at the max. supply voltage incl. process & temperature variation for typical application conditions.

Parameter	Min.	Max.	Unit
VDDD_1V8 power on reset (POR)	1.3 - 1.45	1.45 - 1.55	V
POR on/off hysteresis	100		mV

Table 8 : Power on reset behaviour

When VDDD_1V8 drops under its lower threshold the device will reset. To avoid unwanted behaviour on noisy power supplies the device will only turn on again when VDDD_1V8 reaches its upper threshold voltage level.
A hysteresis of min. 100mV over temperature variation is guaranteed.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction to ambient thermal resistance	θ_{JA}		22.18		°C/W
Junction to package resistance [1]	θ_{JC}, θ_{JB}		1.19		°C/W
Moisture sensitivity level (MSL) [2]			3		

Table 9 : Package thermal behaviour

Note [1] : For an AQFN package incl. thermal pad the thermal resistance junction-board is equal to resistance junction-package
Note [2] : According to IPC/JEDEC J-STD-020E moisture/reflow sensitivity classification

Parameter	Min.	Typ.	Max.	Unit
Modulation frequency	12		40	MHz
Modulation frequency duty cycle	12.5	50	87.5	%
Modulation frequency phase accuracy			1	%
Modulation frequency settling time		20	100	us

Table 10 : Modulation frequency parameters

Parameter	Min.	Typ.	Max.	Unit
Input frequency clock (F_{IN})	40	80	80	MHz
Pixel clock frequency (PIXCLK)		F_{in}		MHz
I^2C frequency (SCL)	20		400	kHz
I^2C sink strength (SDA)	3			mA
VDD_IO buffer sink strength [3] (measured @ 200mV)	8.2	17.2	118	mA
VDD_IO buffer source strength [3] (measured @ VDD_IO - 200mV)	5.03	9.37	40	mA
VDDD_3V3 buffer sink strength (measured @ 200mV)	16.2	26.9	37.2	mA
VDDD_3V3 buffer source strength (measured @ VDDD_3V3 - 200mV)	10.6	17	24.8	mA

Table 11 : IO interface description

Note [3] : Measured at VDD_IO = 1V8, the values depend on the selection of VIDEO_DRIVE .
VIDEO_DRIVE can be selected in register CONFIG (0x1004) as explained in section 0.
Typical values are with VIDEO_DRIVE at low drive strength, max. values are for high VIDEO_DRIVE setting.

Parameter	Min.	Typ.	Max.	Unit
LVDS mode : recommended load impedance		100		Ohm
LVDS mode : output current		3.5		mA
LVDS mode : common mode voltage		1.2		V
Single ended mode : LEDP buffer sink strength (measured @ 200mV)	16.2	26.9	37.2	mA
Single ended mode : LEDP buffer source strength (measured @ VDDD_3V3 - 200mV)	10.6	17	24.8	mA

Table 12 : LED_P & LED_N electrical description

8.3. ADC Characteristics

MLX75123 has four single, general purpose analog to digital converters. All ADCs are used in a single ended configuration and independently from each other convert one analog output from MLX75024. Each pipelined ADC consists of a concurrently operating series of stages, isolated by a sample-hold buffer. For sampling rates > 25 MSPS it is needed to optimize the sample point with register ADC_DELAY_FT as explained in section 0

Parameter	Min.	Typ.	Max.	Unit
ADC resolution		12		bit
ADC input range	0.2		1.9	V
ADC sampling rate	20	$F_{in}/2$	40	MSPS
ADC conversion gain		500		uV/LSB
ADC to ADC gain mismatch		2	5	%
Analog input capacitance DC		5		pF
ADC delay line number of steps		32		
ADC delay line step size		1	3	ns

Table 13 : ADC Characteristics

9. Power Consumption

MLX75123 requires eight different voltage domains, each connected to either 1V8 or 3V3.
An overview of the different types can be found here:

Supply Domain	Voltage (V)	Power (mW)
VDDA_1V8	1.8	8.12
VDDA_ADC_1V8	1.8	77.05
VDDA_ADC_S_1V8	1.8	18.53
VDDD_1V8	1.8	15.57
VDD_IO (at 1V8)	1.8	29.16
VDD_I2C	3.3	n/A
VDDA_3V3	3.3	0.01
VDDD_3V3	3.3	4.24
	TOTAL	**153 mW** [1]

Table 14 : Typical power consumption

Note [1] : Calculations are based on typical application parameters listed in chapter 12.
Note [1] : Calculations are based on the average power consumption of each domain incl. temperature variation.

VDD_I2C and VDD_IO can be connected to 1V8 or 3V3 depending on the microprocessor. For EMC performance and a reduction in power consumption we strongly suggest to connect VDD_IO to 1V8.

We recommend to use independent regulators on each supply, however if from system point of view this is not desirable one could consider three regulators only. In this scenario we suggest to connect certain domains to each other with good decoupling techniques.
1V8 : VDDD_1V8, VDD_IO, VDD_I2C
1V8_Clean : VDDA_1V8, VDDA_ADC_1V8, VDDA_ADC_S_1V8
3V3 : VDDA_3V3, VDDD_3V3

In combination with MLX75023 or MLX75024 an extra MIXH regulator, 3V3_clean and negative ARRAYBIAS supply is required.

9.1. Power Up & Down Sequence

To guarantee a proper operation of MLX75123 it's considered mandatory to apply 1V8 prior to the 3V3 supply voltage. Reversely it's also recommended to disconnect 3V3 before 1V8 on power down. Both conditions are visualized in Figure 5. It's mandatory to keep both supplies within 500mV (δ_V) range of each other during start-up and power down sequences. When 1V8 ramps up too fast, compared to 3V3, a diode will be reversed biased which could lead to permanent HW damage, if 3V3 ramps up too fast, compared to 1V8, internal circuitry could be destroyed because of undefined currents.

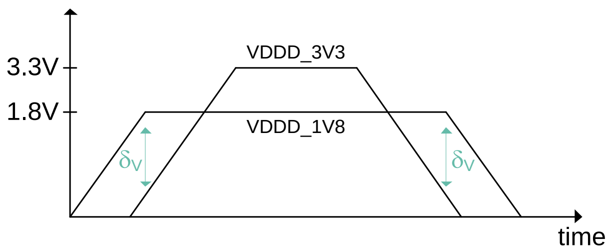


Figure 5 : Voltage domains startup sequence

9.2. Power on reset

In order to respect the power-up sequence, a power on reset circuitry has been implemented in the MLX75123-BA.
The main power on reset is called HPOR and has threshold in a range that guarantees the correct operation of the digital at the maximum specified clock speed.
HPORB is an active high signal which can trigger VDDD_3V3 once VDDD_1V8 is established correctly.
Recommended schematic for implementing that feature can be found below.

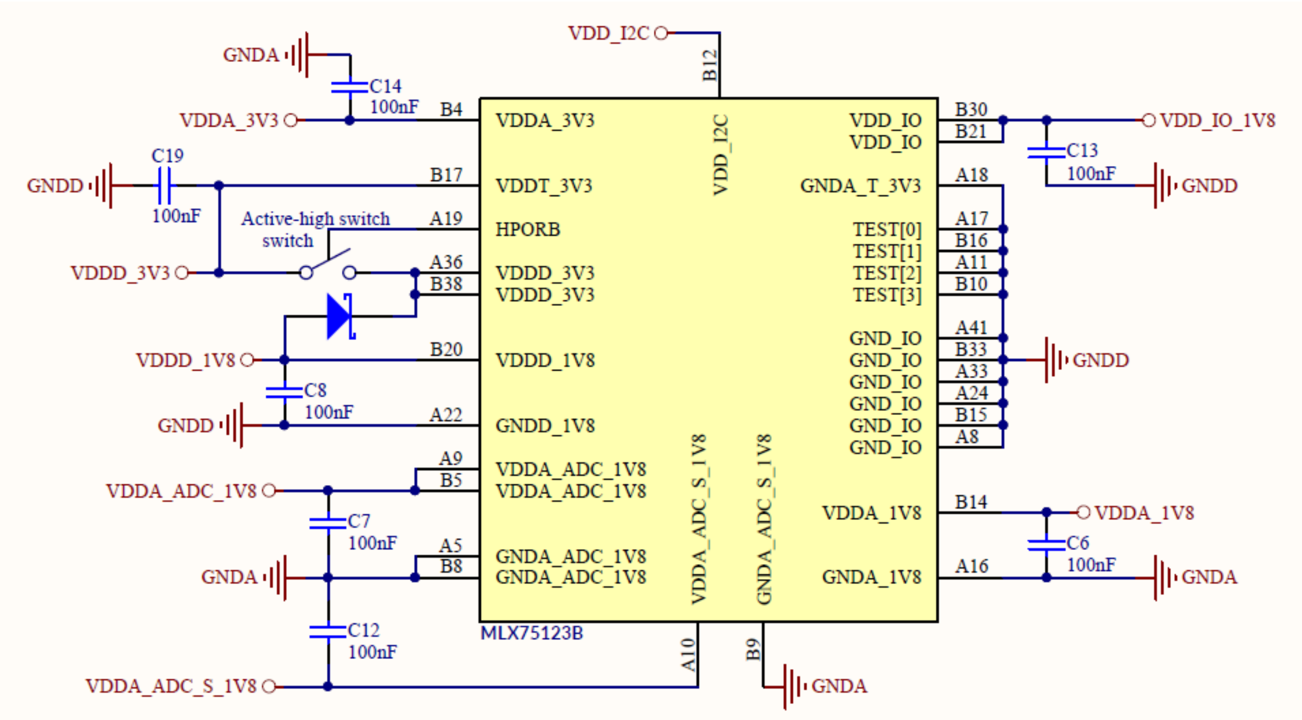


Figure 6: HPORB signal recommended implementation.

10. Output Modes

MLX75123 has six different data output modes. The output mode can be changed via register Tx_Py_SETTINGS as described in section 14.2.9 and can change per phase.

One Depthsense® pixel has two outputs, known as tap A and tap B, each in counterphase of one other. To reduce the calculation time from raw to depth information the data output already combines the information from both taps, either as a sum, or as a subtraction. Each pixel output A or B is a 12 bit value in range of 0 - 4095. The error bit in Mode #0 and Mode #2 is used to indicate if this pixel value before the sum or subtraction of A, or B, is between Tx_UPPER_LIMIT and Tx_LOWER_LIMIT thresholds as defined in the registers in section 14.2.5 and 14.2.6. If both tap A and tap B are between these limits this statistics bit will be high, if one of these outputs fails these criteria it will be set to 0. The MLX75024 test rows and ADC test row values are not evaluated against these thresholds, for these pixels the error bit is always 1.

10.1. Mode#0: 11bit A-B + error bit

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
error bit	11bit A-B pixel data										

The 13bit result of this subtraction is internally truncated to a 11bit value which corresponds to (A-B)/4.

10.2. Mode#1: 12bit A-B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A-B pixel data											

The 13bit result of this subtraction is internally truncated to a 12bit value which corresponds to (A-B)/2.

10.3. Mode#2: 11bit A+B + error bit

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
error bit	11bit A+B pixel data										

The 13bit result of this sum is internally truncated to a 11bit value which corresponds to (A+B)/4.

10.4. Mode#3: 12bit A+B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A+B pixel data											

The 13bit result of this sum is internally truncated to a 12bit value which corresponds to (A+B)/2.

10.5. Mode#4: Raw A

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit A pixel data											

10.6. Mode#5: Raw B

PIXD[11]	PIXD[10]	PIXD[9]	PIXD[8]	PIXD[7]	PIXD[6]	PIXD[5]	PIXD[4]	PIXD[3]	PIXD[2]	PIXD[1]	PIXD[0]
12bit B pixel data											

11. Parallel Output Sequence & Timing

The complete output data interface consists out of 16 parallel lines:

- 1 bit PIXCLK → uses same frequency as input CLK
- 1 bit FSYNC → indicates start of a new frame (one pulse per frame start)
- 1 bit VSYNC → indicates start of a new phase (one pulse per phase start, typically 4 pulses per frame)
- 1 bit HSYNC → indicates start of a new row (one pulse for each row start, typically 240 pulses per phase)
- 12 bit pixel data PIXD[11:0]

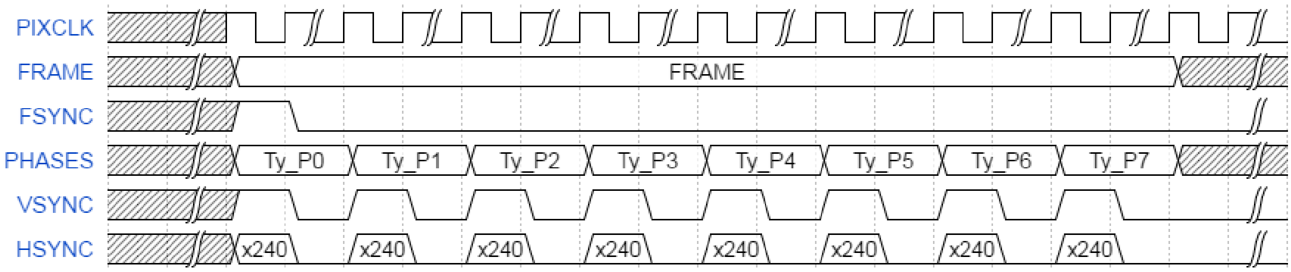


Figure 7 : FSYNC, VSYNC & HSYNC timing diagram[1]

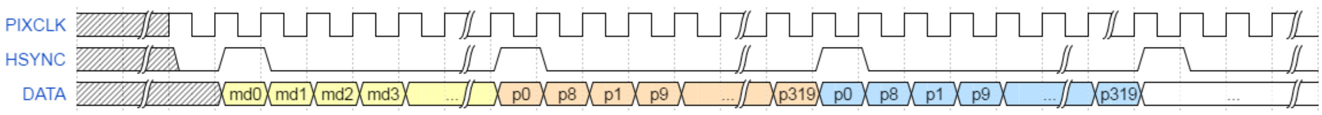
Note [1] : The length of HSYNC, VSYNC and FSYNC is one input clock pulse and is not programmable.

The sequential pixel output per row when used in combination with MLX75024 looks like 0, 8, 1, 9, …, 310, 318, 311, 319.
This means that the pixels should be re-ordered on the microcontroller to reconstruct a presentable distance map.
This pixel re-ordering can be done on the individual phase data or on the calculated distance map.

The serial output order can be simulated with this Matlab example code:

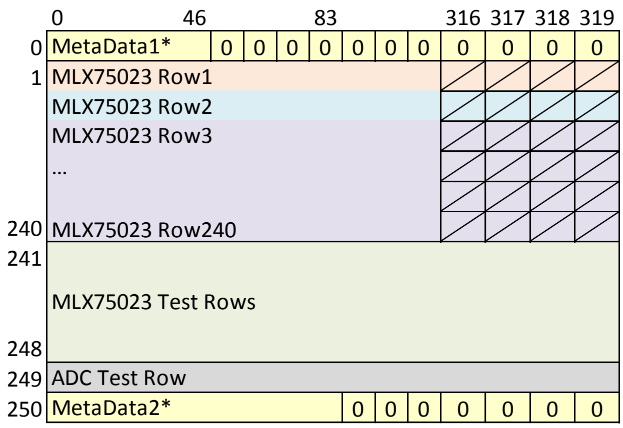
```
for x = 0:1:159
    y = mod(x,8) + 16*floor(x/8);
    z = mod(x,8) + 16*floor(x/8) + 8;
    fprintf('%d, %d, ', y, z);
end
```

On a timing diagram, without ROI, it would look like :



md0, md1, md2, md3, … = MetaData
p0, p8, p1, p9, … , p319 = PixelData / row

During a phase the maximum # of rows is limited to 251, depending on the features that are enabled or disabled.



- 1x MetaData1 line (optional)
- 240x Pixel row data
- 8x MLX75024 Test Rows (optional)
- 1x ADC Test Row (optional)
- 1x MetaData2 line (optional)

12. Distance Calculation

The distance data per pixel [in mm] can be calculated by the following formulas: (Matlab code)

```
p0 = TwoComp(phase0,16);
p180 = TwoComp(phase180,16);
p90 = TwoComp(phase90,16);
p270 = TwoComp(phase270,16);

I = p0 - p180;
Q = p270 - p90;

ampData = sqrt(I.^2 + Q.^2);
Phase = atan2(Q, I);
unAmbiguousRange = 0.5*299792458/modulationFrequency*1000;
coef_rad = unAmbiguousRange / (2*pi);
distData = (Phase+pi) * coef_rad + AbsoluteDistanceOffset;
while sum(distData(distData<0)) ~= 0
    distData(distData<0) = distData(distData<0) + unAmbiguousRange;
end
```

- *phase0, phase180, phase90, phase270* is the raw QVGA A-B data from the sensor at different phase intervals
- *TwoComp* is a local function that converts the unsigned data from Mode#1 A-B for each of the raw phases
- *UnAmbigiousRange* is the maximum range determined by the system modulation frequency
  (at modulation frequency of 20MHz this would be ~7.5m, at 40MHz it will be ~3.75m)
- *coef_rad* is a conversion coefficient from radians to degree
- *AbsoluteDistanceOffset* is a negative value obtained after calibration to measure the absolute distance
  (default value = 0)
- The *while* loop avoids negative distance values after the absolute distance calibration

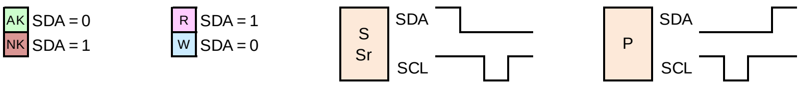
13. I2C Commands

MLX75123 features a standard (up to 400kHz) inter-integrated circuit communication interface, also known as I²C.
This device acts as a I²C slave with address 0x0067. This address can be reprogrammed via register I2C_ADDRESS.
If the input clock is not provided correctly to the device, I²C communication will not be possible and the device will not answer when receiving calls on its address.
More information on custom I²C addresses can be found in chapter 0 .
The size of both the register addresses & register data is 16bit.

I²C follows a strict timing sequence, the master device will initiate all communication, it's in control of the SCL line, data will be transmitted via SDA line. Each slave monitors the I²C bus and will respond to the master when needed.

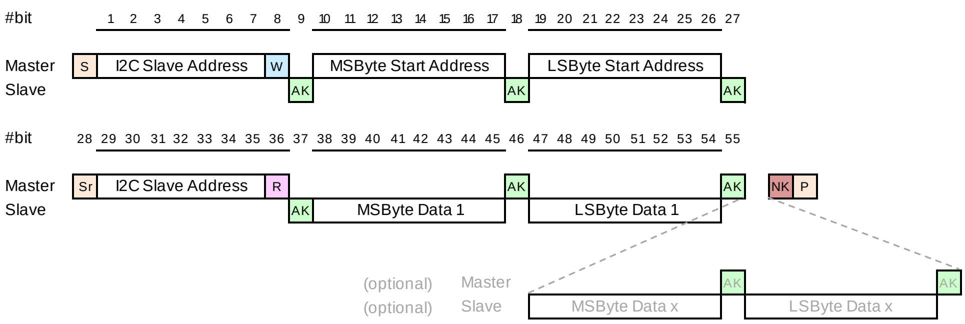
The following sections describe these timings for each of the individual commands.

Legend:



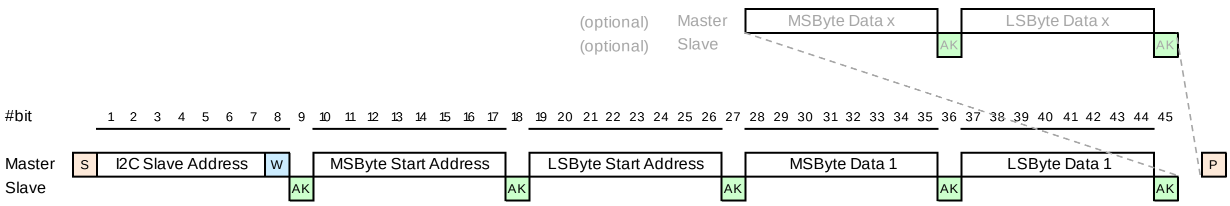
13.1. I²C_READ

This command allows you to read the registers listed in chapter 14. Normally it will read 1x register only, but the slave will continue to transmit data of sequential register addresses until the master terminates the communication.



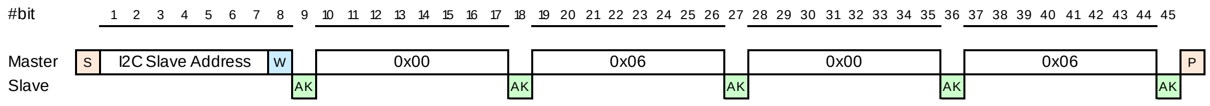
13.2. I²C_WRITE

This command allows you to write the registers listed in chapter 14. Normally you write 1x register only, but optionally the master can continue to transmit data of sequential register addresses to reduce the communication time when a lot of registers should be written.



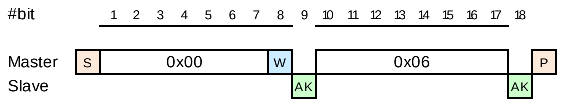
13.3. I^2C_RESET

This command will reset only MLX75123.



13.4. I^2C_GLOBAL_RESET

This command will reset all I^2C devices on the bus which support this standardized, but optional, command.



13.5. I^2C_SAVEREGMAP

On MLX75123 start-up all registers will be copied from the non-volatile memory into the volatile RAM, where they can be changed via the I^2C communication. When the device is restarted it will load all default values from the EEPROM again. It's possible to save your own custom register map into the EEPROM by an I^2C_WRITE of register 0x0000 with value 0x0100. When a copy into NVRAM is completed the register value will change from 0x0100 to 0x0000 (= self-clearing bit). It is advised to poll the register until it has value 0 before continuing any other communication to the device. Please note that an I^2C_READ of register 0x0000 is only possible after the above mentioned I2C command sequence. A full write cycle lasts about ±11 milliseconds. It's very important that during this time the device operation is not interrupted by either a HW or a SW reset, as this can lead to memory corruption.

For long term reliability of the NVRAM there's a maximum defined of I^2C_SAVEREGMAP cycles possible. The limit depends on the junction temperature and operating conditions:

- Max.100000 store cycles at 25°C
- Max.10000 store cycles at 125°C

14. Registers

MLX75123 has internal memory that is used to store the default register values and that can be used to store customer specific parameters like unique module no. identifiers. On start up this EEPROM is loaded into the RAM where it can be accessed during normal operation. Commands to read/write custom RAM settings into the EEPROM are available.
The complete memory map can be found here, it's strongly linked to values that can be read out from the metadata.

Memory Address	Description
0x1000	Configuration Parameters I
…	
0x100E	
0x1010	Table 1 Properties
…	
0x1022	
0x1024	T1_P0_SETTINGS
…	
0x1030	
0x1032	T1_P1_SETTINGS
…	
0x103E	
0x1040	T1_P2_SETTINGS
…	
0x104C	
0x104E	T1_P3_SETTINGS
…	
0x105A	
0x105C	T1_P4_SETTINGS
…	
0x1068	
0x106A	T1_P5_SETTINGS
…	
0x1076	
0x1078	T1_P6_SETTINGS
…	
0x1084	
0x1086	T1_P7_SETTINGS
…	
0x1092	

Memory Address	Description
0x1094	Table 2 Properties
…	
0x10A6	
0x10A8	T2_P0_SETTINGS
…	
0x10B4	
0x10B6	T2_P1_SETTINGS
…	
0x10C2	
0x10C4	T2_P2_SETTINGS
…	
0x10D0	
0x10D2	T2_P3_SETTINGS
…	
0x10DE	
0x10E0	T2_P4_SETTINGS
…	
0x10EC	
0x10EE	T2_P5_SETTINGS
…	
0x10FA	
0x10FC	T2_P6_SETTINGS
…	
0x1108	
0x110A	T2_P7_SETTINGS
…	
0x1116	
0x1118	Configuration Parameters II
0x111A	
0x111C	USER DEFINED (these can be read out in MetaData1)
0x111E	
0x1120	
0x1122	
0x1124	USER DEFINED
…	
0x119A	

14.1. Configuration Parameters Registers

General parameters that influence the behaviour of MLX75123 can be changed in the following registers.

Name : **I^{2}C_ADDRESS**

Address : 0x1000

Default Value : 0x0067

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	**GPO**				-	-	**I^{2}C_ADDRESS [6:0]**						

I^{2}C_ADDRESS : Programmable 8bit I^{2}C slave address.
A change of this register should be followed by a I2C_SAVEREGMAP operation (section 13.5) and a device reset before this new address will be active. Address 0x0032 should not be used.

GPO : Define the state of general purpose outputs at startup.

Name : **START_DELAY**

Address : 0x1002

Default Value : 0x00FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	**START_DELAY**								

START_DELAY : Defines the time between the NVRAM to EEPROM copy and the 3V3_READY signals are available and the start of the digital block for the first frame acquisition. It ranges from 0 - 5.12ms at 80MHz input clock, in steps of 9 bit.

Name : **CONFIG**

Address : 0x1004

Default Value : 0x0100

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	**PIXCLK_ disable**	-

Bit	7	6	5	4	3	2	1	0
	-	-	**VIDEO_ DRIVE**	**LED_MODE**	-	-	-	**HPORB_BUF_ disable**

PIXCLK_disable : Select the behaviour of the PIXCLK signal
- 0 : PIXCLK is enabled all the time
- 1 : PIXCLK is disabled during reset and integration time, and enabled only during readout

VIDEO_DRIVE : Select the drive strength of the video output buffers
- 0 : low drive strength
- 1 : high drive strength

By default the drive strength is set high for board debug processes, however the low drive strength is advised to reduce noise & EMC impact to a minimum in application conditions.

LED_MODE : Select single ended or differential LED control signals
- 0 : LED_P in single ended output mode (with LED_N connected to ground)
- 1 : LED_P and LED_N in LVDS mode

HPOR_BUF_disable : Used to enable or disable the HPORB signal.
- 0 : Buffer is enabled
- 1 : Buffer is disabled

Changing this register should be followed by an I2C_SAVEREGMAP operation (see section 13.5) and a device reset before the changes to become active.

Name : **PIXEL1**

Address : 0x1006

Default Value : 0xF464

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIXEL1_Y								**PIXEL1_X**							

MLX75123 offers the functionality to read out any pixel in addition to the normal read-out sequence. This feature can be used to read out single pixels or test structures from the sensor array. This register holds the X & Y coordinates of one pixel. This pixel will be read out only once per phase frame. PIXEL1_Y and PIXEL2_Y should be from 2 neighbouring rows

Name : **PIXEL2**

Address : 0x1008

Default Value : 0xF564

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIXEL2_Y								**PIXEL2_X**							

MLX75123 offers the functionality to read out any pixel in addition to the normal read-out sequence. This feature can be used to read out single pixels or test structures from the sensor array. This register holds the X & Y coordinates of one pixel. This pixel will be read out once per phase frame. PIXEL1_Y and PIXEL2_Y should be from 2 neighbouring rows

Name : **ADC_DELAY_FT**

Address : 0x100E

Default Value : 0x1000

Bit	15	14	13	12	11	10	9	8
	-	**LATCH_CFG**			**ADC_LATENCY [11:8]**			

Bit	7	6	5	4	3	2	1	0
	ADC_ LATENCY [7]	**-**	**PROG_DELAY**					**FRAME_ TABLE**

LATCH_CONFIG : Defines when the values from T1_BxRow_LATCH and T1_BxCol_LATCH are latched into the imager device :
- 0 : Latching happens only at startup (similar to 75123AB)
- 1 : Latching happens in front of every 1 frame
- 2 : Latching happens in front of every 2 frames
- 3 : Latching happens in front of every 4 frames
- 4 : Latching happens only once in front of the next frame

Note : At startup the latching happens in any case.

ADC_LATENCY : Changes the digital sampling point of the ADCs. Results in a full column shift of the image. Changes to ADC_LATENCY should be programmed into NVRAM (see section 13.5) and are only applied after sensor reset.

PROG_DELAY : The setting for the delay line that shall be applied during a full frame (0 = default sampling point)
This setting is not being applied during the automatic delay line sweep.
This register using GRAY coding : 0, 1, 3, 2, 6, 7, 5, 4, 12, 13, 15, 14, 10, 11, 9, 8,
24, 25, 27, 26, 30, 31, 29, 28, 20, 21, 23, 22, 18, 19, 17, 16 (listed in order of magnitude)
For increasing values, a delay is added, thus the sample point occurs later in time.

Note : Operation at non optimized PROG_DELAY settings can cause vertical stripe image artefacts in the image. More information on this effect and the optimization procedure is available upon request.

FRAME_TABLE : Selection of the Frame Table to be used.
0 : Frame Definition Table 1 is used to generate the frames
1 : Frame Definition Table 2 is used to generate the frames
A definition of these tables can be found in registers 0x1010 and 0x1094

Name : **SENSOR_TYPE**

Address : 0x100C

Default Value : 0x0001

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	**SENSOR_ TYPE**

SENSOR_TYPE : Should be set to 1 when used in combination with MLX75024.

Name : **DELAY_CONFIG**

Address : 0x1118

Default Value : 0x0000

Bit	15	14	13	12	11	10	9	8
	MOD_INV	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

MOD_INV : Inverts the sensor (DMIX0/1) modulation signal

Name : **BxROW_IDLE**

Address : 0x111A

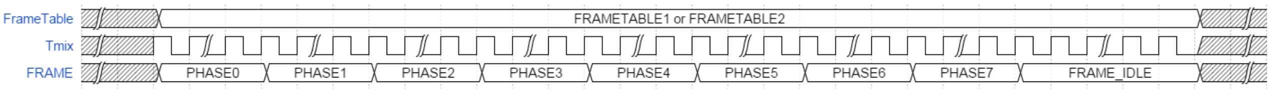
Default Value : 0x00F5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	**BxROW_IDLE**							

BxROW_IDLE : Pattern to be applied to BxROW[7:0] bits during reset, integration & sampling phases

14.2. FrameTable & Phase Registers

MLX75123 has two different FrameTable definitions. Each table consists of eight individual configurable phases as indicated in Table 15. The FrameTable used to capture the frames can be selected register 0x100E *ADC_DELAY_FT*.



FrameTable Definition	Phase Definition
T1_SETTINGS T1_IDLETIME T1_MODE T1_FRAMECOUNT T1_UPPER_LIMIT T1_LOWER_LIMIT T1_ROI_START & T1_ROI_SIZE T1_Bx_LATCH	T1_P0_SETTINGS T1_P0_INTEGRATION T1_P0_PREHEAT T1_P0_PREMIX T1_P0_IDLE T1_P0_SETUP
	... Phase1
	... Phase2
	... Phase3
	... Phase4
	... Phase5
	... Phase6
	... Phase7
T2_SETTINGS T2_IDLETIME T2_MODE T2_FRAMECOUNT T2_UPPER_LIMIT T2_LOWER_LIMIT T2_ROI_START & T2_ROI_SIZE T2_Bx_LATCH	T2_P0_SETTINGS T2_P0_INTEGRATION T2_P0_PREHEAT T2_P0_PREMIX T2_P0_IDLE T2_P0_SETUP
	... Phase1
	... Phase2
	... Phase3
	... Phase4
	... Phase5
	... Phase6
	... Phase7

Table 15 : Frametable configuration

14.2.1. Frame : Tx_SETTINGS

Memory Address	Default Value	
0x1010	0x2C03	T1_SETTINGS
0x1094	0x2C03	T2_SETTINGS

Bit	15	14	13	12	11	10	9	8
	-	**Tx_EN_ TEST_ADC**	**Tx_EN_ TEST_ROW**	-	**Tx_EN_ META2**	**Tx_EN_ META1**	**Tx_BINNING**	

Bit	7	6	5	4	3	2	1	0
	Tx_FLIP_MIRROR		**Tx_QUIET**		-	**Tx_PHASE_COUNT**		

Tx_EN_TEST_ADC : One additional row of pixel data will connected to a known voltage reference (on/off)
The data of this row can only be evaluated in Mode #4 or Mode #5 (from section 9.2)
This known voltage reference per pixel changes with BxCOL[4:3] column addresses.
00 : ADC inputs connected to sensor
01 : ADC inputs connected 0V
10 : ADC inputs connected to +Vref
11 : ADC inputs connected to -Vref

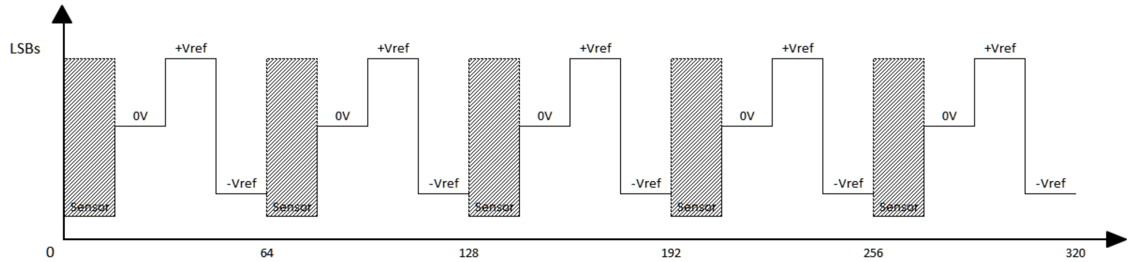


Figure 8 : EN_TEST_ADC row for Mode #4 (12bit A)

Tx_EN_TEST_ROW : Enable the eight MLX75024 test rows (on/off)

Tx_EN_META2 : Enable/disable Metadata2 line (on/off)

Tx_EN_META1 : Enable/disable Metadata1 line (on/off)

Tx_BINNING : Enable/disable the binning feature.
00 : default
01 : 2x2 binning enabled, when 2x2 binning is enabled, ROI has to be limited to 160 x 120 pixels using the registers Tx_ROI_ROW_SIZE = 120 and Tx_ROI_COL_SIZE = 10.
10: 4x4 binning enabled, when 4x4 binning is enabled, ROI has to be limited to 80 x 60 pixels using the registers Tx_ROI_ROW_SIZE = 60 and Tx_ROI_COL_SIZE = 5.

Tx_FLIP_MIRROR : Mirror the image along its horizontal and/or vertical central axis
00 : default
01 : Flip (along horizontal axis)
10 : Mirror (along vertical axis)
11 : Flip & mirror

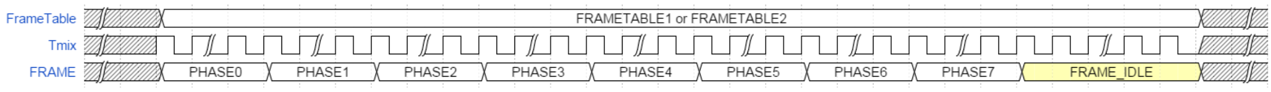
NB: When using Flip and/or mirror, there is not possibility to get the temperature data from the MLX75024 using the Metadata2.

Tx_QUIET : Select behaviour of the quiet pin
00 : default, QUIET is not used
01 : QUIET is high in reset + integration phase
10 : QUIET is high in readout phase
11 : QUIET is high in reset + integration + readout phase

Tx_PHASE_COUNT : # phases to be accumulated in one FrameTable (between 0-7)

14.2.2. Frame : Tx_IDLETIME

After the eight phases it's possible to define a frame idle time. This time can be used to fix the distance framerate. It's defined in number of FMOD pulses and ranges from 0 - 4 294 967 296.



Memory Address	Default Value	
0x1012	0xAE60	T1_IDLETIME0
0x1014	0x000A	T1_IDLETIME1
0x1096	0xAE60	T2_IDLETIME0
0x1098	0x000A	T2_IDLETIME1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Tx_IDLETIME1 [31:16]															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_IDLETIME0 [15:0]															

Tx_IDLETIME in Tmix pulses can be calculated as :

$$\#pulses = time\ (ms) \cdot Fmod\ (kHz)$$

For a typical application setup with Tint = 250us, F_{MOD} = 20MHz and a distance framerate of 25 FPS the Tx_IDLETIME is 35ms.

$$\#pulses = 35 \cdot 20000 = 700\ 000 = \text{0x } \underline{\text{000A}}\ \underline{\text{AE60}} \text{ (hexadecimal)}$$

IDLETIME1 IDLETIME0

14.2.3. Frame : Tx_MODE

Memory Address	Default Value	
0x1016	0x6E80	T1_MODE
0x109A	0x6E80	T2_MODE

Bit	15	14	13	12	11	10	9	8
	Tx_MOD_DUTY_CYCLE			**-**	**Tx_RDIV**			**Tx_NDIV [8]**

Bit	7	6	5	4	3	2	1	0
	Tx_NDIV [7:6]		**Tx_VSYNC**	**Tx_HSYNC**	**Tx_PIXCLK**	**Tx_FSYNC**	**Tx_TRIGGER**	

Tx_MOD_DUTY_CYCLE : Duty cycle correction for the MOD signal

000 : 12.5%
001 : 25%
010 : 37.5%
011 : 50%
100 : 62.5%
101 : 75%
110 : 87.5%

Tx_RDIV : PLL RDIV value (see chapter 18)

Tx_NDIV [8:6] : PLL NDIV value (see chapter 18)

Tx_VSYNC : 0: default / 1: VSYNC inverted

Tx_HSYNC : 0: default / 1: HSYNC inverted

Tx_PIXCLK : 0: default / 1: PIXCLK inverted

Tx_FSYNC : 0: default / 1: FSYNC inverted

Tx_TRIGGER :

00 : Continuous Mode :
Once started, the system will execute the phase measurements according the configured sequence.

01: Triggered Multi Frame Mode:
In this mode the system will acquire a variable number of frames with a preset number of phases, after which time the system will return to idle state. The number of frames to be acquired can be set using register *Tx_FRAME_COUNT*.

14.2.4. Frame : Tx_FRAMECOUNT

This register holds the amount of frames to be captured in triggered multi frame mode in the range of 0 - 65535.

Memory Address	Default Value	
0x1018	0x0000	T1_FRAMECOUNT
0x109C	0x0000	T2_FRAMECOUNT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_FRAMECOUNT															

14.2.5. Frame : Tx_UPPER_LIMIT

The value of this register is used as high threshold value. The amount of pixels that return a value higher than this threshold will be counted and will be available in the statistics. It can be used to indicate low confidence pixels.
This threshold is also used for the error bit in Mode#0 (chapter 10.1) and Mode#2 (chapter 0) to indicate if either of the two raw values (A or B), before subtraction or sum, exceeds this limit.

Memory Address	Default Value	
0x101A	0xFFFF	T1_UPPER_LIMIT
0x109E	0xFFFF	T2_UPPER_LIMIT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_UPPER_LIMIT															

14.2.6. Frame : Tx_LOWER_LIMIT

The value of this register is used as low threshold value. The amount of pixels that return a value lower than this threshold will be counted and will be available in the statistics. It can be used to indicate saturated pixels.
This threshold is also used for the error bit in Mode#0 (chapter 10.1) and Mode#2 (chapter 0) to indicate if either of the two raw values (A or B), before subtraction or sum, exceeds this limit.

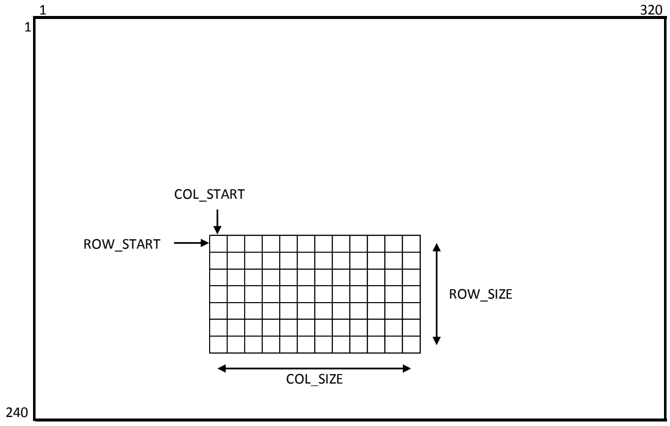
Memory Address	Default Value	
0x101C	0x0000	T1_LOWER_LIMIT
0x10A0	0x0000	T2_LOWER_LIMIT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_LOWER_LIMIT															

14.2.7. Frame : Tx_ROI_START & Tx_ROI_SIZE

The *Region Of Intrest* (ROI) registers enable you to read out only part of the complete MLX75024 pixel array.
This region is defined by its start location and its size.
Rows (vertical orientation) are defined by a multiplier of 1, columns (horizontal orientation) are multipliers of 16.

Memory Address	Default Value	
0x101E	0x0000	T1_ROI_START
0x1020	0xF014	T1_ROI_SIZE
0x10A2	0x0000	T2_ROI_START
0x10A4	0xF014	T2_ROI_SIZE



Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_ROI_ROW_START								**Tx_ROI_COL_START**							

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_ROI_ROW_SIZE								**Tx_ROI_COL_SIZE**							

Tx_ROI_ROW_START : Start coordinate in vertical direction (ROW_START on the graph)
Tx_ROI_COL_START : Start coordinate in horizontal direction (COL_START on the graph)

Tx_ROI_ROW_SIZE : Size in vertical direction (ROW_SIZE on the graph)
Tx_ROI_COL_SIZE : Size in horizontal direction (COL_SIZE on the graph)

NB : ROI readout combined with gain mode of the MLX75024 has to be at least 80 columns wide. Shorter columns widths are not possible due to gain settings.

14.2.8. Frame : Tx_Bx_LATCH

Memory Address	Default Value	
0x1022	0x000C	T1_Bx_LATCH
0x10A6	0x000C	T2_Bx_LATCH

Default Value : 0x000C (in configuration with sensor MLX75024)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_BxCOL_LATCH								**Tx_BxROW_LATCH**							

BxCOL_LATCH : Pattern to be applied to BxCOL[7:0] bits.
BxROW_LATCH : Pattern to be applied to BxROW[7:0] bits .
0x0C : BxROW_LATCH pattern to apply for MLX75024 in application mode
0x0E : BxROW_LATCH pattern to apply for MLX75024 with 4 test columns enabled

Note : For a configuration with MLX75023 this register value must change to 0xFF11.

14.2.9. Phase : Tx_Py_SETTINGS

Each phase frame has its own phase configuration parameters.

Memory Address	Default Value	FRAMETABLE 1
0x1024	0x0281	T1_P0_SETTINGS
0x1032	0x0285	T1_P1_SETTINGS
0x1040	0x0283	T1_P2_SETTINGS
0x104E	0x0287	T1_P3_SETTINGS
0x105C	0x0000	T1_P4_SETTINGS
0x106A	0x0000	T1_P5_SETTINGS
0x1078	0x0000	T1_P6_SETTINGS
0x1086	0x0000	T1_P7_SETTINGS

Memory Address	Default Value	FRAMETABLE 2
0x10A8	0x0281	T2_P0_SETTINGS
0x10B6	0x0285	T2_P1_SETTINGS
0x10C4	0x0283	T2_P2_SETTINGS
0x10D2	0x0287	T2_P3_SETTINGS
0x10E0	0x0000	T1_P4_SETTINGS
0x10EE	0x0000	T2_P5_SETTINGS
0x10FC	0x0000	T2_P6_SETTINGS
0x110A	0x0000	T2_P7_SETTINGS

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	**Tx_Py_OUTPUT_MODE**			**Tx_Py_STATIC**

Bit	7	6	5	4	3	2	1	0
	Tx_Py_DMIX	-	-	**Tx_Py_LIGHT**	**Tx_Py_PHASE_SHIFT**			

Tx_Py_OUTPUT_MODE : Define the output mode per phase

- 000 : Mode #0 : 11bit (A-B)/4 data + 1bit statistics
- 001 : Mode #1 : 12bit (A-B)/2 data
- 010 : Mode #2 : 11bit (A+B)/4 data + 1bit statistics
- 011 : Mode #3 : 12bit (A+B)/2 data
- 100 : Mode #4 : 12bit A
- 101 : Mode #5 : 12bit B

Tx_Py_STATIC : Only evaluated if Tx_Py_DMIX = 1

- 0 : static level on DMIX[1:0] during integration is 2'b00
- 1 : static level on DMIX[1:0] during integration is 2'b11

Tx_Py_DMIX : Enable (0) / disable (1) MIX pulses during the integration time
When disabled DMIX[1] and DMIX[0] signal levels are defined by Tx_Py_STATIC

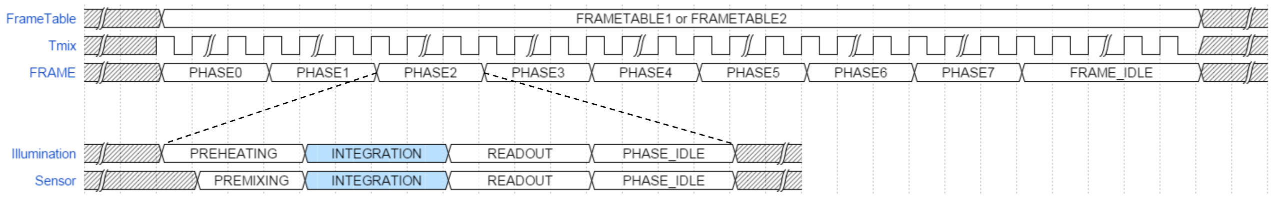
Tx_Py_LIGHT : Enable (1) / disable (0) the illumination pulses during the integration time

Tx_Py_PHASE_SHIFT [3:0] : Selects the phase shift between MOD and DMIX[0] signals.
DMIX[1] is always 180° shift compared to DMIX[0] (except during reset phase)

- 000 : 0°
- 001 : 45°
- 010 : 90°
- 011 : 135°
- 100 : 180°
- 101 : 225°
- 110 : 270°
- 111 : 315°

14.2.10. Phase : Tx_Py_INTEGRATION

These registers are used to define the integration times for each of the different phases.
It ranges from 0 - 4 294 967 295 FMOD periods.



Memory Address	Default Value	FRAMETABLE 1
0x1026	0x1388	T1_P0_INT0
0x1028	0x0000	T1_P0_INT1
0x1034	0x1388	T1_P1_INT0
0x1036	0x0000	T1_P1_INT1
0x1042	0x1388	T1_P2_INT0
0x1044	0x0000	T1_P2_INT1
0x1050	0x1388	T1_P3_INT0
0x1052	0x0000	T1_P3_INT1
0x105E	0x0000	T1_P4_INT0
0x1060	0x0000	T1_P4_INT1
0x106C	0x0000	T1_P5_INT0
0x106E	0x0000	T1_P5_INT1
0x107A	0x0000	T1_P6_INT0
0x107C	0x0000	T1_P6_INT1
0x1088	0x0000	T1_P7_INT0
0x108A	0x0000	T1_P7_INT1

Memory Address	Default Value	FRAMETABLE 2
0x10AA	0x1388	T2_P0_INT0
0x10AC	0x0000	T2_P0_INT1
0x10B8	0x1388	T2_P1_INT0
0x10BA	0x0000	T2_P1_INT1
0x10C6	0x1388	T2_P2_INT0
0x10C8	0x0000	T2_P2_INT1
0x10D4	0x1388	T2_P3_INT0
0x10D6	0x0000	T2_P3_INT1
0x10E2	0x0000	T2_P4_INT0
0x10E4	0x0000	T2_P4_INT1
0x10F0	0x0000	T2_P5_INT0
0x10F2	0x0000	T2_P5_INT1
0x10FE	0x0000	T2_P6_INT0
0x1100	0x0000	T2_P6_INT1
0x110C	0x0000	T2_P7_INT0
0x110E	0x0000	T2_P7_INT1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Tx_Py_INT1 [31:16]															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_Py_INT0 [15:0]															

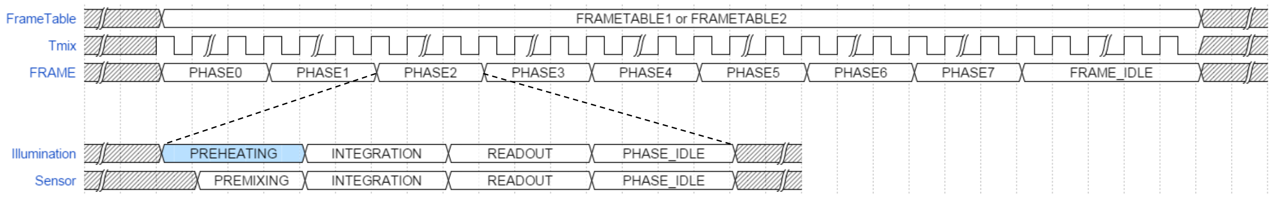
The integration time can be calculated in a similar way as the Tx_IDLETIME time in section 14.2.2.
Example : Tint 250us (= 0.25ms) with F_{MOD} 20MHz

$$\#pulses = 0.25 \cdot 20000 = 5\,000 = \text{0x } \underline{0000}\ \underline{1388} \text{ (hexadecimal)}$$

0000 → Tx_Py_INT1, 1388 → Tx_Py_INT0

14.2.11. Phase : Tx_Py_PREHEAT

Illumination preheating can be used to avoid IU waveform transients at the beginning of each pulse train.
It defines the amount of light pulses before the actual integration time is started.
It ranges from 0 - 65535 FMOD periods.



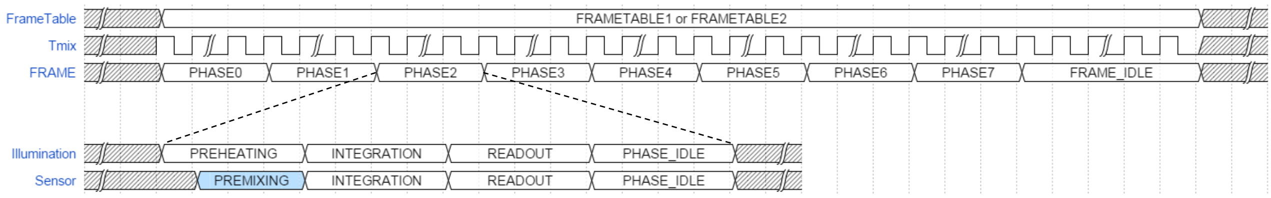
Memory Address	Default Value	FRAMETABLE 1
0x102A	0x0000	T1_P0_PREHEAT
0x1038	0x0000	T1_P1_PREHEAT
0x1046	0x0000	T1_P2_PREHEAT
0x1054	0x0000	T1_P3_PREHEAT
0x1062	0x0000	T1_P4_PREHEAT
0x1070	0x0000	T1_P5_PREHEAT
0x107E	0x0000	T1_P6_PREHEAT
0x108C	0x0000	T1_P7_PREHEAT

Memory Address	Default Value	FRAMETABLE 2
0x10AE	0x0000	T2_P0_PREHEAT
0x10BC	0x0000	T2_P1_PREHEAT
0x10CA	0x0000	T2_P2_PREHEAT
0x10D8	0x0000	T2_P3_PREHEAT
0x10E6	0x0000	T2_P4_PREHEAT
0x10F4	0x0000	T2_P5_PREHEAT
0x1102	0x0000	T2_P6_PREHEAT
0x1110	0x0000	T2_P7_PREHEAT

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_Py_PREHEAT															

14.2.12. Phase : Tx_Py_PREMIX

Sensor premixing can be used to avoid temperature transients at the beginning of each integration time.
It ranges from 0 - 65535 FMOD periods.



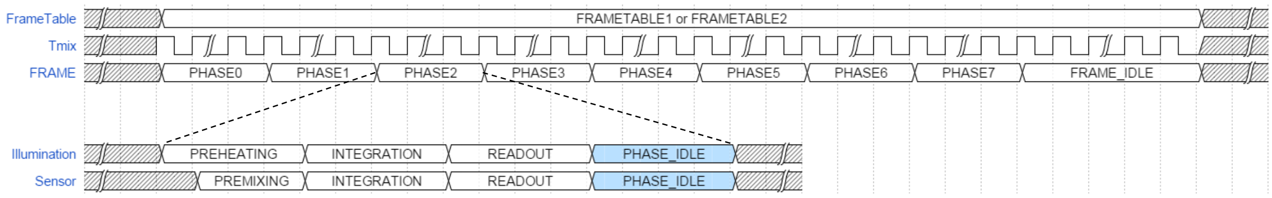
Memory Address	Default Value	FRAMETABLE 1
0x102C	0x0000	T1_P0_PREMIX
0x103A	0x0000	T1_P1_PREMIX
0x1048	0x0000	T1_P2_PREMIX
0x1056	0x0000	T1_P3_PREMIX
0x1064	0x0000	T1_P4_PREMIX
0x1072	0x0000	T1_P5_PREMIX
0x1080	0x0000	T1_P6_PREMIX
0x108E	0x0000	T1_P7_PREMIX

Memory Address	Default Value	FRAMETABLE 2
0x10B0	0x0000	T2_P0_PREMIX
0x10BE	0x0000	T2_P1_PREMIX
0x10CC	0x0000	T2_P2_PREMIX
0x10DA	0x0000	T2_P3_PREMIX
0x10E8	0x0000	T2_P4_PREMIX
0x10F6	0x0000	T2_P5_PREMIX
0x1104	0x0000	T2_P6_PREMIX
0x1112	0x0000	T2_P7_PREMIX

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_Py_PREMIX															

14.2.13. Phase: Tx_Py_IDLE

Increasing PHASE_IDLE time will have impact on motion robustness, ideally keep to 0.



Memory Address	Default Value	FRAMETABLE 1
0x102E	0x0000	T1_P0_IDLE
0x103C	0x0000	T1_P1_IDLE
0x104A	0x0000	T1_P2_IDLE
0x1058	0x0000	T1_P3_IDLE
0x1066	0x0000	T1_P4_IDLE
0x1074	0x0000	T1_P5_IDLE
0x1082	0x0000	T1_P6_IDLE
0x1090	0x0000	T1_P7_IDLE

Memory Address	Default Value	FRAMETABLE 1
0x10B2	0x0000	T2_P0_IDLE
0x10C0	0x0000	T2_P1_IDLE
0x10CE	0x0000	T2_P2_IDLE
0x10DC	0x0000	T2_P3_IDLE
0x10EA	0x0000	T2_P4_IDLE
0x10F8	0x0000	T2_P5_IDLE
0x1106	0x0000	T2_P6_IDLE
0x1114	0x0000	T2_P7_IDLE

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_Py_IDLE															

14.2.14. Phase: Tx_Py_SETUP

PREHEAT and PREMIX are part of SETUP time. The value in the Tx_Py_SETUP register needs to be bigger than the value in Tx_Py_PREHEAT or Tx_Py_PREMIX depending on which of the two durations is longer. If the PREHEAT or PREMIX time are longer than the SETUP time, PREHEAT or PREMIX will not be applied.

Memory Address	Default Value	FRAMETABLE 1
0x1030	0x0000	T1_P0_SETUP
0x103E	0x0000	T1_P1_SETUP
0x104C	0x0000	T1_P2_SETUP
0x105A	0x0000	T1_P3_SETUP
0x1068	0x0000	T1_P4_SETUP
0x1076	0x0000	T1_P5_SETUP
0x1084	0x0000	T1_P6_SETUP
0x1092	0x0000	T1_P7_SETUP

Memory Address	Default Value	FRAMETABLE 1
0x10B4	0x0000	T2_P0_SETUP
0x10C2	0x0000	T2_P1_SETUP
0x10D0	0x0000	T2_P2_SETUP
0x10DE	0x0000	T2_P3_SETUP
0x10EC	0x0000	T2_P4_SETUP
0x10FA	0x0000	T2_P5_SETUP
0x1108	0x0000	T2_P6_SETUP
0x1116	0x0000	T2_P7_SETUP

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tx_Py_SETUP															

14.2.15. Phase : READOUT

The time needed to read a single phase frame is not configurable and mainly depends on the input clock as described in section 8.1. It can be calculated as following:

$$\text{ReadoutTime (in microseconds)} = \frac{\text{Tx\_ROI\_COL\_SIZE} \cdot \text{Tx\_ROI\_ROW\_SIZE}}{\text{input clock (in MHz)}}$$

A full QVGA image readout with a maximum input clock of 80MHz is 960 µs.

14.3. USER Registers

Memory Address	Default Value	
0x111C	0x0000	USER0
0x111E	0x0000	USER1
0x1120	0x0000	USER2
0x1122	0x0000	USER3
0x1124	0x0000	USER4
0x1126	0x0000	USER5
0x1128	0x0000	USER6
0x112A	0x0000	USER7
0x112C	0x0000	USER8
0x112E	0x0000	USER9
0x1130	0x0000	USER10
0x1132	0x0000	USER11
0x1134	0x0000	USER12
0x1136	0x0000	USER13
0x1138	0x0000	USER14
0x113A	0x0000	USER15
0x113C	0x0000	USER16
0x113E	0x0000	USER17
0x1140	0x0000	USER18
0x1142	0x0000	USER19
0x1144	0x0000	USER20
0x1146	0x0000	USER21
0x1148	0x0000	USER22
0x114A	0x0000	USER23
0x114C	0x0000	USER24
0x114E	0x0000	USER25
0x1150	0x0000	USER26
0x1152	0x0000	USER27
0x1154	0x0000	USER28
0x1156	0x0000	USER29
0x1158	0x0000	USER30
0x115A	0x0000	USER31

Memory Address	Default Value	
0x115C	0x0000	USER32
0x115E	0x0000	USER33
0x1160	0x0000	USER34
0x1162	0x0000	USER35
0x1164	0x0000	USER36
0x1166	0x0000	USER37
0x1168	0x0000	USER38
0x116A	0x0000	USER39
0x116C	0x0000	USER40
0x116E	0x0000	USER41
0x1170	0x0000	USER42
0x1172	0x0000	USER43
0x1174	0x0000	USER44
0x1176	0x0000	USER45
0x1178	0x0000	USER46
0x117A	0x0000	USER47
0x117C	0x0000	USER48
0x117E	0x0000	USER49
0x1180	0x0000	USER50
0x1182	0x0000	USER51
0x1184	0x0000	USER52
0x1186	0x0000	USER53
0x1188	0x0000	USER54
0x118A	0x0000	USER55
0x118C	0x0000	USER56
0x118E	0x0000	USER57
0x1190	0x0000	USER58
0x1192	0x0000	USER59
0x1194	0x0000	USER60
0x1196	0x0000	USER61
0x1198	0x0000	USER62
0x119A	0x0000	USER63

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	USERx															

USER : These registers can be used to program any customer specific data.
USER0, USER1, USER2, USER3 can be read out via MetaData1.
Typically these registers are used to store module identifiers like production batch no./date, …

15. MetaData

	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData1									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
0	DIAGNOSTICS [15:8]								0000	Diagnostics of the current phase	P
1	DIAGNOSTICS [7:0]								0000		
2	FIXED_VALUE								0000	FIXED_VALUE : 0x4D = "M"	C
3	FRAME_NUMBER [15:8]								0000	in Continuous Mode : FRAME_NUMBER increments every frame, starting from 0 in Triggered Multi Frame Mode : FRAME_NUMBER increments every frame, resets at new trigger	F
4	FRAME_NUMBER [7:0]								0000		
5	-	-	PHASE_NUMBER			-	-	-	0000	PHASE_NUMBER : Phase number from 0 to PHASE_COUNT	P
6	PIXEL1_X								0000	PIXEL1_X = column number, PIXEL1_Y = row number This pixel will be read out after a full array read out, the pixel value can be found in MetaData2	C
7	PIXEL1_Y								0000		
8	PIXEL2_X								0000	PIXEL2_X = column number, PIXEL2_Y = row number This pixel will be read out after a full array read out, the pixel value can be found in MetaData2	C
9	PIXEL2_Y								0000		
10	-	EN_ DELAY	PROG_DELAY					FRAME TABLE	0000	EN_DELAY : Disabled/enabled ADC delay lines PROG_DELAY : Settings of the ADC delay line FRAMETABLE : Selected FrameTable 1 or 2	F
11	-	EN_ TEST ADC	EN_ TEST ROW	-	EN_ METAD ATA2	EN_ METAD ATA1	-	-	0000	EN_TESTADC : Disabled/enabled ADC test mode EN_TESTROW : Disabled/enabled MLX75024 test rows EN_METADATA2 : Disabled/enabled Metadata2 EN_METADATA1 : Disabled/enabled Metadata1	F
12	FLIP_ MIRROR		QUIET_ DEFINE		PHASE_COUNT				0000	FLIR_MIRROR : - 0x00: no FLIP, no MIRROR - 0x01: Vertical FLIP - 0x10: Horizontal MIRROR - 0x11: FLIP & MIRROR QUIET_DEFINE : - 00 : QUIET is not used - 01 : QUIET is high in reset + integration phase - 10 : QUIET is high in readout phase - 11 : QUIET is high in reset + integration + readout phase PHASE_COUNT : Total numbers of phase frames to be captured	F
13	FRAME_IDLETIME [15:8]								0000	FRAME_IDLETIME : 32 bit value	F
14	FRAME_IDLETIME [7:0]								0000		
15	FRAME_IDLETIME [31:24]								0000		
16	FRAME_IDLETIME [23:16]								0000		

Table 16: MetaData1, part 1.

#	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData1									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
17	MOD_DUTY_CYCLE			-	PLL_RDIV			PLL_ NDIV [2]	0000	MOD_DUTY_CYLE : - 0x000 : 12.5 % - 0x001 : 25 % - 0x010 : 37.5 % - 0x011 : 50 % - 0x100 : 62.5 % - 0x101 : 75 % - 0x110 : 87.5 % PLL_RDIV : Parameter used to calculate FMOD More information can be found in section 18 PLL_NDIV [2] : Parameter used to calculate FMOD More information can be found in section 18	F
18	PLL_NDIV [1:0]		FSYNC	PIXCLK	HSYNC	VSYNC	TRIGGER		0000	PLL_NDIV [1:0] : Parameter used to calculate FMOD More information can be found in section 18 FSYNC : 0x0 (active high) or 0x1 (= active low) PIXCLK : 0x0 (active high) or 0x1 (= active low) HSYNC : 0x0 (active high) or 0x1 (= active low) VSYNC : 0x0 (active high) or 0x1 (= active low) TRIGGER : - 0x00: Continuous Mode - 0x01: Triggered Multi Frame Mode	F
19	FRAME_COUNT [15:8]								0000	FRAMECOUNT : Total number of frames to be captured in triggered multi-frame mode	F
20	FRAME_COUNT [7:0]								0000		
21	FRAME_ROI_START_Y								0000	ROI_START_Y : Y coordinate of ROI start position More information can be found in chapter 14.2.7	F
22	FRAME_ROI_START_X								0000	ROI_START_X : X coordinate of ROI start position More information can be found in chapter 14.2.7	F
23	FRAME_ROI_SIZE_Y								0000	ROI_SIZE_Y : Y size of ROI More information can be found in chapter 14.2.7	F
24	FRAME_ROI_SIZE_X								0000	ROI_SIZE_X : X size of ROI More information can be found in chapter 14.2.7	F
25	Tx_BxCol_LATCH								0000	Readout of Tx_BxCol_LATCH 8bit register value used in current frame	F
26	Tx_BxRow_LATCH								0000	Readout of Tx_BxRow_LATCH 8bit register value used in current frame	F
27	-	-	-	-	OUTPUT_MODE			EN_ DMIX STATIC	0000	OUTPUT_MODE : - 0x000 : Mode #0 : 11b (A-B)/4 + 1b - 0x001 : Mode #1 : 12b (A-B)/2 - 0x010 : Mode #2 : 11b (A+B)/4 + 1b - 0x011 : Mode #3 : 12b (A+B)/2 - 0x100 : Mode #4 : 12b A - 0x101 : Mode #5 : 12b B EN_DMIXSTATIC : (Value is only valid if DMIX_DISABLE = 1) - 0x0: Both DMIX pins are LOW during integration - 0x1: Both DMIX pins are HIGH during integration	P

Table 17: MetaData1, part 2.

	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData1									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
28	DMIX_ DISABLE	-	-	EN_ LIGHT	PHASE_SHIFT				0000	DMIX_DISABLE : - 0x0: DMIX pulses are enabled during integration time - 0x1: EN_DMIXSTATIC is enabled EN_LIGHT : - 0x0: LED pulses are disabled during integration time - 0x1: LED pulses are enabled during integration time PHASE_SHIFT : Shift between MOD and DMIX[0] (DMIX[1] is always 180° shifted compared to DMIX[0], except during reset phase) - 0x000: 0° - 0x001: 45° - 0x010: 90° - 0x011: 135° - 0x100: 180° - 0x101: 225° - 0x110: 270° - 0x111: 315°	P
29	PHASE_INTEGRATION [15:8]								0000	Integration Time (32-bit)	P
30	PHASE_INTEGRATION [7:0]								0000		
31	PHASE_INTEGRATION [31:24]								0000		
32	PHASE_INTEGRATION [23:16]								0000		
33	PHASE_PREHEAT [15:8]								0000	Number of LED pulses before sensor integration	P
34	PHASE_PREHEAT [7:0]								0000		
35	PHASE_PREMIX [15:8]								0000	Number of DMIX pulses before sensor integration	P
36	PHASE_PREMIX [7:0]								0000		
37	PHASE_IDLE [15:8]								0000	Phase idle time at the end of each phase read out	P
38	PHASE_IDLE [7:0]								0000		
39	PHASE_SETUP [15:8]								0000	Setup time before integration	P
40	PHASE_SETUP [7:0]								0000		
41	-	-	-	-	GPO [3:0]				0000	GPO[3:0] represents the current state of the output pins	P
42	LATCH_CFG			ADC_LATENCY					0000		F
43	CRC-8								0000	CRC-8 calculation to cover byte [0:42] of MetaData1	P

Table 18: MetaData1, part 3. The length of MetaData1 can be truncated depending on ROI settings.

	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData2									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
0	DIAGNOSTICS [15:8]								0000	Diagnostics of the CURRENT phase	P
1	DIAGNOSTICS [7:0]								0000		
2	-	-	-	NR_PIXELS_ABOVE [20:16]					0000	# ADC readings above the threshold defined in register Tx_UPPER_LIMIT, see chapter **14.2.5** for more information	P
3	NR_PIXELS_ABOVE [15:8]								0000		
4	NR_PIXELS_ABOVE [7:0]								0000		
5	-	-	-	NR_PIXELS_BELOW [20:16]					0000	# ADC readings above the threshold defined in register Tx_LOWER_LIMIT, see chapter **14.2.6** for more information	P
6	NR_PIXELS_BELOW [15:8]								0000		
7	NR_PIXELS_BELOW [7:0]								0000		
8	PIXEL1_CH0 [11:4]								0000	Returns the ADC values from PIXEL1 with coordinates defined in register 0x1006. See chapter 0 for more information. PIXEL1_CH0 : 12bit data from tap A PIXEL1_CH1 : 12bit data from tap B PIXEL1_CH2 : 12bit data from tap A PIXEL1_CH3 : 12bit data from tap B	P
9	PIXEL1_CH0 [3:0]				PIXEL1_CH1 [11:8]				0000		
10	PIXEL1_CH1 [7:0]								0000		
11	PIXEL1_CH2 [11:4]								0000		
12	PIXEL1_CH2 [3:0]				PIXEL1_CH3 [11:8]				0000		
13	PIXEL1_CH3 [7:0]								0000		
14	PIXEL2_CH0 [11:4]								0000	Returns the ADC values from PIXEL2 with coordinates defined in register 0x1008. See chapter 0 for more information. PIXEL2_CH0 : 12bit data from tap A PIXEL2_CH1 : 12bit data from tap B PIXEL2_CH2 : 12bit data from tap A PIXEL2_CH3 : 12bit data from tap B	P
15	PIXEL2_CH0 [3:0]				PIXEL2_CH1 [11:8]				0000		
16	PIXEL2_CH1 [7:0]								0000		
17	PIXEL2_CH2 [11:4]								0000		
18	PIXEL2_CH2 [3:0]				PIXEL2_CH3 [11:8]				0000		
19	PIXEL2_CH3 [7:0]								0000		
20	USER0 [15:8]								0000	Readout of USER_DEFINED0 16bit register value This can be used to program unique a device identifier	C
21	USER0 [7:0]								0000		
22	USER1 [15:8]								0000	Readout of USER_DEFINED0 16bit register value This can be used to program unique a device identifier	C
23	USER1 [7:0]								0000		
24	USER2 [15:8]								0000	Readout of USER_DEFINED0 16bit register value This can be used to program unique a device identifier	C
25	USER2 [7:0]								0000		
26	USER3 [15:8]								0000	Readout of USER_DEFINED0 16bit register value This can be used to program unique a device identifier	C
27	USER3 [7:0]								0000		
28	CRC-8								0000	CRC-8 calculation to cover byte [0:19] of MetaData2	P
29	DELAY_LINE_PIXEL8								0000	Values of the delay line sweep This feature can be used to optimize the ADC sampling point	P
30	DELAY_LINE_PIXEL9								0000		
31	DELAY_LINE_PIXEL10								0000		
32	DELAY_LINE_PIXEL11								0000		
33	DELAY_LINE_PIXEL12								0000		
34	DELAY_LINE_PIXEL13								0000		
35	DELAY_LINE_PIXEL14								0000		
36	DELAY_LINE_PIXEL15								0000		
37	DELAY_LINE_PIXEL16								0000		
38	DELAY_LINE_PIXEL17								0000		
39	DELAY_LINE_PIXEL18								0000		
40	DELAY_LINE_PIXEL19								0000		
41	DELAY_LINE_PIXEL20								0000		
42	DELAY_LINE_PIXEL21								0000		

Table 19: MetaData2, part 1.

#	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData2									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
43	DELAY_LINE_PIXEL22								0000	Values of the delay line sweep This feature can be used to optimize the ADC sampling point	P
44	DELAY_LINE_PIXEL23								0000		
45	DELAY_LINE_PIXEL24								0000		
46	DELAY_LINE_PIXEL25								0000		
47	DELAY_LINE_PIXEL26								0000		
48	DELAY_LINE_PIXEL27								0000		
49	DELAY_LINE_PIXEL28								0000		
50	DELAY_LINE_PIXEL29								0000		
51	DELAY_LINE_PIXEL30								0000		
52	DELAY_LINE_PIXEL31								0000		
53	DELAY_LINE_PIXEL32								0000		
54	DELAY_LINE_PIXEL33								0000		
55	DELAY_LINE_PIXEL34								0000		
56	DELAY_LINE_PIXEL35								0000		
57	DELAY_LINE_PIXEL36								0000		
58	DELAY_LINE_PIXEL37								0000		
59	DELAY_LINE_PIXEL38								0000		
60	DELAY_LINE_PIXEL39								0000		
61	DELAY_LINE_PIXEL40								0000		
62	DELAY_LINE_PIXEL41								0000		
63	DELAY_LINE_PIXEL42								0000		
64	DELAY_LINE_PIXEL43								0000		
65	DELAY_LINE_PIXEL44								0000		
66	DELAY_LINE_PIXEL45								0000		
67	DELAY_LINE_PIXEL46								0000		
68	DELAY_LINE_PIXEL47								0000		
69	DELAY_LINE_PIXEL48								0000		
70	DELAY_LINE_PIXEL49								0000		
71	DELAY_LINE_PIXEL50								0000		
72	DELAY_LINE_PIXEL51								0000		
73	DELAY_LINE_PIXEL52								0000		
74	DELAY_LINE_PIXEL53								0000		
75	DELAY_LINE_PIXEL54								0000		
76	DELAY_LINE_PIXEL55								0000		
77	DELAY_LINE_PIXEL56								0000		
78	DELAY_LINE_PIXEL57								0000		
79	DELAY_LINE_PIXEL58								0000		
80	DELAY_LINE_PIXEL59								0000		
81	DELAY_LINE_PIXEL60								0000		
82	DELAY_LINE_PIXEL61								0000		
83	DELAY_LINE_PIXEL62								0000		
84	DELAY_LINE_PIXEL63								0000		
85	DELAY_LINE_PIXEL64								0000		

Table 20: MetaData2, part 2.

	PIXD [11]	PIXD [10]	PIXD [9]	PIXD [8]	PIXD [7]	PIXD [6]	PIXD [5]	PIXD [4]	PIXD [3:0]	Description	
#	MetaData2									Value can change on each phase frame = Value is constant = Value can change on each frame =	P C F
86	DELAY_LINE_PIXEL65								0000	Values of the delay line sweep This feature can be used to optimize the ADC sampling point	P
87	DELAY_LINE_PIXEL66								0000		
88	DELAY_LINE_PIXEL67								0000		
89	DELAY_LINE_PIXEL68								0000		
90	DELAY_LINE_PIXEL69								0000		
91	DELAY_LINE_PIXEL70								0000		
92	DELAY_LINE_PIXEL71								0000		

Table 21: MetaData2, part 3.

16. Diagnostics

On top of the Metadata lines there's one extra register that holds information about the device status.

Name : **DIAGNOSTICS**

Address : 0x0002

Default Value : 0x0005

Bit	15	14	13	12	11	10	9	8
	ROI_ERROR	**SEC_ERROR**	**DED_ERROR**	**SEC_LATCH**	**DED_LATCH**	-	-	-

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	**3V3_READY**	-	**PLL_LOCK**

ROI_ERROR : This bit is set high when an incorrect ROI is set via registers *Frame : Tx_ROI_START & Tx*_ROI_SIZE
When a ROI error occurs, the video output stops. It can only be corrected by setting a valid ROI.

SEC_ERROR : Selfclearing bit that indicates single error correction from NVRAM.
The bit gets cleared as soon as the information is shared via the MetaData.

DED_ERROR : Selfclearing bit that indicate when a double error is detected inside the NVRAM.
The bit gets cleared as soon as the information is shared via the MetaData.

SEC_LATCH : This bit is set high as soon as a SEC occurred, and will stay high until it get's cleared.
This bit needs to be actively cleared by the user by writing register 0x0000 with value 0x0004.

DED_LATCH : This bit is set high as soon as a DED occurred, and will stay high until it get's cleared.
This bit needs to be actively cleared by the user by writing register 0x0000 with value 0x0008.

3V3_READY : This bit is set high when the VDDD_3V3 voltage level is higher than 2.8V.

PLL_LOCK : This bit is set high when the PLL is locked at the correct modulation frequency.

17. Sleep Mode(s)

MLX75123 features 1 register that can be used to enable/disable some internal blocks to reduce the power consumption. In normal operation all blocks are enabled. The I^2C communication is always active. This register is not part of the NVRAM and it's not possible to save its value with I2C_SAVEREGMAP as explained in section 13.5.

Name : **BLOCK_DISABLE**

Address : 0x0004

Default Value : 0x0000

Bit	15	14	13	12	11	10	9	8
	-	-	-	-	-	-	-	-

Bit	7	6	5	4	3	2	1	0
	DIS_ADC_REF	**DIS_ADC_BG**	-	-	**DIS_VIDEO_BUFFERS**	**DIS_75024_BUFFERS**	**DIS_PLL**	**DIS_BG**

DIS_ADC_REF : Enable/disable the input test references for the ADC
DIS_ADC_BG : Enable/disable the internal ADC band gap (incl. ADC reference voltages)
DIS_VIDEO_BUFFERS : Enable/disable the video output buffers
DIS_75024_BUFFERS : Enable/disable the MLX75024 control buffers
DIS_PLL : Enable/disable the *FMOD Generator*
DIS_BG : Enable/disable the internal bandgap block

18. FMOD Generator

MLX75123 features a built in timing generator. This block generates all the timings, and phase shifts, for the sensor and illumination. This is often referred to as the modulation frequency. The output frequency changes in function on the input clock frequency, RDIV & NDIV values.
The output modulation frequency is given by $\frac{CLK_{IN}}{2} \cdot \frac{NDIV}{RDIV}$ (in MHz) limited between 12- 40 MHz.

This frequency can change every frame and can be used to minimize interference between one or more TOF cameras operating in the same environment.

Dividing the value of the input clock by 8 MHz is a good way to determine an RDIV value which will guarantee the stability of the modulation frequency. NDIV can then be selected to set the modulation frequency between 12 and 40 MHz.

Examples :

CLK_{IN} = 80MHz ⇒ RDIV = CLK_{IN} / 8 MHz = 10

NDIV	3	4	5	6	7	8	9	10
Fmod (MHz)	12	16	20	24	28	32	36	40

CLK_{IN} = 62MHz ⇒ RDIV = CLK_{IN} / 8 MHz = 7.75 ≈ 8

NDIV	3	4	5	6	7	8	9	10
Fmod (MHz)	[1]	15.5	19.38	23.25	27.13	31	34.88	38.75

CLK_{IN} = 42MHz ⇒ RDIV = CLK_{IN} / 8 MHz = 5.25 ≈ 5

NDIV	3	4	5	6	7	8	9	10
Fmod (MHz)	12.6	16.8	21	25.2	29.4	33.6	37.8	[1]

CLK_{IN} = 40MHz ⇒ RDIV = CLK_{IN} / 8 MHz = 5

NDIV	3	4	5	6	7	8	9	10
Fmod (MHz)	12	16	20	24	28	32	36	40

Note [1] : Not a valid setting, the modulation frequency should be in range 12-40MHz.

The corresponding RDIV & NDIV values to be written into the registers from section 14.2.3 can be found here :

RDIV or NDIV value	Binary
3	000
4	001
5	010
6	011
7	100
8	101
9	110
10	111

19. Package Dimensions

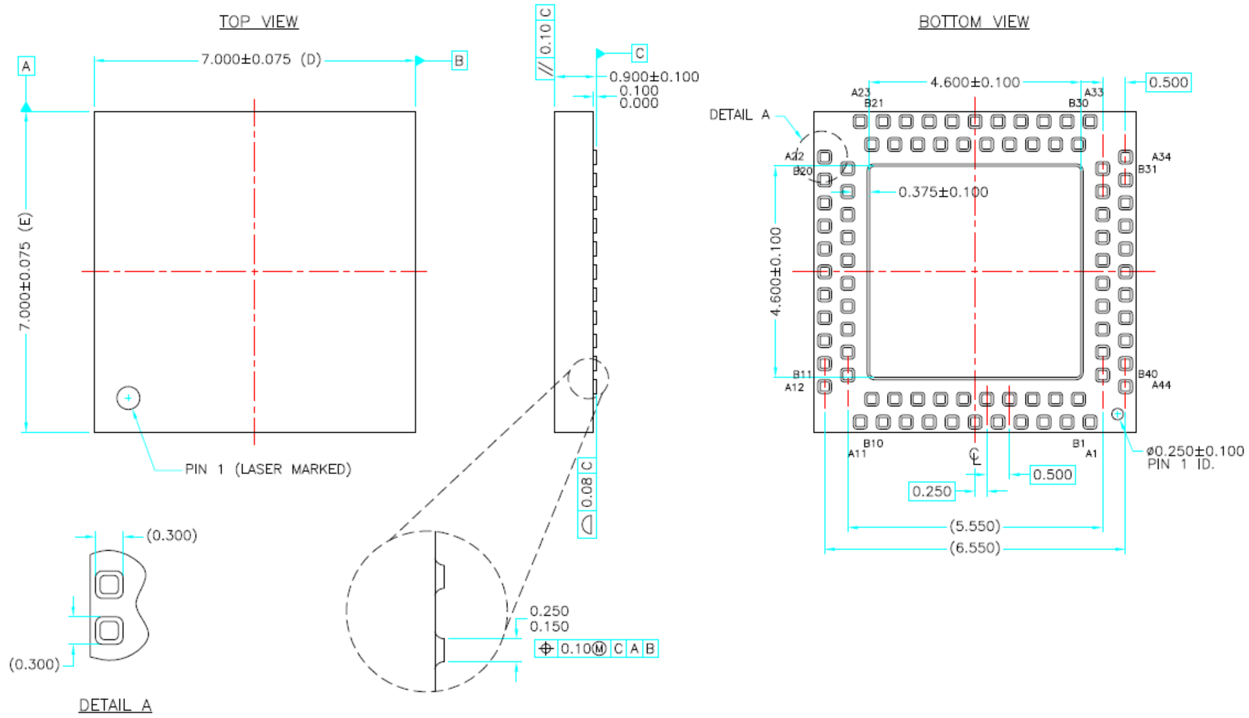


Figure 9 : Package dimensions

20. Layout & Solder Recommendations

20.1. PCB Footprint Design

The design of a printed circuit board for MLX75123 requires special attention to assure a good solder quality during PCB assembly. This chapter describes best practises based on Melexis experiences.

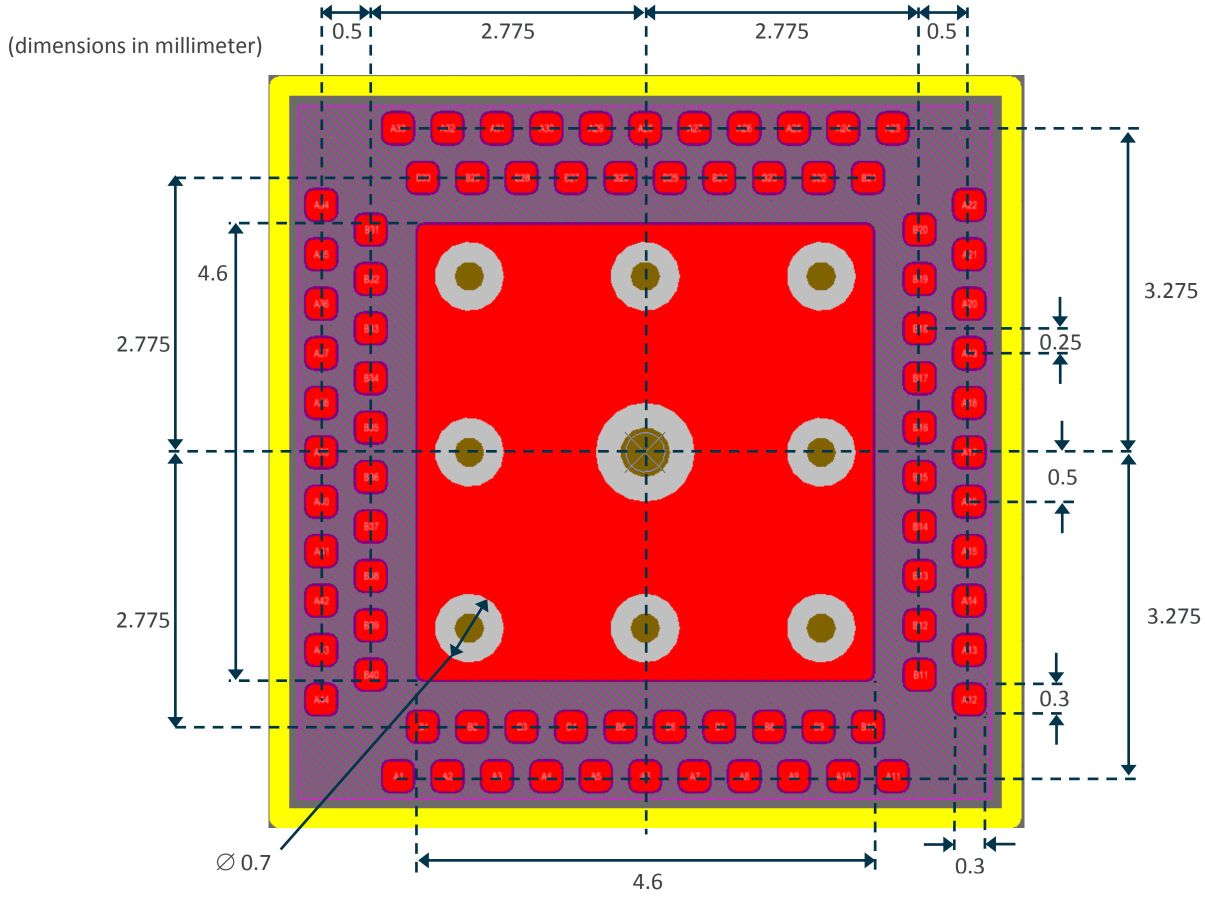
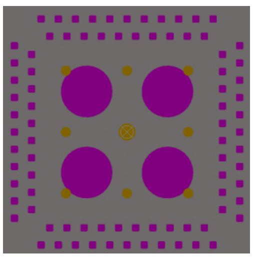


Figure 10 : PCB footprint recommendation (top layer)

Pad size = 0.3 x 0.3 mm (rounded rectangle)
Pad solder mask expansion = 0.35 x 0.35 mm (= NSMD pads)
Pad solder paste = 0.27 x 0.27 mm (rounded rectangle)

The exposed thermal pad has to be connected to a big internal plane (like GND) for good heat dissipation.
Exposed pad size = 4.6 x 4.6 mm (rounded rectangle)
Exposed pad solder paste = 4x 1.5mm dots
Exposed pad via size(s) = 1mm with 0.5mm hole (central via) & 0.7mm with 0.3mm hole (outer eight vias)
Tented or plugged vias are not allowed inside the thermal pad.

Applying more paste to the full thermal pad could cause device tilting because of the excessive amount of solder paste. We suggest applying merely four individual dots of paste solder quality issues. This is shown in the figure on the right, which represents the top paste layer.



Connecting the inner row of pads can be done with small through-hole vias (0.3mm size with 0.15mm hole). We recommend placing them next to the pads without violating other design rules like shown in Figure 11.

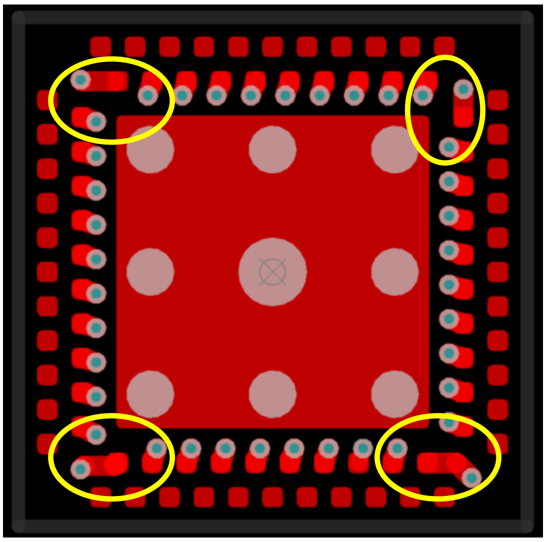


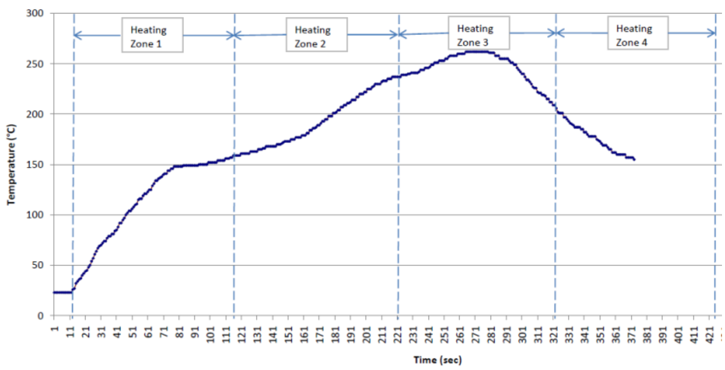
Figure 11 : Suggested through hole via placement of the inner pads

The vias in the yellow marked areas are placed to allow a wide connection of the inner layers for good heat distribution. If your PCB manufacturer does not support small through-hole vias or there's a chance of wicking, these vias have to be replaced by *via in pad* (= active pads) or plugged via technology.

For PCB assembly we recommend using a laser cut nickel plated stencil with a thickness of 100µm. It is mandatory to have smooth stencil aperture walls to improve the solder paste distribution within the cavities and to increase the paste release onto the pads. Using a type 5 solder paste (with a small particle size) further improves this behaviour. (for example Alpha® OM-353 or CVP-390)

20.2. Solder Profile

We recommend a vapor phase soldering process (with linear temperature profile and a melting point of 218degC) for increased solder quality or reflow soldering according to JEDEC-J-STD-020D.



Heating Zone	Temperature (minimum)	Temperature (maximum)
1	350	350
2	240	240
3	350	350
4	340	340

Figure 12 : Reflow solder profile

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